International
IOR Rectifier

APPLICATION NOTE

Application Note AN-0994

Maximizing the Effectiveness of your SMD Assemblies

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Introduction

This application note describes the measurement of thermal resistance for International Rectifier's surface-mounted devices (SMDs). It explains how packages were mounted and the techniques used in heat sinking and testing. It applies only to SMDs, not to through-hole devices such as TO-220, TO-247 and Fulpak.

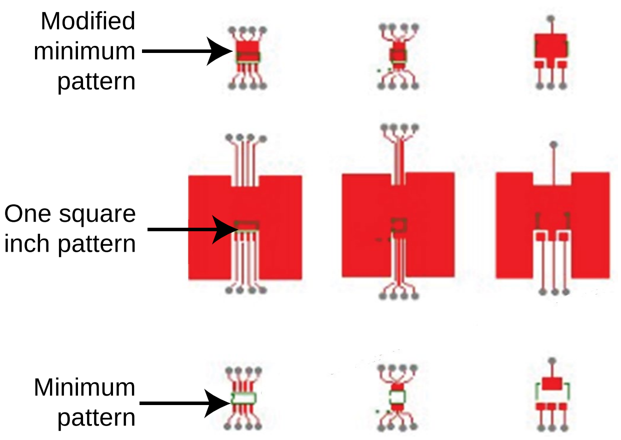
Method

Standard printed circuit boards were developed, to which the devices under test were solder-mounted for measuring thermal resistance. The boards measured 4.75 inches by 4.5 inches, and were made of FR-4 backed with 2 oz copper.

Note: A specific thermal test board was used for DirectFET because of this package's unique connection design.

Three metal patterns were tested (Figure 1):

- one square inch of copper
- modified minimum: copper covered only the space occupied by the device and lead pads
- minimum pattern: copper covered only the space occupied by the lead pads.



The device was placed in the middle of the pads shown.

Figure 1 Device placement used in testing

In accordance with industry practice, thermal resistance was measured by first performing a reference temperature estimate. A temperature sensitive electrical parameter (TSEP) such as V_{sd} was measured and compared with a calibration value to determine the junction temperature (T_j). A heating pulse of known power was then applied. This was followed by a second TSEP measurement, which was compared with a calibration table to estimate T_j. The temperature rise due to the heating pulse was calculated using this equation:

$$\Delta T = R_{TH} \text{ X } P_D$$

where:

ΔT = Temperature difference (C) between junction temperature and reference temperature (T_J - T_{Ref}); T_{Ref} is the ambient, package case or package lead temperature

R_{TH} = Thermal resistance (C/W) between junction and reference point (package case or package lead)

P_D = Power dissipated (W)

We can calculate the thermal resistance by inserting measured values of temperature rise and power. Measurements were taken from representative samples of all the packages listed in Table 1.

Thermal characteristics of SMDs

Table 1 shows typical and maximum $R_{th\,(JA)}$ and typical $R_{th\,(JL)}$ values of International Rectifier's SMD packages mounted using the metal patterns shown in Figure 1. For $R_{th\,(JC)}$ values, refer to the appropriate data sheet.

Table 1 Typical and maximum thermal resistance

Package type	**Thermal resistance**						
	One square inch		**Modified minimum**		**Minimum**		**All**
	Typ $R_{th(JA)}$	**Max $R_{th(JA)}$**	**Typ $R_{th(JA)}$**	**Max $R_{th(JA)}$**	**Typ $R_{th(JA)}$**	**Max $R_{th(JA)}$**	**Typ $R_{th(JL)}$**
D-Pak	20.2	26.3	42.0	54.6	59.5	77.3	2.0
D2-Pak	18.0	23.3	33.6	43.7	36.7	47.7	1.6
SO-8	33.5	50.0	66.3	86.2	70.6	91.8	10.6
SO-8 (dual)	54.5	62.5	73.1	95.1	94.7	123.1	28.7
SOT-223	27.2	60.0	49.0	63.7	66.1	86.0	4.9
TSOP6 (dual)	73.4	125.0	134.7	175.1	170.7	222.0	35.5
TSOP6 (single)	47.3	62.5	112.0	145.6	118.5	154.0	17.0
TSSOP8	60.9	83.0	106.4	138.3	117.0	152.1	35.5
u-3	169.2	230.0	237.1	308.2	263.6	342.6	139.3
u-6	47.1	75.0	112.5	146.3	124.9	162.4	14.7
u-8	39.9	70.0	102.4	133.2	126.1	163.9	17.0
DirectFET	A specific thermal test board was used because of DirectFET's unique connections. This table is split to reflect this difference but, to improve readability, the results are shown together on the following graphs.						
Small can	32.1	60.0	49.2	64.0	68.1	88.5	NA
Medium can	*32.3*	60.0	55.6	72.3	62.2	80.9	NA

Notes

1. Three pieces of each package type were in the sample.
2. $R_{th\,(JL)}$ (typical) and $R_{th\,(JL)}$ (one square inch) were measured at the same time (R_{th} reference to drain lead).
3. Measurement conditions were as described in Method.
4. The board contributes greatly to the total thermal resistance. If its material properties or dimensions vary significantly from those used by International Rectifier, actual thermal resistance may vary.

Using the Max $_{Rth\ (JA)}$ values from Table 1, Figures 2 to 4 plot power dissipation against ambient temperature for each metal pattern.

Larger packages with exposed heat sinks (such as D2-Pak, D-Pak and SOT-223) usually have the highest power dissipation capabilities.

Increasing the area of the metal pattern reduces the thermal resistance. The measurements taken using the three different pattern areas reflect this, with the one square inch pattern giving the lowest resistance.

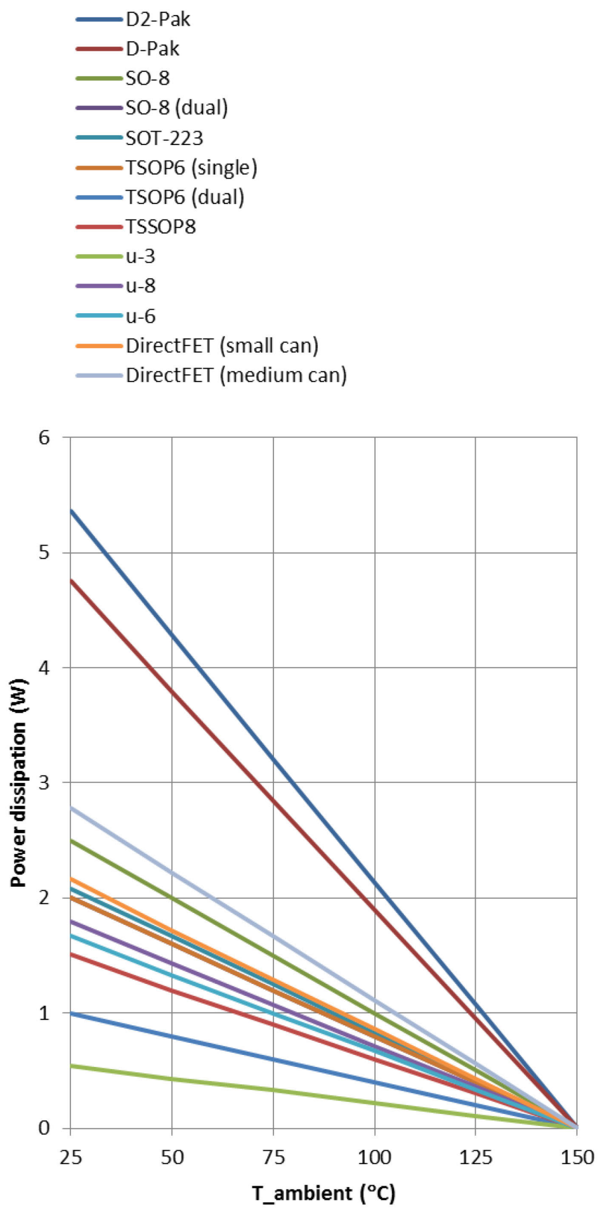


Figure 2 Ambient power dissipation – one square inch

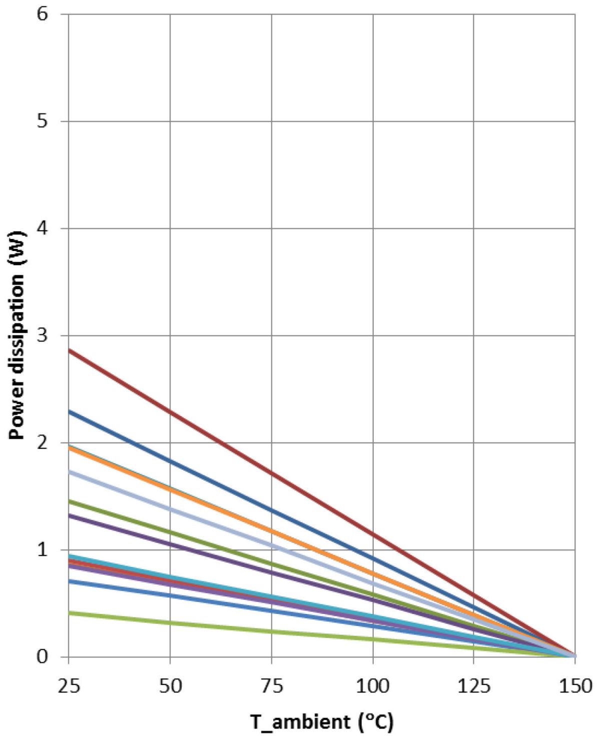


Figure 3 Ambient power dissipation – modified minimum

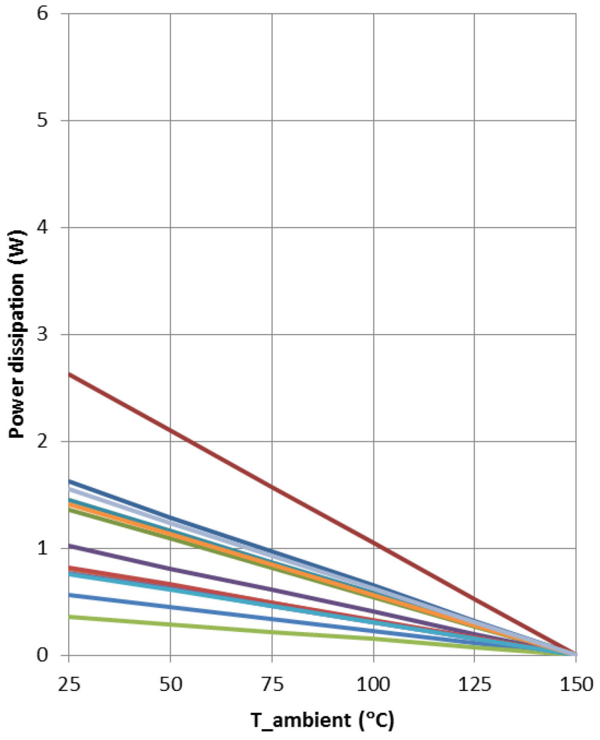


Figure 4 Ambient power dissipation – minimum

Adhesives

As the connections on an SMD do not pass through the board on which it is mounted, such devices rely solely on the strength of the solder joint for mechanical as well as electrical connection.

Many assemblies require devices to be mounted on both sides of the board. The reflow process is typically done only once, with both sides of the board pasted at the same time. Devices are placed on one side of the board, using an adhesive to hold them in place, and then the board is turned through 180 degrees for devices to be placed on the other side. The board is subjected to a thermal process to melt the solder paste. When the devices have been soldered to the board, the adhesive serves no further purpose.

The adhesive used must secure the devices to prevent movement during handling and soldering. However, it must be possible to break the bond with minimal disturbance to the populated board so that incorrectly positioned devices can be moved before soldering. Adhesion must be maintained during preheating and the adhesive should not interfere with solder flow during the reflow or wave soldering process.

Typical adhesives of this type are made from non-activated resins (R), which can be used in a forming gas atmosphere to reduce oxides. Some are mildly activated resin (RMA), which can be used in normal factory environments. The activators in these resins dissolve small amounts of oxidation from solderable surfaces and solder particles in the paste.

Solder pastes

A wide range of solder pastes is available for surface mounting applications. Typically, they are composed of a homogeneous mixture of pre-alloyed solder powder with a specific grain size. Fluxes are included, as they are essential to the surface mounting process.

In today's densely populated assemblies, the leads on SMDs are significantly closer together. Spacing of less than 0.4mm is common and it can cause problems such as solder bridging, insufficient solder on leads and inaccurate device placement. The stencil's thickness, dimensions and registration accuracy and the solder paste's composition and particle size are all critical in soldering these assemblies successfully.

Given these complexities, advising on the choice of solder paste is beyond the scope of this application note. Customers should contact their solder paste vendor and board fabricator for recommendations specific to their application.

Reflow profiles

A major problem associated with mounting SMDs, especially those with mismatched internal expansion coefficients, is the thermal shock of the soldering process. The advent of lead-free assemblies has driven the requirement to develop and implement new handling techniques for SMDs. Lead-free solders typically have higher melting points than traditional lead-based solders. Where lead-based assemblies could be mounted at peak reflow temperatures in the range 220°C to 245°C, lead-free assemblies require temperatures in the range 245°C to 260°C. Higher peak temperatures require careful control of the reflow environment to prevent over-temperature conditions that can severely degrade the reliability of SMDs. Caution must be taken when choosing a reflow profile to optimize the thermal stresses that are applied to the assemblies, whether lead-based or lead-free. Conversely, under-temperature conditions can result in failed mechanical attachment.

A carefully controlled pre-heat and post-cooling sequence is necessary. Properly controlling the pre-heat cycle removes any volatile components of the solder paste, such as alcohol or water, by evaporation before the solder fusing cycle starts. This reduces the chances of forming voids or solder balls. Table 2 shows critical parameters of the reflow profile.

Table 2 Critical parameters by solder paste and device volume

Profile feature	**Lead-free[3]**	**Lead-based**	
	All sizes	**Large body[1]**	**Small body[2]**
Average ramp-up rate, T_L to T_p (°C/sec max)	3	3	3
Preheat			
Temp min, Ts_{min} (°C)	150	100	100
Temp max, Ts_{max} (°C)	200	150	150
Time, Ts_{min} to Ts_{max} (sec)	60–180	60–120	60–120
Max ramp-up rate, Ts_{max} to T_L (°C/sec)	3	—	—
Time maintained above:			
Temp, T_L (°C)	217	183	183
Time, t_L (sec)	60–150	60–150	60–150
Peak temperature, T_p (°C)	260 +0/-5[4]	225 +0/-5	240 +0/-5
Time within 5°C of actual peak temperature, t_p (sec)	10–30	10–30	10–30
Max ramp-down rate (°C/sec)	6	6	6
Max time 25°C to peak temperature (min)	8	6	6

Notes:

1. Large Body: TO-220, D2pak and larger (package thickness ≥2.5 mm or package volume ≥ 350 mm^3)
2. Small Body: Dpak, Ipak and smaller (package thickness < 2.5 mm or package volume < 350 mm^3)
3. Lead-free devices have the suffix PbF in the part number. To check if a device is lead-free, contact the sales representative or the factory.
4. The recommended peak reflow temperature for some large-body packages (such as PLCC-44 / MQFP64) is 250°C +0/-5°C. To check the peak temperature for a device, contact the sales representative.

This thermal conditioning can be applied in several ways, including infrared/convection reflow, vapor phase reflow and wave soldering. Figures 5 and 6 show recommended profiles for infrared/convection reflow and wave soldering. Table 3 and Table 4 give recommendations for specific SMDs.

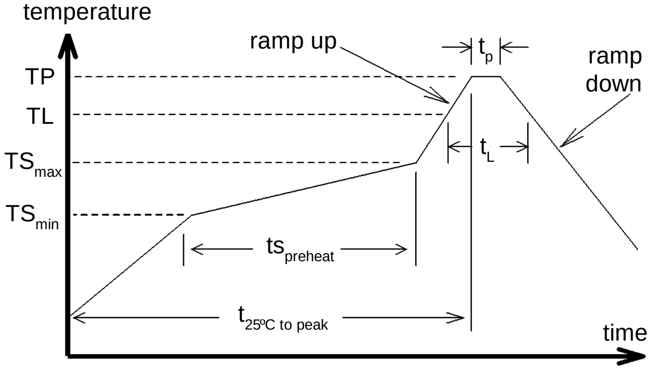
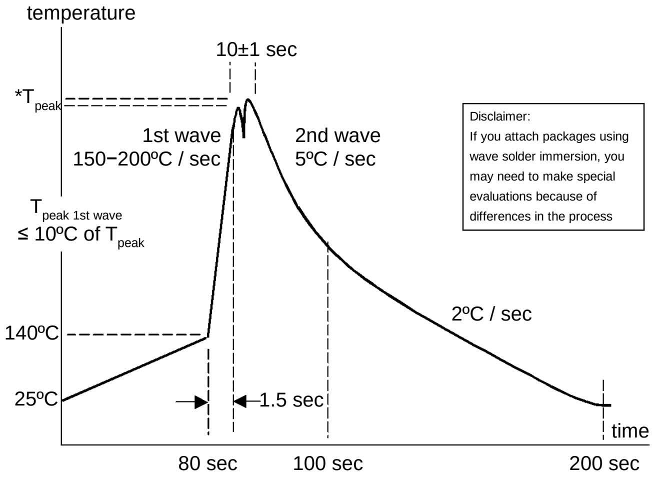


Figure 5 Infrared / convection reflow profile



Disclaimer:
If you attach packages using wave solder immersion, you may need to make special evaluations because of differences in the process

Figure 6 Wave soldering profile

Table 3 Infrared/convection reflow recommendations

Package		**Reflow temp (°C)**	
Name	**Size**	**Lead-free**	**Lead-based**
D2PAK	L	250	225
D-61-8	L	250	225
D-PAK	S	260	245
Micro-3/SOT 23	S	260	245
Micro-6/SOT 6	S	260	245
Micro-8	S	260	245
MLP-20 4x4	S	260	245
MLP-28 5x5	S	260	245
MLP-48 7x7	S	260	245
MLP-6 3x3	S	260	245
MQFP64	L	250	225
PDIP-14	L	250	225
PDIP-16	L	250	225
PDIP-20	L	250	225
PDIP-28	L	250	225
PDIP-8	L	250	225
PLCC44	L	250	225
SMA	S	260	245
SMB	S	260	245
SMC	S	260	245
SOICN-14	S	260	245
SOICN-16	S	260	245
SOICN-8	S	260	245
SOICW-16	S	260	245
SOICW-20	S	260	245
SOICW-28	S	260	245
SOT223	S	260	245
TO-220	L	250	225
TO-247	L	250	225
TO-262	L	250	225
TSSOP20	S	260	245
TSSOP24	S	260	245
TSSOP8	S	260	245

Thickness > 2.5 mm or volume > 350 mm^2, reflow 250+0/-5°C (Pb-free), 225+0/-5°C (SnPb eutectic)

Thickness < 2.5 mm and volume < 350 mm^2, reflow 260+0/-5°C (Pb-free), 240+0/-5°C (SnPb eutectic)

Table 4 Wave solder recommendations

Package	**Reflow temp (°C)**	**Remarks**
D2PAK	225	Not lead-free
D2PAK	260	Lead-free
DPAK	260	Lead-free*
D-PAK	235	Not lead-free*
SOICN-14L	240	Not lead-free
SOICN-14L	260	Lead-free
SOICN-16L	260	Lead-free
SOICN-28L	240	Not lead-free
SOICN-8L	240	Not lead-free
SOICN-8L	260	Lead-free
SOICW-16L	240	Not lead-free
SOICW-16L	260	Lead-free

* Contact manufacturer for more information

Rework

When replacing an SMD that has been soldered onto a substrate, the main problem is applying enough heat to melt all the connections on the device that is being rep laced without overheating adjacent devices. This is achieved by using a soldering iron with a specially shaped tip and, because of the diversity of SMD package styles, a corresponding variety of tips is required. The tip must have a gripping function so that, when the solder is reflowed, the device can be extracted from the board.

When the replacement SMD is mounted, the tool must perform the reverse procedure. Flux must be applied to the new device before localized reflow.