# Control Method for a Reverse Conducting IGBT

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## Abstract

Combining IGBT and diode functionality into one piece of silicon, a reverse conducting IGBT (RC-IGBT) is created. This measure allows equipping a standard IGBT/diode-module with only one piece of chip by replacing IGBT and diode with the new RC-IGBT. The result is an enhanced current carrying capability without increasing the foot print of the module. As a result of the integration, the diode´s electrical performance can be influenced by the control state of the IGBT gate. In order to control the RC-IGBT system in a loss optimized manner, special control aspects need to be considered.

## 1. Device Introduction

Reverse conducting IGBT´s can be built by partially interrupting the p-doped collector area by n-doped regions. Doing so, on the one hand, the diode functionality is given, on the other hand, there is enough area for the IGBT to inject minority carriers into the drift region for low forward voltage $V_{ce(sat)}$.

With such an approach, diode functionality becomes dependent from the state of the gate control (Fig. 1). Such a device, designed for hard switching applications, is called Reverse Conducting IGBT with Diode Control (RCDC-IGBT) [1].

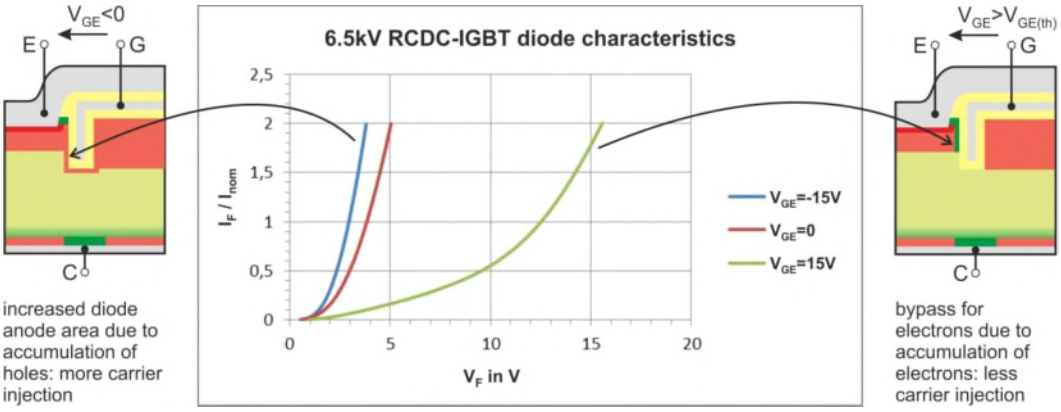


Fig. 1. 6.5kV RCDC-IGBT diode characteristics, $T_j$=125°C, diode performance as a function of gate voltage, in cross section: red color is p-type-doped, green color is n-type-doped

## 2. Loss Optimal RCDC-IGBT Performance

From the device introduction it can be concluded, that the RCDC-IGBT gate state has a major impact on the diode´s forward characteristics. From the static loss perspective, in diode conduction mode the gate needs to be turned off. The lowest $V_F$ can be achieved if $v_{GE}$=-15V, a little higher value is reached at $v_{GE}$=0. Since $V_F$ corresponds to the carrier density inside the chip, in terms of lowest dynamic losses and thus lowest $Q_{rr}$, $V_F$ should be chosen high.

The decision, which gate states to drive in diode conduction mode, depends on the pulse frequency of the application and the ability to desaturate the diode prior to it´s turn off.

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# 3. Special Gate Drive Aspects

A gate driver for low loss RCDC-IGBT operation needs to be able to

- detect the diode conduction mode and prevent the turn-on of the RCDC-IGBT gate
- desaturate the RCDC-IGBT-diode by means of driving $v_{GE}$=15V prior to diode´s turn off
- drive $v_{GE}$=0 in diode conduction mode in case of typical 6.5kV inverter pulse frequency and limited diode desaturation time
- detect a load current zero crossing in diode mode and turn on the RCDC-IGBT gate for smooth current transition from diode to IGBT of the same switch
- detect the load current zero crossing in IGBT mode and turn off the RCDC-IGBT gate for low loss diode operation

## 3.1. Detect the Diode Conduction Mode

In a classical inverter a forward conducting IGBT device is turned off in the beginning of the interlock time period. For the opposite diode this means that first the blocking voltage decreases and then the current starts to rise. After the interlock time period is over, the diode´s antiparallel IGBT gate is turned on. In RCDC-IGBT case, the turn on of the conducting diode´s antiparallel IGBT needs to be prevented by the gate driver logic.

It´s recommend to monitor $v_{CE}$ of a switch before executing the turn on command from the control side. In the mentioned situation, the voltage across the diode´s switch is low already before the interlock time is over. This is a clear indicator that the diode is conducting. In Fig. 2 a) the flow chart of the RCDC-IGBT control scheme is depicted. Figure 2b) gives an example how the system would act.

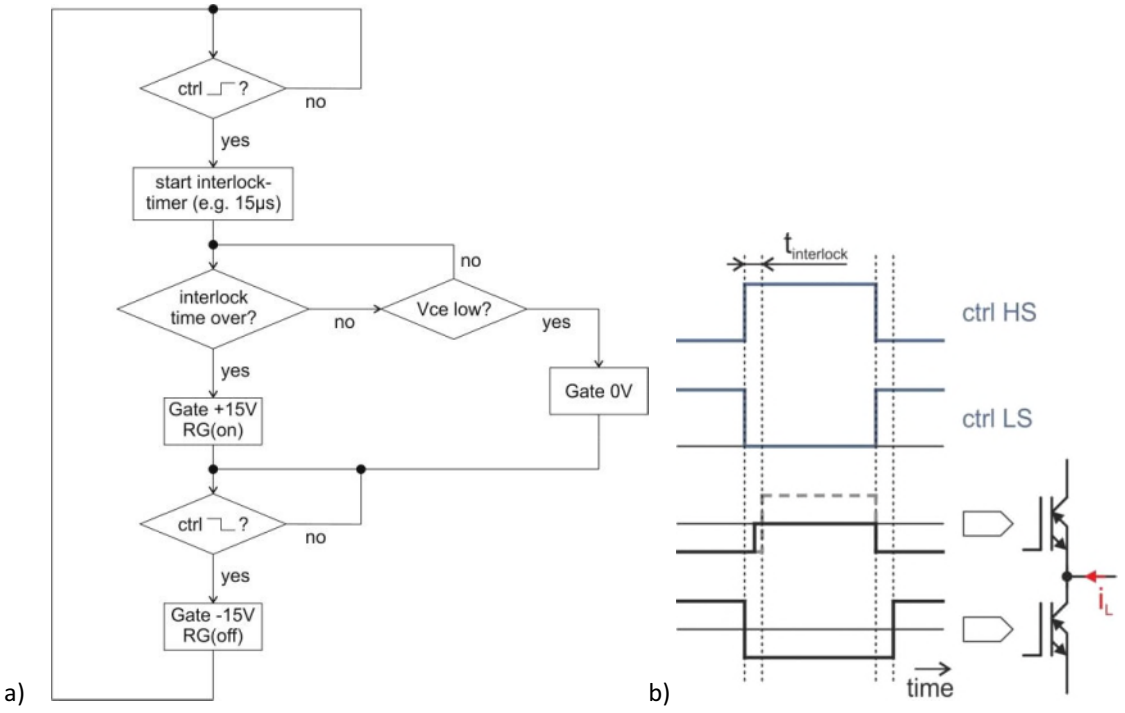


Fig. 2. a) Flowchart of the RCDC gate driver control scheme to monitor the diode conduction mode, if detected, keep the antiparallel IGBT gate in off state, here at 0V; b) RCDC-IGBT gate driver input signals (ctrl) from inverter control stage and RCDC-IGBT gate driver output voltage, interlock time is calculated on each driver stage individually, dashed line: standard inverter driver output

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For diode desaturation purposes the interlock time is calculated on each gate driver individually. As a consequence, the gate driver input signals “ctrl HS” (HS: highside) and “ctrl LS” (LS: lowside) will change at the same time. Falling edges of the ctrl-signal are executed directly, turning off the LS-IGBTs gate immediately. A normal IGBT turn-off happens, the voltage across the HS-switch decreases. A high voltage detector checks weather the HS switch $v_{CE}$ becomes smaller than a defined threshold displayed as “Vce low” in Fig. 2a). In this case, the HS-switch will go into diode conduction mode and the gate is switched from $v_{GE}$=-15V to 0. This transition is executed as soon as the detectors output “Vce low” changes.

The high voltage detector is a simple frequency-compensated voltage divider. In high voltage applications, typically this circuit is already present in the gate driver stage for desaturation detection purposes and adds no additional parts on the driver´s bill of material (BOM).

## 3.2. Diode Desaturation

As explained, it is worth to detect the diode conduction state and keeping the corresponding switch´s gate in the off-state. With this measure a high carrier density inside the device is obtained ensuring low $V_F$-values. From the dynamic loss perspective this device condition is not desired as high carrier density causes high $Q_{rr}$ and hence high IGBT turn on and diode turn off losses.

Turning on the diode´s switch gate for a certain duration before the diode is turned off, the operation point is shifted from a low $V_F$ to a high $V_F$ output curve (Fig. 1). The diode carrier concentration is reduced with a strong effect on the dynamic losses. Typical desaturation times for a 6.5kV RCDC-device lie in between 20 and 100 µs.

In Fig. 3 this effect is demonstrated. From the middle to the right picture the desaturation duration $t_{desat}$ changes from 20 to 100 µs. Accordingly, the reverse recovery peak current does not change that much, but the tail charge is reduced and thus – combined with high voltage $v_{CE}$ in that phase – dynamic losses are significantly lower.

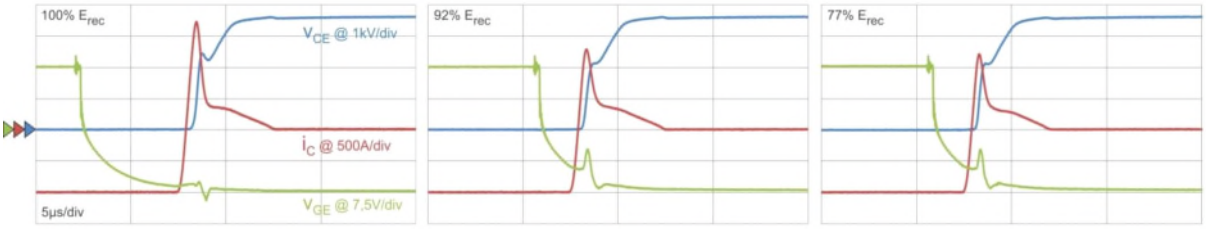


Fig. 3. 6.5kV, 1kA RCDC module diode turn off behavior at $T_j$=125°C, DC-link voltage $V_{CC}$=3600V, load current $i_L$=1000A, prior to desaturation at $v_{GE}$=15V diode were driven at $v_{GE}$=0, left: $t_{desat}$=20µs, $t_{lock}$=4µs; middle: $t_{desat}$=20µs, $t_{lock}$=0.5µs; right: $t_{desat}$=100µs, $t_{lock}$=0.5µs ($t_{lock}$: see Fig. 4)

For the practical implementation, the driver needs to accurately predict the point in time at which the diode turns off. This event corresponds to the opposite IGBT´s turn-on, which – based on the signal definitions – is executed after the IGBT switch´s ctrl-signal changes from low to high and the interlock time $t_{interlock}$ is over.

In Fig. 4 this regime is illustrated. Like shown in Fig. 2, the HS-switch diode conduction state was detected and the gate was switched to $v_{GE}$=0. Now, the HS and LS gate input signal change synchronously. The LS gate driver starts to count the interlock time. If the interlock time is over, it turns on its IGBT gate. The diodes switch gate driver has now time to place the diode´s desaturation pulse by applying $v_{GE}$=15V. Per definition, no active switching in the halfbridge takes place until the interlock timer is over. The diode´s switch gate driver stays at $v_{GE}$=15V for the desaturation time $t_{desat}$. The duration of $t_{desat}$ is shorter than $t_{interlock}$ since a remaining locking time $t_{lock}$ must be applied. The locking time should be kept rather small since otherwise the diode starts to saturate again and the effect of the desaturation becomes less. A typical value $t_{lock}$ for a 6.5kV RCDC-device is 500ns.

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The influence of $t_{lock}$ on the dynamic diode losses is shown in Fig. 3. From the left to the middle picture the locking time changes from 4 to 0.5 µs. In both cases the desaturation time $t_{desat}$ is 20µs. For $t_{lock}$=4µs the reverse recovery peak current is much higher compared to the curve for $t_{lock}$=0.5µs. Applying a small locking time, a loss reduction up to 8% can be achieved.

More details about the diode controllability of a reverse conducting high voltage IGBT are given in [2] and [3].

With this approach, the duration for diode desaturation corresponds to the maximum interlock time tolerated by the application. Long interlock time ensures best device performance but decreases the system dynamic. To utilze the interlock time for best desaturation result, it´s recommended to apply smallest time constants for turning the desaturation-pulse on and off. This is achieved by introducing a very small gate resistor solely for desaturation purpose only. In Fig. 4a) the usage of this resistor is indicated with “RGD”, whereas the nominal gate resistors are “RGIon” and “RGIoff”, respectively.

Assuming a practical 6.5kV traction inverter system with a pulse frequency of several hundred Hertz and maximum interlock time of 20µs, the RCDC-IGBT performs best if the gate runs at 0V in diode conduction mode [2]. By doing so, the static diode losses are slightly higher than compared to operation at $v_{GE}$=-15V. The total losses are the lowest as $Q_{rr}$ is lower compared to $v_{GE}$=-15V diode operation. For other pulse frequencies and possibly longer desaturation times the optimal operation regime can be different.

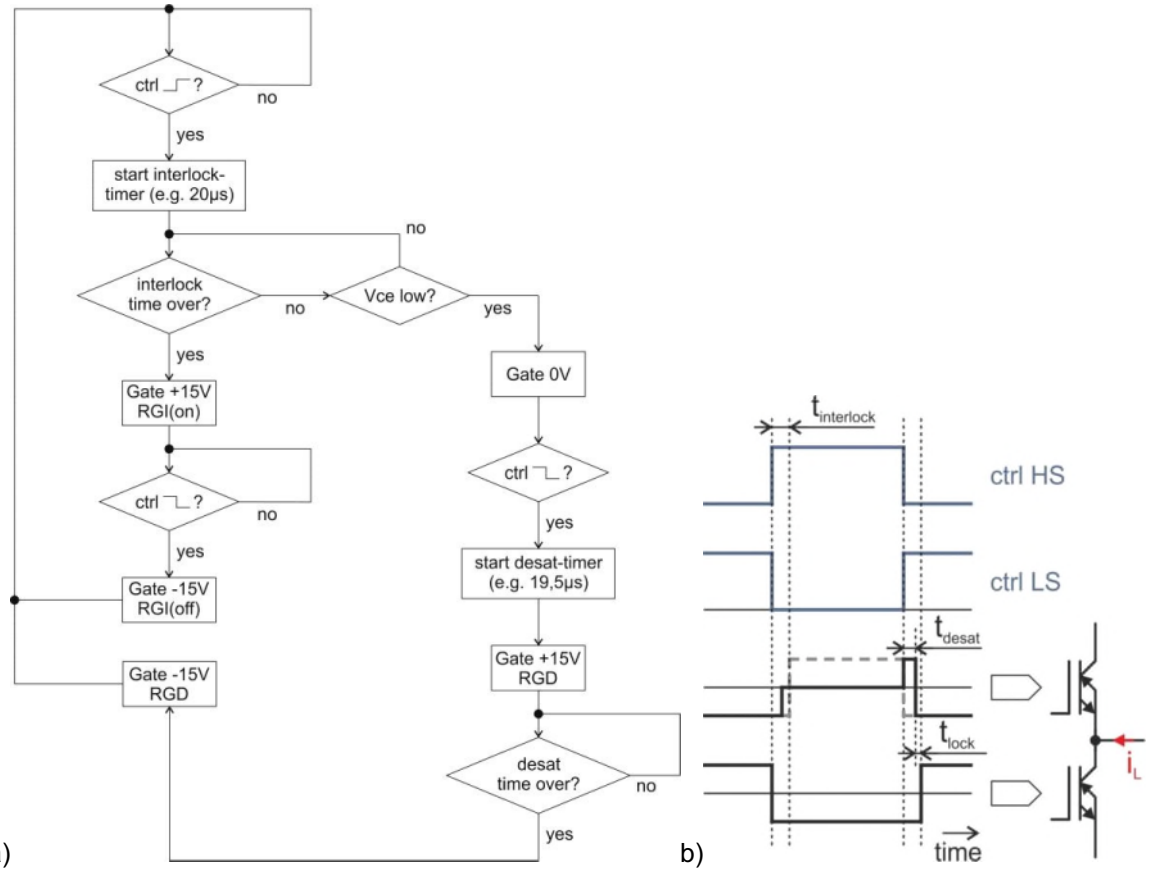


Fig. 4. a) Flowchart of the RCDC gate driver control scheme from Fig. 2a) with the diode desat functionality added; b) RCDC-IGBT gate driver input signals (ctrl) from inverter control stage and RCDC-IGBT gate driver output voltage, interlock time is calculated on each driver stage individually, dashed line: standard inverter driver output

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### 3.3. Load Current Zero Crossing Approach: Diode to IGBT

If in a classical inverter approach a diode is conducting, the load current can easily change sign since the antiparallel IGBT device is typically turned on via it´s gate. In case of RCDC-IGBT, this situation needs to be detected and the gate must be turned on immediately, otherwise the load current is interrupted.

If a pn-diode conducts and the current decreases to zero, the diode is still flooded with carriers. This allows the load current to change direction, although the antiparallel IGBT gate is not turned on. In Fig. 5 the load current $i_L$ changes direction at $t_4$ but, indicated by $i_{C(HS)}$, still flows through the diode. The corresponding IGBT gate is still in off state as it´s corresponding ctrl-signal is low. As soon as the diode´s carriers are removed by the load current, the diode starts to take reverse voltage at time $t_5$. The load current´s di/dt is quite small compared to hard switching di/dt, all this happens relatively slow.

Physically, the gate driver needs to check for positive voltage $v_{CE}$ as long as the diode is in conduction mode. As soon as $v_{CE}$ is positive, the gate is turned on immediately. The detection circuit should be able to react on low positive voltages $v_{CE}$. Otherwise the change in output voltage becomes unnecessarily high. In Fig. 5 at time $t_5$ this effect is depicted in exaggerated manner. For this purpose it´s advised to rely on classical desat-detection-circuit with a high voltage diode chain, a current source and a comparator. A basic schematic is given in Fig. 8.

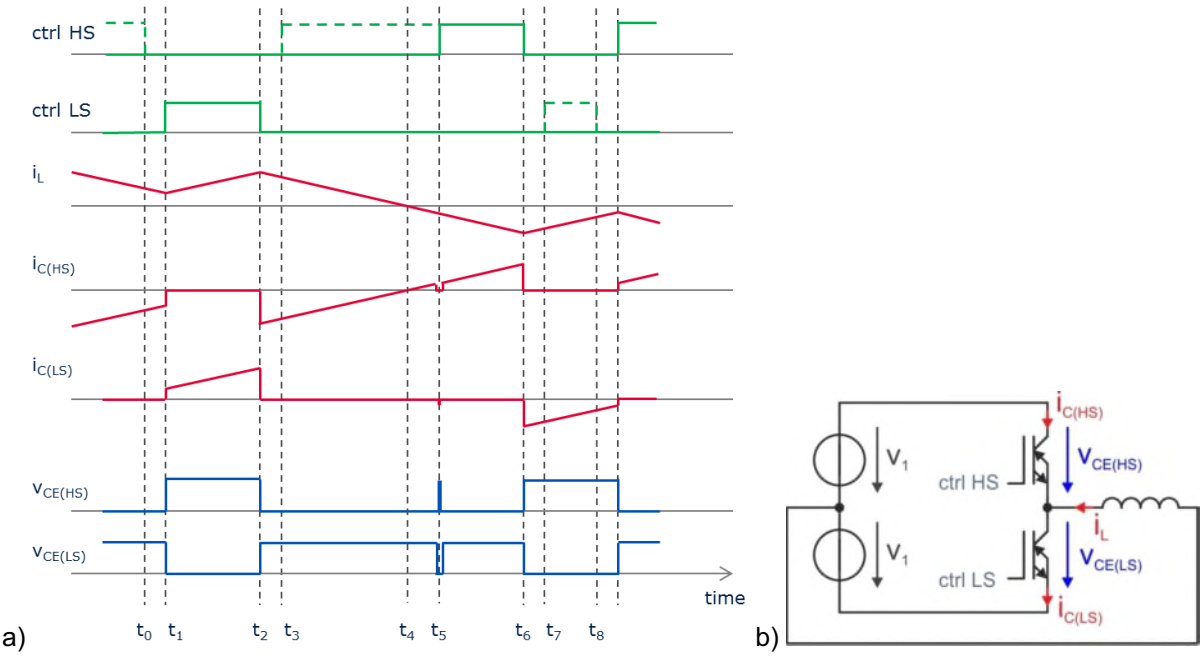


Fig 5. Schematic waveforms (a) of a simplified RCDC-IGBT halfbridge system (b) for demonstration of load current zero crossing at $t_4$, current $i_{C(HS)}$ goes through the diode for $t_2 \leq t < t_5$ and changes into IGBT for $t_5 \leq t < t_6$

Based on a lab experiment, in Fig. 6 the load current commutation from diode to IGBT is demonstrated. This was done by means of an H-bridge RCDC-IGBT module setup. The gate driver circuit detects the small increase in $v_{CE}$, seen in the inset, and turns on the RCDC-IGBTs gate. The load current changes direction without interruption and without excessive voltage distortion.

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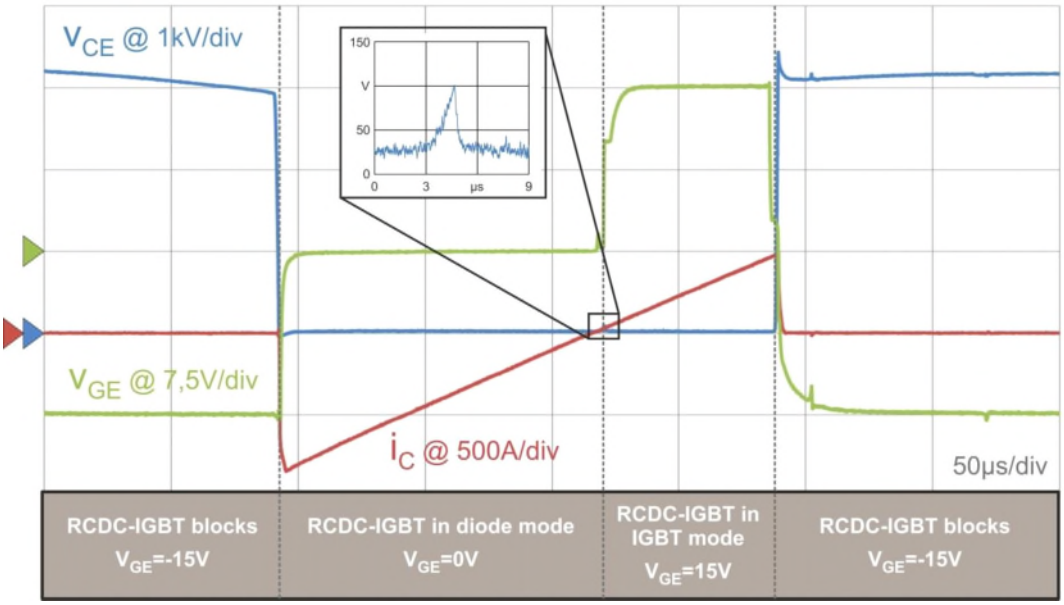


Fig. 6. Example of load current zero crossing, commutating from diode ($i_C$<0) at $v_{GE}$=0 into the antiparallel IGBT ($i_C$>0) with $v_{GE}$=15V; very small increase in $v_{CE}$ (see inset) at the time the detector recognizes the zero crossing event, load current without interruption

### 3.4. Load Current Zero Crossing Approach: IGBT to Diode

In addition to the transition of the load current from diode to IGBT, the current can also change its direction coming from IGBT and further flowing into the antiparallel diode. Latter happens without the risk of interrupting the load current, since the gate remains in on state and the diode takes the current anyway. If the gate would remain at $v_{GE}$=15V, the diode´s $V_F$ would be unnecessarily high and thus the static losses become high until the next ctrl command is received. It´s recommended to make use of the proposed desat-circuit again, now detecting small voltage $v_{CE}$ across the RCDC-IGBT. Since $V_F$ is initially high, the voltage difference in $v_{CE}$ from IGBT to diode conduction becomes high as well and can easily be detected.

## 4. Conclusion

Figure 7 shows the RCDC-IGBT gate driver control scheme from Fig. 4 with the desat-circuit sense information “HV desat” added. The given state machine now is able to handle all specific RCDC-gate drive requirements like diode conduction mode detection, diode desaturation, load current zero crossing from diode to IGBT and vice versa.

In the lab the gate driver shown in Fig. 8 was used. If IGBT switching is required, the nominal $R_G$´s (RGI(on), RGI(off)) are taken. In case of minimum time constant switching is required for diode desaturation purpose, the comparatively small diode $R_G$ (RGD) is chosen. The advanced H-bridge concept allows to drive $v_{GE}$=0 in case of diode conduction mode.

In high voltage IGBT gate drivers a high voltage divider for desaturation detection purpose is commonly used. The RCDC-IGBT gate driver from Fig. 8 is additionally equipped with the desat-circuit consisting of a high voltage diode chain, comparator and current source. On a logic device, three binary input signals “ctrl”, “Vce” and “HV desat” are processed by the state machine given in Fig. 7.

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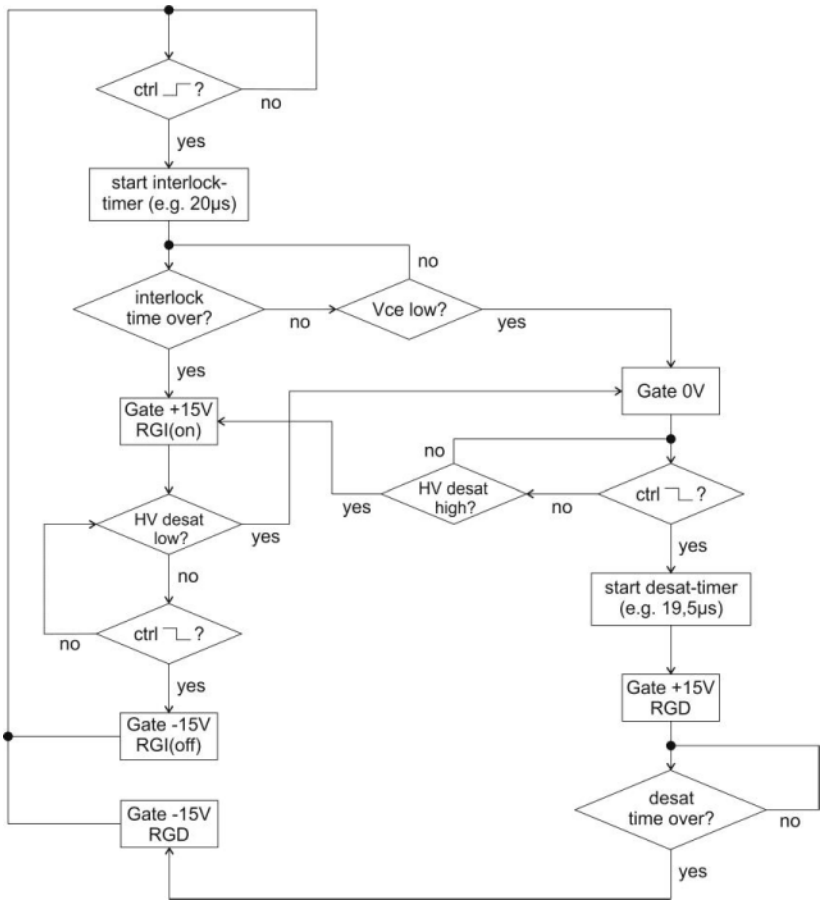


Fig. 7. Final flowchart from the RCDC gate driver control scheme based on Fig. 4 with the load current zero crossing detector added, recommended desat-circuit output signal as “HV desat”, high if $v_{CE}$>threshold, low if $v_{CE}$<threshold

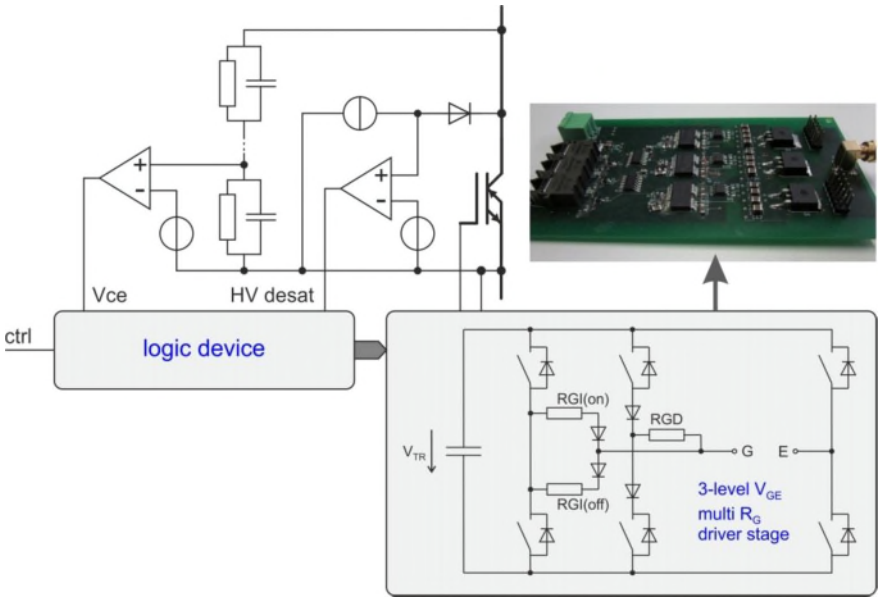


Fig. 8. Schematic gate driver circuit for operating a RCDC-IGBT in a conventional inverter system, from the inverter control stage only the ctrl signal needs to be provided, all RCDC-IGBT specific information is generated and processed inside the gate driver circuit

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## 5. Summary

Based on the properties of a 6.5kV reverse conducting IGBT with diode control, methods for loss optimal gate drive were discussed. The major change compared to standard IGBT/diode combination is the diode functionality, which now can be controlled via the IGBT´s gate. In the present paper, aspects of driving a RCDC-IGBT in an inverter system are discussed and solutions how to treat the special cases are proposed. A state machine for loss optimal control is demonstrated which - apart from the classical control signal - only needs two additional and easy to provide binary input signals. In combination with a special gate driver circuit including one additional detector circuit and a logic device, the RCDC-IGBT can easily operate in a standard inverter environment. Any RCDC specific information is handled inside the gate driver.

## 6. Acknowledgement

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## 7. References

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