Guidelines for CoolSiC™ MOSFET gate drive voltage window

About this document

Infineon strives to enhance electrical systems with comprehensive semiconductor competence. This expertise is revealed in the products themselves and their behavior under relevant use conditions, and also in the sharing of knowledge on the latest semiconductor technologies. For new technologies such as the silicon carbide (SiC) MOSFET, this is of particular importance, since a SiC MOSFET under certain operating conditions shows different characteristics compared to silicon (Si) switches. Moreover, experience with this new technology and accompanying literature is not available to the public to the same extent as for other technologies that have been on the market for a long time.

One important aspect to be considered for the SiC MOSFET is the drift of gate threshold voltage ($V_{GS(th)}$) under long-term operation. Infineon first discoverd the phenomenon of a drift of gate threshold voltage ($V_{GS(th)}$) under long-term operation caused by the dynamic components, and firstly presented the recommended operation gate voltage area to minimize the drift.

With continuous investment in R&D, the CoolSiC™ MOSFET M1H show a significant improvement in $V_{GS(th)}$ stability. The drift caused by the dynamic components is reduced significantly.

This new revision of the application note provides updated guidelines on gate voltage for the CoolSiC MOSFET™.

Scope and purpose

- To explain the long-term behavior of $V_{GS(th)}$ under switching operation
- To discuss its impact on the application
- To provide design guidelines to limit the related increase of on-state resistance $R_{DS(on)}$ as the major implication for the user in the application

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1 $V_{GS(th)}$ drift phenomenon

The nature of the wide-bandgap material SiC and the different properties of the semiconductor-dielectric interface compared to silicon material cause some natural peculiarities in threshold voltage variation and bias-temperature instability (BTI), which need to be understood and assessed. Extensive investigations have been conducted in order to understand such differences, to explain their relation to the semiconductor material, to clarify their relevance for the application, and to define the consequences with respect to specification and system design.

As far as static gate-bias stress is concerned, the standard test procedures typically used to characterize threshold voltage and threshold voltage drifts for Si devices need to be adapted for SiC MOSFETs. Based on these findings, a new measurement stress procedure has been developed for the BTI evaluation of SiC MOSFETs, which allows one to distinguish between reversible threshold voltage hysteresis and more permanent threshold voltage drift (BTI). This measurement technique has been used for an in-depth study assessing the $V_{GS(th)}$ stability of recently launched SiC MOSFET parts. It has been demonstrated that the Infineon 1200 V CoolSiC™ MOSFET excels in overall $V_{GS(th)}$ stability, in particular due to a very low negative BTI and a very narrow drift variation among different devices[1].

Besides the drift driven by static stress, the threshold voltage of SiC MOSFET devices may undergo an additional drift triggered by switching events (turn-on and turn-off of the device). This additional component can only be identified in long- term switching tests. Based on current knowledge, the effect is related to gate-oxide trap dynamics. This effect is a general characteristic of the current SiC MOSFET technologies as related internal studies have shown. It is not limited to Infineon CoolSiC™ MOSFET devices.

The characteristics of this phenomenon for Infineon CoolSiC™ MOSFET have been studied by performing long-term tests under various switching conditions. The data shows that switching stress leads to a slow $V_{GS(th)}$ increase over time. However, irrespective of the parameters chosen, a negative switching-induced $V_{GS(th)}$ drift has never been observed. The $V_{GS(th)}$ drift value is similar among the different devices that have been stressed at the same operation conditions. The increase of the threshold voltage $V_{GS(th)}$ reduces the MOS channel overdrive ($V_{GS(on)} - V_{GS(th)}$) and therefore an increased channel resistance (R_{ch}) can be observed. This phenomenon is described in equation [1], where L is the length of the channel, W is the width of the channel, μ_n is the free electron mobility, C_{ox} is the gate oxide capacitance, $V_{GS(on)}$ is the positive on-state gate voltage, and $V_{GS(th)}$ is the threshold voltage of the device [2].

$$R_{ch} \approx \frac{L}{\mu_n \cdot C_{ox} \cdot W \cdot (V_{GS(on)} - V_{GS(th)})} \qquad [1]$$

The total $R_{DS(on)}$ resistance is determined by the sum of the single resistances. These are namely the channel resistance (R_{ch}), the resistance of the junction field-effect transistor (R_{JFET}), the epitaxial layer resistance of the drift region (R_{epi}) and the resistance of the highly doped SiC substrate (R_{Sub}). The entire chain for the total $R_{DS(on)}$ is described in equation [2].
Thus the increase of $V_{GS(th)}$ causes a slight increase in the channel resistance, which is followed by a slight increase in $R_{DS(on)}$ and a slight increase in on-state losses over time.

$$R_{DS(on)} = R_{ch} + R_{JFET} + R_{epi} + R_{Sub} \qquad [2]$$

VGS(th) drift phenomenon

The noticeable impact of the $V_{GS(th)}$ increase on the $R_{DS(on)}$ differs among the voltage classes of the devices. The higher the voltage class, the more pronounced is the contribution of the epitaxial layer resistance (R_{epi}). Consequently, the R_{epi} is more dominant, and contributes more to the total $R_{DS(on)}$ compared to smaller voltage classes like 650 V. As a consequence, we can conclude that the impact of the drift in $V_{GS(th)}$ on $R_{DS(on)}$ is less severe for higher voltage classes.

Please note that the basic function of the device is not affected, in particular:

- the blocking capability
- the reliability level of the devices, e.g. cosmic radiation robustness, humidity robustness, etc.
- the $V_{GS(th)}$ drift has a negligible effect on the total switching losses

Key parameters that influence the switching-induced $V_{GS(th)}$ drift include:

- the number of switching events, translating into switching frequency and total operation time
- gate drive voltage, mainly $V_{GS(off)}$
- the overshoot and undershoot of the gate-source terminal directly at the chip

The following operation parameters were found to have minor or negligible impact on the switching-induced $V_{GS(th)}$ drift:

- junction temperature
- switching slopes (dV/dt and dI/dt)
- drain-source voltage
- drain current

2 Impact on the application

The major impact of the $V_{GS(th)}$ drift is a long-term increase of the $R_{DS(on)}$ for the chosen V_{GS} in the application. Generally, the increase of $R_{DS(on)}$ increases the conduction losses leading to an increase in junction temperature T_{vj} over time. This increase of T_{vj} over time should also be considered during the assessment of power cycling.

Whether the T_{vj} increase is critical or not depends on the individual applications and the operating conditions. In many cases the impact is minor, and leads to a negligible increase in T_{vj} even after 20 years' lifetime. Other applications could be more critical. Therefore, the design guideline shown in Chapter 3 must be considered.

Below, two examples (half-bridge configuration in a DC-AC-inverter) illustrate the varying impact of a given, fixed-amplitude $V_{GS(th)}$ drift on different applications. The first example represents applications where the conductions losses (P_{con}) dominate the loss distribution. The second example considers an application in which switching losses (P_{sw}) and conduction losses contribute equally. The parameters of the two examples are listed in Table 1.

Table 1 Parameters of two examples

	Example 1: conduction losses dominating	Example 2: conduction losses and switching losses equally distributed
Switching frequency (kHz)	8	30
Nominal current (A)	50	38.5
Output voltage (V)	400	400
Output frequency (Hz)	50	50
DC link voltage (V)	600	600
Power factor	1	1
Thermal resistance (K/W)	3.6	3.6
Ambient temperature (°C)	40	40

For each example, the effects of a $V_{GS(th)}$ drift on the loss distribution and the junction temperature are shown in Figure 1. Both examples have the same $V_{GS(th)}$ drift.

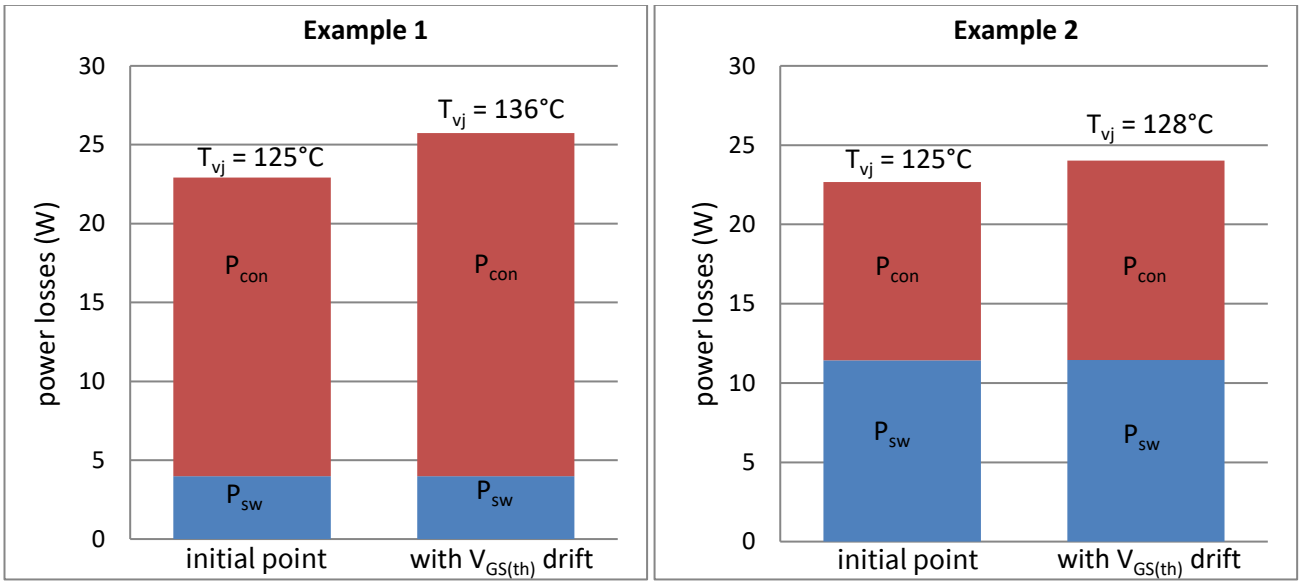

Figure 1 Examples of $V_{GS(th)}$ drift impacts on applications

Impact on the application

As seen from example 1, in which conduction losses dominate, a $V_{GS(th)}$ drift leads to notably higher total losses and thus to higher junction temperatures. For those applications, the design guidelines detailed in Chapter 3 must be considered. For the application with balanced switching and conduction losses, a $V_{GS(th)}$ drift will only have a minor effect on the total losses and the junction temperature. In other applications in which the overall losses are dominated by the dynamic losses, the impact of the $V_{GS(th)}$ drift is nearly negligible.

3 Gate drive voltage guidelines

The subchapters in this section give guidance on how the change in $R_{DS(on)}$ can be predicted for different voltage classes and limited to an acceptable range.

3.1 Guidelines for 1200 V devices

The dynamic drift of the $V_{GS(th)}$ increases with the number of switching events. To understand this more clearly: the total number of switching events is translated into a normalized switching frequency, which takes into consideration 10 years of full operation (24h/7d). With the known actual switching frequency f_{sw} in kHz, the target lifetime in years, and the operation time as a percentage of the total system lifetime, a normalized switching frequency is defined using the following formula:

Normalized f_{sw} = actual f_{sw} [kHz] × lifetime [yrs.] × operation time in percentage [%] ÷ 10 [yrs.]

The recommended operating area provided by Infineon is separately given for CoolSiC™ MOSFETs in module and in discrete packages even though the basic chip technology is the same. It is because over- and undershoots in the gate signal are strongly dependent on operation conditions, circuit design and parasitics. In particular, the recommended operating area (ROA) for discrete devices is more conservative due to the greater flexibility in the circuit design, application conditions, inverter topology, gate-drive design, PCB layout and thermal design. For these reasons, the ROA of discrete devices also includes a potential overshoot of 2 V to account for variabilities in gate-driver design. For modules, no extra overshoot needs to be considered, since 0 V overshoot can be achieved in any case by a proper gate-driver design.

With the estimated normalized switching frequency based on the actual application, the minimum turn-off gate voltage, including a potential undershoot, can be extracted from Figure 2 and Figure 3, respectively for discrete and module products. The diagrams have been updated with new data for the M1H version with improved gate oxide.

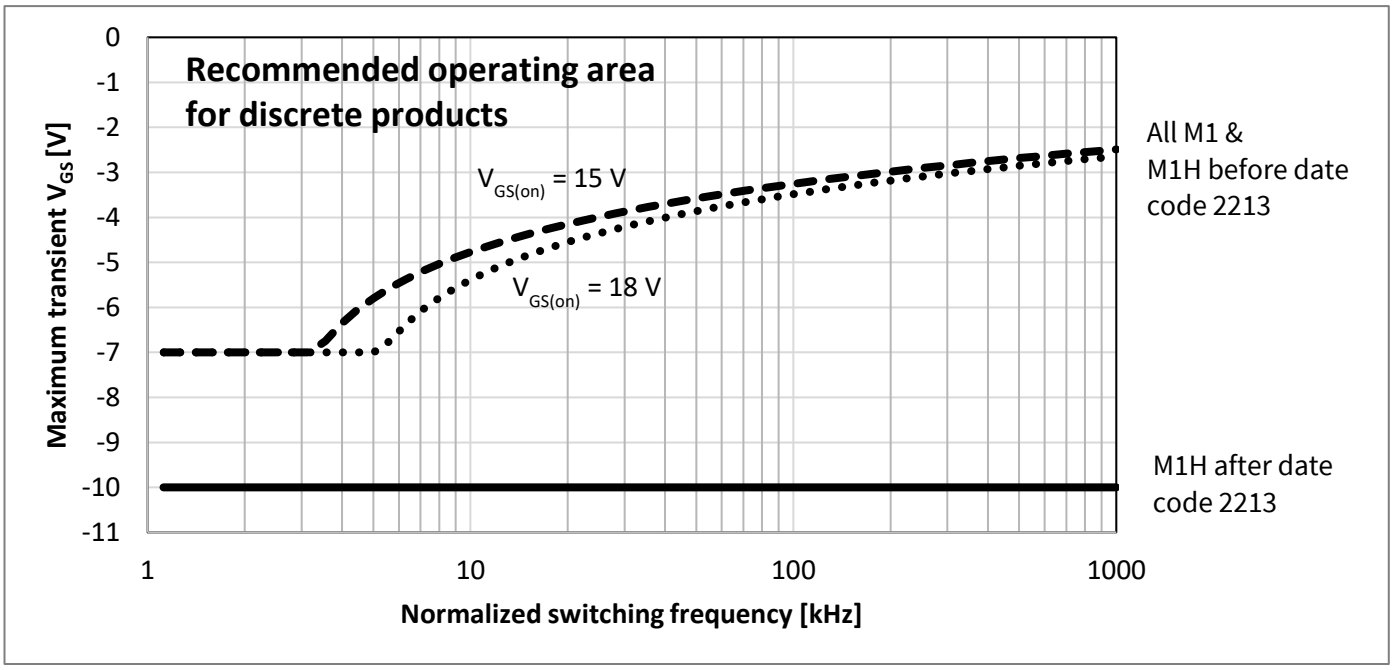

Figure 2 Minimum turn-off gate voltage for 1200 V discrete package products

Gate drive voltage guidelines

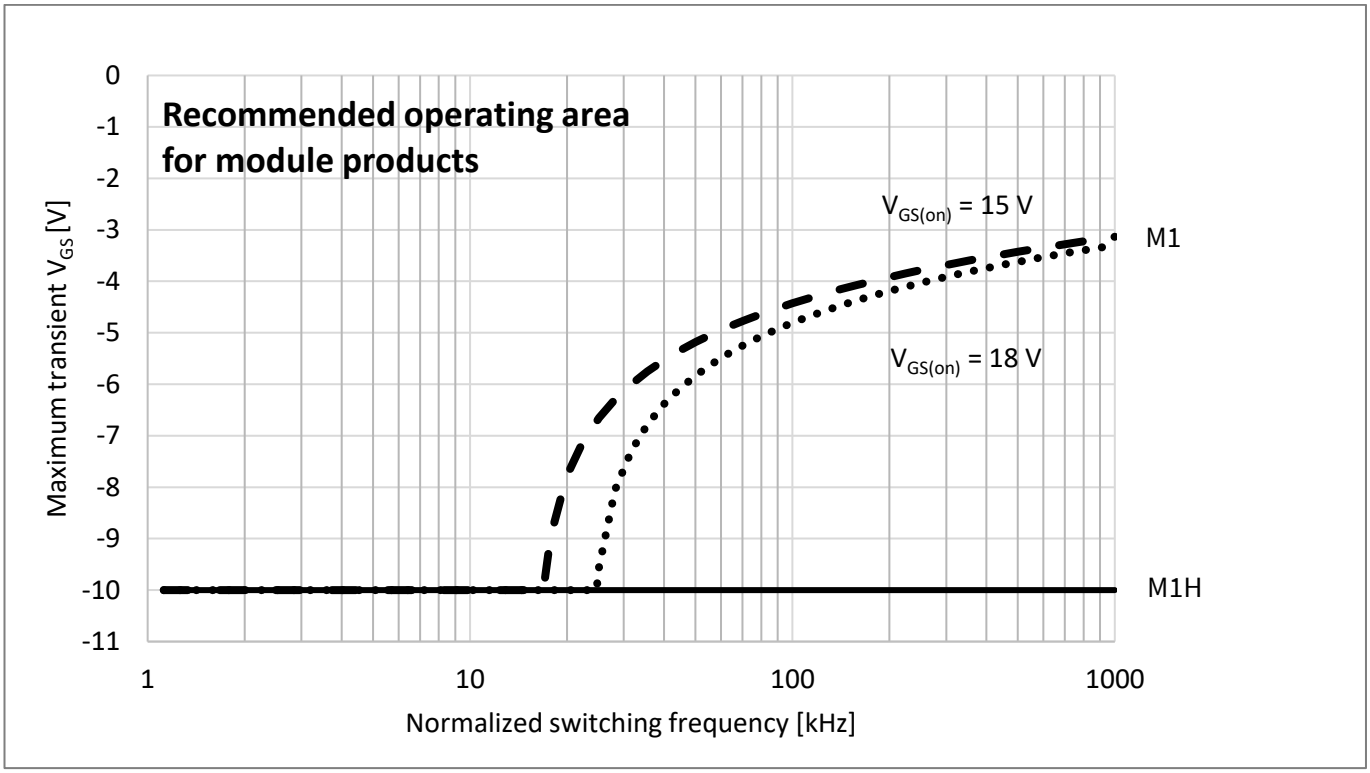

Figure 3 Minimum turn-off gate voltage for 1200 V module products

Details on how to use this information are described in the following example. A solar inverter has:

- an actual switching frequency of 20 kHz
- a targeted lifetime of 20 years
- an operation time of 50%
- a normalized switching frequency of 20 kHz * 20 yrs. * 50% / 10 yrs. = 20 kHz

For a turn-on voltage of 18 V, using CoolSiC™ MOSFETs M1 in discrete packages, the turn-off gate voltage including undershoot has to be between -4.6 V and 0 V, as can be seen in Figure 2. For a turn-on voltage of 15 V, using CoolSiC™ MOSFET M1 modules, the turn-off gate voltage including undershoot has to be designed between -7.7 V and 0 V (see Figure 3).

The minimum turn-off voltage, which defines the recommended operating area is set to ensure that the $R_{DS(on)}$ increase at I_{nom} and T_{vj}=125°C will not exceed 15% of the initial value during the entire product lifetime.

The relative increase of $R_{DS(on)}$ depends on the operating current I_d and junction temperature T_{vj} (see Figure 4).

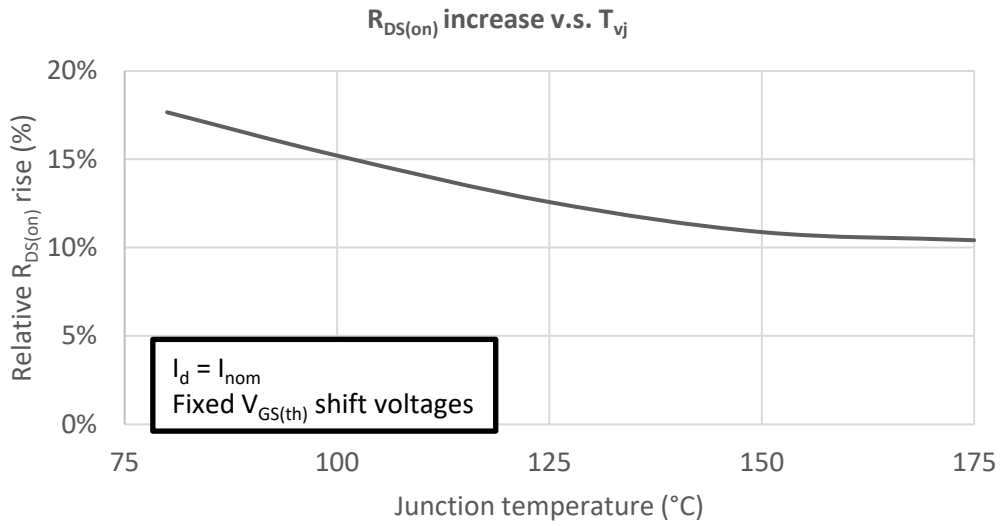

Figure 4 Relative $R_{DS(on)}$ increase at different junction temperatures

As a final remark, please note that independent of the ROA, the lowest peak gate voltage must never exceed the maximum ratings in the data sheet.

3.1.1 Assessment of worst-case $R_{DS(on)}$-drift at the end of the mission profile

Infineon always strives to enhance newer semiconductors generations in regards to their bevavior and performance. Technologies like the 1200 V CoolSiC™ MOSFET M1H shows significant improvements with regard to threshold voltage stability. This allows designers to significantly enhance the allowed gate operation window for 1200 V M1H and still stay well below 15% $R_{DS(on)}$-drift.

Extensive tests under various operation conditions were carried out by Infineon to develop a predictive model that describes the change in $R_{DS(on)}$ as a function of the number of cycles (N_{cycles}) [3]. This gives the opportunity to predict the worst-case $R_{DS(on)}$ change accurately for arbitrary mission profiles.

To assess the worst-case, end-of-mission profile (EoMP) $R_{DS(on)}$ drift for individual applications, one needs to consider the total number of switching events until EoMP. This number can be easily calculated from the lifetime target, the total operation time and the switching frequency of the application. With the number of switching cycles (N_{cycles}) the relative change in $R_{DS(on)}$ can be extracted from Figure 5.

Please note:
Figure 5 considers the maximum positive and negative dynamic gate-source voltage of the respective data sheets. Both diagrams represent drift values under worst-case conditions, and are valid as long as the devices do not exceed the data sheet limits of the respective product. The diagrams enable the customers to choose any parameter set inside the data sheet framework that fits their application best, without spending much effort on considering the drift impact and parasitic over- & undershoots in the gate signal.

Applications running at well-controlled gate-bias levels that are well below the datasheet maximum limits may exhibit even lower $R_{DS(on)}$ drift values for the same number of switching cycles, as shown in Figure 5 [3].

When operating at a less negative turn-off gate voltage (e.g. -2 V instead of -5 V), the impact on the application is slight. Several application-relevant parameters should be considered, e.g. E_{on} and E_{off} will change slightly and the forward voltage of the SiC MOSFET body diode will be reduced.

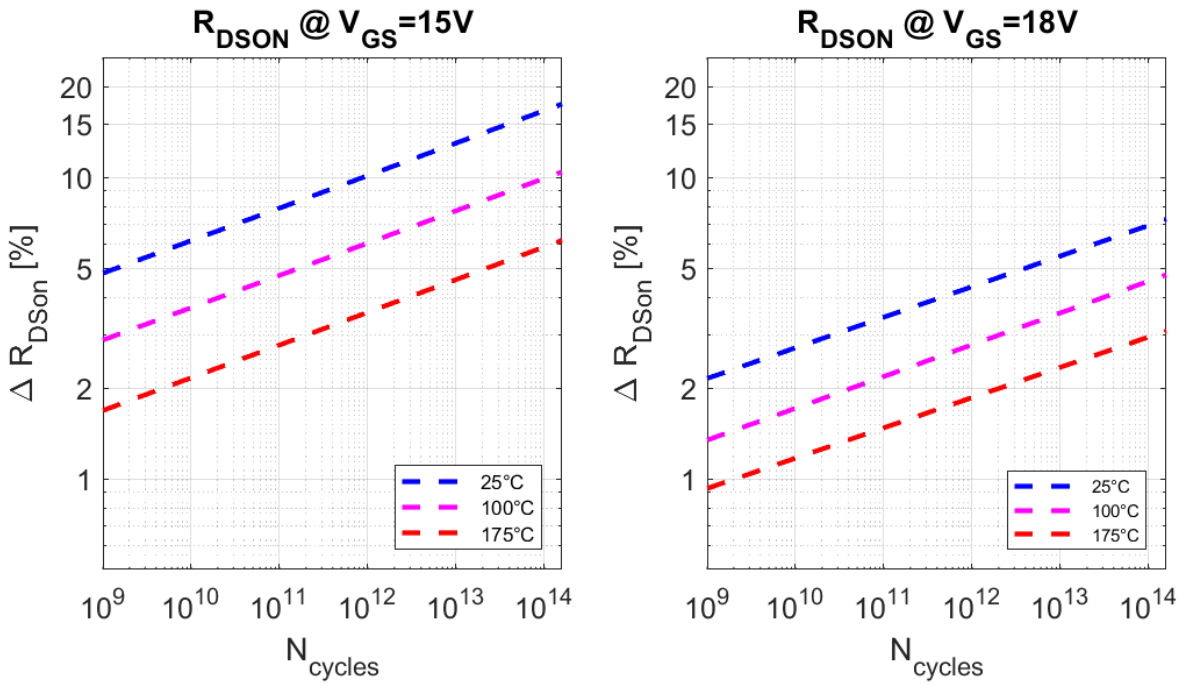

Figure 5 **Left: relative $R_{DS(on)}$ change @ $V_{GS(on)}$ = 15 V, T_{vjop}= 25°C, 100°C & 175°C; Right: relative $R_{DS(on)}$ change @ $V_{GS(on)}$ = 18 V, T_{vjop}= 25°C, 100°C & 175°C;**

How to use this information is explained in the following example:

- Targeted lifetime [years]: 20
- Real operation time [%]: 50 = 10 years
- Real operation time [s]: 315360000 s (10 years)
- Switching frequency [kHz]: 48
- Cycle duration [s]: 1 / switching frequency = 0.0000208
- Number of cycles at end of life: operating time / cycle duration = ~1.52E+13

For a turn-on voltage of 18 V, an $R_{DS(on)}$ change of ~6% @ 25°C and ~3% @ 175°C can be expected, as shown in Figure 5 on the right.
For a turn-on voltage of 15 V, a change in $R_{DS(on)}$ of ~13% (25°C) and ~5% (175°C) can be predicted (see Figure 5 on left).

3.2 Guidelines for 650 V devices

The $R_{DS(on)}$ variation caused by switching events with negative gate voltage turn-off ($V_{GS(off)}$) is more pronounced in 650 V CoolSiC™ MOSFET devices compared to higher breakdown voltage devices (e.g. 1200 V CoolSiC™ MOSFET), given that the R_{ch} has a higher contribution to the overall $R_{DS(on)}$. However, the $R_{DS(on)}$ variation can be reduced to negligible values by operating the device within the gate-source voltage operating range specified in the product datasheet.

3.2.1 Assessment of worst-case $R_{DS(on)}$-drift at the end of the mission profile

In order to extend the negative driving voltage capability of 650V CoolSiC™ MOSFET, several tests under various operating conditions following the methodology presented in [3] were carried out to develop a model that enables to assess the change in $R_{DS(on)}$ as a function of the number of cycles (N_{cycles}).

To assess the worst-case end-of-mission profile (EoMP) $R_{DS(on)}$ - drift for individual applications one needs to consider the total number of switching events until EoMP. This number can be easily calculated from the lifetime target, the total operation time and the switching frequency of the application. With the number of switching cycles (N_{cycles}) the relative change in $R_{DS(on)}$ can be extracted from Figure 6.

Please Note:

At the moment of the publication of this application note revision, Figure 6 is valid for the devices listed in table 1, as long as the V_{GS} overshoots and undershoots are within the V_{GS} maximum ratings specified in Revision 2.0 of the datasheet of the corresponding products. Moreover, the $R_{DS(ON)}$ variation might be reduced to-not exceed the max value stated in the datasheet by operating the device within the gate source voltage operating range stated in the product datasheet.

IMW65R027M1H	IMZA65R027M1H	IMBG65R022M1H
IMW65R030M1H	IMZA65R030M1H	IMBG65R030M1H
IMW65R039M1H	IMZA65R039M1H	IMBG65R039M1H
IMW65R048M1H	IMZA65R048M1H	IMBG65R048M1H
IMW65R057M1H	IMZA65R057M1H	IMBG65R057M1H
IMW65R072M1H	IMZA65R072M1H	IMBG65R072M1H
IMW65R083M1H	IMZA65R083M1H	IMBG65R083M1H
IMW65R107M1H	IMZA65R0107M1H	IMBG65R107M1H
		IMBG65R163M1H
		IMBG65R260M1H

Tabelle 1: Product for which Figure 6 is valid at the moment of this publication

Infineon always strives to improve their technology, hence always check **CoolSiC™ MOSFET 650 V M1 trench power device application note** AN_1907_PL52_1911_144109 for the latest information regarding this topic.

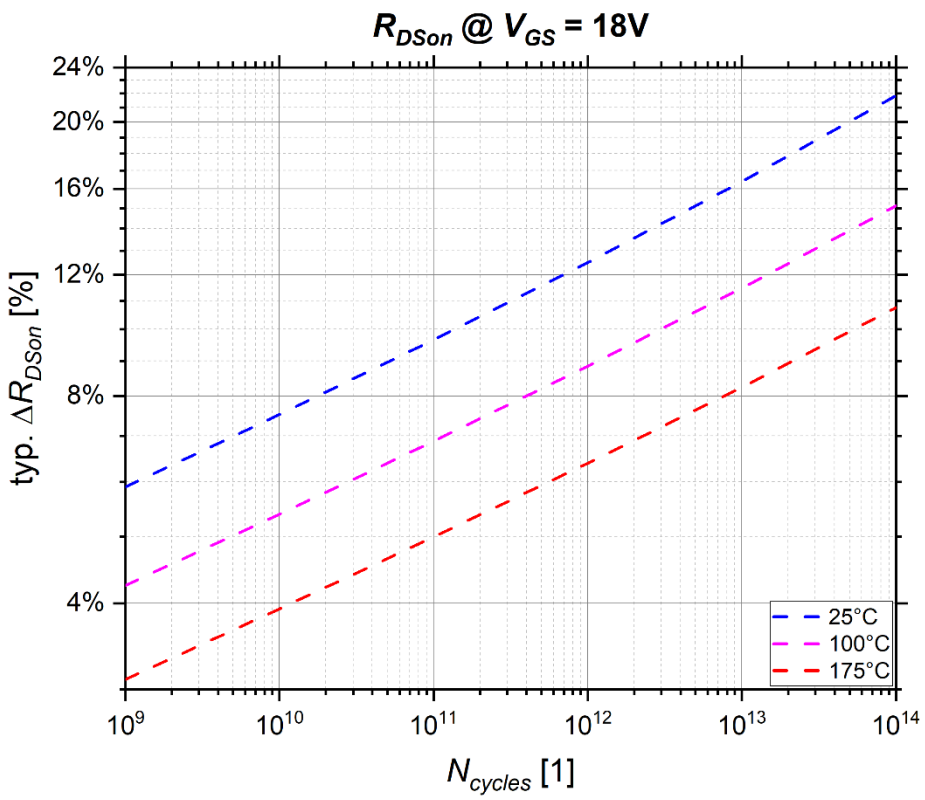

Figure 6 **Relative $R_{DS(on)}$ change @ $V_{GS(on)}$ = 18 V, T_{vjop}= 25°C, 100°C & 175°C based on extrapolation of intermediate readouts.**

How to use this information is explained in the following example:

- Targeted lifetime [years]: 10
- Real operation time [%]: 50= 5 years
- Real operation time [s]: 1.577E8 (5 years)
- Switching frequency [kHz]: 65
- Cycle duration [s]: 1/switching frequency = 0.0000154
- Number of cycles at end of life: operating time/cycle duration = ~1.025 E+13

For a turn-on voltage of 18 V, an $R_{DS(on)}$ change of 15% @ 100°C and 11% @ 175°C can be expected, as shown in Figure 6

3.3 Definition of the gate-voltage overshoot and undershoot

The $V_{GS(th)}$ drift is a long-term effect, therefore only the repetitive overshoot and undershoot should be considered. An overshoot and undershoot of the gate voltage caused by non-standard operating conditions, e.g. power-grid instability, short-circuit conditions, etc. should not be considered.

The overshoot and undershoot are only critical for $V_{GS(th)}$ drifts if the spikes reach the gate- source terminals directly at the chip. To quantify them experimentally, over- and undershoots would ideally be measured

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directly at the chip terminals. However, since this is not always possible, the following guidelines provide a good estimation:

- Use a direct probe with high bandwidth (100 MHz) if isolation is not required
- Alternatively, use a differential probe with high bandwidth and high common-mode rejection capability if isolation is required
- Always try to measure as close to the chip as possible, as shown in Figure 6

Figure 6 Example of gate-voltage measurement points

The shape of the gate voltage overshoot and undershoot may vary between individual inverter designs. The peak voltage should be considered, as shown in Figure 7.

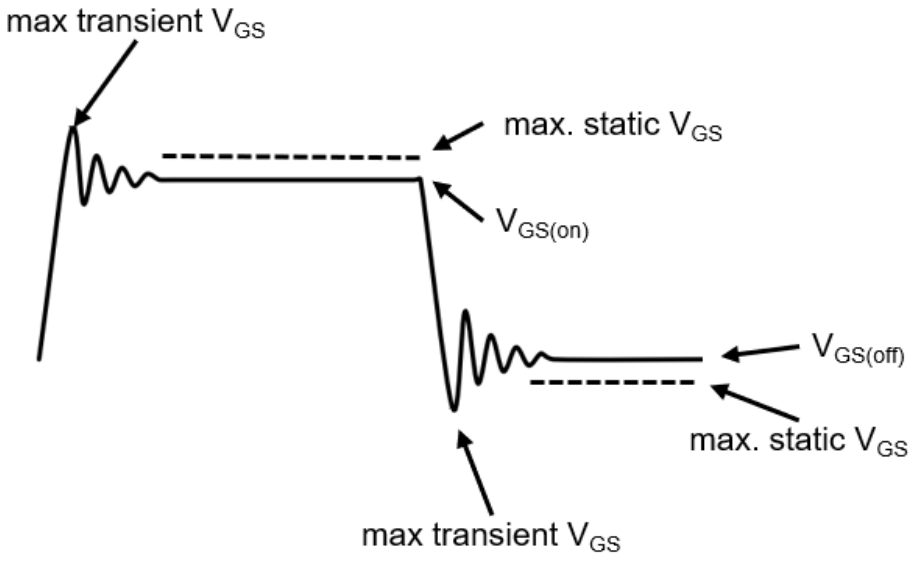

Figure 7 Gate voltage overshoot and undershoot

3.4 References

[1] T. Aichinger, G. Rescher, G. Pobegen: Threshold voltage peculiarities and bias temperature instabilities of SiC MOSFETs; Microelectronics Reliability 80 (2018) 68–78.

[2] Infineon : Whitepaper 08-2020: How Infineon controls and assures the reliability of SiC-based power semiconductors 16–21; www.infineom.com;

[3] P. Salmen, M. W. Feil, K. Waschneck, H.Reisinger, G. Rescher, T. Aichinger: A new test procedure to realistically estimate end-of-life electrical parameter stability of SiC MOSFETs in switching operation; 2021 IEEE International Reliability Physics Symposium (IRPS) (2021).

Revision history

Document version	Date of release	Description of changes
1.0	2018-05-28	Initial version
1.1	2019-05-06	Including the undershoot/overshoot in the ROA, and modify corresponding wording
1.2	2022-03-04	Extended $V_{GS(th)}$ drift phenomenon explaination Including End-of-life assessment for 1200V M1H Including End-of-life assessment for 650V M1H Update of gate over- & undershoot waveform in chapter 3.3 Extended references

Guidelines for CoolSiC™ MOSFET gate drive voltage window

Revision history

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