Guidelines for CoolSiC™ MOSFET gate drive voltage window

About this document

Infineon strives to enhance electrical systems with comprehensive semiconductor competence. This expertise is revealed in the products themselves and also in the sharing of knowledge on the latest semiconductors technologies and their behavior under relevant use conditions. For new technologies such as the silicon carbide (SiC) MOSFET this is of particular importance, since a SiC MOSFET under certain operating conditions shows different characteristics compared to silicon (Si) switches. Moreover, experience with this new technology and accompanying literature is not available to the public to the same extent as for other technologies that have been on the market for a long time.

One important aspect to be considered for the SiC MOSFET is the drift of gate threshold voltage ($V_{GS(th)}$) under long-term operation.

The Bias-Temperature-Instability (BTI) effects caused by continuous bias at the gate are well studied. In addition, a second, dynamic component was revealed. This is related to a drift of $V_{GS(th)}$ which mainly depends on switching frequency and on the selected gate-source voltage for turn off ($V_{GS(off)}$). It is necessary to adjust the operating parameters with respect to the V_{GS} operating window according to potential drift effects.

Scope and purpose

- To explain the long-term behavior of $V_{GS(th)}$ under switching operation
- To discuss its impact on the application
- To provide a design guideline to limit the related increase of on-state resistance $R_{DS(on)}$ as the major implication for the user in the application

Intended audience

Development, design and qualification engineers working with CoolSiC™ MOSFETs.

Table of contents

1 $V_{GS(th)}$ drift phenomenon

The nature of the wide bandgap material SiC and the different properties of the semiconductor-dielectric interface compared to the silicon case cause some natural peculiarities in threshold voltage variation and bias-temperature instability (BTI) which need to be understood and assessed. Extensive investigations have been conducted with the target to understand such differences, to explain their relation to the semiconductor material, to clarify their relevance for the application, and to define their consequences with respect to specification and system design.

As far as static gate bias stress is concerned, the standard test procedures typically used to characterize threshold voltage and threshold voltage drifts for Si devices need to be adapted for SiC MOSFETs. Based on these findings, a new measure-stress-measure procedure has be developed for BTI evaluation of SiC MOSFETs, which allows to distinguish between reversible threshold voltage hysteresis and more permanent threshold voltage drift (BTI). This measurement technique has been used for an in-depth study assessing the $V_{GS(th)}$ stability of recently launched SiC MOSFET parts. It has been demonstrated that the Infineon CoolSiC™ MOSFET excels in overall $V_{GS(th)}$ stability, in particular by a very low negative BTI and a very narrow drift variations among different devices.

Besides the drift driven by static stress, the threshold voltage of SiC MOSFET devices may undergo an additional drift triggered by switching events (turn-on and turn-off of the device). This additional component can only be identified in long- term switching tests. Based on the current knowledge the effect is related to gate oxide trap dynamics. More details will be discussed in upcoming scientific papers. This effect is a general characteristic of the current SiC MOSFET technologies as related internal studies have shown. It is not limited to Infineon CoolSiC™ MOSFET devices.

The characteristics of this phenomenon for Infineon CoolSiC™ MOSFET have been studied by performing long-term tests under various switching conditions. The data shows that switching stress leads to a slow $V_{GS(th)}$ increase over time. However, irrespective of the parameters chosen, a negative switching-induced $V_{GS(th)}$ drift has never been observed. The $V_{GS(th)}$ drift value is similar among different devices, which have been stressed at the same operation conditions. The increase of $V_{GS(th)}$ causes a slight increase in $R_{DS(on)}$, which translates into increased on-state losses over time.

Please note that the basic function of the device is not affected, in particular:

- The blocking capability is not affected.
- The reliability level of the devices is not affected, e.g. cosmic radiation robustness, humidity ruggedness, etc.
- The $V_{GS(th)}$ drift has a negligible effect on the total switching losses.

Key parameters that influence the switching-induced $V_{GS(th)}$ drift include:

- the number of switching events, which translates into switching frequency and total operation time,
- gate drive voltage, mainly $V_{GS(off)}$.

The following operation parameters were found to have less impact on the switching-induced $V_{GS(th)}$ drift:

- junction temperature,
- drain-source voltage,
- drain current,
- switching slopes (dV/dt and dI/dt).

2 Impact on the application

The major impact of the $V_{GS(th)}$ drift is a long-term increase of the $R_{DS(on)}$ for the chosen V_{GS} in the application. Generally, the increase of $R_{DS(on)}$ increases the conduction losses leading to an increase in junction temperature T_j over time. This increase of T_j over time should also be considered during the assessment of power cycling.

Whether the T_j increase is critical or not depends on the individual applications and the used operating conditions. In many cases the impact is minor and leads to a negligible increase in T_j even after 20 years' lifetime. Other applications might be more critical. Therefore, the design guideline shown in Chapter 3 must be considered.

Below, two examples (half-bridge configuration in a DC-AC-inverter) illustrate the varying impact of a given, fixed-amplitude $V_{GS(th)}$ drift on different applications. The first example represents applications where the conductions losses (P_{con}) dominate the losses distribution. The second example considers an application in which switching losses (P_{sw}) and conduction losses contribute equally. The parameters of the two examples are listed in Table 1.

Table 1 Parameters of two examples

	Example 1: conduction losses dominating	Example 2: conduction losses and switching losses equally distributed
Switching frequency (kHz)	8	30
Nominal current (A)	50	38.5
Output voltage (V)	400	400
Output frequency (Hz)	50	50
DC link voltage (V)	600	600
Power factor	1	1
Thermal resistance (K/W)	3.6	3.6
Ambient temperature(°C)	40	40

For each example, the effects of a $V_{GS(th)}$ drift on the losses distribution and the junction temperature are shown in Figure 1. Both examples have the same $V_{GS(th)}$ drift of 1 V, which could be expected at the end of the lifetime.

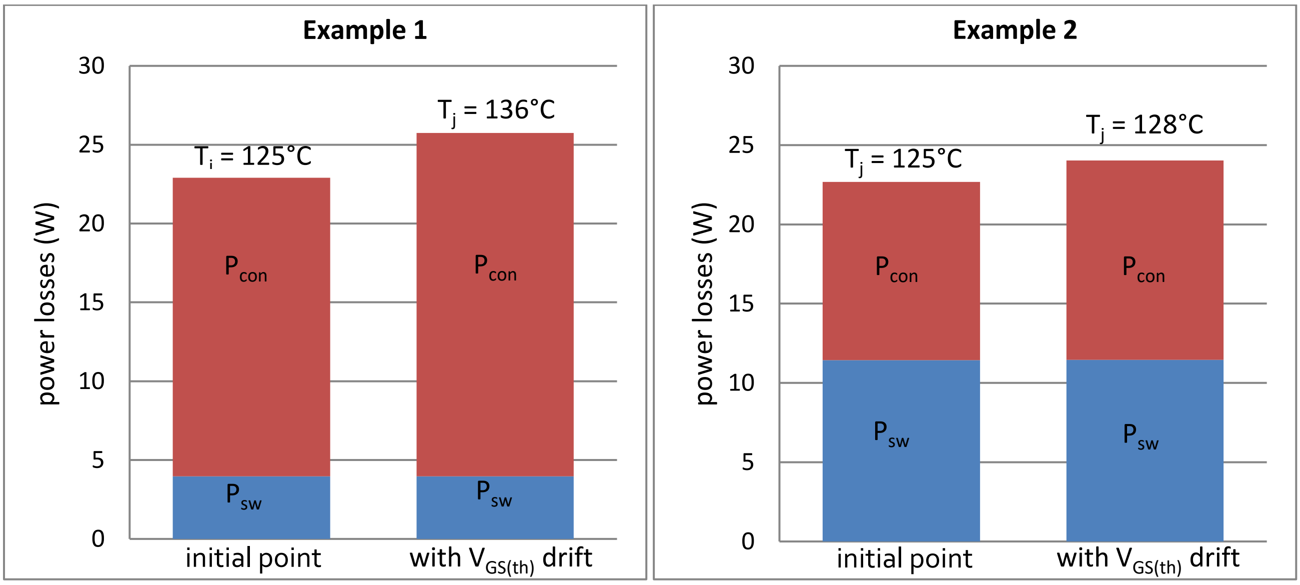

Figure 1 Examples of $V_{GS(th)}$ drift impacts on applications

Impact on the application

As seen from example 1, in which conduction losses dominate, a $V_{GS(th)}$ drift leads to notably higher total losses and thus to higher junction temperatures. For those applications, the design guideline detailed in Chapter 3 must be considered. For the application with balanced switching and conduction losses, a $V_{GS(th)}$ drift will only have a minor effect on the total losses and the junction temperature. In other applications in which the overall losses are dominated by the dynamic losses, the impact of the $V_{GS(th)}$ drift is nearly negligible.

3 Gate drive voltage guidelines

By limiting the gate voltage for turn-off ($V_{GS(off)}$), the $V_{GS(th)}$ drift can be constrained to a range that is acceptable for applications. The upper limit of the turn-off gate voltage is 0 V for all conditions, while the lower limit should be chosen depending on the turn-on voltage, the switching frequency and the total operation time, to limit the $R_{DS(on)}$ increase to an acceptable range.

3.1 Guidelines

The dynamic drift of the $V_{GS(th)}$ increases with the number of switching events. For an easy understanding, the total number of switching events is translated into a normalized switching frequency considering 10 years of full operation (24h/7d). With the known actual switching frequency f_{sw} in kHz, the target lifetime in years, and the operation time in percentage of the total system lifetime, a normalized switching frequency is defined by the following formula:

Normalized f_{sw} = actual f_{sw} [kHz] × lifetime [yrs.] × operation time in percentage [%] ÷ 10 [yrs.]

With the estimated normalized switching frequency based on the actual application, the minimum turn-off gate voltage $V_{GS(off)}$ can be extracted from Figure 2 and Figure 3, respectively for turn-on gate voltage $V_{GS(on)}$ at 15 V and 18 V.

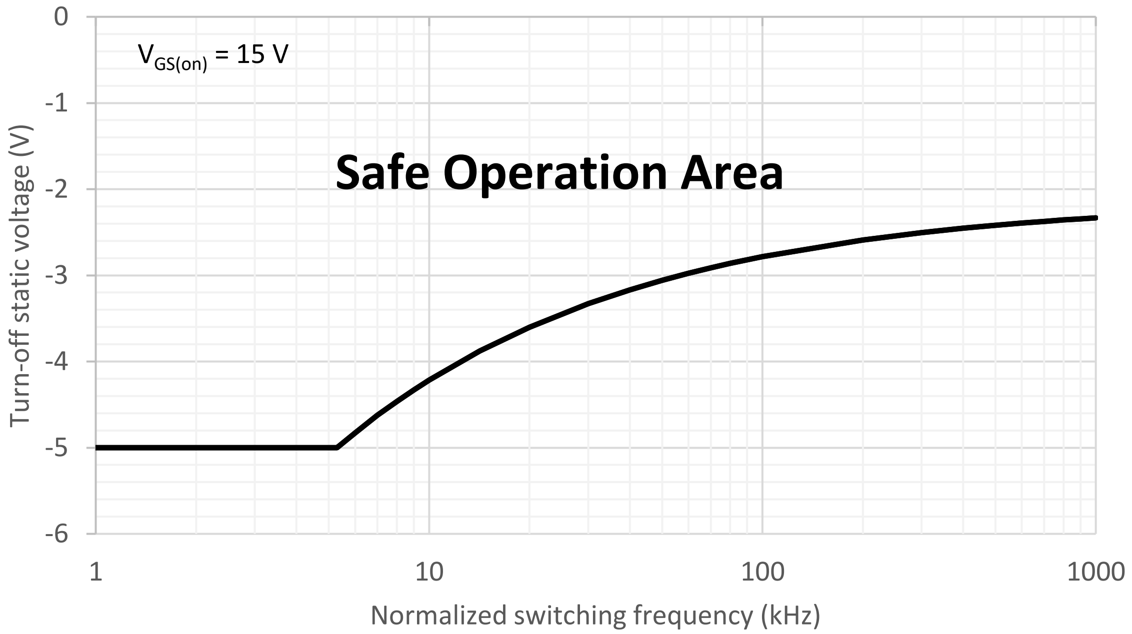

Figure 2 Minimum turn-off gate voltage $V_{GS(off)}$ with $V_{GS(on)}$ = 15 V

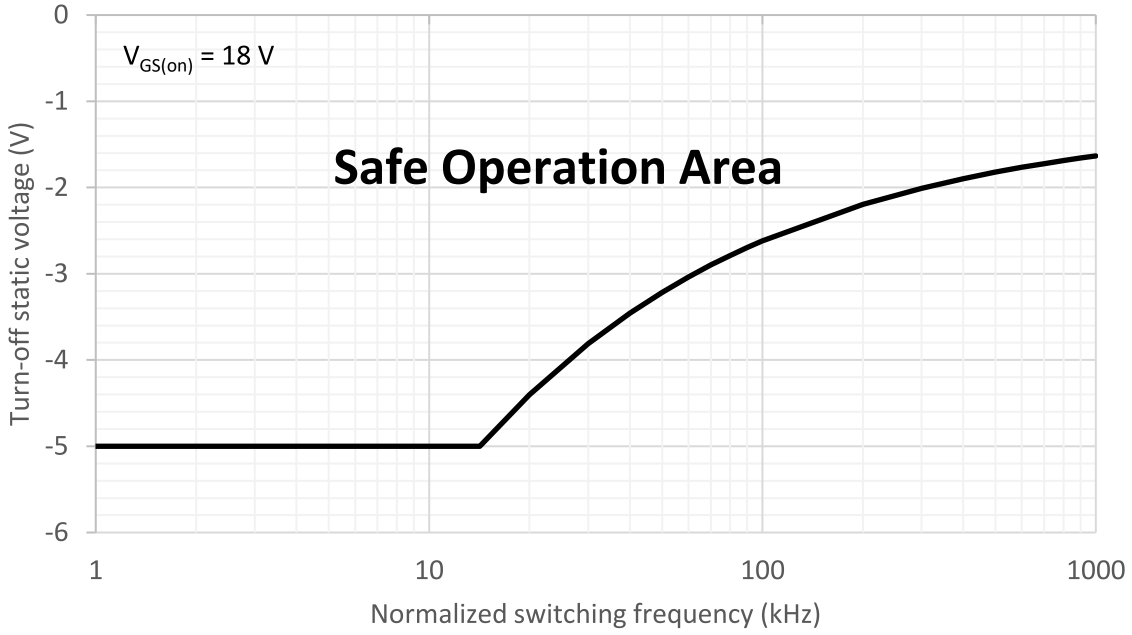

Figure 3 Minimum turn-off gate voltage $V_{GS(off)}$ with $V_{GS(on)}$ = 18 V

How to use this information is explained in the following example. A solar inverter has:

- an actual switching frequency of 20 kHz,
- a targeted lifetime of 20 years,
- operation time of 50%,
- a normalized switching frequency of 20 kHz * 20 yrs. * 50% / 10 yrs. = 20 kHz.

If the turn-on voltage is 15 V, the turn-off gate voltage has to be selected between -3.6 V to 0 V (see Figure 2). For the case of 18 V turn-on gate voltage, the selection has to be between -4.4 V to 0 V, as can be seen in Figure 3.

3.2 Definition of the safe operating area

The minimum turn-off voltage which defines the safe operating area is set to ensure that:

- the lowest recommended gate voltage is -5 V,
- the $R_{DS(on)}$ increases less than 15% of the initial value, at the end of target lifetime.

Hence, using the device within the safe operation area, the expected relative $R_{DS(on)}$ increase will be less than 15% at the end of a lifetime.

The relative increase of $R_{DS(on)}$ depends on the operating current I_d and junction temperature T_j (see Figure 4). Therefore the $R_{DS(on)}$ increase was considered for the most critical, yet realistic, operating conditions. This ensures that the $R_{DS(on)}$ increase at all other relevant operating conditions does not exceed 15%.The following conditions were chosen:

- high current: I_d at twice the nominal current I_{nom},
- intermediate temperature: T_j = 100°C.

Gate drive voltage guidelines

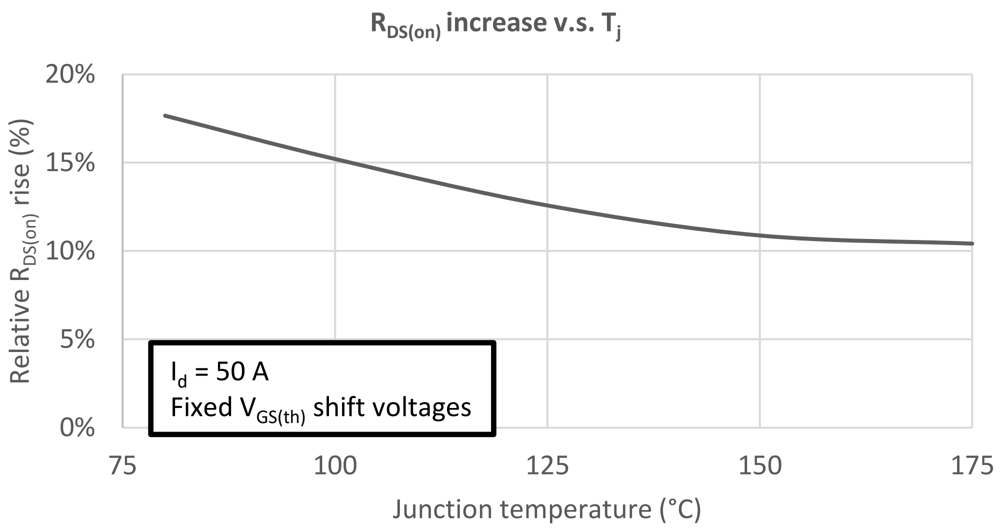

Figure 4 Relative $R_{DS(on)}$ increase at different junction temperature

In general, a 15% $R_{DS(on)}$ increase can be considered as a worst case increase. A higher relative increase is only possible with the combination of high current and low junction temperature operation, which is very rare in applications.

3.3 Notes for 18 V turn-on voltage

To be compatible with other devices, CoolSiC™ MOSFET can be used with 18 V gate voltage.

Please note, a turn-on gate voltage higher than 15 V has two opposing effects on $R_{DS(on)}$:

- it reduces the $R_{DS(on)}$,
- the $V_{GS(th)}$ drift effect is accelerated, meaning $R_{DS(on)}$ will increase faster over time.

For a relatively low switching frequency (approximately <50 kHz), the reduction of the $R_{DS(on)}$ effect dominates. However at a high switching frequency, a less negative turn-off gate voltage is needed to prevent an accelerated $V_{GS(th)}$ drift due to the 18 V turn-on voltage.

It should also be considered that the short circuit current is much higher compared with the 15 V turn-on voltage. Therefore the short current capability of the device, as stated in the datasheet, will be lost at 18V turn-on voltage.

3.4 Notes for less negative turn-off voltage

When operating at a less negative turn-off gate voltage (e.g. -2V instead of -5V), the impact on the application is minor. Several application-relevant parameters should be considered however:

- E_{on} and E_{off} will change slightly.
- The forward voltage of the SiC MOSFET body diode will be reduced.
- Increased risk of parasitic turn-on, which could increase the turn-on losses. This is especially relevant with 0 V turn-off voltage, large turn-off gate resistor and large gate-source loop inductance in the gate driver design.

[1] T. Aichinger, G. Rescher, G. Pobegen: Threshold voltage peculiarities and bias temperature instabilities of SiC MOSFETs; Microelectronics Reliability 80 (2018) 68–78.

Revision history

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Email: erratum@infineon.com

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