Application Note AN-1206

Reference Design for AUIRS2012S

By Cesare Bocchiola, Davide Giacomini

Table of Contents

<table>
<thead>
<tr>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Introduction &amp; Device Overview ............................................................... 2</td>
</tr>
<tr>
<td>Reference Board description ................................................................. 3</td>
</tr>
<tr>
<td>Reference Board Design &amp; Test Results ............................................... 6</td>
</tr>
<tr>
<td>Conclusions ........................................................................................... 13</td>
</tr>
<tr>
<td>References ............................................................................................ 13</td>
</tr>
<tr>
<td>Appendix: Reference Board Schematic and BOM ................................... 13</td>
</tr>
</tbody>
</table>

Paragraph annotation of the contents of this application note.
Introduction & Device Overview

This Application Note describes the AUIRDC2012, reference design for the AUIRS2012S automotive High Voltage High and Low side driver. It is intended to provide an exemplary design, including layout guidelines, and provides results for efficiency tests, as well as few typical measured waveforms.

The AUIRS2012S is an automotive qualified high voltage (200V) high and low side driver, in a compact SO-8 package and is intended to operate in many different automotive applications. One of them is step down (buck) or step up (boost) converters to convert 24V or 48Vdc battery to any voltage (example 12V) or vice-versa, with up several tens of A of output current and switching frequency up to several hundred kHz.

Typical simplified application diagram and main device characteristics are shown in figures 1 and 2.

![Typical Application Diagram](image)

**Product Summary**

<table>
<thead>
<tr>
<th>Topology</th>
<th>High &amp; Low Side Driver</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OS-MAX}$</td>
<td>200V</td>
</tr>
<tr>
<td>$V_{cc}$</td>
<td>10V – 20V</td>
</tr>
<tr>
<td>$I_{o+}$ &amp; $I_{o-}$</td>
<td>2 A</td>
</tr>
<tr>
<td>$t_{ON}$ &amp; $t_{OFF}$</td>
<td>60ns</td>
</tr>
<tr>
<td>Delay matching</td>
<td>20ns</td>
</tr>
</tbody>
</table>

![Main Device Characteristics](image)
Reference Board description

A pictorial view of the board is shown in Figure 3. It is very easy to use: it just needs an auxiliary power supply (10 to 20V, <10 mA), Vdc-IN and VOUT.

The board is basically configured as a step down converter, equipped with a PWM regulator running at fixed 200kHz (IRU3037CS) and regulating output voltage at 12V; by the way, the internal regulator may be by-passed and inputs for two complementary PWM signals are provided.

When operated by external PWM, Vdc-IN and VOUT can be exchanged between each other to achieve step-up (boost) functionality, provided the right jumpers configuration is previously set.

The board is equipped with a 10uA - 25A inductor, therefore inductor current above 25A shall not be forced.

Upon request, the board can mount two mosfets AUIRFS8403, 40V- 3.3 mOhm Max at Tj = 25C, for operation at 24V, or two mosfets AUIRFS9109E-7P, 100V-2.4mOhm Max at Tj=25C, for operation at 48V.
External PWM signals MUST be complementary to each other with a MIN suggested dead time of 100nsec. Their amplitude must NOT exceed 5Vpp (0 to 5V). Input signals of the AUIRS2012S are 3.3V CMos logic compatible.

Depending if operated by the internal IRU3037CS PWM controller, or by external PWM signals, the configuration of the jumpers SD,P3,P4,P5,P6 and of the connector P7 shall be as depicted in Table 1.

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Internal PWM</th>
<th>External PWM</th>
</tr>
</thead>
<tbody>
<tr>
<td>SD(P2)</td>
<td>After Vcc is applied, first short then open to let the controller start</td>
<td>X</td>
</tr>
<tr>
<td>P3</td>
<td>always closed</td>
<td>X, open if in Boost mode</td>
</tr>
<tr>
<td>P4</td>
<td>always open</td>
<td>X</td>
</tr>
<tr>
<td>P5</td>
<td>terminals 1 &amp; 2 shorted</td>
<td>terminals 2 &amp; 3 shorted</td>
</tr>
<tr>
<td>P6</td>
<td>terminals 1 &amp; 2 shorted</td>
<td>terminals 2 &amp; 3 shorted</td>
</tr>
<tr>
<td>P7</td>
<td>X</td>
<td>terminals 1 &amp; 2 PWM, terminal 3 GND</td>
</tr>
</tbody>
</table>

Because of the board layout, the hottest point during operation is the drain of the high side Fet (control Fet in step-down operation). Thermal characterization of the board has been performed with a T-type thermocouple soldered as indicated in figure 3.

IMPORTANT NOTICE: the reference design board is not equipped with current limiting or current protection or thermal protection. Therefore, damage may occur if thermal limits are exceeded, or if external PWM signals are not complementary to each other or if suggested minimum dead time is not introduced.

Layout plays a very important role when developing high frequency dc/dc converters, especially with power devices in SM technology. First of all, from a thermal point of view: the heat dissipation occurs via the pcb so as much as possible copper should be placed around mosfet drain terminals. Second, to reduce as much as possible pcb parasitics.

The exemplary layout of AUIRDC2012 is shown in figure 4. Some classical rules have been followed to generate such layout:

a) signal GND plane and power GND plane isolated between each other and connected to a single GND star point,
b) minimal superposition between pcb tracks interested by fast changing signals (like mosfets center tap) and GND power plane, to reduce parasitic capacitances,
c) ceramic capacitors between VDCIN and power GND are as close as possible to the control fet drain.
d) power stage pcb loop minimization
Copper thickness also plays a major role from a thermal viewpoint. Suggested copper thickness is 2oz/inch² (70um); this thickness is compatible with most manufacturing processes, by considering that the smaller clearance is dominated by the two SO-8 devices.

By the way, the thermal results described in the next paragraph have been achieved with 1oz/inch² (35um) copper thickness.
Reference Board Design & Test Results

While the reference design board can, as said, be used as step down or step up converter, the design was approached by considering the following specifications:

a) 24V operation:

Input voltage range: 16 to 32V  
Output voltage: 12 to 14V  
Output current: 3 to 15A  
Fsw: 100kHz to 200kHz  
Output voltage ripple: not critical (typical case of battery charging)  
Input EMI: not considered for this reference design

b) 48V operation:

Input voltage range: 40 to 56V  
Output voltage: 12 to 14V  
Output current: 3 to 15A  
Fsw: 100kHz to 200kHz  
Output voltage ripple: not critical (typical case of battery charging)  
Input EMI: not considered for this reference design

The minimum average output current to get continuous conduction mode is:

\[
I_{av,min}(Vin,Fsw) = 0.5 \cdot \left( \frac{Vo - \left( 1 - \frac{Vo}{Vin} \right)}{L \cdot Fsw} \right)
\]

At Vin=Vin,nom=24V, Vo=Vo,nom=12V, Iout=3A and Fsw=100kHz, L turns-out to be around 10uH.  
At Vin=Vin,nom=48V, Vo=Vo,nom=12V, Iout=3A and Fsw=100kHz, L turns-out to be around 15uH.  
For sake of simplification, a 10uH-25A inductor has been used in both operation modes.

The reason to stay in CCM as much as possible is that this reference design does not have provisions to block the output inductor current when it becomes negative (average output current below the mask of figure 5, that is at low frequency, high inductor current ripple, low average output current). This introduce efficiency penalty at light load (DCM) conditions.  
For switching frequencies between 100 and 200kHz, and for Vout=12V, the minimum current to stay in CCM can be mapped as shown in figure 5 (24V) and figure 6 (48V).

Because output voltage ripple is not critical and EMI specifications not considered, input and output capacitor's design is mostly related to their self-heating due to input and output current ripples.
Worst case output current ripple is at Fsw=100kHz and Vin=56V
It turns out to be:

\[ I_{L,\text{ripple, max}} = 9.4A \]

Actually, what is important is the RMS value of such current. For a triangular waveform, it is:

\[ I_{L,\text{rms, max}} = \frac{9.4A}{\sqrt{3}} = 5.43A \]

Input rms current ripple is maximum at maximum output current and minimum input voltage
(24V design with Vin=16V, Vo 12V and Io=15A); as a first approximation

\[ I_{in,\text{rms, max}} = 13A \]

In worst case, all this ripple is filtered by the input capacitor, which needs to have very low ESR. The capacitors used in this reference design are 470uF, 50V, 30mOhm ESR and 105°C.

At Io=15A and Vin=48V, the output capacitor will dissipate less than 1W, and the input capacitor will dissipate less than 2W.
Different is the case for the 24V design, where the capacitor’s losses may reach almost 5W. Then, lower ESR and/or multiple input capacitors in parallel need to be considered for a reliable 24V design.

Let’s now move to some test results for the two reference designs.

a) 24V design.

First of all, efficiency of the whole board, with Vin = 24V, Vout = 12V (step-down mode), versus output current. This is shown in Figure 7, for different switching frequencies.

![Figure 7: board efficiency vs Iout at different Fsw](image)

Figure 8 show the pcb temperature (at the reference point shown in figure 3) versus current and Fsw.

![Figure 8 : Tpcb versus Iout and Fsw](image)

Efficiency at very low currents is higher at higher frequency simply because the inductor current ripple is lower (then at higher frequency the inductor current becomes fully positive earlier).
For reference, Vs and Vout ripple have been recorded at 200kHz, 14A and 250kHz, 10A. They are shown in figures 9 and 10.

**Figure 9:** Vs and Vout ripple at 200kHz, 14A

**Figure 10:** Vs and Vout ripple at 250kHz, 10A
b) 48V design:

Again, efficiency of the whole board, with \(\text{Vin} = 48\,\text{V}, \text{Vout} = 12\,\text{V}\) (step-down mode), versus output current is shown in Figure 11, for different switching frequencies.

![Figure 11: board efficiency vs Iout at different Fsw](image)

Figure 11: board efficiency vs Iout at different Fsw

Figure 12 show the pcb temperature (at the reference point shown in figure 3) versus current and Fsw.

![Figure 12: Tpcb versus Iout and Fsw](image)

Figure 12: Tpcb versus Iout and Fsw

Now, efficiency in all the measured current range is lower at higher frequency: even if the inductor current ripple is lower at higher frequency, the higher switching losses due to higher \(\text{Vin}\) operation compensate for that.
For reference, $V_s$, $V_{gs}$ (synch Fet) and $V_{out}$ ripple have been recorded at 200kHz, 10A. They are shown in figures 13 and 14.

Figure 13: $V_s$ and $V_{gs}$ (synch Fet) at 200kHz, 10A

Figure 14: $V_s$ and $V_{out}$ ripple at 200kHz, 10A
Conclusions

The AUIRDC2012 reference design board provides a simple, while quite optimised, example how using the AUIRS2012S to implement a high output current step-down or step-up dc/dc converter for automotive applications, at both 24Vin and 48Vin.

References

AUIRFS8403 Data Sheet, www.irf.com
IRU3037CS Data sheet. www.irf.com
Circad PCB, Omnigliph 6.0B, 2012
Mathcad 11 is a registered trademark by PTC.

Appendix: Reference Board Schematic and BOM

IC1  AUIRS2012S
IC2  IRU3037CS
C1,C2  1uF 50V
C3  470nF 50V
C4,C5  100uF 20V - low ESR
C7  100nF 50V
C8,C9,C10  4.7uF 50V
C11  470uF - 50V - low ESR
CB  470pF 50V
CC1  4.7nF 50V
CC6  100pF 50V
D1  SK 14B
M2,M3  IRFS8403
D4  BYG20J (o DL4937)
D5  Led, miniature
D6,D7  Zener diode, 5.1V, 500mW
D8,D9  1N4148
Pin,Pout  Pcb connector, 2 poles, 10.16mm
P1  Pcb connector, 2 poles, 5.08mm
L1  10uH - 25A
P2 to P4  2-pin Single in-line header
P5 to P7  3-pin Single in-line header
R1,R3  47 Ohm
R2,R4  4.7 Ohm
R5  3.3 Ohm
R6  10 kOhm
R7  4.7 kOhm
R10,R11  470 Ohm
RB  15 kOhm
RC1  20 kOhm
RDOMM  18 kOhm
RUP  150 kOhm