Innovative top-side cooled package solution for high-voltage applications

Application considerations for best performance

About this document

Scope and purpose

This application note shows the benefits of using top-side cooled (TSC) power devices in high-voltage (HV) applications. In addition, it should help designers of such applications to understand how the device can be used and how an efficient and easy-to-assemble approach can be chosen to integrate TSC devices into the system. This application note describes Infineon's new heat-spreader dual small outline package (HDSOP) family, which consists of TSC surface-mount devices (SMDs) designed for HV applications.

The document explains the advantages of TSC and shows the different assembly methods and thermal stacks and their influence on thermal performance. It also addresses the different manufacturing challenges a hardware designer must consider when using TSC packages.

The following information is a guideline for use and should not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

Intended audience

System and hardware development engineers in the field of high-power/HV applications such as onboard chargers, SMPS, drive applications, etc. who want to understand the advantages and challenges of the TSC approach or who already use TSC in their applications. The application note is aimed at the automotive and industrial space.

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1 Introduction

TSC devices are surface-mounted power devices that are soldered onto a printed circuit board (PCB). The generated heat of the semiconductor die is extracted to the top side of the package to the attached coldplate. Thereby the thermal path is decoupled from the electrical connections and the PCB itself. The top side of the package has an exposed pad to dissipate the generated heat. **Figure 1** shows schematically the TSC package approach assembled on a PCB and attached to a coldplate.

Applying the TSC approach also brings various challenges to be solved on a system level. If the mechanical challenges are addressed, the TSC system is a superior device concept that can help to solve system problems. With TSC designs the power density is significantly increased, power dissipation is improved, manufacturing is simplified and electrical performance is improved.

In reality, not all TSC packages will have the same distance from package top to coldplate due to manufacturing decisions. Therefore, the height tolerances must be balanced with some kind of thermal interface material (TIM).

In the following chapters the TSC package family will be introduced and possible assembly methods are explained. An experiment was done to show the thermal performance of different assembled boards.

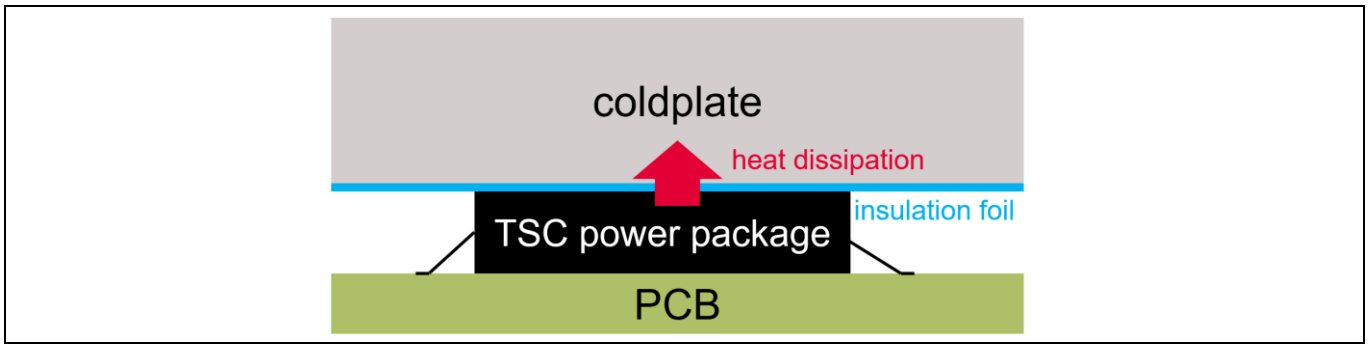


Figure 1 TSC package concept

2 Advantages of top-side cooled devices

2.1 Definition of “thermal performance”

In the context of this application note, “thermal performance” is measured as thermal resistance (R_{th}) in Kelvin per Watt (K/W). The lower this value is, the better the thermal performance.

Generally, the thermal resistance per area of the interface material depends on its thermal conductivity and the thickness of the material. The contact resistance is an additional contributor, which is material and surface dependent.

Consequently, the equivalent R_{th} can be summarized as:

$$R_{th} = R_{contact} + R_{th\_material\_thickness} \qquad (1)$$

The contact resistance ($R_{contact}$) is material dependent and can be reduced by applying a higher force between the coldplate and the power package. This will improve the conformity of the TIM to the contact surfaces and thus reduce the contact resistance. Nonetheless, a high force on the semiconductor could stress the solder joints of the semiconductor components and therefore deteriorate the reliability of the joints.

Note: *For the Infineon TSC package the effect of long-term force stress on the package has been analyzed thoroughly – the results of force stress vs. temperature-cycling onboard show that a force of up to 100 N has no visible impact on the reliability up to 3700 temperature cycles. Details of this investigation are available in* ***Chapter 3.3****.*

The second part of the equation ($R_{th\_material\_thickness}$) depends purely on the conductivity and the thickness of the material, and can be represented as:

$$R_{th\_material\_thickness} = \frac{TIM\_thickness}{TIM\_therm\_cond} \qquad (2)$$

A graphical representation of these formulas is given in **Figure 2**.

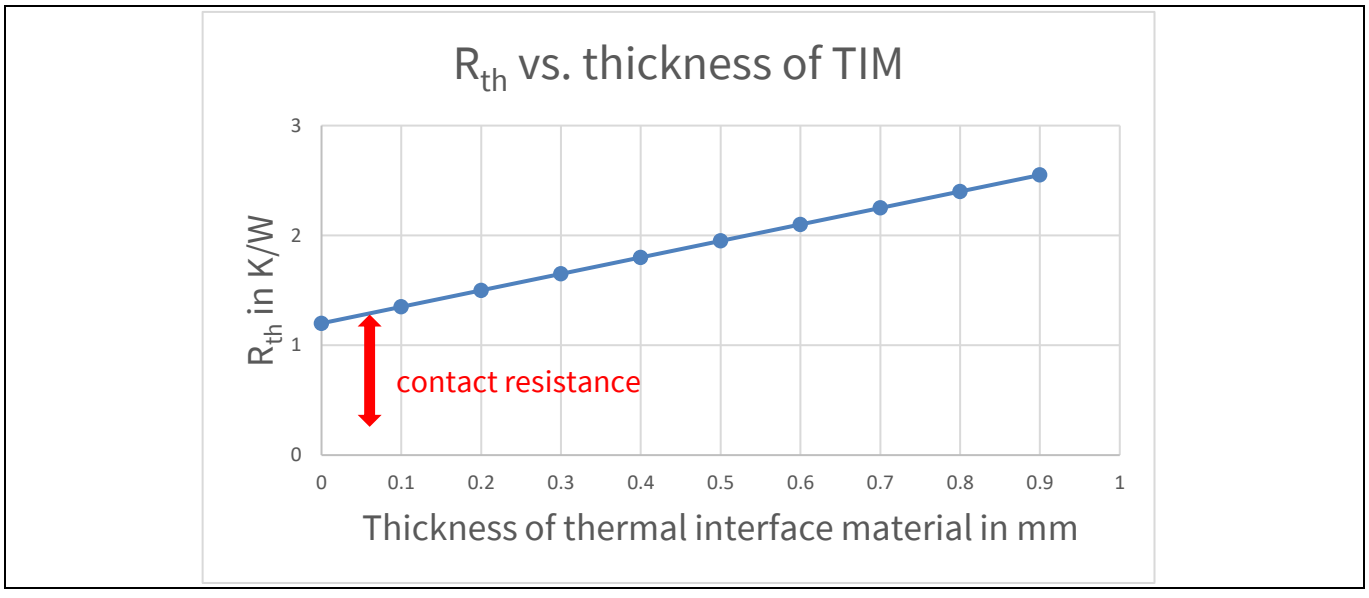


Figure 2 Thermal resistance (R_{th}) vs. thickness (with constant contact resistance)

2.2 Comparison to through-hole devices

Through-hole devices (THDs) like the TO-247 or TO-220 package are still dominant in a number of applications. However, these devices suffer from high manufacturing costs, as they need to be manually inserted into the PCB and soldered onto the bottom side via wave soldering or manually. For this reason, through-hole technology is increasingly being replaced with surface-mount technology (SMT), a standard process in the electronics industry that has several advantages. The automatized placement of SMDs results in higher throughput combined with increased reliability, which in turn reduces system cost. More details on the differences of THT and SMT are described in **[3]** and are therefore not investigated further in this application note.

2.3 Comparison to bottom-side cooled devices

Both TSC and bottom-side cooled (BSC) devices can be assembled with automated pick-and-place machinery. The TSC package family has many advantages compared to a BSC SMD package variant (like D2PAK or DPAK). But first, it is important to distinguish between BSC on FR4 PCB and insulated metal substrate (IMS) board.

Common cooling approaches are shown in **Figure 3**.

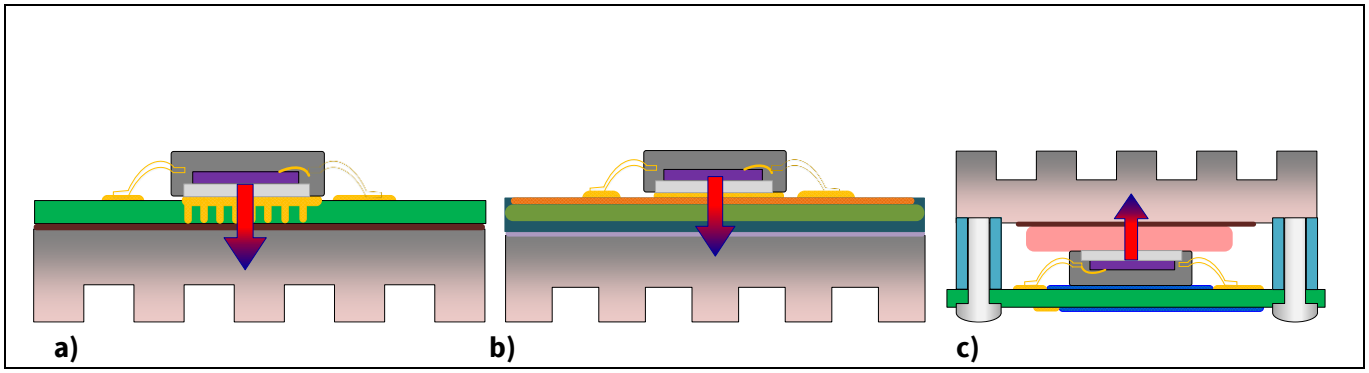


Figure 3 Common cooling concepts for SMD devices: a) BSC approach on FR4 PCB with thermal vias; b) BSC design on IMS board; c) TSC with double insulation approach (gap filler and insulation foil)

When comparing the performance of the TSC vs. BSC on FR4 PCB, the thermal performance of the TSC is improved, as the thermal resistance of the thermal stack from chip to coldplate is reduced. PCBs are not optimized for heat conduction and create a substantial thermal barrier for a SMD device placed on such a board. The designer must improve the thermal dissipation by placing thermal vias in the PCB. But even with optimized thermal design, the thermal resistance is higher in comparison to TSC, as the results from 3D FEM simulations indicate in **Figure 4**. The graph shows that the thermal resistance from junction to coldplate is reduced by 30 percent when comparing BSC on FR4 PBC to TSC. In addition, the routing on the PCB is much more challenging for BSC, as large areas of the PCB are lost to thermal dissipation design elements. By decoupling the electrical and thermal paths, as is done with TSC, the PCB design becomes much easier and more flexible. Potential gains as a result of PCB area reduction and EMC noise mitigation can be expected.

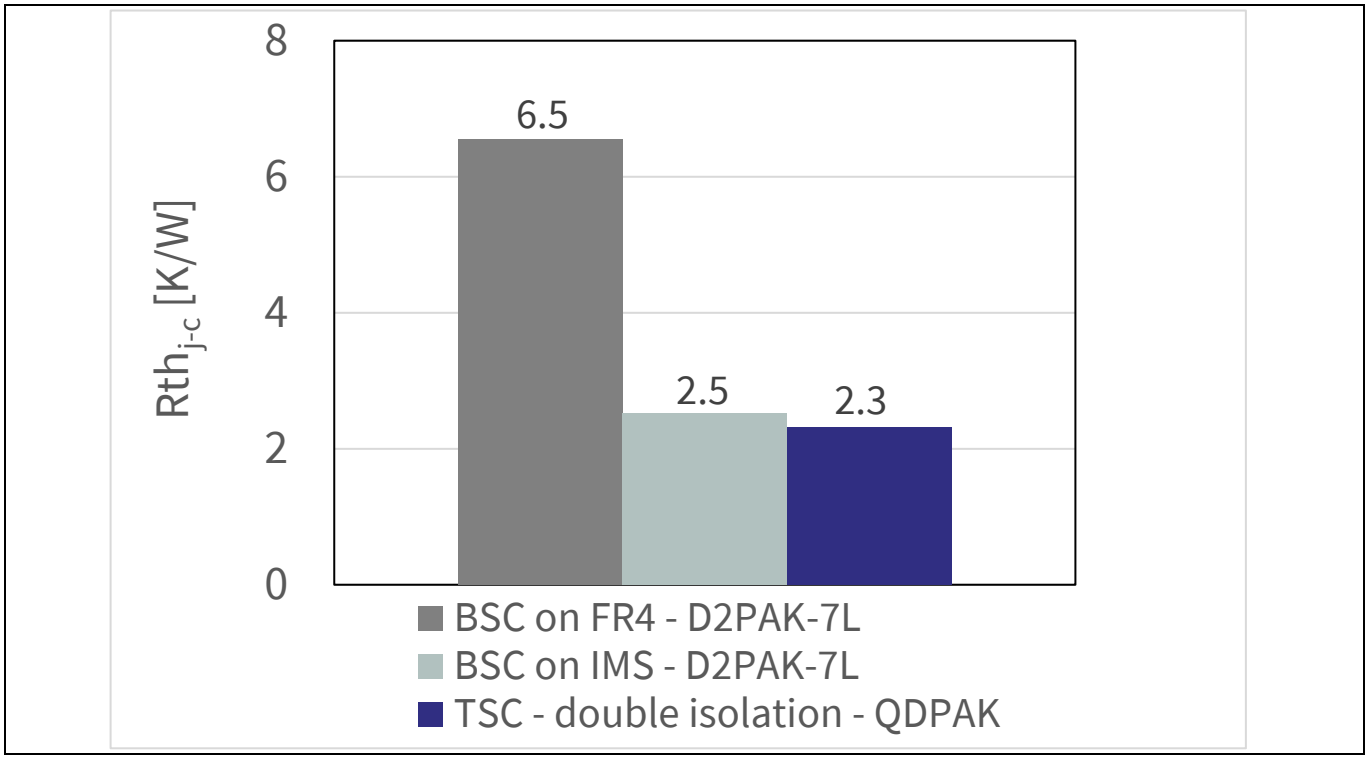


Figure 4 Thermal simulation of Rth$_{j-c}$ (junction to coldplate) for different cooling concepts: BSC on Fr4 PCB with D2PAK-7L, BSC on IMS with D2PAK-7L and TSC with double insulation (gap filler: 5.1 W/(m·K), 200 µm, insulation foil: 0.46 W/(m·K), 70 µm)

When comparing BSC on IMS to a TSC solution, the difference in thermal performance is not the key differentiator. The simulation also shows that for a single-layer IMS board with 50 µm copper similar thermal results can be achieved as for TSC with gap filler material and insulation foil. The main advantage when compared to BSC on IMS is the reduced PCB cost and reduced space required. The IMS board is thermally very accommodating, but also quite costly. With the TSC solution, the expensive IMS can be replaced by a lower-cost FR4 PCB solution while maintaining the very low thermal resistance path from junction to coldplate.

As the IMS board is so costly, only the high-power components are placed on the IMS board, whereas all other electrical components are customarily placed on standard FR4 PCBs and then connected to the IMS. Because these connections are unnecessary when using TSC, the switching cell-loop design can be improved, as both sides of the PCB can be used for routing. The gate driver, for example, can be placed directly above the switch on the other side of the PCB. Therefore, the gate- and power-loop parasitics are reduced, resulting in better and more precise gate control and, in turn, less ringing, higher performance and a smaller risk of failures.

One major advantage of TSC compared to BSC on IMS or FR4 PCB is the increased power density. The usable PCB area is doubled for TSC as the coldplate is not directly attached to the PCB and the heat is not conducted through the PCB. This is indicated in **Figure 5**, where the increased power density is shown schematically. By using TSC packages, one additional layer of the PCB can be used to populate devices, virtually doubling the power density of the assembly.

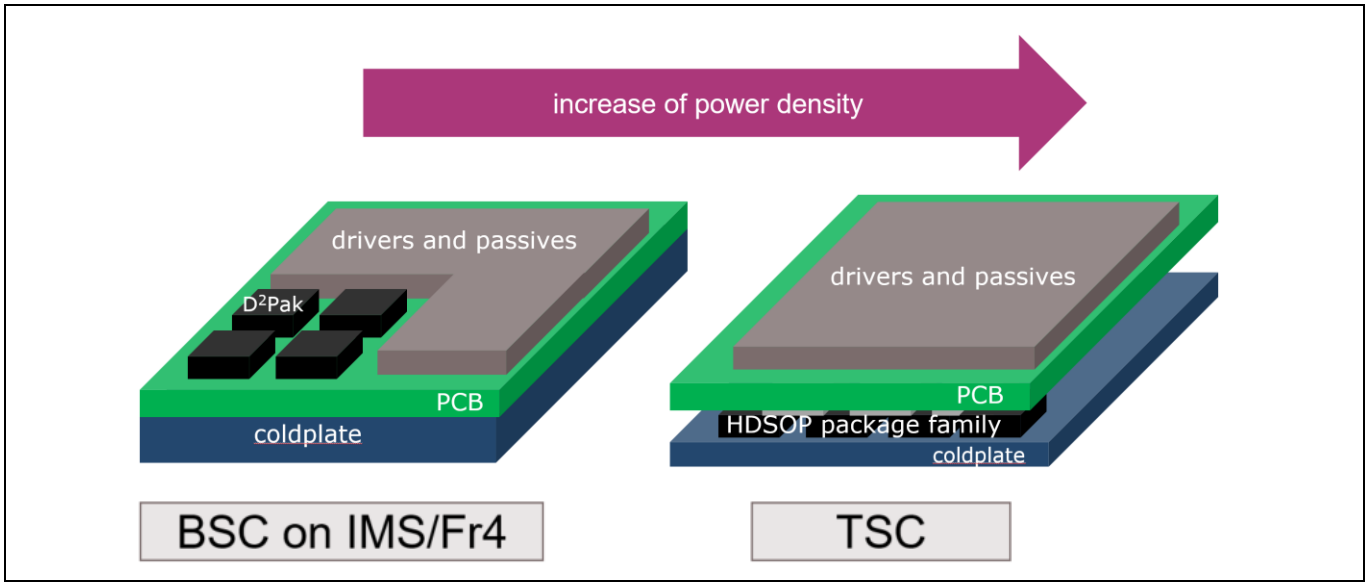


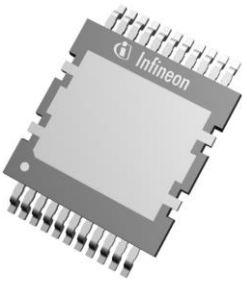
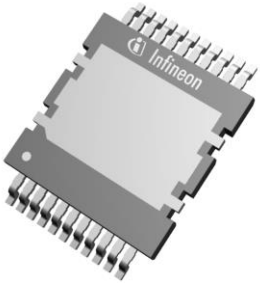
Figure 5 Power density increase of TSC approach

3 HDSOP package family

3.1 Package family overview

Infineon is introducing the HDSOP package family for HV devices above 600 V. In **Table 1**, the already released packages in this family are summarized, with the key package information. One parameter they all have in common is the package height of 2.3 mm. This standard height makes it possible to mix different discrete devices, such as a 650 V SiC diode and LV and HV MOSFETs and attach them to one common coldplate. The TSC packages of Infineon's LV MOSFETs are not included in the overview in **Table 1**. The assembly process is optimized and the distance from the coldplate to the package top side is the same for all power devices populated on the PCB. This reduces the efforts of assembly, and a special structuring of the coldplate is not necessary.

Table 1 HDSOP package family details

Package identifier	Package name	Drawing
PG-HDSOP-10-1	DDPAK	
PG-HDSOP-22-1	QDPAK	
PG-HDSOP-22-2	QDPAK	

3.2 Positive standoff

The TSC HDSOP family for HV applications comes with the industry standard of a positive standoff, shown in **Figure 6**. The package body is up to 150 µm higher than the lower edge of the package leads. One benefit of the positive standoff is that a standard stencil height for reflow soldering can be used. The device only needs to be picked up and placed on the PCB, before the devices can be soldered via reflow soldering. With a positive standoff, no extra board cleaning is required before the SMD device is placed on the PCB for reflow soldering. This enables direct contact between the pins and the solder stencils.

The package can also be fixed with an adhesive material (e.g., SMD glue) to the board, enabling a rigid assembly and double-sided component soldering.

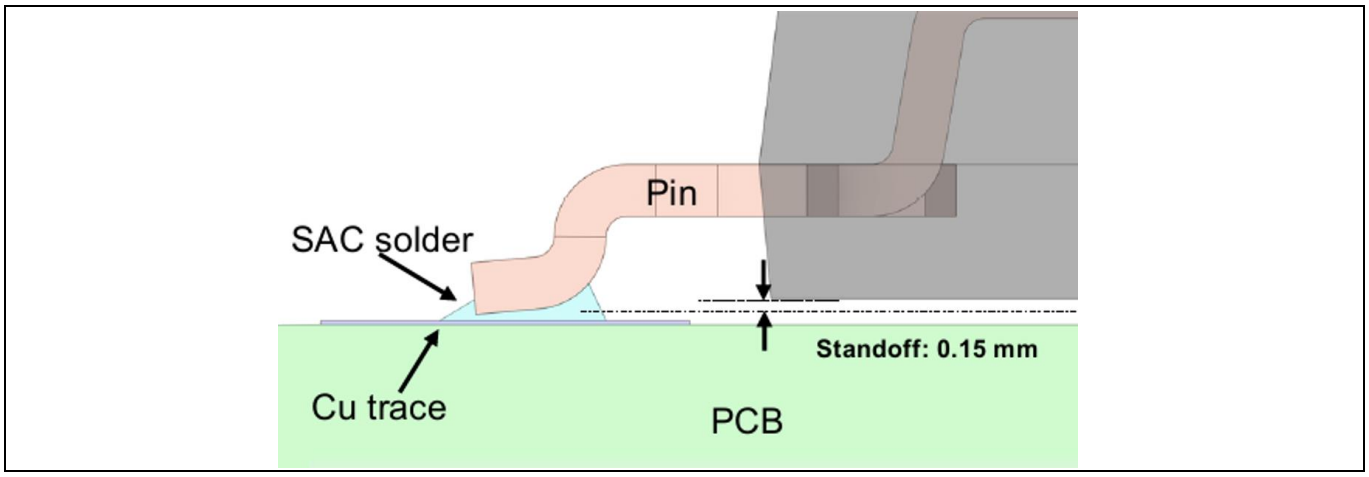


Figure 6 The QDPAK (HDSOP-22-1 package) offers a positive standoff of 150 µm (nominal)

3.3 Reliability of HDSOP packages

Infineon's application note "600 V CoolMOS™ G7 and 650 V CoolSiC™ G6 come in a new top-side cooling package – the DDPAK" [1] shows the results of reliability investigations done for the HDSOP-10-1 (DDPAK), which is one member of the HDSOP package family. In Chapter 4.3 of this application note, the temperature-cycling on board (TCoB) was studied for the DDPAK. TCoB tests were performed for devices which were soldered on four-layer PCBs. No electrical failure or optical abnormalities were observed for over 2000 temperature cycles [1]. In addition to the TCoB tests, some mechanical tests were also performed to investigate the compression reliability of the DDPAK (Chapter 4.4 of [1]). Devices were soldered onto a PCB and pressure was applied and successively increased until device failure. With this test the maximum allowed force can be achieved. No failures were observed for forces up to 2500 N.

By applying a pressure force on top of the device, the leads act as springs and the package body is pressed down to the PCB level. This unique feature of the device results in very high mechanical stress resistance [1].

Similar investigations were also performed for the QDPAK package to prove the reliability for other members of the package family. Two different investigations were performed in parallel. One set of boards was prepared with devices soldered onto a standard FR4 PCB. Another set of boards was additionally stressed with 100 N per package. A pressure force was applied on top of the devices after soldering onto a PCB. Afterward, TCoB investigations were conducted for both setups to identify the influence of an applied force on the TCoB robustness of the packages. Depending on the chosen coldplate, a force can be necessary to press the device against the coldplate. Detailed information on the different thermal stacks is given in **Chapter 4.1**. In **Figure 7**, the solder joints of both variants are shown. It is clearly visible that the additional force on the package does not change the solder joint connection, and no stress is directly imprinted. The leads of the package act like springs and take the applied force. The lead is deformed in the shoulder region of the package. The subsequent device investigations showed that the solder joints after temperature-cycling are more stressed than the devices without any load applied. Nevertheless, no failures were observed for either setup for TCoB cycles for far more than 2000 cycles, proving very high reliability and mechanical stability for both; devices without load but also with 100 N applied. This very good TCoB reliability can be attributed to the spring-like behavior of the package.

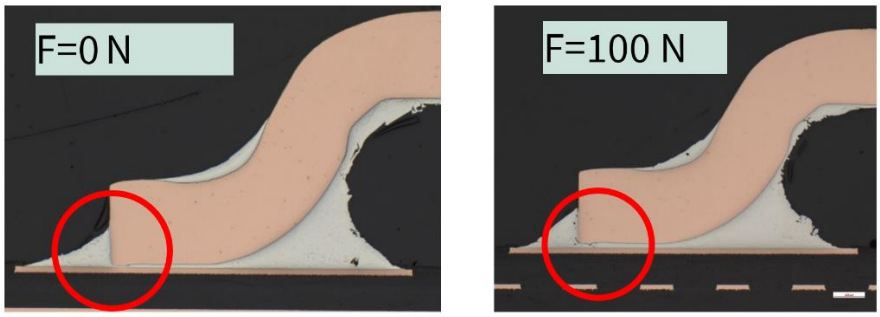


Figure 7 Solder joint without and with applied force of 100 N: no impact on solder joint is visible

4 Assembly methods

This chapter shares best practice examples of how TSC packages can be attached to a common coldplate. The design goal is to maximize the thermal performance while ensuring proper electrical insulation. Therefore, an interface material between the exposed metal pad of the HDSOP power packages and the heatsink is needed. This TIM has the task to conform well to the power package and the coldplate and thus avoid any air voids. These air voids cause several problems. First, air is a very bad thermal conductor and thus the thermal performance will deteriorate. Second, air voids are problematic in terms of insulation and creepage requirements and reliability. Therefore, voids must be avoided as much as possible to achieve high performance and long-term reliability.

Note: Generally, attaching small TSC packages to individual heatsinks is relatively easy, because mechanical tolerances do not need to be considered. Therefore, the individual heatsink mounting for single packages is not covered here. Further information about individual heatsink mounting is available in [1].

4.1 Thermal interface materials

Table 2 gives an overview of common classes of electric non-conductive TIMs.

Table 2 Thermal interface materials

Identifier	Consistency	Contact pressure	Comment
Gap filler pad	Solid (silicone or acrylic)	High	Can be fiberglass enforced
Liquid gap filler	Liquid paste that becomes solid after curing	No pressure needed	Often messy, but dispensation can be automated
Phase-change materials	Solid (at room temperature)	Low	Sticky material, changes from solid to half-liquid state at the specified temperature to fill air gaps

Typical electric and thermal conductive materials are greases, which are excluded in this research as their capacity for providing isolation is very limited.

4.1.1 Gap pad

Gap pads are pre-cured silicone and ceramic powder materials.

Gap pads have a high contact resistance because they do not conform well to their environment without significant force being applied. Therefore, a permanent force needs to be guaranteed over their operating life to achieve good thermal performance.

Gap pads exhibit higher operating temperatures, and they are also more stable than phase-change products.

4.1.2 Liquid gap filler

Liquid gap filler materials can be applied by imparting nearly zero force to the connected component.

They conform very well to different geometries while filling grooves, air voids and surface roughnesses due to their liquid state, and thus achieve excellent thermal performance. These materials are cured in place to become solid. State-of-the-art liquid gap fillers offer thermal conductivities of up to 7 W/(m·K) [14].

4.1.3 Phase-change material

Phase-change materials are solid at around room temperature and become liquid as the temperature increases during operation. Their advantage is that they offer much easier handling in production (because they are solids when they are installed). They are available as isolating or non-isolating materials and need only a low pressure for good thermal performance. The drawback of these materials is that they can only compensate narrow mechanical tolerances (up to 100 µm).

4.2 Experimental results

The goal of the experimental measurements was to benchmark different assembly methods and different materials against each other. The thermal resistance from the junction to the coldplate is used as a benchmarking parameter.

4.2.1 Description of the test PCBs

The test boards contain eight QDPAKs under a common coldplate fixed with spring-loaded push-pins with different interfaces in between (**Figures 9** to **12**). Electrically, each MOSFET can be driven separately via jumper settings, as shown in **Figure 8**.

To have a defined gap between the component and the coldplate, distance spacers were plugged on the push-pins for some boards, as shown in **Figure 9**. The vertical force on the QDPAK is a result of the board stack and the springs chosen. The force in this setup was defined at 20 N per package and is calculated considering the free height and the spring force.

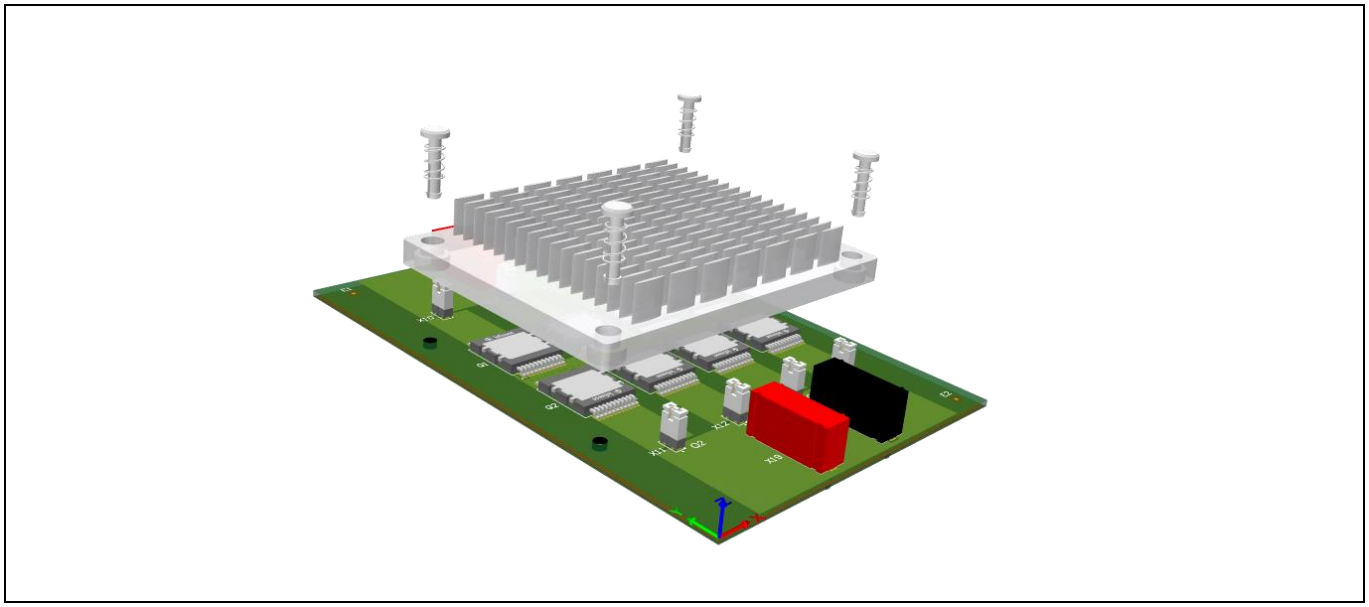


Figure 8 QDPAK test board

Table 3 Test board configurations

Board no.	Interface	Manufacturer	Type	Thermal conductivity	Comment
4	Liquid gap filler	Shin-Etsu	SDP-5040A/B	5.1 W/(m·K)	Spring-mounted without distance holders
18	Gap pad	Henkel	TGP HC 5000	5.0 W/(m·K)	Spring-mounted without distance holders

Board no.	Interface	Manufacturer	Type	Thermal conductivity	Comment
24	Liquid gap filler	Kerafol	GFL 3020	1.8 W/(m·K)	Spring-mounted without distance holders
26	Liquid gap filler	Hala	TDG-U-SI-2C	3.6 W/(m·K)	Additional mounting of isolation foil: Hala dielectric film TFI-KMT-A2 (0.46 W/(m·K); 70 µm thickness) Additional distance holder at coldplate to guarantee minimum distance
40	Liquid gap filler	Henkel	TGF 3600	3.6 W/(m·K)	Spring-mounted without distance holders

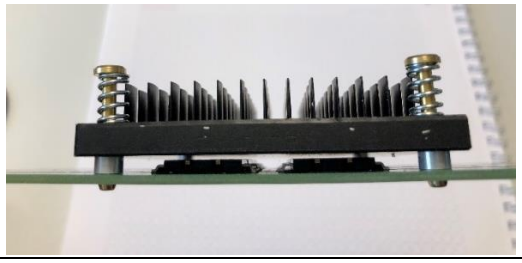


Figure 9 Mechanical mounting method with distance holders (TIM not applied yet)

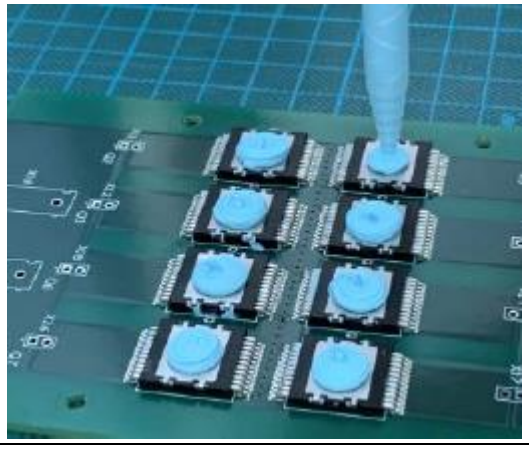


Figure 10 Dispensing of liquid gap filler

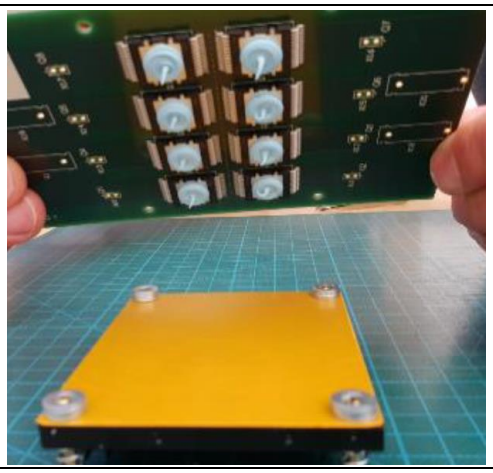


Figure 11 Assembly of board #26 (liquid gap filler with additional isolation foil and distance holders)

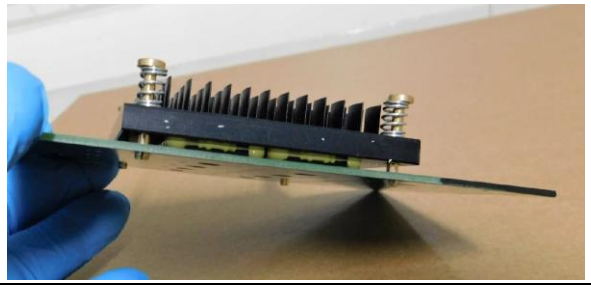


Figure 12 Final assembly of board #24 (liquid gap filler as TIM, spring-mounted coldplate without additional distance holders)

4.2.2 Thermal performance results

Experiments were performed to obtain the indicator for the thermal performance from chip junction to coldplate ($R_{th\_j\_cp}$) for each solution.

The temperature behavior of a P-N junction to determine the junction temperature of the semiconductor switch [7] is used for the MOSFET body diode.

The first step is to calibrate the forward voltage of the body diode over the temperature in steady-state conditions with a constant current source. This was performed by using a climate chamber to control the ambient temperature while measuring the diode forward voltage. The forward voltage was measured for four switches on each PCB to evaluate the variation of the R_{th} results.

Exemplary results for switch Q1 on PCB #40 are shown in **Figure 13**.

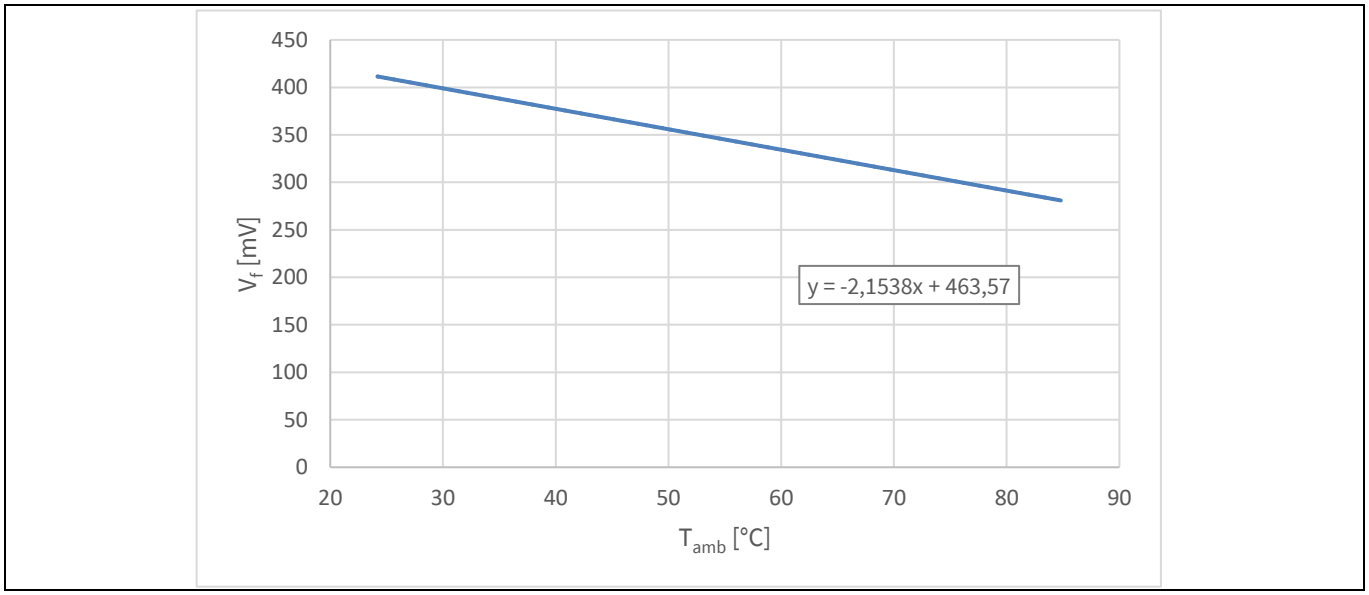


Figure 13 Diode forward voltage vs. temperature on test board #40

The second step was to measure the actual $R_{th\_j\_cp}$ value. Therefore, a known power was dissipated within the semiconductor switch while the coldplate temperature was measured in thermal steady-state. To ensure constant environmental conditions of the coldplate, an enclosure was used to prevent significant convection. Subsequently, the power was turned off and the voltage drop of the diode was measured immediately afterward.

Next, the junction temperature of the semiconductor chip was determined using the calibration data.

The next step was to calculate the actual $R_{th\_j\_cp}$ values. **Table 4** and **Figure 14** summarize these results. The results are explained in **Section 4.3**.

Table 4 R_{th} [K/W] results – test boards

Board no.	$R_{th\_j\_cp\_averaged}$	$R_{th\_j\_cp\_Q1}$	$R_{th\_j\_cp\_Q4}$	$R_{th\_j\_cp\_Q7}$	$R_{th\_j\_cp\_Q8}$
4	1.5	1.5	1.5	1.5	1.5
18	2.2	3.2	2.5	2.0	2.5
24	1.7	1.8	1.9	1.8	1.8
26	4.3	4.2	4.4	4.5	4.4
40	1.6	1.6	1.6	1.6	1.6

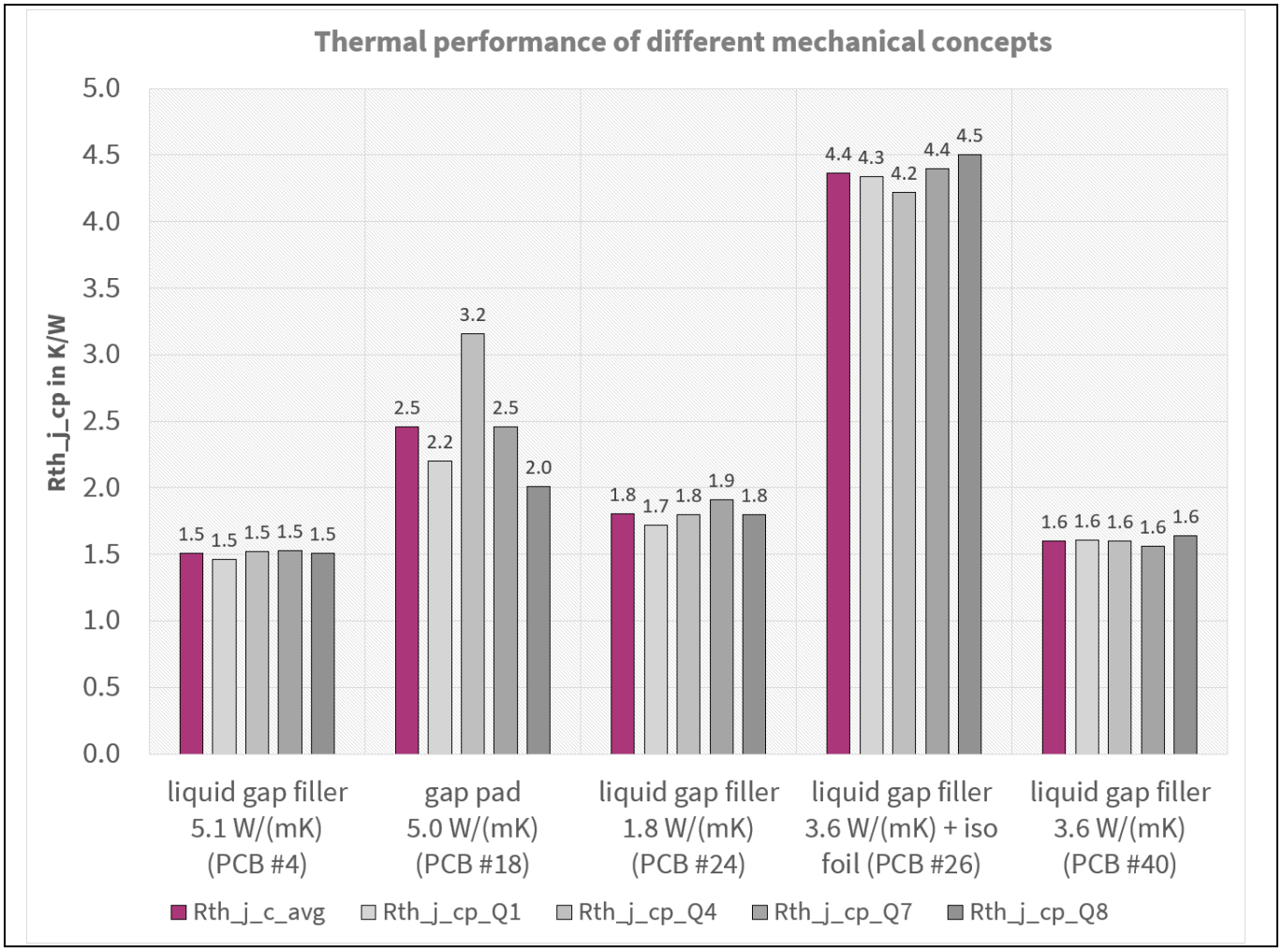


Figure 14 Results of the lab experiment showing the average thermal resistance from semiconductor junction to coldplate for different boards, and the $R_{th\_j\_cp}$ measured for the different power switches (Q1, Q4, Q7 and Q8)

4.2.3 Interface thickness

The thickness of the TIM is a key design parameter. The thinner it is, the better the thermal performance. Therefore, it is important to minimize all mechanical tolerances in the Z-direction (which must be compensated by the TIM eventually). On the other hand, the thinner the TIM gets, the less isolation it will provide. Consequently, it is important to guarantee a minimum distance of the TIM by mechanical means (such as distance holders) because this will also guarantee the minimum electrical isolation strength.

The thicknesses of the individual TIM layers of the test boards were analyzed via a 3D optical scan of the surfaces. These results are shown in **Figure 15**, **Figure 16** and **Figure 17**. Based on this measurement, the maximum thickness of the TIM for the different test boards was extracted, yielding ~160 µm for PCB #24 and ~220 µm for PCB #40, ~270 µm for PCB #4 and 1.5 mm for PCB #26.

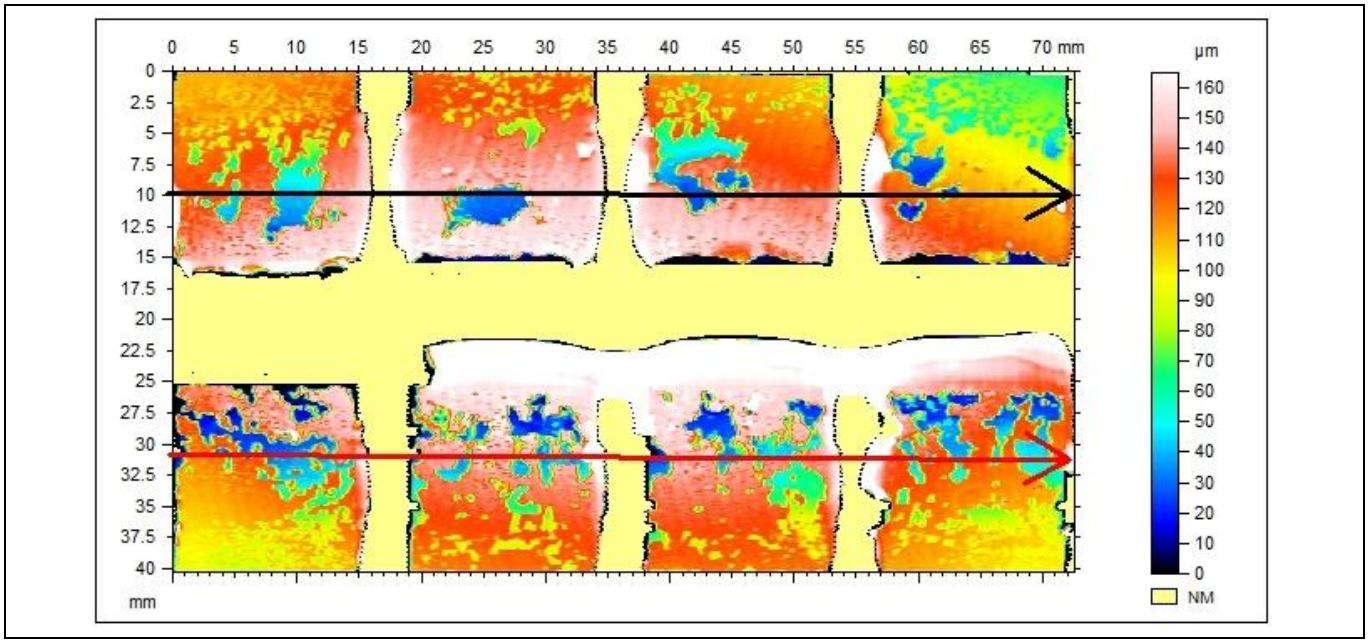


Figure 15 3D optical surface measurement of the TIM of board #24

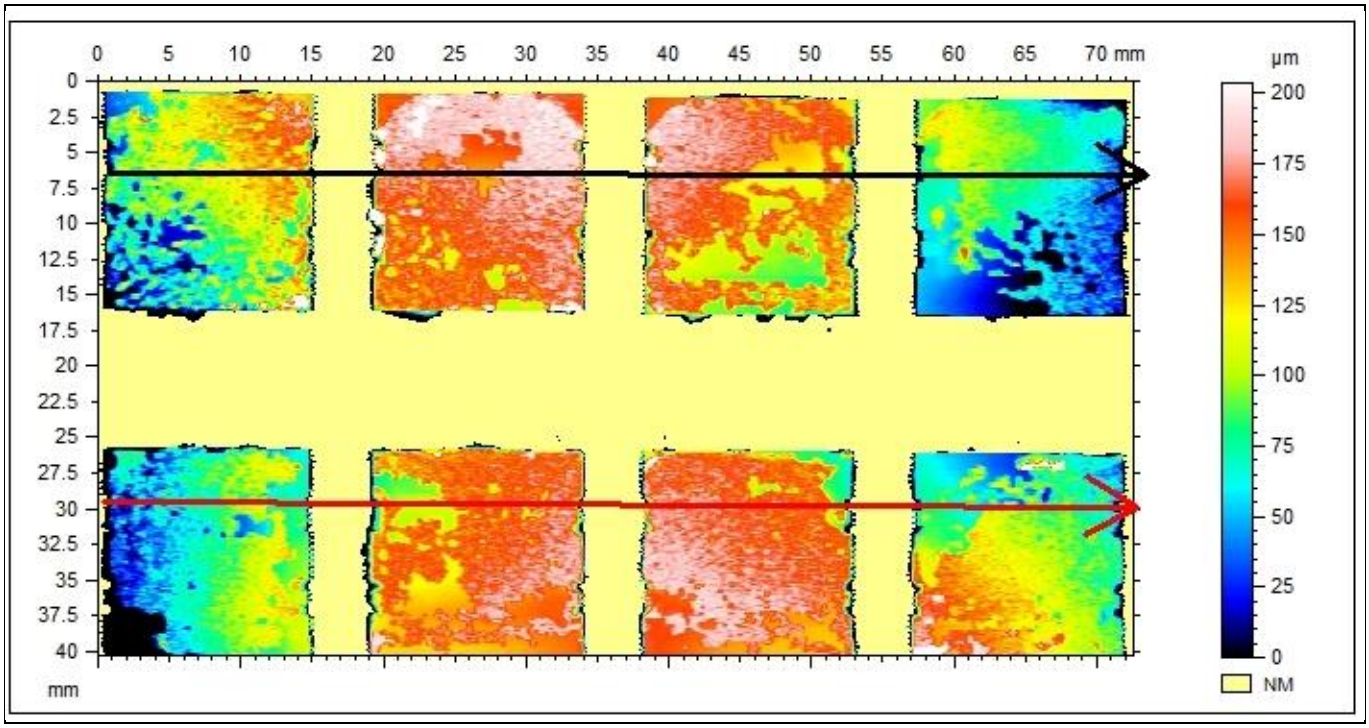


Figure 16 3D optical surface measurement of the TIM of board #40

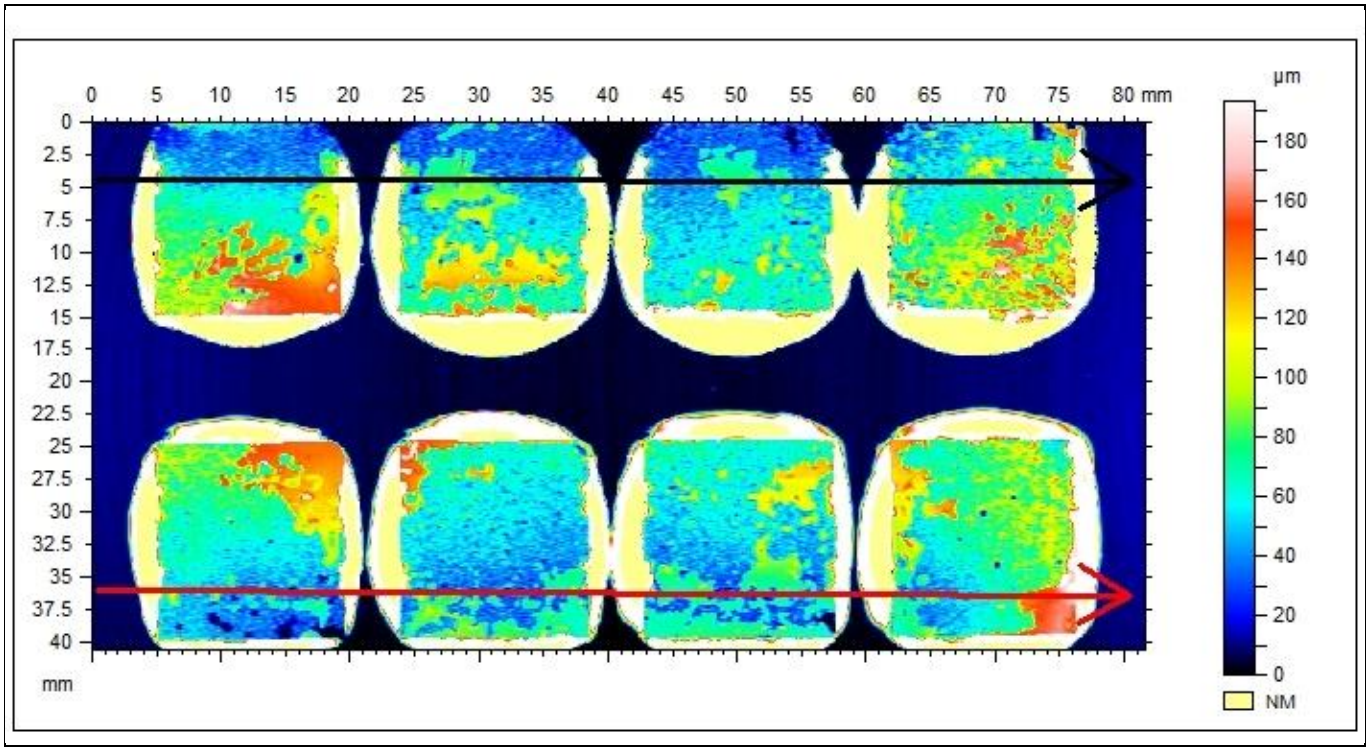


Figure 17 3D optical surface measurement of the residues of the TIM on the coldplate of board #40

4.3 Interpretation of the measurement results

The measurement results shown in **Figure 14** illustrate that the best $R_{th\_j\_cp\_avg}$ values were achieved with board #4, followed by #40 and #24, all using a liquid gap filler as the TIM. The height measurements showed that board #4 has a gap filler thickness of about 270 µm. The thermal conductivity of the gap filler is the highest with 5.1 W/(m·K). Even though the gap filler thickness is not the thinnest measured in the experiment, the overall thermal performance is best, which can be attributed to the very good thermal conductivity of the gap filler.

Aside from the absolute value it is worth mentioning that the spread between the cohabitating packages is negligible.

Board #26 combines a gap filler with a dielectric foil. The height measurements revealed that the gap filler was assembled to be very thick, about 1.5 mm. The thermal resistance of the thick gap filler and the additional dielectric foil results in a total $R_{th\_j\_cp\_avg}$ of 4.4 K/W. The double isolation can be used to guarantee isolation independent of void rate or gap filler height. Nevertheless, to achieve good thermal performance the gap filler thickness in such a setup needs to be reduced, as the thick gap filler increases the thermal resistance of the path from chip junction to coldplate.

Board #18, using a gap pad as interface, shows a notably higher $R_{th\_j\_cp\_avg}$ value. Also, the variation of the individual R_{th} results for the individual transistors is significantly higher than the variation on the board using liquid gap filler.

In conclusion, the liquid gap filler material shows better thermal performance than the pre-cured gap pad arrangements. This can be explained by the higher conformity of the liquid gap filler materials, which reduce the contact resistance (and therefore improve the total $R_{th\_j\_cp\_avg}$).

4.4 Improve thermal performance by reducing mechanical tolerances

A general recommendation in the cooling assembly is to minimize the mechanical tolerances as much as possible to optimize the thermal performance, while guaranteeing a minimum distance of the TIM to guarantee the isolation strength. Infineon is contributing to this optimization with narrow production tolerances for the HDSOP family.

4.4.1 Applying a permanent force with pre-cured gap pads

A permanent force applied on the power semiconductors will reduce the mechanical tolerances, because the standoff tolerances of the package leads are reduced. Hence, the thickness of the TIM can be reduced and the thermal performance can be improved. **Figure 18** gives an example of this technique: the left picture shows a distance measurement from the surface of the PCB to the body of the TSC power package. A standoff of 96.2 µm is visible if no external force is applied to the power package.

The right side of **Figure 18** shows the same measurement with an external force of 100 N. Here, the package standoff (and therefore the distances in the vertical direction) is reduced to ~15 µm. As a result, the TIM can be thinned by ~80 µm and the thermal performance can be improved as well.

Note: *No impact to the thermal-cycling test was observed during reliability testing. This can be explained by the spring-like behavior of the package leads. Details about this investigation are available in **Chapter 3.3**.*

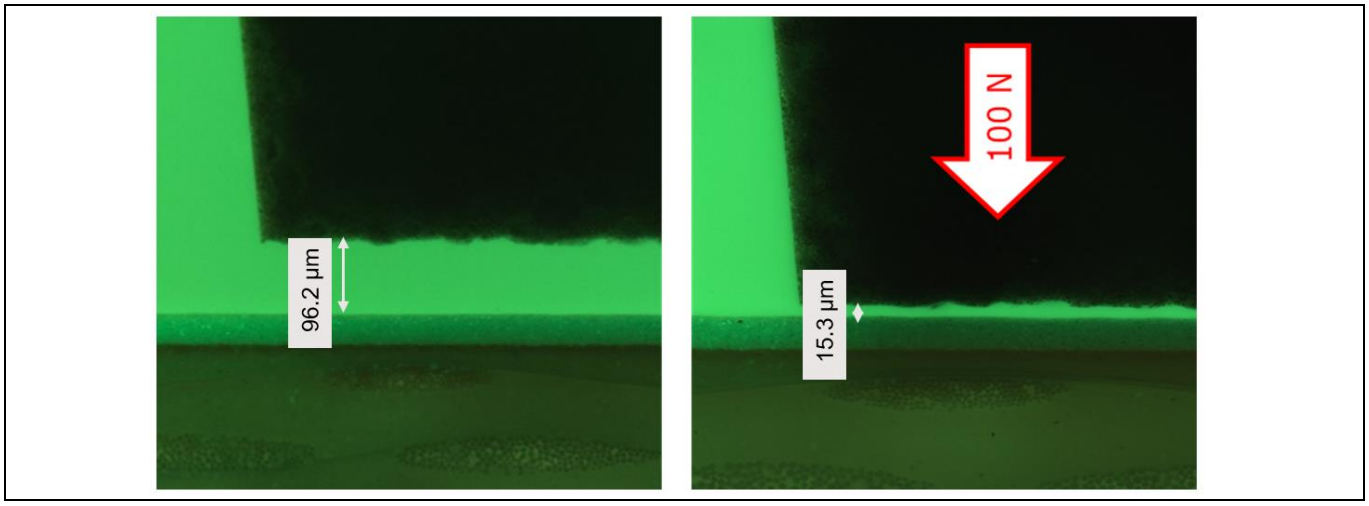


Figure 18 Reduction of package standoff tolerances by applying a vertical force

4.4.2 Reduce warpage of PCBs

We recommend reducing warpage as much as possible to optimize the thermal performance. This can be achieved by using stiff PCB materials or mechanical reinforcements (e.g., with metal carrier structures below the PCB). Also, the dimensions of the PCB correlate with the warpage: the larger the PCB, the more PCB warpage is to be expected. Therefore, it could be beneficial to use many distributed mechanical contact points to improve the conformance of the PCB to the heatsink.

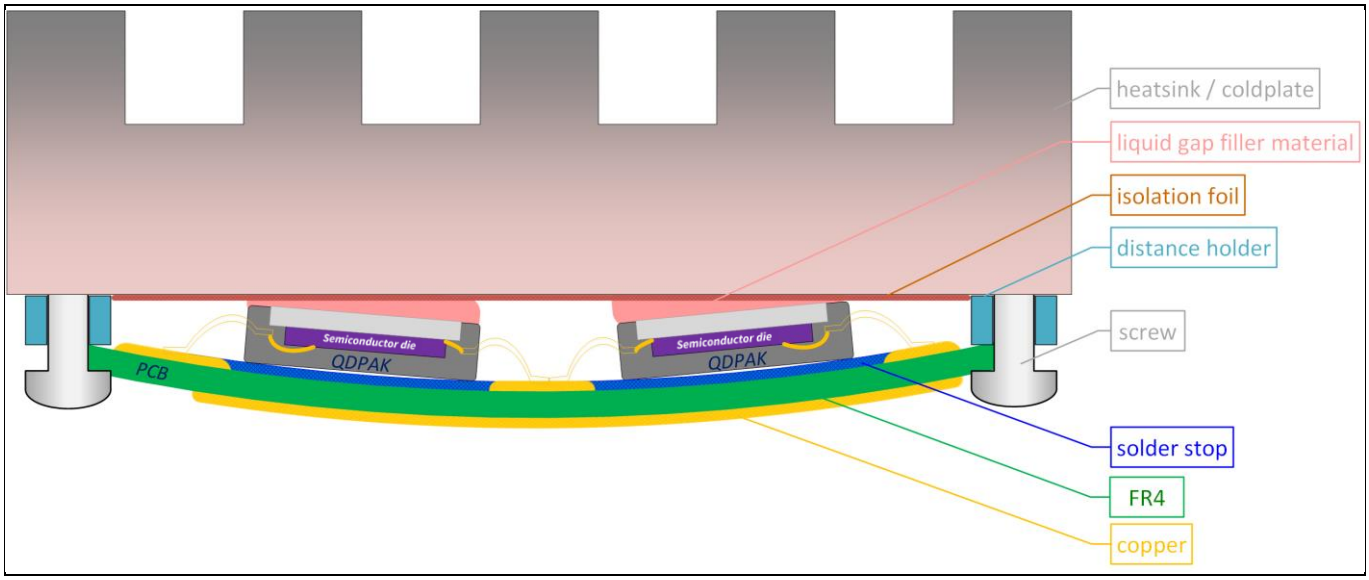


Figure 19 PCB warpage (exaggerated). Recommendation: use as many distributed mechanical contact points as possible (more screws).

4.4.3 Reduce tilting of packages

To maximize the thermal performance, the PCB surface should be as planar as possible to avoid any tilting of the power packages. Cleaning of the board can be one way to avoid unwanted tilting by particles of the power packages during assembly.

Also, tilting effects (such as “tombstoning”) of SMD components caused by the reflow process should be avoided [13].

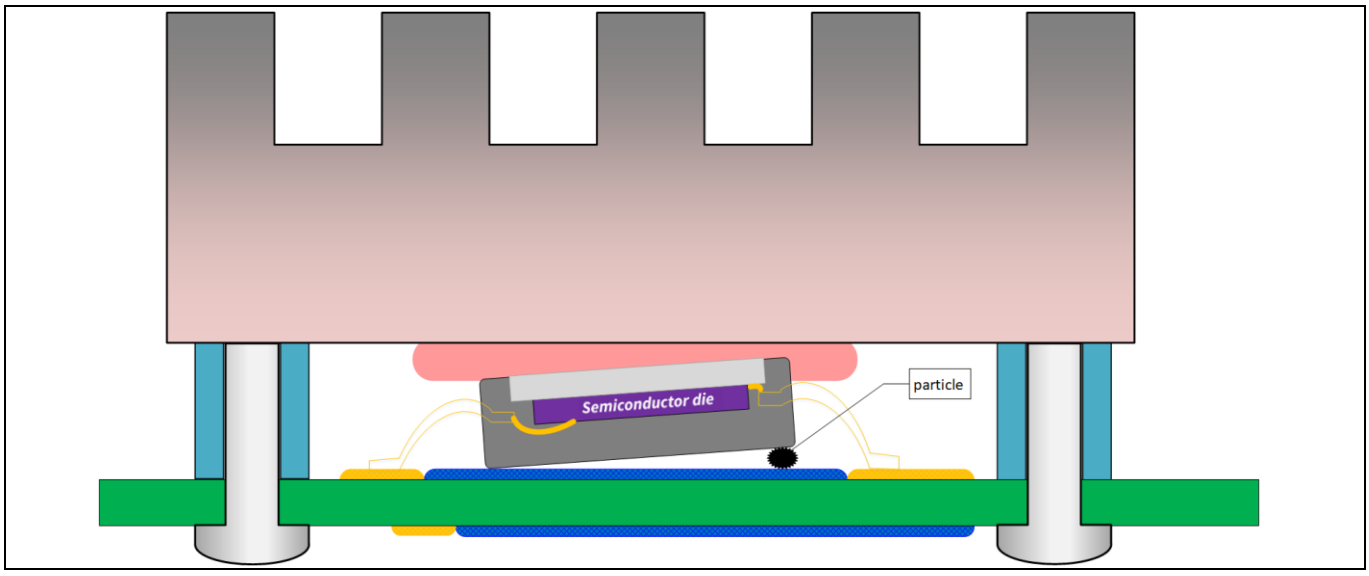


Figure 20 Tilting of SMD components caused by a non-planar surface below the QDPAK. Recommendation: clean PCB of any particles before assembly. Reduce tombstoning effects in reflow process.

4.5 Insulation considerations

Besides achieving good thermal performance, it is important to ensure electrical insulation between the HV potentials and the coldplate. Partial discharge events in particular can erode the insulation and eventually lead to a complete breakdown of it.

Table 5 shows the simulated risk of of partial discharge with a power device attached via an insulating gap filler material to the coldplate. The parameters that were varied were the gap filler thickness, the applied voltage and the void diameter within the single-layer insulation. The risk is indicated as “low”, “medium” and “high”. For the simulation, an analytical method was applied, which is based on a multilayer dielectric model.

The results show that a single-layer insulation with 300 µm thickness is sufficient for 600 V applications, even for void diameters up to 200 µm. For 1200 V applications the single-layer isolation must be applied more thickly, as 500 µm or more, to avoid the risk of partial discharge.

*Note: The two-layer isolation must be at least 50 µm thick to be be considered as double-layer insulation. If one layer is thinner (e.g., the coating), the results for the single-layer insulation (**Table 5**) must be used!*

Independent of these results, the chosen insulation thickness in the application must undergo a holistic assessment, and not one single judgement. During the manufacturing process it is crucial that the void rate of the liquid gap filler is monitored so a minimum void level can be guaranteed.

Table 5 Risk of a partial discharge event for single-layer insulation

Maximal voltage (V)	TIM thickness (µm)	Void diameter (µm)	Risk (likelihood) of a partial discharge event
600	100	10	Medium
600	100	50	High
600	300	10	Low
600	300	50	Low
600	300	200	Low
600	500	10	Low
600	500	50	Low
600	500	200	Low
600	1000	10	Low
600	1000	50	Low
600	1000	200	Low
800	100	10	High
800	100	50	High
800	300	10	Low
800	300	50	Medium
800	300	200	Low
800	500	10	Low
800	500	50	Low
800	500	200	Low

Maximal voltage (V)	TIM thickness (µm)	Void diameter (µm)	Risk (likelihood) of a partial discharge event
800	1000	10	Low
800	1000	50	Low
800	1000	200	Low
1200	100	10	High
1200	100	50	High
1200	300	10	Medium
1200	300	50	High
1200	300	200	Medium
1200	500	10	Low
1200	500	50	Medium
1200	500	200	Low
1200	1000	10	Low
1200	1000	50	Low
1200	1000	200	Low

Table 6 Risk of a partial discharge event for double-layer insulation

Maximal voltage (V)	TIM thickness (µm)	Void diameter (µm)	Risk (likelihood) of a partial discharge event
600	100	10	Low
600	100	50	Low
600	300	10	Low
600	300	50	Low
600	300	200	Low
600	500	10	Low
600	500	50	Low
600	500	200	Low
600	1000	10	Low
600	1000	50	Low
600	1000	200	Low
800	100	10	Low
800	100	50	Medium
800	300	10	Low
800	300	50	Low
800	300	200	Low
800	500	10	Low
800	500	50	Low

Maximal voltage (V)	TIM thickness (µm)	Void diameter (µm)	Risk (likelihood) of a partial discharge event
800	500	200	Low
800	1000	10	Low
800	1000	50	Low
800	1000	200	Low
1200	100	10	Medium
1200	100	50	High
1200	300	10	Low
1200	300	50	Medium
1200	300	200	Low
1200	500	10	Low
1200	500	50	Low
1200	500	200	Low
1200	1000	10	Low
1200	1000	50	Low
1200	1000	200	Low

Double insulation, consisting of a combination of foil and gap filler (like board #4) improves the general insulation robustness (as shown in **Table 6**). A thickness of 100 µm is sufficient for system voltages up to 600 V peak. A thickness of 300 µm fulfills insulation up to 800 V_{peak} and a 500 µm thick TIM can handle peak voltage up to 1200 V_{peak} safely. The void rate is also not so critical if a double-layer isolated approach is chosen.

4.5.1 Maintain a minimum vertical distance

The mechanical design should consider distance holders to guarantee a minimum distance between the coldplate and the cooling plate of the power package (which is on HV potential). This could be achieved by using spacers.

Additionally, liquid gap filler materials are available which ensure a minimum vertical distance with glass balls (which are part of the material mix).

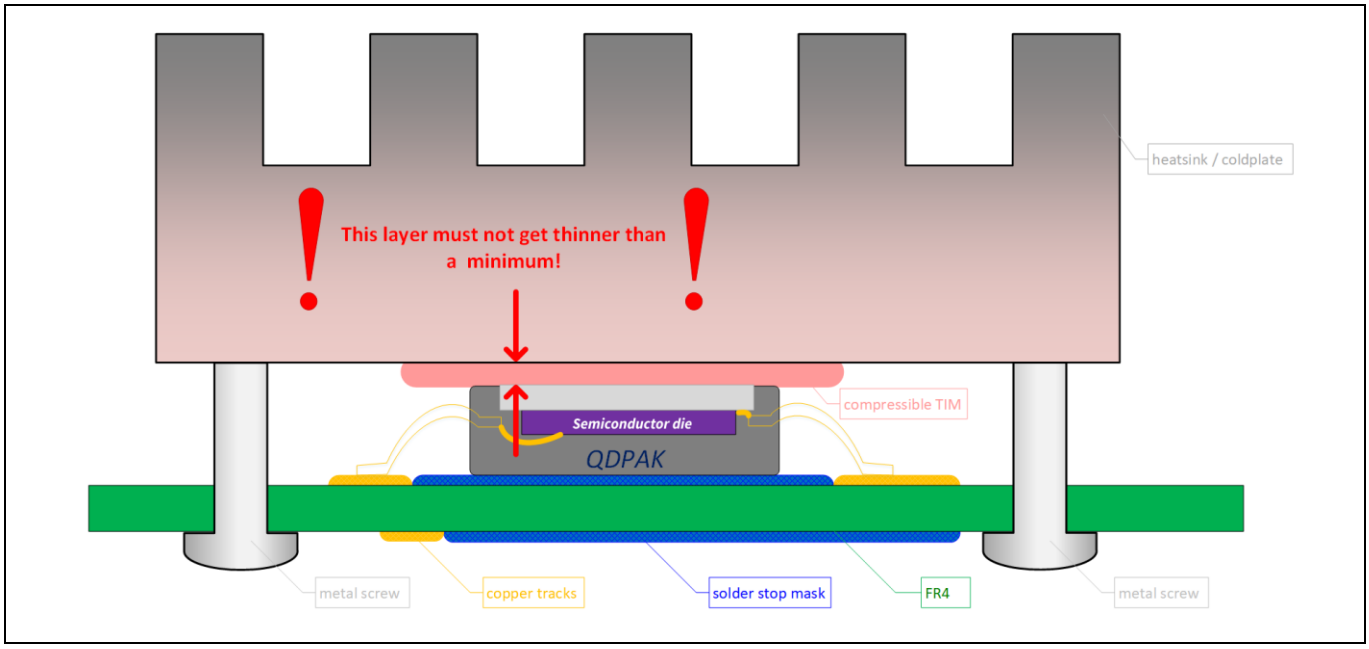


Figure 21 Problem: a minimum thickness of the compressible TIM is needed to safeguard the required insulation

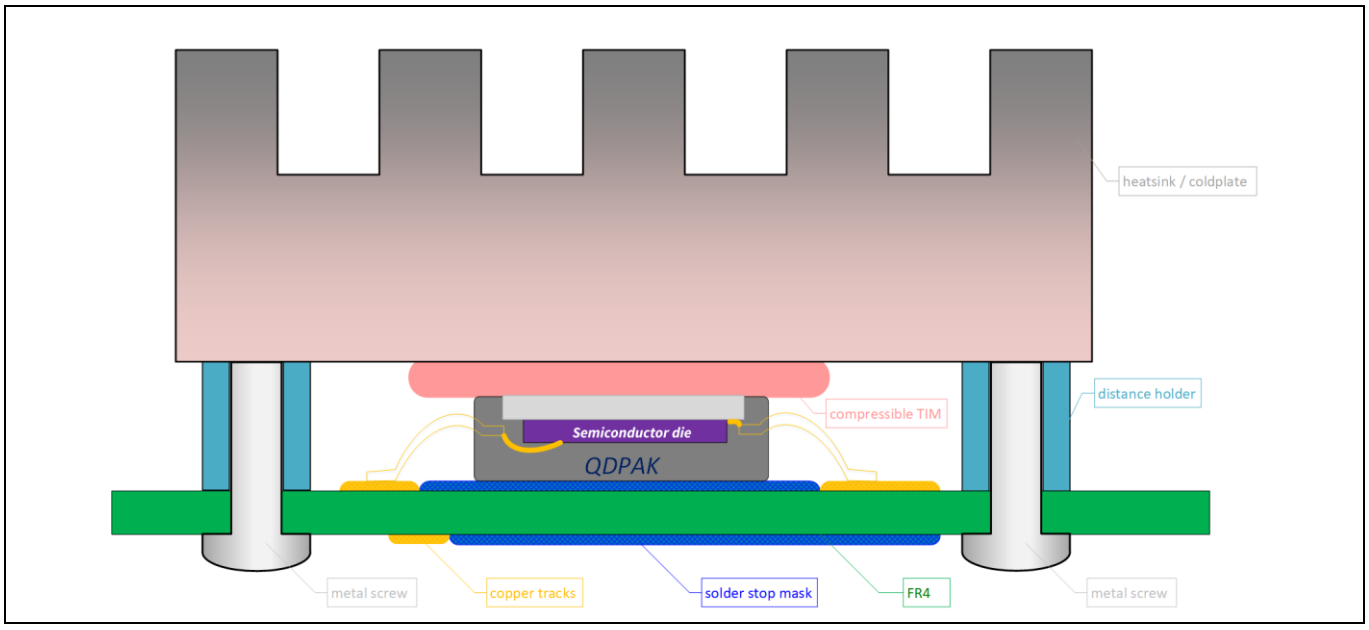


Figure 22 Recommendation: use spacers to guarantee a minimum thickness of the compressible TIM

4.5.2 Reinforced insulation – use of additional insulation foil

The partial discharge simulation presented in **Chapter 4.5** revealed that a single-layer insulation can be used for HV applications only if the void rate and size can be controlled. The use of a double layer of insulation reduces the risk of partial discharge significantly, as shown in **Table 6**. Therefore, an additional insulation foil that is applied on the coldplate can be used to achieve more robust insulation. This approach is shown schematically in **Figure 23**. With this approach the gap filler material can be applied as thinly as necessary without the need for a minimal gap filler height to fulfill the insulation requirements.

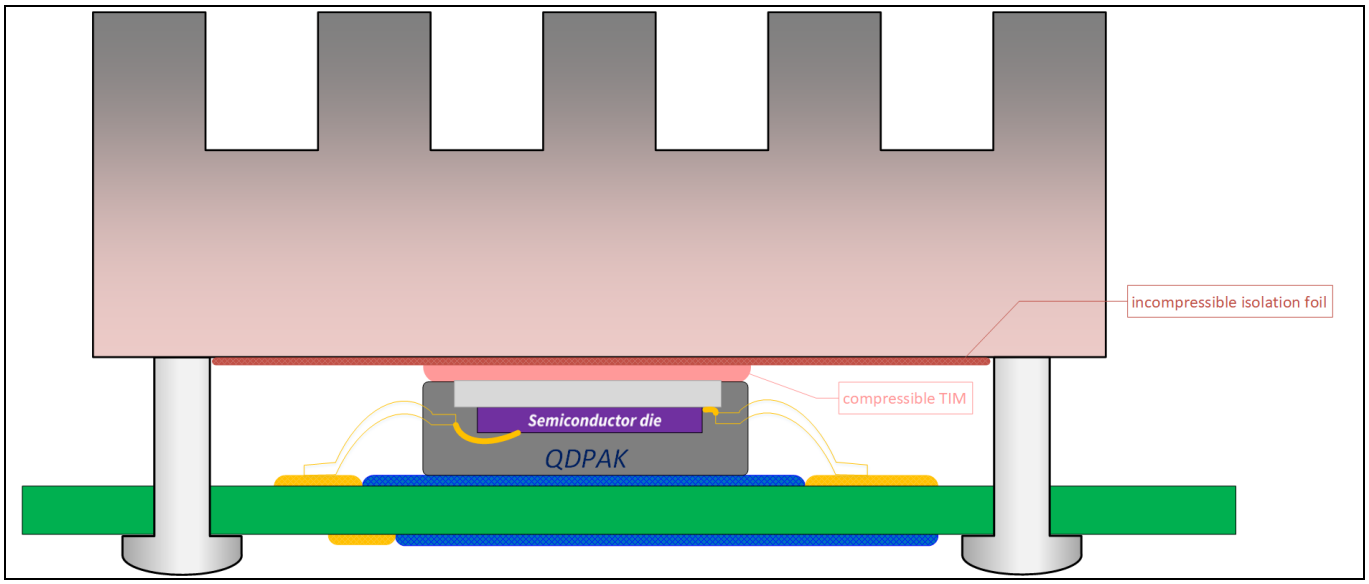


Figure 23 Recommendation: use additional isolation foil for a more robust insulation

4.5.3 Creepage and clearance optimization

Figure 24 shows that both creepage and clearance violations can be observed if the gap filler material is only covering the top side of the power package. The distance from the package leads to the coldplate also needs to be considered. To improve the creepage distance from the package leads to the heatsink, we recommend applying the liquid gap filler or the insulation foil beyond the extent of the package leads. The insulation foil could also be applied to the complete coldplate area, as **Figure 25** shows. In this way the creepage and clearance requirements from the package leads to the coldplate can be fulfilled.

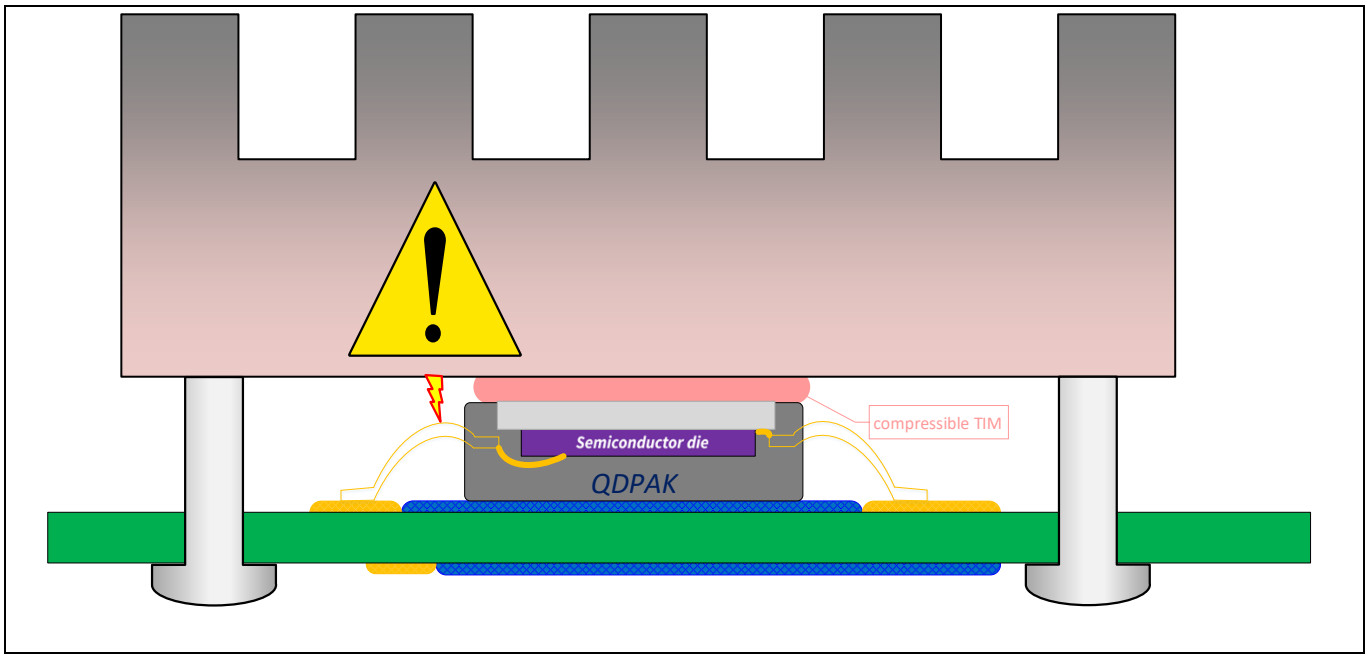


Figure 24 Location of clearance and creepage violation

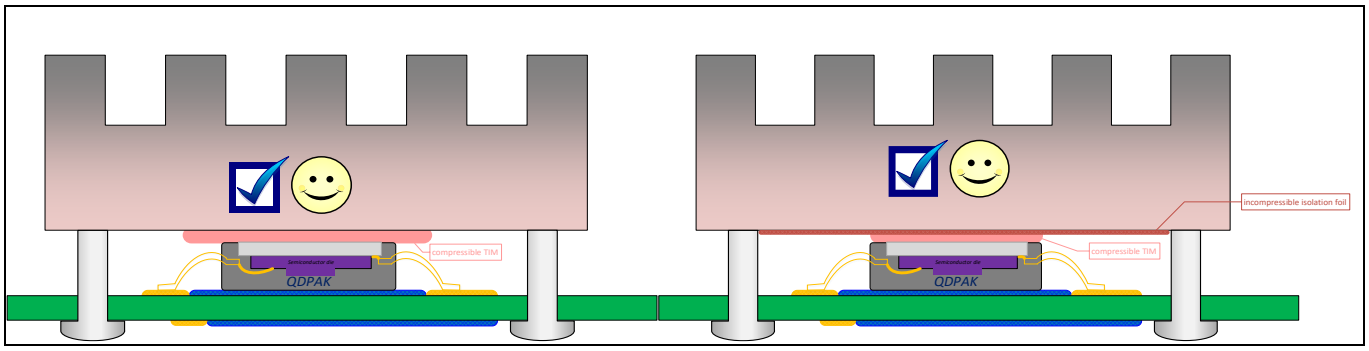


Figure 25 Recommendation: also apply gap filler over lead area or cover coldplate with isolation foil

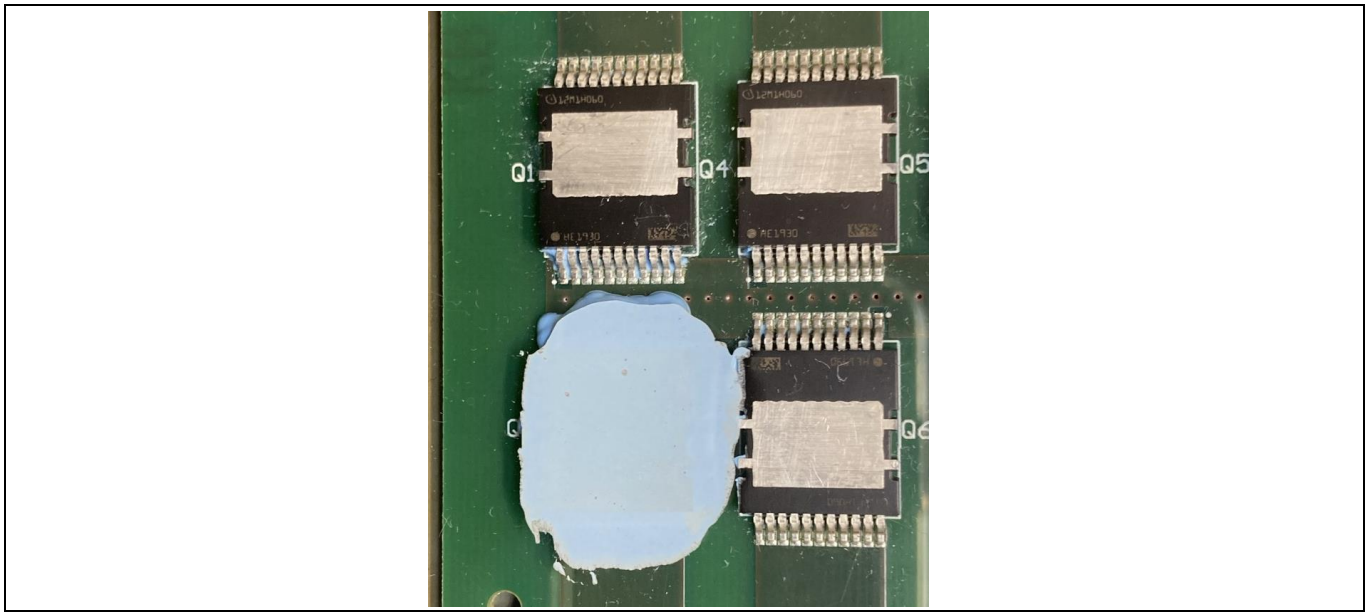


Figure 26 Example: gap filler manually applied on exposed heat pad and package leads

Note: During curing the gap filler material may shrink. This can be ignored for spring-loaded coldplates, but it is important that after application and curing of the liquid gap filler, the screws of the connection between PCB and coldplate are retightened to ensure good contact between the coldplate and the power device.

5 Conclusion

TSC power packages are a promising solution to improve thermal and electrical performance. These packages also help to increase power density and reduce manufacturing effort.

One design target is to minimize all mechanical tolerances to achieve the thinnest possible gap filler thickness for best thermal performance. This can be achieved by different methods, such as using a stiff PCB, pre-cleaning of the board, and ensuring adequate mechanical connections between PCB and coldplate.

Investigations have shown that there is no negative influence on the long-term reliability when using HDSOP packages even if a significant force is applied to the package. The impressed force is absorbed by the leads because they act like springs, and the solder joint connections are not negatively influenced during TCoB tests.

Infineon recommends using a liquid gap filler with high thermal conductivity to compensate the tolerances introduced by the mechanical assembly. The thermal contact resistance is lower for a gap filler compared with a pre-cured gap pad, as shown in **Chapter 4.2**. Also, by using a liquid gap filler no force is needed to press the package to the coldplate, which facilitates the assembly process.

Another important design goal is to ensure the required insulation. If single-layer insulation is used, a certain thickness and a minimum void size needs to be guaranteed. In the case that a gap filler is used as the TIM, a distance holder also needs to be used to guarantee a certain thickness of the compressible gap filler material to ensure insulation. Infineon also recommends applying the gap filler over the whole package area including the leads to improve the creepage from the package to the coldplate.

Greater insulation can be achieved by adding extra dielectric foil to the TIM (double-layer insulation). As shown in **Chapter 4.5**, the risk of partial discharge can be reduced by introducing this foil. Especially for high safety requirements or HV applications (with peak voltages reaching from 800 V to 1200 V), Infineon recommends using double-layer insulation. However, this will reduce the thermal performance because it introduces additional thermal resistance.

In summary, the TSC solution offers many benefits in application if the necessary mechanical challenges are handled accordingly.

Infineon’s TSC package family provides the best solution to ensure successful top-side cooling in the application.

6 References

[1] Infineon Application Note "**600 V CoolMOS™ G7 and 650 V CoolSiC™ G6 come in a new top-side cooling package – the DDPAK**".

[2] AEC – Q101: Failure Mechanism Based Stress Test Qualification for Discrete Semiconductors in Automotive Applications. Rev. D1.

[3] Infineon Publication Additional Information "**General Recommendations for Assembly of Infineon Packages**", JEDEC Solid State Technology Association: IPC/JEDEC J-STD-020*. Moisture/Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices.

[4] JEDEC Solid State Technology Association: IPC/JEDEC J-STD-033*. Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices.

[5] Infineon Guideline "**Storage of Products Supplied by Infineon Technologies**". Revision 7.0.

[6] Infineon Application Note "**Electrical safety and isolation in high voltage discrete component applications and design hints**".

[7] Technical Paper "**Using Forward Voltage to Measure Semiconductor Junction Temperature**" by Keithley Instruments, Inc.

[8] Technical Datasheet "**BERGQUIST GAP PAD TGP HC5000**" by Henkel.

[9] Technical Datasheet "**GFL 3020 & GFL 3025 Gap Filler Liquid**" by KERAFOL.

[10] Technical Datasheet "**BERGQUIST GAP FILLER TGF 3600**" by Henkel.

[11] Technical Datasheet "**Gap Filler SDP-5040A/B**" by Shin-Etsu.

[12] Technical Datasheet "**2-PART SILICONE GAP FILLER TDG-U-SI-2C**" by HALA.

[13] Technical Paper "**Tombstone Troubleshooting**" by EFD.

[14] Technical Information „**Henkel TGF 7000**" by Henkel.

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