# Smart High-Side Switches 

Application Note
What the designer should know
Short introduction to PROFETTM +12 V

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## 1 Abstract

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

This Application Note is intended to provide useful information to designers using PROFET ${ }^{\text {TM }}+$ high side power $^{\text {sin }}$ switch in the automotive environment as well as industrial. Starting from a design perspective, the Application Note describes the application requirements and conclude at device level.

Table 1 Terms in use

| Abbreviation | Meaning |
| :--- | :--- |
| A/D | Analog to Digital converter |
| AWG | American Wire Gauge |
| BCM | Body Control Module |
| CP | Charge Pump |
| CL15 | So called for battery voltage turned OFF during park time of the vehicle |
| CL30 | So called for battery voltage always present |
| CL58 | So called for the battery voltage to the instrument cluster |
| CHMSL | Central High Mounted Stop Light |
| DMOS | Double diffused MOS |
| DRL or DTRL | Day Time Running Light |
| ESD | Electro Static Discharge |
| EMC | Electro Magnetic Compatibility |
| EME | Electro Magnetic Emission |
| EMI | Electro Magnetic Immunity |
| ECU | Electronic Control Unit |
| $E^{2} P r o m ~$ | Electrically Erasable Programable Read Only Memory. |
| GND | Ground |
| GBR | Gate Back Regulation |
| GPIO | General Purpose Input Output |
| HSS | High Side Switch |
| I/O | Input Output (of a digital circuit) |
| IN | Input |
| $I_{\text {SC }}$ | Short circuit current |
| $I_{\text {L(NOM) }}$ | Nominal current |
| $k_{\text {ilis }}$ | Load current mirror factor |
| LED | Light Emitting Diode |
| mission profile | Represents the life cycle of the car, in terms of time, temperature, supply and hazard. |
| OLSF | Metal Oxide Silicon Field Effect Transistor |

App. Note

Abstract

Table 1 Terms in use

| Abbreviation | Meaning |
| :--- | :--- |
| OC | Over current |
| OT | Over temperature |
| OTS | Over temperature swing |
| OL | Open load |
| PROFET | Protected FET |
| PWM | Pulse Width Modulation |
| $P_{\text {LAMP }}$ | Lamp power, expressed in Watts. |
| PCB | Printed Circuit Board |
| $R_{\text {DS(ON })}$ | Resistance of the channel during ON state |
| RPM | Revolution Per Minutes |
| SC | Short Circuit |
| Tier1 | Supplier of the ECU to the OEM: |
| $T_{\mathrm{A}}$ | Ambient temperature |
| $T_{\mathrm{C}}$ | Case temperature, or temperature of the solder |
| $T_{\mathrm{J}}$ | Junction temperature |
| USM | Under hood Switching Module |
| $V_{\mathrm{DD}}$ | Micro controller supply voltage |
| $V_{\mathrm{BAT}}$ | Battery voltage, measured at the battery terminal |
| $V_{\mathrm{S}}$ | Supply voltage of the device, usually battery voltage |
| $Z_{\mathrm{SC}}$ | Short circuit impedance |

App. Note

Abstract


Figure 1 Drawing and Convention

## 2 Introduction. Why High Side Switches.

In the automotive system, a single electrical supply $V_{\text {BAT }}$ potential is available. Five possible solutions exist (refer to Figure 2) to switch electrical loads ON and OFF. The automotive engineering community defines High Side Switches as a switch commuting the battery voltage.


Figure 2 Commutation Possibility of a Load
High Side Switches are used worldwide in automotive applications. Two reasons justify this choice, Short Circuit hazards and System Cost.

### 2.1 Short Circuit Hazard

A Short Circuit (SC) hazard is more likely to occur to GND than to the battery voltage $V_{\mathrm{BAT}}$, thus switching from the high side is considered safer than switching from the low side. Figure 3 represents all possible short circuits in an automotive electrical system. The SC in green will result in the load being permanently ON load. The SC in orange will result in stress to the switch. The SC in red will place stress on the complete vehicle electrical system


Short circuit.vsd
Figure 3 Short Circuit Possibility

### 2.2 System Cost

A Low Side Switch, compared with an equivalent (same package and $R_{\mathrm{DS}(\mathrm{ON})}$ class) High Side Switch is cheaper. Nevertheless, at system level, using High Side Switches architecture is more cost effective. Figure 4 shows a comparison between the 2 architectures. A LSS architecture will usually require an additional wire and fuse for protection.


Figure 4 System cost comparison

### 2.3 Galvanic Corrosion

High Side is often preferred to low side switch while in OFF state there is battery voltage present at the load. With voltage present at the load along with humidity and time a bi-metal galvanic corrosion can occur at the connector for the load. Since High Side does not have voltage present at the during OFF state the amount of corrosion is much less.

### 2.4 Other Switching Solutions

Low side switches are mainly used in applications where one main switch protects several loads switched using the low side.

Push-Pull switches are used in applications which require only one way of current and a very quick deactivation. This architecture includes one HSS. Typical loads include the windshield wipers.
An H-Bridge is the most common method to drive bi-directional motors. Two HSS are used in this architecture.
Serial switching is used where a single failure (such as a short circuit to GND) would cause a critical safety problem e.g. turn the load ON when not acceptable. Typical applications include the Airbag squibs and critical valves. One HSS is used in this architecture.

## 3 Type of supply

### 3.1 Module un-powered during stand-by

Figure 5 shows a typical application where the ECUs are de-powered when the vehicle is parked with the engine off. This type of battery supply is commonly called KL15 (eg in Germany).


Figure 5 Clamp 15 application

### 3.2 Module supplied during stand by

Figure 6 shows a typical application where the ECUs remain powered when the vehicle is parked with the engine off. This type of battery supply is commonly called KL30 (eg in Germany).


Figure 6 Clamp 30 application

### 3.3 Left/Right Front/Rear separation

For safety reasons, supply redundancy is often necessary. Redundancy of the supply is often based on the separation of the left and right side of the vehicle. This is where one battery line supplies all loads on the left side of the vehicle and another line supplies all loads on the right side. The same redundancy can be found with front and rear separation. Adding to this the KL15 and KL30 concepts, a complex ECU can be supplied by up to 8 different supply lines. Figure 7 shows such a supply architecture.

### 3.4 Secondary Supply

Some modules also provide a secondary supply to sub-systems. This architecture is common in door modules and climate systems which can be supplied by a dedicated battery feed switched from the master door or climate ECU. Typical example is the KL58 supply line used to supply the dashboard.


Figure 7 Complex and Mixed of supply line architecture

### 3.5 Ground line

The ground (GND), in a car is the chassis. Therefore, GND is present everywhere and access to GND is always available. In most cases, there is at least one GND pin per module connector. This GND pin is connected via a wire to the chassis. Figure 8 shows different ways to realize a GND connection. On the left hand side is the cheapest method. The most expensive but safest and recommended method is shown on the right and side. Figure 9 show a picture of a GND connection realized on vehicle.


Figure 8 Ground Line Concept


Figure 9 Ground Line Example
One consequence of this architecture can be that some modules don't have the same OV (GND) reference. For example (refer to Figure 10) a high current application such as power steering, starter motor or alternator doesn't have the same $0 V$ reference as the rest of the vehicle. This can also be the case for applications where the connecting cable to GND is long or thin, causing a noticeable impedance. This ground shift voltage can be either positive or negative. Infineon recommends ISO11898-3 (Low Speed CAN network ISO norm) as an umbrella specification. This standard specifies a $\pm 1.5 \mathrm{~V}$ between ECU GND and chassis GND.

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Figure 10 Typical high current application
To simplify this application note, vehicle GND and ECU GND will be considered the same, except where explicitly mentioned. The appropriate terminology is ground shift voltage however this is commonly referred to as simply ground shift. Ground shift represents the difference, $V_{\text {SHIFT }}$ between the 0 V reference of the ECU and the real 0 V of the load. Refer to Figure 11.


Figure 11 Ground shift description

## Automotive Environment

## 4 Automotive Environment

### 4.1 Battery Voltage Supply

Only one supply potential, $V_{\mathrm{BAT}}$ is available in the vehicle. This supply comes from the battery when the engine is off and from the alternator when the engine is running. Figure 12 shows the typical supply topology. The battery voltage is typically 12.6 V (engine off) and 14.55 V when the engine is running although this figure is different for different OEMs. These values can vary in different phases of the mission profile. For simplicity, $V_{\mathrm{BAT}}$ will be used for both the real battery voltage and $V_{\mathrm{ALT}}$, the alternator voltage (engine running).


Figure 12 Typical Supply Chain in a Vehicle

### 4.1.1 Alternator Regulation Loop

The alternator provides current as soon as the engine reaches idle (typically 800RPM). If there is no diode or battery to limit the voltage, an alternator can provide a voltage of greater than 100 V . The current the alternator can provide is between 55A and 200A. This value is mainly dependant on the engine RPM and engine cooling. The alternator current rating is defined by the total vehicle load. The regulation voltage is specified as a function of the alternator temperature ( $T_{\text {ALT }}$ ). The voltage usually decreases with temperature such that the maximum battery voltage is reached when $T_{\mathrm{ALT}}$ is $-40^{\circ} \mathrm{C}$. Refer to Figure 13.


Figure 13 Alternator Regulation Voltage Function of Temperature

## Automotive Environment

### 4.1.2 Alternator Ripple

When the alternator is heavily loaded and providing its maximum possible current, the ripple on the supply line cannot be neglected. $V_{\mathrm{BAT}}$ looks similar to Figure 14. The frequency $f_{\mathrm{AR}}$ and the voltage swing depends on the OEM. As an umbrella specification, the following figures may be used: $V_{\mathrm{AR}}=3 \mathrm{~V}$ peak to peak, $f_{\mathrm{AR}}=[1 \mathrm{kHz} ; 20 \mathrm{kHz}]$.


Figure 14 Typical Alternator Ripple Voltage as a Function of Time

### 4.1.3 Start-Stop Application. Regenerative Braking

The alternator can be a starter-alternator and it can also be used to realize regenerative braking. Each time the car is stationary, the engine is stopped. Engine restart strategies vary between OEMs however the most common method is when the driver releases the brake pedal. This restart will be called in the document "hot ignition", in contrario to "cold ignition" when the car driver turn the ignition key.
A significant increase in "hot ignition" starts needs to be considered. A typical figure is 30 "hot ignition" starts per "cold ignition" start. Since the ignition phase is a severe power consumer (200A for hot ignition, 1000A for cold ignition), it is necessary to recharge the battery quickly. This can be achieved by increasing $V_{\mathrm{BAT}}$ artificiality. Typically to 18 V . An increase in $V_{\mathrm{BAT}}$ results in an increase in electrical power. This increases the engine resistive torque and hence engine gas consumption also increases. This is not acceptable except during braking when kinetic energy is converted into electrical energy.

During acceleration, the resistive alternator torque can be too high and the alternator can be turned OFF during severe acceleration. Figure 15 shows the shape of the battery supply voltage, assuming a starter-alternator with regenerative braking.
As an example, a 14.5 V regulated alternator providing 70A DC current corresponds to 1 kW electrical power. Assuming $30 \%$ efficiency, the mechanical energy required to provide this 1 kW of electrical power is 3.2 kW or 4 horse power (PS). Taking a standard 100PS engine, the driven alternator can offer up to $5 \%$ power increase.

## Car speed



Figure 15 Battery Voltage as a Function of Car Speed.

### 4.1.4 Low Battery Voltage Supply

Low voltage supply phases can be either due to a weak battery (discharged) or during engine cranking. The weak battery is a permanent state (from a semiconductor perspective) while cranking is a transient phenomenon.

### 4.1.4.1 Discharged Battery

A discharged battery is usually due to parasitic leakage current in the vehicle when it has been parked for too long. The minimum battery voltage at which the car can still start is OEM dependant. This voltage is considered as the minimum nominal voltage. Typically 8V.

### 4.1.4.2 Engine Ignition

The voltage during the ignition phase is complex to describe and the values are very dependant on the vehicle OEM as well as the type of engine. All OEMs specify different ignition voltage pulses $V_{\text {CRK_miN }}$ from 3 to 5.5 V (refer to Figure 16). $V_{\text {CRK_osc }}$ is usually 7 V and oscillations range from a couple of Hertz to 800 Hz (800RPM). $V_{\text {BAT_STD }}$ is the battery voltage during the engine stand-by phase and is usually $12.6 \mathrm{~V} . V_{\text {BAT_RUN }}$ is the battery voltage when the engine is running and is usually 14.5 V . For simplicity the red curve is used with $V_{\text {CRK_MIN }}=3$ to 5.5 V , typically $4.5 \mathrm{~V} . t_{\mathrm{CRK}}=65 \mathrm{~ms}, t_{\mathrm{LAUNCH}}=10 \mathrm{~s}$ and $V_{\text {CRK_LAUNCH }}=5.5$ to 8 V .


Figure 16 Ignition pulse

## Automotive Environment

### 4.1.5 High Battery Voltage Supply

The reasons behind a high battery voltage are more numerous than a low battery voltage and include jump start, load dump, faulty alternator regulation and high alternator ripple.

### 4.1.5.1 Jump Start

The jump start for a car (12V) is a situation where a truck battery $(24 \mathrm{~V})$ is bypassing the battery to start the engine. The voltage and the time of the jump start is OEM dependant. A worst case is 28 V for 2 minutes. For Truck, Jump Start is defined when a special electrical equipement connected to power outlet supply for some minutes to 48V the truck battery.

### 4.1.5.2 Load Dump

Load dump occurs when the battery terminal is suddenly disconnected while the alternator is providing current. The battery is essentially a capacitor and hence stabilizes the system. Load dump can also occur during the switching of high current inductive loads. Refer to Figure 17. When the battery is disconnected, the system becomes unstable and the voltage rises until the alternator low side diodes reach avalanche, limiting the voltage to $V_{\text {loaddump }}$. Some OEMs replace the diodes with Zener diodes. The advantage Zener diodes provide is to reduce the load dump (avalanche) voltage to the Zener voltage. $V_{\text {loaddump }}$ and $t_{\text {loaddump }}$ are specified by the OEM. After a delay, ( $t_{\text {loaddump }}$ ) the alternator begins to regulate again and the voltage decreases. As an umbrella specification, Infineon consider $V_{\text {loaddump }}=40 \mathrm{~V}$ for $t_{\text {loaddump }}=400 \mathrm{~ms}$. After the load dump event, a high ripple voltage is observed on the battery line while the battery remains disconnected. As an umbrella specification, Infineon consider $V_{\text {ALT_MAX }}=18 \mathrm{~V}$ and $V_{\text {ALT_MIN }}=12 \mathrm{~V}$. The oscillation frequency is considered to be between 1 kHz and 20 kHz and can be up to 10 hours long. Refer to Figure 18.


Figure 17 Load Dump Configuration


Figure 18 Load Dump Pulse

## Automotive Environment

### 4.1.6 Reverse Polarity

A Reverse polarity condition exists when the battery supply line $V_{\mathrm{BAT}}$ is connected to ground and the ground line GND to the battery supply. Reverse polarity mainly occurs for two reasons. During the module handling and installation, where some awkward movements can be assumed, or when the vehicle has a low battery and the driver connects jumper cables incorrectly from an external battery (Start help), reverse polarity can result. The voltage and time for which the vehicle can withstand this reverse polarity is defined by the OEM. As an umbrella specification, Infineon considers -16 V for 2 mn at ambient temperature $+25^{\circ} \mathrm{C}$. Some loads such as a lamp or resistor can tolerate current flowing in the reverse direction whilst others cannot such as motors, polarized capacitors, etc...

### 4.1.7 Loss of Battery

In an architecture such as CL15, loss of battery is a normal case. In an architecture with shared fuse, when the fuse blows due to a short circuit somewhere else, the loss of the supply line should not result in a module failure.

### 4.1.8 Umbrella Specification for Battery Voltage

To sum up the above discussion, refer to Figure 19.


Figure 19 Infineon Umbrella Specification for Battery Voltage

### 4.2 Temperature

The ambient temperature $T_{\mathrm{A}}$ range in an automotive application is one of the harshest found in electronics. Only space and aeronautical activities can be more challenging. If the minimum temperature is universally agreed to be $-40^{\circ} \mathrm{C}$, the maximum temperature varies with applications, OEM, tier1, module housing, etc.. As an umbrella specification, Infineon considers $T_{\text {A_max }}=+85^{\circ} \mathrm{C}$ for cockpit application, $T_{\text {A_MAX }}=+105^{\circ} \mathrm{C}$ for under hood application.

### 4.2.1 Ambient Module Temperature

Ambient module temperature follows the seasons as shown in Figure 20. Ambient module temperatures are cold in winter, hot in summer. While $-40^{\circ} \mathrm{C}$ is considered to be the minimum temperature to start the car in winter, it is not valid for every engine start in winter as the system heats up during driving. The same logic can be applied to the hot season. It is possible to assume $+85^{\circ} \mathrm{C}$ or $+105^{\circ} \mathrm{C}$ for example, as the maximum ambient temperature (car parked in summer) at start up, but it is incorrect to assume that $T_{\mathrm{A} \_ \text {MAX }}=+85^{\circ} \mathrm{C}$ is a permanent condition during summer. In other words, $-40^{\circ} \mathrm{C}$ and $+85^{\circ} \mathrm{C}$ are considered as starting points, but not as permanent conditions. As an umbrella specification, Infineon considers an ambient temperature profile shown in Figure 21.


Figure 20 Suggested Ambient Module Temperature, over one Year


Figure 21 Suggested Temperature Distribution over Car Life Time

### 4.2.2 Internal Module Temperature

The devices, soldered on the PCB, are subject to the heat radiated by neighboring devices. Each module design is different, hence the heat generated is dependent on the design of the module. As an umbrella specification, Infineon considers a self heating of the module of $+15^{\circ} \mathrm{C}$ in operation mode.

### 4.3 Ground

As described in Chapter 3.5, a ground shift $V_{\text {SHIFT }}$ can exist between the module ground and device ground. Loss of ground should also be a consideration in module design. There are two possible failures which can cause loss of ground, loss of device ground and loss of module ground. Refer to Figure 22. As a device supplier, Infineon assumes any loss of ground to be loss of device ground unless explicitly indicated.


Figure 22 Loss of Module or Device Ground

### 4.4 Lifetime

The life time of one car / module / device is assumed to be 15 years or 131400 hours.

### 4.4.1 Running Time

Running time is an accumulation of time over which the module is in operation (micro controller active, load activated or ready to be activated) is assumed to be 10000 hours. ( $\sim 2 h o u r s$ per day for 15 years)

### 4.4.2 Stand-by Time

Stand-by time corresponds to the remaining time over 15 years where the module is not in operation. With the above assumptions, this is 121400 hours.

### 4.4.3 Number of Ignition

The number of ignitions cycles is determined by the strategy of the car OEM. As an umbrella specification, Infineon consider 100000 cold ignitions over the car life time. This leads to almost $\sim 20$ (18.6) ignitions per day. This number doesn't include the additional start and stop cycles due to the future introduction of starter-alternators. 30 hot ignitions are considered per cold ignition.

## 5 Load and Application

The diversity of loads driven by high side switches is enormous. To cluster these loads is always challenging. Nevertheless, three different categories can be outlined. Lamps or capacitive loads, Motors or inductive loads, and LED or resistive loads.

### 5.1 Lamps / Capacitive and Resistive Loads

Switching lamps for exterior lighting always been the major application of HSS. By law, in every country, 20 lamps covering 8 different functions must be implemented in a vehicle. Table 2 lists the required lighting including the minimum wattage.

Table 2 Lamps Required by Law

| $\mathbf{N}^{\bullet 1)}$ | Function | Abbreviation | Number of Load | Position | Minimum wattage |
| :--- | :--- | :--- | :--- | :--- | :--- |
| $\mathbf{1}$ | Brake light | STOP | 3 | Rear | $3 \times 21 \mathrm{~W}^{2)}$ |
| 2 | Park light | PL | 4 | 2 Front, 2 rear | $4 \times 5 \mathrm{~W}^{3)}$ |
| 3 | Licence plate | LIC | 1 | Rear | $1 \times 5 \mathrm{~W}^{3)}$ |
| 4 | Fog | FOGR | 1 | Rear | $1 \times 21 \mathrm{~W}^{4)}$ |
| 5 | Reverse light | REV | 1 | Rear | $1 \times 21 \mathrm{~W}^{2)}$ |
| 6 a | Side indicators left | SI | 3 | 1 Front, 1 center, 1 rear | $2 \times 21 \mathrm{~W}^{2)}+1 \times 5 \mathrm{~W}^{3)}$ |
| 6 b | Side indicators right | SI | 3 | 1 Front, 1 center, 1 rear | $2 \times 21 \mathrm{~W}^{2)}+1 \times 5 \mathrm{~W}^{3)}$ |
| 7 | Low beam | LB | 2 | Front | $2 \times 55 \mathrm{~W}^{5)}$ |
| 8 | High beam | HB | 2 | Front | $2 \times 55 \mathrm{~W} / 65 \mathrm{~W}$ |

1) The number is arbitrary
2) 27 W in the NAFTA
3) 7 W in the NAFTA
4) Not required in the NAFTA
5) 65 W in the NAFTA

Additional lamps are often present. Table 3 provides a list of the more common optional lamps. On modern vehicles there are typically up to 40 lamps covering more than 14 functions.
Table 3 Optional Lamps

| $\mathrm{N}^{\circ 1}$ | Function | Abbreviation | Number of Load | Position | Wattage |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 2 | Park light | PL | 4 | 2 Front, 2 rear | $4 \times 5 \mathrm{~W}^{2)}$ |
| 3 | Licence plate | PP | 1 | Rear | $1 \times 5 \mathrm{~W}^{2}$ |
| 10 | Side marker | SM | 2 | Center | $2 \times 5 \mathrm{~W}^{2}$ |
| 4 | Fog | FOGR | 1 | Rear | $1 \times 21 W^{3}$ |
| 5 | Reverse light | REV | 1 | Rear | $1 \times 21 \mathrm{~W}^{3)}$ |
| 11 | Fog | FOGF | 2 | Front | 2x55W |
| 12 | Interiors | INT | From 1 to 10 | Interior | From $1 \times 5 \mathrm{~W}^{2}$ ) to 100W |
| 13 | Cornering lamp | CL | 2 | Front | 2x55W |
| 14 | Daytime Running Light ${ }^{4)}$ | DRL | 2 | Front | 2x35W |

1) The number is arbitrary
2) 7 W in NAFTA
3) 27 W in NAFTA
4) Required by law in some countries, can be realized with Low Beam

### 5.1.1 Lamps Regulation

The United Nation Organization (UNO) has regulated automotive lamps in terms of mechanical structure, light emission power and electrical power. These regulations can be found at UNO under the title "Agreement concerning the adoption of uniform technical prescription for Wheeled vehicles, equipment and parts which can be fitted and/or used on wheeled vehicles and the conditions for reciprocal recognition of approvals granted on the basis of these prescriptions". The reference numbers are E/ECE/324 and E/ECE/TRANS/505, dated October 19, 2001. This document is considered the umbrella specification of Infineon in terms of lamp wattage.

### 5.1.2 Lamp Wattage

The lamp wattage is defined at a specific voltage with a percentage tolerance. Table 4 shows the most commonly used lamps in terms of electrical wattage, tolerance and voltage.
The lamp current is dependent on the supply voltage $V_{\text {LAMP }}$. Equation (1) gives the current, function of $V_{\text {LAMP }}$, supply voltage of the lamp. $V_{\text {REF }}$ is the voltage where the power of the lamp is defined.

$$
\begin{equation*}
I_{\text {LAMP }}=\sqrt{\frac{V_{\text {LAMP }}}{V_{\text {REF }}}} \times \frac{\mathrm{P}_{\text {LAMPREF }}}{\mathrm{V}_{\text {REF }}} \tag{1}
\end{equation*}
$$

### 5.1.3 Cold Lamp / Inrush Current

Before switch ON, the lamp is cold. To produce light, it is necessary for the lamp filament to reach a very high temperature (above $1000^{\circ} \mathrm{C}$ ). At switch ON, a significantly higher current is flowing in the filament. This current is called inrush current $I_{\text {INRUSH }}$. Depending on the OEM or tier1 manufacturer, a certain ratio is applied which relates the nominal current of the lamp to the inrush current. As an umbrella specification, Infineon considers an inrush factor of 10x. Figure 23 shows an ideal 27W bulb inrush current without any system limitation. Inrush current increase while temperature decreases.
There is an inherent time required to turn the lamp ON which is defined as $t_{\text {LAMP_ON }}$. Due to the inrush current, the lamp turn ON time, $t_{\text {LAMP_ON }}$ cannot be defined unambiguously. As an umbrella specification, Infineon considers the lamp is ON when the load current reaches $50 \%$ of the $I_{\text {INRUSH }}$, the last retry in case of retry. Infineon considers suitable a switch which allows a $t_{\text {LAMP_ON }}<30 \mathrm{~ms}$.

Table 4 Electrical Wattage Lamp

| Lamp <br> $\mathbf{W}$ | Accuracy <br> $\%$ | $\boldsymbol{V}_{\text {REF }}$ <br> V | Max DC current <br> in $\mathbf{A}^{\mathbf{1}}$ | Max Inrush <br> in $\mathbf{A}$ | Max PWM current <br> $\mathbf{A}^{2)}$ | Maximum current <br> $\mathbf{A}^{\mathbf{3})}$ |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 5 | 10 | 13.5 | 0.5 | 5 | 0.7 | 0.9 |
| 7 | 10 | 12.8 | 0.7 | 7 | 1 | 1.3 |
| 10 | 10 | 13.5 | 1 | 9 | 1.3 | 1.8 |
| 15 | 10 | 13.5 | 1.4 | 14 | 2 | 2.7 |
| 21 | 6 | 12 | 2.3 | 22 | 3.1 | 4.3 |
| 27 | 6 | 12.8 | 2.7 | 26 | 3.7 | 5.0 |
| 55 | 6 | 13.2 | 5.2 | 50 | 7.1 | 9.7 |
| 65 | 6 | 13.2 | 6.1 | 60 | 8.4 | 11.5 |

1) At 18 V
2) At 18 V with light emission regulation (with duty cycle calculated in Chapter 5.1.4)
3) At 18 V with $2 \% \mathrm{PWM}$


Figure 23 Ideal Inrush of a Lamp

### 5.1.4 Life Time

The life time of a lamp is dependent on several parameters with one of the most critical being the supply voltage. As a rule of thumb there is a life time reduction of $50 \%$ per volt increase for supply voltages above 13 V . Ideally, a constant supply voltage should be provided to the lamp. The cost of such a solution is prohibitive, in practice this strategy is never implemented.
Another approach is to use Pulse Width Modulation to drive the lamp. The basic idea of PWM is to maintain constant power in the lamp. The trick is to use the filament thermal inertia to absorb the PWM waveform, making it invisible to the naked eye. The larger the wattage, the bigger the thermal inertia so the PWM waveform can be lower in frequency. The PWM duty cycle is calculated using Equation (2), $V_{\mathrm{PWM}}$ is the optimum lamp voltage.

$$
\begin{equation*}
\mathrm{d}=\frac{\mathrm{V}_{\mathrm{PWM}}{ }^{2}}{\mathrm{~V}_{\text {LAMP }}{ }^{2}} \tag{2}
\end{equation*}
$$

Typically values are $V_{\mathrm{PWM}}=13.2 \mathrm{~V}$ in Europe and $V_{\mathrm{PWM}}=12.8 \mathrm{~V}$ in North America.

### 5.1.5 Light intensity

The intensity of the light is linked to the lamp supply voltage. The aim is to minimize the light intensity fluctuation, which is a function of the battery voltage. The PWM duty cycle, derived from the battery voltage measurement has to be refreshed fast enough to eliminate light fluctuation. However a simple modification of the duty cycle corresponding to a spike in battery voltage is not acceptable. A software strategy should be implemented to leverage the battery voltage as for example Equation (3).
( $V_{\mathrm{BAT}}(\mathrm{t})$ corresponding to the measured $V_{\mathrm{BAT}}$ at the given quantum t )

$$
\begin{equation*}
\left|\mathrm{V}_{\mathrm{BAT}}\right|(\mathrm{t})=\frac{\mathrm{V}_{\mathrm{BAT}}(\mathrm{t}-2)+\mathrm{V}_{\mathrm{BAT}}(\mathrm{t}-1)+\mathrm{V}_{\mathrm{BAT}}(\mathrm{t})}{3} \tag{3}
\end{equation*}
$$

With this strategy, the system is able to react in a maximum of $t_{\text {MAX }}$ which is equal to three time $t_{\text {sample } \mu \mathrm{C}}$, the micro controller sample period. $t_{\mathrm{MAX}}$ is given by the OEM. As umbrella specification, Infineon consider $t_{\mathrm{MAX}}=30 \mathrm{~ms}$.
Figure 24, is an example of PWM voltage regulation to 13 V . These graphs show the worst case scenario when fluctuations in the battery voltage occur just after a battery measurement.
$V_{\mathrm{BAT}}$ is the real supply voltage of the system;
d is the PWM duty cycle;
$<V_{\text {LAMP }}>$ matches the equivalent lamp voltage.


Figure 24 Reaction Time and Strategy for PWM

### 5.2 Light Emitting Diode (LED)

LEDs are increasingly being used to replacing standard lamp bulbs. They offer a longer lifetime as well as lower current consumption for an equivalent light intensity output. Two kinds of LED modules are often used, standard and advanced. For the HSS designer, the difference between these 2 types of modules is negligible and they can both be modeled as a resistive load. An advantage of a LED is that it starts to emit light, far much quicker than a lamp, as soon as a voltage large enough to overcome the forward bias of the device is applied. This voltage depends mainly on the LED color. A very small current (as an umbrella specification, Infineon considers $10 \mu \mathrm{~A}$ ) is enough to cause a LED to glow. This justifies the usage of the $R_{\text {OL_LED }}$ in case open load diagnosis is required.

### 5.2.1 Standard LED Module

In a standard LED module, when one LED is an open circuit, the other LEDs are not affected. This behavior is particularly desirable for rear lighting. The standard LED module, shown in Figure 25 consists of a series resistor $R_{\text {LED }}$ to limit the current and a cluster of LEDs in parallel and serial. The advantage of this circuit is the simplicity. The drawback is the continuous power loss in the resistor (at least 500 mW ) and the susceptibility to transient over voltages and currents. This kind of LED modules are often found for rear light system. As an umbrella specification, Infineon considers $R_{\text {LED }}=50 \Omega, R_{\text {OL_LED }}=680 \Omega$.


Figure 25 Standard LED Module

### 5.2.2 Advanced LED Module

In an advanced LED module, when one LED is an open circuit, the entire module is OFF. This behavior is particularly hazardous for headlights. The advanced LED module, shown in Figure 26 consists of a DC/DC converter driving LEDs in serial. The advantage of this architecture is robustness and immunity to voltage transients. The disadvantage is the relative electronic complexity of the DC/DC converter. As an umbrella specification, Infineon considers the module OFF if $V_{\text {IN }}-V_{\text {OUT }}<7 \mathrm{~V}$. When the LED is broken, the module doesn't consume more than 30 mA max, typically 15 mA (current needed by the DC/DC supply itself).


Figure 26 Advanced LED Module

### 5.2.3 LED Cluster

The number of LED per string, and the number of string are application and OEM dependant. Nevertheless, a rough estimation can be realized in Table 5

Table 5 LED cluster

| Function | Number of string | Number of LED per string | Standard / Advanced |
| :--- | :--- | :--- | :--- |
| Brake light | 7 to 10 | 1 to 3 | Standard |
| Park light | 2 to 5 | 1 to 3 | Standard |
| Side indicators left | 1 or 2 | 7 to 10 | Advanced |
| Side indicators right | 1 or 2 | 7 to 10 | Advanced |
| Low beam | 1 or 2 | 9 to 12 | Advanced |
| High beam | 1 or 2 | 9 to 12 | Advanced |
| Side marker | 2 to 5 | 1 to 3 | Standard |

App. Note

Table 5 LED cluster

| Function | Number of string | Number of LED per string | Standard / Advanced |
| :--- | :--- | :--- | :--- |
| Front Fog | 1 or 2 | 9 to 12 | Advanced |
| Daytime Running Light | 1 or 2 | 7 to 10 | Advanced |

### 5.3 Motors

There is often a requirement to drive a motor in both directions. The driver architecture must then be an H -bridge where two HSS are used. Some motors always run in the same direction, such as wipers, water pump, etc hence only a single HSS is required.

### 5.3.1 Inductive Load

Inductive loads are described by inductance $L$ and resistance R. At switch ON, the inductive load causes a slow current ramp up, based on the time constant $\tau=L / R$. At switch OFF due to the inductance, the current attempts to continue to flow in the same direction which causes the load voltage to invert. Refer to Figure 27, which demonstrates the general voltage and current characteristics of an inductive load at switch ON and OFF. Voltage in blue, current in red, power in green.


Figure 27 Inductive Load Switch ON / OFF

### 5.3.2 Demagnetization Energy

As stated previously, each time an inductive load is switched OFF, a demagnetization energy has to be considered. If the over voltage protection limit is known, this demagnetization energy can be calculated according to Equation (4)

$$
\begin{equation*}
\mathrm{E}=\mathrm{V}_{\mathrm{DS}(\mathrm{AZ})} \times \frac{\mathrm{L}}{\mathrm{R}} \times\left[\frac{\mathrm{V}_{\mathrm{S}}-\mathrm{V}_{\mathrm{DS}(\mathrm{AZ})}}{\mathrm{R}} \times \ln \left(1-\frac{\mathrm{R} \times \mathrm{I}}{\mathrm{~V}_{\mathrm{S}}-\mathrm{V}_{\mathrm{DS}(\mathrm{AZ})}}\right)+\mathrm{I}\right] \tag{4}
\end{equation*}
$$

### 5.3.3 Freewheeling Diode

To keep the current running, and to get advantage of the stored energy in the coil, a freewheeling diode can be used. In such a case, current and voltage in the switch appears as shown in Figure 28 describing a load of 195 mH and $3.5 \Omega$. The PROFET ${ }^{\text {TM }}+$ in use is the BTS5090-2EKA. The battery voltage $V_{\text {BAT }}$ is set to 15 V . PWM is set to 400 Hz . From this example, it is observable that the power in the diode cannot be neglected.


Figure 28 Voltage and Current Profile with Freewheeling Diode in PWM starting phase

### 5.4 Number of Activations

The total number of activations (brake pedal depressed, low beam activation, compressor activation, etc..) depends largely on the habits of the vehicle driver. This does not including extra switching done by the ECU e.g. PWM, software retry strategies etc... The exact mission profile is usually given by the OEM, but nevertheless loads can generally be placed in one of five categories as defined in Table 6.

Table 6 Load activations per engine ignition

| $\mathbf{N}^{\circ}$ of activation | $\mathbf{N}^{\circ}$ of activation <br> per ignition | Type of load example | Average <br> activation time | $\mathbf{N}^{\circ}$ of activation <br> per year |
| :--- | :--- | :--- | :--- | :--- |
| High | 30 | Brake light, Side Indicators | $<1 \mathrm{mn}$ | 220000 |
| High | 30 | Low beam with automatic activation | $>1 \mathrm{mn}$ | 220000 |
| Mid | 1 or 2 | Reverse, Interiors lamp | $>1 \mathrm{mn}$ | 15000 |
| Mid | 1 or 2 | Low beam with manual activation | $>1 \mathrm{mn}$ | 15000 |
| Low | $1 / 3$ | High beam, Fog lamps | $>1 \mathrm{mn}$ | 2500 |

### 5.5 Wiring

To completely define a wire, three parameters are necessary, the diameter, the length and the insulator materials. The diameter and length give the electrical characteristics ( $\Omega / \mathrm{km}$ and $L_{\text {cable }} / \mathrm{km}$ ). The insulator and the environment gives the maximum current.

### 5.5.1 Wire as a Parasitic Electrical load

Although the wire is not a load, it has to be considered in automotive applications during the design phase. Wires offer a benefit to the system by limiting surge currents such as bulb lamp inrush current thanks to parasitic inductance ( $L_{\text {cable }}$ ), as well as resistive ( $R_{\text {CABLE }}$ ). The wire will limit the current. On the other hand, the inductive energy stored in the cable is sometimes not neglectable, especially for long wire harness found in truck or trailer application.

### 5.5.2 Maximum Current in a Wire

Wires require protection from excessive current. The maximum current which can flow in the wire is time dependent and defined by a square law function $I^{2} t=$ constant. The maximum current the wire can handle is limited by the insulation material. The OEM defines the wires to be used in a vehicle and this information is usually kept confidential. Figure 29 shows an example of the current time coupling limitation of a cable as a function of the time.

The maximum current in the wire is a thermal law. This constant depends, as previously stated on the insulation material and also neighboring cables. For example, a wire within a group of 20 wires in a wire harness will have a lower maximum current rating than the same wire when it is not in a group. As an umbrella specification, Infineon considers a reduction of $40 \%$ of the nominal current.
Table 7 sums up the types of wire often use in an automotive environment. Note that these values are indicative and must be crossed-checked with the application and the OEM.

Table 7 Wire Characteristics as a function of Diameter

| Cross section <br> $\left(\mathbf{m m}^{2}\right)$ | Gauge <br> $(\text { AWG })^{\mathbf{1})}$ | Impedance <br> $(\Omega / \mathbf{k m})$ | Inductance <br> $(\mathbf{m H} / \mathbf{k m})$ | Max DC current <br> $(\mathbf{A})^{\mathbf{2})}$ |
| :--- | :--- | :--- | :--- | :--- |
| 50 | 0 | 0.4 | 1.1 | 228 |
| 25 | 3 | 0.8 | 1.16 | 150 |
| 10 | 7 | 1.9 | 1.20 | 85 |
| 6.0 | 9 | 3.1 | 1.25 | 60 |
| 4.0 | 11 | 5 | 1.30 | 45 |
| 2.5 | 13 | 7.6 | 1.36 | 34 |
| 1.5 | 15 | 12.7 | 1.4 | 24 |

App. Note

Load and Application

Table 7 Wire Characteristics as a function of Diameter

| Cross section <br> $\left(\mathbf{m m}^{\mathbf{2}}\right)$ | Gauge <br> $(\mathbf{A W G})^{\mathbf{1})}$ | Impedance <br> $(\Omega / \mathbf{k m})$ | Inductance <br> $(\mathbf{m H} / \mathbf{k m})$ | Max DC current <br> $(\mathbf{A})^{\mathbf{2})}$ |
| :--- | :--- | :--- | :--- | :--- |
| 1.0 | 17 | 18.5 | 1.45 | 19 |
| 0.75 | 19 | 24.7 | 1.49 | 16 |
| 0.50 | 20 | 37 | 1.55 | 12 |
| 0.30 | 21 | 56 | 1.65 | 9 |

1) Approximation only
2) Assuming $T_{\text {ambient }}=85^{\circ} \mathrm{C}$ and wire alone in free air. Approximation only


Figure 29 Example of Current Limitation of Wire Harness

### 5.6 Platform and Vehicle Diversity

With the aim of developing better and cheaper new vehicles faster, OEMs have for some years adopted a platform strategy. This strategy offers the possibility of developing a generic module to address different vehicle platforms, or different configurations within the same vehicle platform. A vehicle today is offered with 3 or 5 doors in sedan, coupé, convertible, commercial or with towing capability. The diversity of models is huge. A platform approach offers a great benefit to the OEM. At a module level, the challenge is in the flexibility which can be offered. Figure 30 shows different HSS configurations to meet the needs of basic legal requirements, up to the high end solutions required by some OEMs. The example given is of a reverse light and a fog light, with or without trailer and with or without battery feed split. The example is not exhaustive!


Figure 30 Example of Different Vehicle with One Platform Approach for Same Function

## $6 \quad$ Failures in the Field

Possible failures in the field are usually linked to inter-connection (e.g., short circuit or open circuit load).

### 6.1 Short Circuit to Ground

The short circuit to GND is extensively described in the AEC Q100-012 documentation. This is considered as an umbrella specification by Infineon. Figure 31 shows the hardware configuration of the AEC-Q100-012. The chassis of the vehicle is the GND. The probability of a short circuit to GND is significant, compared with all other possible short circuit events. This is a challenging aspect of designing with High Side Switches and will be described later in Chapter 8, which is dedicated to protection. Without any kind of protection measures, the current will be limited only by the wiring and thus will reach $14 \mathrm{~V} / 30 \mathrm{~m} \Omega=450 \mathrm{~A}$. This test is obviously destructive.


AEC short circuit hardware set up .vsd
Figure 31 AEC-Q100-012 Hardware Set-up for Short Circuit Test
The exact short circuit impedance is described in the AEC-Q100-012 document also, an extract of which is shown in Figure 32.

Table 1: Definition of Impedances for Short Circuit Characterization

| Operating Point | Description | $R_{\text {short }}(m \Omega)$ <br> $\pm 20 \%$ | $L_{\text {short }}(\mu \mathrm{H})$ <br> $\pm 20 \%$ |
| :--- | :--- | :---: | :---: |
| Terminal Short Circuit | Short at module | 20 | $<1$ |
| Load Short Circuit | Short at load, $I_{\text {short }} \leq 20 \mathrm{~A}$ | See Section 3.2.2.1 | 5 |
| Load Short Circuit | Short at load, $20 \mathrm{~A}<I_{\text {short }} \leq 100 \mathrm{~A}$ | 100 | 5 |
| Load Short Circuit | Short at load, $I_{\text {short }}>100 \mathrm{~A}$ | 50 | 5 |

AEC short circuit impedance .vsd
Figure 32 AEC-Q100-012 Short Circuit Impedance

### 6.2 Short Circuit to Battery

There is generally a low probability of a short circuit to the battery, nevertheless it is possible to reach a critical situation with such a failure. Figure 33 shows a typical case where a short circuit is applied to one of the five outputs of a given ECU module. When this switch allows the current to flow (in this case, in an inverse mode), the
four other outputs and the module are all supplied by the switch. If the fuse or the relay connection to the supply battery feed is broken, the complete module supply current will then flow from the output shorted to the battery.


Figure 33 Example of Stressful Short Circuit to Battery Case

### 6.3 Open Load

Open load can be caused by two phenomena, a broken wire or a broken load. Although this is not a critical scenario, the application usually requires diagnostic information to be sent to the driver. Note that the definition of an open load is usually OEM dependant. As an umbrella specification, Infineon considers $R_{\text {DIRT }}=4.7 \mathrm{k} \Omega$ resistor to GND. By law, side indicators have to be reported missing by doubling the flashing frequency. All other open load diagnosis are OEM requirements only.

### 6.4 Short Circuit Between Load

A short circuit between loads can occurs anywhere in the wiring path. Consequences can range from a complete overload, similar to short circuit or a simple additional current with no adverse behavior, except for the unexpected parasitic switch ON of another load. In Figure 34, the OUT2 switch will be overloaded by the higher load, while OUT1 will virtually neglect the failure. In generally an OEM will request that this type of failure is diagnosed. Note that the wiring can also be stressed by such a short circuit event.


Figure 34 Short Circuit Between Load

## $7 \quad$ Power Stage

The power stage of PROFET ${ }^{\text {TM }}+$ is a high side switch consisting of a vertical N channel power MOSFET. The power MOSFET technology is called DMOS. The capability of this power element to pass current can be expressed in terms of its $R_{\mathrm{DS}(\mathrm{ON}) \text {. }}$. The smaller the $R_{\mathrm{DS}(\mathrm{ON})}$, the higher the current capability.

### 7.1 Power Element

The power element for switches is a $N$ channel power MOSFET (DMOS) in the majority of cases. PROFET ${ }^{\text {TM }}+$ also use an N channel power DMOS MOSFET as power element. Table 8 summarizes the advantages and disadvantages of DMOS versus bipolar power structures, assuming the same specifications can be realized with either technology. It is shown that DMOS offers better performance in short circuit robustness, high voltage capability and chip size.

Table 8 Comparison between Bipolar and DMOS

| Topic | Bipolar | DMOS |
| :--- | :--- | :--- |
| Accuracy |  |  |
| Offset |  | - |
| Process deviation |  |  |
| Chip area |  |  |
| Voltage capability |  | $\mathbf{+}$ |
| High current robustness |  |  |
| Current consumption |  |  |
| Input current |  |  |

Figure 35 shows the differences between planar and trench (vertical) DMOS technologies. With identical $R_{\mathrm{DS}(\mathrm{ON})}$, it can be seen that the trench DMOS device is smaller. This also results in a smaller gate charge $Q_{\mathrm{G}}$ for the trench DMOS device. Since the planar DMOS device is larger, less cooling is required and the $E_{\text {AS }}$ is better than the trench DMOS device. In PROFET ${ }^{\text {TM }}+$, the supply is the drain which means that the supply is at the bottom of the chip.


Figure 35 Planar (Left) versus Trench (Right)

App. Note

The $R_{\mathrm{DS}(\mathrm{ON})}$ of $\mathrm{PROFET}^{\mathrm{TM}}+$ can be described as a function of temperature (expressed in ${ }^{\circ} \mathrm{C}$ ) See Equation (6). Figure 36 provides the derating of $R_{\mathrm{DS}(\mathrm{ON})}$, assuming $100 \%$ at maximum junction temperature.

$$
\begin{equation*}
\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}=\left.\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}\right|_{150 \mathrm{C}} \times\left(1+\left(\mathrm{T}_{\mathrm{J}}-150\right) \times 3,584 \times 10^{-3}\right) \tag{5}
\end{equation*}
$$



Figure 36 Relative $R_{\mathrm{DS}(\mathrm{ON})}$, Function of Junction Temperature $\boldsymbol{T}_{\mathrm{J},}$, base 100 at $150^{\circ} \mathrm{C}$

### 7.2 Voltage Limitation

As with every device based on a given semi-conductor technology, $\mathrm{PROFET}^{T M}+$ devices has a maximum voltage. If this voltage is exceeded, the DMOS power stage and/or the logic will avalanche and the device will quickly be destroyed. Figure 37 shows the influence of temperature on the zenering voltage.


Figure 37 Min Typical and Maximum Avalanche Voltage, Function of the Temperature $\boldsymbol{T}_{J}$

### 7.3 Charge Pump

When the DMOS is ON, the output voltage is very close to the supply voltage $V_{\mathrm{S}}$. As the power stage is an N channel power DMOS, the device requires a charge pump to provide a $V_{G S} \sim 7 \mathrm{~V}$. The concept of a charge pump is described in Figure 38. In the first phase, the $C_{\text {LOAD }}$ capacitor is charged up to the $V_{\mathrm{S}}$ voltage. In phase two, the $C_{\text {LOAD }}$ is discharged through a diode into $C_{\mathrm{CP}}$, the charge pump capacitor. The charge pump runs at a frequency of 2.5 MHz . The voltage rises in steps of $C_{\mathrm{LOAD}} / C_{\mathrm{CP}}$, to theoretically twice the battery voltage. In practice, this voltage is limited to 10 V above $V_{\mathrm{S}}$. The ratio is $C_{\mathrm{CP}}=C_{\mathrm{LOAD}}$.


Figure 38 Charge Pump Block Diagram

### 7.4 Slope Control Mechanism

For EMC reasons (refer to Chapter 14), PROFET ${ }^{\text {TM }}+$ devices have embedded slope control for both switch ON and switch OFF. The actual switching event is divided into three stages. Refer to Figure 39. First, the gate of MOSFET is connected to $V_{\mathrm{S}}$ via current generator. $t_{\text {ON_delay }}$ is linked to the necessary time for the gate to reach $\sim 2 \mathrm{~V}$. Then the MOSFET switches ON quickly. A fast switch ON time is required to minimize switching power losses (refer to Chapter 7.5). As soon as $V_{\text {OUT }}$ reaches $\sim 70 \%$ of the supply voltage $V_{S}$, the charge pump starts to drive the gate to obtain the minimum $R_{\mathrm{DS}(\mathrm{ON})}$ of the device. The slope is reduced due to the necessary time to completely load the gate capacitance.


Figure 39 Switch ON and Switch OFF timing

At switch OFF, a similar behavior is observed. First, the charge pump is disconnected and a strong current generator $I_{\text {FASTGATEUNLOAD }}$ quickly discharges the gate charged of electrons until $V_{\text {OUT }}$ reaches $\sim 70 \%$. Then the gate is discharged with a constant current $I_{\text {GATEUNLOAD }}$ until the gate voltage is zero. Figure $\mathbf{4 0}$ shows the block diagram of the gate driver.


Figure 40 Gate Driver Schematic
The EMC performance when driving the HSS with a PWM waveform has been improved thanks to the addition of current matching measures. PROFET ${ }^{\text {TM }}+$ offers matching of the loaded current $I_{\text {GATELOAD }}$ and the unloaded current $I_{\text {GATEUNLOAD }}$. This matching can be found in all PROFET ${ }^{\text {TM }}+$ datasheets under the Slew rate matching parameter $\Delta \mathrm{dV} / \mathrm{dt}$.

### 7.5 Power Losses Calculation

The power losses P in the device, assuming a resistive load $R_{\mathrm{L}}$, can be calculated as follow. (Refer to Figure 41). The instantaneous power in the switch is the result of the load current $I_{\mathrm{L}}$ multiplied by the drain to source voltage $V_{\mathrm{DS}}=V_{\mathrm{S}}-V_{\text {OUT. }}$. The resulting curve is shown in Figure 41. A good approximation is realized by the orange isosceles triangles and the rectangle.
The triangle has as vertex at $P_{\text {MATCH }}$ which is the physical point where the switch resistance corresponds to the exact load resistance i.e. $R_{\mathrm{DS}(\mathrm{ON})}=R_{\mathrm{L}}$. Equation (6) gives the relationship between $P_{\mathrm{MATCH}}$ and $R_{\mathrm{L}}$.

$$
\begin{equation*}
\mathrm{P}_{\mathrm{MATCH}}=\frac{\mathrm{V}_{\mathrm{S}}}{2} \times \frac{\mathrm{I}_{\mathrm{L}}}{2}=\frac{\mathrm{V}_{\mathrm{S}}^{2}}{4 \times \mathrm{R}_{\mathrm{L}}} \tag{6}
\end{equation*}
$$

As the drivers are very symmetrical, it is assumed switching ON $t_{\text {SON }}$ and switching OFF $t_{\text {SOFF }}$ times are identical i.e. $t_{\text {SON }}=t_{\text {SOFF }}$. The area of the triangle represents the switching energy and is defined by Equation (7).

$$
\begin{equation*}
\mathrm{E}_{\mathrm{SON}}=\mathrm{E}_{\mathrm{SOFF}}=\frac{1}{2} \times \mathrm{P}_{\mathrm{MATCH}} \times\left(\mathrm{t}_{\mathrm{ON}}-\mathrm{t}_{\mathrm{ONdelay}}\right) \tag{7}
\end{equation*}
$$

The orange rectangle represents the energy $E_{R(O N)}$ lost during the ON state of the DMOS power element and is easily calculated by Equation (8).

$$
\begin{equation*}
\mathrm{E}_{\mathrm{RON}}=\mathrm{R}_{\mathrm{DSON}} \times \mathrm{I}_{\mathrm{L}}^{2} \times \mathrm{t}_{\mathrm{RON}} \tag{8}
\end{equation*}
$$

In conclusion, the power losses in the DMOS power element calculated by using Equation (9).

$$
\begin{equation*}
\mathrm{P}=\frac{\left(2 \times \mathrm{E}_{\mathrm{SON}}+\mathrm{E}_{\mathrm{RON}}\right)}{\mathrm{t}_{\mathrm{CYCLE}}} \tag{9}
\end{equation*}
$$



Figure 41 Power Losses Calculation

### 7.6 Switch Behavior with PWM Input

Pulsed Width Modulation is a special case where the cycle time, $t_{\mathrm{CYCLE}}$ is the inverse of the PWM frequency $f_{\mathrm{PWM}}$. There are four limitations of PROFET ${ }^{\text {TM }}+$ which need to be considered when using a PWM waveform. These are power loss, EMC emissions, switching time and diagnostic limitations. Power loss and switching time issues will be described below. The EMC and diagnostic limitations will be described in dedicated chapters (Chapter 9.8 and Chapter 14).

### 7.6.1 PROFET $^{\text {TM }}+$ PWM Limitations due to Power Losses

The feasibility of driving a load with a PWM waveform is often limited by the maximum power loss allowable in an application. This is critical when the $f_{\text {PWM }}$ frequency is high or when the load has a relatively low resistance. (Refer to Chapter 7.5 for details how to calculate the power losses). To calculate the maximum power losses an application can support, refer to Chapter 7.7. Where the power losses are unacceptable for the device, the easiest solution is to either reduce $f_{\mathrm{PWM}}$, or to use a device with lower $R_{\mathrm{DS}(\mathrm{ON})}$.
Figure 42 shows the power loss in a BTS5045-2EKA when driving a 27 W bulb. The PWM regulation voltage of 13 V with PWM frequencies of zero, 100 Hz and 200 Hz is shown. The switching time is assumed to be $t_{\text {SON }}=t_{\text {SOFF }}$ $=120 \mu \mathrm{~s}$. Figure 43 shows the power losses in a BTS5045-2EKA when driving a 27 W bulb, with a PWM regulation

App. Note
voltage of 13 V and PWM frequencies up to 1 kHz . From these graphs, it is clear that the BTS5045-2EKA has higher power losses at higher PWM frequencies. Refer to Chapter 13.1 for detailled calcuation.


Figure 42 BTS5045-2EKA Power Losses in PWM with a 27W Bulb Load. $V_{\text {PWm }}=13 \mathrm{~V}$


Figure 43 BTS5045-2EKA Power Losses in high PWM frequency with a 27W Bulb Load. $V_{\mathrm{PWM}}=13 \mathrm{~V}$

### 7.6.2 PROFET $^{\text {TM }}+$ PWM Limitations Due to Switching Time

To determine the minimum turn ON time, it is necessary to define when the DMOS power switch is actually ON. This is assumed to be when the output reaches a minimum of $90 \%$ of $V_{\mathrm{S}}$. As described in Chapter 7.4, PROFET ${ }^{\text {™ }}$ $+s$ have a defined switching sequence. The minimum turn on time, $t_{\text {RON }}$ represents the minimum time the switch ON. Refer to Figure 44. The specified turn ON time to $90 \%$ of $V_{\mathrm{S}}, t_{\mathrm{ON}}$ defines the fastest input pulse which will turn the switch ON. With an input pulse of this length, $t_{\text {RON }}$ is smaller than the turn off delay, $t_{\text {OFF_delay }}$ which is the smallest ON time a PROFET ${ }^{\text {TM }}+$ reaches. A similar example can be used to show the minimum O$\overline{F F}$ time possible which is limited by $t_{\text {ON_delay }}$ assuming the switch is OFF if the output voltage is below $10 \%$ of $V_{\mathrm{S}}$.


Figure 44 Minimum $t_{\text {RON }}$
$t_{\text {OFF_delay }}{ }^{*} f_{\text {PWM }}$ is the smallest duty cycle, $d_{\text {MIN }}$ the device can handle. At this point, it is useful to compare the PWM input parameters with the corresponding PWM output parameters. To perform this comparison the accuracy, minimum and maximum duty cycle and maximum $f_{\text {PWм }}$ of the PROFET ${ }^{\text {TM }}+$ must be known. An example of this comparison is shown in Table 9. Improved accuracy and resolution has been realized with better device symmetry (see Chapter 7.4). This can be measured by the introduction of $\Delta t_{\mathrm{SW}}$, the turn-ON/OFF matching parameter.

Table 9 PROFET ${ }^{\text {TM }}+$ PWM Timing Limitation

| Parameter | Symbol | Formula | $\begin{aligned} & f_{\mathrm{PWM}}= \\ & 100 \mathrm{Hzz} \end{aligned}$ | $\begin{aligned} & f_{\mathrm{PWM}}= \\ & 200 \mathrm{HZz} \end{aligned}$ | $\begin{aligned} & f_{\mathrm{PWM}}= \\ & \mathbf{4 0 0 H z} \end{aligned}$ | $\begin{aligned} & f_{\mathrm{PWM}}= \\ & 1 \mathrm{kHz} \end{aligned}$ | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Period | $T_{\text {PWM }}$ | $1 / f_{\text {PWM }}$ | 10 | 5 | 2.5 | 1 | ms |
| $\underline{\text { min duty cycle at the output }}$ | $d_{\text {OUT_MIN }}$ | $t_{\text {OFF_delay }} / T_{\text {PWM }}$ | 0.8 | 1.6 | 3.2 | 8 | \% |
| min duty cycle at the input | $d_{\text {IN_MIN }}$ | $t_{\mathrm{ON}} / T_{\text {PWM }}$ | 2.5 | 5 | 10 | 25 | \% |
| max duty cycle at the output | $d_{\text {OUT_MAX }}$ | $t_{\text {ON_delay }} / T_{\text {PWM }}$ | 99.2 | 98.2 | 96.8 | 92 | \% |
| max duty cycle at the input | $d_{\text {IN_MAX }}$ | $t_{\text {OFF }} / T_{\text {PWM }}$ | 97.5 | 95 | 90 | 75 | \% |
| Accuracy | $a_{\text {PWM }}$ | $\Delta t_{\text {SW }} / 2 T_{\text {PWM }}$ | 0.5 | 1 | 2 | 5 | \% |

It is important to note that the resolution is mainly determined by the software and the microcontroller. PROFET ${ }^{\text {TM }}$ + will have an influence on the accuracy of the resolution only.

### 7.7 Thermal Considerations

PROFET ${ }^{\text {TM }}+$ devices are embedded in exposed pad packages. Exposed pad packages offer excellent thermal resistance ( $Z_{\text {TH(JA) }}$ characteristics) between the junction and the case compared with non-exposed pad packages. PROFET ${ }^{\text {TM }}+$ devices in exposed pad packages also have better immunity to variations in the power supply and power surges. Limitations to the system are based on two different thermal aspects:

### 7.7.1 Maximum Junction Temperature

PROFET ${ }^{\text {TM }}+$ should be kept below $T_{\mathrm{J}(\mathrm{SC})}=150^{\circ} \mathrm{C}$. Equation (10) expresses this constraint mathematically.

$$
\begin{equation*}
\mathrm{P}_{\mathrm{MAXTJ}}=\frac{\mathrm{T}_{\mathrm{J}(\mathrm{SC})}-\mathrm{T}_{\mathrm{MODULE}}}{\mathrm{R}_{\mathrm{THJA}}} \tag{10}
\end{equation*}
$$

A minimum of 1 W (high ambiente temperature and/or bad cooling) and a maximum 2 W are seen. Typically a maximum of 1.4 W gives good results.

### 7.7.2 Maximum Case Temperature

PROFET ${ }^{T M}$ + case temperature should be kept below the destruction temperature of the PCB. This is application dependent. As an umbrella specification, Infineon uses max $T_{\mathrm{C}}=130^{\circ} \mathrm{C}$ for standard FR4. Equation (11) expresses this constraint mathematically.

$$
\begin{equation*}
\mathrm{P}_{\text {MAXTC }}=\frac{\mathrm{T}_{\mathrm{CMAX}}-\mathrm{T}_{\text {MODULE }}}{\mathrm{R}_{\mathrm{THJA}}-\mathrm{R}_{\text {THJC }}} \tag{11}
\end{equation*}
$$

### 7.7.3 Maximum Power in PROFET ${ }^{T M}+$

The maximum power a PROFET ${ }^{T M}$ + can handle in an application is limited by the lesser of these two quantities, $P_{\text {MAXTJ }}$ and $P_{\text {MAXTC. }}$. Table 10 provides some examples of how $P_{\text {MAXTJ }}$ or $P_{\text {MAXTC }}$ limit the maximum power of the device for different values of ambient temperature and different thermal resistances. A maximum PCB temperature of $130^{\circ} \mathrm{C}$ is assumed.

Table 10 Comparison between Exposed and Non Exposed Package with PCB Limitation $=130^{\circ} \mathrm{C}$

| Ambient Temp | Package | $\boldsymbol{R}_{\text {THJC }}$ | $\boldsymbol{R}_{\text {THJA }}$ | Max power due to PCB temperature ${ }^{1)}$ | Maximum power due to junction temperature ${ }^{2)}$ | Maximum power |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 85 | Exposed | 1 | 30 | 1.6 | 2.2 | 1.6 |
|  | Exposed | 1 | 40 | 1.2 | 1.6 | 1.2 |
|  | Exposed | 1 | 50 | 0.9 | 1.3 | 0.9 |
|  | Standard | 15 | 50 | 1.3 | 1.3 | 1.3 |
|  | Standard | 15 | 60 | 1.0 | 1.1 | 1.0 |
|  | Standard | 15 | 70 | 0.8 | 0.9 | 0.8 |
| 105 | Exposed | 1 | 30 | 0.9 | 1.5 | 0.9 |
|  | Exposed | 1 | 40 | 0.6 | 1.1 | 0.6 |
|  | Exposed | 1 | 50 | 0.5 | 0.9 | 0.5 |
|  | Standard | 15 | 50 | 0.7 | 0.9 | 0.7 |
|  | Standard | 15 | 60 | 0.6 | 0.8 | 0.6 |
|  | Standard | 15 | 70 | 0.5 | 0.6 | 0.5 |

1) $T_{\mathrm{C}}<130^{\circ} \mathrm{C}$
2) $T_{J}<150^{\circ} \mathrm{C}$

## $7.8 \quad$ Inverse Current

There are four main reasons for inverse currents in an application. The reasons are: driving of a capacitive load; output wired to the battery (on purpose or by accident), driving an inductive load, and severe alternator ripple.

### 7.8.1 Capacitive Load

Figure 45 shows a typical case where inverse current can be observed.


Figure 45 Capacitve Load and Inverse Current Illustration
$C_{\mathrm{L}}$ is charged up to voltage $V_{\text {OUT }}$. An inrush current $I_{\text {BAT_ECU }}$ applied inside the module induces a voltage drop $V_{\text {BAT_DROP }}$ in the module's supply wiring. The consequence of this is that $V_{\mathrm{S}}$, the voltage supply of the module can drop below $V_{\text {OUT }}$. During a severe $I_{\text {BAT_ECU }}$ inrush event, the difference between $V_{\text {OUT }}$ and $V_{\mathrm{S}}$ can be sufficient to activate the internal parasitic diode ( $V_{\text {BAT_DROP }}>V_{\text {diode }}$ e.g. 300 mV ) or use the $R_{\mathrm{DS}(\mathrm{ON})}$ of the power DMOS to cause $I_{\mathrm{INV}}$ current to flow.

### 7.8.2 Output wired to Battery

A short circuit to battery is very similar to the capacitive load except that a permanent inverse current can be assumed. With a short circuit to the battery, $V_{\text {OUT }}$ is $V_{\text {BAT }}$. $V_{\text {BAT_DROP }}$ can be more than 300 mV permanently which can create extra stress on the switch. Refer to Chapter 6.2.

### 7.8.3 Inductive Load

With an inductive load, such as an H bridge motor, the current can freewheel in either the low side or the high side of the bridge again causing and inverse current to flow in the switch.

### 7.8.4 Alternator Ripple

Ripple caused by the alternator is common and is most noticeable when the alternator has a large load current. As an umbrella specification, Infineon uses a ripple of 3 V peak to peak at the module supply $V_{\mathrm{S}}$, with a frequency of minimum 1 kHz , maximum 20 kHz . During the negative slope of the ripple, the capacitor, $C_{\mathrm{L}}$ can be sufficient to provide current to the load. In this situation, the switch is ON and the current is slowly decreasing until crossing 0 and continuing in a negative direction, limited by the $R_{\mathrm{DS}(\mathrm{ON})}$ or the body diode of the switch. Figure 46 shows this

App. Note
situation, assuming a 3 A resistive load decoupled with a $50 \mu \mathrm{~F}$ capacitor and a ripple frequency of 1 kHz ripple. This example is based on the BTS5045-2EKA.


Figure 46 Alternator Ripple. Voltage and Current of PROFET ${ }^{\text {TM }}+$ with Capacitor as Load $^{\text {P }}$

### 7.8.5 Consequences for PROFET ${ }^{\text {TM }}$

During inverse current, due to internal parasitic behavior, two kinds of phenomenon can be observed. With a large inverse current $I_{\mathrm{INV}}$, well above the nominal current of the device, $I_{\mathrm{L}(\mathrm{NOM})}$, a parasitic switch ON or OFF of a neighboring channel can be seen (in devices with two or more channels of course). The second effect, described in Figure 47 is where the DMOS power switch will not turn ON if the input on the IN pin is changed to high while the inverse current is flowing (see case 3). In all other cases, the MOSFET switches according to the IN pin logic level. The inverse current also impacts the diagnosis behavior. Refer to Chapter 9. The parameter $I_{\mathrm{L}(\mathrm{INV})}$ in datasheet represents the current below which no parasitic behavior of a neighboring channel or parasitic diagnosis is observed.


Figure 47 Behavior of PROFET ${ }^{\text {TM }}$ + in Inverse Current

## 8 Protection

A comprehensive set of protection functions are one of the most important features offered by PROFET ${ }^{\text {TM }}+$ switches.

### 8.1 Band gap

PROFET ${ }^{\text {TM }}+$ have an embedded band gap reference. Although the band gap reference is not a protection circuit in itself, most of the protection circuits rely on this reference voltage. The band gap voltage is $V_{\mathrm{BG}}=1.25 \mathrm{~V}$. The accuracy is $4 \%$ over temperature and supply voltage.

### 8.2 Short Circuit to Ground

As mentioned previously (refer to Chapter 6.1), a short circuit to GND is the most likely short circuit event in a vehicle. As a result, PROFET ${ }^{\text {TM }}+$ devices embed several mechanisms to protect against short circuits to ground.

### 8.2.1 PROFET $^{\text {TM }}+$ Current Limitation

As with all types of power MOSFET technology, the DMOS switch in PROFET ${ }^{\text {TM }}+$ should not exceed a certain power or current density. The power density reflects the power in the DMOS switch per unit of surface area. Since the power $P_{\text {MOS }}=V_{\mathrm{DS}}{ }^{*} I_{\text {MOS }}$, and $P_{\text {MOS }}$ is limited to a constant, the $I_{\text {MOSMAX }}$ the DMOS can handle is then given by Equation (12).

$$
\begin{equation*}
\mathrm{I}_{\mathrm{MOSMAX}}=\frac{\mathrm{P}_{\mathrm{MOS}}}{\mathrm{~V}_{\mathrm{DS}}}=\frac{\text { Constante }}{\mathrm{V}_{\mathrm{DS}}} \tag{12}
\end{equation*}
$$

Interestingly, with such an equation, a OV drop voltage will lead to an infinite current. Obviously, this is theoretical only, and the real current limitation, for low voltage drop, is related to wire bonding. The bonding cannot support more current than a certain fixed value. The constraints, linked to the technology looks as the given curve Figure 48. The blue curve matches the MOSFET power density only. The red curve sketches the overall device limit. The protection concept should guarantee to limit the current below the device system limitation.


Figure 48 Power DMOS and Package SOA

### 8.2.2 PROFET $^{\text {TM }}+$ Current Limitation Concept

PROFET ${ }^{\text {TM }}+$ devices limit the current flowing through the DMOS switch. The reason for limiting instead of tripping, is due to the fact that PROFET ${ }^{\text {TM }}+$ devices are designed to drive lamps. As described in Chapter 5.1.3, lamps have a significant inrush current at turn ON. To ensure a lamp is turned ON in the worst case scenario, it is necessary to allow this inrush current to flow for a short period of time. The current limitation looks as described on Figure 49, the blue colors reflecting the tolerance.


Figure 49 Current Limitation
As described in Table 4, each lamp has an inrush. Figure 50 shows the consequence for the PROFET ${ }^{\text {TM }}+$ when $^{\text {wh }}$ turning on a lamp. The orange line represents the inrush current of the bulb. The device will be considered suitable for a lamp when the $I_{\text {INRUSH }}$ will not touch the low current limitation (risk of accelerated aging) hence it may touch the high limit one when $V_{\mathrm{Ds}}$ is smaller 3 V . In that case, a restart due to an over temperature swing can be observed.


Figure 50 Turning ON 2*27W+5W with BTS5020-2EKA. Inrush versus Current Limitation

Protection

### 8.2.3 Temperature Swing Limitation

Severe temperature gradients on chip cause significant thermo mechanical stress and aging of the device to the point of destruction. The smaller the temperature gradient, the higher the number of cycles the PROFET ${ }^{\text {TM }}+$ can withstand. A temperature swing of 60Kelvin minimum is a good compromise value to use for lamp turn ON and to protect against severe short circuits. Figure 51 shows the hardware realization of the $2 \times 20 \mathrm{~m} \Omega$ BTS5020-2EKA. Two temperature sensors, one measuring the DMOS, one measuring the chip temperature are compared. The channel turns OFF when a too high temperature gradient is reached. To guarantee the functionality accuratly, variation due to temperature and production spread is greatly reduced thanks to the use of the internal band gap reference.


Figure 51 Temperature Swing Limitation Concept

### 8.2.4 Maximum Temperature Limitation

The device (chip + package) is qualified for junction temperature up to $T_{\mathrm{J}}=150^{\circ} \mathrm{C}$ continuous. Above, the over temperature sensor of the chip is met. This sensor is typically activated at a temperature of $T_{\mathrm{J}}=175^{\circ} \mathrm{C}$. The hardware designer should guarantee with its thermal design the device to operate below $T_{J}=150^{\circ} \mathrm{C}$ by verifying Equation (10).

### 8.2.5 Restart Strategy

During the switch ON phase of a cold lamp, with a high battery voltage, the temperature rise in the device can be higher than 60K. To ensure that the lamp is turned ON in less than 30ms (refer to Chapter 5.1.3), even under these conditions, a restart strategy is implemented. When the temperature swing reaches $T_{\text {SWING }}=60 \mathrm{~K}$ min, the device switches OFF for protection. When the temperature has decreased to $T_{\text {SWING_HYS }} 75 \%$ of $T_{\text {SWING }}$, the device restarts. $75 \%$ has been tested and confirmed as the best value to improve short circuit robustness, as well as the most efficient to switch ON the load. Figure 52 shows a typical restart phase.

Protection


Figure 52 DMOS Temperature Behavior during Restart Phase

### 8.2.6 PROFET $^{\text {TM }}+$ Life Time Limitation

Although significant design effort has been put into protecting against a short circuit to GND, PROFET ${ }^{\text {TM }}+$ devices are not indestructible. To protect the device, it is necessary to limit the number of restarts to a minimum. Refer to Figure 53. The measured acceptable number of thermal event restart is in range of 5 to 20 maximum restart. The application software should monitor the diagnostic line of the PROFET ${ }^{T M}+$ shortly after switch ON and limit the restart time ( $t_{\text {RESTART }}$ ) if necessary. The recommended value is $t_{\text {RESTART }}=100 \mathrm{~ms}$ mini, 300 ms maxi, which results in a range of $N=10$ to 20 , depending on the PROFET ${ }^{\top M}+$ cooling. If this type of strategy is not implemented, the number of short circuit events that a PROFET ${ }^{\text {TM }}+$ can handle will be limited.


Figure 53 Number of Restart Limitation
Thanks to this strategy, the definition of short circuit is as follows: If after $t_{\text {RESTART }}$ or N restarts, the device is still reporting a short circuit, a short circuit condition exists.

### 8.2.7 Activation Limitation

Figure 54 provides a picture of a BTS5241L which has been exposed to repetitive short circuit stress. The channel on the right hand side has not experienced any events while the other channel has experienced thousands of repetitions. This provides a visual confirmation of the aging effect due to repetitive short circuit events.


Figure 54 Device Exposed to Short Circuit Stress

As soon as a short circuit is detected, a plausibility check should be performed. This is achieved by changing the IN pin status from LOW to HIGH again to ensure the diagnosis is correct. If a certain number of short circuit events are detected, the system should then inhibit the function controlled by the switch until the next ignition cycle of the vehicle starts.
To implement this strategy, a counter $C_{\text {DRIVE }}$ has to be created. $C_{\text {DRIVE }}$ is used to count the number of short circuit events each PROFET ${ }^{\text {TM }}+$ output has encountered in an ignition cycle (a short circuit cycle corresponds to an event where after $T_{\text {RESTART }}$, the device is still in short circuit). When $C_{\text {DRIVE }}$ reaches a predefined value, the load is inhibited (i.e. no further activation).
Another counter, $C_{\text {LIFE }}$ is then incremented. $C_{\text {LIFE }}$ should be stored in a non volatile memory such as Flash or E $^{2}$ Prom. Infineon provides the quantity $C_{\text {DRIVE }}{ }^{*} C_{\text {LIFE }}$ in datasheet based on the short circuit robustness test. In Chapter 5.4 a rough clustering of loads or load families based on the number of activations per ignition cycle was given. Although the final decision always rests with the OEM, Table 11 provides suggested values for $C_{\text {DRIVE }}$ for a given load family.
Table 11 Load Family, Function of Engine Ignition

| $\mathbf{N}^{\circ}$ of driver <br> activation | Load example | Average activation <br> time | Plausibility check <br> realized by | Inhibition after <br> $\boldsymbol{C}_{\text {DRIVE }}$ |
| :--- | :--- | :--- | :--- | :--- |
| High | Brake light | $<1 \mathrm{mn}$ | Car driver | 3 to 5 |
| High | Low beam | $>1 \mathrm{mn}$ | Car driver | 3 to 5 |
| Mid | Interiors | $>1 \mathrm{mn}$ | Application | 5 |
| Mid | Low beam | $>1 \mathrm{mn}$ | Application | 5 to 10 |
| Low | High beam | $>1 \mathrm{mn}$ | Application | 5 to 10 |

Using Table 11, a software strategy can be implemented based on the number of activations per ignition cycle, the average driver usage as well as the length of time of activation. A load which is known to be used often will not need an automated retry. A load which is activated once in a while but for long periods of time will need an automated retry. Figure 55 shows these two possibilities. $T_{\text {WAIT }}$ is usually selected by the OEM. (in the range of 1 s to 2 mn ). Figure 56 shows a suggested software flow chart.

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Protection


Figure 55 Software Strategy


Figure 56 Short Circuit Software Strategy

### 8.3 Short Circuit to Battery

A short circuit to the battery can be a very stressful event for a PROFET ${ }^{T M}+$ device. Refer to Chapter 6.2 and Chapter 7.8. Several workarounds can be implemented with the best solution being to place a diode in series with the output. While this solution is good in theory, the cost is often prohibitive. An alternative strategy is to guarantee that no excessive current will flow in the device. To implement this, the system must perform a short circuit to battery test. If a short circuit to the battery is indicated, the battery supply line of the PROFET ${ }^{\text {TM }}+$ must not be switched OFF. If the battery's supply line is not available (for example due to a blown fuse), the alternative is to use a semiconductor which will perform intelligent restart. At last, turn-OFF every device connected to the faulty supply line in order to reduce the inverse current in the body diode. The three solutions are summarized in Figure 57.


Figure 57 Short Circuit to Battery Protection Possibilities

### 8.4 Open Load

Open Load is not considered has a destructive case for the device.

### 8.5 Loss of battery

The loss of the battery while the switch is ON has no influence on device's robustness when load and wire harness are purely resistive. In the case of inductivity, the energy stored in the inductance brings additional issues which should be handled with care. Figure 58 shows the system set up in that case.


Figure 58 Loss of inductive load
Due to the inductivity, the current searches the easiest (lowest ohmic) path to flow. This path consists in the freewheeling of the GND circuitry and of the over voltage $Z_{D(A Z)}$ diode. For that reason, it is necessary to let the current flow in the opposite direction in the GND circuitry, otherwise thousands of Volt will be seen at the pins. The power DMOS is big enough to handle the energy, the $Z_{\mathrm{D}(\mathrm{AZ})}$ diode is less robust. An equivalent robustness would mean a GND DMOS as big as the power DMOS which is financially not sustainable. PROFET ${ }^{\text {TM }}+$ devices handles inductivity of the wire harness, up to $10 \mu \mathrm{H}$ with the nominal current of the given device. In the case of applications where currents and / or the inductivity should be exceeded, an external freewheeling diode, in parallel to the device or in parallel to the load is necessary to handle the energy.

### 8.6 Short Circuit Between Loads

Short circuit between loads is usually detrimental to the application affecting PCB traces, connectors and wiring. For PROFET ${ }^{\text {TM }}+$, the consequences depend mainly on which additional load is added by the short circuit.
As extreme example, a 55 W lamp which is short circuited to a 5 W lamp will bring no difference to the 55 W PROFET ${ }^{\text {TM }}$ BTS6143D driver while the 5W PROFET ${ }^{\text {TM }}+$ BTS5180-2EKA driver will effectively be short $^{\text {B }}$ circuited to ground.
Thanks to the embedded temperature swing limiter and restart strategy, the PROFET ${ }^{\mathrm{TM}}+$ will be able to turn the over-load inrush ON. If the ambient temperature is below the maximum ambient temperature the system is designed for, the PROFET ${ }^{\text {TM }}+$ will either go into thermal shutdown very late or not at all. Nevertheless, it's life expectancy will be reduced by the over current events.
To define the maximum current acceptable for a device the $Z_{\mathrm{TH}(\mathrm{JA})}$ information must be known. Any current which is applied for a period of time and leads to a temperature swing of more than 60 K is considered to be outside the nominal range. This current will accelerate the ageing of the PROFET ${ }^{\text {TM }}+$. As an example, Figure 59 shows the maximum current that can be handled by each PROFET ${ }^{T M}+$.

Protection


Figure 59 Typical Couple Current / Time to 60K Temperature Swing

### 8.7 UndervoItage

A low supply voltage condition brings two challenges which must be addressed, protection and switching capability. Refer to Figure 60.

### 8.7.1 Protection

Thanks to the internal band gap (BG) reference, PROFET ${ }^{\text {TM }}+$ devices are protected in under-voltage conditions. A valid band gap allows the device to turn ON. In this case, all protection mechanisms are functional. An invalid band gap, due to insufficient supply voltage causes the PROFET ${ }^{\text {TM }}+$ to turn OFF. When the BG is valid, the charge pump (CP) voltage is not necessarily valid, however, the charge pump is monitored and BG will prevent switch from turning ON when the CP voltage is invalid.

### 8.7.2 Switching Capability

The capability of a PROFET ${ }^{T M}+$ to turn ON and to reach the correct $R_{\mathrm{DS}(\mathrm{ON})}$ area is based on the charge pump's capability to drive the gate of the power DMOS transistor (refer to Chapter 7.3). This is defined in the data sheet by the supply voltage $V_{\mathrm{S}}$ being the range $V_{\text {NOM }}$. When the supply voltage $V_{\mathrm{S}}$ is below this range, the situation prior to reaching the under-voltage zone is of primary importance. If $V_{\mathrm{s}}$ is decreasing, the device is kept ON down to a threshold in the range of $V_{\mathrm{S}(\mathrm{UV})}$. This is assuming the IN pin is kept to a HIGH level. If $V_{\mathrm{s}}$ is increasing, the device will switch ON when $V_{\mathrm{S}}$ reaches the threshold $V_{\mathrm{SOP}(\text { min })}$. Figure 60 shows the behavior in the three areas of supply voltage with respect to time.

Protection


Figure 60 Behavior during Undervoltage Reset and Ramp up test

### 8.7.3 Ignition

During ignition, and depending on the OEM minimum voltage $V_{\text {CRK_MIN }}$, a switch which was previously ON can turn OFF. Refer to Figure 61. When the $V_{S}$ voltage rises again, the switch will automatically restart and turn ON if the IN pin is kept in the high state. During $t_{\mathrm{LAUNCH}}, V_{\mathrm{S}}$ can be below $V_{\mathrm{S}(\mathrm{OP}) \text { min }}$. As a consequence, the $R_{\mathrm{DS}(\mathrm{ON})}$ can be higher than specified. To avoid an intermediate state, every PROFET ${ }^{T M}+$ is tested to provide a voltage drop of less than 1.5 V .


Figure 61 Ignition Pulse and PROFET ${ }^{\mathrm{TM}}$ + Behavior

### 8.7.4 Low Battery Voltage Phase

During a low battery condition, a parasitic under-voltage turn OFF could occur, especially if a capacitive load with $I_{\text {INRUSH }}$ peak current has to turn ON or if there is a short circuit to GND. Since the wiring is inductive, $I_{\text {INRUSH }}$ will produce a $V_{\text {DROP }}$ voltage. Refer to Figure 62. $V_{\text {DROP }}$ can be estimated by Equation (13).

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$R$ and $L$ are the respective resistance and inductance of the supply line. $\Delta t$ corresponds to the $\mathrm{PROFET}^{\mathrm{TM}}+$ switching time. $I_{\text {INRUSH }}$ is the worst case peak current of the short circuit current or current limitation. As umbrella specification, Infineon consider $L=10 \mu \mathrm{H}, \mathrm{R}=20 \mathrm{~m} \Omega$. Refer to Table 12 for expectable voltage drop during $I_{\text {INRUSH }}$.

$$
\begin{equation*}
\mathrm{V}_{\text {DROP }}=\mathrm{L} \times \frac{\mathrm{I}_{\text {INRUSH }}}{\Delta \mathrm{t}}+\mathrm{R} \times \mathrm{I}_{\text {INRUSH }} \tag{13}
\end{equation*}
$$



Figure 62 Low Battery Voltage Condition. Inrush and Inductive Wiring Influence

Table 12 Load and Maximum Instantaneous Expectable Voltage Drop

| Load (W) | Inrush (A) | Maximum Voltage Drop (V) |
| :--- | :--- | :--- |
| 5 | 5 | 0.35 |
| 7 | 7 | 0.5 |
| 10 | 9 | 0.65 |
| 15 | 14 | 1 |
| 21 | 22 | 1.5 |
| 27 | 26 | 1.9 |
| $2^{*} 27+5$ | 57 | 4 |
| $3^{* 27+5}$ | 85 | 6 |
| 55 | 50 | 3.5 |
| 65 | 60 | 4.2 |

### 8.8 Overvoltage

Overvoltage is considered to be everything above $V_{\mathrm{BAT}(\mathrm{SC})}$. As described in Chapter 4.1.5, the main causes of over voltage are external jump start and load dump. ISO pulses are described separately in Chapter 14.1.

### 8.8.1 Jump Start

Jump start is usually not a stressful situation. The only situation in which PROFET ${ }^{\text {TM }}+$ devices cannot cope during a jump start is during a simultaneous short circuit to GND at the output. This is considered a double fault, and it is not usually required to survive such a coincidence. In this case, the device will survive a single short circuit event. Turning OFF the load is recommended when the voltage increases above $V_{\mathrm{BAT}(\mathrm{SC}) \text {. If the load is a lamp, this }}$ procedure is even recommended to maintain the life time of the bulb.

### 8.8.2 Load Dump

Load dump is an extreme application scenario for a PROFET ${ }^{\text {TM }}+$ and can be destructive test due to thermal overstress. Refer to Figure 63. As soon as the $V_{\mathrm{S}}$ potential is higher than $V_{\mathrm{S}(\mathrm{AZ)}}, V_{\mathrm{IS}(\mathrm{AZ})}$ or $V_{\mathrm{DS}(\mathrm{AZ)}}$, the respective Zener diode conducts. The temperature and current coefficients are positive which means that all the Zener diodes are conducting almost at the same time. The load dump is specified with $R_{1}$ (internal load dump generator resistor) which will limit the current. Note that this resistor is OEM dependant. The $I_{\text {Sov }}$ current flows via the sense protection Zener $Z_{\text {IS(AZ) }}$, the logic protection Zener $Z_{\mathrm{D}(\mathrm{AZ})}$, and the power stage Zener $Z_{\mathrm{DS}(\mathrm{AZ)}}$.
To define the robustness of the system against load dump, the currents and voltages of Figure 63 must be solved (Millman theorem helps). When this is complete, a power calculation can be done to determine if the system is capable of handling the total energy. Resistors $R_{\mathrm{IS}}, R_{\mathrm{IN}}$ and $R_{\mathrm{GND}}$ are used to limit the current ( $I_{\mathrm{SOV} \text { _SENSE }}, I_{\mathrm{DESD}}$, $I_{\text {SOVLOGIC }}$ respectively). It is important to note that in a load dump situation, the load is activated and some current $I_{\text {SOV_LOAD }}$ flows. The choice of $R_{\text {GND }}$ is explained in Chapter 10.1.


Figure 63 Over Voltage Protection. Example with 60V

### 8.9 Reverse Polarity

In reverse polarity situations where loads have symmetrical characteristics, such as lamps or resistors, the current is allowed to flow through the load and the DMOS body diode. For loads such as inductive loads (motors, relays, etc..) special care must be taken to ensure safe operation.

### 8.9.1 Loads with Symmetrical Polarity Characteristics

Refer to Figure 64. The following currents must be considered and limited with resistors :

- $I_{\mathrm{DS}(\mathrm{REV})}$ :The parasitic body diode of the power DMOS is conducting. This means that current will flow in the load. The load will actually limit the current in the body diode power DMOS.
- $I_{\text {SREV_LoGIC }}$ : This current will flow in Zener $Z_{\mathrm{D}(\mathrm{AZ)}}$, which acts as a diode.
- $I_{\mathrm{D}_{-} E S D}$ : Since the pin GND is at a diode voltage $\left(Z_{\mathrm{D}(\mathrm{AZ)}}\right)$ above GND and the IN pin is more or less at battery potential, the $Z_{\mathrm{DESD}}$ diode should be protected with a resistor $R_{\mathrm{IN}}$. (this is valid for all the logic pins).
- $I_{\text {IS(REV) }}$ : Via the sense resistor, the current will flow in the $Z_{\text {IS(AZ) }}$ Zener which will act as a diode.


Figure 64 Reverse Polarity Protection with Symetrical Polarity Load. Example with 16V

### 8.9.2 Reverse Polarity Protection for the Load

There are many applications where the methods of protection against applied reverse polarity described above cannot be used. Some examples are: the load is in a DMOS bridge; the load has an integrated freewheeling diode; the load itself must be protected from wrong polarity as electrochemical capacitors; the load consists of an inductance with PWM regulated current or the load has a small resistive component. In all of these cases, it is necessary to block the current.

## 9 Diagnostics

The diagnostic functions embedded in the PROFET ${ }^{\text {TM }}+$ is a function getting increasing importance driven by LED and short circuit to GND requirements. PROFET ${ }^{T M}$ + devices use a current sense method to offer complete diagnostic coverage over the output current range. Diagnostics are synchronized with the input, meaning the PROFET ${ }^{\text {TM }}+$ always provides the status of the present state of the power DMOS and the logical signal IN i.e. there is no memory effect.

### 9.1 Current Sense

Current sense is implemented using a current generator which provides a current proportional to the load current $I_{\mathrm{L}}$. The ratio between $I_{\mathrm{IS}}$ and $I_{\mathrm{L}}$ is called $k_{\mathrm{ILIS}}$. When a failure occurs the current generator is set to $I_{\mathrm{IS}(\mathrm{FAULT})}$, the maximum sense current the current generator can provide.
Refer to Figure 66. The current sense generator is based on the $P$ channel MOSFET T4. The gate of T4 is driven by op-amp OPA which set the voltage at T4 gate equal to the output voltage. The sense feed consists of the DMOS transistor T2, which is not connected to the output, but supplies T4 only. As with all current generators, the current sense is connected to a voltage supply, here $V_{\mathrm{S}}$. This means that the voltage at the $I_{\mathrm{S}}$ pin, $V_{\text {IS }}$ should always be smaller than $V_{\text {IS(RANGE) }}$ min, otherwise the current generator cannot provide the required current.
The maximum current supplied by the current generator is given by the parameter $I_{\mathrm{IS} \text { (FAULT) }}$. The size of T4 determines the value of $I_{\text {IS(FAULT) }}$. There is no current limit mechanism or thermal sensor for T4 hence the system designer should ensure that T4 is adequate protected. T1 provides protection against over voltage and ESD by acting as a Zener diode. One limitation of T1 is that two PROFET ${ }^{\text {TM }}+$ with different battery feeds can not share a common sense line. This could result in one of the PROFET ${ }^{T M}+$ supplying the other one through transistor T 1 .


Figure 66 Current Sense Generator

App. Note

Diagnostics

### 9.2 Gate Back Regulation

PROFET ${ }^{\text {TM }}+\mathrm{s}$ use gate back regulation (GBR). The aim of GBR is to improve the current sense accuracy at low load current.

### 9.2.1 Influence on the Power Stage

The GBR monitors the drain source voltage $V_{\mathrm{Ds}}$. As $V_{\mathrm{Ds}}$ is gets low, the gate driver partially reduce the gate voltage to increase the channel resistance. $V_{\mathrm{DS}}$ is limited to $V_{\mathrm{DS}(\mathrm{NL})}$. Figure 67 graphs the $V_{\mathrm{DS}}$ voltage on the left hand side with and without GBR as a function of the load current. On the right hand side is a graph of the artificial $R_{\mathrm{DS}(\mathrm{ON})}$ for low load currents. These graphs are based on the BTS5020-2EKA.


Figure 67 Gate Back Regulation Influence on Voltage Drop. ${ }^{\text {1 }}$

### 9.2.2 Sense Accuracy Improvement

The main purpose of GBR is to improve the $k_{\text {ILIS }}$ accuracy at low load current. Equation (15) is used to calculate the current sense ratio $k_{\text {ILIS }}$ where:
$V_{\text {OFFSET }}$ is the parasitic offset voltage of the op-amp. (it can be negative or positive)
$V_{\mathrm{DS}}$ is the voltage drop in the power MOSFET which is $R_{\mathrm{DS}(\mathrm{ON})}{ }^{*} I_{\mathrm{L}}$.
$k_{\text {ILISO }}$ is the target central value.

$$
\begin{equation*}
\mathrm{k}_{\mathrm{ILIS}}=\mathrm{k}_{\mathrm{iILIS} 0} \times \frac{1}{1+\frac{\mathrm{V}_{\mathrm{OFFSET}}}{\mathrm{~V}_{\mathrm{DS}}}} \tag{14}
\end{equation*}
$$

From this equation, when the load current $I_{\mathrm{L}}$ is going to 0 , the $k_{\text {IILIS }}$ spread is increased to infinite because $V_{\mathrm{DS}}=$ 0 V . GBR compensates for this behavior by limiting $V_{\mathrm{DS}}$ to $V_{\mathrm{DS}(\mathrm{NL})}$. Figure 68 provides the famous $k_{\text {IIIS }}$ trumpet, with and without gate back regulation.

[^0]

Figure 68 Gate Back Regulation Influence on $\boldsymbol{k}_{\text {ILIS }}$ accuracy, in \%

### 9.2.3 Sense Resistor

Refer to Chapter 10.3.

### 9.3 Short Circuit to Ground

### 9.3.1 Short Circuit to Ground in OFF State

Note that short circuit to GND in OFF state cannot be detected. When this failure occurs, the PROFET ${ }^{\text {TM }}+$ does not report a fault condition.

### 9.3.2 Short Circuit to Ground in ON State

A short circuit to ground in the ON state is detected by the logic as one of the three logic signals, "over current OC", which comes from current limitation circuitry, "over temperature OT" which comes from the temperature sensor and "over temperature swing OTS" which comes from the temperature swing sensor. As soon as one of these three logic signals is high, the PROFET ${ }^{\text {TM }}+$ is considered to be in a stressful situation which will result in an activation of the sense signal $I_{\text {IS(FAULT) }}$.
Figure 70 describes the different signals involved on a large time scale, from the power DMOS transistor $T_{\text {MOSFET }}$ temperature and $I_{\mathrm{L}}$ load current to the logic signals shows for different failures.
It is interesting to zoom in on the point where the device restarts. At this point, the power DMOS transistor switching ON and the load current has not yet reached the $I_{\mathrm{L}(\mathrm{SC})}$ current limitation. In this situation, the OC signal is not set to 1 and the OT or OTS are at 0 . Without filtering, this would lead to a glitch in the output from HIGH to LOW to HIGH. To avoid this, a small delay is embedded into the PROFET ${ }^{\text {TM }}+$. This delay is defined by the parameter $t_{\text {sIS(OT_blank). }}$. Refer to Figure 69.


Figure 69 Short Circuit to GND Logic


Figure 70 Hard Start Timing

### 9.3.3 Observable Parasitic Effect of the Strategy

This concept can exhibit parasitic diagnostics due to extreme temperature or load current conditions.

### 9.3.3.1 Very high Ambient Temperature

If the ambient temperature reaches a very high level and the switch is ON, a nominal current can be sufficient to activate the maximum over temperature sensor. In this case, the current sense will oscillate between nominal and $I_{\text {IS(FAULT) }}$. Refer to Figure 71.


Figure 71 Very High Ambient Temperature Diagnostic Parasitic Effect

### 9.3.3.2 High Load Current

If the load current is significantly high (Refer to Figure 59) in a cold temperature environment, this can be enough to activate the OTS sensor. This will result in the same behavior as for the previous case i.e. the $I_{I S}$ pin can toggle.

### 9.4 Short Circuit to Battery

### 9.4.1 Short Circuit to Battery in OFF State

During a short circuit to the battery in OFF state, the output voltage of the PROFET ${ }^{\text {TM }}+$ rises up to $V_{\text {BAT }}$. PROFET ${ }^{\text {TM }}+$ have an embedded comparator to monitor the output voltage. If this voltage rises above $V_{\text {OL(OFF) }}$, the device considers this as a fault condition and sets the sense signal accordingly. To prevent parasitic short circuit to battery diagnostic when the ouput is floating (open load), an external pull down resistor $R_{\mathrm{Sc}} \mathrm{vs}=47 \mathrm{k} \Omega$ is recommended. Refer to Figure 72.


Figure 72 Short Circuit to Battery Detection Hardware Set up

### 9.4.2 Short circuit to Battery in ON State

A short circuit to battery in the ON state is more difficult to diagnose. Fortunately, the consequence of such an event is simply that the sense current $I_{\text {IS }}$ is lower than expected. Depending on the short circuit impedance, it will be diagnosed as open load in ON or under-load. A discriminating diagnosis should then be performed in the OFF state.

### 9.5 Inverse Current

Inverse current is similar to short circuit to battery. Nevertheless, parasitic inverse current can bring additional challenges to be overcome. Refer to Figure 73. If the inverse current is too high, a parasitic current $I_{\text {IS_INV }}$ will flow at the sense pin IS.


Figure 73 Inverse Current Diagnostic

### 9.6 Open Load

### 9.6.1 Open Load in OFF State with Bulb and Inductive Load

During the OFF state, open load can be diagnosed using an external pull up resistor $R_{\text {OL }}$. Open load in OFF is detected using a comparator to check the output voltage. In normal operation, the load acts as a strong pull down. When the load connection is lost or the load blown, the output voltage is pulled up to the battery voltage through $R_{\text {OL }}$. An additional switch is usually necessary to reduce the stand by power consumption of the module during parking to prevent a permanent leakage current $V_{\mathrm{BAT}} / R_{\mathrm{OL}}$ from flowing in the load. A PNP transistor, T 1 such as a BC807 will fit this requirement. This transistor can be shared by other devices which share the same battery feed. The value of $R_{\text {OL }}$ depends on the OEM specified minimum parasitic impedance $R_{\text {DIRT }}$. As an umbrella specification, Infineon considers $R_{\text {DIRT }}$ as open load impedance $4.7 \mathrm{k} \Omega$ as a minimum value.

Knowing $R_{\text {DIRT }}$, $R_{\text {OL }}$ can be obtained by the following Equation (15) where $V_{\text {BATMIN }}$ is the minimum battery voltage during which the open load in ON diagnostic is performed. Refer to Chapter 13.2 for detailed calculation.

$$
\begin{equation*}
\mathrm{R}_{\mathrm{OL}}<\mathrm{R}_{\mathrm{DIRT}} \times \frac{1}{\left(\frac{\mathrm{~V}_{\text {BATMIN }}}{3 \mathrm{~V}}-1\right)} \tag{15}
\end{equation*}
$$

$R_{\mathrm{OL}}$ should be large enough to ensure that the power loss in this resistor can be neglected. Assuming a maximum $P_{\text {RMAX }}$ of 250 mW (pulsed during the open load diagnosis) $R_{\mathrm{OL}}$ is defined by Equation (16).

$$
\begin{equation*}
\mathrm{R}_{\mathrm{OL}}>\frac{\mathrm{V}_{\mathrm{BAT}}{ }^{2}}{\mathrm{P}_{\mathrm{RMAX}}}=\frac{\mathrm{V}_{\mathrm{BAT}}{ }^{2}}{0,25} \tag{16}
\end{equation*}
$$

$R_{\mathrm{OL}}=1.5 \mathrm{k} \Omega$ is recommended value.


Figure 74 Open Load in OFF Hardware

### 9.6.2 Open Load in OFF State with LED Module

LED modules are quite challenging to diagnose in OFF state. On one hand, the leakage current of the dirt resistance is in the mA range. On the other hand, $10 \mu \mathrm{~A}$ is sufficient to illuminate an LED. The only way to diagnose either a standard or advanced LED module is to guarantee the voltage $V_{\text {Out }}$ is below the illumination level. To achieve this, the LED module must have a resistor $R_{\text {OL_LED }}$ at the input. Refer to Figure 25 and Figure 26. This resistor is polarized by the $R_{\mathrm{OL}}$. In case of open load, the $R_{\mathrm{OL}}$ will pull up the voltage as in the case of bulb. In normal conditions, the $R_{\text {OL_LED }}$ will sink the current and limit the output voltage below the LED illumination threshold.

### 9.6.3 Open Load in ON state

To determine if a PROFET ${ }^{\text {TM }}+$ can diagnose an open load in the ON state, it is necessary to precisely define the characteristics of this condition. As described earlier, an open load in an automotive environment is the resistance $R_{\mathrm{OL}}$ as a minimum. In the case of an LED module powered from a DC/DC converter, if one LED is blown, the DC/DC converter will still consume some current. This current is defined by the OEM. As an umbrella specification, Infineon considers an open load to be a current in between of 5 to 30 mA . When the open load current range has been defined, it is easy to determine the minimum sense current considered to be an open load, using the current sense specification. Figure 75 and Table 13 shows an give open load currents considered.


Figure 75 Current Sense Accuracy at Small Load

Table 13 PROFET ${ }^{\text {TM }}$ +s Open Load Definition

|  | $\mathbf{2 0 m} \Omega$ | $\mathbf{3 0 m} \Omega$ | $\mathbf{4 5 m} \Omega$ | $\mathbf{9 0 m} \Omega$ | $\mathbf{1 2 0 m} \Omega$ | $\mathbf{1 8 0 m} \Omega$ |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| $k_{\text {ILIS }}$ ratio typical | 3000 | 2150 | 1500 | 1500 | 550 | 550 |
| $I_{\text {IS(OL) }}(\mu \mathrm{A})$ | 4 | 5.6 | 8 | 8 | 21 | 21 |
| $I_{\mathrm{L}(\mathrm{OL})} \min (\mathrm{mA})$ | 5 | 5 | 5 | 5 | 5 | 5 |
| $I_{\mathrm{L}(\mathrm{OL})} \max (\mathrm{mA})$ | 30 | 30 | 30 | 30 | 30 | 30 |

### 9.7 Partial Loss of Load

Some applications use loads in parallel which can lead to partial loss of load. Refer to Figure 30.

### 9.7.1 Partial Loss of Load during OFF state

During the OFF state, a partial loss of load caused by losing one out of X loads cannot be detected.

### 9.7.2 Partial Loss of Load during ON state

During the ON state, diagnosis of the loss of one out of X loads can be realized using the current sense function. Accuracy of the PROFET ${ }^{T M}+$, as well as the complete system accuracy can challenge the diagnosis. To answer the question "can you diagnose the loss of xW , out of yW ", it is necessary to determine the following as described in Figure 76. Red color indicates min typical and max with one load loss, Green color indicates min typical and max with nominal load.

Step 1, Which lamps are used? Different lamps have different accuracies. Refer to Chapter 5.1.
Step 2, Supply voltage range. Lamp current changes with supply voltage. Refer to Chapter 5.1
Step 3, Ground shift range. Refer to Chapter 3.5
Step 4, If PWM used and the PWM accuracy. Refer to Chapter 7.6
Step 5, Current sense conversion, $k_{\text {ILIS }}$ accuracy?
Step 6, Eventual additional leakage current on the sense line?
Step 7, Sense resistor accuracy?

Step 8, A/D converter accuracy ? A/D converter reference voltage, A/D resolution and LSB error?


Figure 76 Diagnostic of Partial Load Loss
When all of this information is known, it is possible to determine if the PROFET ${ }^{\text {TM }}+$ can diagnose a partial loss of load. Table 14 gives the required PROFET ${ }^{\text {TM }}+k_{\text {ILIS }}$ accuracy to detect the loss of specific partial loads.

Table 14 PROFET ${ }^{\text {TM }}+$ Planned Load and Diagnosis

|  | $20 \mathrm{~m} \Omega$ | $30 \mathrm{~m} \Omega$ | $45 \mathrm{~m} \Omega$ | $90 \mathrm{~m} \Omega$ | $120 \mathrm{~m} \Omega$ | $180 \mathrm{~m} \Omega$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Load | $\begin{aligned} & 2 \times 27 \mathrm{~W}+ \\ & 5 \end{aligned}$ | 2x21W | 27W+5 | 2x10W | 2x5W | 1x5W |
| Target diagnostic | 1x27W | 1x21W | 27W | 10W | 1x5W | OL |
| Accuracy | $\begin{array}{r} 10 \% \\ @ 2 A \end{array}$ | $10 \%$ <br> @ 2A | 20\% <br> @ 1A | $\begin{aligned} & 10 \% \\ & @ 500 \mathrm{~mA} \end{aligned}$ | $10 \%$ <br> @250mA | $70 \%$ $@ 20 \mathrm{~mA}$ |

### 9.7.3 Current Sense Accuracy Improvement

Sometimes, the current sense accuracy is not good enough to diagnose a required loss of load. In this case, PROFET ${ }^{\text {TM }}+$ devices offer a calibration strategy. In details, it means the application should "learn" the real $k_{\text {ILIS }}$

## Diagnostics

ratio of the given device soldered on the PCB. This value should be stored in a non volatile memory. Figure 77 describes in details the reasons for unaccuracy and compensation effects.


Figure 77 Calibration Strategy to Improve Current Sense Accuracy
Drawing 1 describes the ideal behavior expected. The load current is recopied with a certain reduction factor $k_{\text {IIIS }}$. Drawing 2 provides the missmatch in the number cells. Going back to Figure 66, the ratio between the number of cells of T1 and T2 give the $k_{\text {ILIS }}$ factor. A missmatch in the cells of T1 and / or T2 causes the $k_{\text {ILIS }}$ factor to be different to the expected theoretical value. Drawing 3 describes the influence of the non perfect offset of the opamp.
Drawing 4 shows the offset compensation via G.B.R. Drawing 5 exhibits the $k_{\text {ILIS }}$ accuracy the device can provide over temperature, production spread, supply voltage etc...
Drawing 5a demonstrates the benefit of one point calibration. During testing of the module, the micro controller learns the real sense current $I_{\text {IS_REAL }}$, at a known $I_{L_{-} \text {CAL }}$ load current for calibration. The current sense is then guaranteed to be in a conic stripe. The calibration in this case is compensating the offset of the op-amp.
Drawing 5 b demonstrates the benefit of a two points calibration. Knowing $I_{\text {IS_REAL1 }}$ and $I_{\text {IS_REAL2 }}$, giving resp. $I_{\text {L_CAL1 }}$ and $I_{L_{-C A L 2}}$, the current sense is then guaranteed to be in stripe. On top of the offset compensation, the calibration procedure has compensated the missmatch in the $k_{\text {ILIS }}$ factor.

### 9.8 Current Sense and PWM

(Refer to Chapter 7.6 for details). During PWM, the application still requires diagnosis. Of primary importance is short circuit to GND information which is used to limit the number of short circuit events. (Refer to Chapter 8.2.7).

App. Note

PWM usage with current sense diagnosis can be limited by the inherent timing limitations of PROFET ${ }^{\text {TM }}+$. The aim is to give valid current sense information as fast as possible.
$t_{\mathrm{sIS}(\mathrm{ON})}$, the time required for the IN pin to transition from LOW to HIGH limits the minimum ON time necessary to get valid sense information. $t_{\text {sIS(FAULT) }}$ also limits the minimum ON time to get valid short circuit information. Table 15 sums up the minimum PWM duty cycle which can be used with a PROFET $^{\text {TM }}+$.

Table 15 PROFET ${ }^{\text {TM }}+$ PWM Timing Limitation

| Parameter | Symbol | Formula | $\boldsymbol{f}_{\mathrm{PWM}}=$ <br> $\mathbf{1 0 0 H z}$ | $\boldsymbol{f}_{\mathrm{PWM}}=$ <br> $\mathbf{2 0 0 H z}$ | $\boldsymbol{f}_{\mathrm{PWM}}=$ <br> $\mathbf{4 0 0 \mathrm { Hz }}$ | $\boldsymbol{f}_{\mathrm{PWM}}=$ <br> $\mathbf{1 k H z}$ | Unit |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| Period | $T_{\text {PWM }}$ | $1 / f_{\text {PWM }}$ | 10 | 5 | 2.5 | 1 | ms |
| min duty cycle at the output | $d_{\text {OUT_MIN }}$ | $t_{\text {OFF_delay }} / T_{\text {PWM }}$ | 0.8 | 1.6 | 3.2 | 8 | $\%$ |
| min duty cycle at the output for <br> diagnostic | $d_{\text {MIN }}$ | $t_{\text {SIS(FAULT) }} / \mathrm{T}$ | 2.5 | 5 | 10 | 25 | $\%$ |

When the current is established in the Power DMOS, the sense signal $I_{\text {IS }}$ takes far much lower time to establish.

## 10 The Micro Controller Interface

### 10.1 GND Pin

Although the GND pin is not directly interfaced to the micro controller, GND is of primary importance in controlling a PROFET ${ }^{\text {TM }}+$. Figure 78 shows the ideal GND protection circuitry. What ever the GND circuit chosen in the application, this circuit can be shared with other devices having the same battery feed and only with these ones.

- Region 1. For current in the magnitude of operating current ( 10 mA or below), the voltage drop should be kept to a minimum as a shift in the PROFET ${ }^{\text {TM }}+$ GND potential leads to a shift in the input threshold.
- Regions 2. To provide overvoltage protection for voltages above the breakdown voltage, the current through the Zener diode $Z_{\mathrm{D}(\mathrm{AZ)}}$ must be limited to a few tens of milliamps. This limit does not apply for ESD protection.
- Region 3. This ensures the necessary current limitation when reverse polarity is applied. The current in this mode should be as low as possible (below $I_{G N D}$ ) to reduce the loss generated in the diode $Z_{\mathrm{D}(\mathrm{AZ})}$.


Figure 78 Ideal GND Circuitry

### 10.1.1 GND Resistor

A compromise must be found in the GND resistor value which approximates the different regions of the above characteristic. For over voltage (refer to Chapter 8.8) and reverse polarity (refer to Chapter 8.9) protection, the value of the GND resistor should be as high as possible. The upper value is restricted by the ground shift potential ( $V_{\mathrm{GND}}=R_{\mathrm{GND}} \times I_{\mathrm{GND}}$ ) caused by the operating current flowing via the GND pin. In practice, a value of $150 \Omega$ per chip protected has proven satisfactory.
The main disadvantage of the GND resistor is high power dissipation in the event of an applied reverse polarity $\left(V_{\mathrm{S}(\mathrm{REV})}{ }^{2} / R_{\mathrm{GND}}\right)$. This leads to a relatively large resistor on the PCB. With $16 \mathrm{~V}, 1.7 \mathrm{~W} .1206$ package is necessary.
A capacitor can be used in parallel with the resistor which to limit the influence of $I_{\text {GND }}$ variation during switching of the channel. A capacitor placed between VS pin and GND will filter the charge pump perturbations.

### 10.1.2 GND Diode

To protect against reverse polarity events, a diode can be used. The reverse voltage is limited by the reverse breakdown voltage of the diode or the losses in the PROFET ${ }^{\text {TM }}+$ generated by the load current. A suggested diode is the BAS52-02V. The diode approximates only regions 1 and 3 of Figure 78 and does not protect against over voltage or loss of battery. Refer to Chapter 8.5. In this particular case, a $1 \mathrm{k} \Omega$ resistor can be used in parallel with the diode. PROFET ${ }^{\text {TM }}+$ are then limited in case of over voltage.

### 10.1.3 Different Ground for One System

At least two different Grounds are defined at a system level and usually three are necessary for optimum design. The chassis GND is the system OV reference. The module GND is the OV module reference. The module GND is sometimes split into digital GND (reference voltage for the digital sections such as the voltage regulator, micro controller, A/D converter, CAN transceivers etc.) and power GND (reference voltage for the power elements such as LSS, HSS, H bridges etc.). A fourth GND can also be defined which corresponds to the device GND. These different GNDs are shown in Figure 79. For simplification it doesn't describe the redundancy of GND wiring connection as shown in Figure 8. In a real system, the GND schematic can be even more complicated!


Figure 79 GND Definition

### 10.1.4 Loss of Ground

According to Figure 79, up to four GND can be lost. In case of module GND loss, the PROFET ${ }^{\text {TM }}+$ automatically turns OFF or remains OFF. In case of analog or device loss of GND, the micro controller can play the role of a parasitic GND via the logic inputs. To avoid this, a serial resistor (e.g $4.7 \mathrm{k} \Omega$ ) should be placed in between each micro controller and PROFET ${ }^{\text {TM }}+$ interfaces.

### 10.2 Digital Pins

All the digital pins of PROFET ${ }^{\text {TM }}+$ are identical. The digital pins are voltage driven. An internal current source is used to default the digital pins to logic level 0 . Where a pin is not required, it is recommended to leave it open. If this is not done, the ESD diode can be destroyed.
In binary digital circuits, there are two distinct voltage levels which represent the two binary states. In order to allow for the inevitable components tolerances, two voltage ranges are usually defined to represent these states. As shown in Figure 80, if the signal voltage lies in the range $V_{\operatorname{IN}(\mathrm{AMR}) \text { min }}$ to $V_{\mathrm{IN}(\mathrm{L})}$, it is interpreted (by the power device) as a logic 0 . If the signal voltage falls in the range of $V_{\operatorname{IN(H)}}$ to $V_{\operatorname{IN}(A M R) m a x}$, it is interpreted as a logic 1 . The two voltage bands are separated by a region in which the logic state is undefined. Voltages in this undefined region should be avoided.

input voltage.vsd
Figure 80 Two Distinct Voltage Ranges used to Represent two Values of Binary Variables

### 10.2.1 Absolute Maximum Rating

During two normal conditions, absolute maximum rating on input pins can be met.
Figure 81 describes the reason for the 6 V absolute maximum rating. During the OFF state of the module, where, the voltage regulator is OFF, a wake event is generated either by the communication (eg CAN, LIN, etc...), or by a digital input. In such a case, the voltage at the I/O of the micro controller is limited by the Zener diode at the $V_{\mathrm{DD}}$ line and the ESD structure internally the micro controller. The current is limited by the serial resistor.


Figure 81 Normal Application Condition to reach Absolute Maximum Rating

As shown in Figure 82, in order to activate the channel, it is necessary to pull the input pin up to $V_{\mathrm{BAT}}$, as it cannot be assumed that the voltage regulator is operating. Nevertheless, the voltage at the input should not exceed 6V permanently. To bypass the microcontroller, the easiest way is to use two diodes, such BAV 70S, in an OR combination. The battery voltage is divided by resistor $R_{\mathrm{LH} 1}$ and $R_{\mathrm{LH} 2}$. A ratio of $1 / 3$ will guarantee that even with 18 V battery voltage, the input pin will not see more than 6 V while a low battery voltage case such as 8 V will provide sufficient voltage at the input to guarantee the switching ON.


Figure 82 Limp Home Scenario

### 10.2.2 High level input voltage

With an input signal in this region, the digital circuitry will determine the input to be a high logic level and thus will turn the output ON or keep it ON. The application must ensure that the minimum voltage applied to the input pin is higher than $V_{\operatorname{IN}(H)}$ to guarantee an ON condition. The micro-controller specification usually provides the minimum output voltage for a logic 1 signal. As an umbrella specification, Infineon considers $V_{\mathrm{IN}(\mathrm{H})} \mathrm{MIN}=3.6 \mathrm{~V}$. Adding a resistor $R_{I / O}$ between the micro-controller and the power device is recommended. However, the voltage drop across this resistor must also be considered in the design. The equivalent circuit is described in Figure 83 where the $V_{\text {IOMIN }}$ value defined by Equation (17) must be guaranteed.

$$
\begin{equation*}
\mathrm{V}_{\mathrm{IO} \min }=\mathrm{V}_{\mathrm{IN}(\mathrm{H}) \min }+\mathrm{R}_{\mathrm{IO}} \times \mathrm{I}_{\mathrm{IN} \max }+\mathrm{Z}_{\mathrm{GND}} \times \mathrm{I}_{\mathrm{GND}} \tag{17}
\end{equation*}
$$

All parameters are given in the respective datasheets. Please note that the voltage drop caused by the resistor $R_{\text {I/O }}$ severely limits the number of devices which can be driven from one I/O pin of the microcontroller.


Figure 83 High level Equivalent Circuit

The purpose of the $I_{\mathbb{N}(H)}$ current source is to guarantee the device is OFF when the micro controller pin is floating, (e.g. during reset, un-powered, etc...).

### 10.2.3 Undefined region

The undefined region contains the switching thresholds for ON and OFF. The exact value $V_{T H}$ where this switching takes place is unknown and dependant on the device manufacturing process and temperature. To avoid crosstalk and parasitic switching, hysteresis is implemented. This ensures a certain immunity to noise.
This noise immunity can be defined, assuming that the exact turn ON and turn OFF thresholds are known. As an example, a rising or falling signal with parasitic noise will see several ON / OFF states before going to a stable state. Figure 84 gives an example of this situation. At turn ON, the parasitic noise is sufficiently intrusive to turn the device ON and OFF. At turn OFF, the parasitic noise is filtered by the hysteresis circuitry. The bigger the hysteresis, the higher the immunity to noise, but the difference between $V_{\operatorname{IN(H)} \text { MIN }}$ and $V_{\operatorname{IN}(L) / M A X}$ also increases, limiting the application's range. PROFET ${ }^{T M}$ + use a typical hysteresis voltage of 200 mV .


Figure 84 Benefit of the Hysteresis for Immunity to Noise
The hysteresis value is not tested during production, due to the test complexity.

### 10.2.4 Low level input voltage

With an input signal in this region, the digital circuitry will determine the input to be a low logic level and thus will turn the output OFF or keep it OFF. The application must ensure that the maximum voltage applied to the input pin is lower than the $V_{\operatorname{IN}(L) \max }$ voltage to guarantee an OFF condition. As umbrella specification, Infineon consider $V_{\text {IN(L)_MAX }}=1.1 \mathrm{~V}$. Refer to Figure 85 for details.
The equivalent circuit is described in Figure 85 where the $V_{\text {IOmin }}$ value defined by Equation (18) must be guaranteed.

$$
\begin{equation*}
\mathrm{V}_{\mathrm{IOMAX}}=\mathrm{V}_{\mathrm{IN}(\mathrm{~L}) \mathrm{MAX}}+\mathrm{R}_{\mathrm{IO}} \times \mathrm{I}_{\mathrm{IN} \max }+\mathrm{Z}_{\mathrm{GND}} \times \mathrm{I}_{\mathrm{GND}} \tag{18}
\end{equation*}
$$



Figure 85 Low level Equivalent Circuit

### 10.3 Sense Pin

As described in Chapter 9.1, the current sense function is driven by a current generator. The sense pin is a combination of two current generators, one for nominal conditions and one for fault conditions. Micro-controllers measure voltage, not current hence a sense resistor is required. To find the value of the sense resistor $R_{\text {IS }}$, it is important to know the maximum load current amplitude the system is required to diagnose.

### 10.3.1 Maximum Load Current

To define the maximum current $I_{\mathrm{L}(\mathrm{NOM}) \text { _MAX }}$ which can flow in the power DMOS, a solution is to define the minimum PWM duty cycle at the maximum battery voltage. For example, assuming a duty cycle of $8 \%$ as a minimum functionality (as an example for lamp dimming) and a maximum 18 V battery voltage, it is equivalent to start the PWM at a battery voltage of 5 V . Determining the lamp resistance at 5 V , out of Equation (1), it is possible then to determine the maximum current which flows at 18 V battery voltage. Refer to Figure 86 with a 27 W bulb example. Out of the graph, it is seen the maximum current which can flow in a 27 W during a PWM of $8 \%$ at 18 V is roughly 5 A . A system using BTS5045-2EKA to drive 27 W bulb should be able to diagnose 5 A current. With $I_{\mathrm{L}(\mathrm{NOM}) \_\max }$ known, the minimum current ratio, $k_{\text {ILIS_MIN }}$ at this point can be determined. With this value, the maximum sense current the PROFET ${ }^{\text {TM }}+$ can provide is $I_{\text {IS_MAX }}$ is known. All current above this value will be considered as a short circuit. Taking into account the micro controller supply $V_{\mathrm{DD}}$, the maximum sense resistor is $R_{\mathrm{IS}}=V_{\mathrm{DD}} / I_{\mathrm{IS}}$ MAX . Refer to Figure 87 and Table 16.

Note that the PROFET ${ }^{\text {TM }}+$ current sense range is limited by the maximum current the $P$ channel MOSFET can provide. Refer to Figure 66. Table 17 summurizes the maximum load currents $\mathrm{PROFET}^{\mathrm{TM}}+$ devices can diagnose.

Table 16 Optimized $R_{\text {IS }}$ calculation example

|  | $20 \mathrm{~m} \Omega$ | $30 \mathrm{~m} \Omega$ | $45 \mathrm{~m} \Omega$ | $90 \mathrm{~m} \Omega$ | $120 \mathrm{~m} \Omega$ | $180 \mathrm{~m} \Omega$ |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| Load planned <br> (W) | $2 \times 27+5$ | $2 \times 21$ | $27+5$ | 21 | $2 \times 5$ | $1 \times 5$ |
| Load current <br> max (A) | 11 | 8 | 8.6 | 4.0 | 1.9 | 0.8 |
| $k_{\text {ILIS }}$ mini | 2610 | 1870 | 1305 | 1305 | 480 | 480 |
| $R_{\text {IS }}(\mathrm{k} \Omega)$ | 1.2 | 1.2 | 0.8 | 1.6 | 1.2 | 2.9 |

App. Note


Figure 86 Maximum Current with 8\% PWM Function of the Battery Voltage. 27W Lamp


Figure 87 Sense Current Function of the Load Current with BTS5020-2EKA

Table 17 PROFET ${ }^{\text {TM }}$ +s Maximum Diagnosable Current

|  | $20 \mathrm{~m} \Omega$ | $30 \mathrm{~m} \Omega$ | $45 \mathrm{~m} \Omega$ | $90 \mathrm{~m} \Omega$ | $120 \mathrm{~m} \Omega$ | $180 \mathrm{~m} \Omega$ |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| Target Load | $2 \times 27 \mathrm{~W}$ <br> +5 W | $2 \times 27 \mathrm{~W}$ | 27 W | 21 W | $2 \times 5 \mathrm{~W}$ | 5 W |
| Maximum current <br> with $8 \%$ PWM | 11 A | 8.6 A | 5 A | 4.3 A | 1.8 A | 0.9 A |
| $k_{\text {LIS }}$ ratio typical | 3000 | 2150 | 1500 | 1500 | 550 | 550 |
| Diagnosable load <br> current $I_{\text {LMAX }}$ | 15 A | 11 A | 8 A | 8 A | 2.8 A | 2.8 A |

### 10.3.2 Minimum Load Current

The minimum load current the PROFET ${ }^{\text {TM }}+$ devices will experience is the open load. As described in Chapter 6.3 and Chapter 9.6.3, in that case, the minimum current $I_{\mathrm{IS}(\mathrm{OL})}$ shall be too small to be detectable by the $R_{\text {IS }}$ defined in Chapter 10.3.1. In such a case, the usage of an additional sense resistor $R_{\text {IS_Lowload }}$ and a switch has to be considered. Figure 88 sketches the circuitry to be employed. A suggested value for $R_{\text {IS_Lowload }}$ is $10 \mathrm{k} \Omega$.


Figure 88 Low Load Current Detection Circuitry

### 10.3.3 Sense Pin Voltage

The sense pin has no particular clamping structure, except the ESD structure, referenced to $V_{\mathrm{S}}$. It means if no external limitation is applied, $V_{\text {IS }}$ can go up to $V_{S}$. Refer to Figure 89. To protect the micro controller, a serial resistor is necessary, as a minimum. In that case, the micro controller protection diode will limit the voltage while the serial resistor will limit the current.


Figure 89 Current Sense Circuitry and Minimum Protection Circuitry
It is also possible to use a Zener diode to clamp against over voltage. This improves the over voltage robustness of the system. Refer to Figure 90. The $I_{\mathrm{A} / \mathrm{D}}$ is dramatically reduced and most of the voltage is clamped by the Zener diode. $R_{\text {SENSE }}$ is necessary to protect the sense structure from destructive power dissipation under normal conditions and from reverse polarity.


Figure 90 Current Sense Circuitry with Improved Protection Circuitry
It is important to notice the power in the sense circuitry $\left(I_{I_{-} \text {LIN }} ; I_{I_{\text {S_FAULT }}}\right)$ is not negligible, thus the $V_{\text {IS }}$ should not be limited, either by too low sense resistor, either by Zenering.

App. Note

PROFET ${ }^{\text {TM }}+$ Scalability

## 11 PROFET ${ }^{\text {TM }}$ + Scalability

PROFET ${ }^{\text {TM }}+$ belongs to a family. Every electrical parameter is scaled around the $R_{\mathrm{DS}(\mathrm{ON})}$ value. The $R_{\mathrm{DS}(\mathrm{ON})}$ value scales mainly $k_{\mathrm{ILIS}}$ ratio, $E_{\mathrm{AS}}$ capability and $I_{\mathrm{L}(\mathrm{SC})}$ current limitation. All other parameters are identical!

### 11.1 High Ohmic Family

Table 18 summarizes the difference between the high ohmic PROFET ${ }^{\text {TM }}+$.

Table 18 Difference in High Ohmic Family

| Number | Parameter | Symbol | $\begin{aligned} & \text { BTS } \\ & 5020 \end{aligned}$ | $\begin{aligned} & \text { BTS } \\ & 5030 \end{aligned}$ | $\begin{aligned} & \text { BTS } \\ & 5045 \end{aligned}$ | $\begin{aligned} & \text { BTS } \\ & 5090 \end{aligned}$ | $\begin{aligned} & \text { BTS } \\ & 5120 \end{aligned}$ | $\begin{aligned} & \text { BTS } \\ & 5180 \end{aligned}$ | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Overview | Load | $P_{\text {LOAD }}$ | 2*27+5 | $\begin{aligned} & 2 * 27 \\ & 1 * 27+5 \end{aligned}$ | 1*27 | $\begin{aligned} & 1 * 21 \\ & 2 * 10 \end{aligned}$ | $\begin{aligned} & 1 * 10 \\ & 2 * 5 \end{aligned}$ | 1*5 | W |
| Overview | Typical kilis ratio | $k_{\text {ILIS }}$ | 3000 | 2150 | 1500 | 1500 | 550 | 550 | - |
| P_4.1.22 | Maximum power | $P_{\text {TOT }}$ | 1.9 | 1.9 | 1.6 | 1.6 | 1.4 | 1.4 | W |
| P_4.1.23 | Inductive energy | $E_{\text {AS }}$ | 80 | 60 | 40 | 30 | 15 | 10 | mJ |
| P_4.3.2 | Junction to ambient | $R_{\text {thJA }}$ | 33 | 33 | 35 | 35 | 40 | 40 | K/W |
| $\begin{aligned} & \hline \text { P_5.5.1 } \\ & \text { P_5.5.21 } \end{aligned}$ | On state resistance | $R_{\text {DS(ON) }}$ | $\begin{aligned} & 44 \\ & 20 \end{aligned}$ | $\begin{aligned} & 60 \\ & 30 \end{aligned}$ | $\begin{aligned} & 90 \\ & 45 \end{aligned}$ | $\begin{aligned} & 180 \\ & 90 \end{aligned}$ | $\begin{aligned} & 240 \\ & 120 \end{aligned}$ | $\begin{aligned} & 360 \\ & 180 \end{aligned}$ | $\mathrm{m} \Omega$ |
| $\begin{aligned} & \text { P_5.5.2 } \\ & \text { P_5.5.3 } \end{aligned}$ | Nominal load current | $\begin{array}{\|l\|l} I_{\text {nom1 }} \\ I_{\text {nom2 }}{ }^{1)} \\ \hline \end{array}$ | $\begin{aligned} & 7 \\ & 5 \end{aligned}$ | $\begin{aligned} & 6 \\ & 4 \end{aligned}$ | $\begin{aligned} & 5 \\ & 3 \end{aligned}$ | $\begin{aligned} & 3.5 \\ & 2.5 \end{aligned}$ | $\begin{aligned} & 3 \\ & 2 \end{aligned}$ | $\begin{aligned} & 2 \\ & 1.4 \end{aligned}$ | A |
| P_5.5.9 | Inverse current capability | $-I_{\mathrm{L}(\mathrm{INV})}{ }^{1)}$ | 5 | 4 | 3 | 2.5 | 2 | 1.4 | A |
| P_5.5.19 | Switch ON energy | $E_{\mathrm{ON}}$ | 1 | 1 | 0.675 | 0.675 | 0.34 | 0.12 | mJ |
| P_5.5.20 | Switch OFF energy | $E_{\text {OFF }}$ | 1 | 1 | 0.675 | 0.675 | 0.3375 | 0.12 | mJ |
| P_6.6.4 | Load current limitation | $I_{\text {L5(SC) }}$ | $\begin{aligned} & 50 \\ & 65 \\ & 80 \end{aligned}$ | $\begin{aligned} & 36 \\ & 47 \\ & 57 \end{aligned}$ | $\begin{aligned} & 25 \\ & 32 \\ & 40 \end{aligned}$ | $\begin{aligned} & 20 \\ & 30 \\ & 40 \end{aligned}$ | $\begin{array}{\|l\|} \hline 9 \\ 12 \\ 15 \end{array}$ | $\begin{array}{\|l\|} \hline 8 \\ 11 \\ 15 \end{array}$ | A |
| P_6.6.7 | Load current limitation | $I_{\text {L28(SC) }}$ | $\begin{aligned} & 25 \\ & 32 \\ & 40 \end{aligned}$ | $\begin{aligned} & 18 \\ & 23 \\ & 29 \end{aligned}$ | $\begin{aligned} & 12 \\ & 16 \\ & 20 \end{aligned}$ | $\begin{aligned} & 10 \\ & 15 \\ & 20 \end{aligned}$ | $\begin{array}{\|l} 4 \\ 6 \\ 8 \end{array}$ | $\begin{aligned} & 2 \\ & 4 \\ & 8 \end{aligned}$ | A |
| P_6.6.12 | Short circuit average current after several minutes of thermal toggling | $I_{\text {L(RMS) }}$ | 8 | 7 | 6 | 6 | 3.5 | 3 | A |
| P_7.5.2 | Open load threshold in ON state | $I_{\text {IS(OL) }}$ | 4 | 5.6 | 8 | 8 | 21 | 21 | $\mu \mathrm{A}$ |
| P_7.5.9 | $I_{\mathrm{L}}$ for $k_{\text {ILIS } 1}$ | $I_{L 1}$ | 0.5 | 0.5 | 0.5 | 0.5 | 0.25 | 0.25 | A |
| P_7.5.10 | $I_{\mathrm{L}}$ for $k_{\text {ILIS2 }}$ | $I_{L 2}$ | 2 | 2 | 1 | 1 | 0.5 | 0.5 | A |
| P_7.5.11 | $I_{\mathrm{L}}$ for $k_{\text {ILIS }}$ | $I_{L 3}$ | 4 | 4 | 2 | 2 | 1 | 1 | A |
| P_7.5.12 | $I_{\mathrm{L}}$ for $k_{\text {ILIS }}$ | $I_{L 4}$ | 7 | 7 | 4 | 4 | 2 | 2 | A |

[^1]App. Note

Appendix

## 12 Appendix

### 12.1 PWM Power Losses Calculations

$$
\begin{equation*}
\mathrm{P}_{\mathrm{PWM}}=\mathrm{P}_{\mathrm{RON}}+\mathrm{P}_{\mathrm{SW}} \tag{19}
\end{equation*}
$$

Power losses are splitted in losses during $R_{\mathrm{DS}(\mathrm{ON})}$ phases $P_{\mathrm{RON}}$ and switching phases $P_{\mathrm{SW}}$.

$$
\mathrm{P}_{\mathrm{RON}}=\mathrm{R}_{\mathrm{DSON}} \times \mathrm{I}_{\mathrm{PWM}}^{2} \times \mathrm{t}_{\mathrm{ON}} \times \mathrm{F}
$$

Power losses in the $R_{\mathrm{DS}(\mathrm{ON})}$ phases depends on the PWM frequency F , the time $\mathrm{ON} t_{\mathrm{ON}}$, the $R_{\mathrm{DS}(\mathrm{ON})}$ and the load current $I_{\text {PWM }}$.

$$
\begin{equation*}
\mathrm{d}=\mathrm{F} \times \mathrm{t}_{\mathrm{ON}}=\frac{\mathrm{V}_{\mathrm{PWM}}{ }^{2}}{\mathrm{~V}_{\mathrm{BAT}}{ }^{2}} \tag{21}
\end{equation*}
$$

The duty cycle is dependant on the $V_{\text {PWM }}$ voltage where PWM starts (usually 13.2 V ) and the effective battery voltage $V_{\mathrm{BAT}}$.

$$
\begin{equation*}
\mathrm{P}_{\mathrm{RON}}=\mathrm{R}_{\mathrm{DSON}} \times \mathrm{F} \times \mathrm{V}_{\mathrm{PWM}}^{2} \times \frac{\mathrm{I}_{\mathrm{PWM}}^{2}}{\mathrm{~V}_{\mathrm{BAT}}^{2}}=\mathrm{K}_{1} \times \frac{\mathrm{I}_{\mathrm{PWM}}^{2}}{\mathrm{~V}_{\mathrm{BAT}}^{2}} \tag{22}
\end{equation*}
$$

Replacing Equation (21) in Equation (20), and defining a constant value $K_{1}$ to simplify the term.

$$
\begin{equation*}
I_{\text {PWM }}=\frac{V_{\text {BAT }}}{R_{\text {LAMP }}} \tag{23}
\end{equation*}
$$

The load current $I_{\mathrm{PWM}}$ is depending on battery voltage $V_{\mathrm{BAT}}$ and $R_{\mathrm{LAMP}}$, resistor of the lamp, constant due to PWM.

$$
\begin{equation*}
P_{\mathrm{RON}}=\frac{\mathrm{K}_{1} \times \mathrm{V}_{\mathrm{BAT}}^{2}}{\mathrm{~V}_{\mathrm{BAT}}^{2} \times \mathrm{R}_{\mathrm{LAMP}}^{2}}=\frac{\mathrm{K}_{1}}{\mathrm{R}_{\mathrm{LAMP}}^{2}}=\mathrm{K}_{2} \tag{24}
\end{equation*}
$$

Replacing Equation (23) in Equation (22), and defining a constant value $K_{2}$ to simplify the term, power losses in the $R_{\text {DSON }}$ phase is constant!

$$
\mathrm{P}_{\mathrm{SW}}=2 \times \mathrm{P}_{\mathrm{SWON}}=2 \times \mathrm{t}_{\mathrm{SWON}} \times \frac{1}{2} \times \frac{\mathrm{V}_{\mathrm{BAT}}}{2} \times \frac{\mathrm{I}_{\mathrm{PWM}}}{2}
$$

Switching losses $P_{\mathrm{Sw}}$ are twice the $P_{\mathrm{swoN}}$ (assuming switch ON and OFF is symetric).

$$
\begin{equation*}
\mathrm{P}_{\mathrm{SW}}=\mathrm{t}_{\mathrm{SWON}} \times \frac{1}{4} \times \frac{\mathrm{V}_{\mathrm{BAT}}^{2}}{\mathrm{R}_{\mathrm{LAMP}}} \tag{26}
\end{equation*}
$$

Replacing Equation (23) in Equation (26)

$$
\begin{equation*}
\mathrm{P}_{\mathrm{SW}}=\mathrm{K}_{3} \times \mathrm{V}_{\mathrm{BAT}}^{2} \tag{27}
\end{equation*}
$$

$P_{\text {sw }}$ is depeding on the $V_{\mathrm{BAT}^{2}}{ }^{2}$.

$$
\mathrm{P}_{\mathrm{PWM}}=\mathrm{K}_{2}+\mathrm{K}_{3} \times \mathrm{V}_{\mathrm{BAT}}^{2}
$$

Replacing Equation (24) and Equation (27) in Equation (19)

### 12.2 Open Load Resistor Calculation

The maximum acceptable value for $R_{\mathrm{OL}}$, (open load pull up resistor) is searched for.

$$
\mathrm{V}_{\mathrm{BAT}}-3 \mathrm{~V}<\frac{\mathrm{R}_{\mathrm{DIRT}}}{\mathrm{R}_{\mathrm{DIRT}}+\mathrm{R}_{\mathrm{OL}}} \times \mathrm{V}_{\mathrm{BAT}}
$$

The voltage at the output $V_{\text {OUT }}$ should be higher than the highest voltage possible understood as a present load. This voltage is given by the voltage divider formed by $R_{\mathrm{DIRT}}$ and $R_{\mathrm{OL}}$.

$$
\mathrm{V}_{\mathrm{BAT}} \times\left(\mathrm{R}_{\mathrm{DIRT}}+\mathrm{R}_{\mathrm{OL}}\right)-3 \mathrm{~V} \times\left(\mathrm{R}_{\mathrm{DIRT}}+\mathrm{R}_{\mathrm{OL}}\right)<\mathrm{R}_{\mathrm{DIRT}} \times \mathrm{V}_{\mathrm{BAT}}
$$

Enlarging the equation,

$$
\left(\mathrm{V}_{\mathrm{BAT}-3 \mathrm{~V}) \times \mathrm{R}_{\mathrm{OL}}<3 \mathrm{~V} \times \mathrm{R}_{\mathrm{DIRT}}}\right.
$$

Symplifying and bringing $R_{\mathrm{OL}}$ on the right hand side.

App. Note

## 13 Revision History

Table 21 Revision History

| Version | Date | Chapter | Change |
| :--- | :--- | :--- | :--- |
| 1.0 | 2010.12 .15 | All | First release |
|  |  |  |  |

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[^0]:    1) Typical $R_{\mathrm{DS}(\mathrm{ON})}$, worst case GBR
[^1]:    1) For dual channel only
