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THIS SPEC IS OBSOLETE

Spec No: 002-08493

Spec Title: S6AE101A ENERGY HARVESTING PMIC FOR WIRELESS SENSOR NODE

Replaced by: NONE

S6AE101A

Energy Harvesting PMIC for Wireless Sensor Node

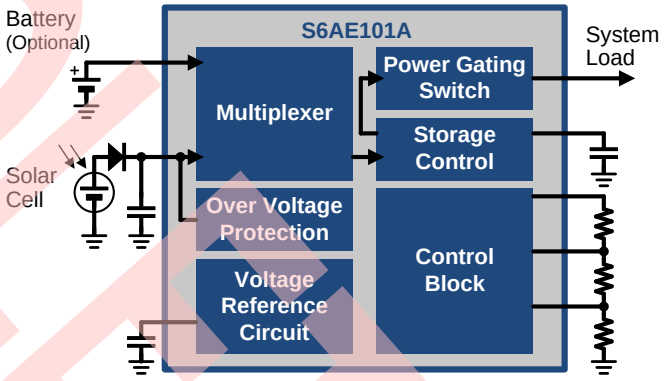
The S6AE101A is a power management IC (PMIC) for energy harvesting that is built into circuits of solar cells connected in series, output power control circuits, output capacitor storage circuits, and power switching circuits of primary batteries. Super-low-power operation is possible using a consumption current of only 250 nA and startup power of only 1.2 µW. As a result, even slight amounts of power generation can be obtained from compact solar cells under low-brightness environments of approximately 100 lx. The S6AE101A stores power generated by solar cells to an output capacitor using built-in switch control, and it turns on the power switching circuit while the capacitor voltage is within a preset maximum and minimum range for supplying energy to a load. If the power generated from solar cells is not enough, energy can also be supplied in the same way as solar cells from connected primary batteries for auxiliary power. Also, an over voltage protection (OVP) function is built into the input pins of the solar cells, and the open voltage of solar cells is used by this IC to prevent an overvoltage state. The S6AE101A is provided as a battery-free wireless sensor node solution that is operable by super-compact solar cells.

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Features

- Input power selection control: Solar cell or primary battery
- Operated by solar cells without the need for primary batteries
- Storage of energy from power supply to storage capacitors
- Output power gating control, output voltage regulation
- Operation input voltage range
  - Solar cell power : 2.0V to 5.5V
  - Primary battery power : 2.0V to 5.5V
- Adjustable output voltage range : 1.1V to 5.2V
- Low-consumption current : 250 nA
- Minimum input power at startup : 1.2 µW
- Input overv oltage protection : 5.4V
- Compact SON-10 package : 3 mm × 3 mm

Block Diagram



Applications

- Energy harvesting power system with a very small solar cell
- Bluetooth® Smart sensor
- Wireless HVAC sensor
- Wireless lighting control
- Security system
- Smart home / Building / Industrial wireless sensor

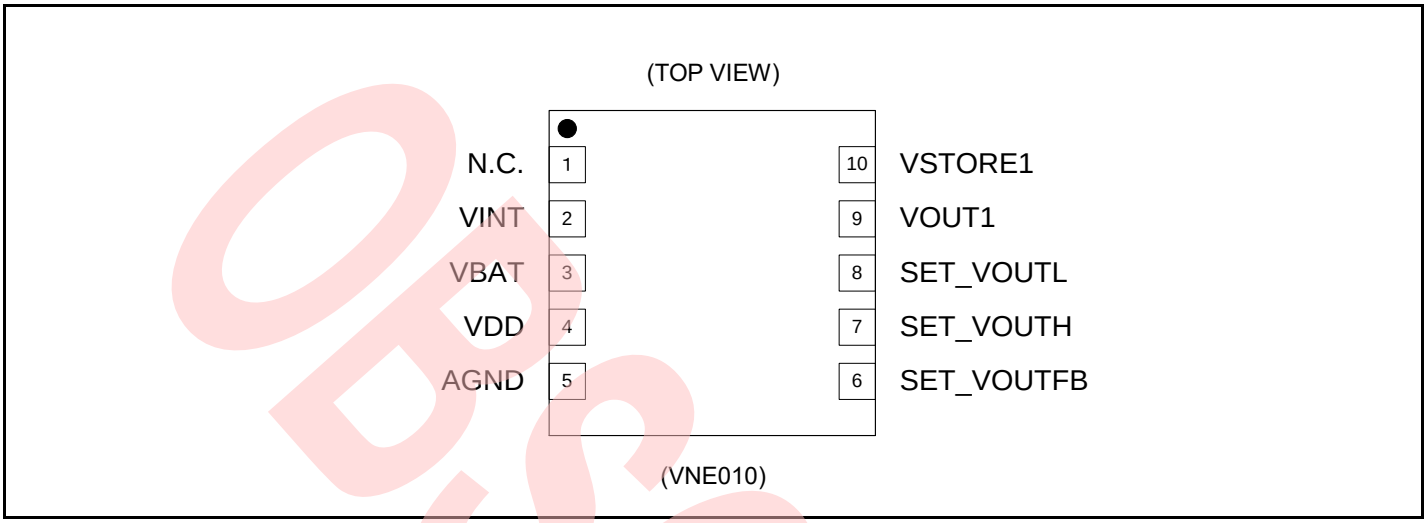
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1. Pin Assignment

Figure 1-1 Pin Assignment

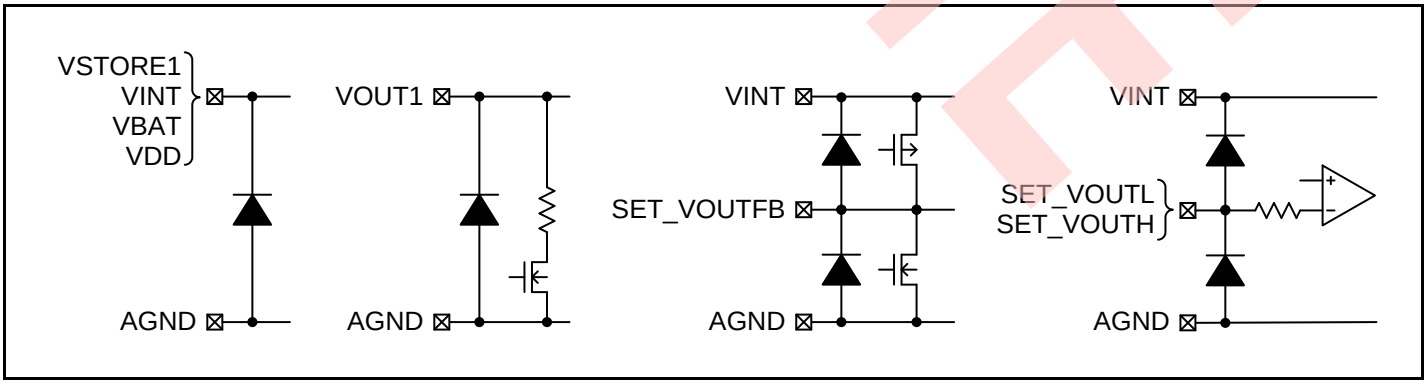


2. Pin Descriptions

Table 2-1 Pin Descriptions

Pin No.	Pin Name	I/O	Description
1	N.C	–	Non connection pin (Leave this pin open)
2	VINT	O	Internal circuit storage output pin
3	VBAT	I	Primary battery input pin (when being not used, leave this pin open)
4	VDD	I	Solar cell input pin (when being not used, leave this pin open)
5	AGND	–	Ground pin.
6	SET_VOUTFB	O	Reference voltage output pin (for connecting resistor)
7	SET_VOUTH	I	VOUT1 output voltage setting pin (for connecting resistor)
8	SET_VOUTL	I	VOUT1 output voltage setting pin (for connecting resistor)
9	VOUT1	O	Output voltage pin
10	VSTORE1	O	Storage output pin

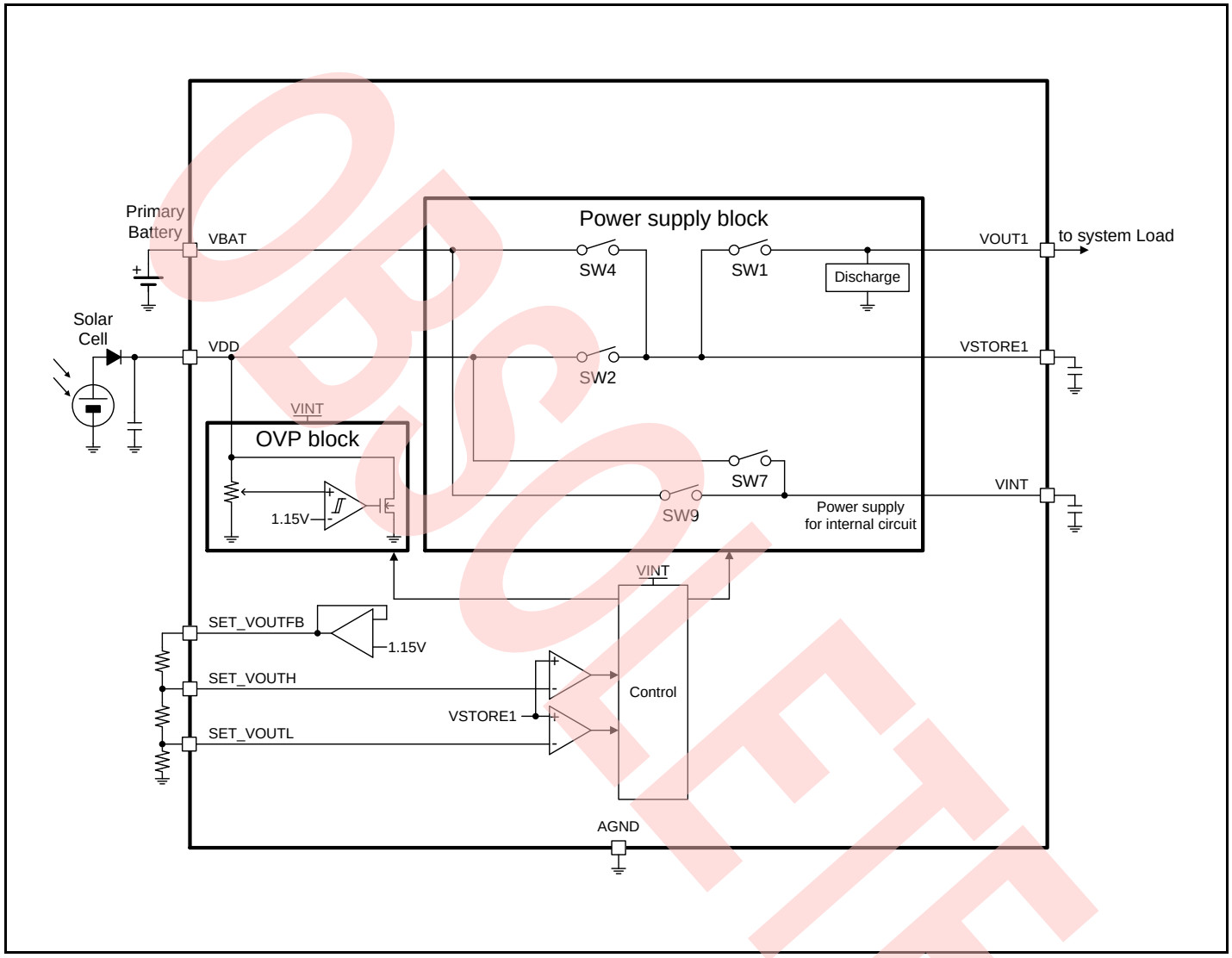
Figure 2-1 I/O Pin Equivalent Circuit Diagram



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3. Architecture Block Diagram

Figure 3-1 Architecture Block Diagram



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4. Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage (*1)	V_{MAX}	VDD, VBAT pin	−0.3	+6.9	V
Signal input voltage(*1)	$V_{INPUTMAX}$	SET_VOUTH, SET_VOUTL pin	−0.3	V_{VDD}	V
VDD slew rate	V_{SLOPE}	VDD pin	−	0.1	mV/µs
Power dissipation (*1)	P_D	Ta ≤+ 25°C	−	1200 (*2)	mW
Storage temperature	T_{STG}	−	−55	+125	°C

*1: When GND=0V

*2: θja (wind speed 0m/s): +58°C/W

Warning:

1. *Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.Do not exceed any of these ratings.*

5. Recommended Operating Conditions

Parameter	Symbol	Condition		Value			Unit
				Min	Typ	Max	
Power supply voltage 1 (*1)	V_{VDD}	VDD pin		2.0	3.3	5.5	V
Power supply voltage 2 (*1)	V_{VBAT}	VBAT pin		2.0	3.0	5.5	V
Signal input voltage (*1)	V_{INPUT}	SET_VOUTH, SET_VOUTL pin		−	−	VINT pin voltage	V
VOUT1 setting resistance	R_{VOUT}	Sum of R1, R2, R3		10	−	50	MΩ
VDD capacitance	C1	VDD pin		10	−	−	µF
VINT capacitance	C2	VINT pin		1	−	−	µF
VSTORE1 capacitance	C3	VSTORE1 pin		100	−	−	µF
VOUT maximum setting voltage	V_{SYSH}	VSTORE1 pin		1.3	−	5.2	V
VOUT minimum setting voltage	V_{SYSL}	VSTORE1 pin	V_{SYSH} ≥ 1.7V	1.1	−	V_{SYSH} × 0.90	V
			V_{SYSH} < 1.7V	1.1	−	V_{SYSH} × 0.85	V
Operating ambient temperature	Ta	−		−40	−	+85	°C

*1: When GND = 0V

Warning:

1. *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.*
2. *Any use of semiconductor devices will be under their recommended operating condition.*
3. *Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.*
4. *No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.*

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6. Electrical Characteristics

The electrical characteristics excluding the effect of external resistors and external capacitors are shown in below.

Table 6-1 Electrical Characteristics (System Overall)

(Unless specified otherwise, these are the electrical characteristics under the recommended operating environment.)

Parameter	Symbol	Condition		Value			Unit
				Min	Typ	Max	
Minimum Input power in start-up	W_{START}	VDD pin, Ta = +25°C, V_{VOUTH} setting =3V, By applying 0.4 µA to VDD, when VOUT1 reaches 3V × 95% after the point when VDD reaches 3V.		–	–	1.2	µW
Consumption current 1	I_{QIN1}	VDD pin input current, VDD=3V, Open VBAT pin, SW2 = OFF, Ta = +25°C, SET_VOUTFB resistance = 50 MΩ, VOUT1 Load = 0 mA		–	250	390	nA
Power detection voltage	V_{DETH}	VDD, VBAT ,VINT pin		1.0	1.4	2.0	V
Power undetection voltage	V_{DETL}	VDD, VBAT ,VINT pin		0.9	1.3	1.9	V
Power detection hysteresis	V_{DETHYS}	VDD, VBAT ,VINT pin		–	0.1	–	V
VOUT maximum voltage	V_{VOUTH}	VSTORE1 pin, VOUT1 Load=0 mA	V_{SYSH} ≥ 2V	V_{SYSH}×0.950	V_{SYSH}	V_{SYSH}×1.050	V
			V_{SYSH} < 2V	V_{SYSH}×0.935	V_{SYSH}	V_{SYSH}×1.065	V
Input power reconnect voltage	V_{VOUTM}	VSTORE1 pin, VOUT1 Load=0 mA	V_{SYSH} ≥ 2V	V_{VOUTH} ×0.90250	V_{VOUTH} × 0.95	V_{VOUTH} × 0.99750	V
			V_{SYSH} < 2V	V_{VOUTH} ×0.88825	V_{VOUTH} × 0.95	V_{VOUTH} ×1.01175	V
VOUT minimum voltage	V_{VOUTL}	VSTORE1 pin, VOUT1 Load=0 mA	V_{SYSL} ≥ 2V	V_{SYSL}×0.950	V_{SYSL}	V_{SYSL}×1.050	V
			V_{SYSL} < 2V	V_{SYSL}×0.935	V_{SYSL}	V_{SYSL}×1.065	V
OVP detection voltage	V_{OVPH}	VDD pin		5.2	5.4	5.5	V
OVP release voltage	V_{OVPL}	VDD pin		5.1	5.3	5.4	V
OVP detection hysteresis	V_{OVPHYS}	VDD pin		–	0.1	–	V
OVP protection current	I_{OVP}	VDD pin input current		6	–	–	mA

Table 6-2 Electrical Characteristics (Switch)

VDD ≥ 3V, VBAT ≥ 3V, VINT ≥ 3V, V_{VOUTL} ≥ 3V, VSTORE1 ≥ V_{VOUTL}

(Unless specified otherwise, these are the electrical characteristics under the recommended operating environment.)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
On resistance 1	R_{ON1}	SW1, In connection of VSTORE1 pin and VOUT1 pin	–	1.5	2.5	Ω
On resistance 2	R_{ON2}	SW2, In connection of VDD pin and VSTORE1 pin	–	5	10	kΩ
On resistance 4	R_{ON4}	SW4, In connection of VDD pin and VSTORE1 pin	–	5	10	kΩ
Discharge resistance	R_{DIS}	VOUT1 pin	–	1	2	kΩ

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7. Functional Description

7.1 Power Supply Control

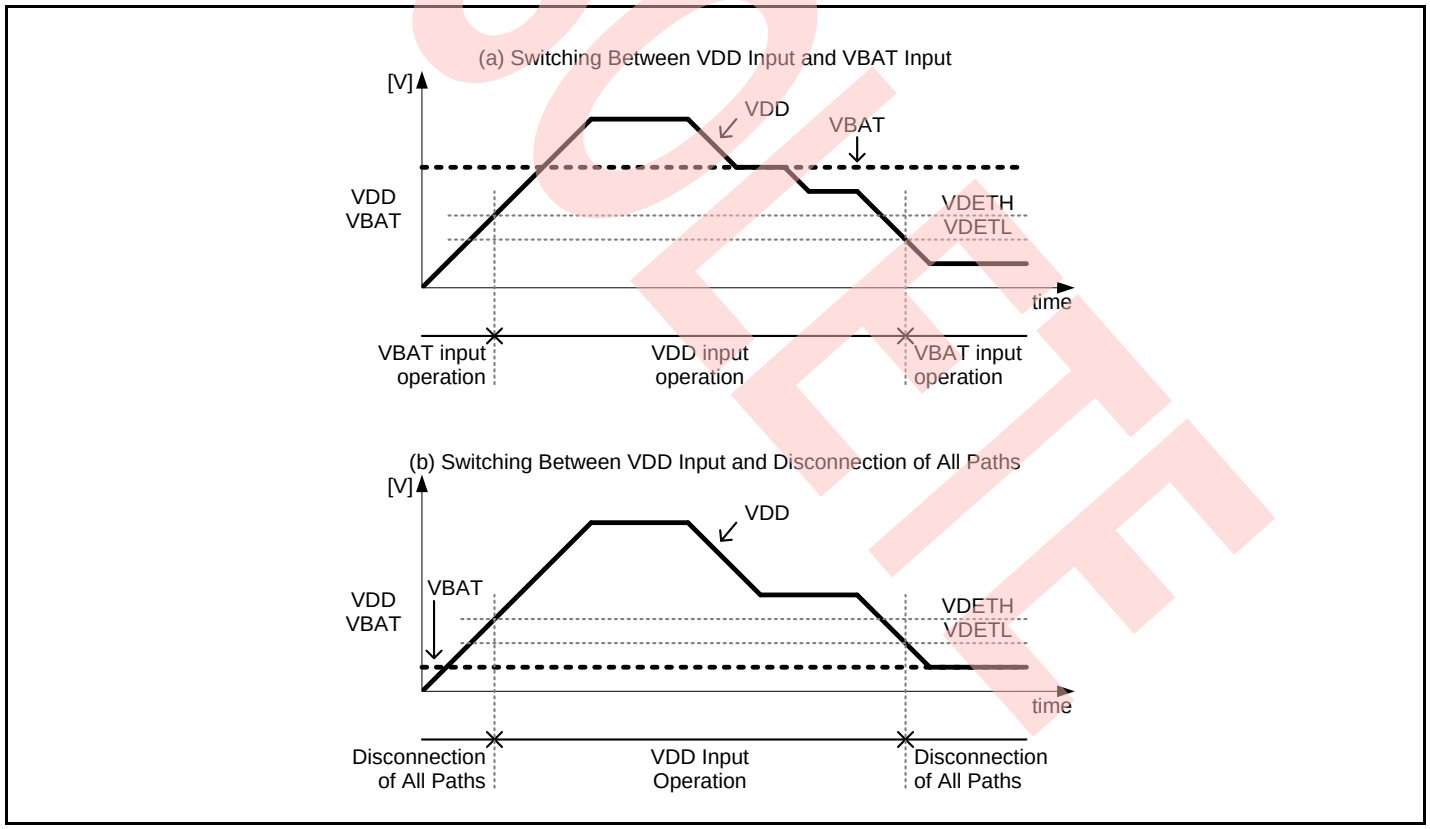
This IC can operate by two input power supplies, namely, the solar cell voltage VDD and the primary battery voltage VBAT. The voltages at the VDD pin and VBAT pin are monitored, and selection control of the input power supply is performed based on this voltage state (Figure 7-1).

The input power (solar cell or primary battery) is temporarily stored to a capacitor connected to the VSTORE1 pin. When the voltage of the VSTORE1 pin reaches a certain threshold value or higher, the power switching switch (SW1) connects VSTORE1 and VOUT1.

Table 7-1 Input Power Supply Selection Control

VDD Voltage (Solar Cell)	VBAT Voltage (Primary Battery)	Operation
V_{DETH} (1.55V) or higher	V_{DETH} (1.55V) or higher	VDD input power supply is performed
	V_{DETL} (1.45V) or less	VDD input power supply is performed
V_{DETL} (1.45V) or less	V_{DETH} (1.55V) or higher	VBAT input power supply is performed
	V_{DETL} (1.45V) or less	All paths are disconnected

Figure 7-1 Input Power Selection Control



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1. VDD input voltage operation

This section describes operation when the VDD pin is set as the input power (Figure 7-2).

[1] When the voltage of the VDD pin reaches the power detection voltage (V_{DETH} = 1.55V) or higher, the switch (SW2) connects VDD and VSTORE1 (path S1). Also, when the voltage of the VDD pin falls to the power undetection voltage (V_{DETL} = 1.45V) or less, SW2 disconnects the path S1.

[2] When the voltage of the VSTORE1 pin reaches the threshold value (V_{VOUTH}) or higher that was set by the SET_VOUTH pin, SW2 disconnects the path S1. Also, the VOUT switch (SW1) connects VSTORE1 and VOUT1 (path S2).

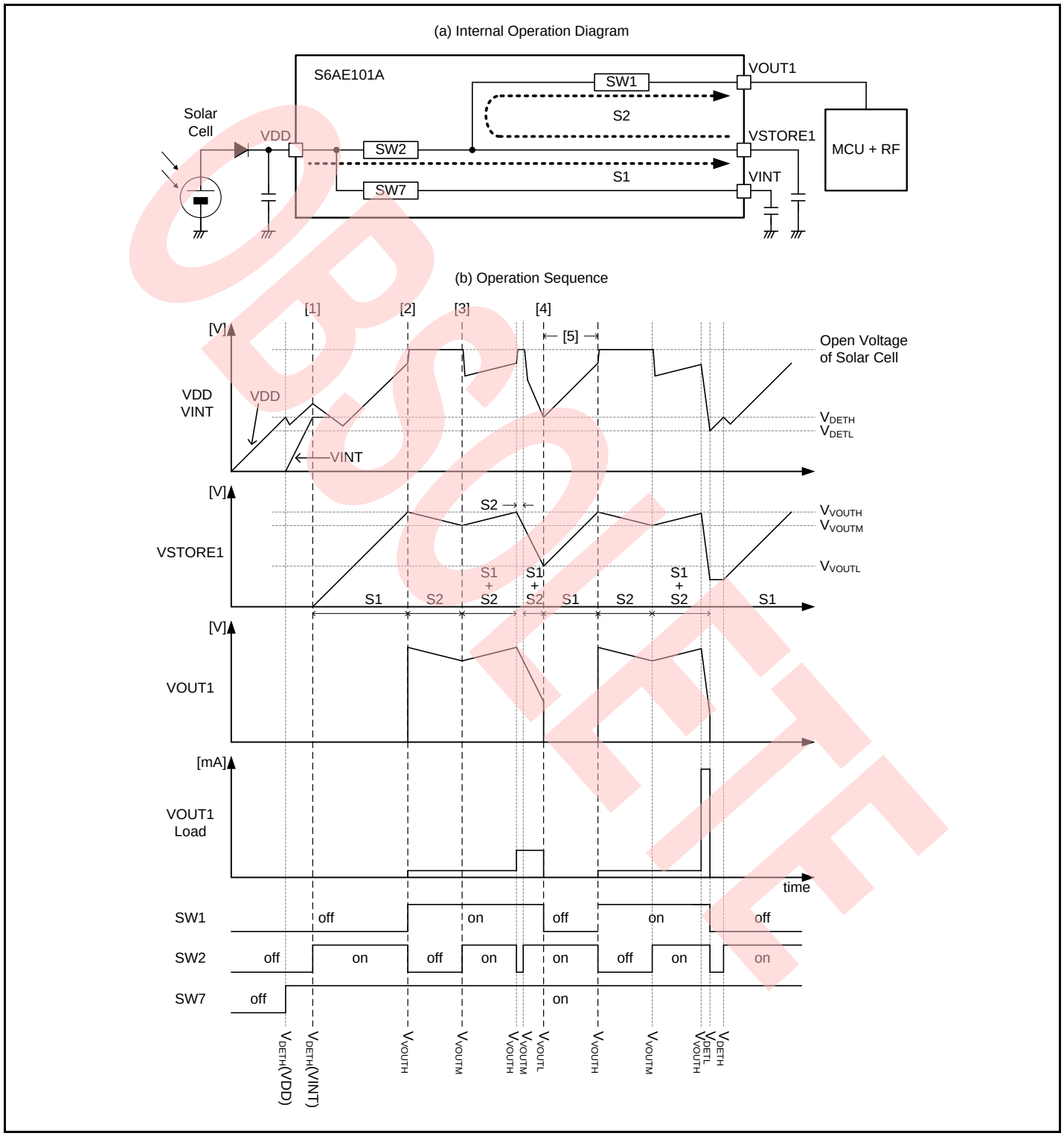
[3] When the voltage of the VSTORE1 pin falls to the input power reconnect voltage (V_{VOUTM}) or less, SW2 connects the path S1 (path S1+S2).

[4] In addition, when the voltage falls to the threshold value (V_{VOUTL}) or less that was set by the SET_VOUTL pin, SW1 disconnects the path S2.

[5] When SW1 disconnects the path S2, the discharge function is activated.

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Figure 7-2 VDD Pin Input Power Operation



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2. VBAT input voltage operation

This section describes operation when the VBAT pin is set as the input power (Figure 10-3).

[1] When the voltage of the VBAT pin reaches the power detection voltage (VDETH = 1.55V) or higher, the switch (SW2) connects VBAT and VSTORE1 (path S3). Also, when the voltage of the VDD pin falls to the power undetection voltage (VDETL = 1.45V) or less, SW4 disconnects the path S3.

[2] When the voltage of the VSTORE1 pin reaches the threshold value (VVOUTH) or higher that was set by the SET_VOUTH pin, SW4 disconnects the path S3. Also, the VOUT switch (SW1) connects VSTORE1 and VOUT1 (path S2).

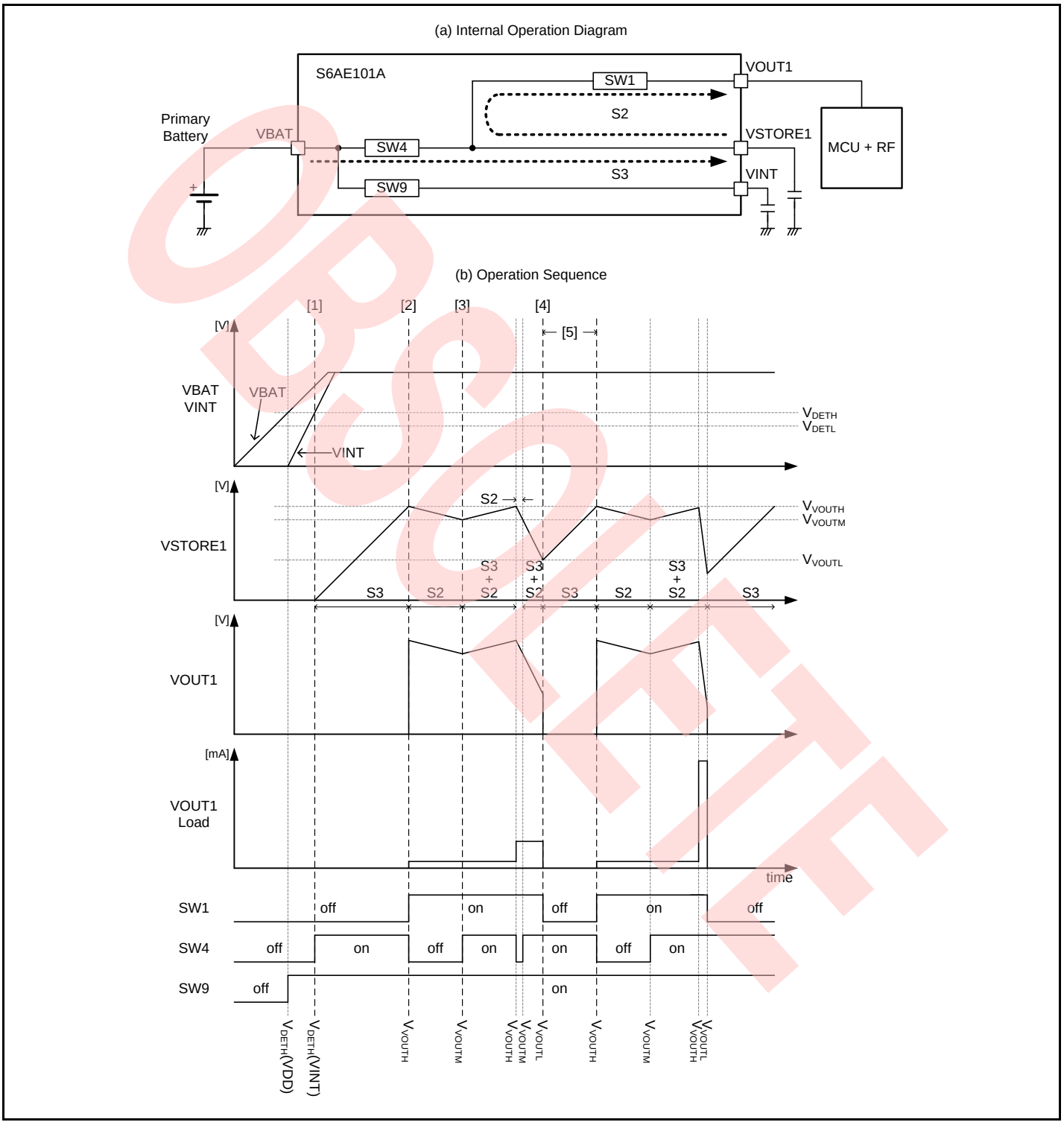
[3] When the voltage of the VSTORE1 pin falls to the input power reconnect voltage (VVOUTM) or less, SW4 connects the path S3 (path S3+S2).

[4] In addition, when the voltage falls to the threshold value (VVOUTL) or less that was set by the SET_VOUTL pin, SW1 disconnects the path S2.

[5] When SW1 disconnects the path S2, the discharge function is activated.

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Figure 7-3 VBAT Pin Input Power Operation



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3. Input power supply switching

This section describes the input power switching operation (Figure 7-4).

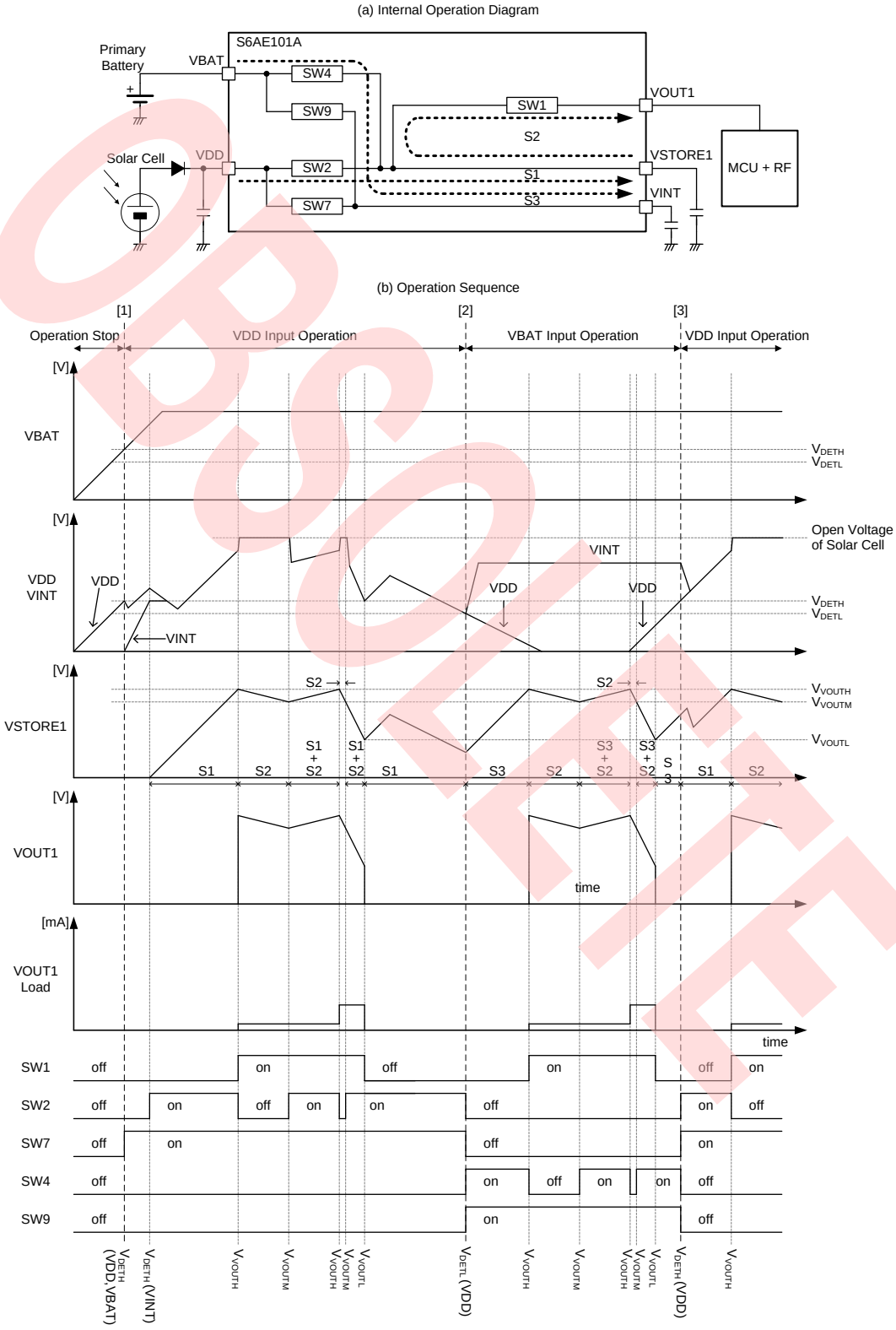
[1] If the voltages of the VDD pin and VBAT pin increase from a state where both are less than the power detection voltage (V_{DETH} = 1.55V) so that the voltage of the VDD pin reaches the power detection voltage (V_{DETH} = 1.55V) or higher, and operation switches to VDD input power operation back from the stage of disconnecting all paths.

[2] When the voltage of the VBAT pin increases to the power detection voltage (V_{DETH} = 1.55V) or higher, if the power from the solar cell is reduced, and when the voltage of the VDD pin falls to the power undetection voltage (V_{DETL} = 1.45V) or less, operation switches from VDD input power operation to VBAT input power operation.

[3] When the amount of power supplied from the solar cell increases, and the voltage of the VDD pin reaches the power detection voltage (V_{DETH} = 1.55V) or higher, operation switches back to VDD input power operation. After switching, operation is performed based on VDD input power operation.

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Figure 7-4 Input Power Switching

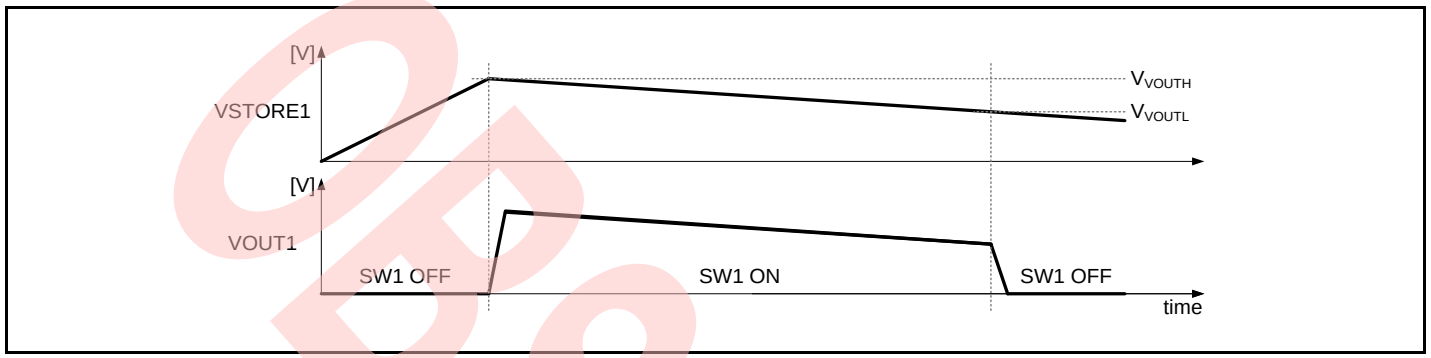


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7.2 Power Gating

This IC has a power gating function for the external system. Once it is detected that the voltage of the VSTORE1 pin has reached the VOUT maximum voltage (VVOUTH), the VSTORE1 pin and VOUT pin are connected by an internal switch until the VOUT minimum voltage (VVOUTL) is reached.

Figure 7-5 Power Gating Operation



7.3 Discharge

This IC includes a VOUT1 pin discharge function.

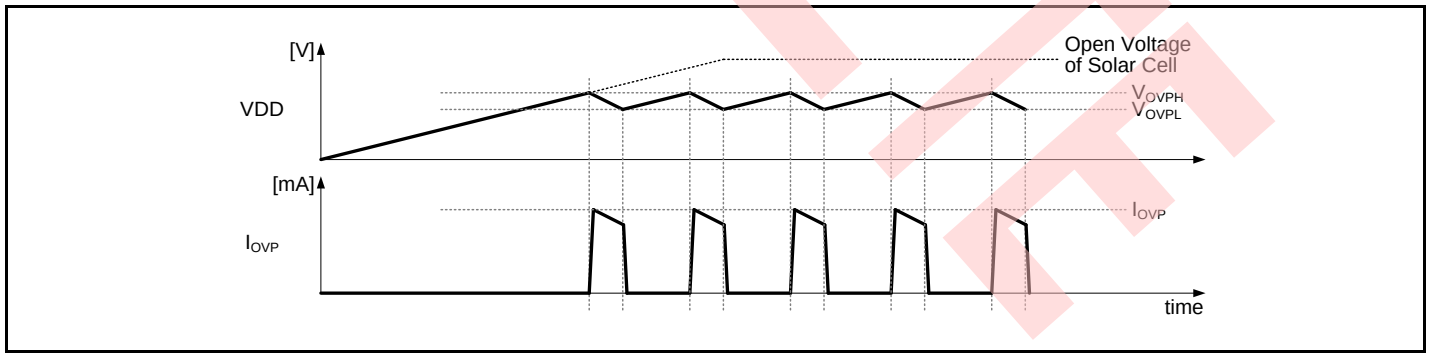
When SW1 disconnects the VSTORE1 and VOUT1 path, the discharge circuit is activated between the VOUT1 pin and GND. The power of the VOUT1 pin is discharged to the GND level.

7.4 Over Voltage Protection (OVP Block)

This IC includes an input overvoltage protection (OVP) function for the VDD pin voltage.

When the VDD pin voltage reaches the OVP detection voltage (V_{OVPH}=5.4V) or higher, the OVP current (IOVP) from the VDD pin is drawn in for limiting the increase in the VDD pin voltage for preventing damage to the IC. Also, when the OVP release voltage (V_{OVPL}=5.3V) or less is reached, drawing-in of the OVP current is stopped.

Figure 7-6 OVP Operation



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8. Application Circuit Example and Parts list

Figure 8-1 Application Circuit Example

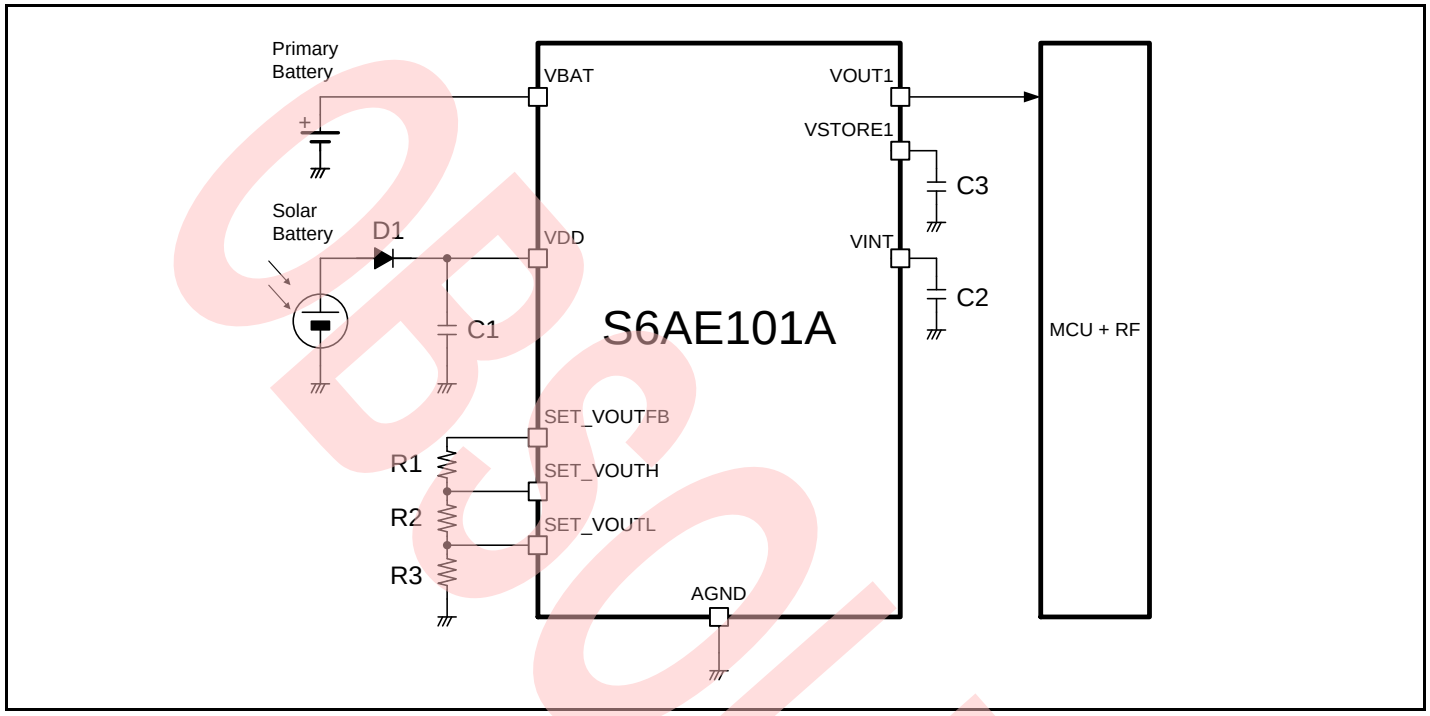


Table 8-1 Parts List

Symbol	Item	Value	Remarks
C1	Ceramic capacitor	10 µF	–
C2	Ceramic capacitor	1 µF	–
C3	Ceramic capacitor	100 µF	–
R1	Resistor	6.8 MΩ (*1)	–
R2	Resistor	2.7 MΩ (*1)	–
R3	Resistor	9.1 MΩ (*1)	–
D1	Diode	–	–

*1: Setting of VOUT maximum voltage: $V_{VOUTH} \approx 3.3V$, VOUT minimum voltage: $V_{VOUTL} \approx 2.6V$.

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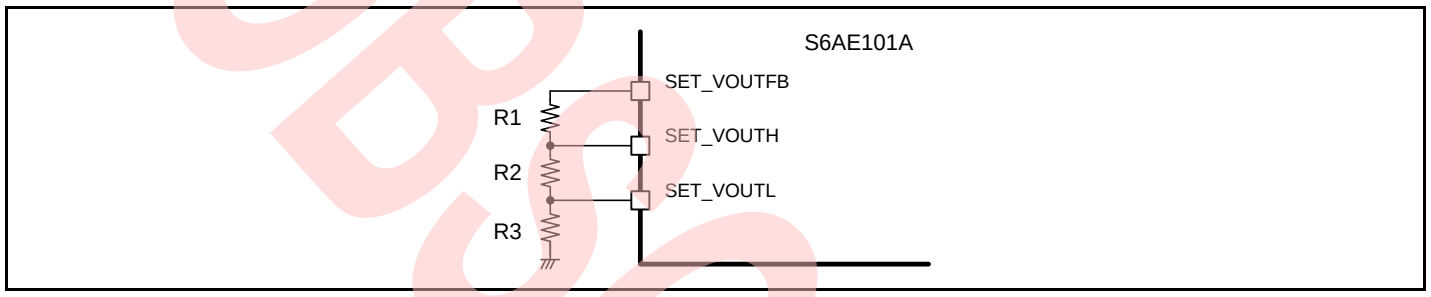
9. Application Note

9.1 Setting the Operation Conditions

Setting of output voltage (VOUT1)

The resistor connecting the SET_VOUTH pin and SET_VOUTL pin can be changed to set the VOUT1 output voltage of this IC. This is because the VOUT maximum voltage (V_{VOUTH}) and VOUT minimum voltage (V_{VOUTL}) are set based on the connected resistance. The SET_VOUTFB pin outputs a reference voltage for setting the VOUT maximum voltage and VOUT minimum voltage. Resistor voltage division can be performed on this reference voltage outside the IC for creating a voltage applied to the SET_VOUTH pin and SET_VOUTL pin.

Figure 9-1 Setting of output voltage (VOUT1)



The VOUT maximum voltage (V_{VOUTH}) and VOUT minimum voltage (V_{VOUTL}) can be calculated using the formulas below.

VOUT maximum voltage

$$V_{VOUTH}[V] = \frac{57.5 \times (R2 + R3)}{11.1 \times (R1 + R2 + R3)}$$

VOUT minimum voltage

$$V_{VOUTL}[V] = \frac{57.5 \times R3}{11.1 \times (R1 + R2 + R3)}$$

The characteristics when the total value for R1, R2, and R3 is from 10 MΩ to 50 MΩ are shown in "6. Electrical Characteristics".

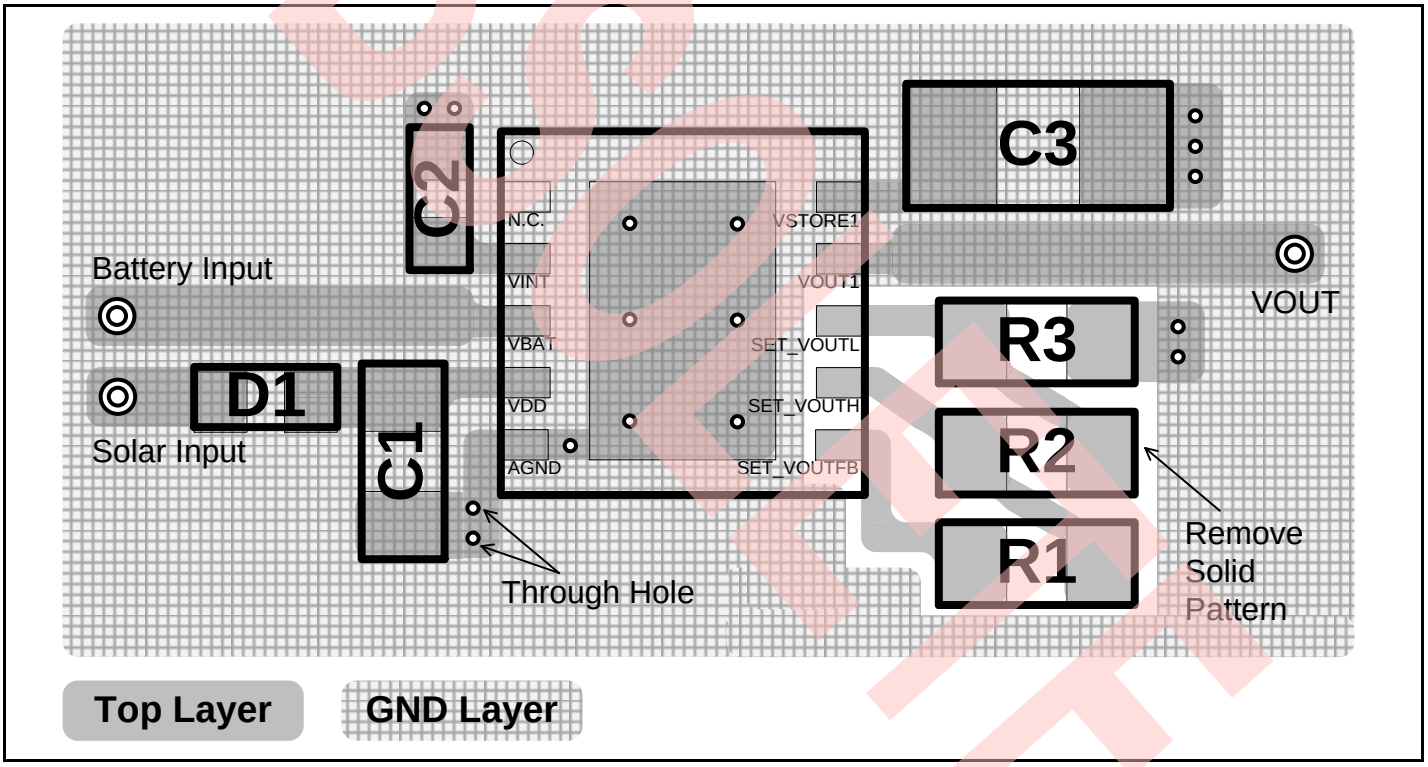
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9.2 PCB Layout

Take into account the following points when designing the layout.

- Try to route the wiring for the diode (D1) and input capacitor (C1) for connecting the solar cell on the top layer as much as possible, and avoid implementing a connection using a through hole.
- For the AGND pin of S6AE101A, provide a through hole nearby, and connect it to the GND plane.
- Locate the capacitor (C2) for the internal power as near as possible to the VINT pin.
- Locate the resistors (R1, R2, R3) for setting the output voltage in a grid-type configuration with small loops, and locate them as near as possible to each pin (SET_VOUTFB, SET_VOUTH, SET_VOUTL). Also, removing the GND plane under the parts can be effective in preventing malfunctions due to the leakage current.
- To prevent a leakage current, locate and route the storage capacitor (C3) as far as possible from patterns that are different from the electrical potential of VSTORE1 (such as the GND line). Generally, the insulation resistor of printed circuit boards is extremely high, and normally, the passing of leakage current through the board does not pose a problem. However, in certain rare cases, the surface of the board may have a low insulation resistance, and when using these boards, a leakage current that cannot be ignored may occur.

Figure 9-2 PCB Layout Example



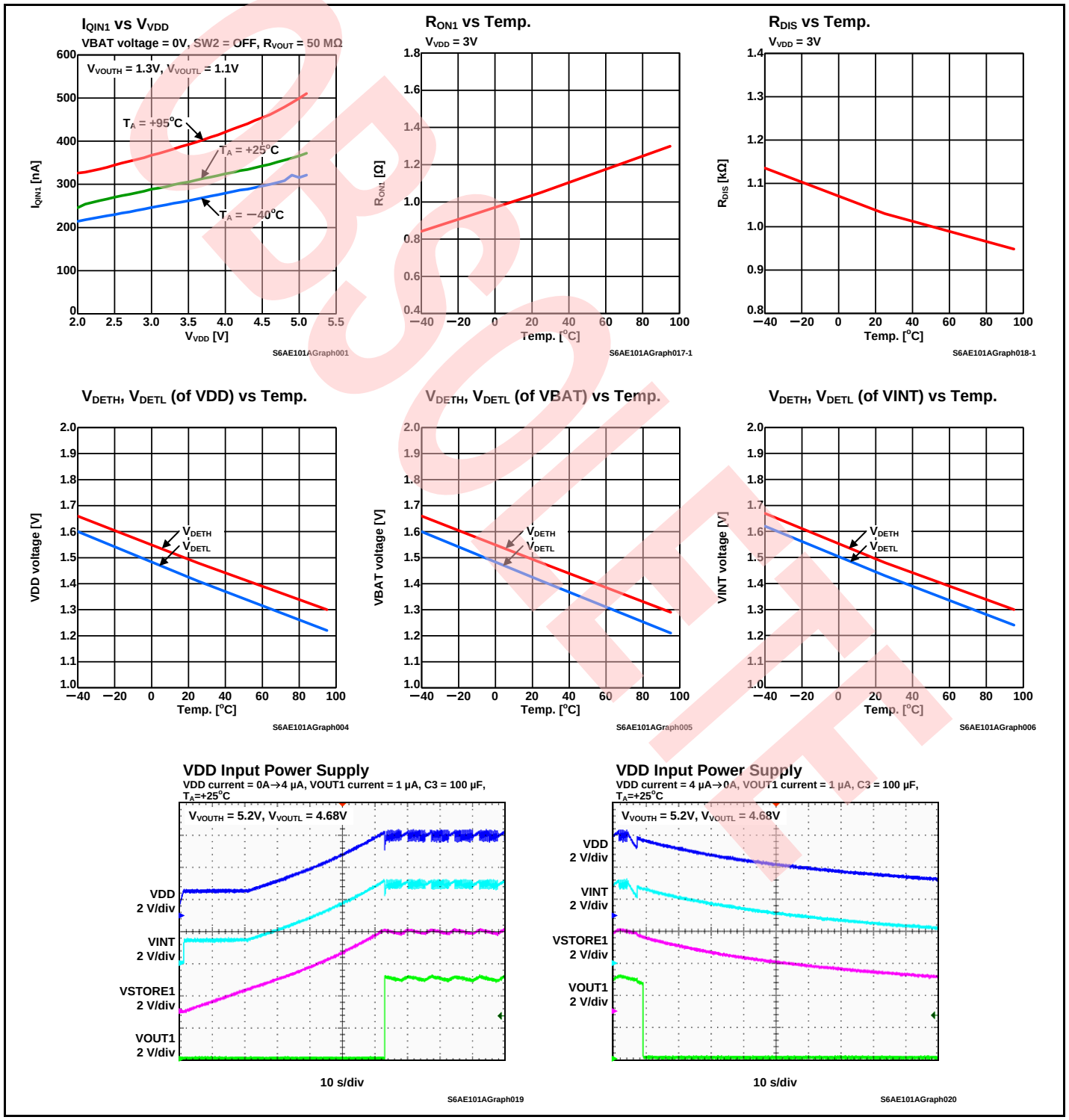
10. Development Support

This IC has a set of documentation, such as application notes, development tools, and online resources to assist you during your development process. Visit www.cypress.com/energy-harvesting to find out more.

11. Reference Data

For the circuit diagram of the reference data, Refer to "Figure 8-1 Application Circuit Example".

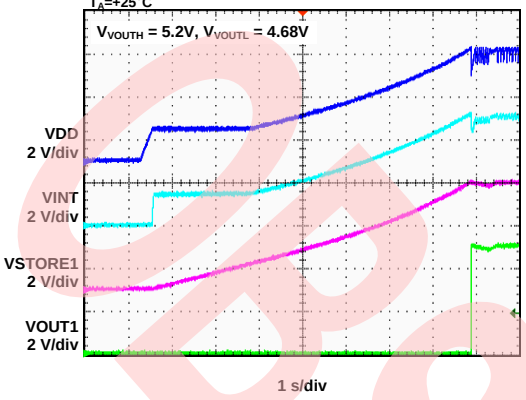
Figure 11-1 Reference Data



Preliminary

VDD Input Power Supply

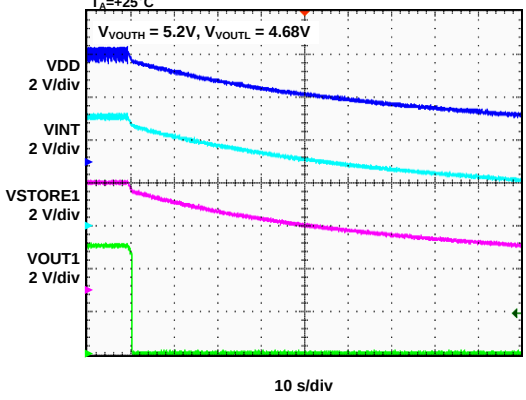
VDD current = 0A→40 µA, VOUT1 current = 10 µA, C3 =100µF, T_A=+25°C



S6AE101AGraph021

VDD Input Power Supply

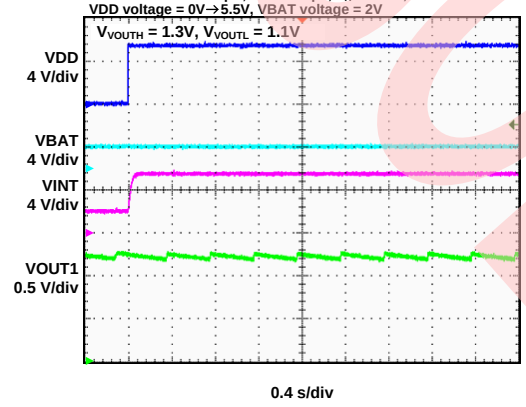
VDD current = 40 µA→0A, VOUT1 current = 10 µA, C3 =100µF, T_A=+25°C



S6AE101AGraph022

VDD & VBAT Input Power Supply

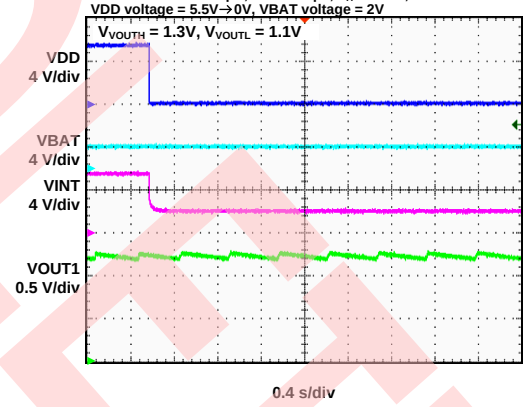
VOUT1 current = 10 µA, C3 = 100 µF, T_A= +25°C, VDD voltage = 0V→5.5V, VBAT voltage = 2V



S6AE101AGraph027

VDD & VBAT Input Power Supply

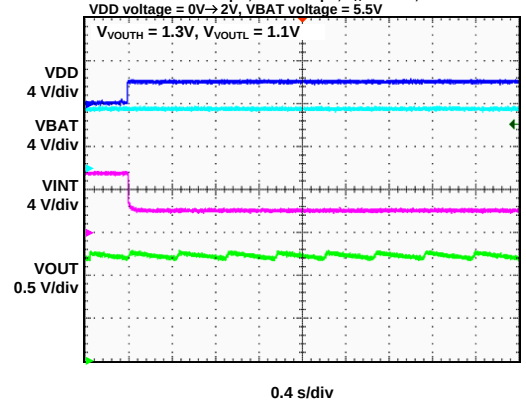
VOUT1 current = 10 µA, C3 = 100 µF, T_A= +25°C, VDD voltage = 5.5V→0V, VBAT voltage = 2V



S6AE101AGraph028

VDD & VBAT Input Power Supply

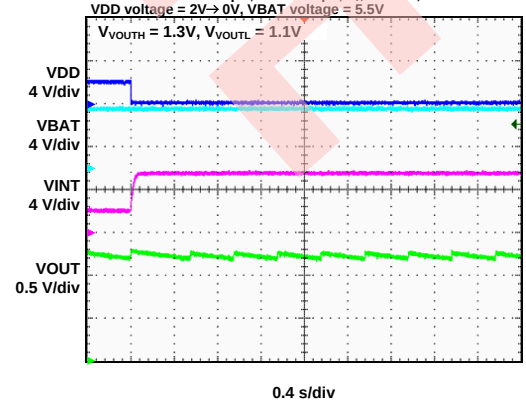
VOUT1 current = 10 µA, C3 = 100 µF, T_A= +25°C, VDD voltage = 0V→2V, VBAT voltage = 5.5V



S6AE101AGraph029

VDD & VBAT Input Power Supply

VOUT1 current = 10 µA, C3 = 100 µF, T_A= +25°C, VDD voltage = 2V→0V, VBAT voltage = 5.5V



S6AE101AGraph030

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12. Usage Precaution

Printed circuit board ground lines should be set up with consideration for common impedance.

Take appropriate measures against static electricity.

- Containers for semiconductor materials should have anti−static protection or be made of conductive material.
- After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
- Work platforms, tools, and instruments should be properly grounded.
- Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ in serial body and ground.

Do not apply negative voltages.

The use of negative voltages below −0.3 V may make the parasitic transistor activated to the LSI, and can cause malfunctions.

13. RoHS Compliance Information

This product has observed the standard of lead, cadmium, mercury, Hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE).

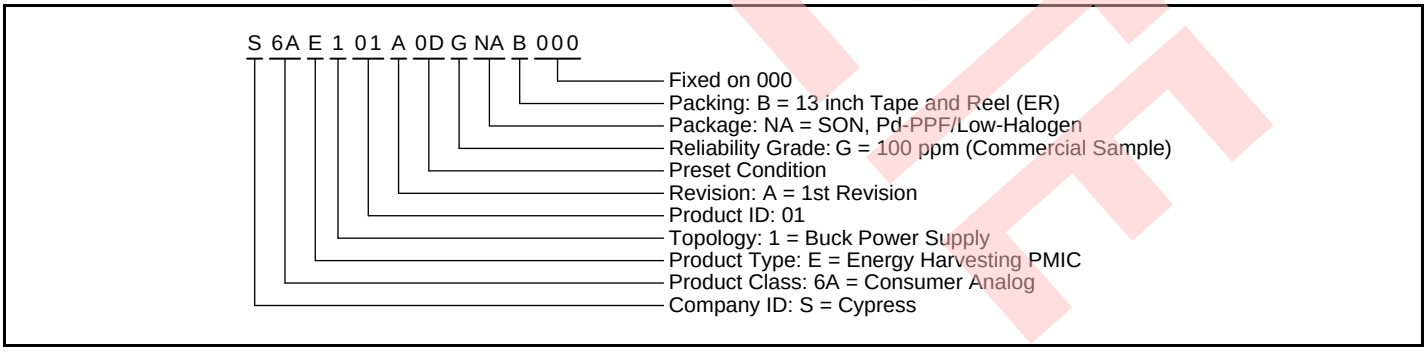
14. Ordering Information

Table 14-1 Ordering Part Number

Part number (MPN)	Package
S6AE101A0DGNAB000	10-pin plastic SON (0.5mm pitch) (VNE010)

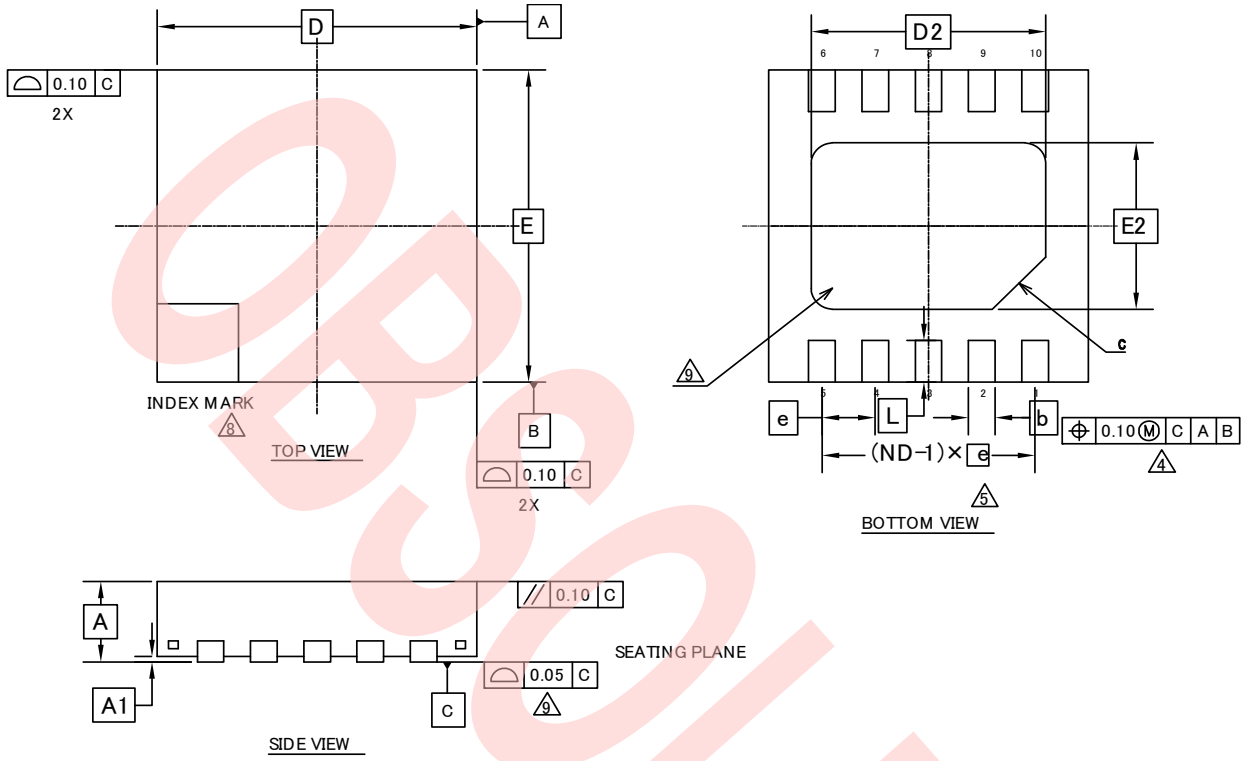
MPN: Marketing Part Number

Figure 14-1 Ordering Part Number Definitions



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15. Package Dimensions



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	0.90
A1	0.00	——	0.05
D	3.00 BSC		
E	3.00 BSC		
b	0.20	0.25	0.30
D_2	2.20 BSC		
E_2	1.60 BSC		
e	0.50 BSC		
c	0.50 REF		
L	0.30	0.40	0.50

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING CONFORMS TO ASME Y14.5-1994.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND REFER TO THE NUMBER OF TERMINALS ON D OR E SIDE.
6. MAX. PACKAGE WARPAGE IS 0.05mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LOCATED WITHIN INDICATED ZONE.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

002-10864 **

PACKAGE OUTLINE, 10 LEAD DFN
3.0X3.0X0.9 MM VNE010 2.2X1.6MM EPAD (SAWN) REV**

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16. Major Changes

Spansion Publication Number: S6AE101A_DS405-00026

Page	Section	Change Results
Preliminary 0.1		
–	–	Initial release

NOTE: Please see "Document History" about later revised information.

Document History

Document Title: S6AE101A Energy Harvesting PMIC for Wireless Sensor Node
Document Number: 002-08493

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	–	TAOA	04/27/2015	New Spec.
*A	5054369	TAOA	12/17/2015	Added Block Diagram Updated 5. Recommended Operating Conditions Updated 6. Electrical Characteristics Updated Table 8-1 Parts List Updated 9.1 Setting the Operation Conditions: Changed the formulas for the VOUT maximum voltage and VOUT minimum voltage.
*B	5103619	HIXT	01/25/2016	Added Figure 2-1 I/O Pin Equivalent Circuit Diagram Updated Figure 3-1 Architecture Block Diagram Added 10. Development Support Added 11. Reference Data
*C	5738855	GNKK	05/16/2017	Updated the Cypress logo.
*D	6364689	EIFU	10/25/2018	Remove Easy DesignSim comment
*E	7622363	ATTS	01/27/2022	Obsolete document. Completing Sunset Review.

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