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"Positive Only" Gate Drive IGBTs Created by Cres Minimization

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Previously, the general practice is to provide Insulated Gate Bipolar Transistors (IGBTs) with a gate characteristic that requires a negative gate drive bias to assure adequate turn-off when a high dv/dt is applied to the IGBT in a half bridge topology. However, providing the negative bias adds gate drive complexity. It also makes it difficult to use high voltage IC drivers because the ICs are designed to operate at ground reference – the same as the control circuitry. Thus it would be desirable to develop an IGBT that has high dv/dt capability when "positive only" gate drive is used. Such a device has been developed. The developed device performance is examined against an IGBT that requires negative gate drive. Successful results under high dv/dt applied conditions are reported.

To minimize the device partial turn-on when high dv/dt is imposed on the partial turn-on, the first step is to fully understand the cause elements. The three major IGBT parasitic capacitances are shown in Figure 1. – Cce, Cgc, and Cge.

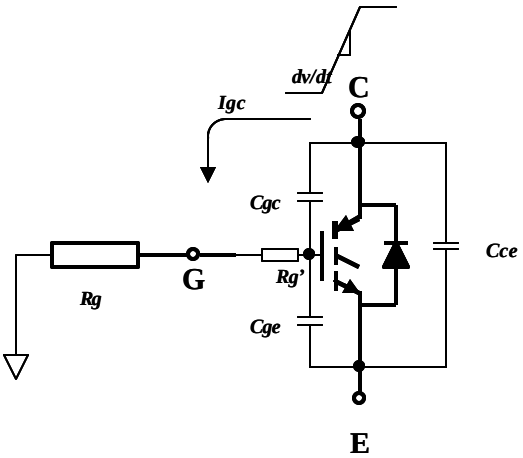


Figure 1. IGBT device parasitic capacitances

Because this is a major issue in bridge converter design, Cies, Coes, and Cres are reported in most IGBT datasheets
where

Coes = Cce + Cgc
Cres = Cgc

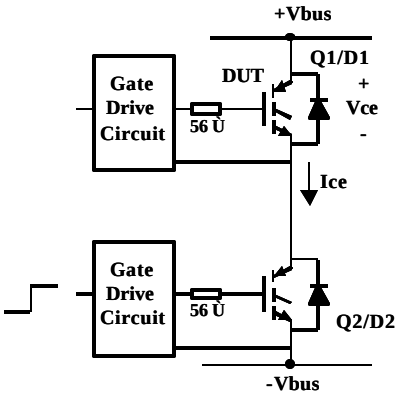


Figure 2. Half Bridge Circuit

A typical half bridge circuit, used in many converter designs is shown in Figure 2. Due to the parasitic capacitance, Cgc, a high voltage rate of rise during turn on of Q2 can induce momentary turn on Q1. This can happen even though the gate drive is biased to ground or even slightly negative. This is known as dv/dt turn on. It is due to the dv/dt imposed on the collector creating a current from collector to gate through the capacitor Cgc. The magnitude of the induced current in the gate is dependent upon

1. the size of Cgc
2. the proportionate values of Cgc and Cge
3. the value of the dv/dt
4. the value of Rg, Rg'

If the current is high enough, then a positive voltage is present on the gate of Q1 with respect to ground. This in turn will cause partial turn-on of Q1 – or dv/dt turn-on. This can represent significant power loss because high voltage is also present across Q1 when the dv/dt induced turn-on occurs.

To minimize this cross coupling current and prevent the device from turning on, the following steps can be taken…

A. During turn-off, bring the gate to a negative voltage large enough to override the dv/dt effect. This requires the use of more complex gate drive circuits.

B. Or design the IGBT to reduce Cgc parasitic capacitance and the internal Rg'.

Further, there is a secondary effect to the Cgc that is worth investigating. Looking at a typical set of IGBT parasitic capacitance curves for an IGBT that requires negative gate drive, the Cres curve (as well as the other curves) shows that it exhibit a characteristic of remaining quite high until the Vce voltage reaches almost 15V. The effective value of Cres could be further reduced if this "plateau" characteristic were reduced or eliminated.

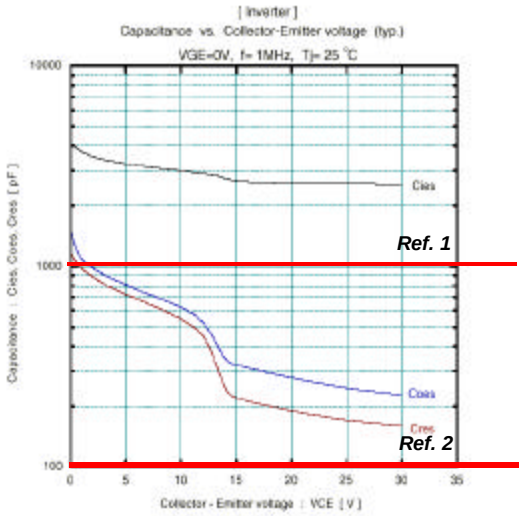


Figure 3. Cies, Coes, and Cres vs. Vce
For an IGBT that requires negative gate drive

The Cres and Coes curves remain at a value close to the value at Vce = 0 and then at Vce=14V, the finally reduce to a lower level for values of Vce beyond 15V. The phenomenon is caused by the intrinsic JFET with in the IGBT. If the JFET could be minimized, Cies and Coes would reduce much faster with increased Vce. Again this could potentially reduce the effective Cres and in turn reduce the susceptibility of the IGBT to dv/dt turn-on.

C. Thus we come to the last improvement element – reduction of the JFET effect

One of the IGBTs developed with reduced Cres and reduced JFET effect is the IRGP30B120KD-E 1200V, 30 Ampere NPT IGBT. It is a CoPak™ device with an anti-parallel diode soft recovery ultrafast diode contained within the package with the IGBT.

These target parameters were minimized by
Using smaller polysilicon gate width
Minimizing the JFET effect
Use cellular geometry

The performance is compared between two 25 Ampere NPT 1200V IGBT devices – a device that requires negative drive and a device that the IR IRGP30B120KD-E device. It was shown that the competitive device exhibited significantly higher cross coupling current when driven from a resistive impedance of 56 ohms.

Comparing the parasitic capacitances reported in the data sheets for both of these devices…

@Vce = 0V	Cies (pf)	Coes (pf)	Cres (pf)
Neg. Gate Dr. IGBT	4000	1400	1100
IRGP30B120KD-E	3000	900	350

Figure 4. Parasitic Capacitance Comparison

There has been reduction in all three capacitances
Cies is reduced 25%
Coes is reduced 35%
And
Cres is reduced 68%

Further reviewing these capacitances as Vce transcends the first 35 volts in Figure 5. This shows that the IRGP30B120KD-E has been designed to effectively reduce the Cres capacitance. At Vce = 0V, the negative gate drive device shows a Cres of 1100 pf while the IRGP30B120KD-E is 350 pf. At Vce = 30V, the negative gate drive device shows a Cres of 170pf, as compared with the IRGP30B120KD-E Cres = 78 pf. This clearly shows that the IRGP30B120KD-E has been designed to have significantly less Cres and it would be expected that for the same dv/dt condition, the dv/dt turn-on current would be significantly less.

Reference lines 1 and 2 are provided to help the visual comparison of the capacitances vs. Vce.

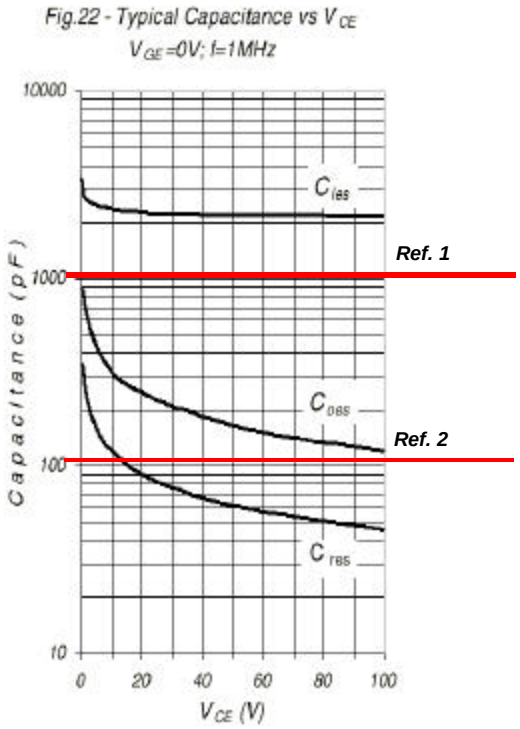


Figure 5. Cies, Coes, and Cres vs. Vce
For IRGP30B120KD-E

Now examining the comparative performance in the circuit, both the IRGP30B120KD-E and the negative gate drive IGBT were placed in the identical test circuit and the dv/dt turn-on current was measured.

The test circuit is shown in Figure 6

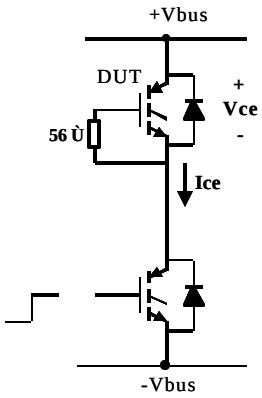


Figure 6. dv/dt turn-on current test circuit

Test conditions:

Dv/dt = 3000V/usec
Vbus = 600V
Rg = 56 ohms
Ta = 125 deg. C

The negative gate drive IGBT had a dv/dt induced turn-on current of 18 amperes as shown in figure 7

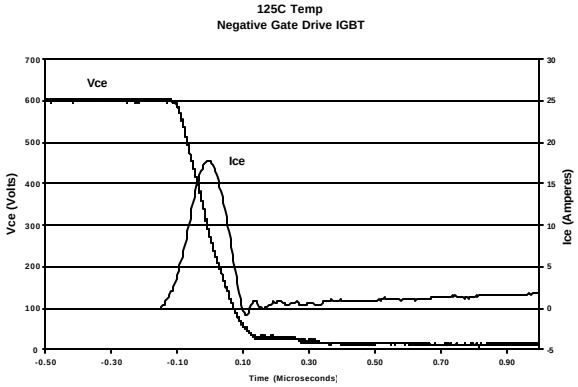


Figure 7. Vce & Ice vs. time
dv/dt turn-on current

The IRGP30B120KD-E "positive only" gate drive IGBT showed only 1.9 amperes dv/dt induced turn-on current as shown in the waveforms in figure 8.

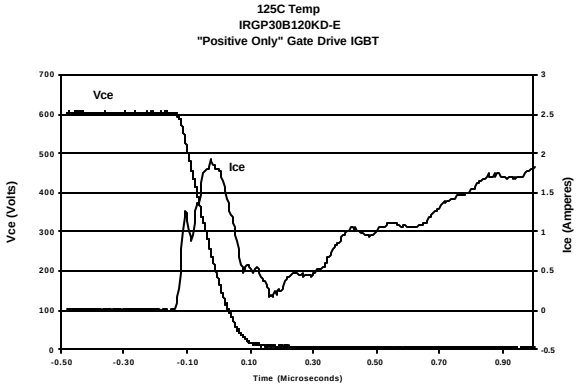


Figure 8. Vce & Ice vs. time
dv/dt turn-on current

It could be concluded that the reduction a 1.9/18 amperes or a 9:1 reduction. However, the effect of the diode current has not been fully considered in this test. To isolate the IGBT contribution to the coupled current, the current

was measured with only the antiparallel diode D1 as shown in Figure 9 as Ice (cntrl).

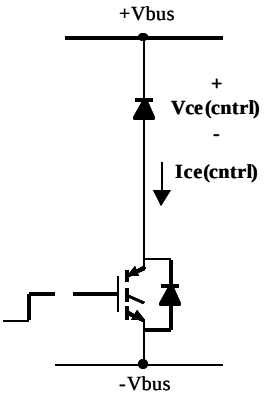


Figure 9. dv/dt turn-on current test circuit - diode only

The Ice current without any IGBT is shown in figure 10 for the negative gate drive IGBT and in figure 11 for the IRGP30B120KD-E "positive only" gate drive. The current for both is quite low at 1 ampere and 0.8 ampere respectively.

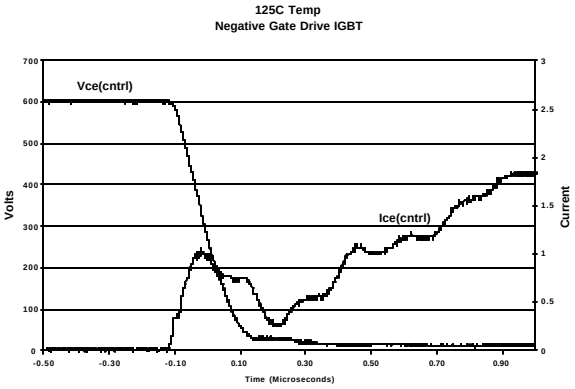


Figure 10. Vce & Ice vs. time dv/dt turn-on current test -diode only

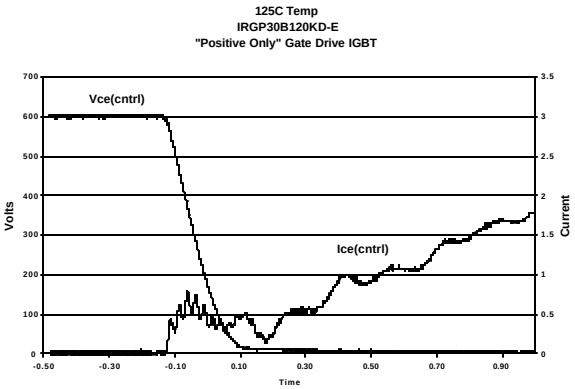


Figure 11. Vce & Ice vs. time dv/dt turn-on current test -diode only

Now if the diode current is removed from the total IGBT/diode current of figures 10 and 11, the result is

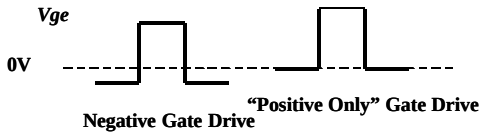
Ice (negative gate drive IGBT) = 18 – 1 = 17 amperes

Ice (IRGP30B120KD-E) = 1.9 – 0.8 = 0.8 ampere

So the total reduction is 17/0.8 = 21

Under these same conditions, the circuit performance of the IRGP30B120KD shows a 21:1 reduction in dv/dt induced turn-on current when the gate is at 0V or the "positive only" gate drive condition. The current is low enough that there is little further contribution to power loss if the IGBT is driven in that manner.

There many benefits to having a "positive only gate drive IGBT.



Gate Drive Waveforms
Figure 12

These benefits are:

- Don't need minus power supply
- Simpler gate drive circuit
- Lower cost gate drive
- Higher gate noise immunity
- Higher IGBT dv/dt capability
- Compatible with IR high voltage IC Gate Drivers - Much less shoot thru current

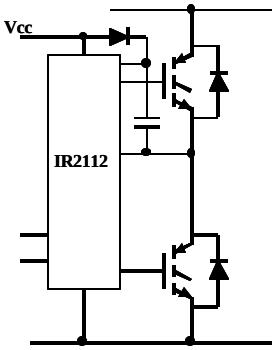


Figure 13. Schematic with high voltage gate drive IC

The above design has been equally successfully implemented in Punch Through IGBTs.

Conclusions

The "positive only" gate drive IGBT is a significant step forward in device design. In fact, the IRGP30B120KD-E Cres value is low enough to allow very acceptable switching performance with a positive-only gate drive condition. Indeed, the device is rated to have that type of gate drive. No negative gate drive is necessary to assure the device is off – even 3 Volt/nsec dv/dt imposed on the collector. This makes it very compatible for use with high voltage IC gate drivers that have positive-only voltage output to drive the IGBT.

This provides an IGBT that has compatibility with high voltage IC drivers now available in the market. It also enables much higher dv/dt topology designs for the future. It is expected that future designs will build on the development shown here.

Bibliography

[1] International Rectifier Application Note AN-983A, 'IGBT Characteristics', S. Clemente, A. Dubhashi, B.Pelly, G. Dokopolous

[2] International Rectifier Application Note AN-990, 'Application Characterization of IGBTs', S. Clemente