3.3 kW high-frequency, high-density PSU with three-level flying capacitor PFC for server and data center applications

REF_3K3W_3LFC_PSU

About this document

Scope and purpose

This document presents a comprehensive system solution from Infineon for a high-power density 3.3 kW power supply unit (PSU) specifically designed to meet the stringent performance and efficiency requirements of server and data center applications.

The PSU solution described implements a three-level flying capacitor (3LFC) power factor correction (PFC) and incorporates a planar magnetic construction in the LLC DCDC stage, enabling efficient and reliable operation in various applications.

The document summarizes the converter hardware design and presents experimental results to provide design guidelines for an Infineon-based solution.

The REF_3K3W_3LFC_PSU evaluation board features a two-stage plus baby-boost architecture containing a front-end three-level AC-DC converter that utilizes bridgeless topology. The board offers improved PFC and a lower total harmonic distortion (THD), resulting in a more efficient and reliable power conversion process.

An intermediate baby-boost converter addresses the hold-up time requirements without needing a bulky DC link capacitor, increasing power density. The backend isolated DC-DC converter employs a GaN half-bridge (HB) LLC converter with full-bridge (FB) rectification, providing safety isolation and regulating the output voltage.

The PSU solution offers several benefits, including improved PFC and reduced THD, increased power density due to reduced overall bulk capacitance, high peak efficiency of 97.6% at 230 VAC input line (excluding internal fan), and a compact overall dimension of 72 mm x 192 mm x 40 mm, resulting in a power density of almost 98 W/inch^3.

The design guidelines presented in this document provide a comprehensive overview of the converter hardware design and experimental results, enabling designers to develop their own high power density PSU solutions.

Intended audience

The document and the related REF_3K3W_3LFC_PSU hardware is intended for R&D engineers, hardware designers, and developers of power electronic systems.

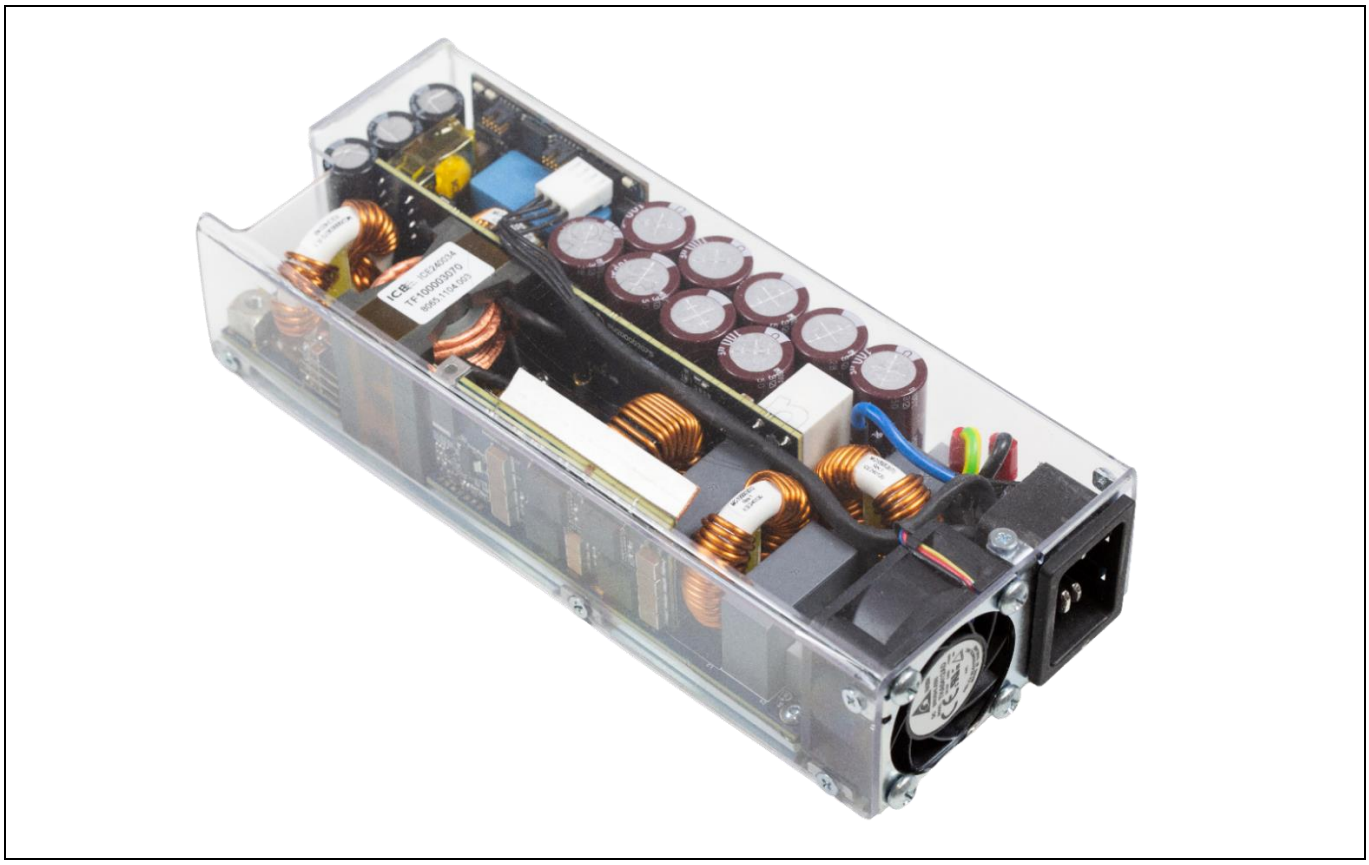

Figure 1 3.3 kW REF_3K3W_3LFC_PSU server power supply

The main Infineon components used in REF_3K3W_3LFC_PSU are:

- CoolSiC™ 400V M2, 25 mΩ TOLL (IMT40R025M2H) and EiceDRIVER™ 1EDB8275 for the 3LFC PFC converter
- CoolMOS™ 600 V CM8, 16 mΩ TOLL (IPT60R016CM8), EiceDRIVER™ 1EDN8511B, and 1EDB8275F for the slow leg of the 3LFC PFC converter and the static switch of the baby boost converter
- CoolGaN™ 650 V GIT, 35 mΩ TOLL (IGT65R035D2), EiceDRIVER™ 1EDN8550B, and 1EDB8275F for half-bridge switches at the primary side of the LLC converter
- OptiMOS™ 80 V, 4.6 mΩ source-down (IQE046N08LM5), and EiceDRIVER™ 2EDB7259K for the synchronous rectification (SR) switches at the secondary side of the LLC converter
- CoolMOS™ 600 V G7, 80 mΩ (IPT60R080G7), CoolSiC™ 600 V diode (IDL10G65C5), and EiceDRIVER™ 1EDB8275F for the baby-boost converter
- ISOFACE™ 4DIR1400H digital isolator for the primary to secondary isolation in the LLC converter
- XMC4200-Q48K256 microcontroller for the implementation of the PFC control

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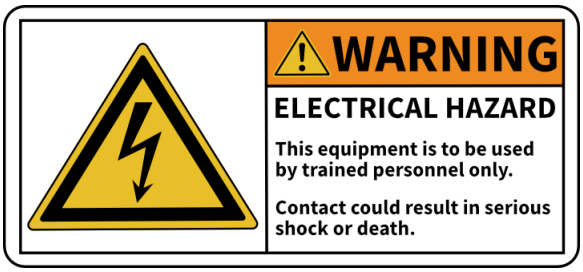
Safety information

Please read this document carefully before starting up the device.



Important notice

Evaluation boards, demonstration boards, reference boards and kits are electronic devices typically provided as an open-frame and unenclosed printed circuit board (PCB) assembly. Each board is functionally qualified by electrical engineers and strictly intended for use in development laboratory environments. Any other use and/or application is strictly prohibited. Our boards and kits are solely for qualified and professional users who have training, expertise, and knowledge of electrical safety risks in the development and application of high-voltage electrical circuits. Please note that evaluation boards, demonstration boards, reference boards and kits are provided “as is” (i.e., without warranty of any kind). Infineon is not responsible for any damage resulting from the use of its evaluation boards, demonstration boards, reference boards or kits. To make our boards as versatile as possible, and to give you (the user) opportunity for the greatest degree of customization, the virtual design data may contain different component values than those specified in the bill of materials (BOM). In this specific case, the BOM data has been used for production. Before operating the board (i.e. applying a power source), please read the application note/user guide carefully and follow the safety instructions. Please check the board for any physical damage, which may have occurred during transport. If you find damaged components or defects on the board, do not connect it to a power source. Contact your supplier for further support. If no damage or defects are found, start the board up as described in the user guide or test report. If you observe unusual operating behavior during the evaluation process, immediately shut off the power supply to the board and consult your supplier for support.

Operating instructions

Do not touch the device during operation, keep a safe distance. Do not touch the device after disconnecting the power supply, as several components may still store electrical voltage and can discharge through physical contact. Several parts, like heatsinks and transformers, may still be very hot. Allow the components to discharge and cool before touching or servicing. All work such as construction, verification, commissioning, operation, measurements, adaptations, and other work on the device (applicable national accident prevention rules must be observed) must be done by trained personnel. The electrical installation must be completed in accordance with the appropriate safety requirements.

Safety precautions

Note: *Please note the following warnings regarding the hazards associated with development systems.*

Table 1 Safety precautions

	**Warning:** *The evaluation or reference board contains DC bus capacitors, which take time to discharge after removal of the main supply. Before working on the converter system, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *The evaluation or reference board is connected to the AC input during testing. Hence, high-voltage differential probes must be used when measuring voltage waveforms by oscilloscope. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *Remove or disconnect power from the converter before you disconnect or reconnect wires, or perform maintenance work. Wait five minutes after removing power to discharge the bus capacitors. Do not attempt to service the drive until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.*
	**Caution:** *The heatsink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with the converter, power electronics and associated equipment should plan, install, commission, and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *A converter that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as undersizing the cabling, supplying an incorrect or inadequate AC supply, or excessive ambient temperatures may result in system malfunction.*

1 Background and board overview

1.1 Background

Recently, rack level power demand in server and data centers has grown substantially to accommodate the higher computing workload in limited floor space. This increase in power demand is consistently tightening the requirements in terms of power density and efficiency in power supplies – to reduce the space occupied and heat dissipated.

These requirements are defined in the “OCP rectifier v3 specifications for server and datacenter power supplies” [1], which mandates a peak efficiency of 97.5% at 230 VAC, a minimum power density of 32.15 W/inch^3 (1.96 W/cm^3), maximum dimensions of 520 × 73.5 × 40 mm, and a 20 ms hold-up time at full load.

In 2021, Infineon developed the EVAL_3KW_50V_PSU [2] board, which fully complies with these specifications. Building upon this design, EVAL_3k3_HFHD_PSU was later proposed, demonstrating techniques to further increase power density. Finally, leveraging this latter platform, the 3LFC topology discussed here was developed and implemented in REF_3K3W_3LFC_PSU. This latest solution improves efficiency and reduces PFC magnetic components while maintaining performance.

1.2 Power supply unit description

The REF_3K3W_3LFC_PSU evaluation board is made of a frontend AC-DC converter and a backend isolated DC-DC converter. The AC-DC converter is a three-level flying capacitor bridgeless PFC that provides power factor correction and limits the total harmonic distortion. The backend DC-DC is a GaN half-bridge LLC converter with full-bridge rectification. The backend provides safety isolation and regulates the output voltage. The PSU also features a baby-boost converter to comply with the hold-up time specifications of server applications with a reduced overall bulk capacitance, increasing the overall power density.

REF_3K3W_3LFC_PSU is mounted over a metallic frame and covered by a plastic enclosure to ensure proper airflow and cooling. Its dimensions are 192 mm × 72 mm × 40 mm, including a fan and an AC inlet connector. For comparison, OCP v3 specifies a maximum dimension of 520 mm × 73.5 mm × 40 mm. The measured peak efficiency of the complete PSU at 230 V_{AC} input line is 97.6%, not including the internal fan, with a power density of 98 W/inch^3. The distribution of the main blocks of the PSU is shown in Figure 2. The fan airflow sucks the air out of the chassis for a better thermal performance.

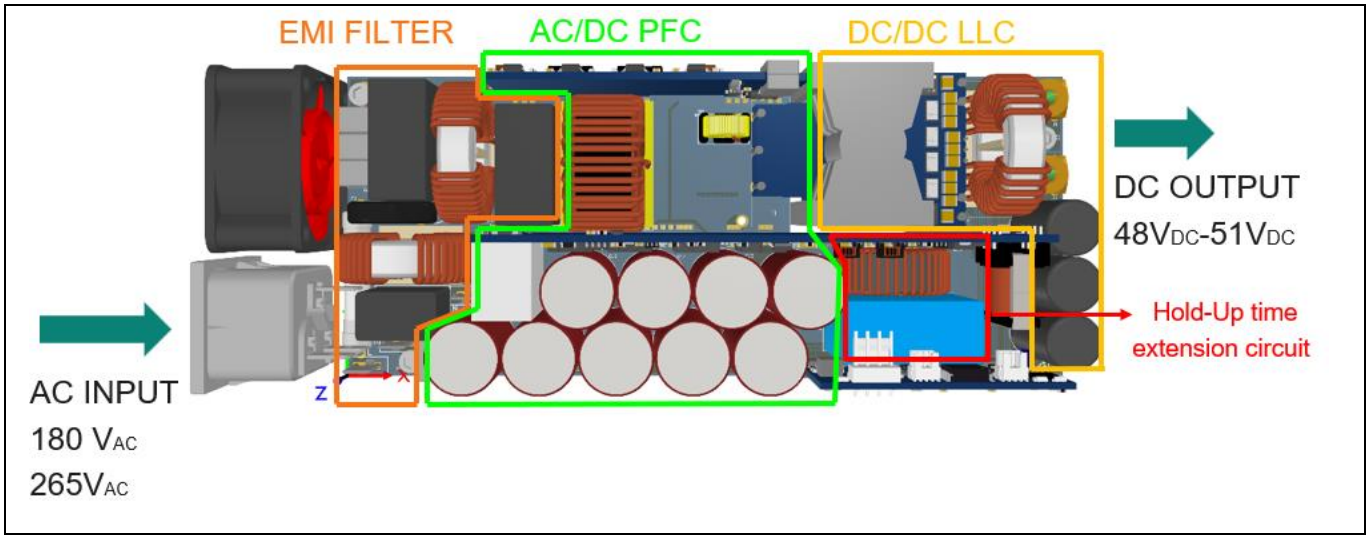


Figure 2 Overview of REF_3K3W_3LFC_PSU

To achieve the power density target, a tri-dimensional mechanical assembly is necessary and multiple daughterboards are assembled on the main PCB, as shown in Figure 3.

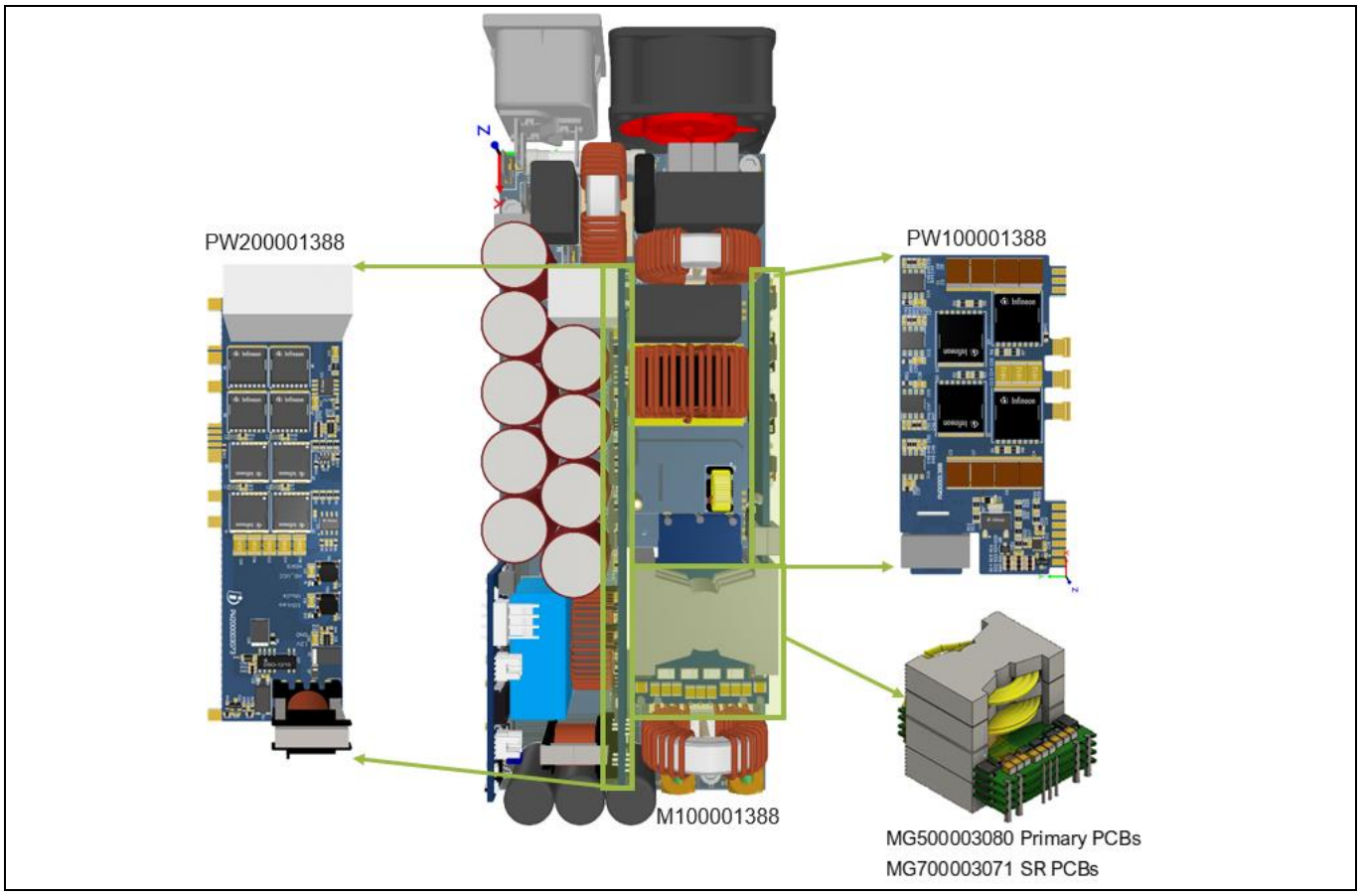


Figure 3 REF_3K3W_3LFC_PSU main board and daughter cards with their assembly

The board uses the following daughterboards:

- The main board (M1000001388) hosts the passive components of the input and output EMI filters, the PFC inductor choke, the capacitors of the intermediate bulk, and provides mechanical support and electrical connections for the daughterboards
- The three-level PFC high-frequency board (PW100001388) mounts the three-level PFC and is mounted perpendicular to the main board
- The LLC and PFC SR power card (PW200001388) is assembled at the center of the board, and hosts the PFC SR stage, the LLC primary-side, the inrush relay, and the flyback power supply for housekeeping
- The planar primary and secondary PCBs (MG500003080 and MG700003071) are embedded in the transformer structure for primary- and secondary-side planar windings
- The control PCB (CD100001388) hosts the two primary- and secondary-side controllers, and provides isolation to the UART communication channel and the PWM of the LLC half-bridge MOSFETs

1.3 Converter architecture

REF_3K3W_3LFC_PSU is a unidirectional PSU containing two stages and an auxiliary baby-boost converter. The architecture includes:

- A front-end three-level AC-DC converter that performs PFC and maintaining low THD

- An isolated half-bridge LLC DC-DC converter that provides safety isolation and regulated output voltage
- A baby-boost DC-DC stage that activates exclusively during line cycle dropouts to ensure hold-up time compliance

Figure 4 shows a simplified block diagram of the full PSU.

The control of the 3LFC AC-DC converter is implemented using Infineon's XMC™ 4200 MCU with PFC, THD, voltage regulation, inductor overcurrent protection (OCP), overvoltage protection (OVP), undervoltage protection (UVP), undervoltage lockout (UVLO) for the bulk and the flying capacitor, soft-start, synchronous rectification (SR) control, adaptive dead-times, and serial communication interface towards the LLC secondary-side controller.

The control of the LLC converter is implemented using a third-party MCU referenced to the secondary-side ground – and features voltage regulation, burst-mode operation, output OCP, OVP, UVP, UVLO, soft-start, SR control, adaptive dead-times, and a serial communication interface. The isolation between the two controllers (UART communication and PWM signals for the primary-side half-bridge of the LLC) is managed using a quad-channel digital isolator.

In the frontend AC-DC converter, the high-frequency leg uses in total four 25 mΩ CoolSiC™ 400 V switches driven by two EiceDRIVER™ 1EDB8275Y gate drivers. The low-frequency leg uses four 16 mΩ CoolMOS™ switches in parallel with a combination of EiceDRIVER™ 1EDB8275F (high-side) and EiceDRIVER™ 1EDN8115B (low-side).

For the LLC converter, four 42 mΩ CoolGaN™ are used for the half-bridge HV primary-side in conjunction with a combination of EiceDRIVER™ 1EDB8275F (high-side) and EiceDRIVER™ 1EDN8550B (low-side). For the secondary-side SR, an integrated approach is followed – the SR MOSFETs are mounted on the secondary-side PCB windings and integrated on the same magnetic structure that realizes the main transformer, the resonant inductance, and the magnetizing inductance. The LLC SR stage uses 32 pieces of 4.6 mΩ OptiMOS™ 5 power transistors, driven by 8 EiceDRIVER™ 2EDB7259K. See Section 3.3 for more information on the integrated transformer assembly.

To ensure hold-up time specifications are met while reducing the amount of bulk capacitance of the PSU, a baby-boost converter is used to decouple the bulk voltage from the LLC input during the hold-up event. During steady-state operation, the baby-boost is bypassed by a low-ohmic 16 mΩ CoolMOS™ switch.

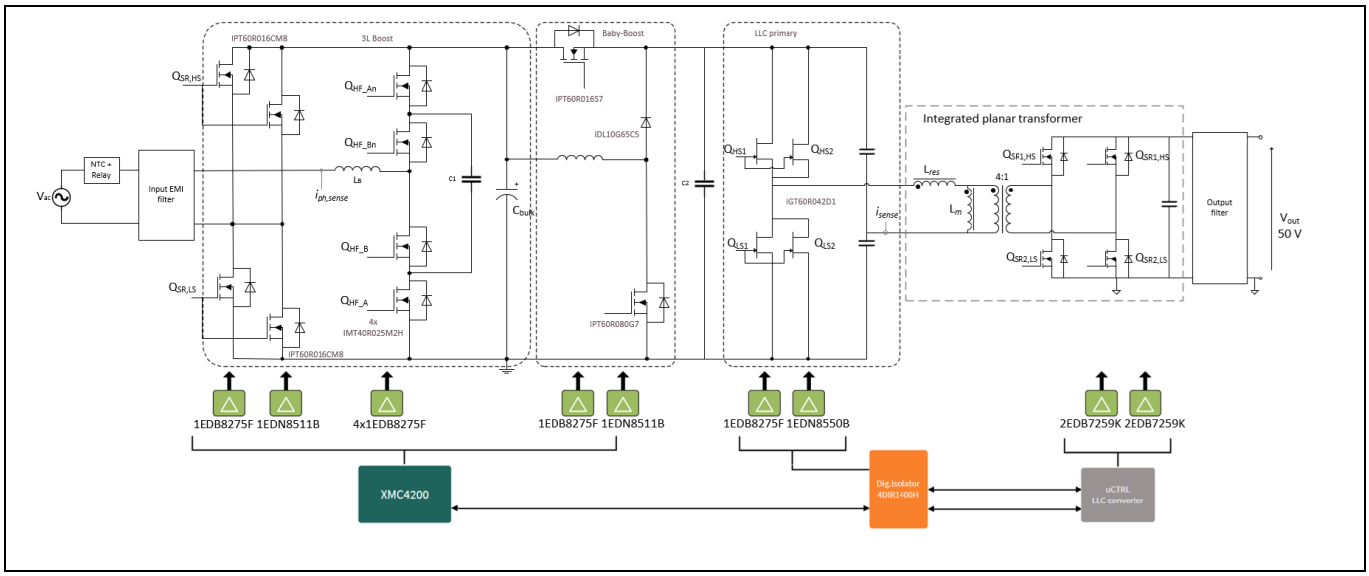


Figure 4 Simplified schematic of the REF_3K3W_3LFC_PSU prototype

2 Single-phase three-level PFC

A simplified schematic of the three-level PFC stage of REF_3K3W_3L_PSU is shown in Figure 4 while the hardware implementation of the fast SiC leg and its location within the board is shown in Figure 5. The AC inlet is followed by the NTC and relay and two-stage input EMI filter.

The AC line is connected to the high-frequency CoolSiC™ fast-leg of the three-level PFC (Q_{HF_A}, Q_{HF_B}, Q_{HF_Bn}, and Q_{HF_An} in Figure 5) via the PFC-inductor and neutral to the SR leg of the converter (Q_{SR_HS} and Q_{SR_LS} in Figure 5). The high-frequency SiC leg operates at 45 kHz switching frequency, whereas the two SR legs rectify the AC current according to the detected line voltage.

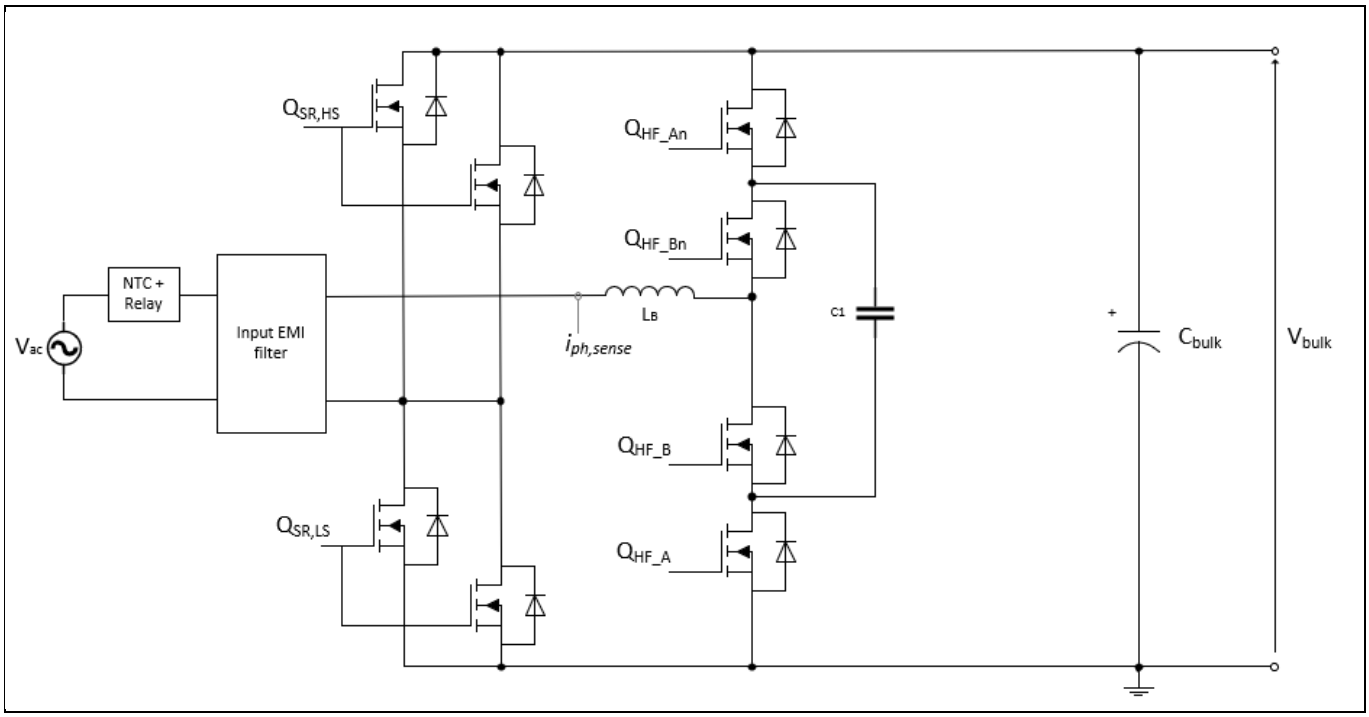


Figure 5 Simplified schematic of the AC-DC converter in REF_3K3W_3LFC_PSU

2.1 Three-level PFC converter operation

This section delves into the detailed operation of the three-level PFC converter, which can be divided into two main scenarios: when the duty cycle is lower than 0.5 and when it is higher than 0.5.

Specifically, the section examines the current flow paths involved in the charging and discharging of the flying capacitor when phase-shifted modulation is applied, providing a comprehensive understanding of the converter's behavior under these conditions. The analysis is described only for positive AC, with the inductor current returning through the low-side MOSFETs in the low-frequency half-bridge. Similar operation happens for negative AC, when the PFC choke current returns through the high-side switches of the slow leg.

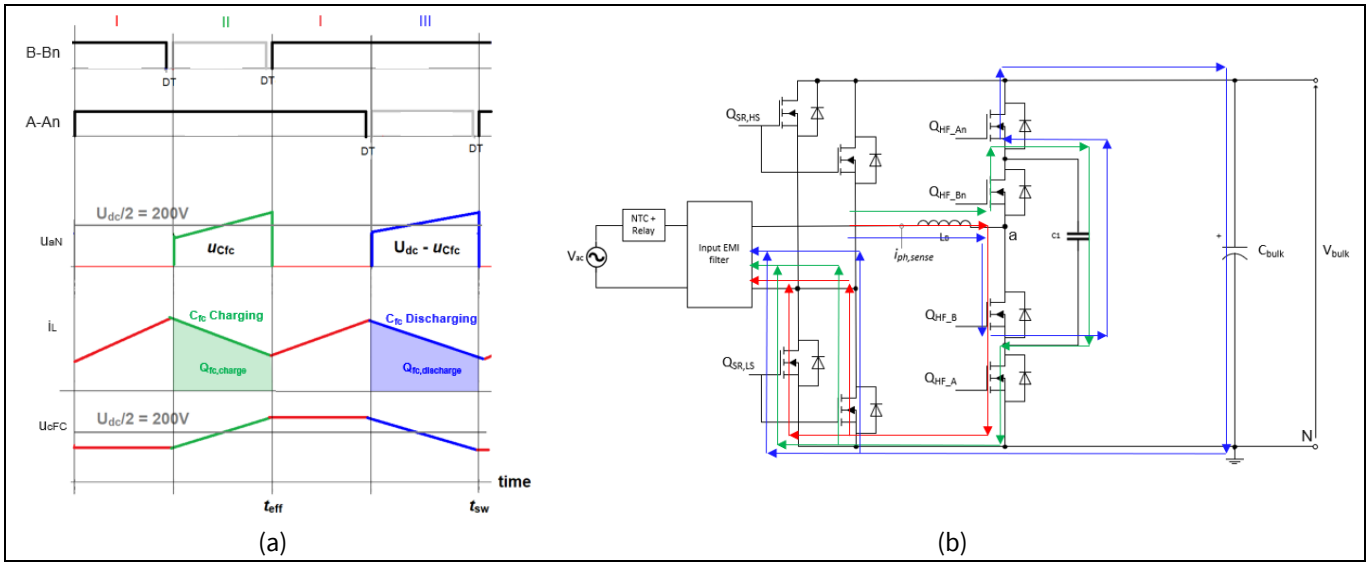


Figure 6 Involved current flow paths when the duty cycle is higher than 0.5

When the duty cycle is higher than 0.5, the converter operation can be divided into four distinct phases, as shown in Figure 6.

Each phase is characterized by a specific current flow path and switching configuration:

- **Phase I:** The inductor is charged, and the current i_L increases, following the path highlighted by the red arrows in plot b. The voltage across the flying capacitor remains constant, with both MOSFETs Q_A and Q_B closed
- **Phase II:** The flying capacitor begins to charge, dependent on the duty cycle and inductor current. MOSFET Q_A and Q_{Bn} are closed, and MOSFET Q_B and Q_{An} are open, as highlighted by the green arrows in plot b
- **Phase III:** The energy stored in the inductor is transferred to PFC converter output, resulting in a reduction in the voltage across the flying capacitor. The current flow path is highlighted by the blue arrows in plot b, with MOSFET Q_B and Q_{An} closed

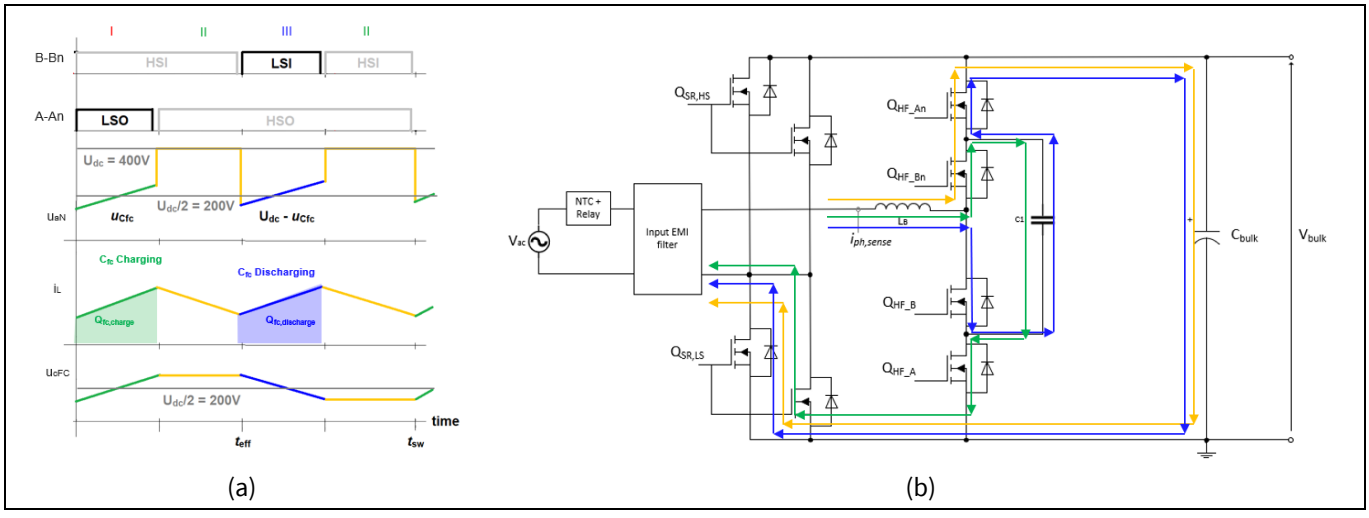


Figure 7 Involved current flow paths when the duty cycle is lower than 0.5

When the duty cycle is lower than 0.5, the converter operation can also be divided into four distinct phases, as shown in Figure 7.

Each phase is characterized by a unique current flow path and switching configuration:

- **Phase I:** The flying capacitor begins to charge, dependent on the duty cycle and inductor current. MOSFET Q_A and Q_{Bn} are closed, and MOSFET Q_B and Q_{An} are open, as highlighted by the green arrows in plot b
- **Phase II:** The inductor discharges, transferring power to the output, and the voltage across the flying capacitor remains constant. Both MOSFETs Q_{An} and Q_{Bn} are closed, and the current flow path is highlighted by the yellow arrows in plot b
- **Phase III:** The inductor is charged, and the current i_L increases, following the path highlighted by the red arrows in Plot b. Both MOSFETs Q_{An} and Q_B are closed, and the voltage across the flying capacitor remains constant

2.2 Active pre-charging solution for startup

The operation of flying capacitor (FC) multilevel converters relies on natural voltage balancing during steady-state conditions. However, at startup, the absence of PWM control prevents the FC from charging, resulting in uneven voltage distribution across semiconductor devices.

This issue is particularly critical for 400 V CoolSiC™-based designs in higher-voltage AC applications, where excessive voltage stress on outer devices can occur.

A significant challenge arises when the AC voltage is applied before PWM starts, as the FC charging path is blocked by stacked devices in the multilevel structure. This prevents the pre-charge of the flying capacitor, and if any pre-charge technique is applied, the outer devices must block the full AC peak voltage. In the worst-case scenario, this can result in a 422 V peak voltage for a 300 VRMS AC, posing a risk of overvoltage to 400 V-rated SiC devices.

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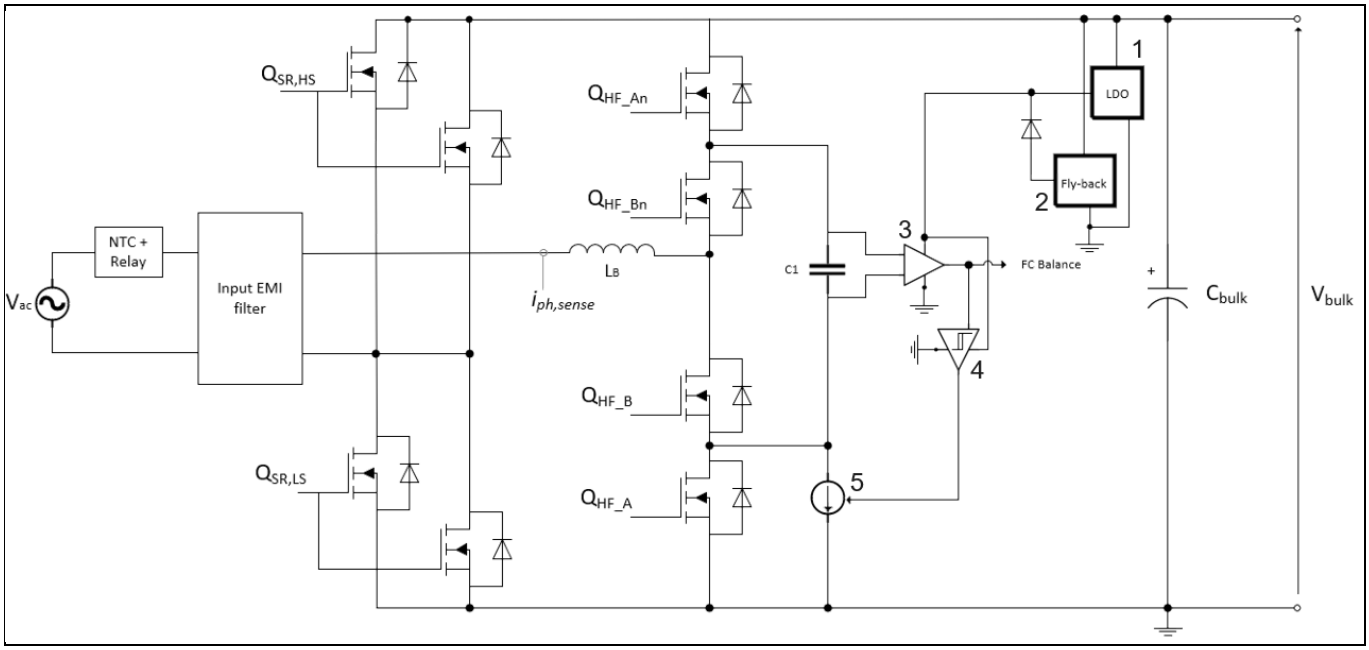

Figure 8 Simplified diagram of the removable current path added for FC charge during start-up and required circuitry

To address this issue, a controlled charging method is proposed, which implements a dedicated current source Figure 8 (marked in the figure as 5), Figure 9 (b) to pre-charge the flying capacitor to the target voltage, typically half of the DC-Link voltage when the AC is applied to the converter. Once the target voltage is achieved, the current source is automatically disabled.

A key feature of this solution is that it incorporates a hysteresis band (see **4** within Figure 8 and Figure 9 (c)), which maintains the flying capacitor voltage charged around the targeted voltage when the AC is connected but the PFC is inactive. This ensures the flying capacitor voltage is sustained without control intervention. The hysteresis control is achieved using the voltage sensing op-amp (see **3** and **4** within Figure 8 and Figure 9 (c)), which is also utilized for PFC control, thereby reusing existing circuitry.

To provide power to the flying capacitor voltage sensing op-amp, a low-dropout (LDO) (**1** within Figure 8 and Figure 9 (a)) regulator is implemented. The LDO supplies the op-amp from the beginning and is automatically disabled when the flyback (**2** within Figure 8) starts to operate.

The proposed circuit offers multiple benefits beyond the pre-charge sequence. It provides a continuous regulated voltage at the flying capacitor without control intervention – even when the converter is not enabled but plugged into the AC. The current path is disabled during steady-state operation. The implementation of the LDO makes the operation of the FC charge circuit independent from the bias converter.

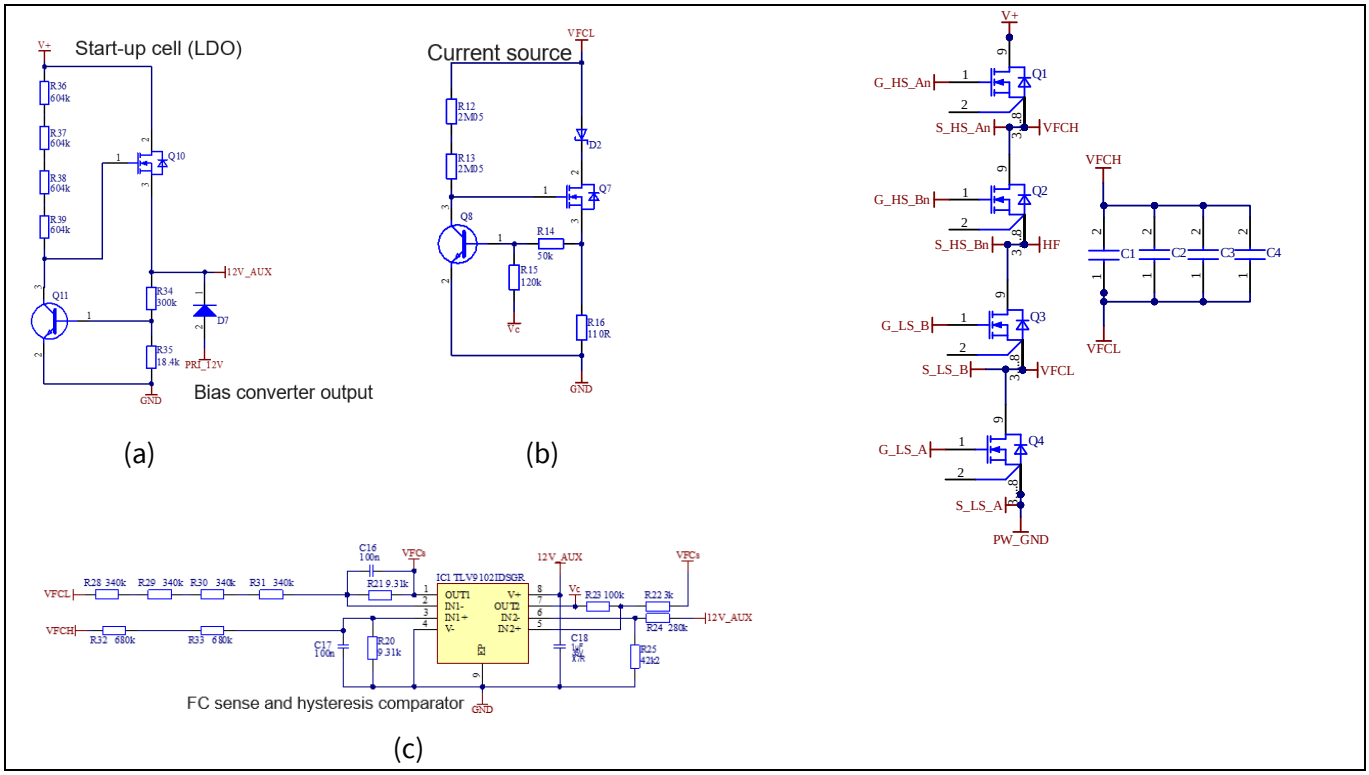

Figure 9 Active pre-charge circuit implementation

Figure 10 and Figure 11 show the complete startup sequence of the PSU – with a particular focus on the pre-charge circuit sequence. The startup process is divided into five distinct phases:

- **First phase (T0 to T1):** When the AC input is connected to the PSU. At this point, the current source provides an alternative path for pre-charging the flying capacitor, while the LDO regulator supplies power to the voltage sensing operational amplifier. As the flying capacitor reaches its target voltage, the comparator disables the current source at T1
- **Second phase (T0 to T2):** Represents the time required for the flyback converter to power on and provide the supply voltage to the full PSU. After this phase, the LDO is auto-disabled by the flyback
- **Third phase (T2 to T3):** The PFC control checks if the voltage of the flying capacitor is within the acceptable range, typically around half of the DC-link voltage
- **Fourth phase (T3 to T4):** Marks the beginning of the PFC operation. The voltage in the DC-link increases up to 400 V, and the flying capacitor voltage is auto-regulated to 200 V
- **Fifth phase (T4 to T5):** When the PFC is in range and sends a startup command to the LLC. This triggers the LLC startup sequence

Finally, at T5, The converter operates in a steady-state condition.

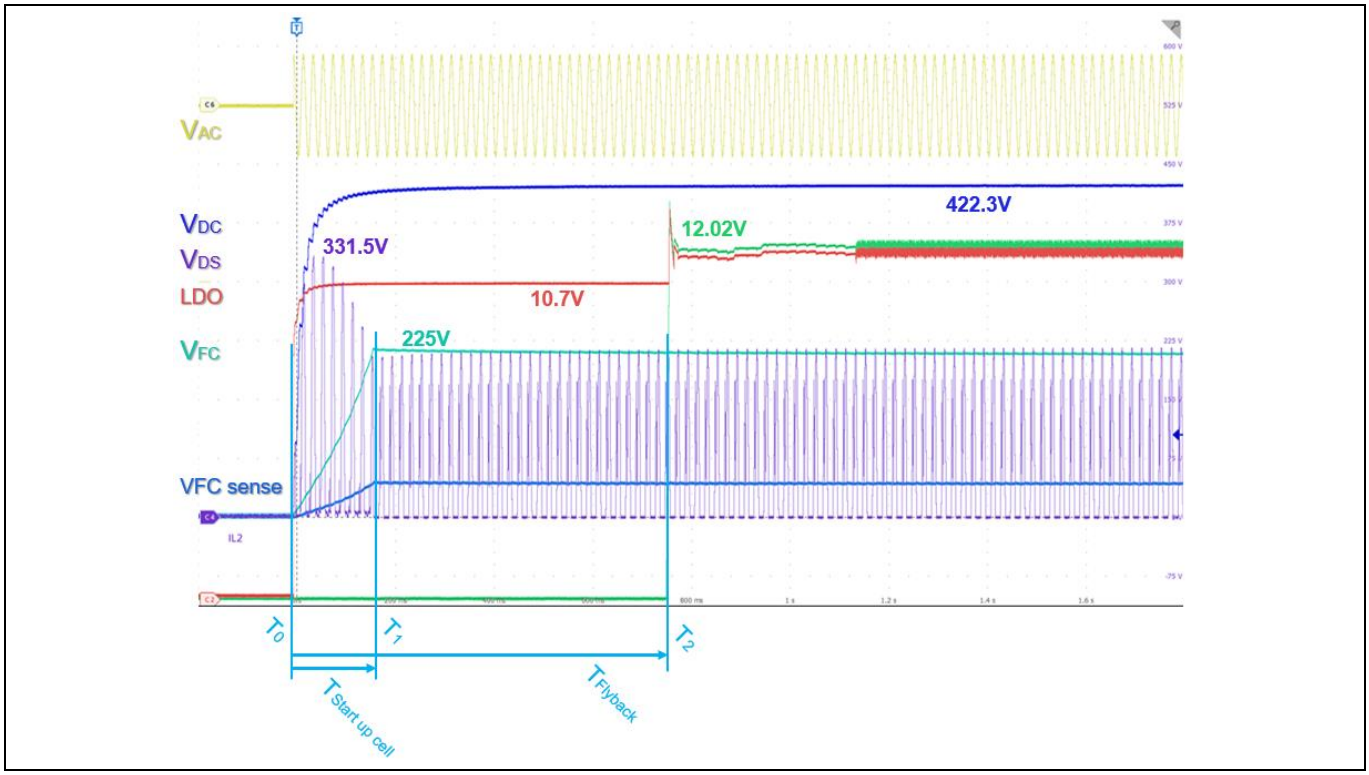

Figure 10 Pre-charge circuit and PSU startup

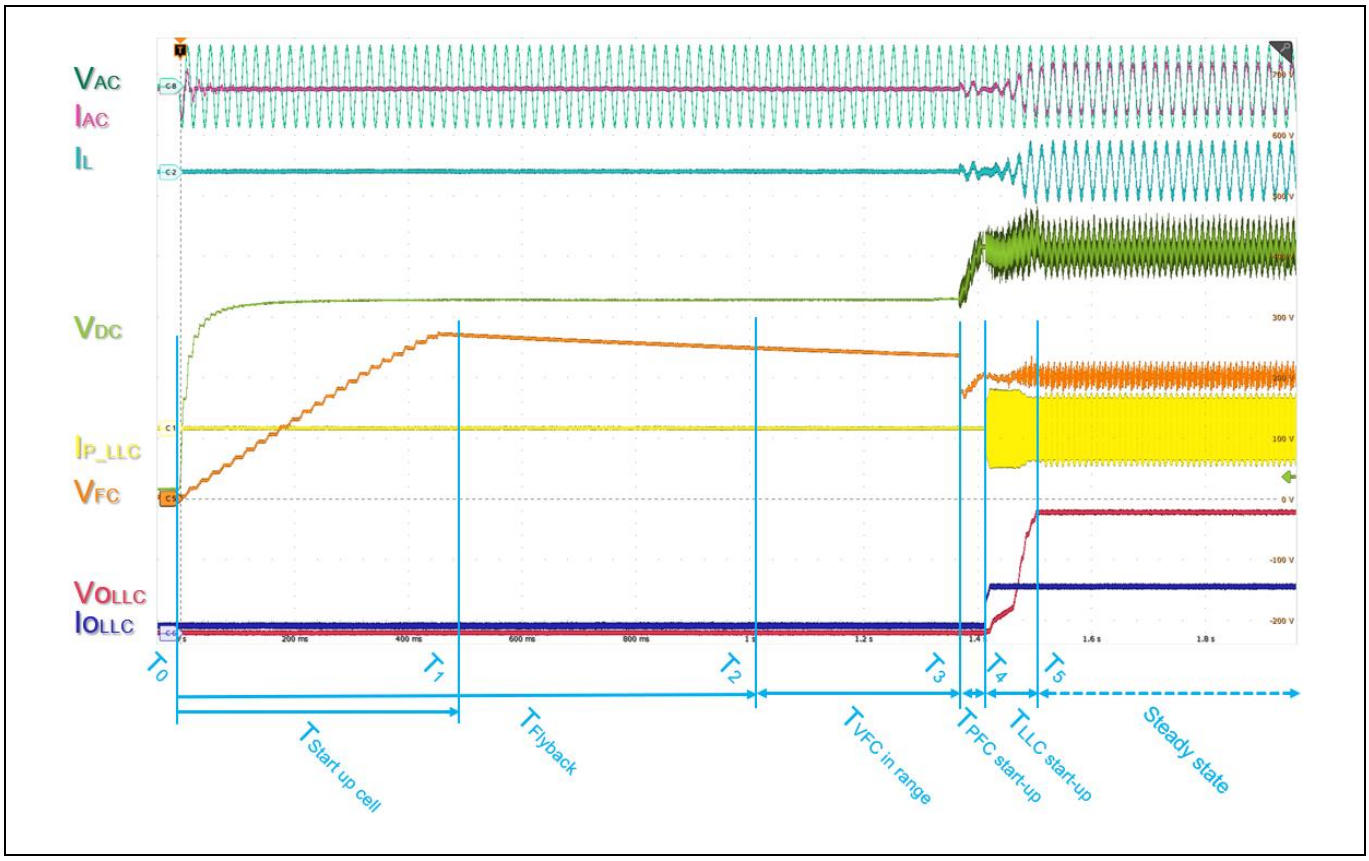

Figure 11 Pre-charge circuit and PSU startup

2.3 Signal conditioning for the digital control of 3LFC CCM PFC

The three-level PFC of REF_3K3W_3LFC_PSU implements CCM average current mode control with duty and load feed forward. Unlike the classic PFC where the AC voltage is rectified by the diode bridge, in the bridgeless totem-pole PFC converter, the inductor current is both positive and negative. In addition, isolation or common mode rejection is required to measure the inductor current if the control ground is placed in the negative rail of the bulk voltage, as is traditionally done in the classic PFC. A Hall-effect sensor is therefore a good solution for this kind of system.

The output of the Hall-effect sensor matches the ADC inputs when supplied with the same voltage – positive and negative currents are measured with the span of the ADC and a shift to half of the ADC range for zero current. The sensor has enough bandwidth to also sense the high-frequency ripple and therefore, the same signal can be used for peak current limitation and input OCP. In case of a lower bandwidth, the Hall-effect sensor typically offers an overcurrent detection signal, which can be used for the same purpose.

Regarding the bulk and LLC input voltage, they are sensed by the PFC controller via resistive partition as shown in blue in Figure 12. The AC sensing chain is shown in violet. It is split into positive and negative AC sensing with respect to ground and the two resulting signals are then summed in the analog domain. Lastly, the polarity of the AC input is obtained via comparator, shown in orange.

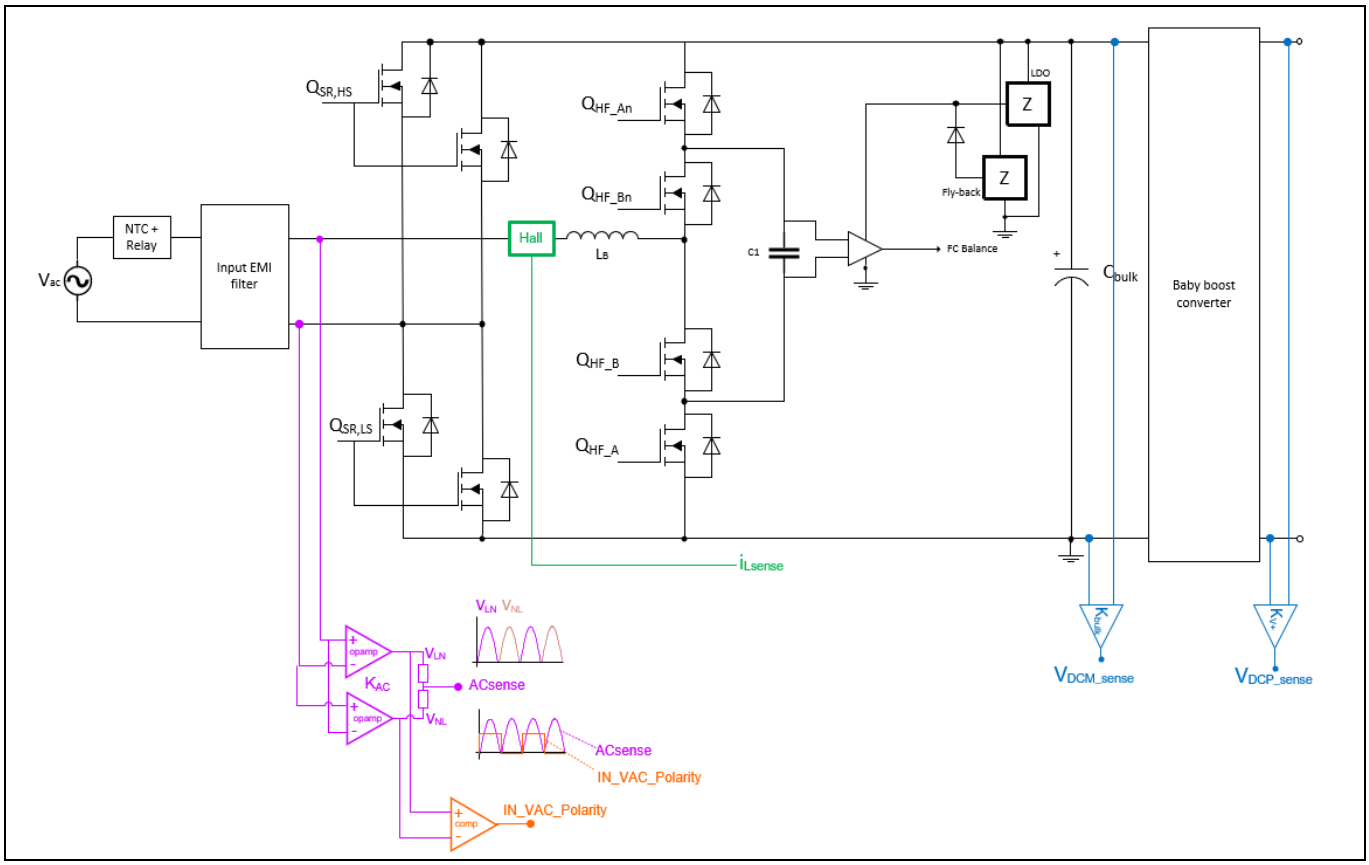

Figure 12 Sensing circuitry required to control the three-level PFC converter with XMC™

Since the AC voltage is used for the current reference generation in the selected average current mode structure, the current reference is a full-wave rectified sinusoidal sequence. However, the current sense after the ADC is a sinusoidal sequence with offset at half of the ADC span. Therefore, the ADC result from the current sense requires the offset to be removed before being rectified according to the AC polarity signal. These two steps, together with extra gain, are implemented by the XMC™ controller software.

Figure 13 shows the block diagram of the control implemented in the 3LFC PFC. Its main difference from a totem-pole control implementation is the addition of the flying capacitor balance block, as shown in blue within Figure 13.

The FC balancing is implemented to support the natural balancing of the 3LFC converter in case of possible asymmetry in the MOSFET-driving signals or dynamic conditions during operation.

A proportional controller modifies the duty cycle of one of the phase-shifted PWM, so the FC can be further charged or discharged according to the sensed error.

The control has been implemented using a XMC4200 MCU.

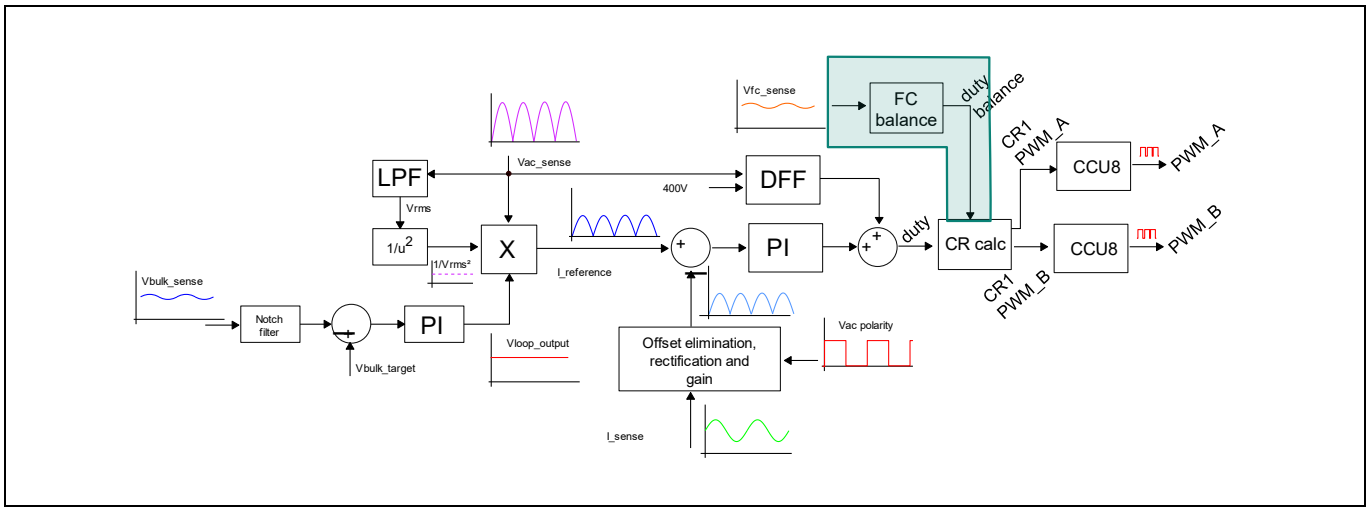

Figure 13 Current loop structure with duty-cycle feed-forward (DFF) and flying capacitor balancing control

2.4 Measured efficiency and loss distribution estimation

The performance of the PFC converter in REF_3K3W_3LFC_PSU has been measured without the backend DC-DC. Figure 14 presents the measured efficiency and losses of the flying capacitor AC-DC converter for different input voltages. For a nominal AC voltage (230 V), the AC-DC PFC stage is capable of near 99.2% peak efficiency at 45% of the rated load, which remains above 98.8% up to full load. A higher efficiency is obtained at 265 V input voltage, taking advantage of the lower current in the PFC converter. On the contrary, at the lowest voltage of the AC input range, the efficiency rapidly degrades with the load. Figure 14 also includes the measured losses for these efficiency points. The demonstrated measurements do not include fan consumption.

The input current performance is introduced in Figure 15. Total harmonic distortion of the input current remains under 10% for all the measured points with a THD under 3% for nominal input voltage and full load operation. The power factor is over 0.99 from 30% of the load and very close to the unity power factor for full load operation for the whole AC voltage range.

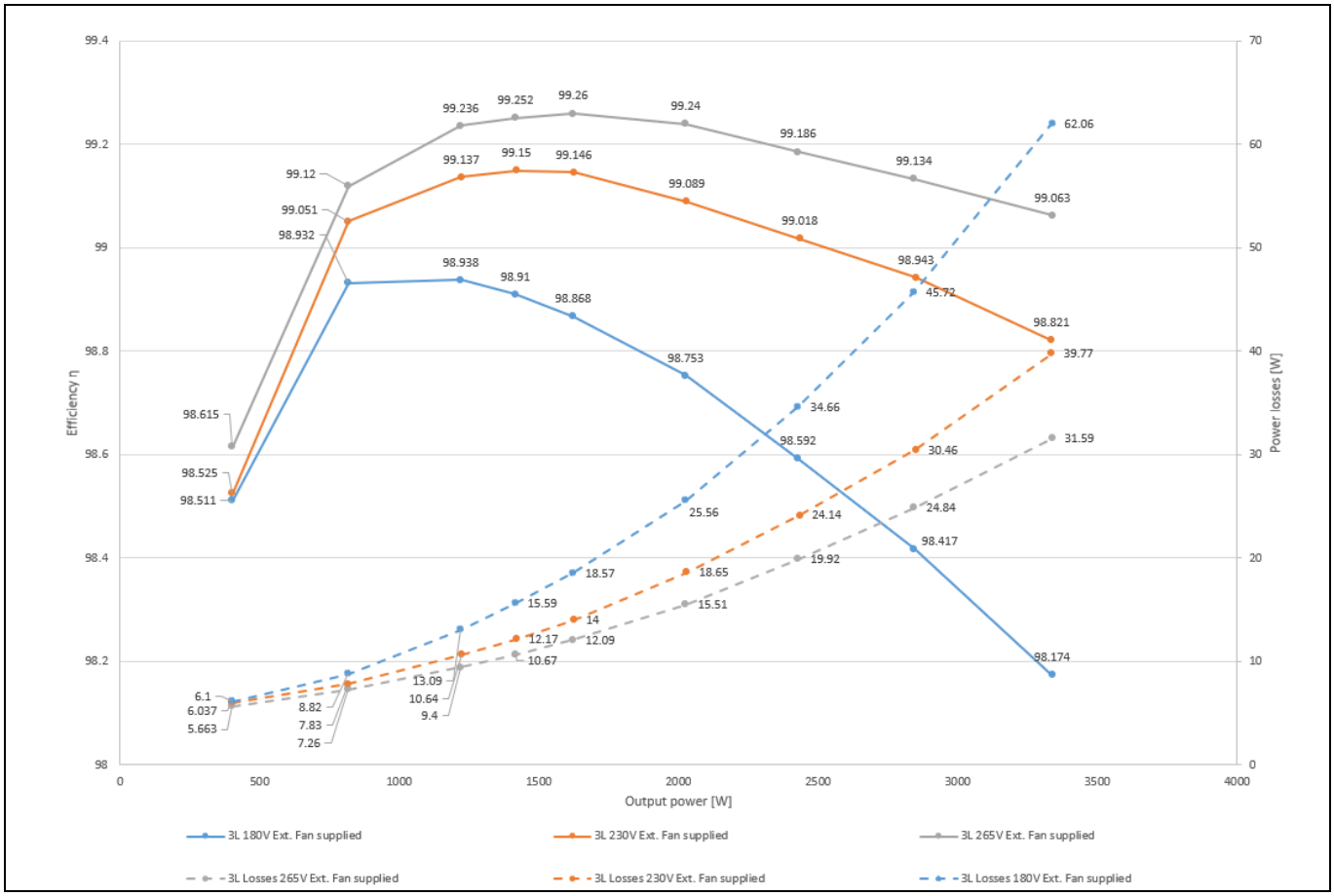

Figure 14 **Measured efficiency and power losses of the 3LFC PFC in REF_3K3W_3LFC_PSU excluding fan consumption**

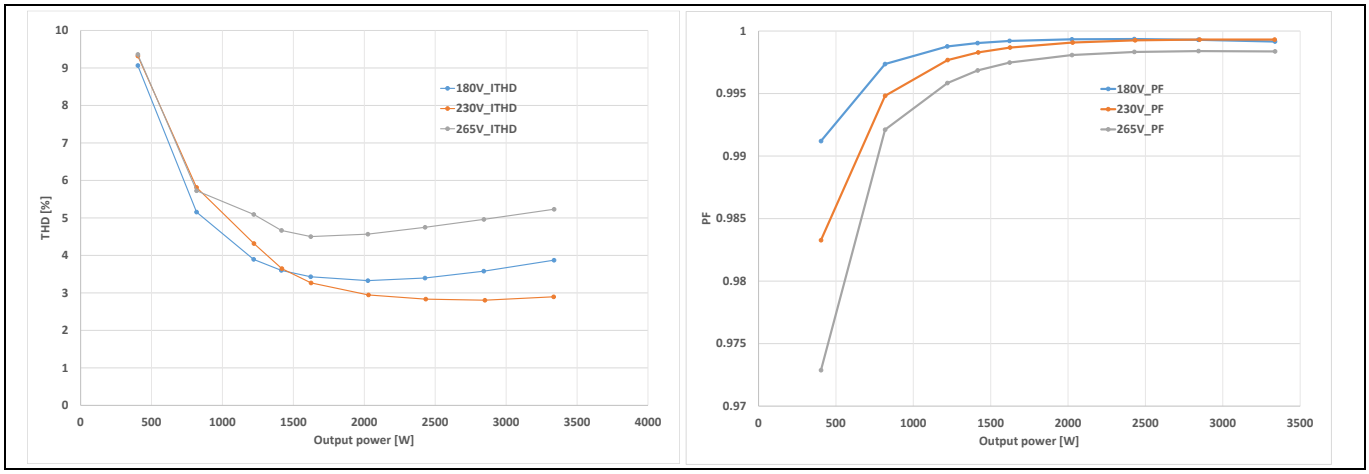

Figure 15 **Measured iTHD (left) and PF (right) for 230 V_{AC} and 180 V_{AC} line voltage, both at 50 Hz operation**

2.4.1 Loss distribution for 3LFC PFC

A loss estimation model has been tuned according to the efficiency measurements shown earlier. Figure 16 shows the results of the losses model. It demonstrates the excellent switching performance of CoolSiC™ 400 V devices, and how the conduction losses are dominant in the high-frequency stacked devices of the 3LFC PFC.

The volt-second reduction in the PFC choke, motivated by the doubling effect of the switching frequency and the switching node voltage reduction of the multilevel topology, reflects in the core losses and enables a lower inductance. Because of that, it is possible to reduce both the PFC choke size and turn number. Consequently, the winding diameter can be increased, which is visible in the copper losses on the PFC choke.

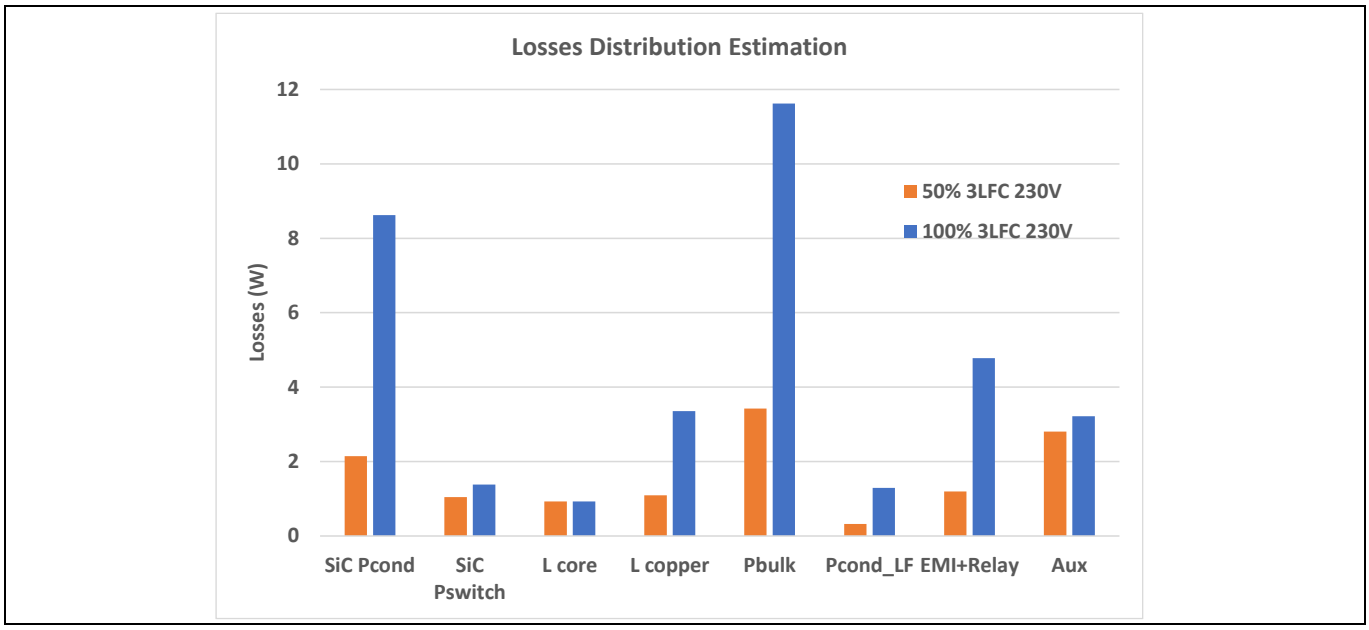

Figure 16 Estimated loss distribution for 230 V AC voltage, and 50% and 100% load operation of the 3LFC PFC in REF_3K3W_3LFC_PSU

2.4.2 Comparison with interleaved totem-pole PFC

This section compares the flying capacitor multilevel topology presented in this document, with the interleaved totem-pole PFC implemented in [10]. Both REF_3K3W_3LFC_PSU and REF_3K3W_HFHD_PSU have the same power rating and dimensions, which leads to the same power density. Both designs implement the same LLC converter and EMI filter, and the hold-up time extension circuit.

Two of the three main design aspects, including a high impact in power density, are common between the interleaved totem-pole and 3LFC compared in this section. On one hand, the required bulk capacitance (with or without hold-up time extension circuit) is the same if both converters are designed for the same hold-up request. On the other, since both achieve a doubling of the switching frequency and a ripple reduction of the input current, the EMI filter can be considered the same. Therefore, the comparison in this section focuses on the PFC choke volume and the achievable efficiency using CoolSiC™ 400 V devices.

The PF chokes for the interleaved configuration are rated at half of the input current. However, in a 3LFC PFC, the single PFC choke is rated at the full input current. Despite that, the much lower inductance required due to the four times volt-second reduction of the 3LFC enables a PFC choke volume reduction of up to 60% compared to the interleaved totem-pole.

The PFC choke design of both reference designs are given in Table 1. The PFC choke volume reduction might not have a significant impact on the total volume of the PSU, but it offers the possibility of a mechanical optimization for a better cooling or improved airflow within the PSU.

Table 1 PFC choke design comparison between interleaved totem-pole and 3LFC PFC

	Number	Core	Turns	Inductance@0A
Interleaved Totem-pole	2	CH270060GT14	64	384 µH
3LFC	1	CH270060GT	42	131 µH

Moreover, this PFC choke volume reduction comes together with increased performance of the converter. This combination makes this topology very attractive for applications where performance and power density are key requirements. Figure 17 shows the comparison between the measured efficiency of the PFC converter of REF_3K3W_3LFC_PSU and REF_3K3W_3LFC_PSU. The interleaved design implements 57 mΩ CoolSiC™ 650 V devices, while the 3LFC mounts 25 mΩ CoolSiC™ 400 V devices. The increased peak efficiency at nominal input voltage (230 V) is 0.3%, with a considerably higher improvement at light load. For full load operation, the efficiencies of both options are similar.

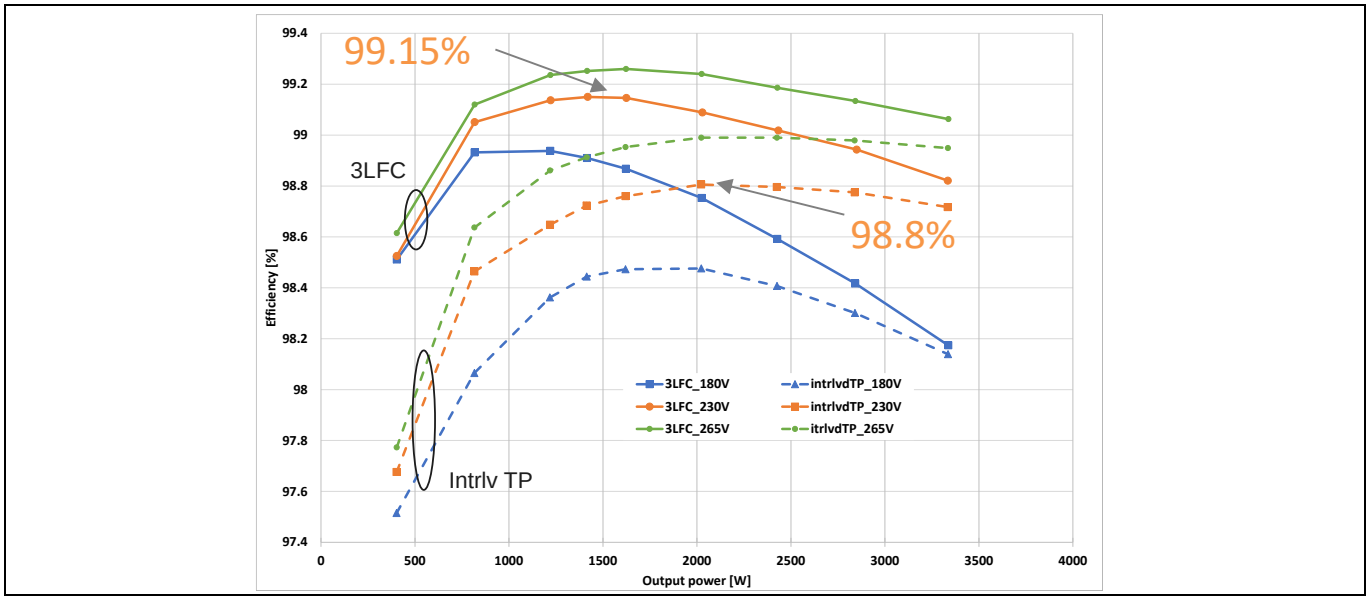

Figure 17 Measured efficiency comparison between 3LFC and interleaved totem-pole PFC [10]

Figure 18 shows a loss estimation comparison of both solutions for the semiconductors and PFC chokes. The other losses included in Figure 16 are not compared since they are common for both implementations.

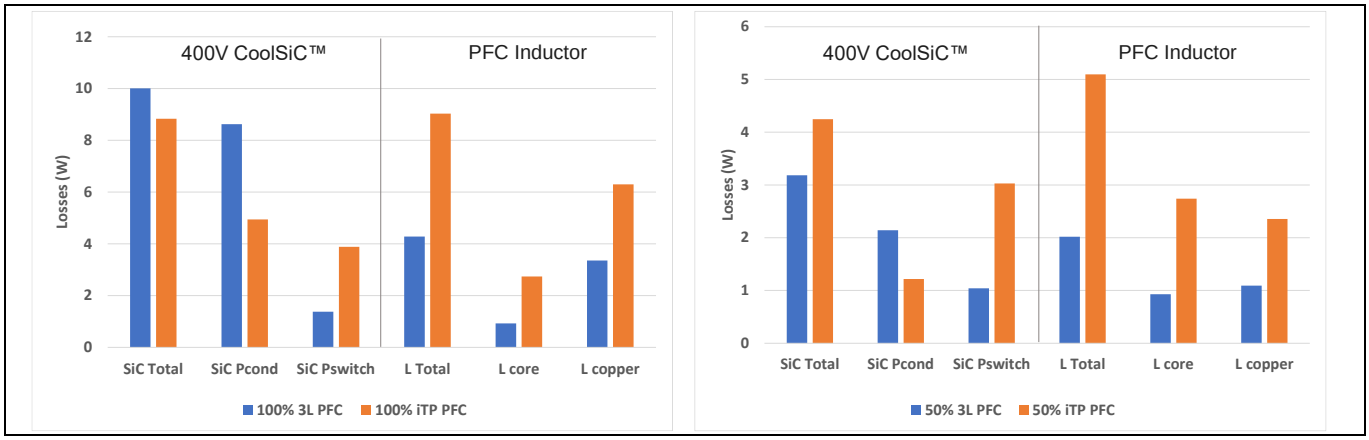

Figure 18 Power loss breakdown comparison between 57 mΩ ITTP PFC (orange) and 25 mΩ 3LFC PFC (blue) for 100% (left) and 50% (right) load

Regarding the high-frequency semiconductors, the total losses are clearly lower in the multilevel approach at 50% load condition due to lower switching losses, thanks to the lower voltage to be switched and better figure of merit of CoolSiC™ 400 V devices. At full load, the losses in CoolSiC™ devices of both designs are quite similar, with slightly higher losses for the three-level design due to increased conduction losses, for the multilevel topology. The inductor losses are reduced in 3LFC due to the volt-second reduction (improved core losses), and the thicker wire enabled by the turn number reduction (reduced winding losses), as mentioned above.

2.5 Driving CoolSiC™ and CoolMOS™ in the 3LFC PFC

In a totem-pole PFC, the bootstrapping technique is typically implemented – but the behavior of this technique is unknown to this topology. Therefore, an isolated supply is designed for the drivers of the four stacked devices because the CoolSiC™ MOSFETs are sensitive to gate voltage supply. Hence, reducing the recommended voltage leads to a channel-resistance increase.

Using the proposed isolated supply circuit shown in Figure 19 guarantees a reliable and stable supply for the drivers in all the conditions, including abnormal AC conditions or dynamic operation.

The isolated supply is based on an oscillator driving a PCB-integrated transformer, as shown in Figure 19. The presented circuit generates four isolated 18 V outputs from the 12 V supply provided by the bias converter. The transformer implements four turns for each winding in a six-layered PCB and an inexpensive ER14.5/6 ferrite core.

Figure 21 shows how the isolated bias supply is implemented with the PFC power card (PW100001389) along with the 400 V SiC devices in TOLL package and the ceramic flying capacitors.

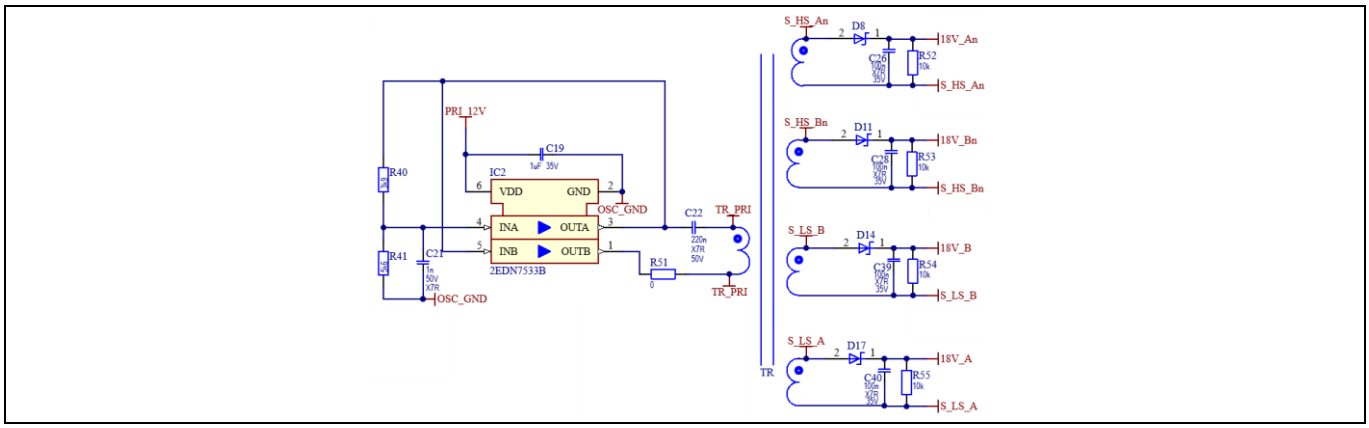

Figure 19 Driving CoolSiC™ with EiceDriver™ 1EDB8275F

The driving of the CoolMOS™ MOSFET for low-frequency half-bridge in the bridgeless PFC is shown in Figure 20. A hybrid driving approach with an isolated high-side and non-isolated low-side drivers has been adopted [8]. Also, a bootstrap approach has been adopted to minimize costs. In this case, proper capacitor dimensioning is required to avoid discharging and breaching the UVLO threshold of the driver.

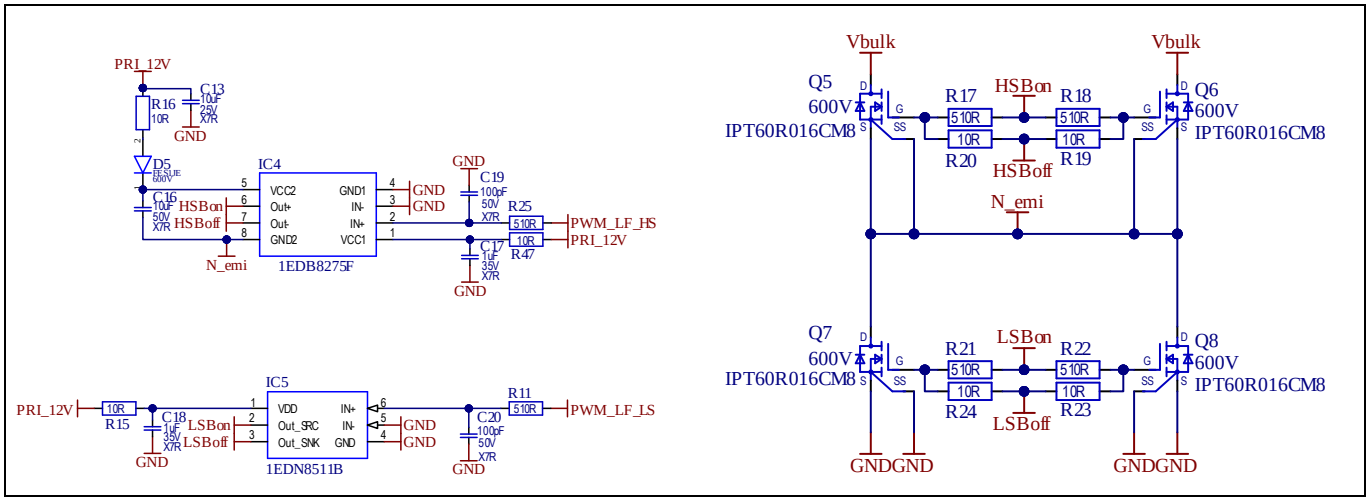

Figure 20 Driving CoolMOS™ with hybrid driving: EiceDriver™ 1EDB8275F along with 1EDN8511B

2.6 Hardware implementation

The hardware implementation of the PFC is distributed among the PFC power card (PW100001389) hosting the high-frequency MOSFETs, the LLC power card (PW200001388) hosting the synchronous rectification stage and the main board hosting the PFC inductor, input line filter, and NTC. Figure 21 shows the top view of the power daughter cards and their location. The PFC power card implements not only the multilevel PFC, but also the previously presented driving supply and FC pre-charging circuit.

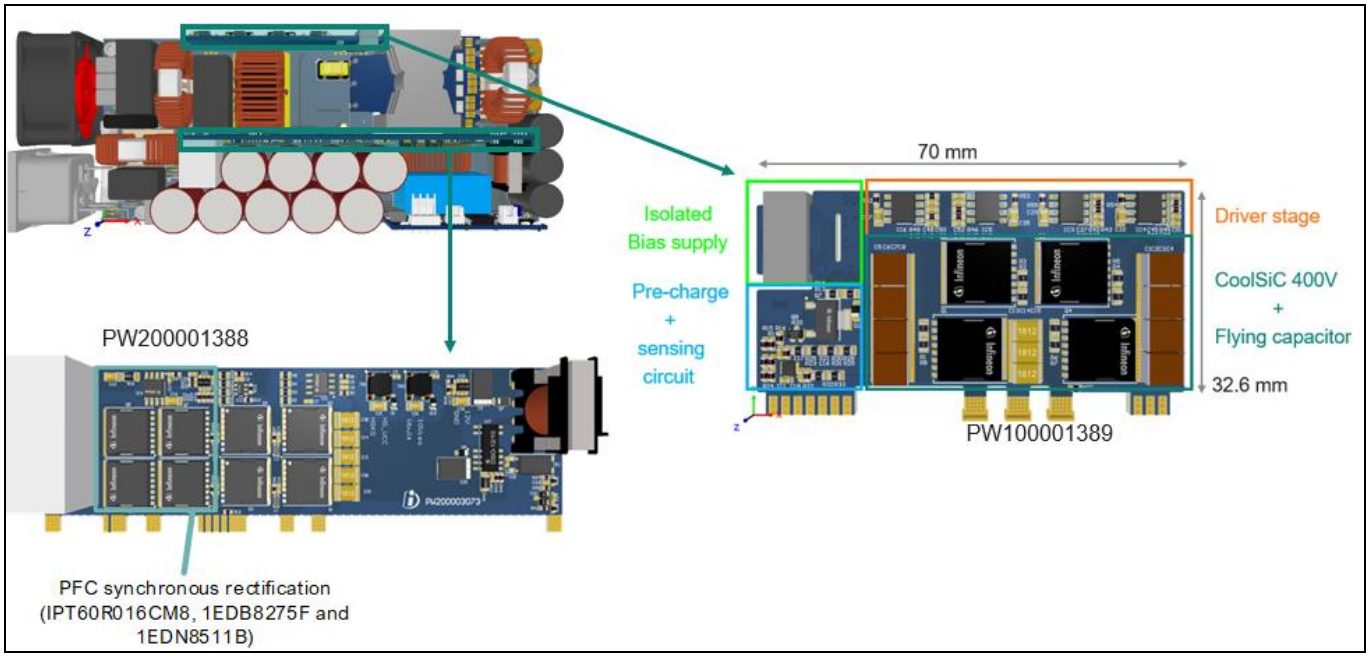

Figure 21 Hardware implementation of the interleaved totem-pole PFC

2.7 Baby-boost stage to extend hold-up time

To have a significant improvement in the power density, a viable and accepted approach is to implement a reduction of the bulk capacitance. Indeed, under steady-state conditions, the converter can operate with a lower bulk capacitance – provided that the 100 Hz ripple of the bulk voltage remains below the maximum

voltage rating of the components, the maximum RMS current can still be handled by the remaining bulk capacitors and the converter still meets the requirements in terms of load transients.

Overall, two criteria need to be satisfied:

The total PFC output AC current stress must be lower than the maximum RMS current the capacitor bank can handle and the capacitance value must be high enough to:

- Prevent the bulk voltage to exceed the voltage rating (usually capacitors limit the voltage stress)
- Enable the PFC stage to operate with the required power factor and total harmonic distortion (that is, the minimum steady-state bulk voltage coming too close to the V_{AC} peak at the input)
- Supply the LLC converter for 10 ms at full output power (3.3 kW) during the AC line dropout (ACLCDO)

In a standard server power supply with 3.3 kW maximum nominal output power, assuming the average bulk volta ($V_{bus,nom}$) is 410 V_{DC} and the minimum bulk voltage ($V_{bus,min}$) is 395 V_{DC} during steady-state operation at full load, and the minimum bulk voltage during LCDO ($V_{bus,LCDOmin}$) is 360 V_{DC} (as shown in Figure 22) the minimum capacitance required to achieve the 10 ms hold-up time is:

$$\frac{2\,P_{out,max}\,t_{HUP}}{[V_{bus,min}^2 - V_{bus,LCDOmin}^2]}$$

Equation 1

which results in around 2.5 mF total capacitance.

For REF_3K3W_3LFC_PSU, by allowing the $V_{bus,LDCOmin}$ to go to a voltage as low as 290 V_{DC}, the amount of capacitance required to continue providing full-load current is in the 900 µF range, which is far lower than the 2.5 mF estimated above, enabling higher power density.

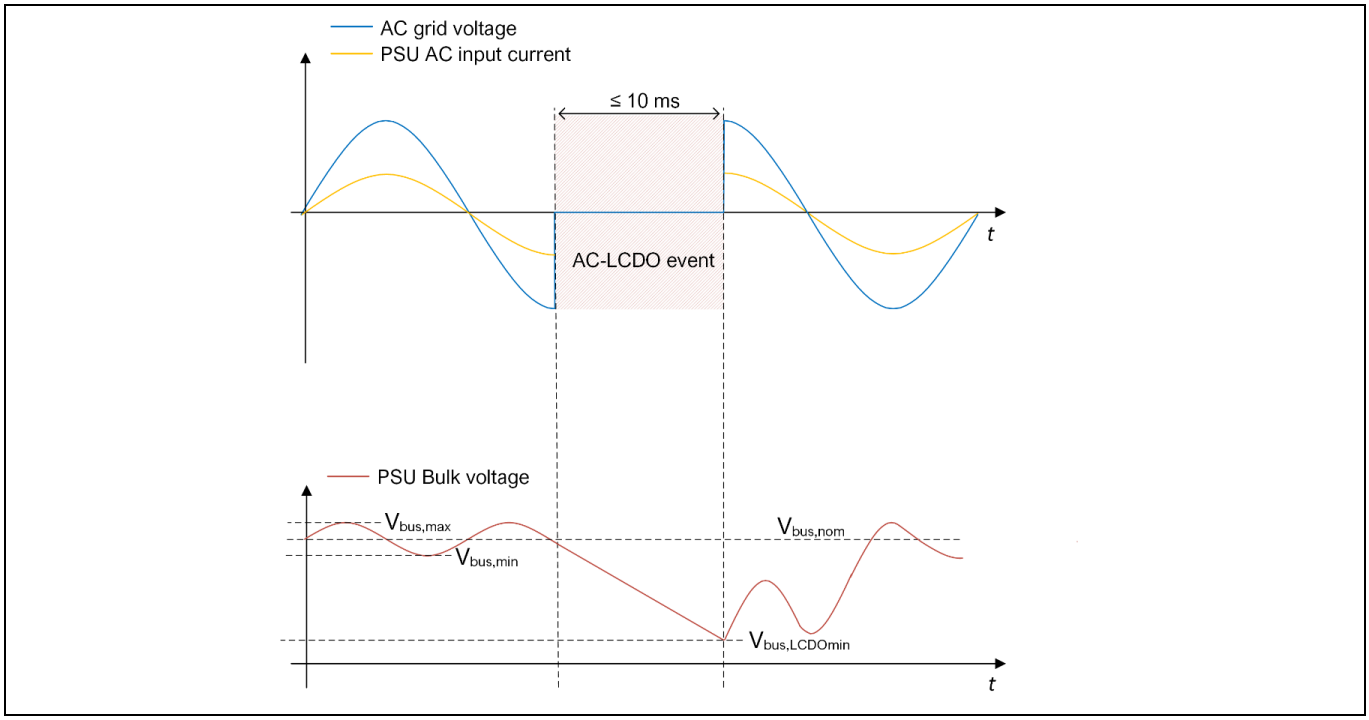

Figure 22 Simplified waveforms of the AC voltage, AC current and bulk voltage during a 10 ms LCDO event

Figure 23 shows an excerpt of schematic of the baby-boost converter implemented in REF_3K3W_3LFC_PSU, where V_{bulk} is the bulk voltage (input of the baby-boost converter), and V+ is the input voltage of the LLC DC-DC backend stage (output of the baby-boost converter).

During an ACLDO event, the static switch Q3 disconnects the V+ and the V_{bulk} rails, and as soon as an undervoltage is detected along with the absence of grid voltage, the baby-boost starts operating to bring the V+ voltage back to the nominal value allowing a deeper discharge of the bulk cap voltage.

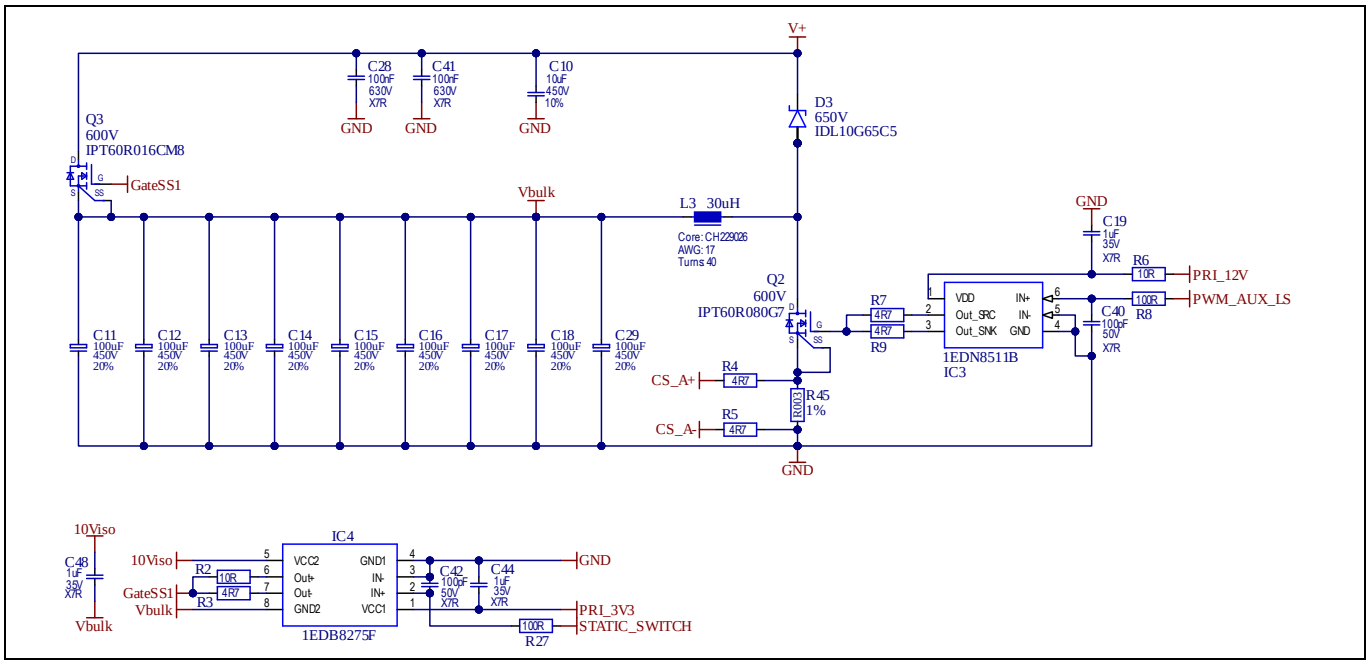

Figure 23 Schematic of the baby-boost circuity on the main board to comply with ACLDO specs

3 Half-bridge LLC converter

As a backend DC-DC converter, a half-bridge LLC topology with full-bridge rectification has been selected. This conversion stage provides safety isolation and regulates the output from the 400 V bulk voltage. A simplified schematic of the chosen topology is given in Figure 24.

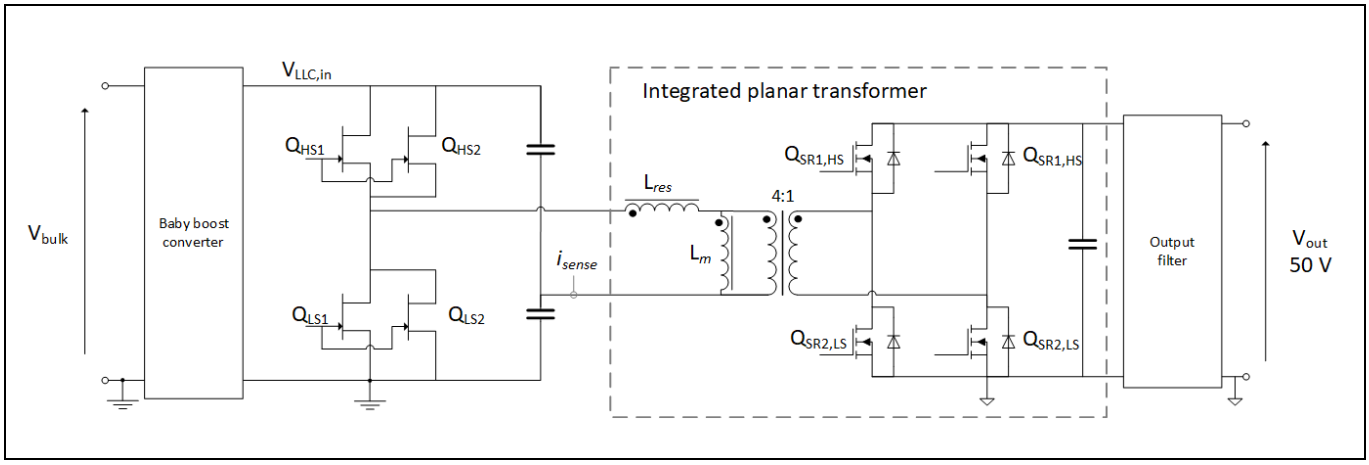

Figure 24 Simplified schematic of the LLC HB DC-DC converter in REF_3K3W_3LFC_PSU

3.1 Hardware implementation

The LLC DC-DC converter primary is placed on the LLC power card Figure 25, which drives the integrated transformer that integrates the secondary-side synchronous rectifiers. The primary side half-bridge is implemented in the LLC power card (PW200001388), which also holds the low-frequency half-bridge of the PFC and the bias converter.

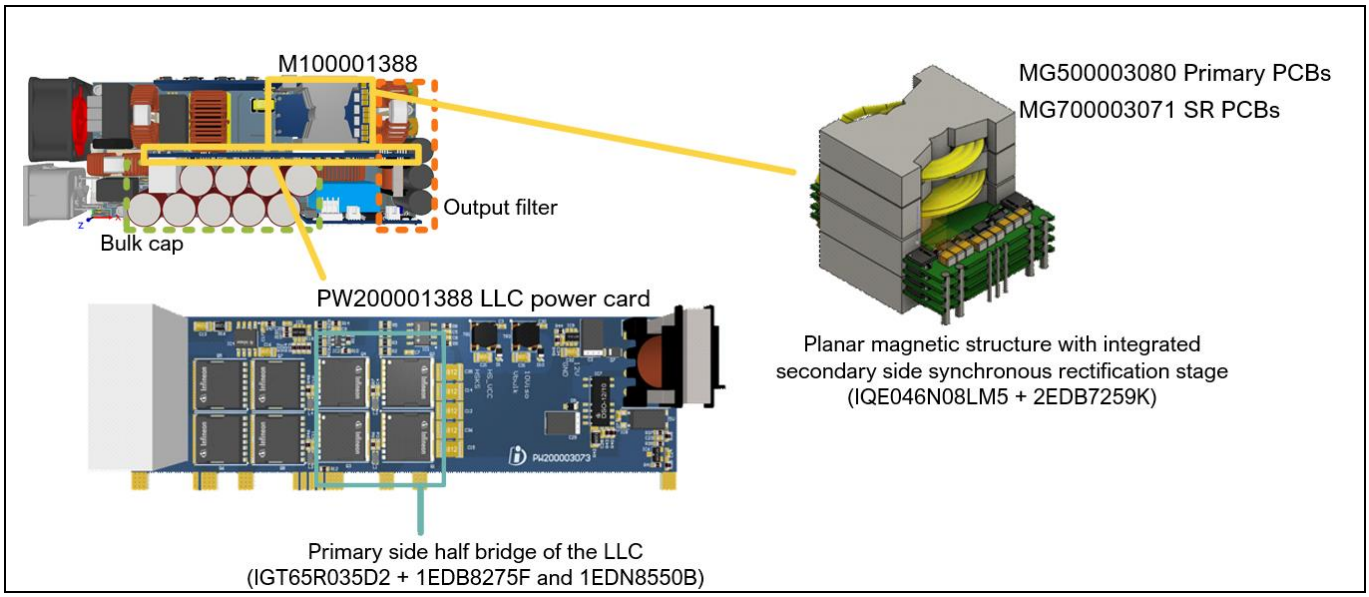

Figure 25 Primary and secondary sides of the LLC converter

3.2 Efficiency and losses

The measured efficiency of the half-bridge LLC converter is plotted for 400 VDC nominal input voltage in Figure 26. Efficiency is near 98.5% at 50% of the rated load and remains around 98 percent at full load.

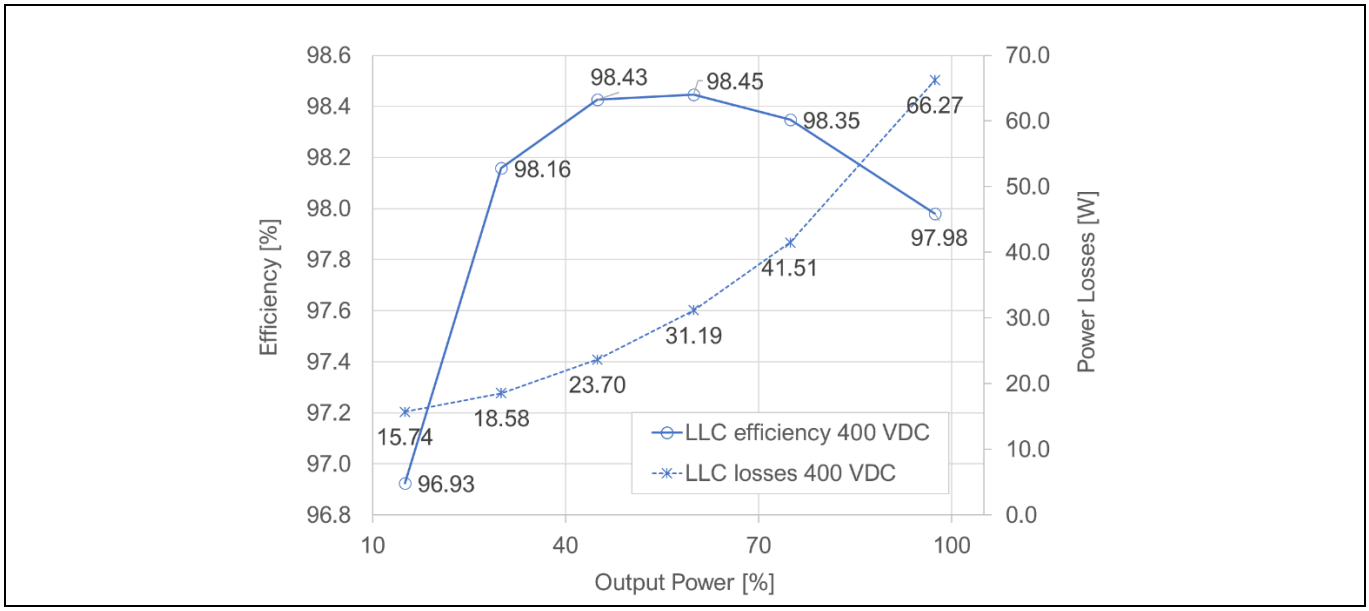

Figure 26 Efficiency of the LLC DC-DC stage with a CoolGaN™ device having a 35 mΩ on-resistance

Figure 27 shows an estimated power losses breakdown for only the LLC converter. The main contributors to power losses are conduction losses of the primary side, the synchronous rectifiers, total copper losses of the series and parallel inductance, and the main transformer itself.

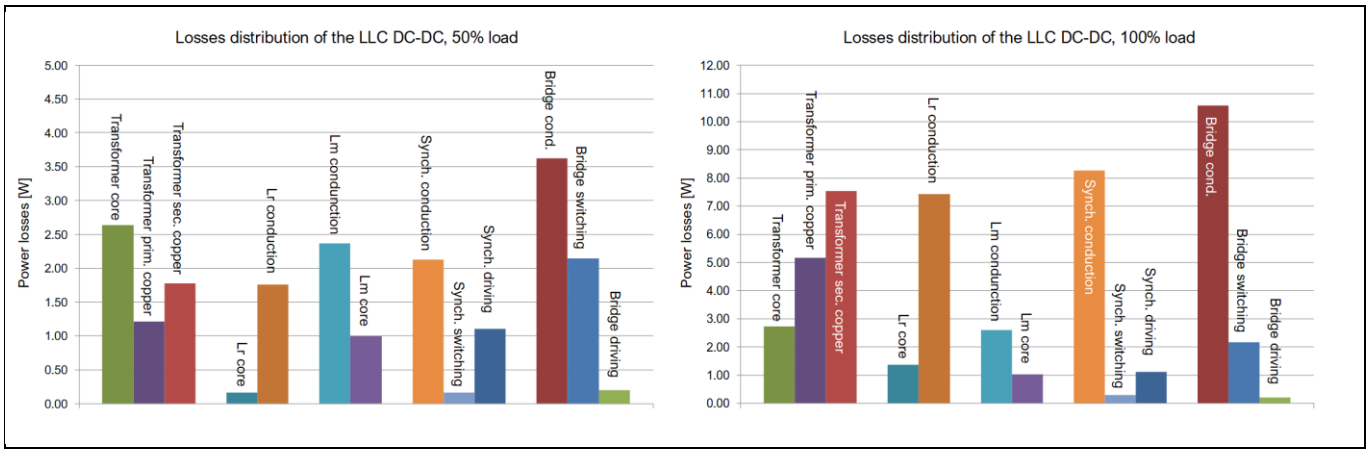

Figure 27 Power loss breakdown for the LLC DC-DC stage with a CoolGaN™ device with a 35 mΩ on-resistance

3.3 Integrated LLC half-bridge magnetics and SR

One advantage of the LLC topology is reusing the leakage inductance of the main transformer as the resonant inductance of the tank and the magnetizing inductance of the transformer as a parallel resonant inductor. However, this compromises the overall efficiency and therefore, the REF_3K3W_3LFC_PSU design has series and parallel inductors integrated in the main transformer structure to minimize space. Figure 28 shows the cross section of the transformer structure.

It is important to mention that the magnetic structure presented in Figure 28 is key to this design achieving the target efficiency of 98.5 percent (LLC only), integration of the synchronous rectification stage, and the required power density.

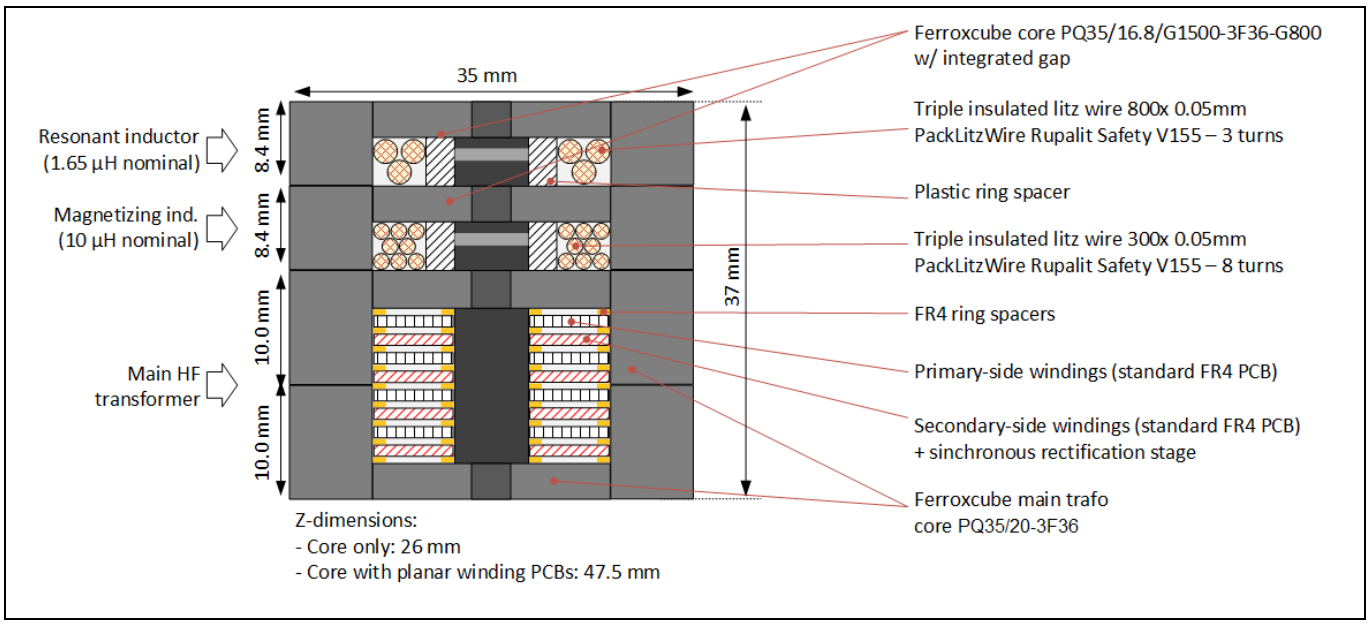

Figure 28 Integrated planar transformer assembly – cross section

The overall size of the full magnetic structure, including series and parallel inductors of the LLC converter, is 35 mm × 37 mm × 47.5 mm. The magnetic structure adopts two PQ35/20-3F36 cores from Ferroxcube for the main transformer, and two PQ35/16.8/G1500-3F36-G800 cores with integrated gaps from Ferroxcube for the resonant series inductor and the parallel inductor of the LLC converter. The 8:2 main transformer stack uses four primary and four secondary PCBs, as shown in Figure 29, with full interleaving to reduce high-frequency copper losses.

Inbetween each PCB couple, an FR4 spacer is also inserted to increase the air gap between the windings. This consequently reduces the interwinding capacitance for each interleaving layer and keeps it constant. It has been measured that the ring spacers between PCBs decrease the interwinding capacitance from about 140 pF with no spacers to about 60 pF with FR4 spacers.

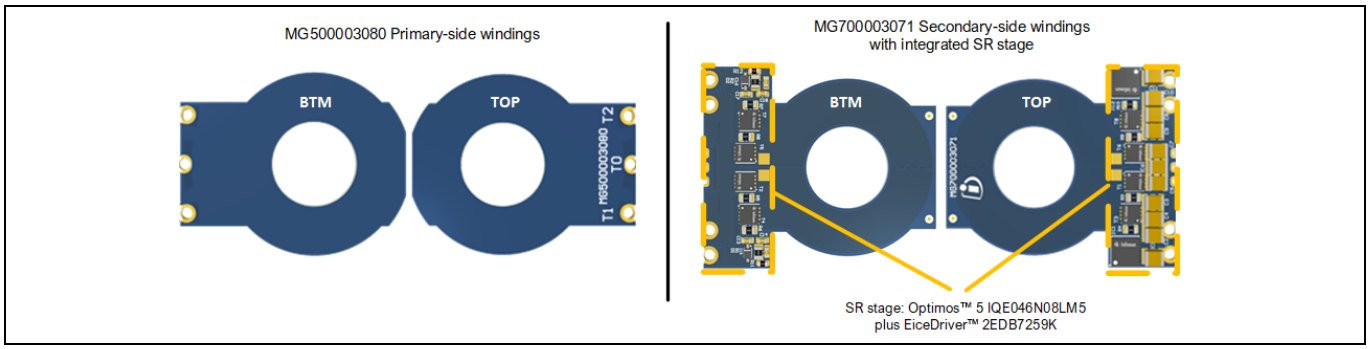

Figure 29 Primary- and secondary-side winding PCBs of the transformer

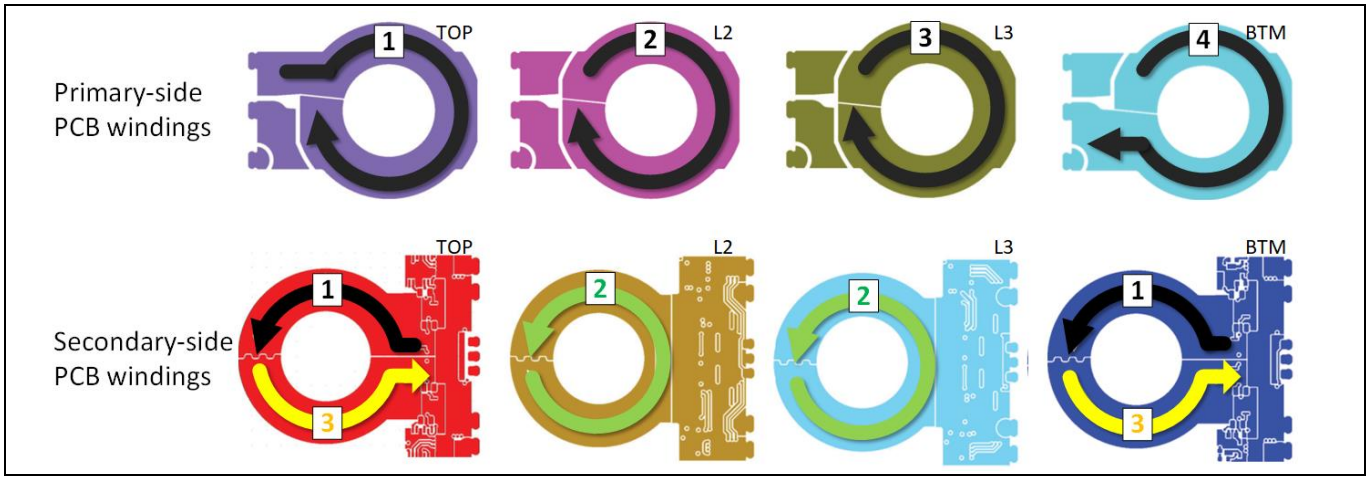

Figure 30 Planar winding arrangement in the main transformer

As mentioned, both the series and parallel inductors use cores with distributed gaps to reduce losses caused by stray magnetic fields. Litz wires are employed to reduce AC resistance and high-frequency copper losses. The series resonant inductor uses three turns of 800 strand 0.05 mm triple-insulated wire, and the parallel inductor uses eight turns of 300 strand 0.05 mm, both Rupalit Safety V155 from PackLitzWire. This results in the overall height of the full magnetic structure being only 37 mm, enabling it to fit in the 40 mm 1U maximum height limit according to the standards.

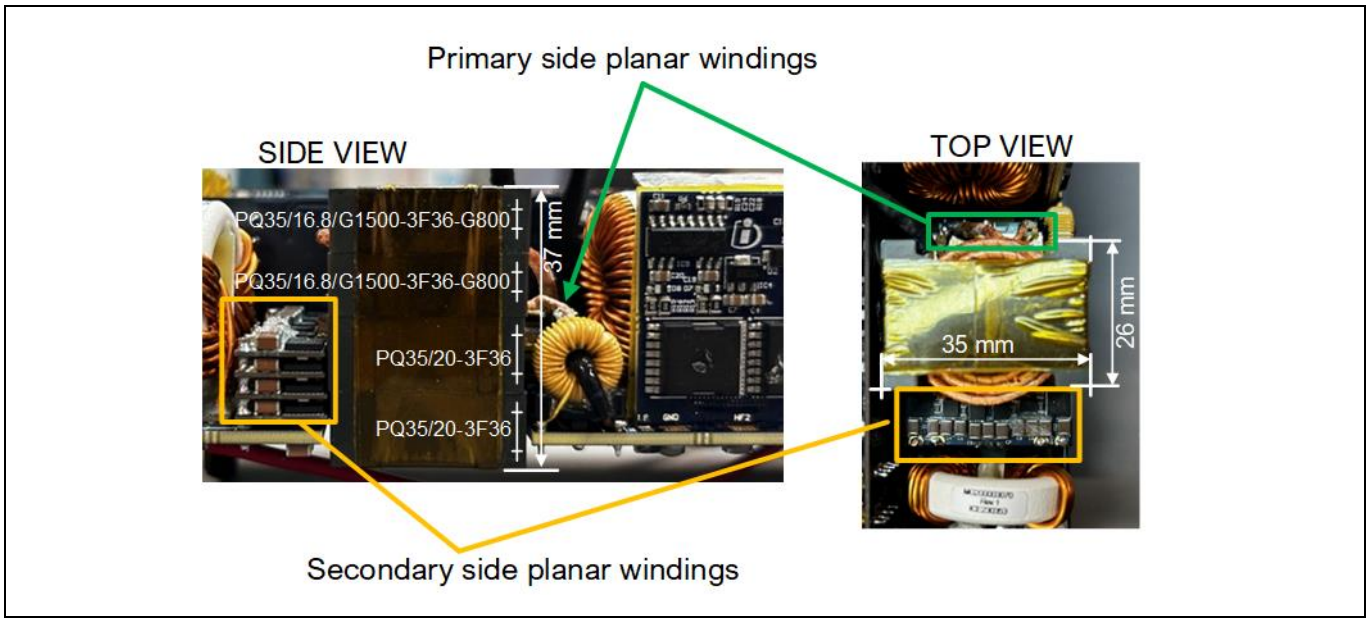

Figure 31 Integrated planar transformer assembly – picture of an assembled prototype

3.4 Driving CoolGaN™ and OptiMOS™ in the LLC converter

The primary-side of the LLC converter uses four CoolGaN™ power transistors, each having a 35 mΩ on-resistance in a TOLL package (CoolGaN™ IGT65R035D2), with both high and low sides having two devices in parallel. To drive the CoolGaN™ devices efficiently while paralleling, a common mode (CM) choke is suggested in series with the gate loop in order to increase CM impedance without affecting the differential mode (DM) impedances, which could affect the driving loop. For this purpose, four CM chokes from Bourns (SRF2012-361YA) have been used, as shown in Figure 32. See References [6] for further information about GaN paralleling.

The GaN half-bridge primary leg of the LLC does not require isolation since it is already implemented with ISOFACE™ digital isolators Figure 32. Hence, hybrid driving is employed to ensure high CMTI, flexible placement, and a lower overall impedance due to gate loop optimization. For further information on hybrid driving for CoolGaN™, see References ([7]-[9]).

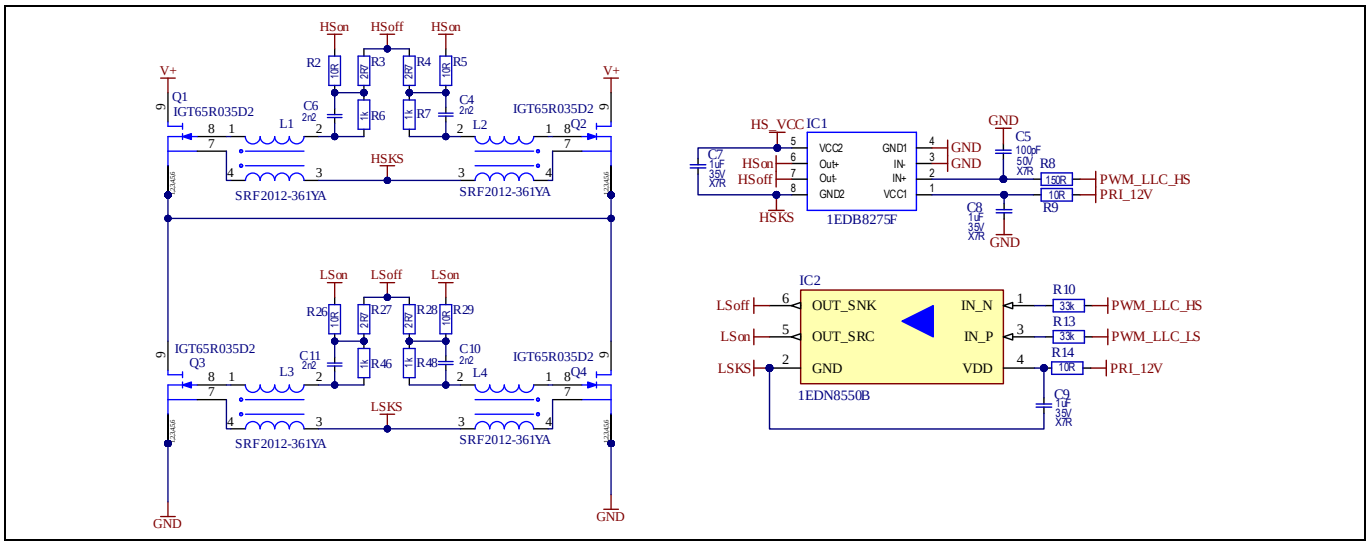

Figure 32 Driving CoolGaN™ with hybrid driving (EiceDriver™ 1EDB8275F with 1EDN8550B)

For the bias supply of the OptiMOS™ MOSFETs on the secondary-side, a bootstrapped solution with a 5 V_{DC} bias is used, as shown in Figure 33. Due to space constraints, EiceDriver™ 2EDB7275K in a 5 mm × 5 mm package is used, which precisely fits the small space available on the secondary board stacked in the transformer structure (see Figure 28).

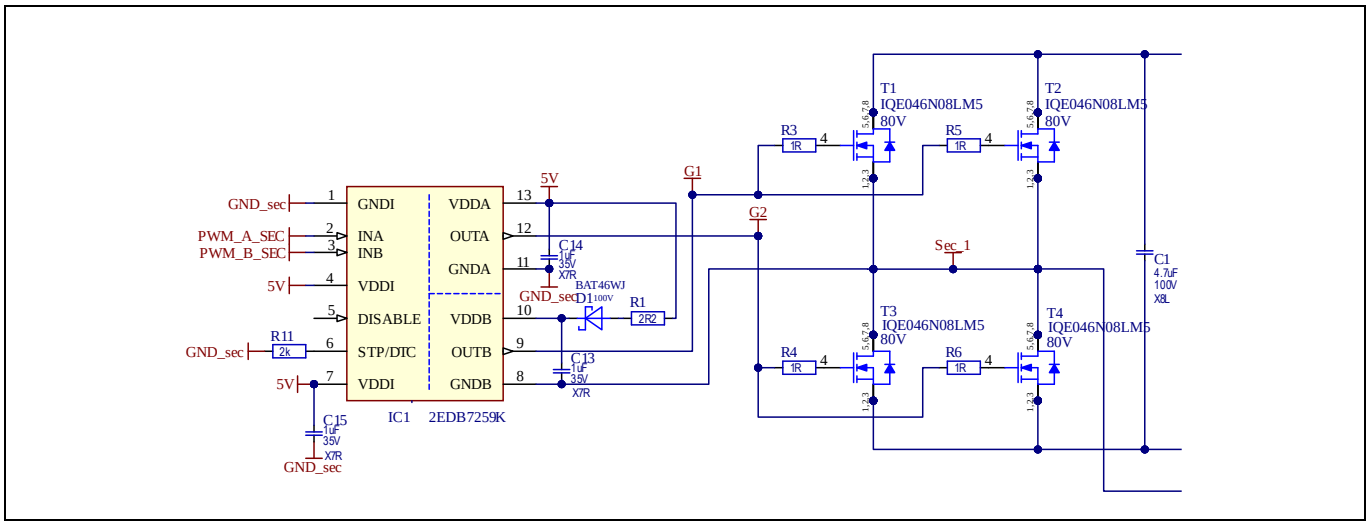

Figure 33 Driving OptiMOS™ with EiceDriver™ 2EDB7259K

4 Experimental results

4.1 Power supply unit specifications

This section provides the specifications, performance, and behavior of the PSU for each single block and the overall PSU. Table 2 shows the required performance and specifications under several steady-state and dynamic conditions.

Table 2 Summary of specifications and test conditions for the 3300 W PSU

Test	Conditions	Specification
Input voltage V_{AC}	–	180 V_{AC} to 265 V_{AC}
Output voltage V_{DC}	–	50 V_{DC} nominal
Output power	Input 180 V_{AC} to 265 V_{AC}	3300 W
Steady-state ripple (max.)	–	± 500 mV peak-to-peak max.
Efficiency test (full PSU)	Input 230 V_{AC} at 50 Hz 30% to 100% of full load	97.63% peak
		96.75% min.
	Input 230 V_{AC} at 50 Hz 10% to 30% of full load	97.15% min.
iTHD (max.)	230 V_{AC} at 50 Hz	8%
Power factor	30% to 100% load	0.98 min.
Dynamic Load	Load jumps from 10% to 90% every 25ms	
Hold-up time	100% load	10 ms
Overcurrent protection (OCP)	Shut down and latch	>65 A
Overvoltage protection (OVP)	PFC bulk voltage	440 V_{DC}
Undervoltage protection (UVP)	PFC bulk voltage	330 V_{DC} in LCDO conditions
AC line cycle dropout (LCDO)	100% load	10x [10 ms dropout, 100 ms interval]
Sag voltage (T<500ms)	230 V to 160 V at full load at 0° and 45° for 500 ms	
Sag voltage (T>500ms)	230 V to 160 V at full load at 0° and 45°	The board has to work for 500 ms and then restart when the AC is back in range
EMI	EMI at full load (measured in the lab with an uncertified setup)	The board has to be compliant with Class A requirement

4.2 PSU efficiency and power losses

Figure 34 shows the efficiency measurements for the steady-state operation of the overall PSU at different AC voltages. The efficiency measurements have been obtained with a WT3000 power analyzer with any input output line filters, and the plots do not include fan power consumption.

Note: Due to production and measurement tolerances, variations of ±0.2% was observed.

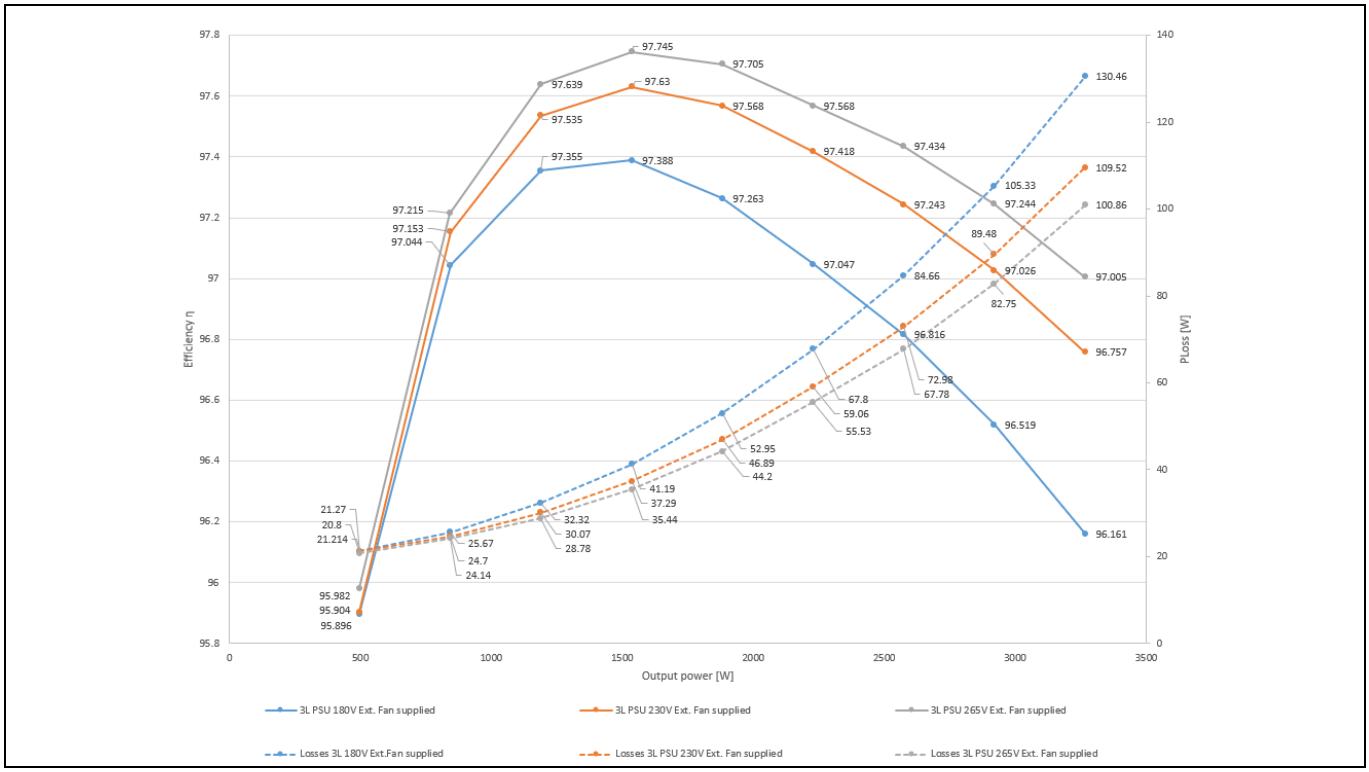

Figure 34 Measured efficiency and power losses of REF_3K3W_3LFC_PSU (no fan) for different input line voltages at 50 Hz

Figure 35 shows the efficiency measurements for steady-state operation including fan power consumption. Fan speed is automatically adjusted for achieving the maximum efficiency in all load ranges.

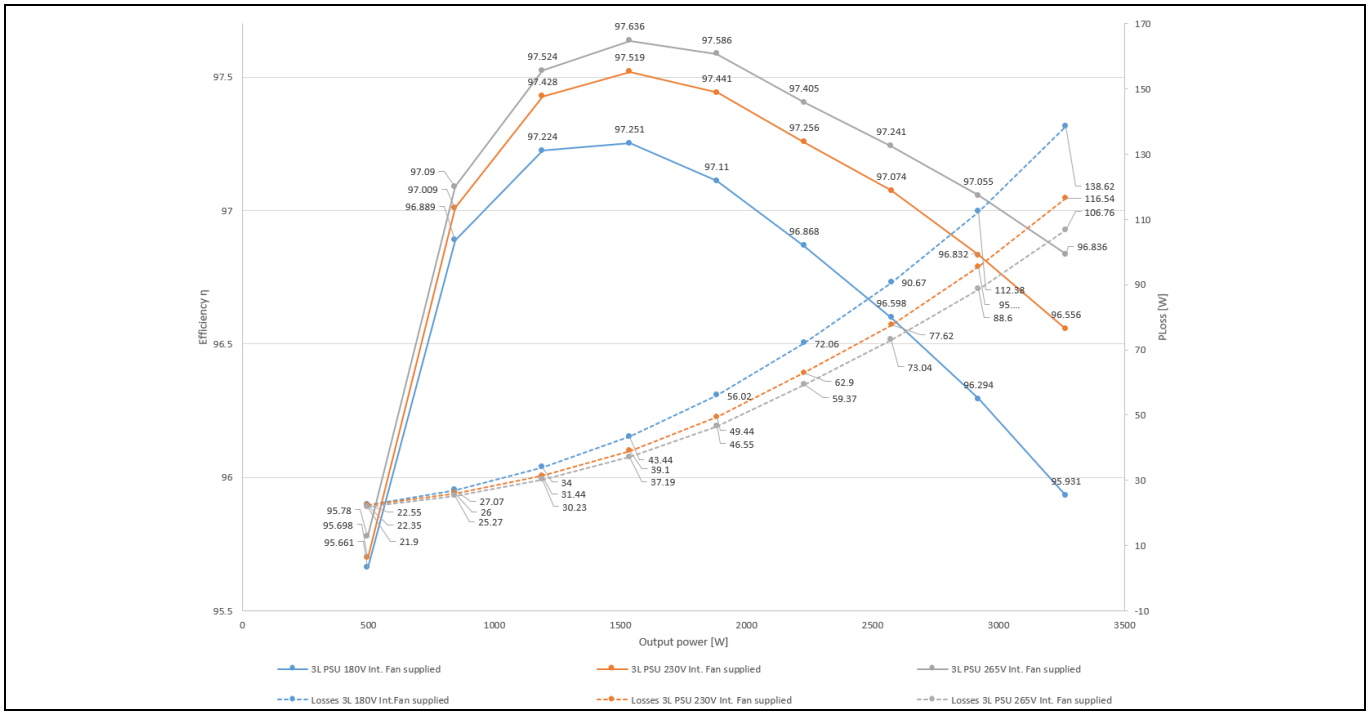

Figure 35 Measured efficiency and power losses of REF_3K3W_3LFC_PSU (with fan) for different input line voltages at 50 Hz

4.3 PFC Steady-state waveforms

Figure 36 and Figure 37 show the PSU startup sequence at 100 V AC and 230 V AC respectively. These figures demonstrate the startup and steady state condition of the full power supply at full load conditions.

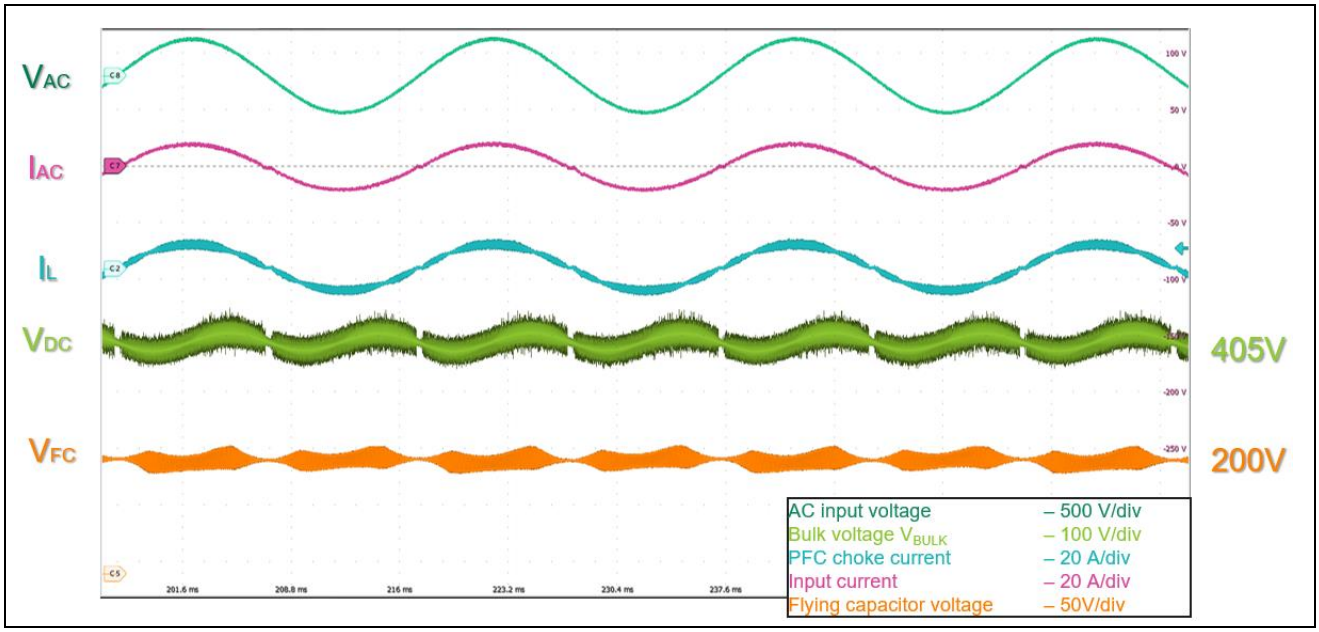

Figure 36 PFC steady-state operation at 230 V_{AC}, full-load

4.4 Output and bulk voltage ripple

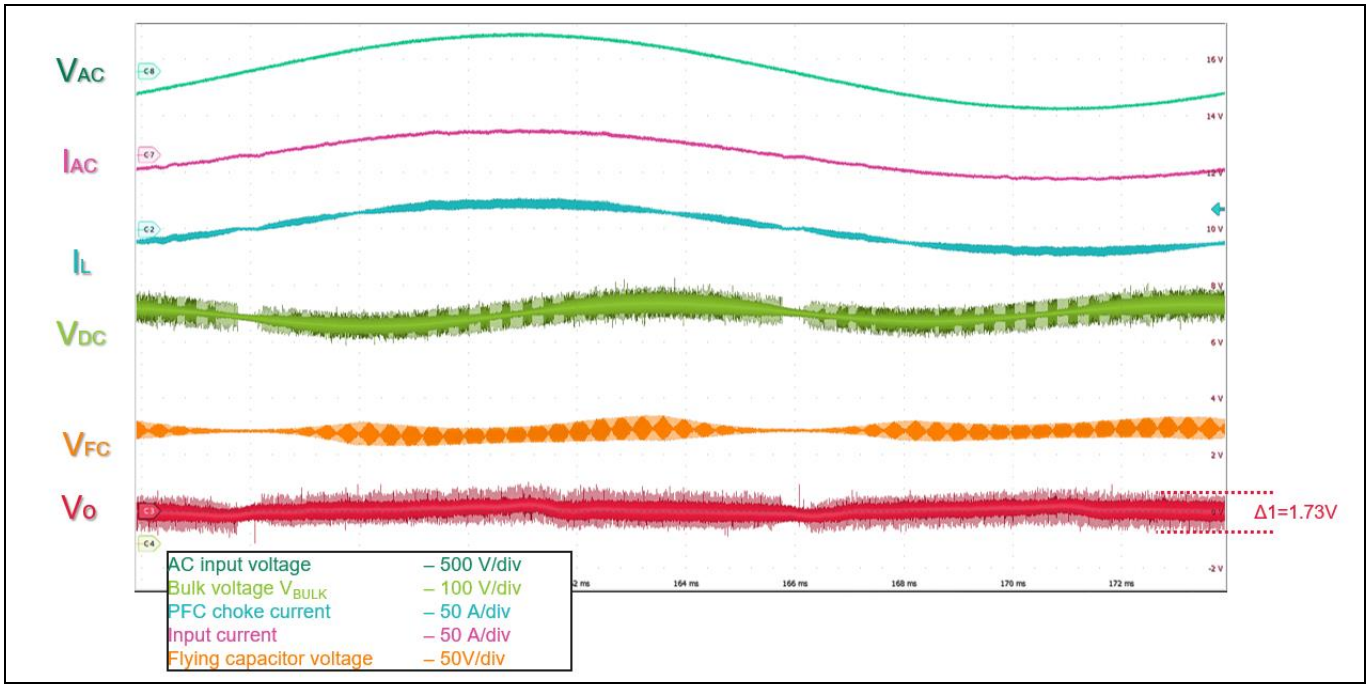

Figure 37 Output voltage ripple for 100 percent load conditions

4.5 Half-bridge LLC

The half-bridge LLC using CoolGaN™ IGT65R035D2 on the primary-side and IQE046N08LM5 for the SR stage. Figure 38 and Figure 39 show ZVS turn-on and the lossless turn-off of the half-bridge LLC at 100% and 50% of the rated load.

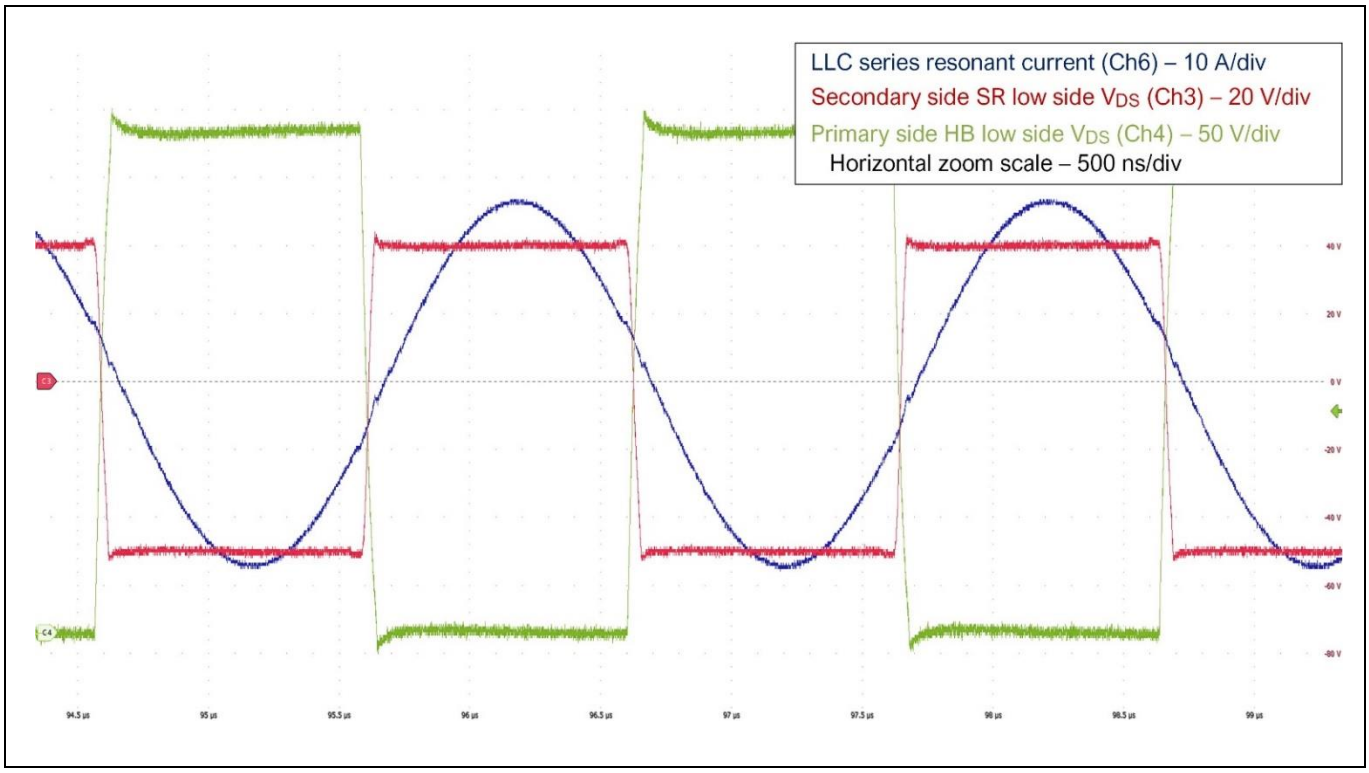

Figure 38 LLC waveforms during steady-state operation at 100% of the rated load

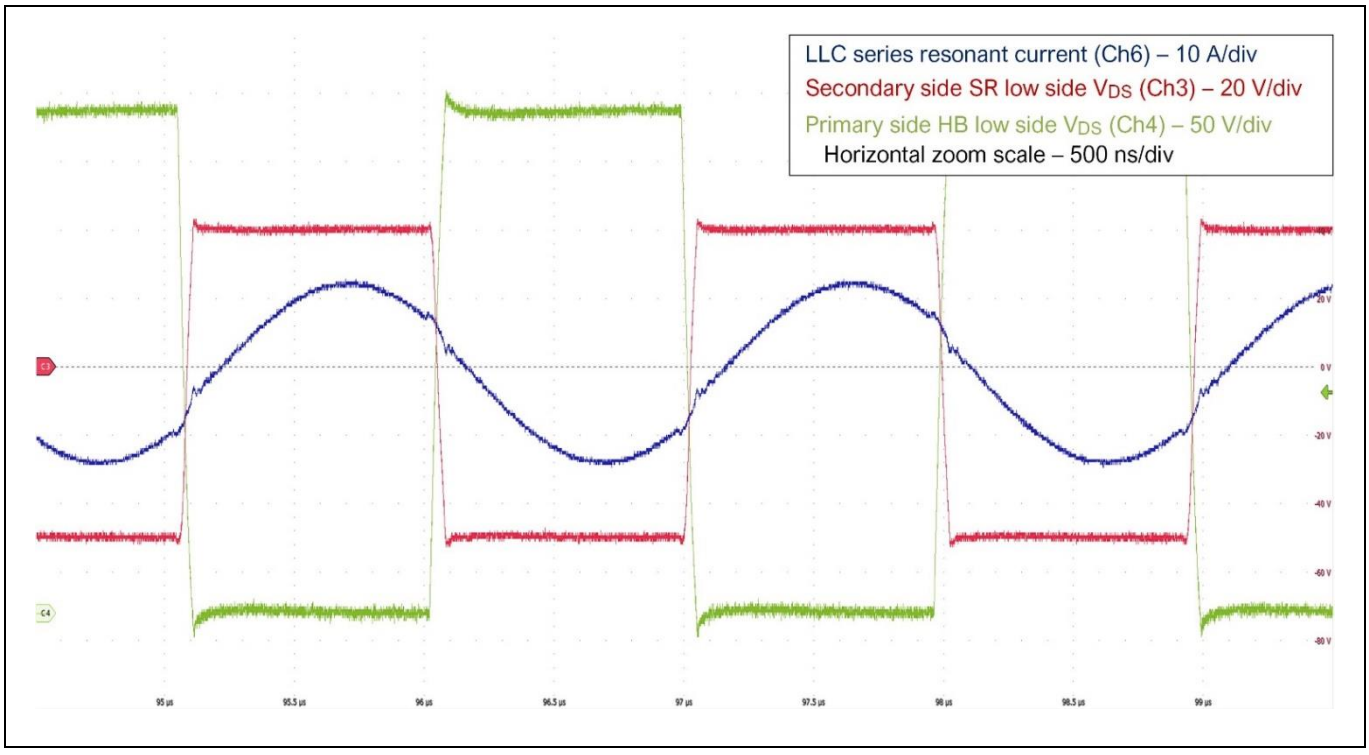

Figure 39 LLC waveforms during steady-state operation at 50% of the rated load

The frequency variation of the LLC during steady-state operation due to the bulk voltage ripple is shown in Figure 40.

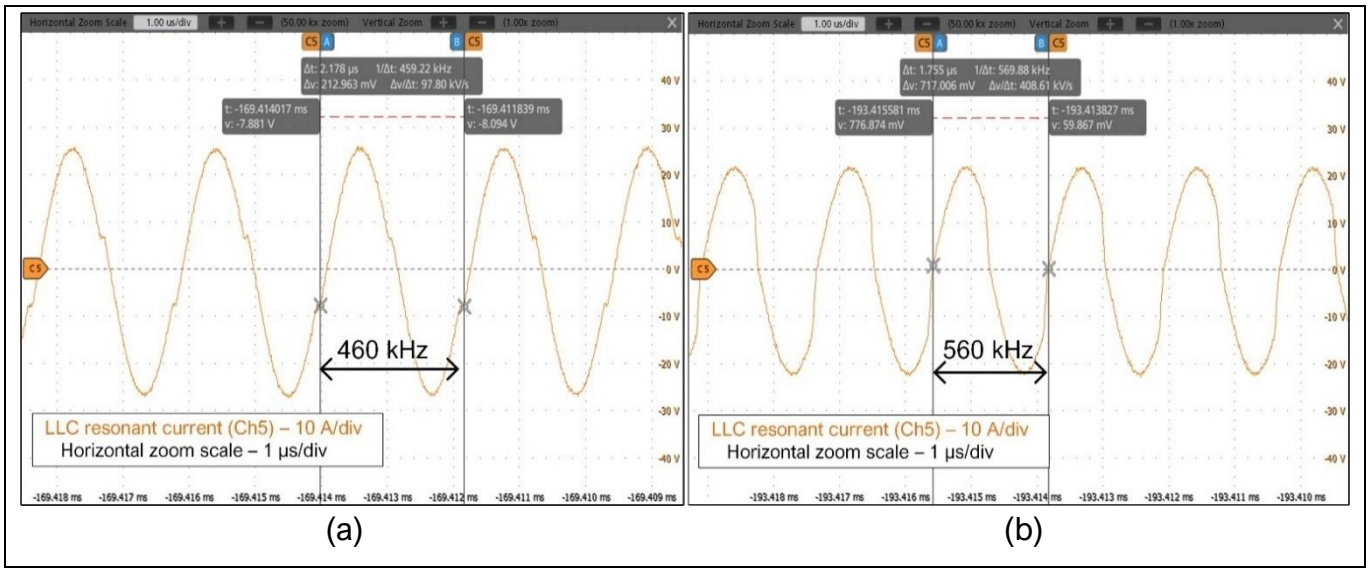

Figure 40 LLC Resonant current at full-load, steady-state for (a) maximum and (b) minimum bulk voltage

4.6 Dynamic conditions

4.6.1 Load transients

The PSU has been tested for 10% to 90% load transient with 1 A/µs slew rate and 20 Hz repetition rate, as shown in Figure 41 and Figure 42.

A feed-forward mechanism of the output current to the PFC voltage loop has been implemented. This allows ultra-fast recovery of the bulk voltage in less than 25 ms, enabling the PSU to withstand the transients with 20 Hz repetition rate even without a power buffer like the baby-boost converter.

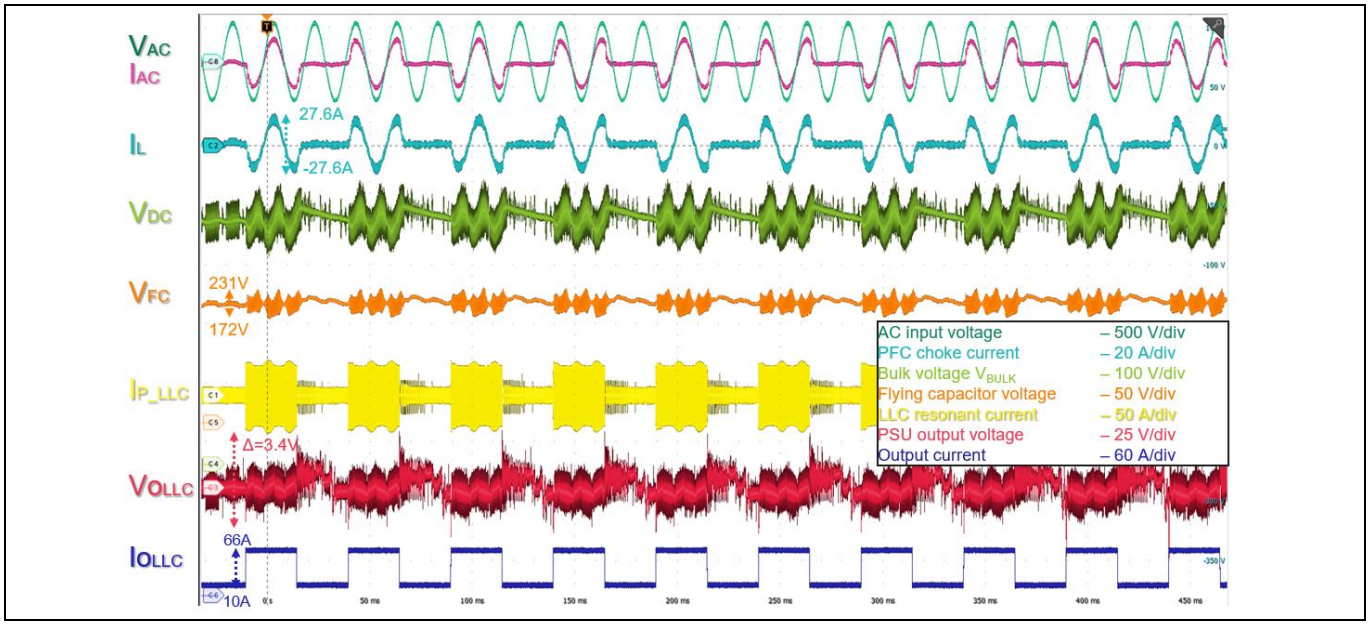

Figure 41 10% to 90% to 10% load transients of the full PSU at 20 Hz repetition rate

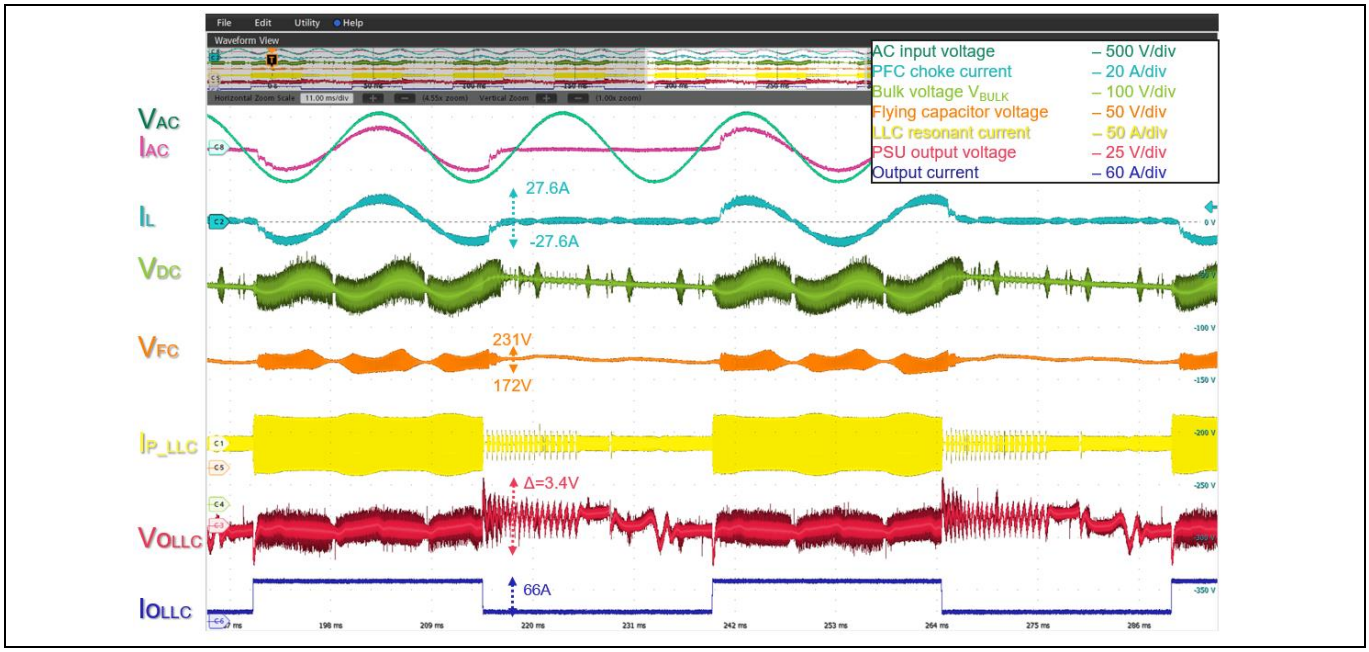

Figure 42 Zoomed view of 10% to 90% to 10% load transients of the full PSU at 20 Hz repetition rate

4.6.2 Voltage sag test

For this high-line design, a single voltage sag condition is considered and tested (Figure 43). The considered condition is 500 ms at 70% of the nominal AC voltage, which implies a temporal operation of the PSU with 160 V AC input. Figure 43 and Figure 44 show the PSU performance under specified sag conditions for different starting angles. It demonstrates that the flying capacitor DC level remains around the steady-state value with an increased high-frequency component due to the increased inductor current. Not only is the average inductor current limitation applied in the REF_3K3W_3LFC_PSU board, but the inductor peak current is also limited to 45 A.

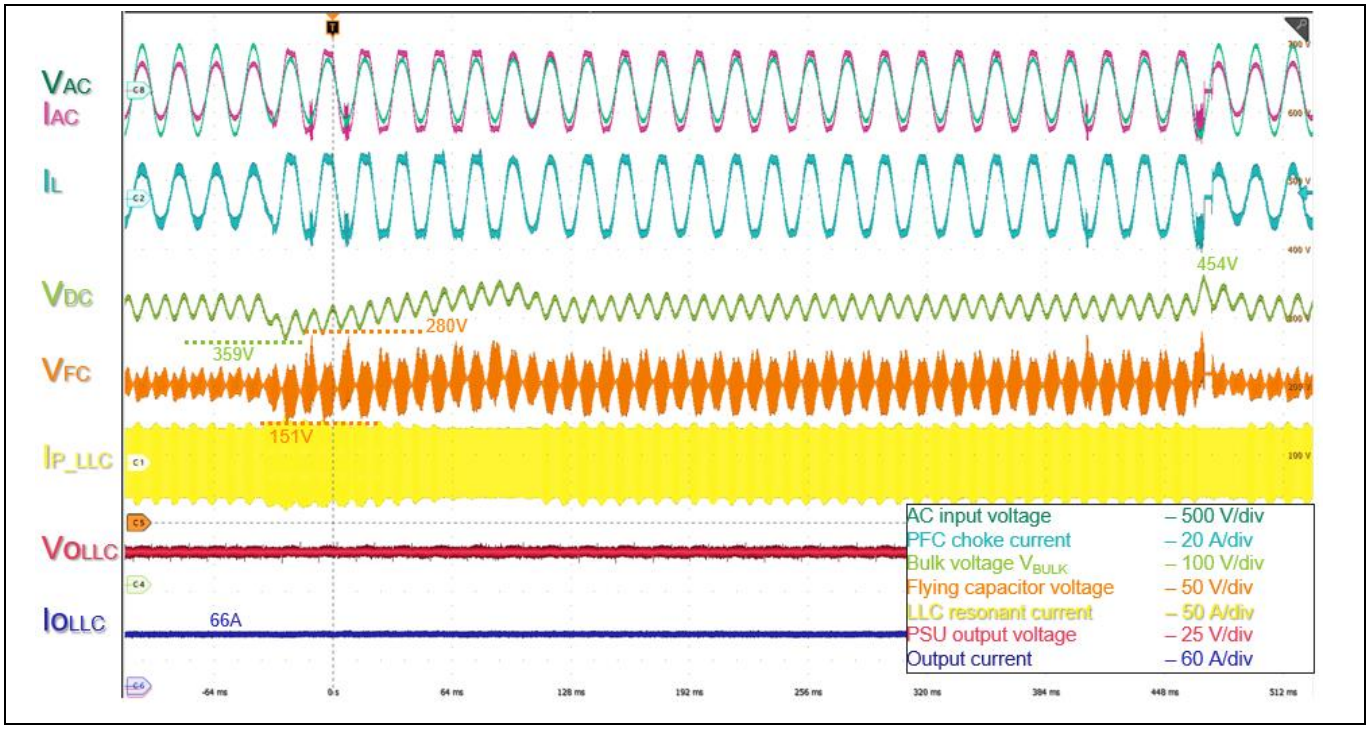

Figure 43 Sag test 230 V - 160 V at 0 Deg at full load for 500 ms

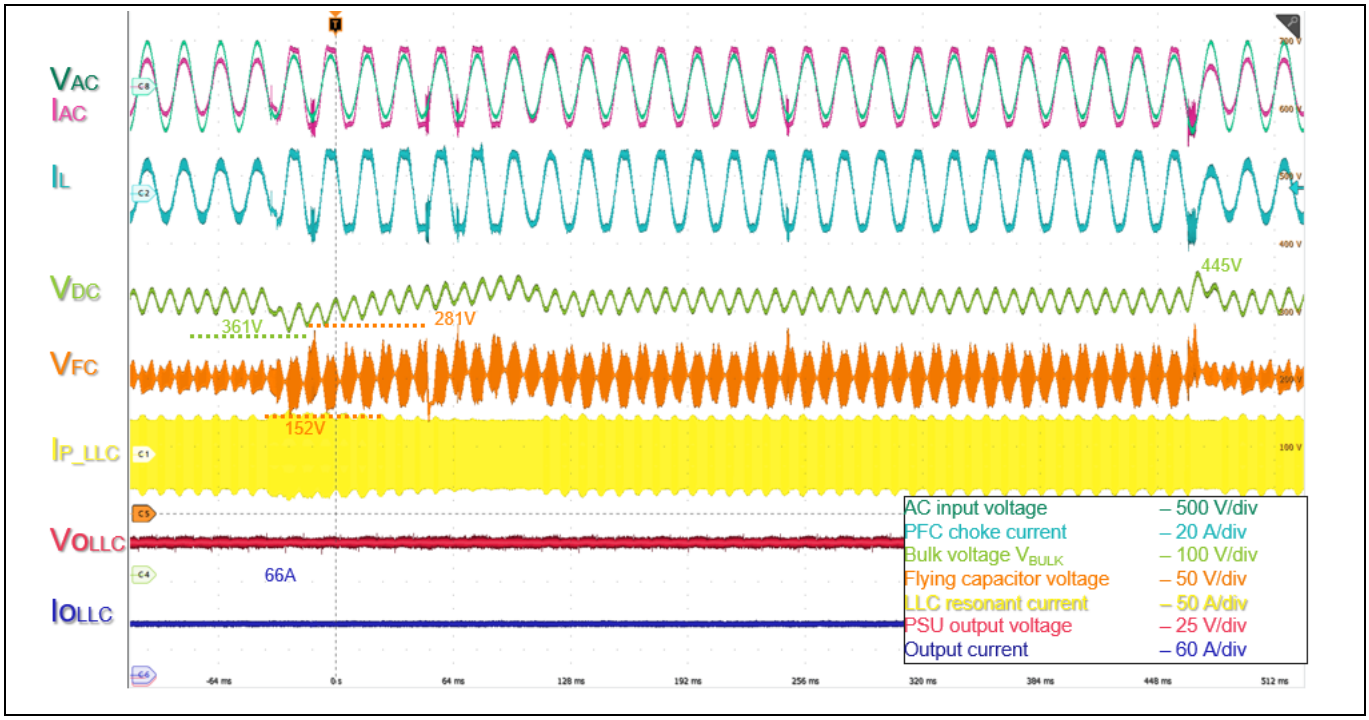

Figure 44 Sag test 230 V-160 V at 45 Deg at full load for 500 ms

Figure 44 shows this behavior when a voltage sag to 160 V_{RMS} is applied for 500 ms at full load.

However, if the voltage is under the nominal range for longer than the time specified in Table 1, the PSU turns off and restarts with a soft-start after an idle time, as shown in Figure 45.

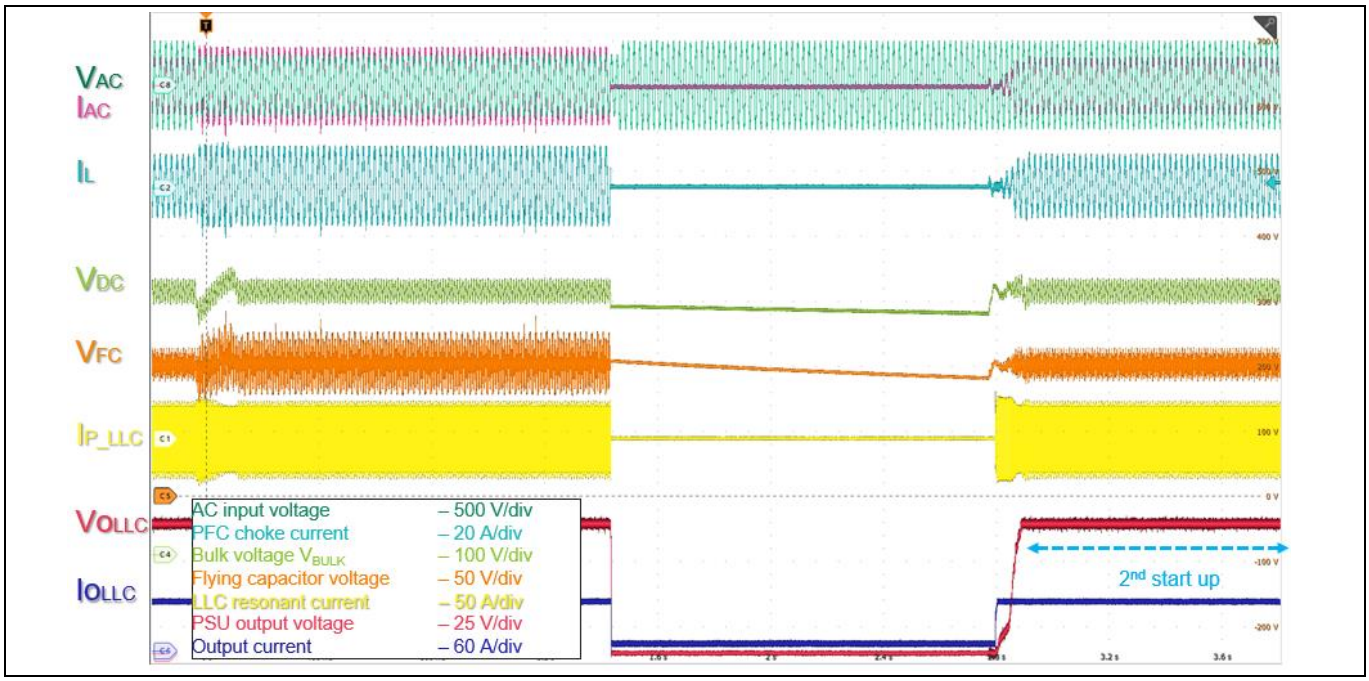

Figure 45 Sag test 230 V-160 V at 0 Deg at full load for more than 500 ms

4.7 Hold-up time extension

Hold-up time extension with the baby-boost converter (Figure 46) has been tested within the PSU. From an operation point of view, the baby-boost stage is not always active, and triggers when a bulk voltage drop below 380 V_{DC} is detected along with the absence of AC line input. At this point, the CM8 static switch opens and the voltage at the LLC input is boosted (taking the energy from a deep discharge of the bulk capacitors) until the bulk voltage achieves a cut-off threshold of 250 V_{DC}. Under these conditions, a maximum hold-up time extension of 14.8 ms has been proven at full load until the PSU output drops, with 900 µF nominal bulk capacitance.

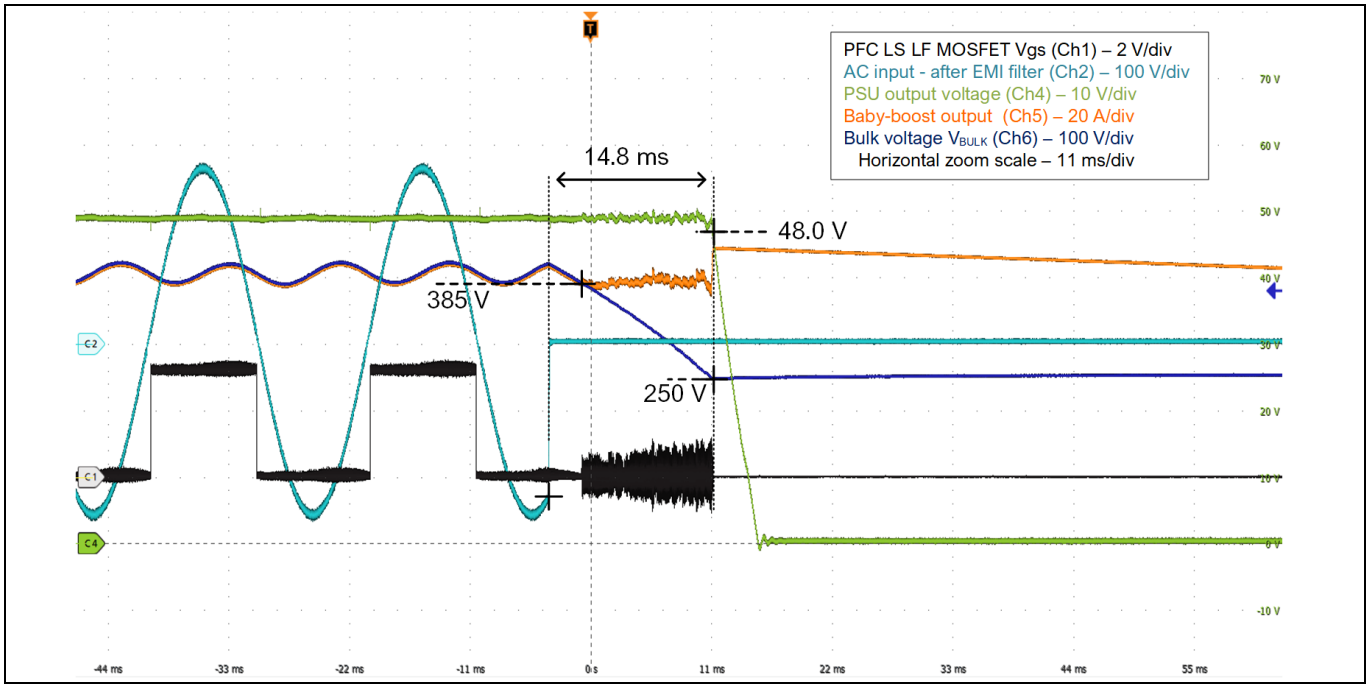

Figure 46 Hold-up time at 100 percent of the rated load

4.7.1 AC line cycle dropout test

During line cycle dropout (LCDO), the baby-boost converter activates, and the resulting waveform is shown in Figure 46. LCDO testing was conducted at full load, with phase voltage drops applied at 0° and 45°, the last condition represent the worst-case condition, as the bulk voltage reaches its minimum peak. The test sequence consisted of ten repeated LCDO events, each featuring a 10 ms complete line voltage interruption, with 100 ms intervals between successive dropouts. The main results of the LCDO test are reported in Figure 47 to Figure 49.

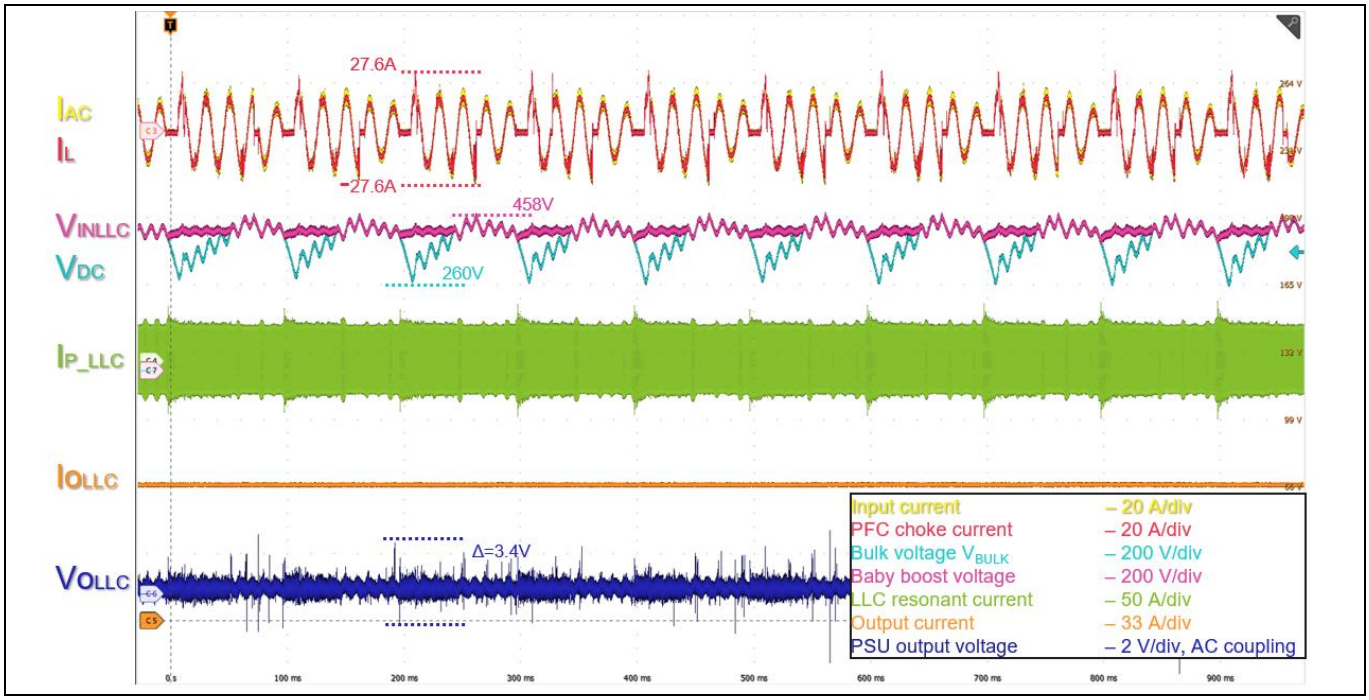

Figure 47 AC line cycle dropout (ACLDO) at 100 percent load, AC phase 0 degrees

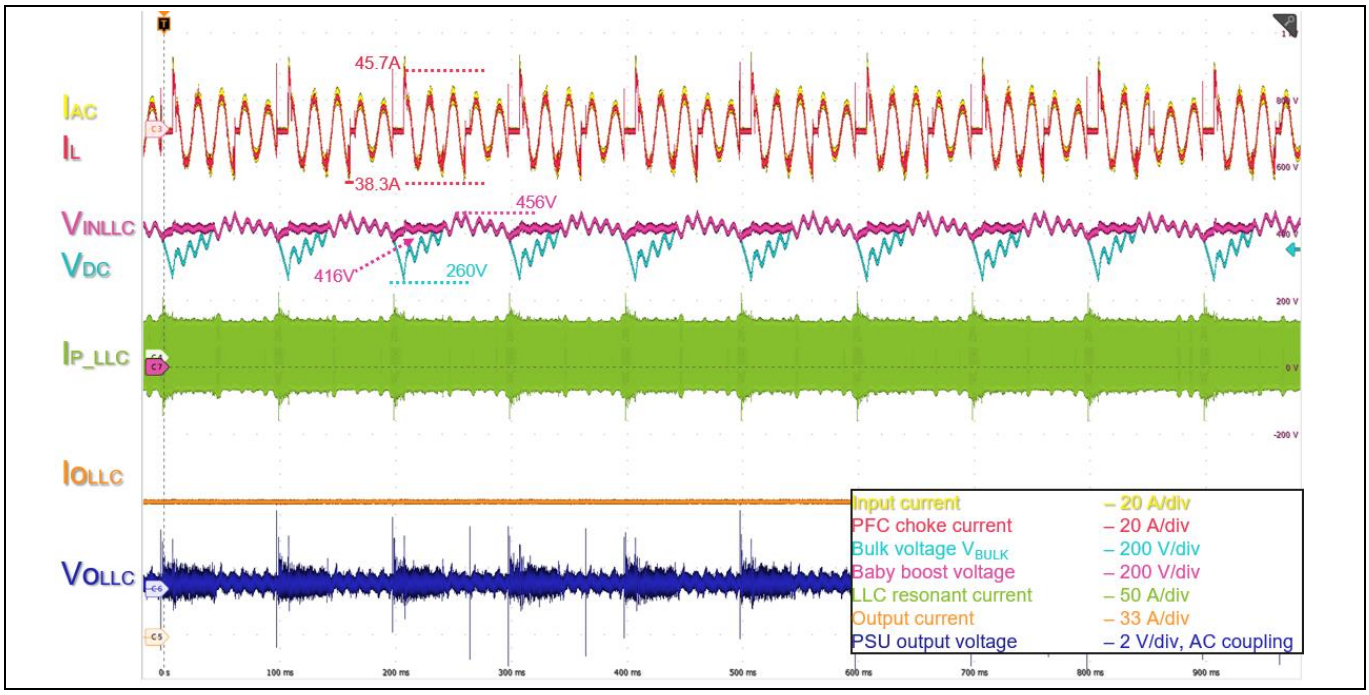

Figure 48 AC line cycle dropout (ACLDO) at 50 percent load, AC phase 45 degrees

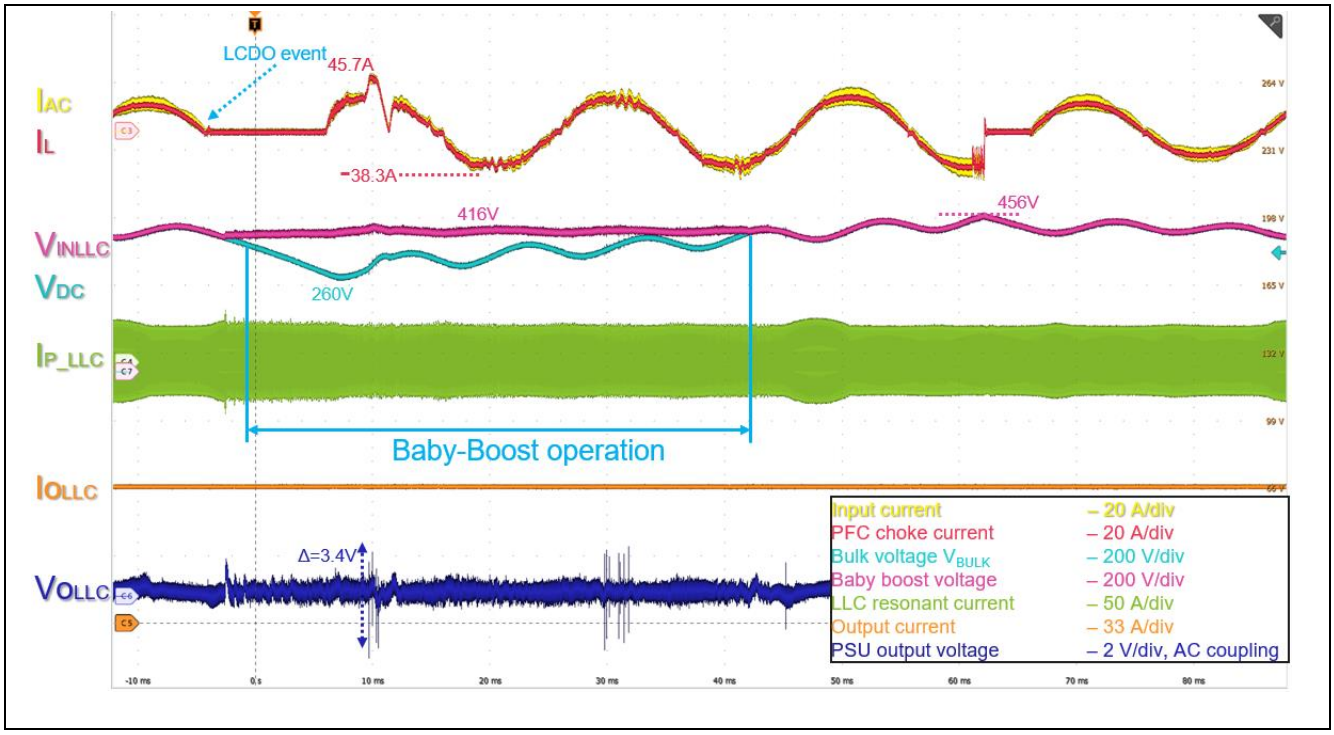

Figure 49 Detailed single event of AC line cycle dropout at 100 percent load, AC phase 45 degrees

4.8 Thermal performance

Thermal performance of the full rectifier has been taken with Type J thermocouples, fan supplied externally, and a 25°C ambient temperature. The PSU temperature has been taken with full enclosure to provide proper cooling as the enclosure conveys the airflow through the high-temperature component through a “pipe” on the right-hand side of the converter. As Figure 50 (left) shows, the fan sucks air out of the unit, being the LLC SR getting the cold air entering the PSU. Critical hotspots such as the PFC high-frequency leg, LLC primary-side, and SR MOSFETs and drivers are shown in Figure 50.

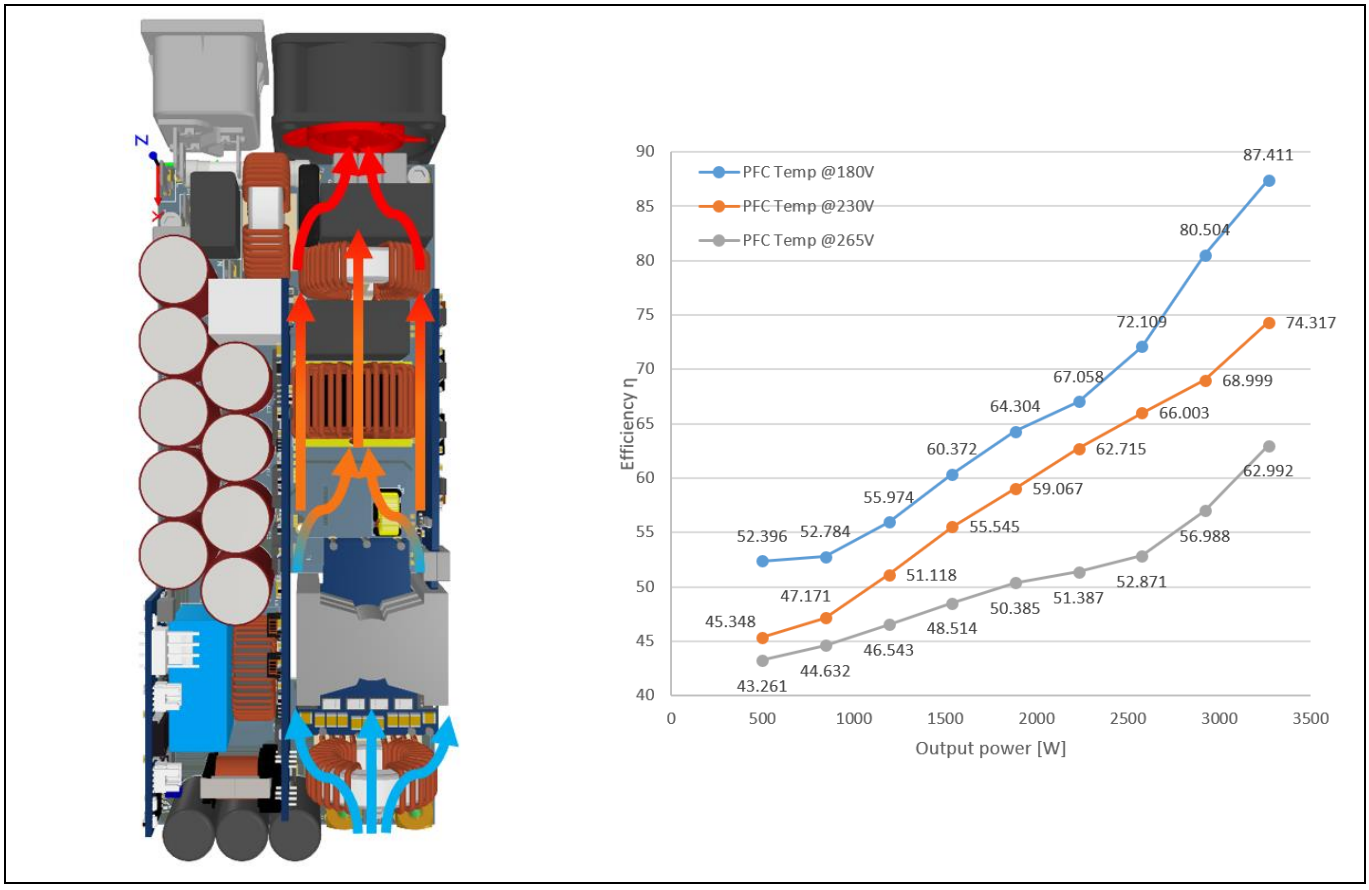

Figure 50 PSU temperature vs. load with IMT65R025M2H at 180 V_{AC} and 230 V_{AC}

4.9 EMI measurements

The conducted electromagnetic interference (EMI) of the full PSU was measured with the setup shown in Figure 51. The AC voltage is generated by an AC source and the connection to the PFC is established with a line impedance stabilization network (LISN). The spectrum analyzer is connected to the LISN. The load used for the test is a passive resistive load.

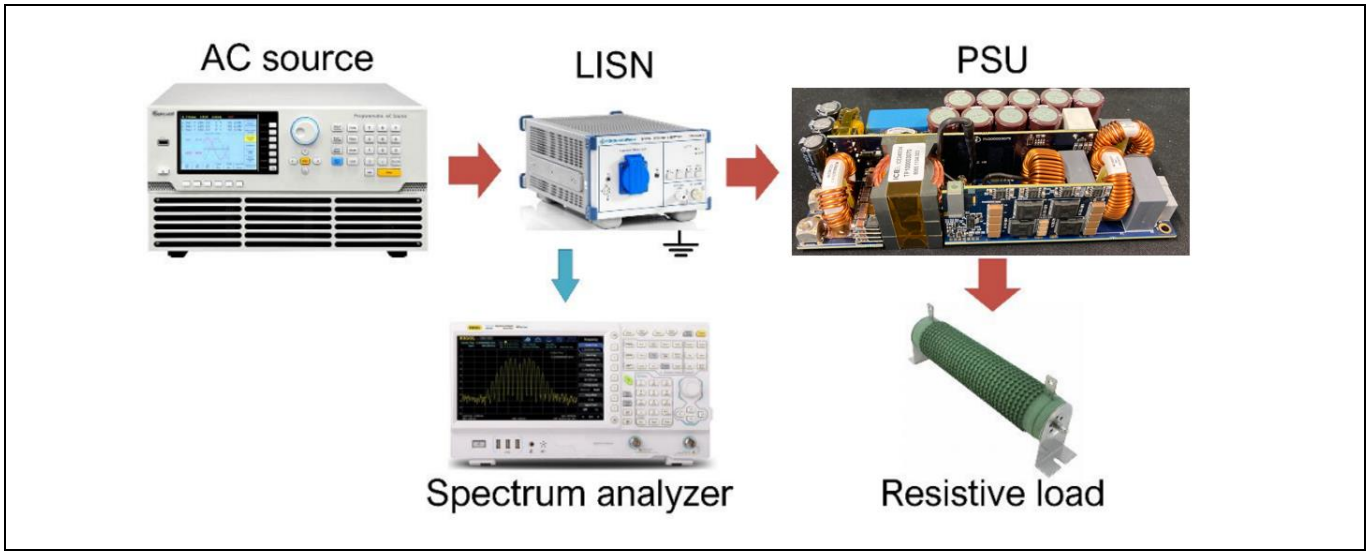

Figure 51 Setup used for EMI test

The EMI tests were performed with an input of 230 V_{AC} and 3.3 kW output power. Figure 52 shows the noise present in the setup while Figure 53 shows the results of the average (AVG) and the positive-peak measurements at 230 V_{AC}. The PSU is fully compliant with Class A limits in both peak and average measurements. The measured positive peak values represent a worst-case compared to the quasi-peak of the standard. A margin of 6 dB is also always achieved.

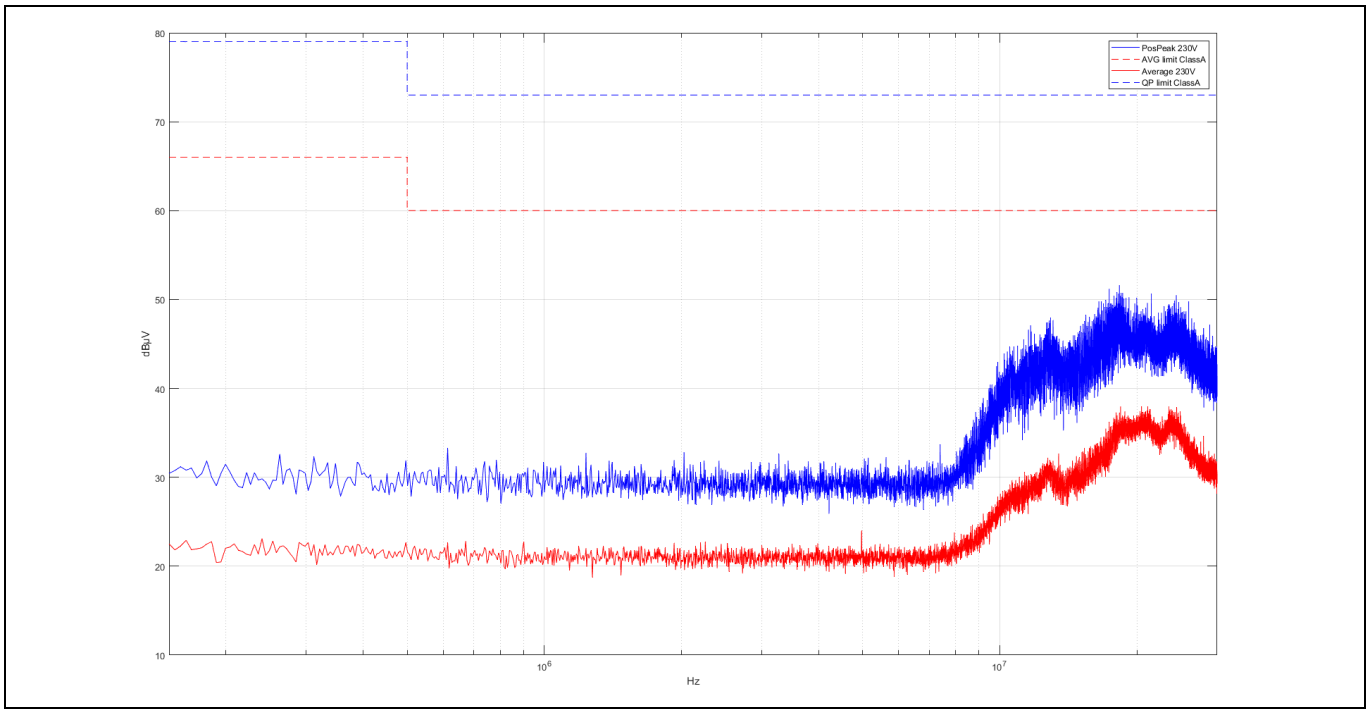

Figure 52 EMI setup noise measurements

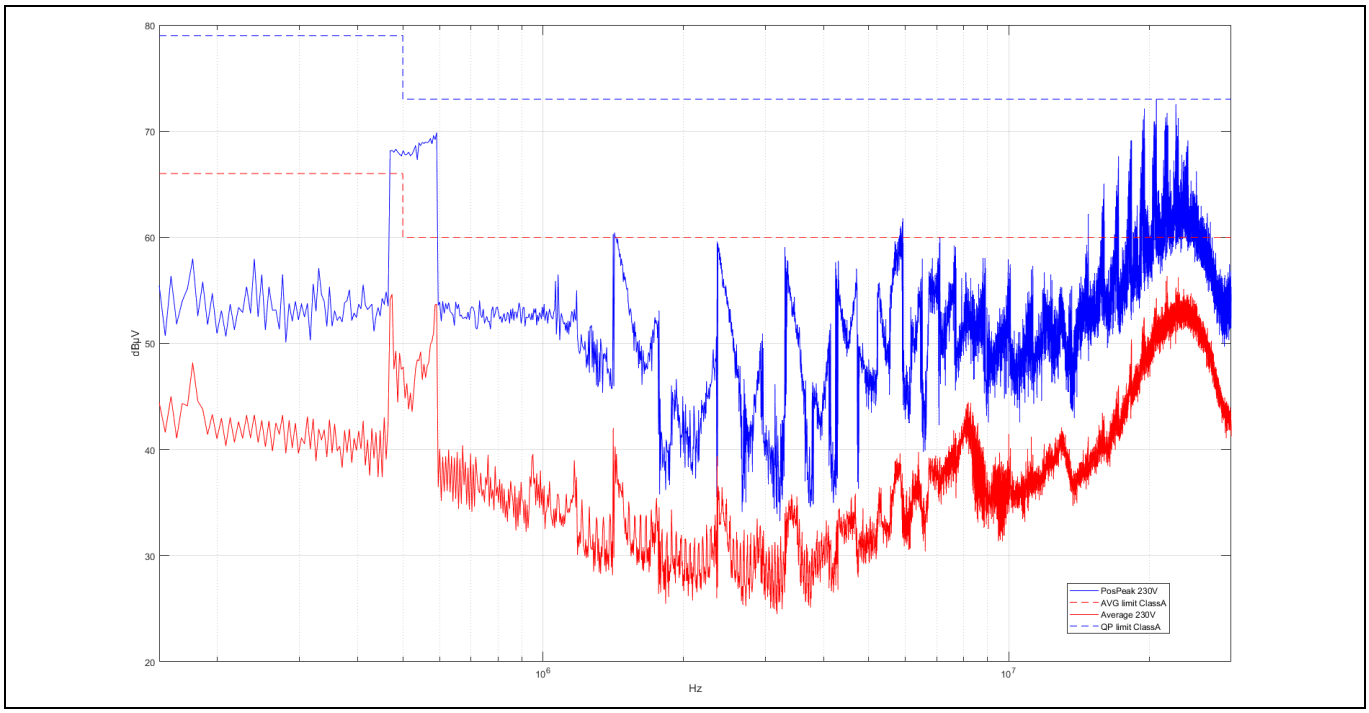

Figure 53 AC input EMI of the PSU at 230 V_{AC} input and 3.3 kW, and a comparison with the EN 55032 limit

4.10 Efficiency: EVAL_3K3_3L_PSU vs EVAL_3K3_HFHD_PSU

Figure 54 shows the efficiency comparison between EVAL_3K3_3L_PSU and EVAL_3K3_HFHD_PSU. To ensure consistency in the comparison between the two boards, the efficiency of the HFHD was reassessed. It is important to note that the efficiency test was conducted on a different bench compared to the previous measurements taken for the HDHF application note. This change in setup may result in some discrepancies between the earlier and current measurements, as differences in the tolerances of the two setups can affect the results.

Figure 54 provides a detailed comparison of the efficiency of the two boards across different AC input voltages, specifically at 180 V, 230 V, and 265 V AC. In all three plots, the red line represents EVAL_3K3_3L_PSU, while the blue line represents EVAL_3K3_HFHD_PSU.

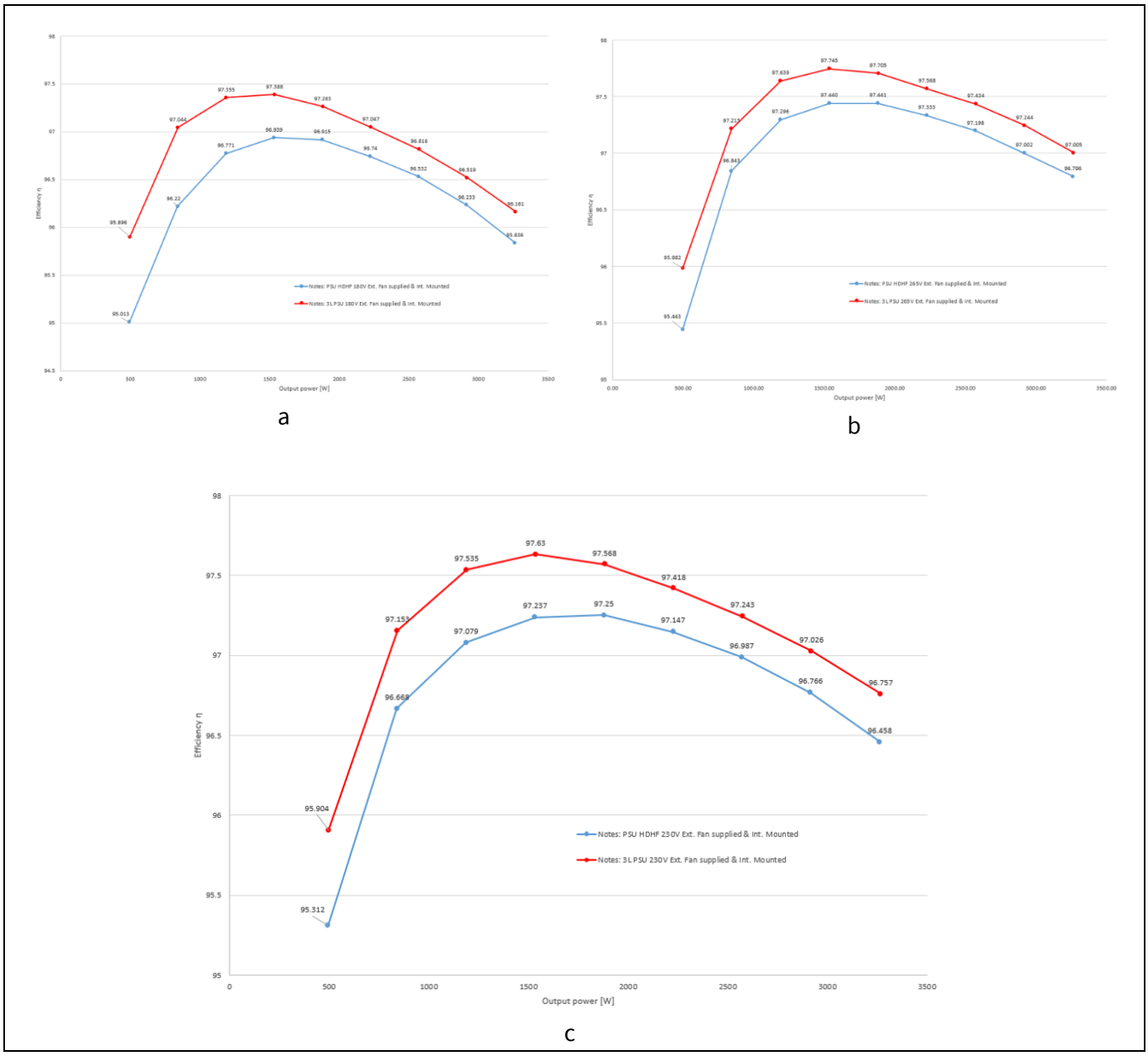

Figure 54 (a) PSU efficiency at 180 V_{AC} , (b) PSU efficiency at 265 V_{AC} , (c) PSU efficiency at 230 V_{AC}

5 Summary

This document presents a comprehensive system solution from Infineon, designed for server PSU applications. The solution integrates a bridgeless interleaved totem-pole PFC converter and a DC-DC isolated half-bridge LLC converter, achieving a power density of 98 W/in^3 and an efficiency level of 97.64% at 265 V_{AC}, 97.52% at 230 V_{AC}, and 97.1% at 180 V_{AC} (with fan). Tested without a fan, it also achieves 97.75% at 265 V_{AC}, 97.63% at 230 V_{AC}, and 97.39% at 180 V_{AC}.

The REF_3K3W_3L_PSU reference board employs CoolSiC™ 650 V and 600 V CoolMOS™ MOSFETs, and CoolGaN™ power transistors in TOLL packages along with OptiMOS™ 6 MOSFETs. This combination of CoolSiC™, CoolMOS™, CoolGaN™, and OptiMOS™ transistors enables high performance within a compact form factor, as detailed in the document. The bridgeless PFC and half-bridge LLC incorporate full digital control through an XMC™ 4000 MCU.

The PSU's performance excels not only in steady-state conditions, it also meets power line disturbance and hold-up time requirements. This is achieved with an additional hold-up time boost converter, which can deliver the required 10 ms hold-up at full load.

Furthermore, the REF_3K3W_HFHD_PSU board has been tested using a programmable AC source and an electronic load. Efficiency, THD, and PF results were obtained using the WT3000 power analyzer from Yokogawa, alongside waveform analysis with the MSO58 (1 GHz; 6.25 GS/s) oscilloscope from Tektronix.

6 Bill of materials

Infineon main components are marked in bold.

Table 2 Bill of materials for the main board M100001388

Designator	Value	Tolerance	Voltage	Description
C1, C2, C6, C7	4.7 nF	Y2	300V	Capacitor ceramic
C3	0.82 µF X2	20%	275Vac	Capacitor foil
C4, C5	2.2 µF X2	20%	275Vac	Capacitor foil
C8, C9, C32, C33, C34, C35	10 nF	5%	630V	Capacitor ceramic
C10	10 uF	10%	450V	Capacitor foil
C11, C12, C13, C14, C15, C16, C17, C18, C29	100 uF	20%	450V	Capacitor polarized
C19, C20, C21, C44, C48	1 uF	X7R	35V	Capacitor ceramic
C22, C23, C26, C27, C37, C43, C45, C46, C47, C49, C50, C51, C52	4.7 uF	X8L	100V	Capacitor ceramic
C28, C36, C38, C41, C53, C54	100 nF	X7R	630V	Capacitor ceramic
C30, C31, C39	820 uF	20%	63V	Capacitor electrolyt
C40, C42	100 pF	X7R	50V	Capacitor ceramic
D1, D2	S8KCDICT		800V	Standard diode
D3	IDL10G65C5		650V	Schottky-diode
F1	20A			Sicherung
IC1	MCR1101-20-3			Hall sensor
IC3	1EDN8511B			Integrated circuit
IC4	1EDB8275F			Integrated circuit
J1, J2	7460307-			Screw terminal
L1, L2	1.4 mH			Common mode choke
L3	30 uH			Buffer choke
L4				Inductor
L6	32 uH			Inductor
NTC1	14 R	25%		NTC resistor
Q2	IPT60R080G7		600V	NMOSFET
Q3	IPT60R016CM8		600V	NMOSFET
R1, R17, R18, R19, R20, R21, R22, R23, R24, R29, R30, R31, R32, R33, R35, R38	309k	0.1%		Resistor
R2, R6	10R	1%		Resistor
R3	4R7	1%		Resistor
R4, R5	4R7	1%		Resistor
R7, R9	10R	1%		Resistor
R8, R27	100R	1%		Resistor

Designator	Value	Tolerance	Voltage	Description
R15	0R	1%		Resistor
R45	R003	1%		Resistor
T1	TF100003070			PWR transformer
TR1	MG600003070			Current sense transformer
X1				Pin header, 26 contacts
X1, X4	Faston Connector TE1217421-1			Connector
X3				Female header, 10 contacts
X5	Faston Connector TE1217421-1			Connector
X6				Female header, 26 contacts 2mm

Table 3 Bill of materials for the 3L PFC HF power card PW100001389

Designator	Value	Tolerance	Voltage	Description
C1, C2, C3, C4, C5, C6, C7, C8				Capacitor
C13, C14, C15	100 nF	X7R	630V	Capacitor ceramic
C16, C17	100 n	X7R		Capacitor unpolarized
C18, C19, C27, C50, C51, C52	1 uF	X7R	35V	Capacitor ceramic, capacitor unpolarized
C21	1 n	X7R	50V	Capacitor unpolarized
C22	220 n	X7R	50V	Capacitor unpolarized
C26, C28, C39, C40	100 n	X7R	35V	Capacitor unpolarized
C29, C32, C35, C37	1 uF	X7R	35V	Capacitor unpolarized
C42, C43, C44, C45, C46, C47, C48, C49	100p	X7R	50V	Capacitor unpolarized
D2				Schottky-diode
D7, D8, D11, D14, D17				Medium power AF schottky diode, SOD323, reel, green
IC1				Integrated circuit
IC2				Dual channel 5A / 4A, high-speed, low-side gate driver IC
IC3, IC4, IC5, IC6				Integrated circuit
NTC	10kNTC			Resistor
Q1, Q2, Q3, Q4				Insulated-gate field-effect transistor (IGFET), N-Channel, enhancement, body diode, Pin 1 gate, 2 driver source, 3 source, 4 source, 5 source, 6 source, 7 source, 8 source, 9 drain, 9 pins

Designator	Value	Tolerance	Voltage	Description
Q7, Q10				IGFET, N-Channel, enhancement, body diode, Pin 1 gate, 2 drain, 3 source, 3 pins
Q8, Q11				Bipolar (BJT) transistor NPN 600 V SOT323
R1, R3, R5, R7	3R3	1%		Resistor
R2, R4, R6, R8	2R2	1%		Resistor
R12, R13	2M55	1%		Resistor
R14	51k	1%		Resistor
R15	62k	1%		Resistor
R16	110R	1%		Resistor
R20, R21	9.31k	0.1%		Resistor
R22	7k5	0.1%		Resistor
R23	100k	0.1%		Resistor
R24	261k	0.1%		Resistor
R25	42k2	0.1%		Resistor
R28, R29, R30, R31	340k	0.1%		Resistor
R32, R33	680k	0.1%		Resistor
R34	300k	0.1%		Resistor
R35	18k4	0.1%		Resistor
R36, R37, R38, R39	604k	0.1%		Resistor
R40	3k9	1%		Resistor
R41	5k6	1%		Resistor
R42, R43, R44, R45, R46, R47, R48, R49	510R	1%		Resistor
R51, R56, R58	0	1%		Resistor
R52, R53, R54, R55	10k	1%		Resistor

Table 4 Bill of materials for the LLC power card PW200001388

Designator	Value	Tolerance	Voltage	Description
C2, C26	150 uF	20%	16 V	Capacitor polarized
C3, C7, C8, C9, C17, C18, C30	1 uF	X7R	35 V	Capacitor ceramic
C4, C6, C10, C11	2n2	X7R	50 V	Capacitor ceramic
C5, C19, C20, C23, C28	100 pF	X7R	50 V	Capacitor ceramic
C12, C14, C15, C35, C36	100 nF	X7R	630 V	Capacitor ceramic
C13	10 uF	X7R	25 V	Capacitor ceramic
C16, C21, C31, C32	10 uF	X7R	50 V	Capacitor ceramic
C24	100 nF	X7R	25 V	Capacitor ceramic
C27	1 nF	X7R	50 V	Capacitor ceramic
C29	33 uF	10%	20 V	Capacitor polarized
C34	330 pF	X7R	50 V	Capacitor ceramic

Designator	Value	Tolerance	Voltage	Description
D1, D9, D10	BAT165	–	40 V	Schottky-diode
D2, D7, D8	DFLS1200	–	200 V	Diode
D5	FES1JE	–	600 V	Diode
IC1, IC4	**1EDB8275F**	–	–	**Gate driver IC**
IC2	**1EDN8550B**	–	–	**Gate driver IC**
IC5, IC9	**1EDN8511B**	–	–	**Gate driver IC**
IC6	TLV431B	0.5%	1.24 V	TLV431B- adjustable precision shunt regulator 0.5%
IC7	**ICE2QR2280G**	–	–	**Integrated circuit**
IC8	VOL617A-3	–	–	Integrated circuit
L1, L2, L3, L4	SRF2012-361YA	–	–	Common mode power line choke
Q1, Q2, Q3, Q4	**IGT60R042D2**	–	–	**GaN HEMT transistor**
Q5, Q6, Q7, Q8	**IPT60R016CM8**	–	**600 V**	**MOSFET**
Q9, Q10	**BSS138N**	–	**60 V**	**MOSFET**
R2, R5, R9, R14, R15, R16, R19, R20, R23, R24, R26, R29, R47	10R	1%	–	Resistor
R3, R4, R27, R28	2R7	1%	–	Resistor
R6, R7, R46, R48	1k	1%	–	Resistor
R8	150R	1%	–	Resistor
R10, R13, R45	33k	1%	–	Resistor
R11, R17, R18, R21, R22, R25, R36	510R	1%	–	Resistor
R12	10K NTC	3%	–	Resistor
R30, R31, R32, R33	270R	1%	–	Resistor
R34, R35, R40	15k	1%	–	Resistor
R37, R39	825R	1%	–	Resistor
R38	3k6	1%	–	Resistor
R41	1k18	0.1%	–	Resistor
R42	1R5	1%	–	Resistor
R43	2K7	1%	–	Resistor
R44	10k	1%		Resistor
REL1	G2RL-1A-E2-CV-HA - DC12	–	12 V	Relay
TF1	ICE 8032.0205.024	–	–	Transformer
TR1, TR3	XT01	–	–	Common Mode Power Line Choke

Table 5 Bill of materials for the control card CD100001388

Designator	Value	Tolerance	Voltag	Description
C1, C2, C8, C18, C24, C26, C28, C31, C33, C35, C36, C42, C49, C50, C54, C59, C65, C66, C67, C68, C74, C75	100 nF	X7R	25 V	Capacitor ceramic
C3, C4, C40, C41	10 pF	X7R	50 V	Capacitor ceramic
C5	10 uF	X5R	25 V	Capacitor ceramic
C6, C9, C14, C15, C16, C17, C19, C45, C46, C47, C57, C58, C61, C63, C64, C71	330 pF	X7R	50 V	Capacitor ceramic
C7, C70, C72	100 pF	X7R	50 V	Capacitor ceramic
C10, C23, C25, C27, C30, C32, C34, C48, C55, C56, C69	10 uF	X5R	6.3 V	Capacitor ceramic
C43, C52	47 pF	X7R	50 V	Capacitor ceramic
C60, C62	4n7	X7R	50 V	Capacitor ceramic
D3, D7, D8, D9, D10, D12	BAT165	–	40 V	Schottky-diode
D5, D6, D11	GREEN LED	–	–	LED
IC1	**4DIR1400H**	–	–	**Integrated circuit**
IC2	**TLS4120D0EPV33**	–	–	**Synchronous step-down regulator**
IC3	**TLV1391IDBVR**	–	–	**Single differential Comparators**
IC4, IC10	**TLV2376IDR**	–	–	**Integrated circuit**
IC8	dsPIC33CK256MP 203-I/M5	–	–	MCU
IC11, IC12	LMH6642MF	–	–	Integrated circuit
IC13	**TLS820D0ELV33X UM**	–	–	**Low dropout linear voltage regulator**
IC14	**XMC4200-Q48K256**	–	–	**Integrated circuit**
L1	100uH	–	–	Magnetic
L2, L3	Ferrite bead 60Ohm@100MHz	–	–	Magnetic
NTC1	10K	1%	–	NTC Resistor
R1, R6, R11, R12, R17, R41, R44, R71, R72, R76, R77	510R	1%	–	Resistor
R2, R3, R4, R5, R34, R39, R43, R60, R69	15k	1%	–	Resistor
R7, R16, R23, R24, R26, R28	309k	0.1%	–	Resistor
R8, R9, R13, R15, R25, R47, R53	10k	0.1%	–	Resistor
R10, R30, R37, R42, R62	2k7	1%	–	Resistor
R14, R18, R19, R20, R45, R70	100R	1%	–	Resistor

Designator	Value	Tolerance	Voltag	Description
R21, R22, R27, R29	17k8	0.1%	–	Resistor
R31	1k	1%	–	Resistor
R48, R56, R57, R63, R65	4k99	0.1%	–	Resistor
R49, R52	124R	0.1%	–	Resistor
R50, R54, R58	49k9	0.1%	–	Resistor
R51, R55, R59	54k9	0.1%	–	Resistor
R66, R68, R73, R74	261R	1%	–	Resistor
R75	1R8	1%	–	Resistor
X1, X5	FTSH-105-01-L-DV-K	–	–	Connector
X2	TMM-113-03-L-D	–	–	Pin Header, 26 Contacts
X3	Fan connector	–	–	Pin Header, 4 Contacts
X4	TMM-106-03-L-D	–	–	Pin Header, 26 Contacts
X6	B2B-ZR	–	–	Connector
XTAL1	QT325S-12.000MEEQ-T	–	–	Crystal Oscillator

Table 6 Bill of materials for the secondary-side transformer PCB MG700003071

Designator	Value	Tolerance	Voltage	Description
C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11	4.7 uF	X8L	100 V	Capacitor Ceramic
C13, C14, C15, C16, C17, C18	1 uF	X7R	35 V	Capacitor Ceramic
D1, D2	**BAT46WJ**	–	**100 V**	**Schottky Diode**
IC1, IC2	**2EDB7259K**	–	–	**Gate driver IC**
R1, R2	2R2	1%	–	Resistor
R3, R4, R5, R6, R7, R8, R9, R10	1R	1%	–	Resistor
R11, R12	2k	1%	–	Resistor
T1, T2, T3, T4, T5, T6, T7, T8	IQE046N08LM5	–	80 V	MOSFET

7 Schematics

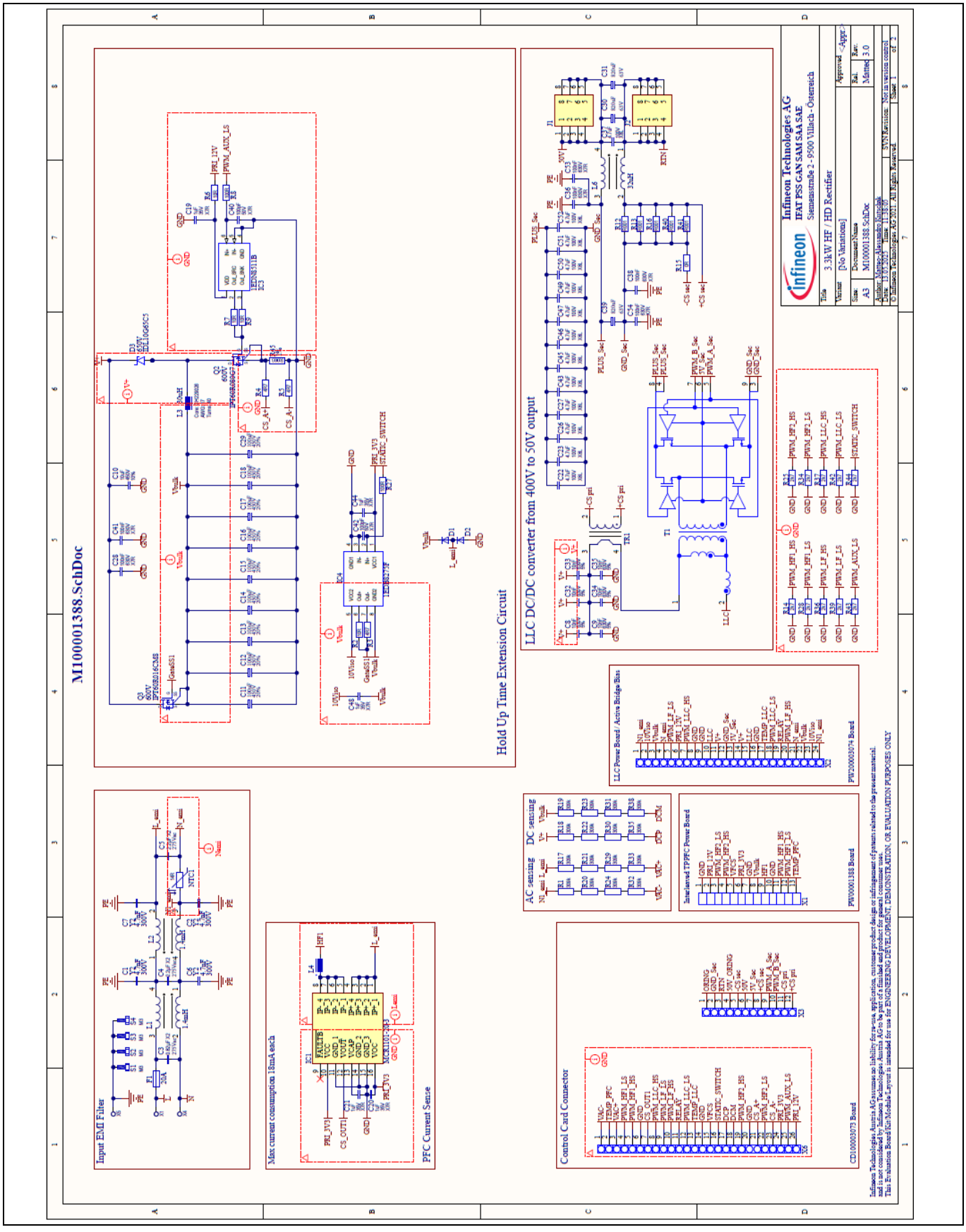

Figure 55 Schematic diagram of the main board (M100003074)

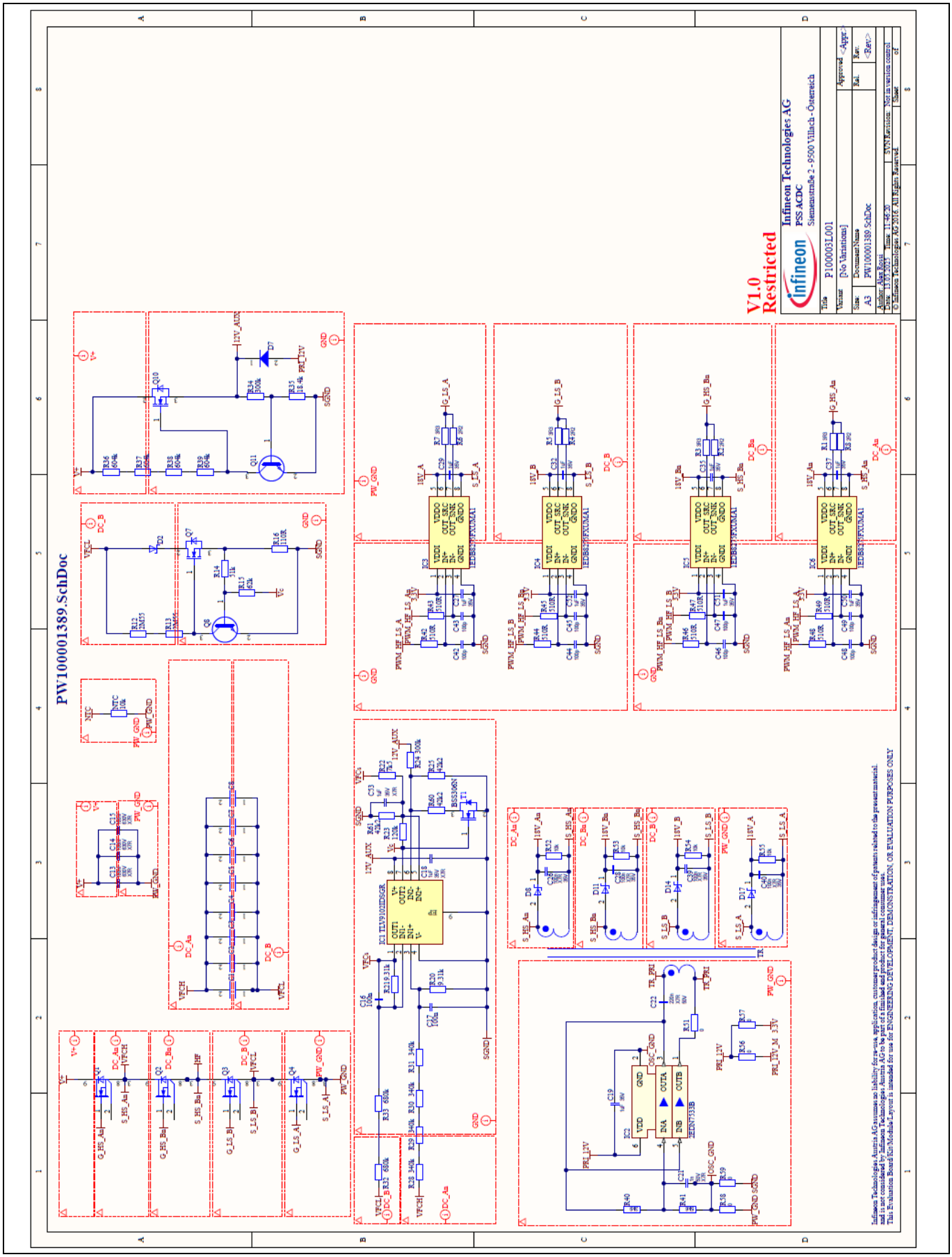

Figure 56 Schematic diagram of the ILTP-PFC high-frequency board (PW400003071)

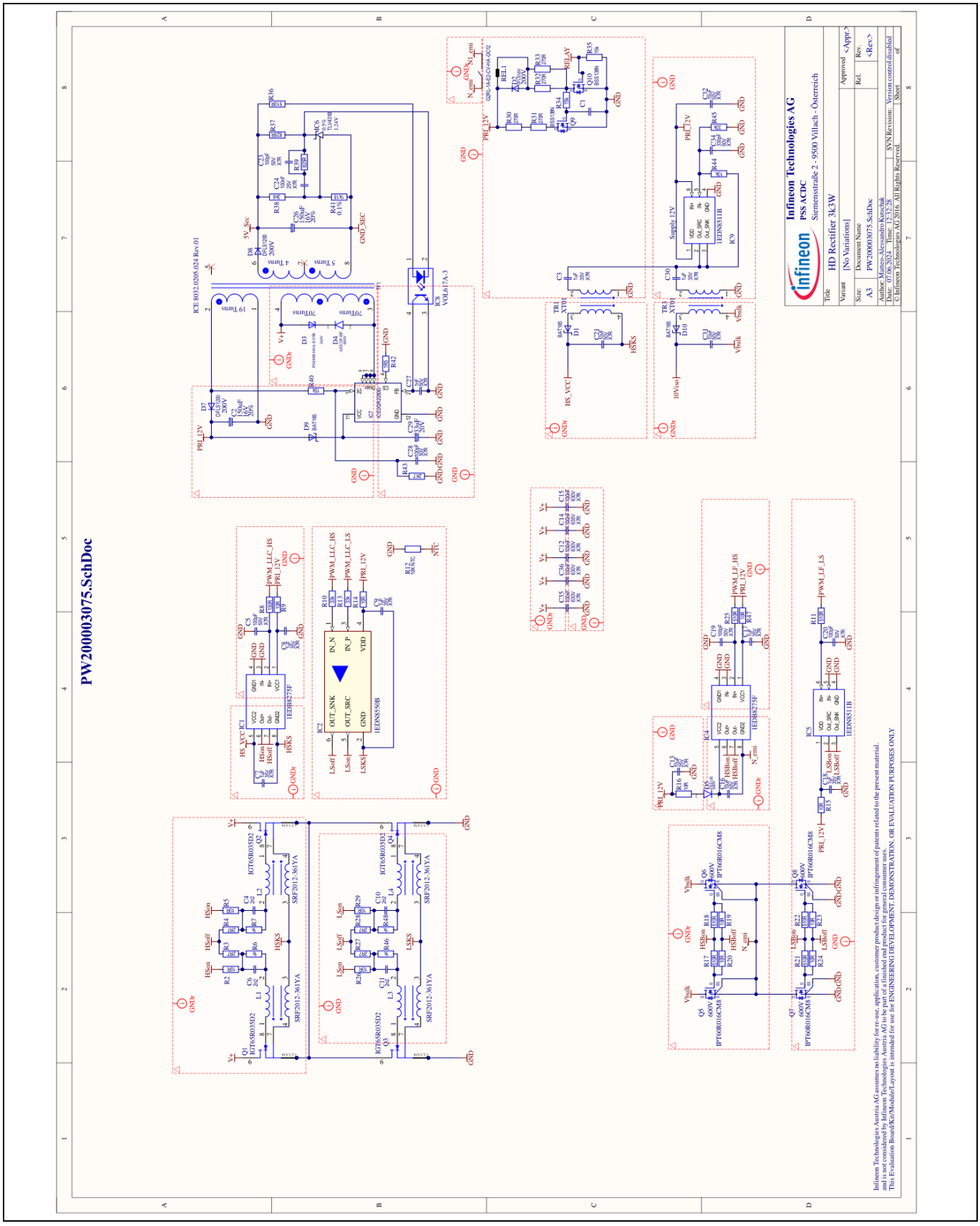

Figure 57 Schematic diagram of the LLC and PFC SR power card (PW200003075)

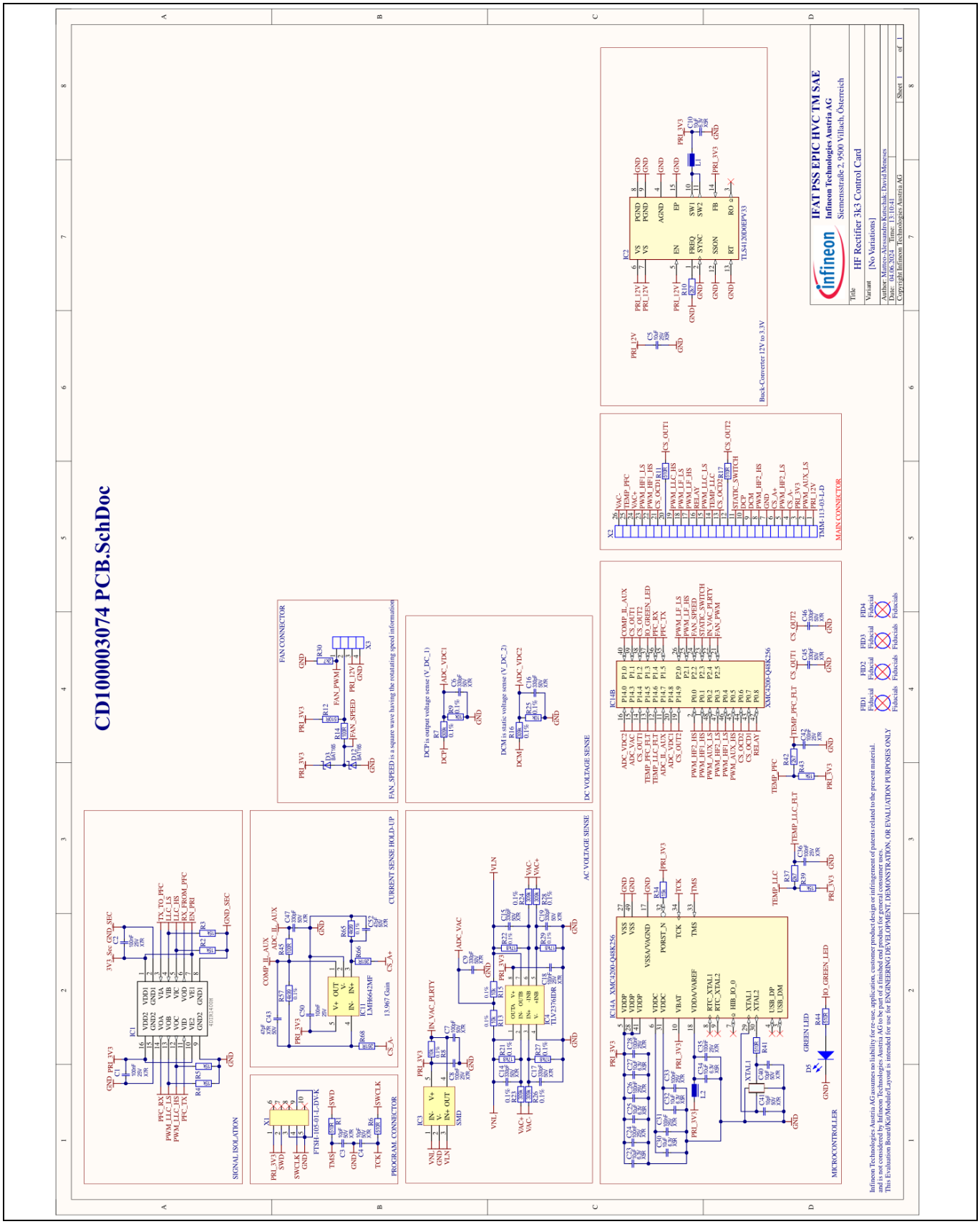

Figure 58 Schematic diagram of the control PCBA (CD100003074) – part 1: PFC control

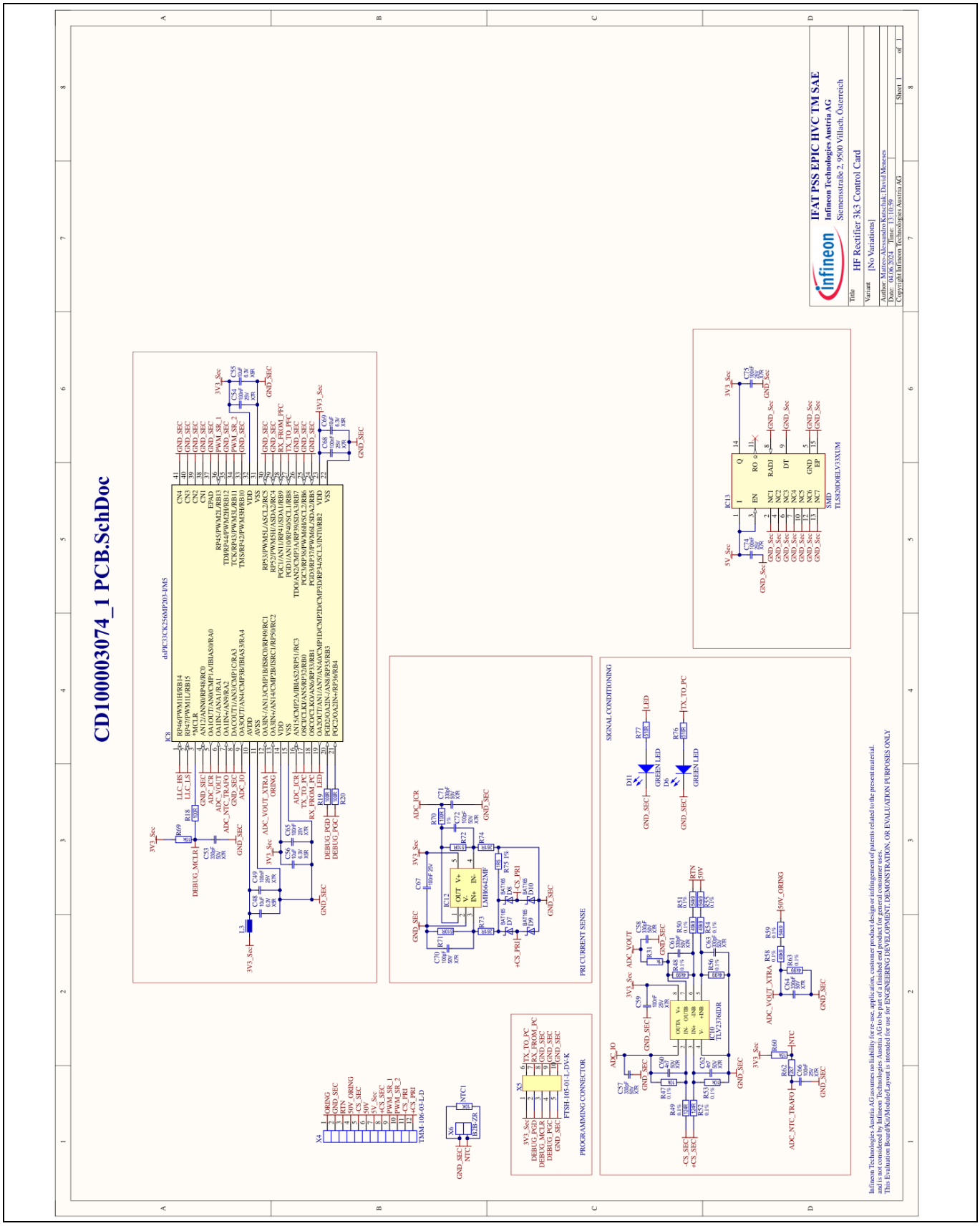

Figure 59 Schematic diagram of the control PCBA (CD100003074) – part 2: LLC control

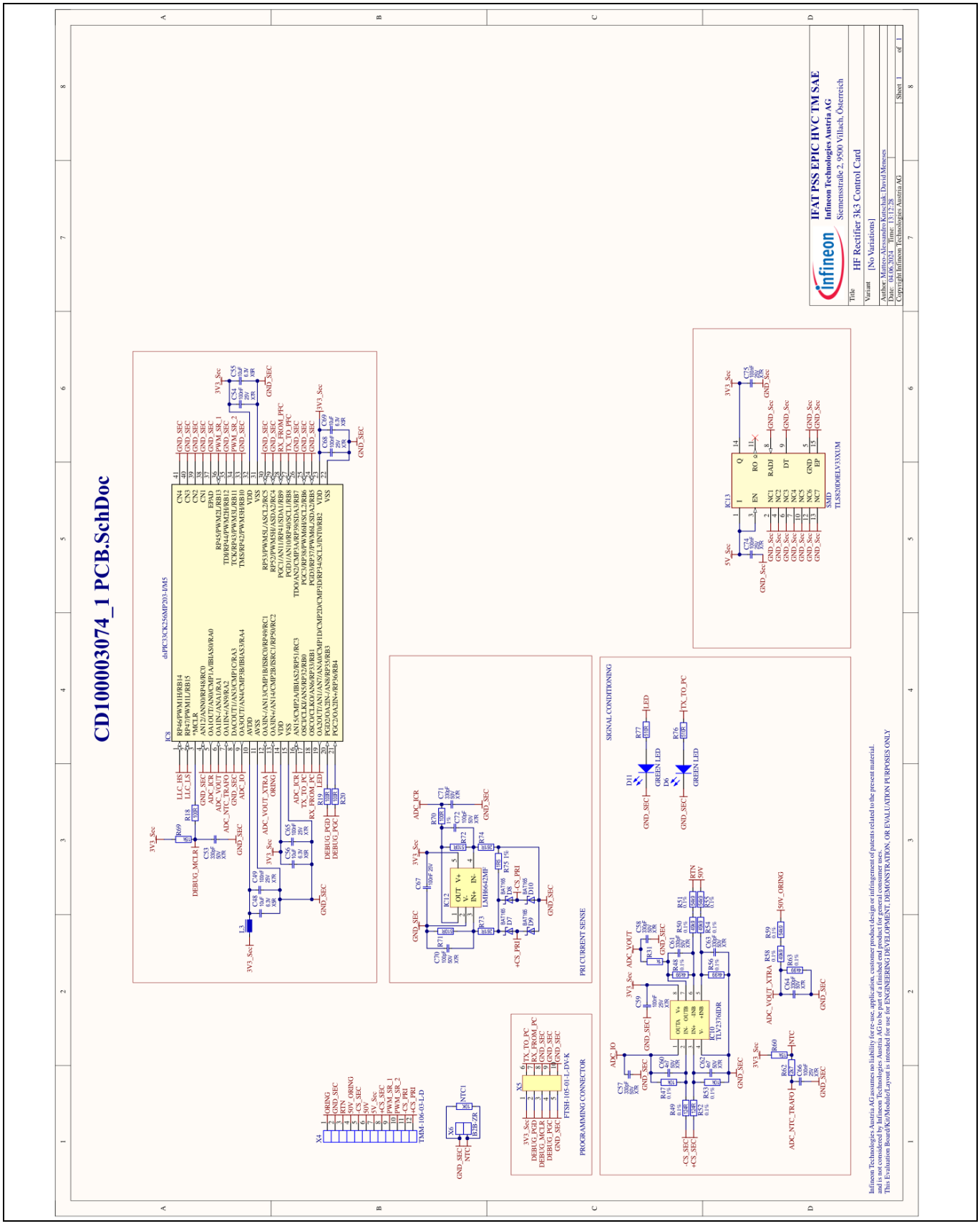

Figure 60 Schematic diagram of the secondary PCBs (MG700003071)

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Acronyms/abbreviations

Table 7 Acronyms/abbreviations

Acronym	Description
ACLDO	AC line-cycle dropout
BW	Bandwidth
BTM	Bottom
CCM	Continuous conduction mode
DFF	Duty-cycle feed-forward
FB	Full-bridge
GaN	Gallium nitride
HB	Half-bridge
HV	High voltage
iTHD	input current total harmonic distortion
LCDO	Line cycle drop out
LDO	Low dropout voltage regulator
LLC	Series parallel resonant converter
OCP	Overcurrent protection
OVP	Overvoltage protection
PF	Power factor
PFC	Power factor correction
PSU	Power supply unit
PWM	Pulse width modulation
Si	Silicon
SiC	Silicon carbide
SMPS	Switched mode power supply
SR	Synchronous rectification
THD	Total harmonic distortion
UVLO	Undervoltage lockout
UVP	Undervoltage protection
WBG	Wide-bandgap

Revision history

Document revision	Date	Description of changes
V 1.0	2025-06-20	Initial release

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