International
IOR Rectifier

APPLICATION NOTE

Application Note AN-999

International Rectifier's Total Dose Radiation Hardness Assurance (RHA) Test Program

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For many years, IR has been the leader in radiation hardened MOSFETs. The design and processing of these devices has been carefully planned and implemented to result in a superior product. The thorough hardness assurance testing imposed on our product is an important component of this product line which has been overlooked by many in the industry. The philosophy behind the hardness assurance testing is based on the military requirements outlined in MIL-PRF-19500 and its associated detail slash sheets. IR has elected to exceed the military requirement and is currently using sampling plans as much as 2 times greater than is required.

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Baseline Requirements

MIL-PRF-19500 and the detail slash sheets work hand-in-hand to establish the required tests for radiation hardness assurance. MIL-PRF-19500 sets the sampling rate based upon the maximum number of die per wafer as shown in Table 1.

DIE per WAFER (MAXIMUM)	SAMPLES per WAFER per Bias
≥ 4000	4
> 500 < 4000	2
≤ 500	1

Table 1

The detail slash sheets specify the VGS and VDS bias schemes. Thus the actual samples required to meet a given slash sheet requirement is twice that indicated in Table 1. IR offers four RAD HARD die sizes each fabricated with 5 inch wafers. Die size 5 and 6 are fabricated with maximum die counts of less than 500 per wafer. Die size 3 and 1 are fabricated with maximum die counts of between 500 and 4000 per wafer. Accordingly, the required sample size to meet the slash sheet requirements is two die per wafer for size 5 and 6 die, and four die per wafer for size 1 and 3 die.

IR Guidelines

The RHA test process is charted in the attached flowchart, Figure 1. IR is currently sampling each wafer at a rate of 4 die per wafer, i.e. 2 die per wafer per bias. An example of typical data is attached for reference, Figure 2. Given the large number of wafers per lot this quickly becomes an enormous sample, a resource of data which helps the engineering staff understand and improve the product line. Each sample is tested prior to irradiation. The data from this test and all post-irradiation testing is logged and stored in a database for "post-processing." The samples are irradiated in accordance with MIL-STD-750 test method 1019, condition A. Test method 1019 specifies the dose rate, test temperature, test window, and other parameters critical to total dose irradiation.

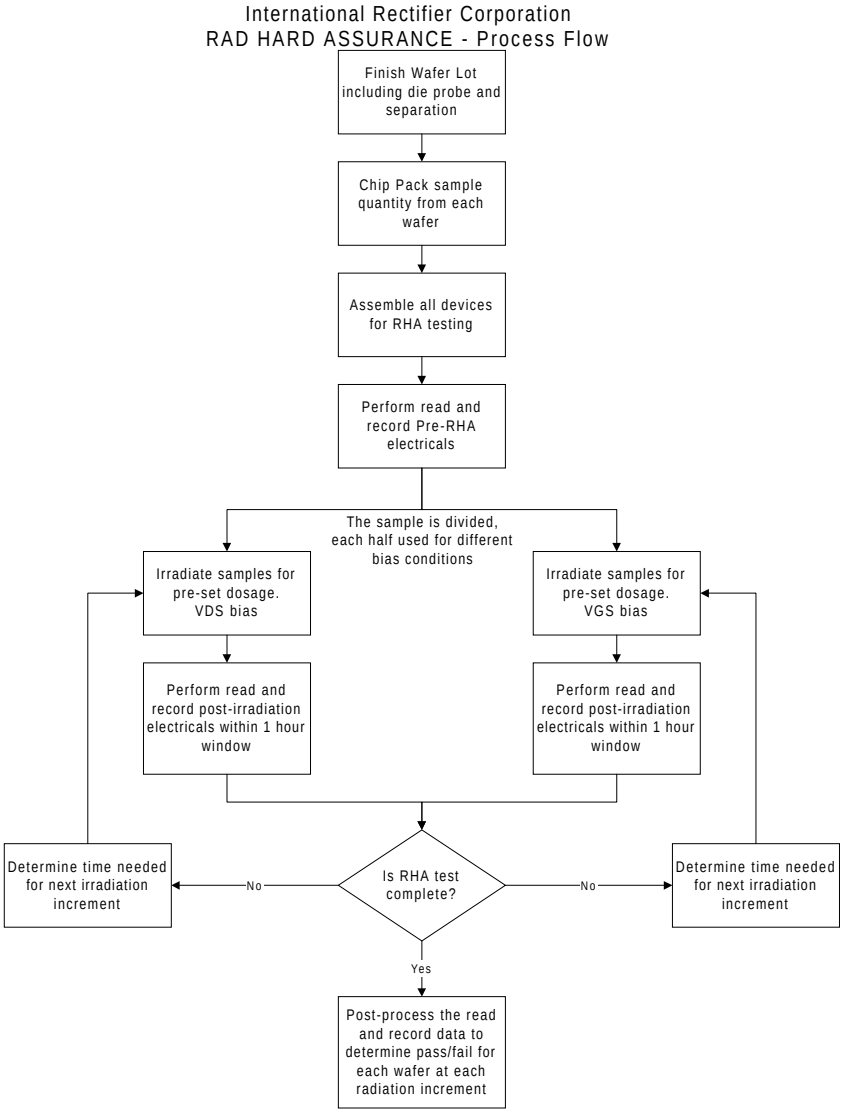
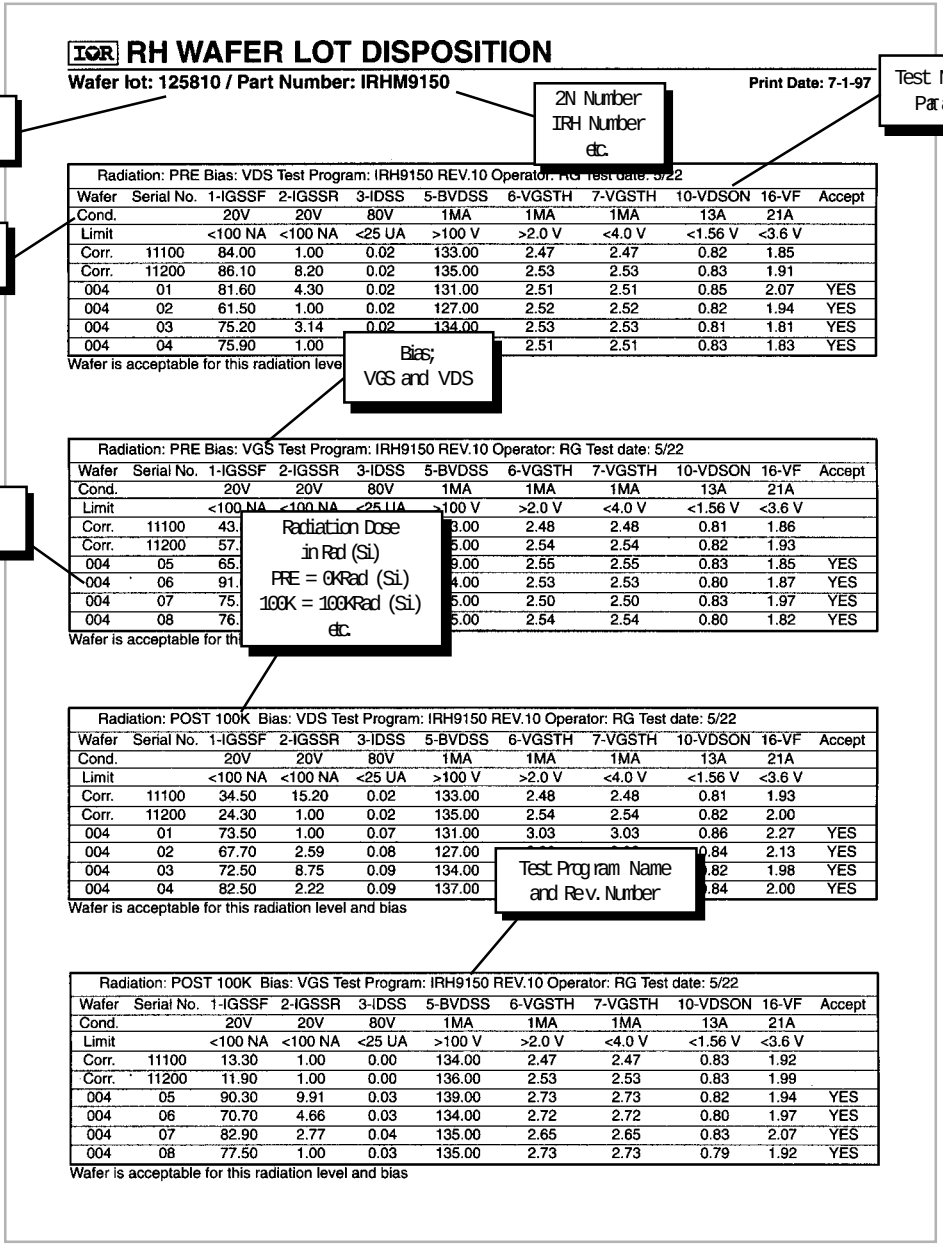


Figure 1

Samples are continued to higher levels of irradiation and subsequent testing according to the wafer fabrication process under consideration. For example, the SEE hardened process has a total dose capability of 100Krad (Si). IR will test all samples from SEE hardened wafers at 0, 50, and 100Krad (Si). The N channel MEGA RAD HARD process samples are irradiated and tested at 0, 100, 300, 600 and 1000Krad (Si). Finally, the P channel MEGA RAD HARD process samples are irradiated at 0, 100 and 300Krad (Si). Given the test program consists of several parametric tests, an N channel wafer lot can easily result in more than 100,000 data points. As already noted this data is post-processed to determine the hardness of each



Radiation: PRE Bias: VDS Test Program: IRH9150 REV.10 Operator: RG Test date: 5/22

Wafer	Serial No.	1-IGSSF	2-IGSSR	3-IDSS	5-BVDSS	6-VGSTH	7-VGSTH	10-VDSON	16-VF	Accept
Cond.		20V	20V	80V	1MA	1MA	1MA	13A	21A	
Limit		<100 NA	<100 NA	<25 UA	>100 V	>2.0 V	<4.0 V	<1.56 V	<3.6 V	
Corr.	11100	84.00	1.00	0.02	133.00	2.47	2.47	0.82	1.85	
Corr.	11200	86.10	8.20	0.02	135.00	2.53	2.53	0.83	1.91	
004	01	81.60	4.30	0.02	131.00	2.51	2.51	0.85	2.07	YES
004	02	61.50	1.00	0.02	127.00	2.52	2.52	0.82	1.94	YES
004	03	75.20	3.14	0.02	134.00	2.53	2.53	0.81	1.81	YES
004	04	75.90	1.00			2.51	2.51	0.83	1.83	YES

Wafer is acceptable for this radiation leve

Radiation: PRE Bias: VGS Test Program: IRH9150 REV.10 Operator: RG Test date: 5/22

Wafer	Serial No.	1-IGSSF	2-IGSSR	3-IDSS	5-BVDSS	6-VGSTH	7-VGSTH	10-VDSON	16-VF	Accept
Cond.		20V	20V	80V	1MA	1MA	1MA	13A	21A	
Limit		<100 NA	<100 NA	<25 UA	>100 V	>2.0 V	<4.0 V	<1.56 V	<3.6 V	
Corr.	11100	43.			3.00	2.48	2.48	0.81	1.86	
Corr.	11200	57.			5.00	2.54	2.54	0.82	1.93	
004	05	65.			9.00	2.55	2.55	0.83	1.85	YES
004	06	91.			4.00	2.53	2.53	0.80	1.87	YES
004	07	75.			5.00	2.50	2.50	0.83	1.97	YES
004	08	76.			5.00	2.54	2.54	0.80	1.82	YES

Wafer is acceptable for th

Radiation: POST 100K Bias: VDS Test Program: IRH9150 REV.10 Operator: RG Test date: 5/22

Wafer	Serial No.	1-IGSSF	2-IGSSR	3-IDSS	5-BVDSS	6-VGSTH	7-VGSTH	10-VDSON	16-VF	Accept
Cond.		20V	20V	80V	1MA	1MA	1MA	13A	21A	
Limit		<100 NA	<100 NA	<25 UA	>100 V	>2.0 V	<4.0 V	<1.56 V	<3.6 V	
Corr.	11100	34.50	15.20	0.02	133.00	2.48	2.48	0.81	1.93	
Corr.	11200	24.30	1.00	0.02	135.00	2.54	2.54	0.82	2.00	
004	01	73.50	1.00	0.07	131.00	3.03	3.03	0.86	2.27	YES
004	02	67.70	2.59	0.08	127.00			0.84	2.13	YES
004	03	72.50	8.75	0.09	134.00			.82	1.98	YES
004	04	82.50	2.22	0.09	137.00			.84	2.00	YES

Wafer is acceptable for this radiation level and bias

Radiation: POST 100K Bias: VGS Test Program: IRH9150 REV.10 Operator: RG Test date: 5/22

Wafer	Serial No.	1-IGSSF	2-IGSSR	3-IDSS	5-BVDSS	6-VGSTH	7-VGSTH	10-VDSON	16-VF	Accept
Cond.		20V	20V	80V	1MA	1MA	1MA	13A	21A	
Limit		<100 NA	<100 NA	<25 UA	>100 V	>2.0 V	<4.0 V	<1.56 V	<3.6 V	
Corr.	11100	13.30	1.00	0.00	134.00	2.47	2.47	0.83	1.92	
Corr.	11200	11.90	1.00	0.00	136.00	2.53	2.53	0.83	1.99	
004	05	90.30	9.91	0.03	139.00	2.73	2.73	0.82	1.94	YES
004	06	70.70	4.66	0.03	134.00	2.72	2.72	0.80	1.97	YES
004	07	82.90	2.77	0.04	135.00	2.65	2.65	0.83	2.07	YES
004	08	77.50	1.00	0.03	135.00	2.73	2.73	0.79	1.92	YES

Wafer is acceptable for this radiation level and bias

Figure 2

wafer. All samples from a wafer must pass the parametric limits for qualification at a specific hardness assurance level. For example, a wafer sample consisting of 8 devices may pass all tests at 0, 100 and 300Krad (Si), yet if one device fails the VGS(th) at 600Krad (Si) the wafer will only be qualified to 300Krad (Si). The parametric test limits and thus the acceptability of each wafer are controlled by the slash sheet or customer SCD, depending on the amount of parametric shifting allowed in the design.

Summary

Samples are built, tested and evaluated to qualify each wafer produced. The resultant data is stored, analyzed and used to improve the process capability. This data is also provided to customers in the test report accompanying the deliverable units.