# 3.3 kW ARCP topology for high-efficiency and high-density PSU in server and data center applications

## EVAL_3K3W_ARCP_PSU

## About this document

### Scope and purpose

EVAL_3K3W_ARCP_PSU introduces a complete system solution from Infineon for a high-power density 3.3 kW power supply unit (PSU), which targets specifications for server and data center applications utilizing the ARCP topology.

This document describes the converter hardware, provides a summary of the experimental results and design recommendations for the complete Infineon solution, including an innovative planar magnetic construction. The EVAL_3K3W_ARCP_PSU comprises a front-end AC-DC converter and a back-end isolated DC-DC converter.

The front-end AC-DC converter is a CoolGaN™ auxiliary resonant commutated pole bridgeless totem pole (ARCP-TP) stage that provides power factor correction (PFC) and limits total harmonic distortion (THD). The back-end DC-DC is a CoolGaN™ half-bridge (HB) LLC converter with full-bridge (FB) rectification, which provides safety isolation and regulates the output voltage. The PSU also features a baby-boost converter to comply with the hold-up time specifications of server applications with a reduced overall bulk capacitance, increasing the overall power density.

The measured peak efficiency of the complete PSU at 230 $V_{AC}$ input line is 97.82% including the internal fan. It yields a power density of 98 W/inch$^3$ within a compact 72 mm x 192 mm x 40 mm outer frame.

### Intended audience

The document and the related EVAL_3K3W_ARCP_PSU hardware is intended for R&D engineers, hardware designers, and developers of power electronic systems.

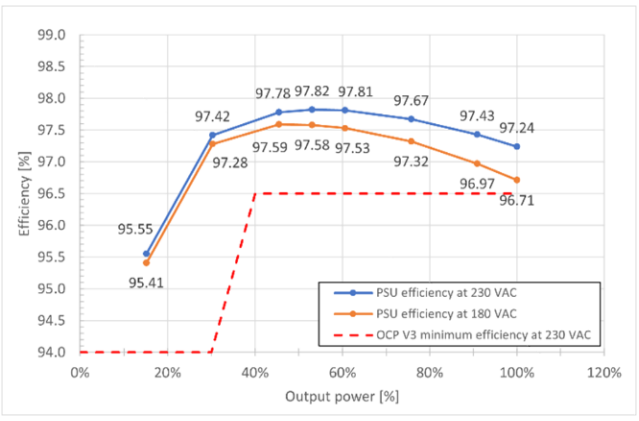


**Figure 1 3.3 kW EVAL_3K3W_ARCP_PSU server power supply overview and measured efficiency**

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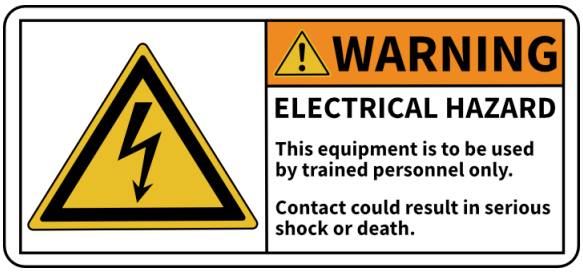
## Safety information

**Please read this document carefully before starting up the device.**





## Important notice

Evaluation boards, demonstration boards, reference boards and kits are electronic devices typically provided as an open-frame and unenclosed printed circuit board (PCB) assembly. Each board is functionally qualified by electrical engineers and strictly intended for use in development laboratory environments. Any other use and/or application is strictly prohibited. Our boards and kits are solely for qualified and professional users who have training, expertise, and knowledge of electrical safety risks in the development and application of high-voltage electrical circuits. Please note that evaluation boards, demonstration boards, reference boards and kits are provided “as is” (i.e., without warranty of any kind). Infineon is not responsible for any damage resulting from the use of its evaluation boards, demonstration boards, reference boards or kits. To make our boards as versatile as possible, and to give you (the user) opportunity for the greatest degree of customization, the virtual design data may contain different component values than those specified in the bill of materials (BOM). In this specific case, the BOM data has been used for production. Before operating the board (i.e. applying a power source), please read the application note/user guide carefully and follow the safety instructions. Please check the board for any physical damage, which may have occurred during transport. If you find damaged components or defects on the board, do not connect it to a power source. Contact your supplier for further support. If no damage or defects are found, start the board up as described in the user guide or test report. If you observe unusual operating behavior during the evaluation process, immediately shut off the power supply to the board and consult your supplier for support.

### Operating instructions

Do not touch the device during operation, keep a safe distance. Do not touch the device after disconnecting the power supply, as several components may still store electrical voltage and can discharge through physical contact. Several parts, like heatsinks and transformers, may still be very hot.  Allow the components to discharge and cool before touching or servicing. All work such as construction, verification, commissioning, operation, measurements, adaptations, and other work on the device (applicable national accident prevention rules must be observed) must be done by trained personnel. The electrical installation must be completed in accordance with the appropriate safety requirements.

## Safety precautions

*Note:* *Please note the following warnings regarding the hazards associated with development systems.*

**Table 1 Safety precautions**

| | |
|---|---|
|  | **Warning:** *The evaluation or reference board contains DC bus capacitors, which take time to discharge after removal of the main supply. Before working on the converter system, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.* |
|  | **Warning:** *The evaluation or reference board is connected to the AC input during testing. Hence, high-voltage differential probes must be used when measuring voltage waveforms by oscilloscope. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.* |
|  | **Warning:** *Remove or disconnect power from the converter before you disconnect or reconnect wires, or perform maintenance work. Wait five minutes after removing power to discharge the bus capacitors. Do not attempt to service the drive until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.* |
|  | **Caution:** *The heatsink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.* |
|  | **Caution:** *Only personnel familiar with the converter, power electronics and associated equipment should plan, install, commission, and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.* |
|  | **Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.* |
|  | **Caution:** *A converter that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as undersizing the cabling, supplying an incorrect or inadequate AC supply, or excessive ambient temperatures may result in system malfunction.* |

# 1 Background and board overview

Recently, rack level power demand in servers and data centers has grown substantially to accommodate the higher computing workload in limited rack space. This increased power demand is consistently tightening power density and efficiency requirements in power supplies – to reduce the space occupied and the heat dissipated.

These requirements can be observed in the OCP rectifier v3 specification for server and datacenter PSU [1]. In terms of efficiency and power density, a 97.5% peak efficiency at 230 $V_{AC}$ is required, with additional requirements of a minimum power density of 32.15 W/inch$^3$ (1.96 W/cm$^3$), 520 mm × 73.5 mm × 40 mm maximum dimensions, and 20 ms hold-up time at full power. Infineon's previous design, EVAL_3KW_50V_PSU [2], met all these specifications. Infineon's REF_3K3W_HFHD_PSU [3] further improved upon it by increasing the power density to close to 100 W/in$^3$.

EVAL_3K3W_ARCP_PSU showcases an enhanced full system efficiency. The AC-DC front-end of the server PSU implements a totem-pole (TP) PFC with auxiliary resonant commutated pole (ARCP), which guarantees soft-switching (ZVS) operation. The LLC keeps the same structure as REF_3K3W_HFHD_PSU, with some improvements implemented in the transformer structure and LLC devices to further improve efficiency.

## 1.1 Power supply unit description

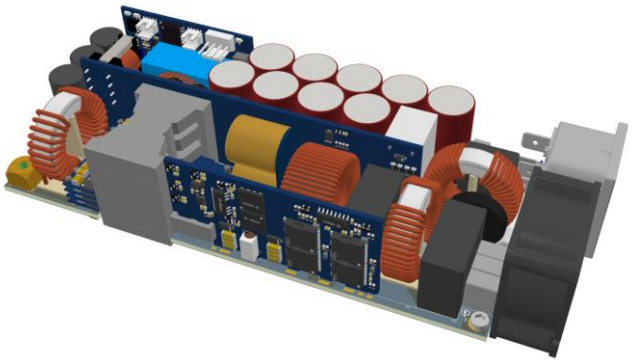
EVAL_3K3W_ARCP_PSU (Figure 2) includes a front-end AC-DC converter and a back-end isolated DC-DC converter.

- The front-end AC-DC converter is an auxiliary resonant commutated pole totem-pole PFC stage that provides PFC and limits THD
- The back-end DC-DC is a GaN half-bridge LLC converter with full-bridge rectification – it provides safety isolation and regulates the output voltage
- It also features a baby-boost converter to comply with the hold-up time specifications of server applications

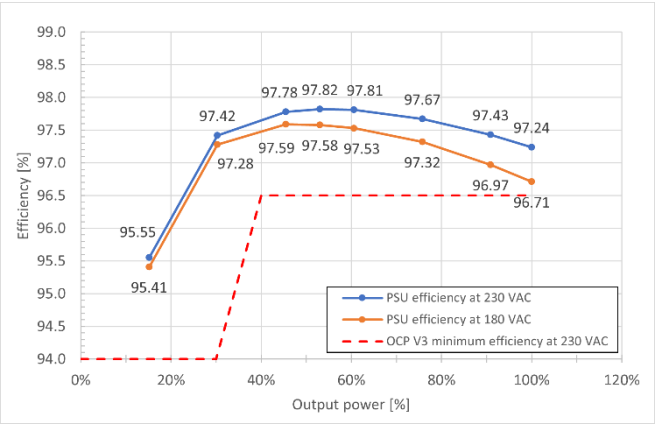
The soft-switching PFC topology and the optimized LLC converter leads to an increased overall efficiency of the PSU compared to its predecessors.

The measured peak efficiency of the complete PSU at 230 $V_{AC}$ input line is 97.82% (Figure 2), (97.96% excluding the internal fan consumption) and overall outer dimensions of 72 mm × 192 mm × 40 mm, yielding a 98 W/inch$^3$ power density.

## Background and board overview



(a)




(b)

**Figure 2 3.3 kW EVAL_3K3W_ARCP_PSU (a) and its efficiency curves (b)**

*Note: In EVAL_3K3W_ARCP_PSU, the ACDC and DCDC blocks share power earth (PE) via the metallic chassis and cooling is done via piping of the airflow by means of the plastic enclosure. For electrical safety and cooling reasons, it is therefore, recommended not to operate the board without enclosure or chassis. It is the user's responsibility to ensure proper cooling and connections when operating the unit outside of the recommended operating conditions.*

The main Infineon components used in EVAL_3K3W_ARCP_PSU are:

- CoolGaN™ IGT65R035D2 transistor, 650 V G5 35 mΩ TOLL, and EiceDRIVER™ 2EDB8259Y for the fast-legs of the totem-pole PFC converter
- CoolGaN™ IGLD65R055D2 transistor, 650 V G5, 55 mΩ PG-LSON-8-1, and 2EDB8259Y for the resonant pole of the totem-pole PFC converter
- CoolMOS™ IPT60R016CM8 MOSFET, 600 V CM8 16 mΩ TOLL, EiceDRIVER™ 1EDN8511B for the slow leg of the totem-pole PFC converter, and EiceDRIVER™ 1EDB8275F
- CoolGaN™ IGT65R035D2 transistor, 650 V GIT 35 mΩ TOLL, EiceDRIVER™ 1EDN8550B, and 1EDB8275F for HB switches at the primary side of the LLC converter
- OptiMOS™ IQE031N08LM6CG MOSFET, 80 V 3.3 mΩ source-down, and EiceDRIVER™ 2EDB7259K for the synchronous rectification (SR) switches at the secondary-side of the LLC converter
- CoolMOS™ IPT60R080G7 MOSFET, 600 V G7 80 mΩ, and CoolSiC™ IDL10G65C5, 600 V diode, and EiceDRIVER™ 1EDB8275F for the baby-boost converter
- ISOFACE™ 4DIR1400H digital isolator for the primary to secondary isolation in the LLC converter
- XMC4200-Q48K256 microcontroller for the implementation of the PFC control
- CoolSET™ ICE2QR2280G, 800 V quasi-resonant flyback controller

The evaluation board EVAL_3K3W_ARCP_PSU is mounted over a metallic frame and covered by a plastic enclosure to ensure proper airflow and cooling. Its dimensions are 192 mm × 72 mm × 40 mm, including a fan and an AC inlet connector. For comparison, OCP v3 specifies a maximum dimension of 520 mm × 73.5 mm × 40 mm). Overall, the PSU offers a power density of 98 W/inch$^3$.

## EVAL_3K3W_ARCP_PSU

### Background and board overview

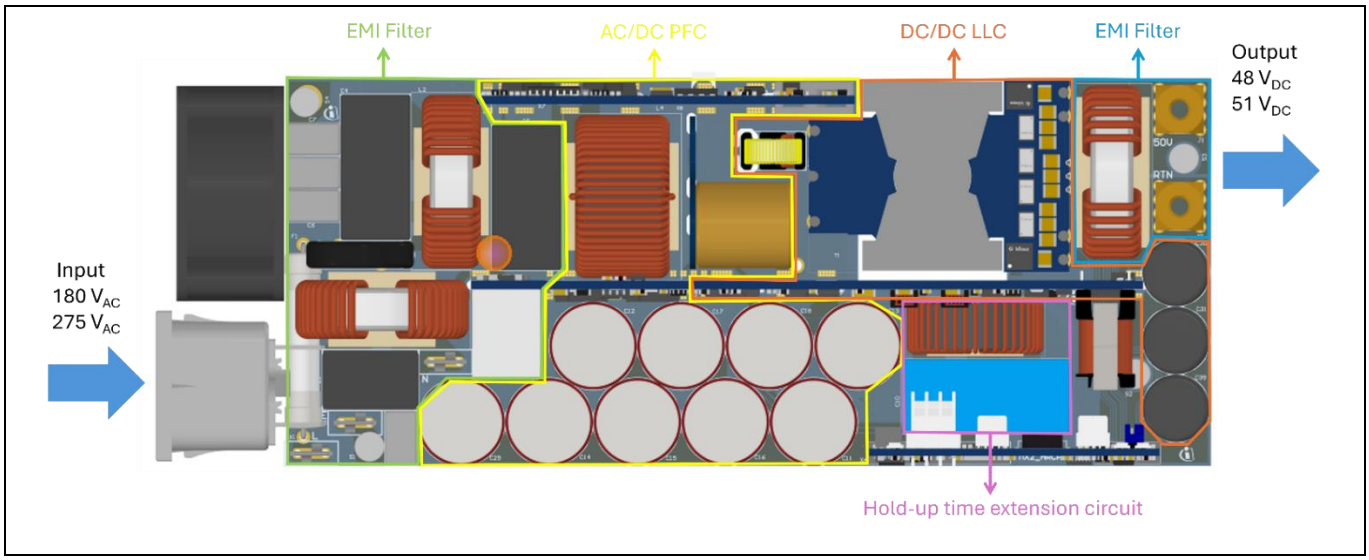



**Figure 3 Overview of EVAL_3K3W_ARCP_PSU**

To achieve the power density target, a tri-dimensional mechanical assembly is necessary and multiple daughterboards are assembled on the main PCB, as shown in Figure 4.

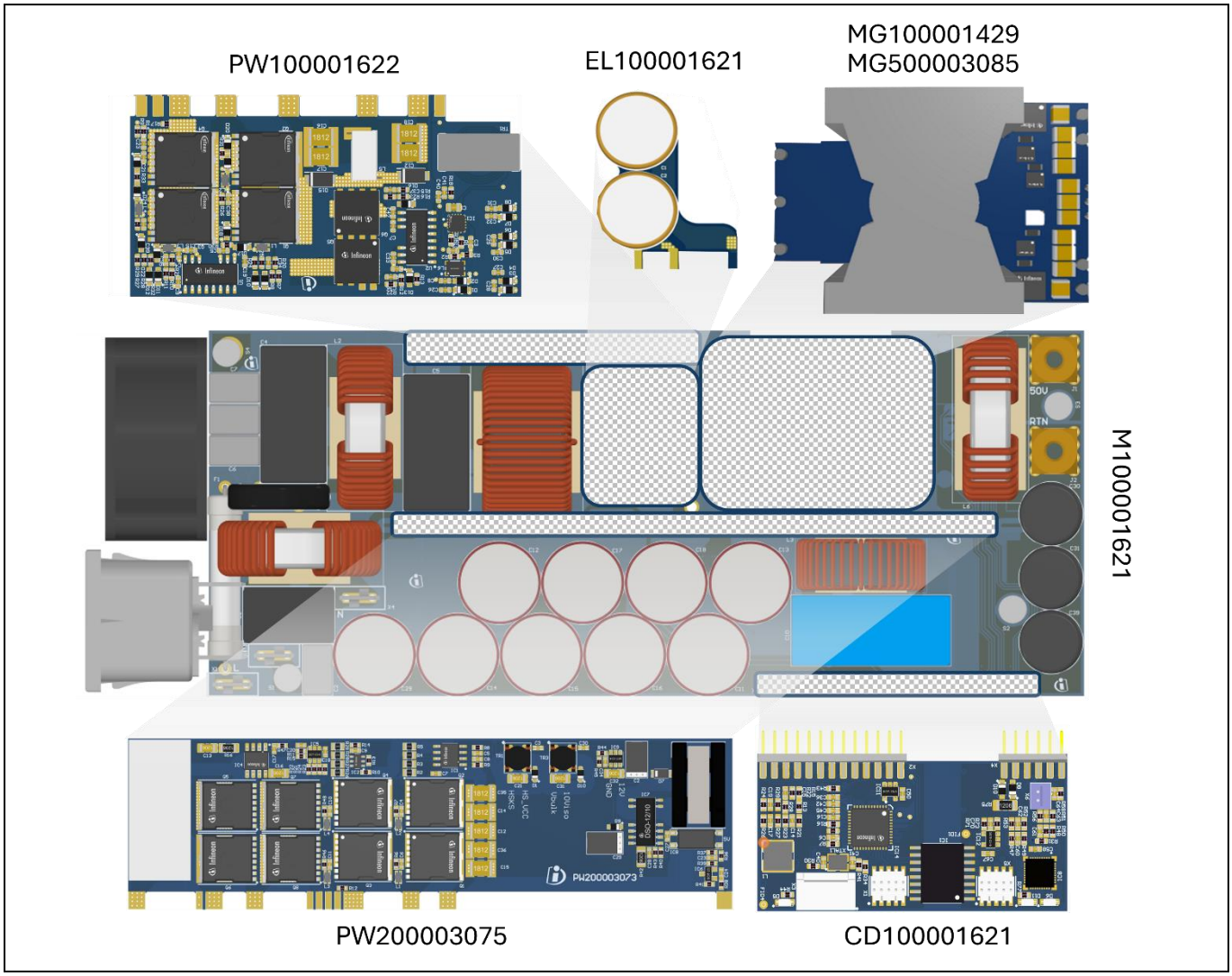



**Figure 4 EVAL_3K3W_ARCP_PSU main board and daughterboards with their assembly**

The following daughterboards are used:

- The main board, M1000001621, hosts the passive components of the input and output EMI filters, the PFC inductor choke, the capacitors of the intermediate bulk, and provides mechanical support and electrical connections for the daughterboards
- The ARCP-TP-PFC high-frequency board, PW100001622, is a daughterboard encompassing the high-frequency leg of the PFC and the resonant pole components, mounted perpendicular to the main board
- The LLC and PFC SR power card, PW200003075, is assembled in the center of the board, and hosts the PFC SR stage, the LLC primary-side, the in-rush relay and the flyback power supply for housekeeping
- The planar primary and secondary PCBs, MG500003085 and MG100001429, are embedded in the transformer structure for primary- and secondary-side planar windings
- The control PCB (CD100001621) hosts the two primary- and secondary-side controllers and provides isolation to the UART communication channel and the PWM of the LLC HB MOSFETs. The fan airflow sucks the air out of the chassis for better thermal performance.

## 1.2 Converter architecture

EVAL_3K3W_ARCP_PSU is a unidirectional PSU consisting of two stages; Figure 5 shows its simplified block diagram.

- A front-end auxiliary resonant commutated pole totem-pole AC-DC converter that provides PFC and THD
- A half-bridge LLC DC-DC converter that provides safety isolation and regulated output

The control of the totem-pole AC-DC converter is implemented using Infineon XMC™ 4200 MCU with PFC, THD, voltage regulation, overcurrent protection (OCP), overvoltage protection (OVP), undervoltage protection (UVP), undervoltage lockout (UVLO), soft-start, synchronous rectification (SR) control, adaptive dead-times, and serial communication interface towards the LLC secondary-side controller. This controller is also responsible for the calculation of the ARCP timings and application of the required PWM pattern to obtain ZVS operation with a minimized current in the ARCP inductor.

The control of the LLC converter is implemented with a third-party MCU referenced to the secondary-side ground, and features voltage-regulation functionality, burst-mode operation, output OCP, OVP, UVP, UVLO, soft-start, SR control, adaptive dead-times, and a serial communication interface. The isolation between the two controllers (UART communication and PWM signals for the primary-side HB of the LLC) is managed using a quad-channel digital isolator.

In the front-end AC-DC converter, the high-frequency HB leg uses four 35 mΩ 650 V CoolGaN™ switches in total, two of each placed in parallel, driven by two EiceDRIVER™ 2EDB8259Y gate drivers, while the back-to-back switches are CoolGaN™ 650 V 55 mΩ switches. The low-frequency leg uses four 16 mΩ 600 V CoolMOS™ 8 switches in parallel with a combination of EiceDRIVER™ 1EDB8275F and EiceDRIVER™ 1EDN8115B in a hybrid configuration.

The LLC converter uses four CoolGaN™ 650 V, 35 mΩ switches for the HB HV primary-side with a combination of EiceDRIVER™ 1EDB8275F and EiceDRIVER™ 1EDN8550B gate drivers. For the secondary-side SR, an integrated approach is followed – the SR MOSFETs are mounted on the secondary-side PCB windings and integrated on the same magnetic structure that realizes the main transformer, resonant inductance, and magnetizing inductance. The LLC SR stage uses 32 instances of the 3.1 mΩ OptiMOS™ 6 power transistor, driven by eight EiceDRIVER™ 2EDB7259K. See 3.3 for more information about the integrated transformer assembly.

To ensure hold-up time specifications are met while reducing the amount of bulk capacitance of the PSU, a baby-boost converter is used to decouple the bulk voltage from the LLC input during the hold-up event. During steady-state operation, the baby-boost is bypassed by a low-ohmic CoolMOS™ 8 16 mΩ, 600 V switch.

## EVAL_3K3W_ARCP_PSU

## Background and board overview

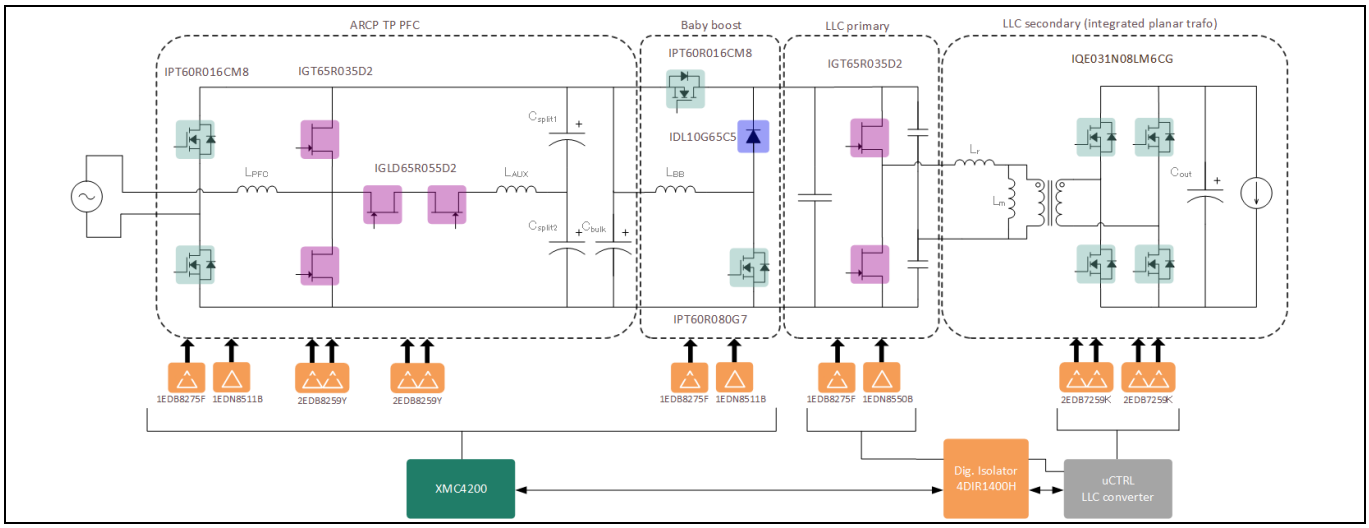



**Figure 5 Simplified schematic of EVAL_3K3W_ARCP_PSU**

# 2 Auxiliary resonant commutated pole TP PFC

A simplified schematic of the ARCP totem-pole PFC stage of EVAL_3K3W_ARCP_PSU is shown in Figure 6. The AC inlet is followed by a two-stage input EMI filter and the inrush limitation circuit. The AC line is connected to the high-frequency CoolGaN™ fast-leg of the totem-pole PFC ($Q_{HS}$, $Q_{LS}$ ) via the PFC-inductor while its neutral wire is connected to the SR leg of the converter ($Q_{SR\_HS}$ and $Q_{SR\_LS}$). The high-frequency CoolGaN™ half-bridge with parallel devices operates at 135 kHz switching frequency, whereas the SR half-bridge rectifies the AC current according to the detected line voltage polarity. Two capacitors are in a series through the bulk to provide half of the bulk voltage nominally. $Q_{BB1}$ and $Q_{BB2}$ are back-to-back switches connected between the switching node of the half-bridge and an inductor connected to the split capacitors. They provide the required charge to achieve soft switching in the totem-pole switches.

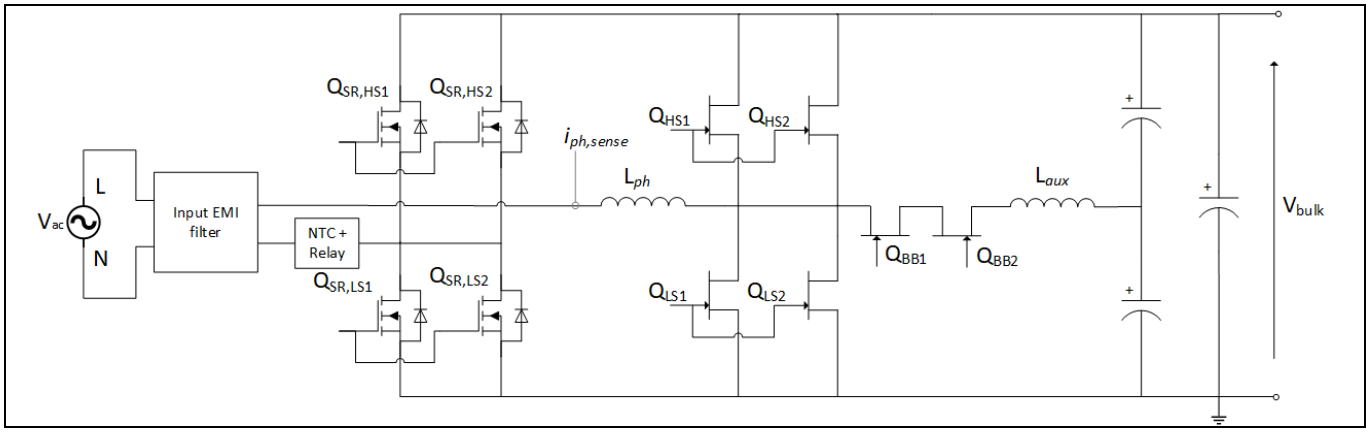



**Figure 6 Simplified schematic of the ARCP totem-pole AC-DC converter in EVAL_3K3W_ARCP_PSU**

## 2.1 ARCP operation and design

The ARCP has historically been used in inverter applications. However, due to the advances in wide-bandgap power switches such as CoolGaN™ and CoolSiC™, it is now feasible to use it in the PFC stage of an SMPS.

In the fast-switching leg of a standard totem-pole PFC, the transition from switch to diode is soft-switched, while the transition from diode to switch is hard-switched. This second transition generates losses which scale with the switching frequency, impacting the efficiency.

By adding the ARCP to the TP PFC, the diode to switch transition becomes soft-switched. This reduces the switching losses of the topology to near zero, which increases efficiency. It is also possible to increase the switching frequency of the PFC due to a reduced thermal stress in the switches. This allows minimization of the PFC choke.

Figure 7 shows the basic operation of the topology in the diode to switch transition for the positive AC halfwave. First, when the current needs to be removed from the boost diode (I), the back-to-back switches turn on until the current in the auxiliary inductor matches the current in the PFC choke (II). This reduces the current in the boost diode (top-side switch) and have a zero current switching (ZCS) turn-off event.

Once the diode is turned off, the current in the auxiliary switch pushes the midpoint of the half bridge downwards, creating a resonance between the $C_{oss}$ of the half-bridge switches and the auxiliary inductor. Due to the resonance, the voltage of the midpoint reaches zero volts, where the bottom-side switch turns on in a zero voltage switching (ZVS) turn-on event. The current in the auxiliary inductor is ramped down until it reaches zero ampere, therefore having a ZCS turn-off event in the back-to-back switches. The current of the main PFC

inductor is not affected by the addition of the ARCP due to its much higher inductance compared to the auxiliary inductor. Therefore, no special consideration is required to control the PFC inductor current.

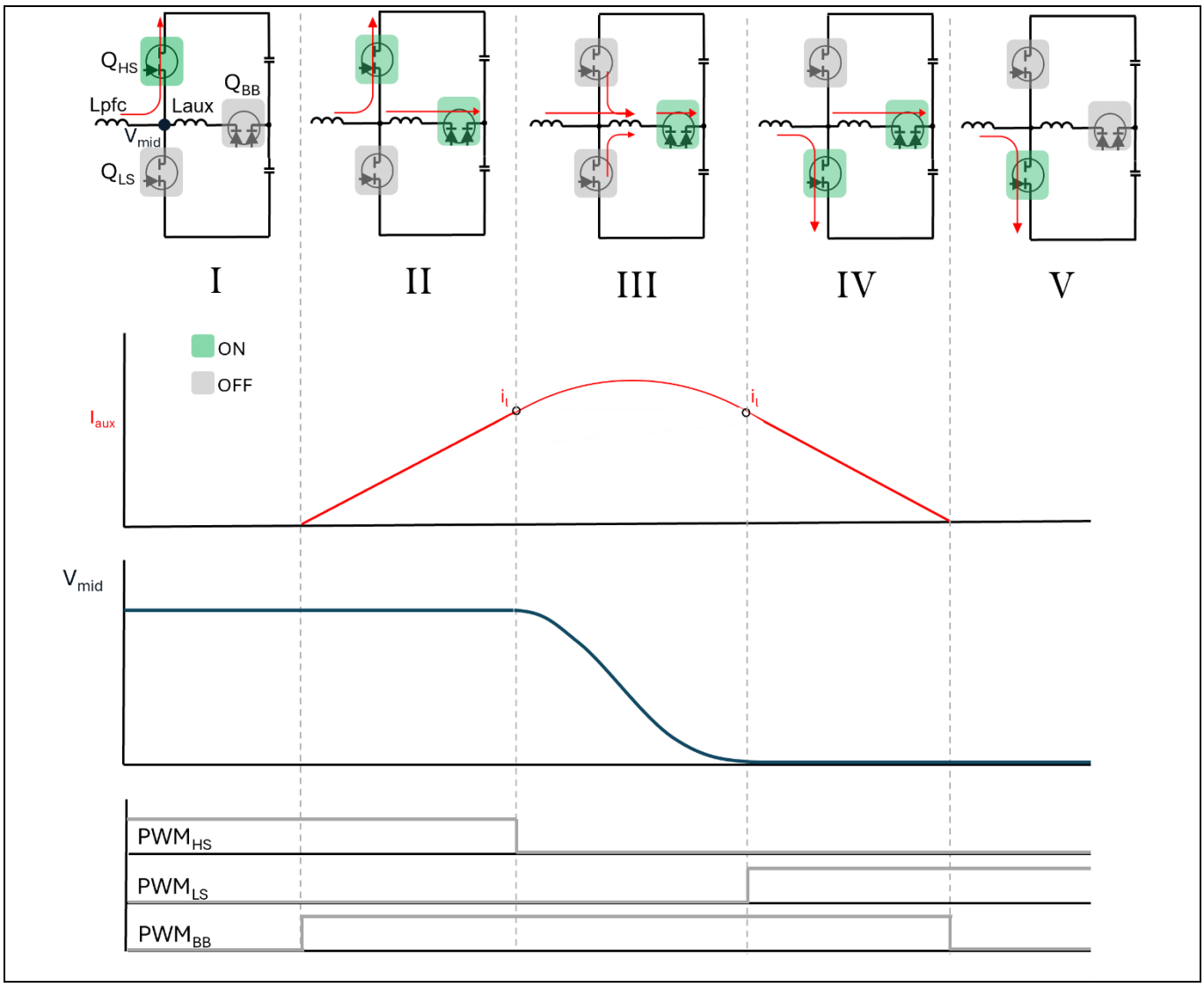



**Figure 7 Basic functionality of ARCP totem-pole PFC diode to switch transition with current flow, auxiliary current shape, midpoint voltage shape, and PWM signals**

The timing and synchronization of the half-bridge and back-to-back (BB) PWM signals is crucial to achieve minimum losses. If well-timed, all the switching events should be ZVS or ZCS. The only hard-switched turn-on event occurs in the BB switches, but that occurs at a voltage of $V_{bulk}/2$ and the $R_{DS(on)}$ class needed in the BB is higher than in the HB, having much lower losses than a hard-switched HB. As reference, in EVAL_3K3W_ARCP_PSU, the HB switches are paralleled 35 Ω devices, while the BB switches are non-paralleled 55 Ω devices.

The time it takes for the auxiliary inductor to ramp up to the PFC choke's current level mainly depends on the auxiliary inductance. For operations where the voltage of the split capacitor is close to half the bulk voltage, the following approximation can be used to calculate the ramp time:

$$T_{ramp} = \frac{2L_{aux}i_{PFC}}{V_{bulk}}$$

**Equation 1**

Where:

- $L_{aux}$: ARCP inductance value
- $i_{PFC}$: PFC choke's current at the time of the commutation event
- $V_{bulk}$: Voltage of the bulk capacitor bank

Stray inductance, conduction losses in the resonant path, gate driver propagation mismatch, and a low di/dt at the start of the conduction influence the timing, which can be compensated by extending the ramp time accordingly.

$$T_{ramp} = \frac{2L_{aux}i_{PFC}}{V_{bulk}} + T_{comp}$$

**Equation 2**

The resonant time during the totem-pole diode to switch commutation depends on the output charge $Q_{oss}$ of the devices in the half-bridge and the auxiliary inductance. For operation where the voltage of the split capacitor is close to half of the bulk voltage, the following approximation can be used to calculate the resonant time:

$$T_{res} = \frac{2\pi Q_{oss}}{\sqrt{2Q_{oss}V_{bulk}/L_{aux}}}$$

**Equation 3**

Where $Q_{oss}$ is the output charge of a single switch (or X times for a paralleled design) from zero volts to the voltage of the bulk capacitors at the time of the event.

In EVAL_3K3W_ARCP_PSU, to reduce the load on the microcontroller, $T_{ramp}$ is calculated every second switching cycle, while $T_{res}$ is a fixed value. The selection of the auxiliary inductor affects both times, which encourages a minimization of the inductor. A lower inductance results in lower conduction losses of the BB switches. However, a lower inductance implies higher di/dt, which requires an enhanced resolution in the PWM to achieve the required PWM pattern. Infineon's XMC4200 family of MCUs contain a high resolution PWM (HRPWM) unit, with a resolution of 150 ps. In EVAL_3K3W_ARCP_PSU the nominal di/dt is about 1 A/ns, as the nominal bulk voltage is 405 V and the auxiliary inductance is 206 nH. As a result, the design can control the auxiliary current at a maximum resolution of 150 mA.

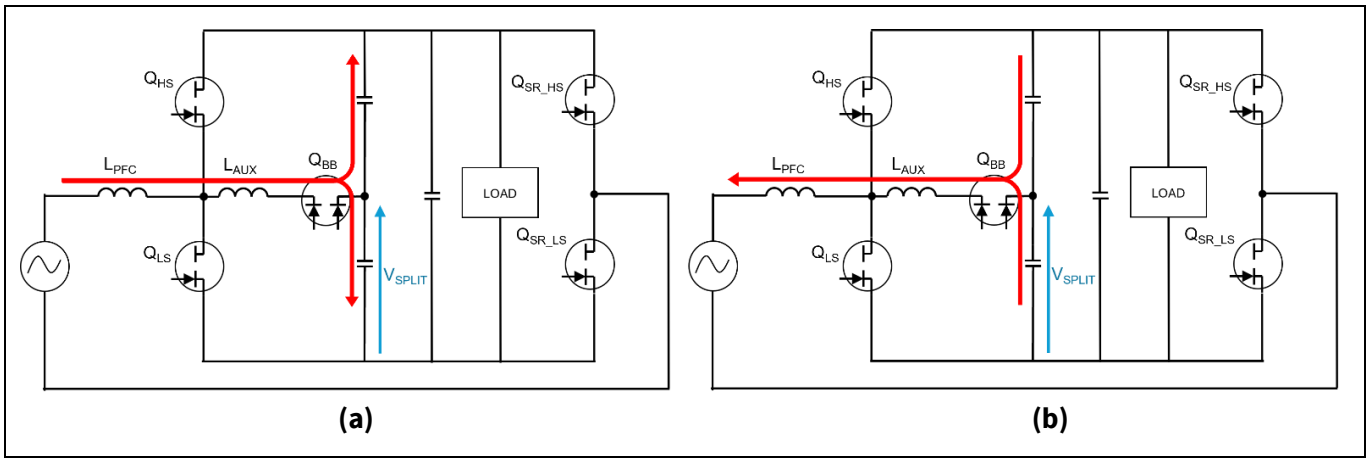



**Figure 8** **Current direction of the auxiliary inductor in (a) positive half-cycles and (b) negative half-cycles**

The charge for the ZVS event is absorbed (in positive AC half-cycles) and supplied (in negative half-cycles) by the capacitance of the split capacitor. This capacitance must be enough to sustain full-load steady state, load jumps, and line cycle dropouts (LCDO) while maintaining the voltage at the split capacitors within a deviation margin.

The more the voltage deviates from half the $V_{bulk}$, the less accurate Equation 1 and Equation 2 become, thus reducing efficiency and introducing potential failure conditions. Therefore, the bigger the capacitance, the steadier the switching events. For EVAL_3K3W_ARCP_PSU, the harshest condition is LCDO at full load, which is how the capacitors were sized, with a deviation of $V_{split}$ of ±6V in full-load steady state, and a maximum deviation of ±18V for a 10 ms LCDO event. Equation 4 gives an estimation of the split capacitance needed for steady-state operation.

$$C_{split,SS} = f_{sw} \frac{2Q_{oss} + T_{ramp,rms} i_{rms} + T_{res} i_{rms}}{8 f_{AC} \Delta V_{split}}$$

**Equation 4**

Where,

- $C_{Split\_SS}$: Capacitance needed to store the charge coming out or going into the split capacitors in a single AC half-cycle at full-load,
- $f_{sw}$ : Switching frequency of the half-bridge
- $f_{AC}$ : Line frequency
- $i_{rms}$: RMS PFC current at full-load
- $T_{ramp,rms}$ : Ramp time needed for the RMS PFC current at full-load
- $\Delta V_{split}$: Deviation of $V_{split}$ from the nominal $V_{bulk}/2$

The maximum charge required is at an LCDO event of 10 ms at 0° of the AC cycle. The $\Delta V_{split,LCDO}$ exhibited by the split capacitor increases in this condition, depending on how fast the response of the design is to a recovery from LCDO. EVAL_3K3W_ARCP_PSU exhibits a 3 times higher $\Delta V_{split}$ and therefore, the control and design need to account for this abnormal deviation and ensure a continued PFC operation.

**Table 2 Summary of parameters for the ARCP in EVAL_3K3W_ARCP_PSU**

| Parameter | Value |
|---|---|
| $L_{aux}$ | 206 nH |
| $V_{bulk,nominal}$ | 405 V |
| $Q_{oss}$ | 2*56 pC |
| $i_{rms}$ | 14.3 A |
| $f_{sw}$ | 135 kHz |
| $T_{res}$ | 33.5 ns |
| $T_{ramp,rms}$ | 14.5 ns |
| $\Delta V_{split}$ | ±7 V |
| $C_{split,SS}$ | 52 µH (56 µH selected by closest value) |

After a load jump or a LCDO event, the $V_{split}$ deviates from the nominal voltage. The topology brings the voltage back to $V_{bulk}/2$ naturally, although this might take longer than the required time in, for example, a repetitive LCDO event. Several techniques can be used to balance the voltage, in EVAL_3K3W_ARCP_PSU, a DC offset is introduced to the AC input current until the average value of $V_{split}$ equals to $V_{bulk}/2$.

*Note: No additional current measurement is required for the operation of the ARCP compared to the standard totem pole PFC.*

In addition to the switches, small diodes are recommended to clamp any currents which might occur at the turn-off of the BB switches. The placement of the auxiliary inductor and the BB switches can be swapped. In EVAL_3K3W_ARCP_PSU, the inductor is connected to the split capacitors while the BB switches are placed between the inductor and the half-bridge. During testing, it was found that this configuration reduced the clamping currents of the diodes, eliminating the need of damping resistors in series to the diodes.

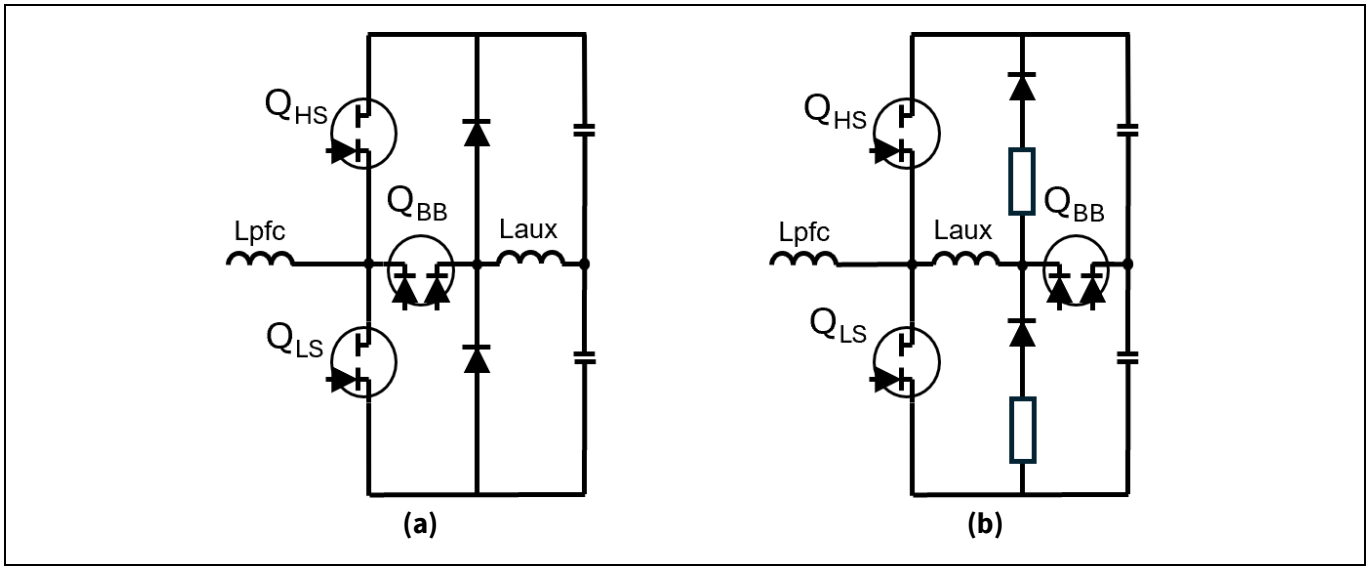



**Figure 9 Possible configurations of ARCP: (a) Chosen configuration with BB switches connected to HB and (b) BB switches connected to split capacitor**

## 2.2 Hardware implementation

The hardware implementation of the PFC is distributed among the PFC power card (PW100001622) hosting the high-frequency CoolGaN HEMTs, the LLC power card (PW200003075) hosting the synchronous rectification stage and the main board (M100001621) hosting the PFC inductor, input line filter, and NTC. Figure 10 shows the main board and a top view of the power daughter cards and their location. The PFC inductor uses a CH270060GT from Chansung Corporation with 44 turns. The split capacitor uses two EKXN351ELL560ML16S from United Chemi-Con and the auxiliary air-core inductor is a 744918220 from Würth Electronics.

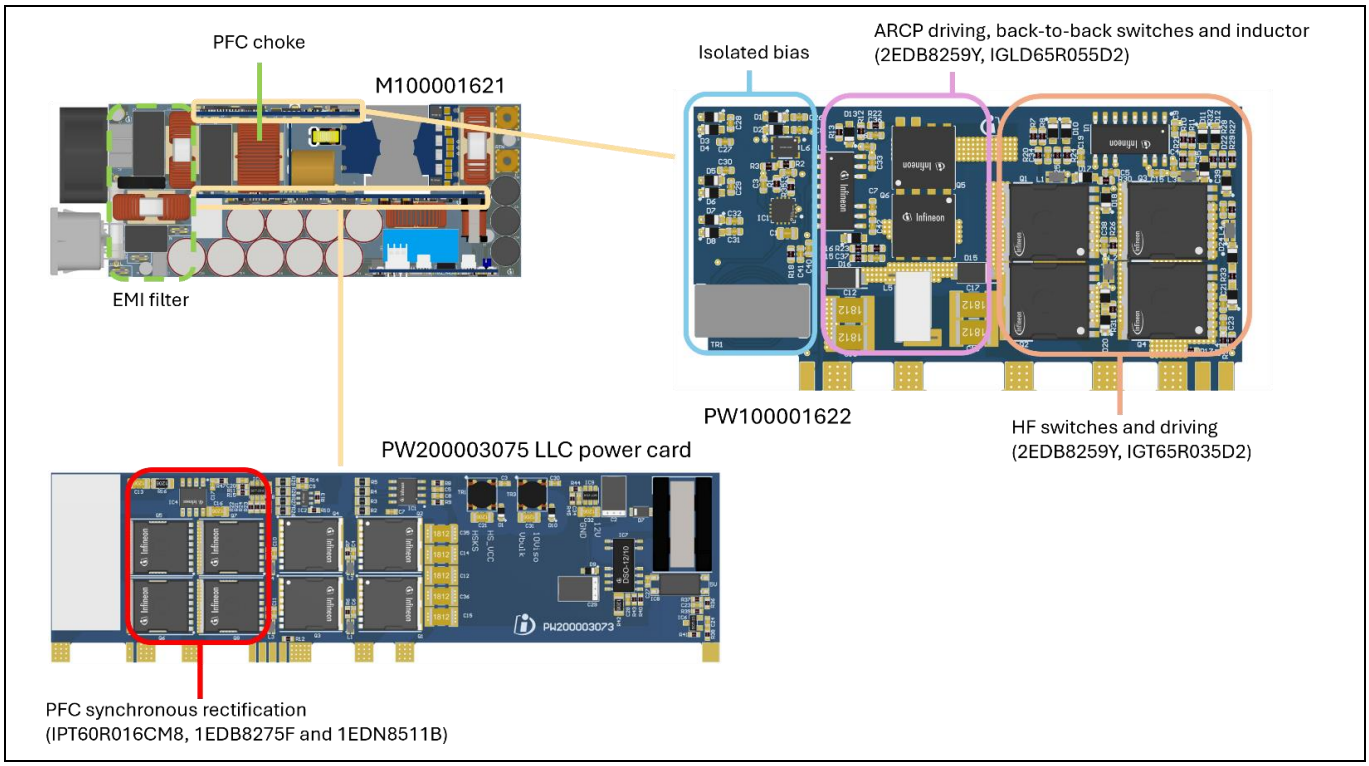



**Figure 10 Hardware implementation of the ARCP totem-pole PFC**

## 2.3 Efficiency and losses

Figure 11 shows the efficiency measurements for steady-state operation of only the PFC at different AC voltages. The efficiency measurements have been obtained with a WT5000 power analyzer with 5 kHz input and no output line filters at 50 Hz line voltage, excluding the fan power consumption. The fan has been powered externally at 12.4 V, and the spaces between the metal chassis and the plastic shroud have been taped in order to mimic the airflow that a steel server or data center PSU would have, as shown in Figure 48. The measurement point for the input voltage is right before the insertion of the input connector into the PCB, while the output voltage measurement point is in one of the bulk capacitor pins.

*Note: Due to production and measurement setup tolerance, worst-case efficiency variations of a maximum of ±0.1% can be observed.*

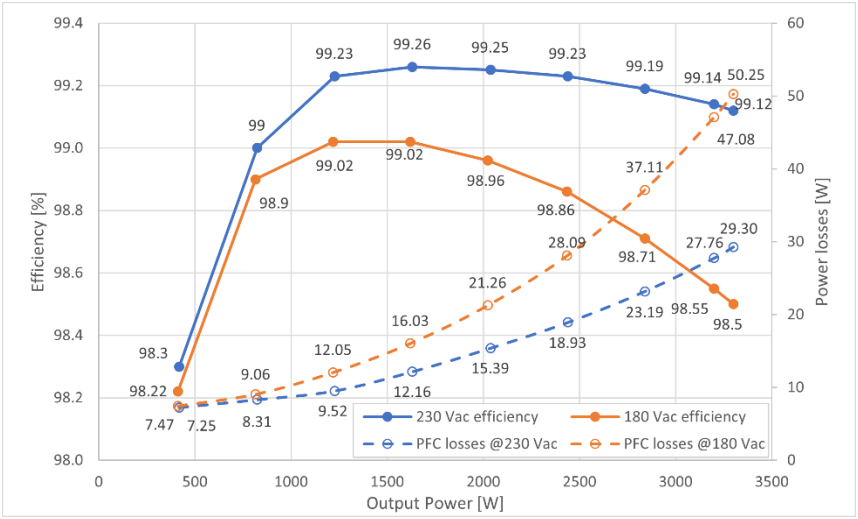



**Figure 11 Efficiency of the ARCP TP PFC**

## 2.4 Driving CoolGaN™ and CoolMOS™ in the ARCP TP PFC

To ensure the correct operation of the PFC converter, proper operation of the driving stage is crucial. For CoolGaN™ devices, 9 $V_{DC}$/-3 $V_{DC}$ bipolar driving voltage is used as per the driving voltage recommendations [4]. The bias supplies are initially generated via a compact transformer from the 3.3 $V_{DC}$ generated from the buck converter on the control card. Both the positive and negative rails are generated from the same transformer for all four channels (two for the HB and two for the resonant pole).

The main reason for using this method is that it is high-density and efficient. As a single transformer is used, at least 6 PCB layers are needed, without extensive use of buried vias. In fact, only four buried vias are used in the design. The transformer is fed by a voltage regulator IC, with direct feedback to the low-side HB leg. Direct feedback enables precise and dynamic voltage setting, as opposed to an unregulated design. 3.3 $V_{DC}$ are boosted to 12 $V_{DC}$, which are divided into 9 $V_{DC}$ and -3 $V_{DC}$ via the winding. Figure 12 and Figure 13 show the schematic and the stacking of the bias channels within the ER14.5 core. Another benefit of having isolated bias supply instead of bootstrapping is that the voltage is stable in abnormal conditions such as LCDO or burst operation and it simplifies the control implementation, since no special sequence is required to ensure nominal voltage.

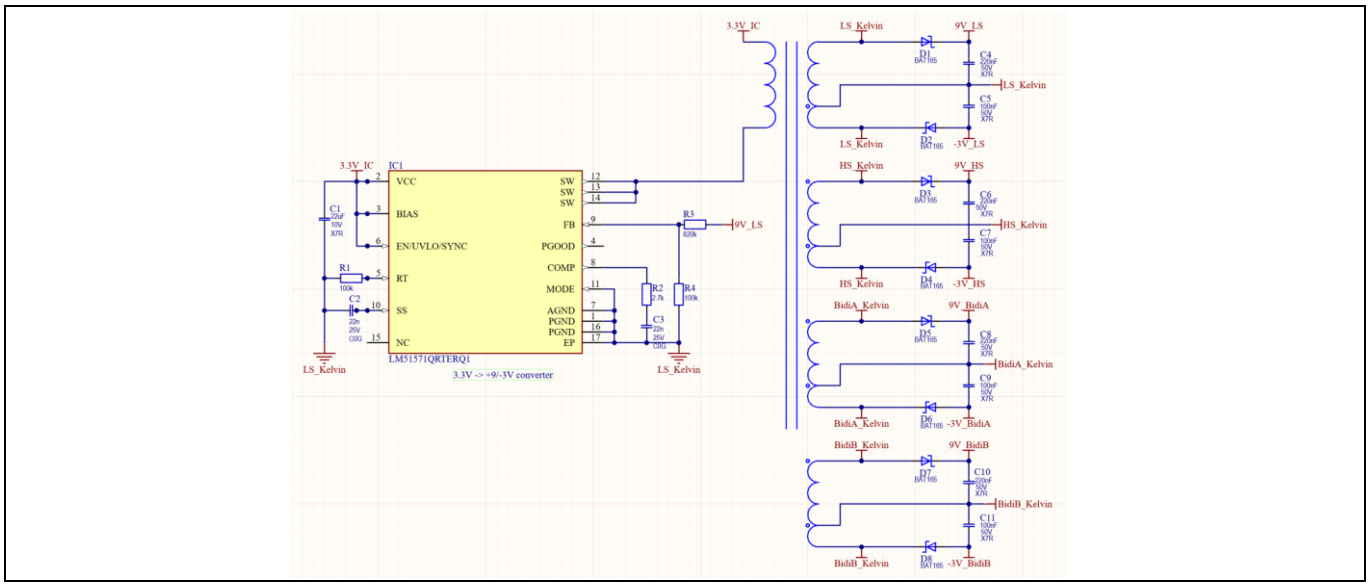



**Figure 12 HB and ARCP bias supply schematic view**

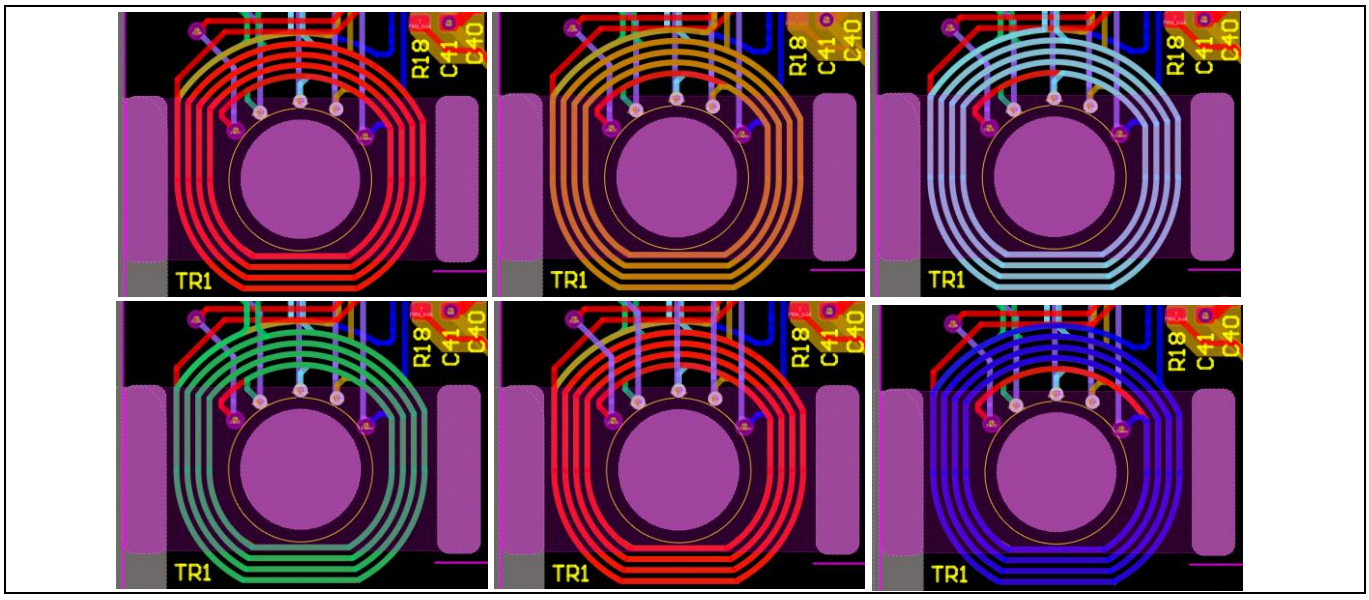



**Figure 13 HB and ARCP bias supply transformer stack – Stack layers from left to right: L1 Vin, L2 HB high-side, L3 ARCP A, L4 ARCP B, L5 Kelvin source of all channels, and L6 HB low-side**

Infineon's CoolGaN™ transistors are driven by an RC network that provides the turn-on and turn-off charge, while a resistor is used to keep the transistor turned-on in steady state. Two CoolGaN™ switches are paralleled [5], which introduces the risk of conducting the channel current through the Kelvin source pins. To drive the CoolGaN™ devices efficiently while paralleling, a common mode (CM) choke is suggested in series with the gate loop to increase the CM impedance without affecting the differential mode (DM) impedances, which could affect the driving loop. For this, four CM chokes from Bourns (SRF2012-361YA) have been used, as shown in Figure 15.

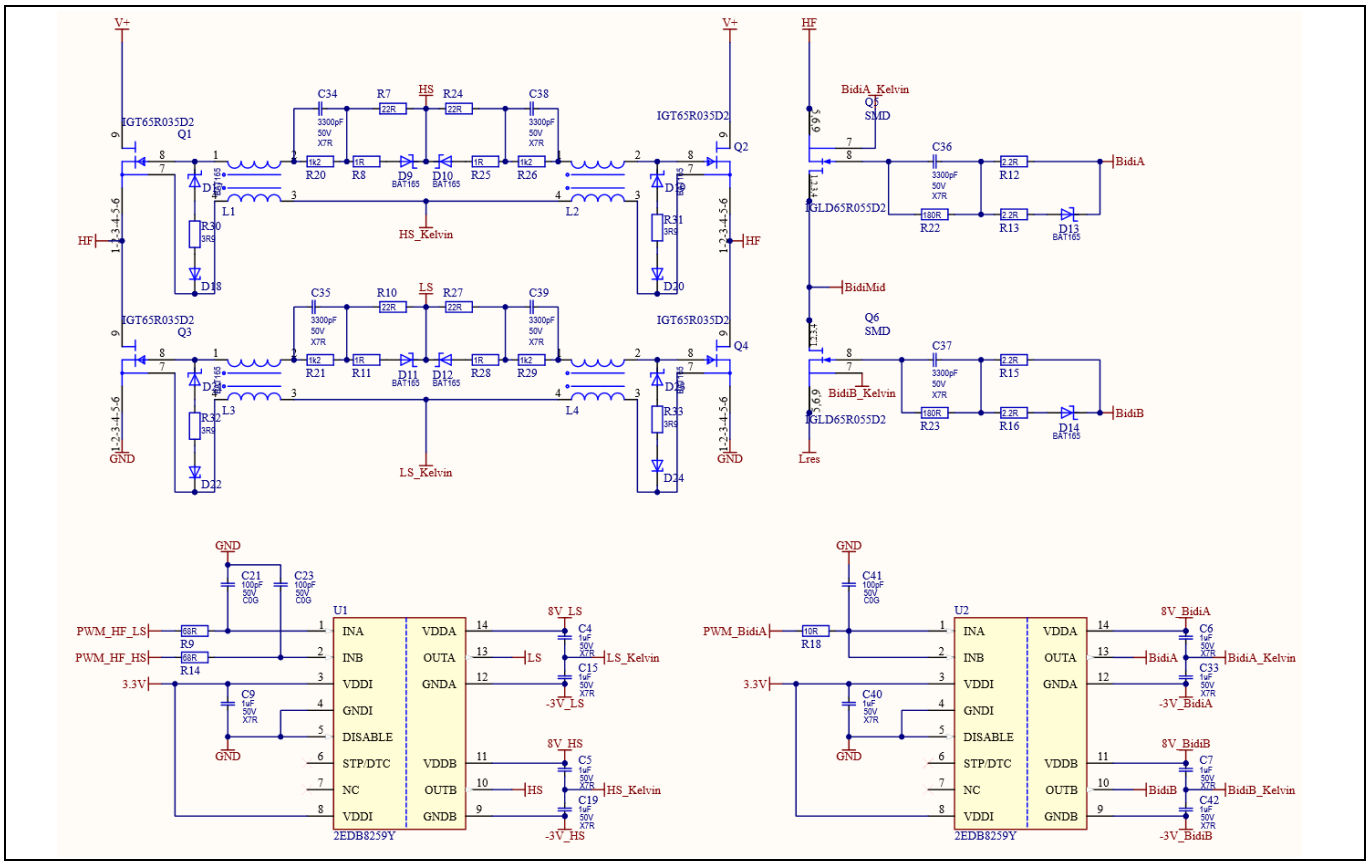



**Figure 14 Driving CoolGaN™ in parallel (EiceDriver™ 2EDB8275Y)**

*Note: In EVAL_3K3W_ARCP_PSU, the back-to-back switches are placed in a common-drain configuration. However, if a reduction of BOM is preferred, the switches can be placed in common-source configuration, therefore requiring only one channel to drive them.*

Although the ARCP is a fully soft-switched topology in steady-state conditions, the totem-pole PFC needs to operate under unwanted circumstances such as voltage sags and LCDO. Depending on the conditions, hard-switching events might occur.

In addition, it has been observed that using a CM choke in the gate of paralleled GaN devices can introduce a significant gate impedance in normal mode, weakening the clamping of the gate driver while being off. This can lead to pronounced negative voltage spikes in the HB switches in the switch to diode transition. To protect the gate from such events, a zenner diode is used to clamp excessive negative voltages, with a resistor in series to dampen the effect. A Schottky diode is placed in anti-series not to affect the positive driving of the device.

The driving of the CoolMOS™ is shown in Figure 15. A hybrid driving approach with an isolated high-side and non-isolated low-side switch has been adopted [7]. For the CoolMOS™ synchronous rectification leg that is switching at 50 Hz, a bootstrap approach has been adopted to minimize costs. In this case, proper capacitor dimensioning is required to avoid discharging and breaching the UVLO threshold of the driver.

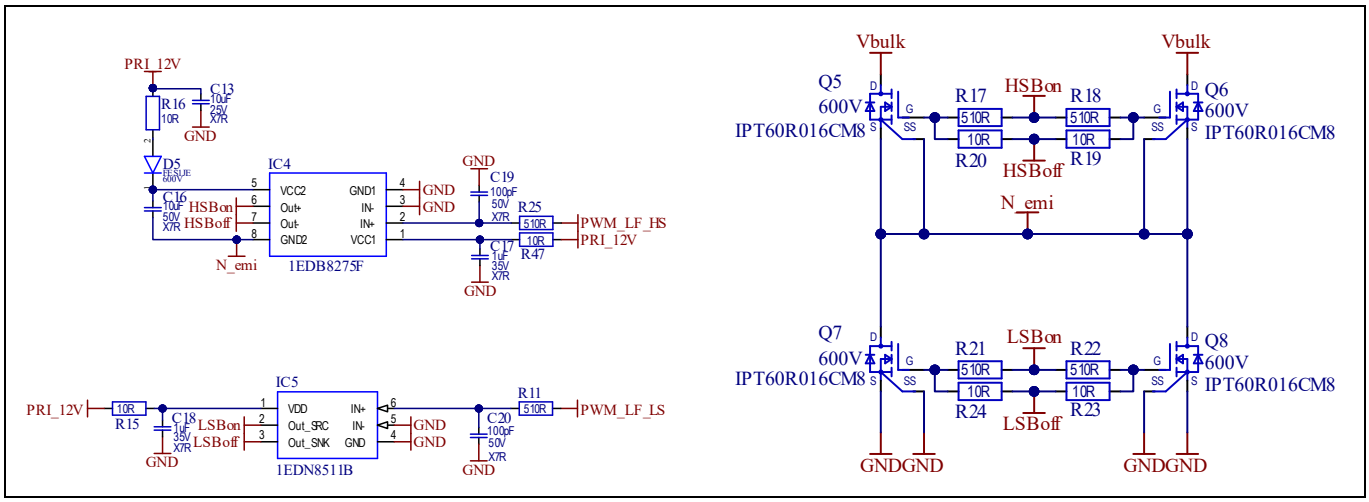



**Figure 15 Driving CoolMOS™ with hybrid driving (EiceDriver™ 1EDB8275F along with 1EDN8511B)**

## 2.5 Signal conditioning and digital control of ARCP-TP CCM PFC

The PFC of EVAL_3K3W_ARCP_PSU implements CCM average current mode control with duty and load feed-forward. Unlike the classic PFC where the AC voltage is rectified by the diode bridge, in the bridgeless totem-pole PFC converter, the inductor current is both positive and negative. In addition, isolation or common-mode rejection is required to measure the inductor current if the control ground is placed in the negative rail of the bulk voltage, as has been traditionally done in the classic PFC. A Hall-effect sensor is therefore a good solution for this kind of system.

The output of the Hall-effect sensor matches the ADC inputs when supplied with the same voltage – positive and negative currents are measured with the span of the ADC and a shift to half of the ADC range for zero current. The sensor has enough bandwidth to also sense the high-frequency ripple and therefore, the same signal can be used for peak-current limitation and input overcurrent protection (OCP). In case of a lower bandwidth, the Hall-effect sensor typically offers an overcurrent detection signal, which could be used for the same purpose.

The bulk and the LLC input voltage are sensed by the PFC controller via a resistive partition, as shown in Figure 16 in blue (for simplicity, only the voltage gain is reported). The AC sensing chain is shown in in violet. It is split into positive and negative AC sensing with respect to ground and the two resulting signals are then summed in the analog domain. Lastly, the polarity of the AC input is obtained via a comparator, shown in orange.

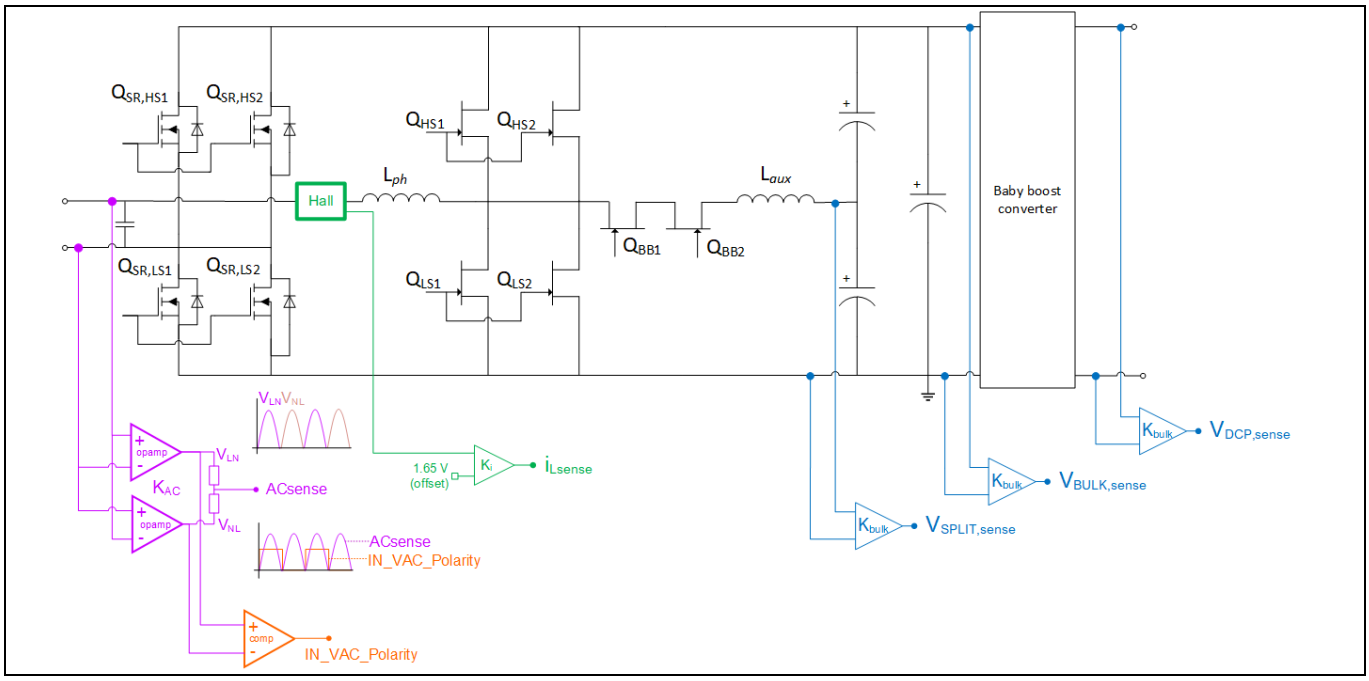



**Figure 16 Sensing circuit required to control the ARCP-TP PFC converter with XMC™**

Since the AC voltage is used for the current reference generation in the selected average current mode structure, the current reference is a full-wave rectified sinusoidal sequence. However, the current sense after the ADC is a sinusoidal sequence with offset at half of the ADC span. Therefore, the ADC result from the current-sense requires the offset to be removed before being rectified according to the AC polarity signal. These two steps, together with extra gain, are implemented by software in the XMC™ controller.

Because of the low amount of bulk capacitance available in EVAL_3K3W_ARCP_PSU, feed-forward of the PSU load current to the PFC voltage loop is required to enhance the response during 10% to 100% and 10% to 50% load jumps with 20 Hz repetition rate, as required by server and data center standards. Experimental results for load jump tests are discussed in Section 4.4.1.

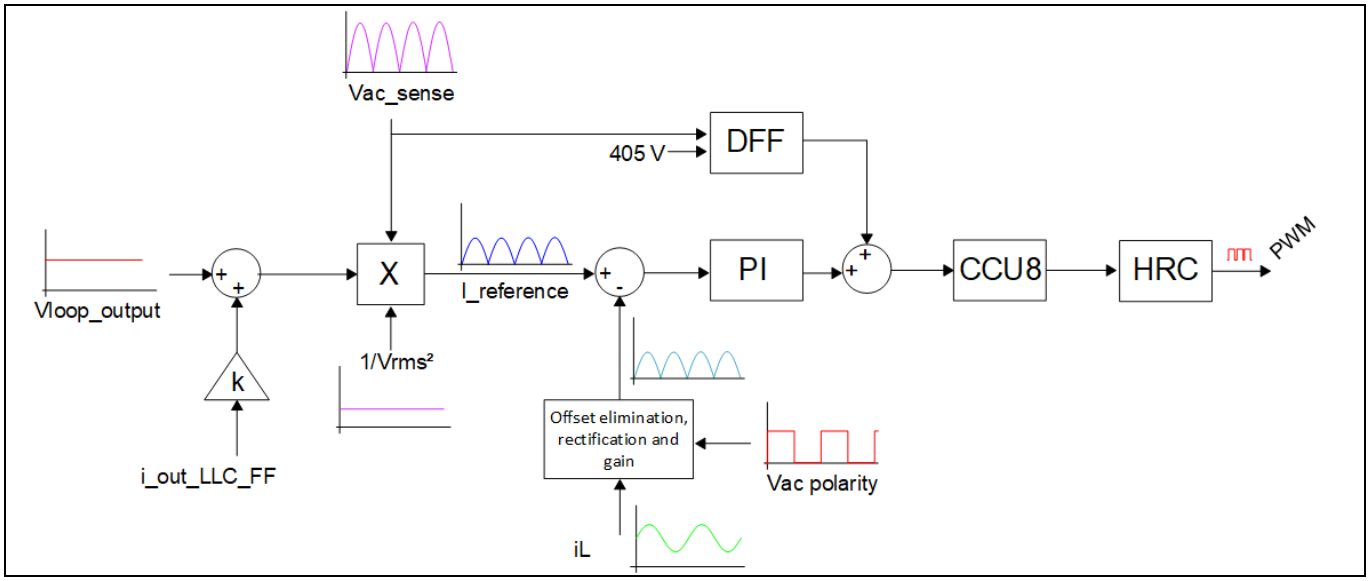



**Figure 17 Current loop structure with duty cycle feed-forward (DFF) and PSU load feed-forward**

## 2.6 PWM pattern for the ARCP totem-pole

The auxiliary resonant commutated pole enables full soft-switching of the CCM totem-pole PFC by providing or absorbing the charge of the CoolGaN™ switches of the half-bridge. While transitioning from switch to diode, the CCM TP PFC naturally discharges the diode-mode CoolGaN™ by forward biasing.

In traditional CCM TP PFC, the transition from diode to switch is hard-switched, as the full output charge of the switch ($Q_{oss}$) is removed by the commutation of the half-bridge counterpart. In contrast, in the ARCP TP PFC, the current in the auxiliary inductor is ramped up to the main inductor current by turning on both back-to-back switches. Once the current of the main inductor is matched, the diode-mode CoolGaN™ is turned off. At this point a resonance happens between the auxiliary inductor and the output capacitance ($Q_{oss}$) of all switches of the half-bridge. The resonance pushes the voltage of the switch down to almost zero volts, after which it is turned off. The back-to-back switches are kept turned on until the current in the auxiliary inductor reaches zero. The basic operation and switching pattern are discussed in Section 2.1.

To calculate the correct timing for the switches, the information of the current in the main choke is necessary. It is not necessary to measure the current of the auxiliary inductor, but the split capacitor voltage is measured for OVP and UVP along with balancing in case of dynamic conditions. The CCU8 timer of the XMC™ controller assigned to the back-to-back switches has the same frequency as the HB switch CCU8 blocks. After the timings are calculated, the high resolution PWM blocks are used to generate the PWM pattern for the switches, as these provide a resolution of 15 ps. The HRPWM is required because the di/dt of the auxiliary inductor is 1 A/ns nominally, and therefore, sub-nanosecond resolution is paramount for a good timing control.

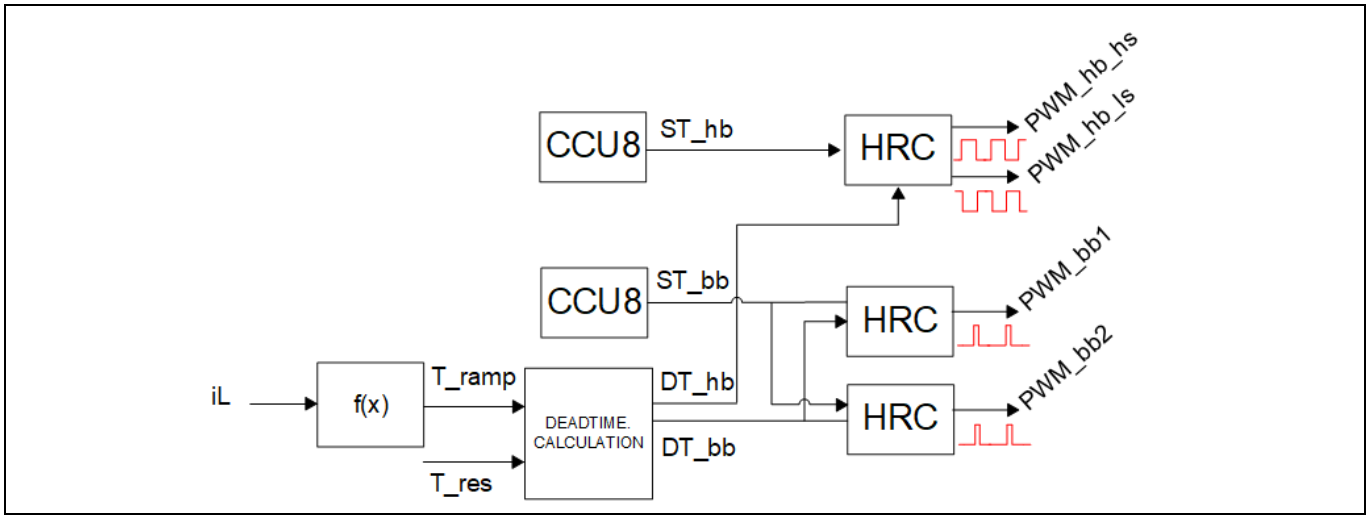



**Figure 18 PWM signal generation of HB and BB switches in EVAL_3K3W_ARCP_PSU**

## 2.7 Comparison with interleaved totem-pole PFC

This section compares the ARCP TP TPF topology presented in this document with the interleaved totem-pole PFC implemented in [2]. Both EVAL_3K3W_ARCP_PSU and REF_3K3W_HFHD_PSU have the same power rating and dimensions, which leads to the same power density. Both designs implement the same hold-up time extension, while the LLC of EVAL_3K3W_ARCP_PSU is an updated version.

The main difference between the topologies is the fact that the classic TP PFC is a hard-switching topology in terms of the diode to switch transition of the fast-switching leg, while the ARCP is a full soft-switching topology. This reduction in switching losses enables increased switching frequency – for the same total power loss. Given the higher switching frequency, the main PFC inductor's size can be reduced.

## Auxiliary resonant commutated pole TP PFC

The PFC inductors of 3K3W_HFHD_PSU are rated to half of the input current due to the interleaving implemented in the design. EVAL_3K3W_ARCP_PSU's PFC inductor sees the full input voltage, as there is only one phase in the PFC stage. Despite that, a much smaller inductance is needed due to the higher switching frequency of the ARCP topology. A 50% reduction of the PFC inductor of has been achieved in EVAL_3K3W_ARCP_PSU. This can be further reduced by increasing the switching frequency at the cost of efficiency. The PFC choke design of both reference designs is presented in .

*Note: In order to keep the split capacitor voltage within nominal values and to comply with LCDO requirements, electrolytic capacitors were needed for EVAL_3K3W_ARCP_PSU. These capacitors take about 60% of the space of the PFC inductor.*

**Table 3 PFC choke design comparison between interleaved totem-pole and ARCP TP PFC**

| Reference design | Number | Core | Turns | Inductance@0A |
|---|---|---|---|---|
| Interleaved totem-pole | 2 | CH270060GT14 | 64 | 384 µH |
| ARCP TP PFC | 1 | CH270060GT14 | 44 | 182 µH |

The main advantage of the ARCP design is its outstanding efficiency across the power range. The interleaved design implements 57 mΩ CoolSiC™ 650 V devices, while the ARCP mounts 35 mΩ CoolGaN™ 650 V devices. The improved peak efficiency at nominal input voltage (230 V) is 0.36%, with a considerably higher improvement at light load. For full-load operation, the efficiency of the ARCP is kept higher than 0.32% than the interleaved TP.

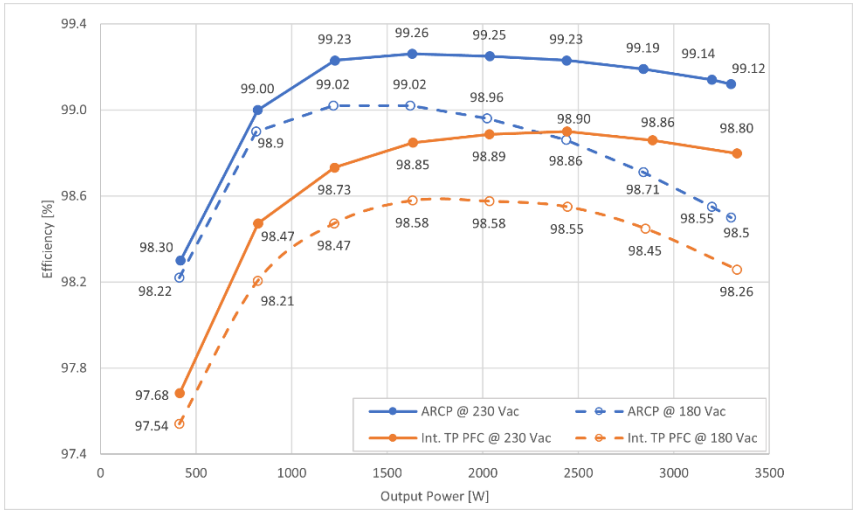



**Figure 19 Measured efficiency comparison between ARCP and interleaved totem-pole PFC [2]**

At light load, the efficiency is higher due to the half-bridge ZVS . There are still losses in the back-to-back switches (35 mΩ CoolGaN™ 650 V devices) of the ARCP, but these occur in a ZCS transition and at half the bulk voltage. As the load is increased, the benefit of the ZVS and the low $R_{DS(ON)}$ of the paralleled 35 mΩ CoolGaN™ 650 V devices keep the losses lower than that in the interleaved design. This is true even for the 180 $V_{AC}$ condition, where the minimum efficiency gain is still about 0.25%.

# 3 Half-bridge LLC converter

As a back-end DC-DC converter, a half-bridge LLC topology with full-bridge rectification has been selected. This conversion stage provides safety isolation and regulates the output from the 400 V bulk voltage. A simplified schematic of the chosen topology is shown in Figure 20.

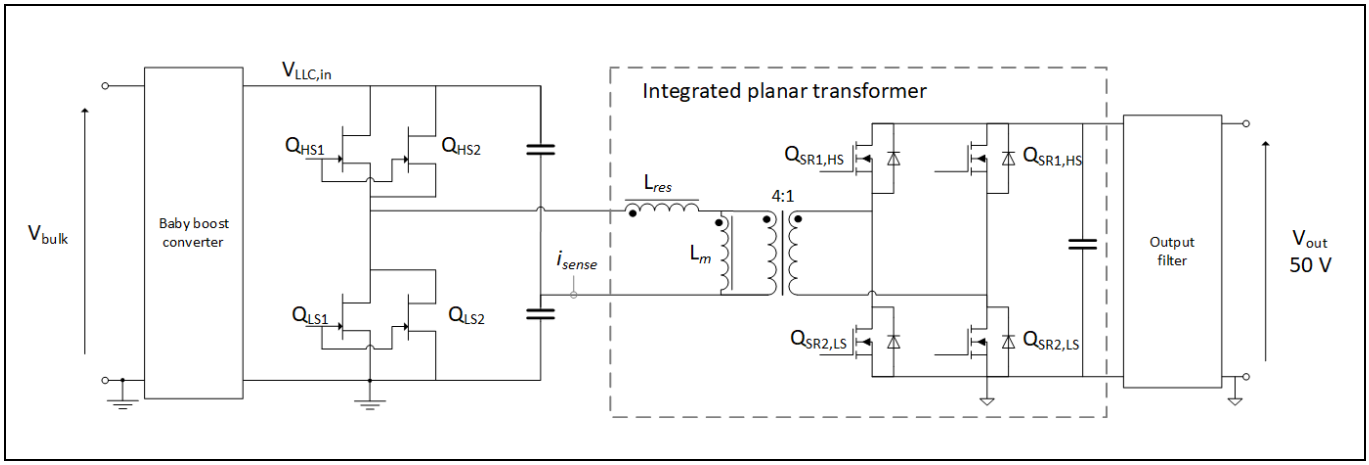



**Figure 20 Simplified schematic of the LLC HB DC-DC converter in EVAL_3K3W_ARCP_PSU**

## 3.1 Hardware implementation

The LLC DC-DC converter primary is placed on the LLC power card, which drives the integrated transformer that integrates the secondary-side synchronous rectifiers.

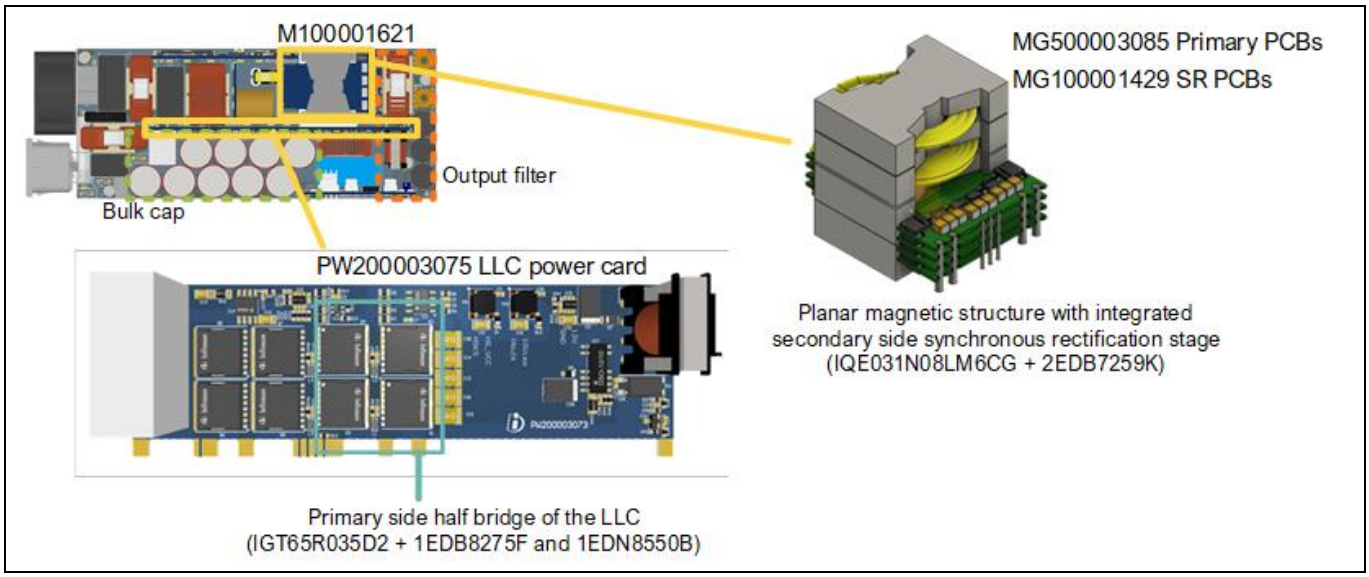



**Figure 21 Primary and secondary sides of the LLC converter**

## 3.2 Efficiency and losses

The efficiency measurements have been obtained with a WT5000 power analyser with no input and no output line filters. The measured efficiency of the half-bridge LLC converter is plotted for 400 VDC nominal input voltage in Figure 22. Efficiency is near 98.7% at 50% of the rated load and remains around 98.3% at full-load.

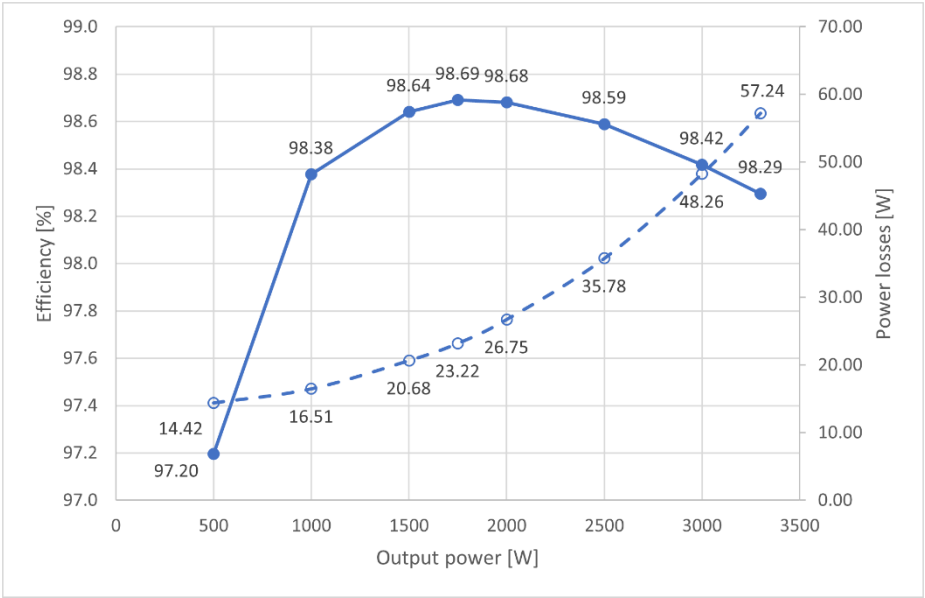



**Figure 22 Efficiency of the LLC DC-DC stage with a CoolGaN™ device having a 35 mΩ on-resistance**

## 3.3 Integrated LLC half-bridge magnetics and SR

One of the advantages of the LLC topology is reusing the leakage inductance of the main transformer as the resonant inductance of the tank and the magnetizing inductance of the transformer as a parallel resonant inductor. However, this compromises the overall efficiency and therefore, the design of EVAL_3K3W_ARCP_PSU has series and parallel inductors integrated in the main transformer structure to minimize space. Figure 23 shows the cross section of the transformer structure.

It is important to mention that the magnetic structure presented in Figure 23 is key to this design achieving the high efficiency of the LLC, integration of the synchronous rectification stage, and the required power density.

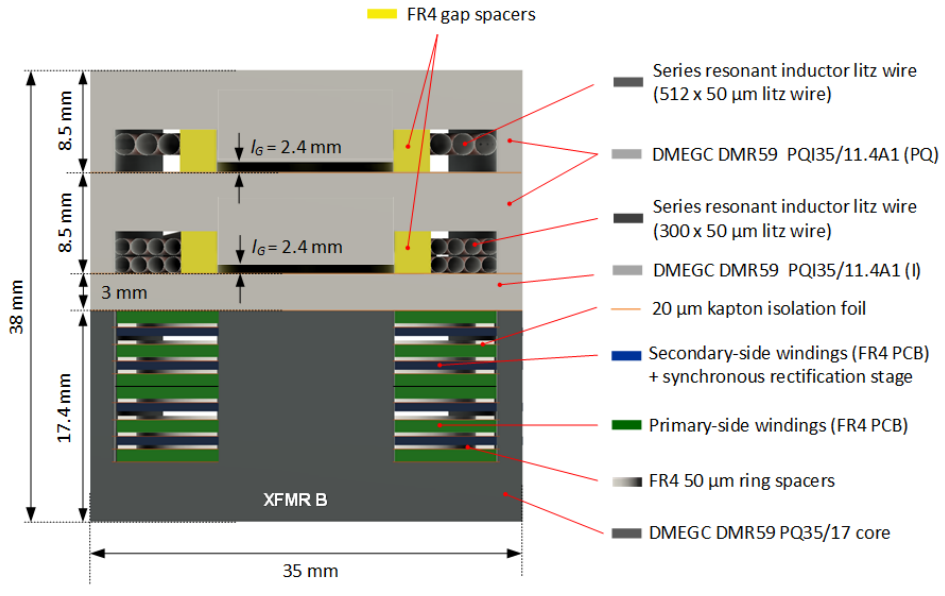



**Figure 23 Integrated planar transformer assembly – cross section**

The overall size of the full magnetic structure including series and parallel inductors of the LLC converter is 35 mm × 37 mm × 47.5 mm. The magnetic structure adopts two PQ35 DMR59 cores from DMEGC for the main transformer, and two PQI35 DMR59 cores with integrated gaps from DMEGC for the resonant series inductor and the parallel inductor of the LLC converter. The 8:2 main transformer stack uses six primary and four secondary PCBs, as shown in Figure 24, with full interleaving to reduce high-frequency copper losses. Inbetween each PCB couple, an FR4 spacer is also inserted to increase the air gap between the windings, consequently reducing the inter-winding capacitance for each interleaving layer and keeping it constant.

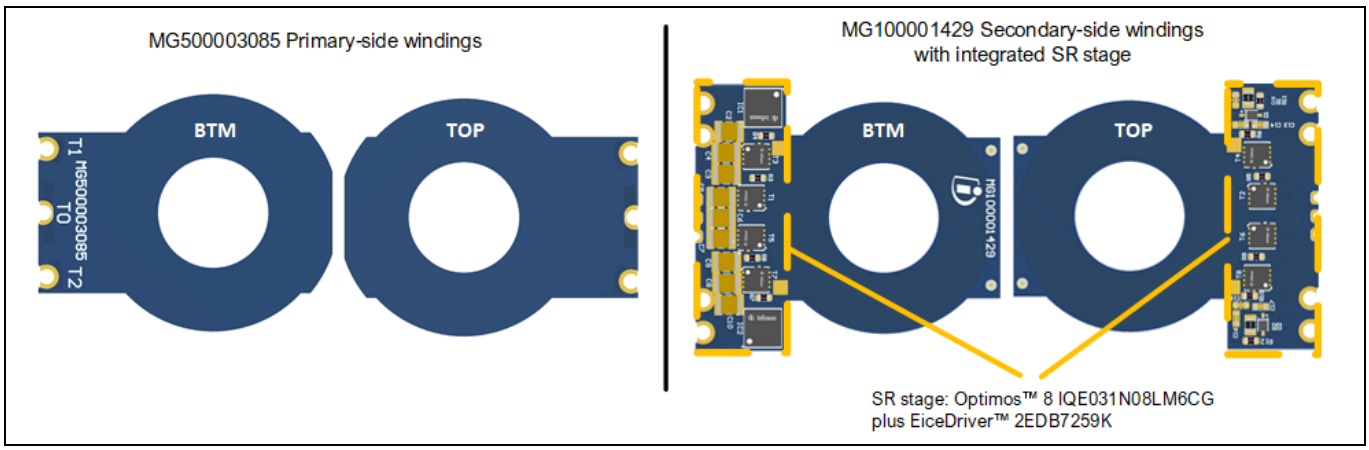



**Figure 24 Primary- and secondary-side winding PCBs of the transformer in Figure 23**

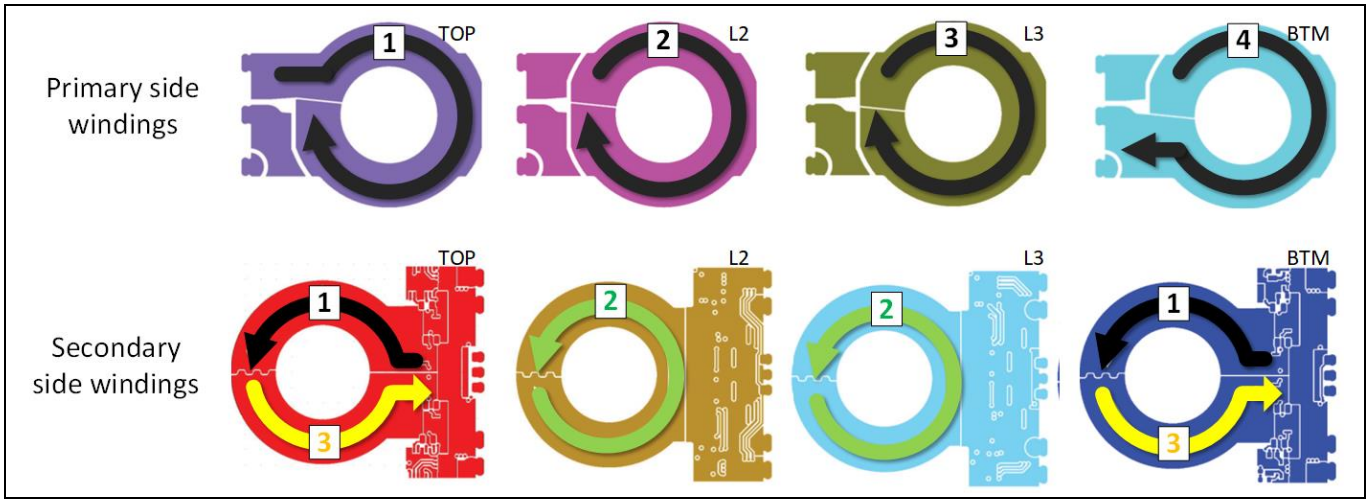



**Figure 25 Arrangement of the planar windings in the main transformer**

As mentioned earlier, both the series and parallel inductors use cores with distributed gaps to reduce losses caused by stray magnetic fields. Litz wires are employed to reduce AC resistance and high-frequency copper losses. The series resonant inductor uses three turns of 512 strand 0.05 mm triple-insulated wire, and the parallel inductor uses eight turns of 300 strand 0.05 mm, both Rupalit Safety V155 from PackLitzWire. This results in the overall height of the full magnetic structure being only 37 mm, enabling it to fit in the 40 mm 1U maximum height limit according to the standards.

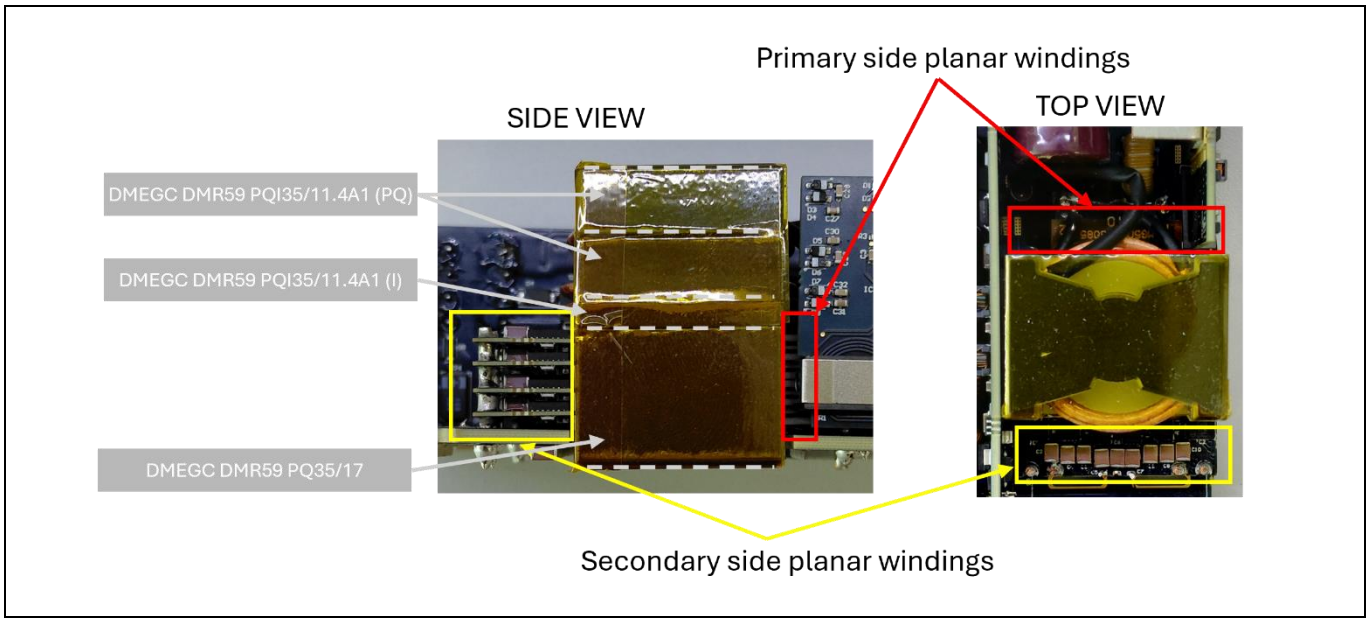



**Figure 26 Integrated planar transformer assembly – picture of an assembled unit**

## 3.4 Driving CoolGaN™ and OptiMOS™ in the LLC converter

The primary-side of the LLC converter uses four CoolGaN™ devices, each having a 35 mΩ on-resistance in TOLL package (CoolGaN™ IGT65R035D2), with both high and low sides having two devices in parallel. The resonant frequency of the LLC is about 460 kHz, and therefore, the typical switching frequency of the CoolGaN™ devices is between 400 kHz and 520 kHz. To drive the CoolGaN™ devices efficiently while paralleling, a CM choke is suggested in series with the gate loop to increase CM impedance without affecting the differential mode (DM) impedances, which could affect the driving loop. For this purpose, four CM chokes from Bourns (SRF2012-361YA) have been used, as shown in Figure 27. For further information about GaN paralleling, see References [5].

The GaN HB primary leg of the LLC does not require isolation since it is already implemented with digital isolators. For this reason, hybrid driving is employed to ensure high CMTI, flexible placement, and a lower overall impedance due to gate-loop optimization. For further information on hybrid driving for CoolGaN™, see References [7].

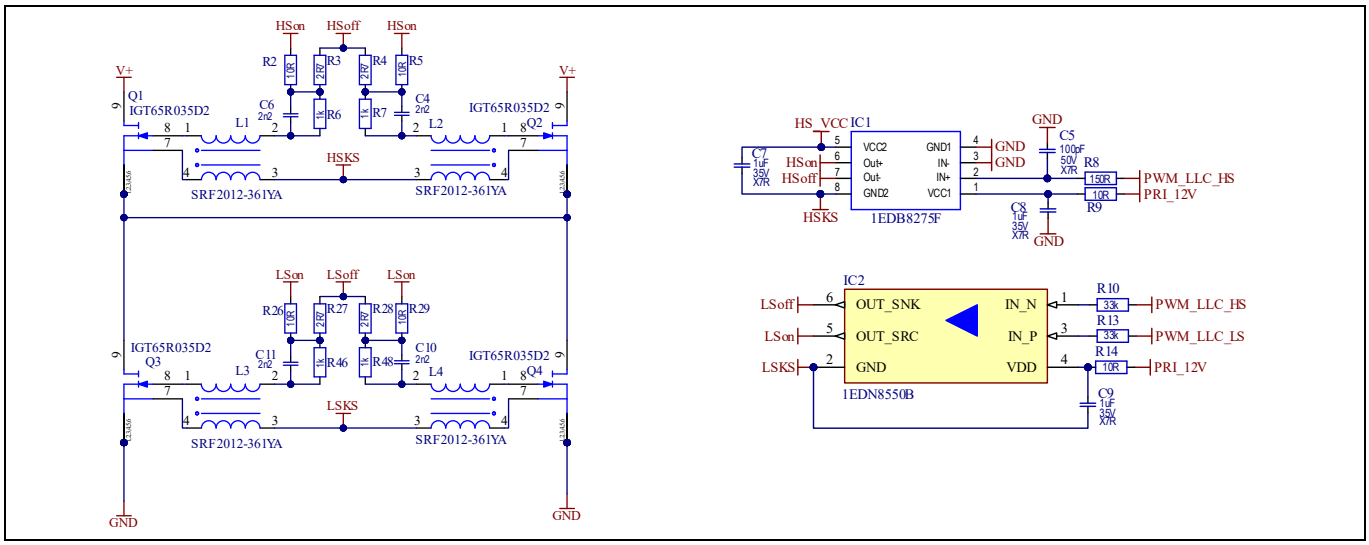



**Figure 27 Driving CoolGaN™ with hybrid driving (EiceDriver™ 1EDB8275F with 1EDN8550B)**

For the bias supply of the OptiMOS™ MOSFETs on the secondary side, a bootstrapped solution with a 5 $V_{DC}$ bias is used, as shown in Figure 28. Because of the space constraints, EiceDriver™ 2EDB7275K in a 5 mm × 5 mm package is used, which exactly fits the small space available on the secondary board stacked in the transformer structure (see Figure 24).

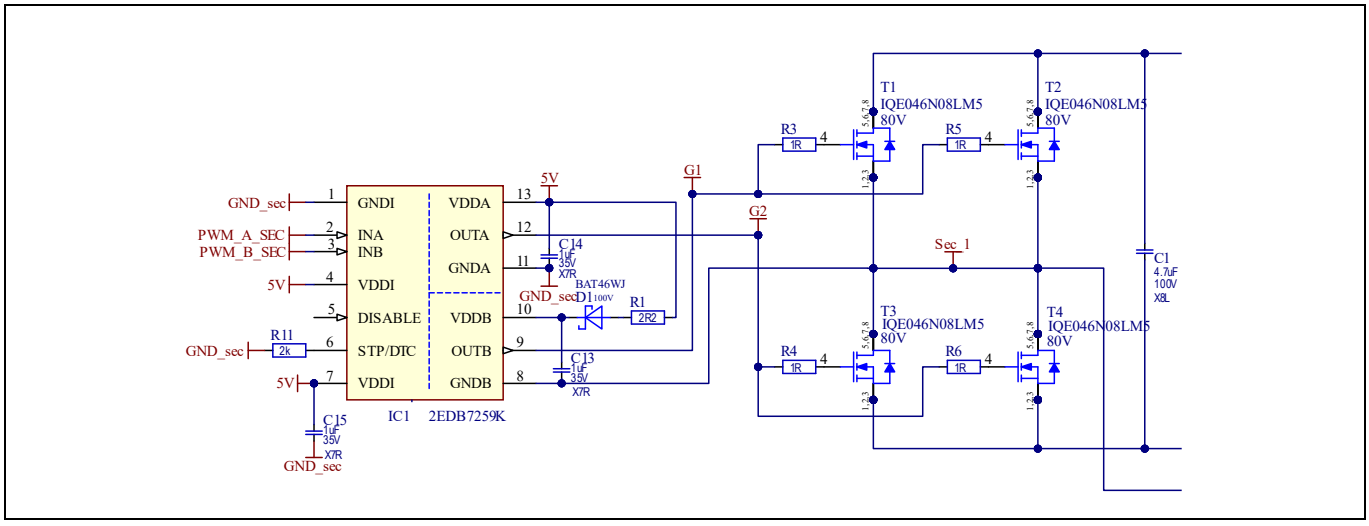



**Figure 28 Driving OptiMOS™ with EiceDriver™ 2EDB7259K**

## 3.5 Baby-boost stage to extend hold-up time

To have a significant improvement in the power density, a viable and widely accepted approach is to implement a reduction of the bulk capacitance. Indeed, under steady-state conditions, the converter can operate with a lower bulk capacitance, provided that the 100 Hz ripple of the bulk voltage keeps below the maximum voltage rating of the components, the maximum RMS current can still be handled by the remaining bulk capacitors and the converter still meets the requirements in terms of load transients.

Overall, two criteria need to be satisfied: the total PFC output AC current stress must be lower than the maximum RMS current that the capacitor bank can handle, and the capacitance value must be high enough to:

- Prevent the bulk voltage from exceeding the voltage rating (usually capacitors limit the voltage stress)
- Allow the PFC stage to operate with the required power factor and THD (that is, minimum steady-state bulk voltage coming too close to the $V_{AC}$ peak at the input)
- Supply the LLC converter for 10 ms at full output power (3.3 kW) during AC line dropout (ACLCDO)

In a standard server power supply with 3.3 kW maximum nominal output power, assuming an average ($V_{bus,nom}$) bulk voltage 410 $V_{DC}$ and minimum bulk voltage ($V_{bus,min}$) being 395 $V_{DC}$ during steady-state operation at full-load, and a minimum bulk voltage during LCDO ($V_{bus,LCDOmin}$) being 360 $V_{DC}$ as shown in Figure 29, the minimum capacitance required to achieve the 10 ms hold-up time is $2\ P_{out,max}\ t_{HUP}/[V_{bus,min}^2 - V_{bus,LCDOmin}^2]$ which results in around 2.5 mF total capacitance.

For EVAL_3K3W_ARCP_PSU, by allowing the $V_{bus,LDCOmin}$ to go to a voltage as low as 260 $V_{DC}$, the amount of capacitance required to continue providing full-load current is in the 900 µF range, which is far lower than the 2.5 mF estimated above, enabling higher power density.

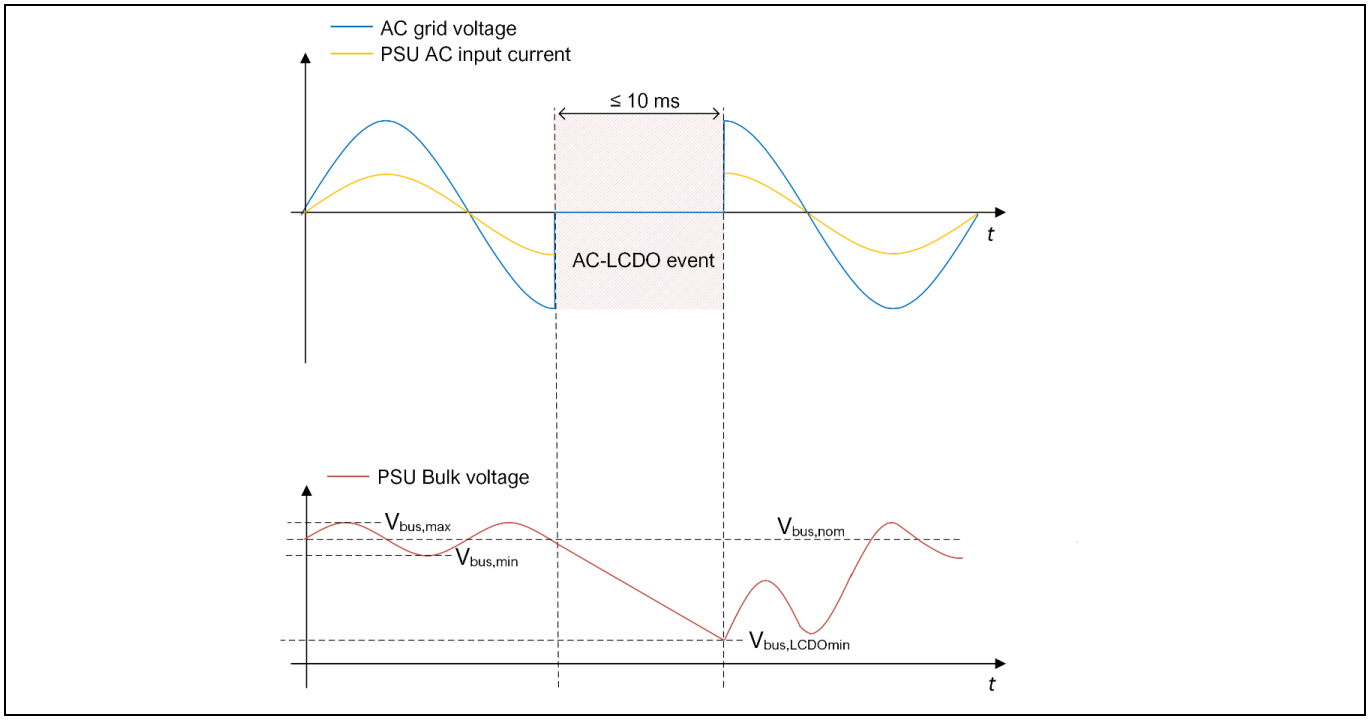



**Figure 29 Simplified waveforms of the AC voltage, AC current, and bulk voltage during a 10 ms LCDO event**

Figure 30 shows an excerpt of the schematic of the baby-boost converter implemented in EVAL_3K3W_ARCP_PSU, where $V_{bulk}$ is the bulk voltage (input of the baby-boost converter), and V+ is the input voltage of the LLC DC-DC back-end stage (output of the baby-boost converter).

During an ACLCDO event, the static switch Q3 disconnects the V+ and the $V_{bulk}$ rails, and as soon as an undervoltage is detected together with absence of grid voltage, the baby-boost starts operating to bring the V+ voltage back to the nominal value allowing a deeper discharge of the bulk cap voltage.

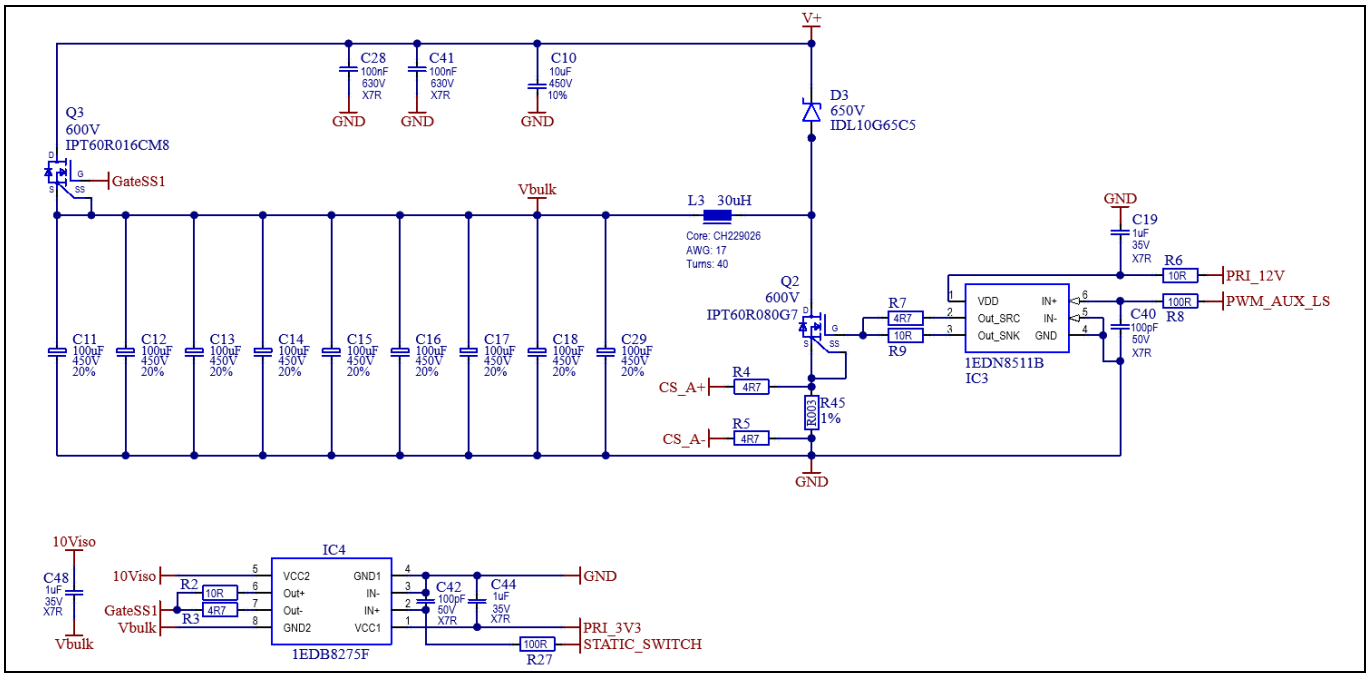



**Figure 30** **Schematic of the baby-boost circuity on the main board to comply with (AC line-cycle dropout) ACLDO specs**

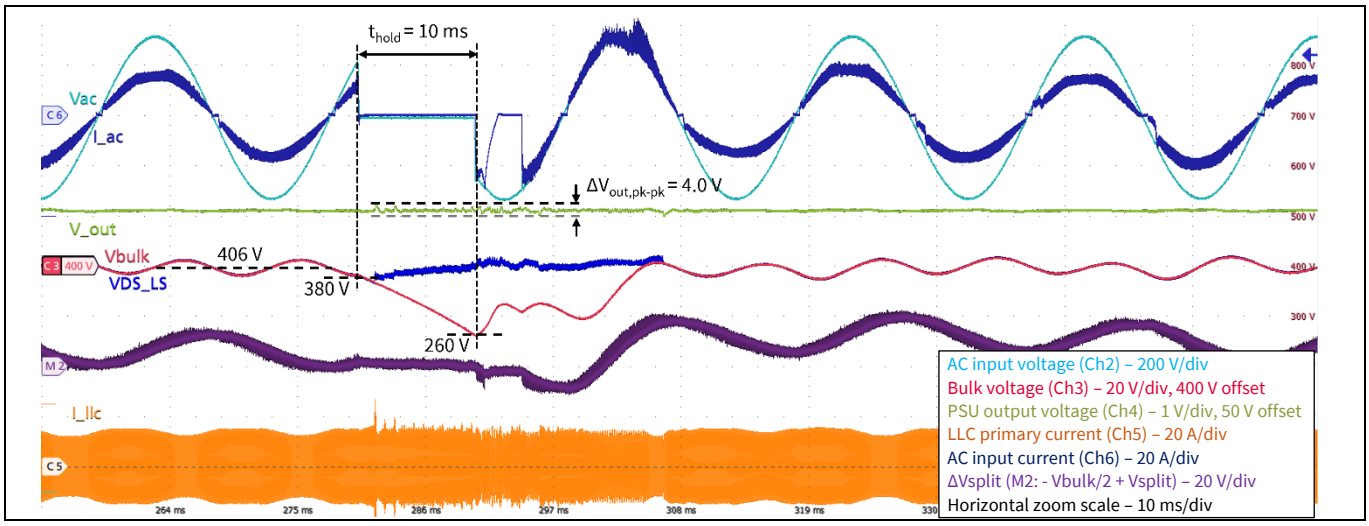



**Figure 31** **Baby-boost operation during ACLDO event at 100 percent load**

# 4 Experimental results

## 4.1 Power supply unit specifications

This section presents the specifications, performance, and the behaviour of the PSU for each single block and the overall PSU. Table 4 shows the required performance and specifications under several steady-state and dynamic conditions. Efficiency, THD, and PF results are obtained using the WT5000 power analyzer from Yokogawa, alongside waveform analysis with the MSO56 (2 GHz; 6.25 GS/s) oscilloscope from Tektronix.

**Table 4 Summary of specifications and test conditions for the 3300 W PSU**

| Test | Conditions | Specification |
|---|---|---|
| Input voltage $V_{AC}$ | – | 180 $V_{AC}$ to 275 $V_{AC}$ |
| Output voltage $V_{DC}$ | Input 230 $V_{AC}$ at 50 Hz | 50 $V_{DC}$ nominal |
| Output power | Input 180 $V_{AC}$ to 275 $V_{AC}$ | 3300 W |
| Steady-state ripple (max.) | – | ± 500 mV peak-to-peak max. |
| Efficiency test (full PSU including fan) | Input 230 $V_{AC}$ at 50 Hz 30% to 100% of full-load | 97.82% peak |
| | | 97.24% min. |
| | Input 230 $V_{AC}$ at 50 Hz 10% to 30% of full-load | 94% min. |
| iTHD (max.) | 230 $V_{AC}$ at 50 Hz; 5-10% load | 25% |
| | 230 $V_{AC}$ at 50 Hz; 10-30% load | 20% |
| | 230 $V_{AC}$ at 50 Hz; 30-100% load | 5% |
| Power factor | 30% to 100% load | 0.99 min. |
| Dynamic response (output voltage overshoot) | 10% to 50% load; 20 Hz; 1 A/µs | 0.55 V max. |
| | 10% to 90% load; 20 Hz; 1 A/µs | 1.0 V max. |
| Hold-up time | 100% load | 10 ms min. |
| Overcurrent protection (OCP) | Shut down and latch | >68 A |
| Overvoltage protection (OVP) | PFC bulk voltage | 440 $V_{DC}$ |
| Undervoltage protection (UVP) | PFC bulk voltage | 250 $V_{DC}$ in LCDO conditions |
| AC Line cycle dropout (LCDO) | 100% load | 10x [10 ms dropout, 100 ms interval] |
| Brownout | AC voltage | 180 $V_{AC}$ on, 176 $V_{AC}$ off |

## 4.2 Steady-state performance and waveforms

### 4.2.1 PSU efficiency and power losses

Figure 32 shows the efficiency measurements for steady-state operation of the full PSU at different AC voltages. The efficiency measurements have been obtained with a WT5000 power analyser with 5 kHz input and no output line filters at 50 Hz line voltage, and excluding the fan power consumption.

The fan has been powered externally at 12.4 V. The spaces between the metal chassis and the plastic shroud have been taped in order to mimic the airflow that a steel server or data center PSU would have, as shown in Figure 48. The measurement point for the input voltage is right before the insertion of the input connector into the PCB, while the output voltage measurement point is the output connector.

*Note: Due to production and measurement tolerances, variations of ±0.1% can be observed.*

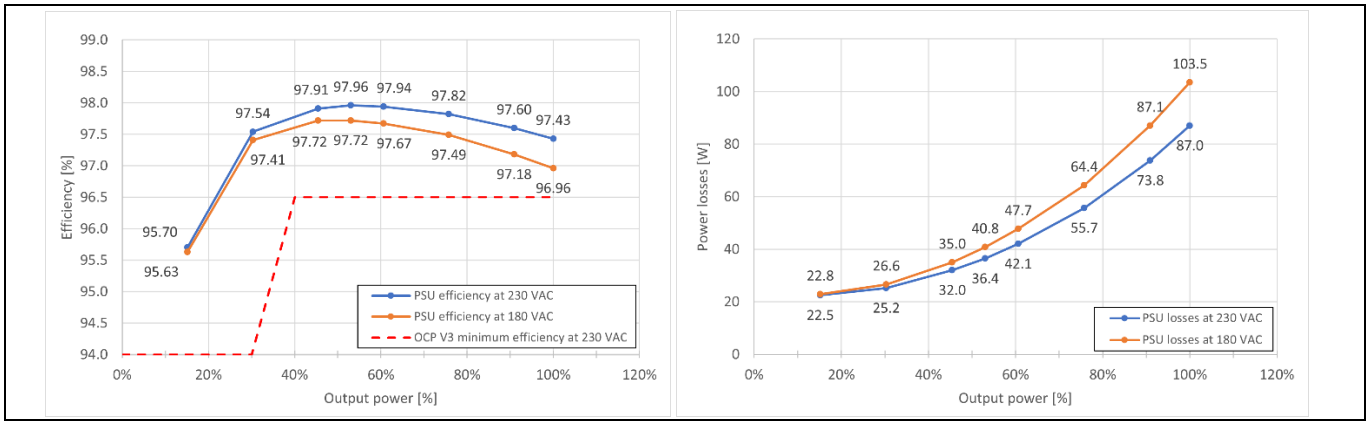



**Figure 32 Measured efficiency and power losses of EVAL_3K3W_ARCP_PSU (no fan) for different input line voltages at 50 Hz, with comparison to minimum OCP efficiency targets**

Figure 33 shows the efficiency measurements for the steady-state operation including fan power consumption and internal fan supply. Fan speed is not optimized for minimum power losses at the peak efficiency point.

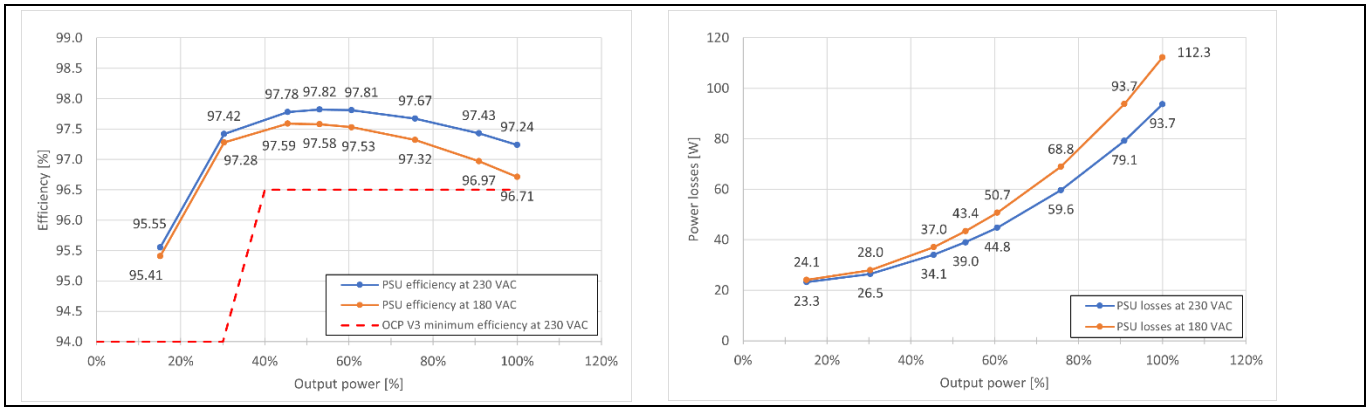



**Figure 33 Measured efficiency and power losses of EVAL_3K3W_ARCP_PSU (with fan) for different input line voltages at 50 Hz**

### 4.2.2 Output and bulk voltage ripple

The bulk voltage ripple is kept within ±15 V in steady state at full load, the average bulk voltage is set to 406 V. The voltage ripple of the output is 450 mV nominally peak-to-peak. The LLC varies its switching frequency to keep the output voltage as low as possible. This means that the LLC switching frequency has a maximum of about 520 kHz at the peak of the bulk ripple, while having a minimum of about 400 kHz at the valley of the bulk ripple. This frequency change is shown in Figure 35 and Figure 36.

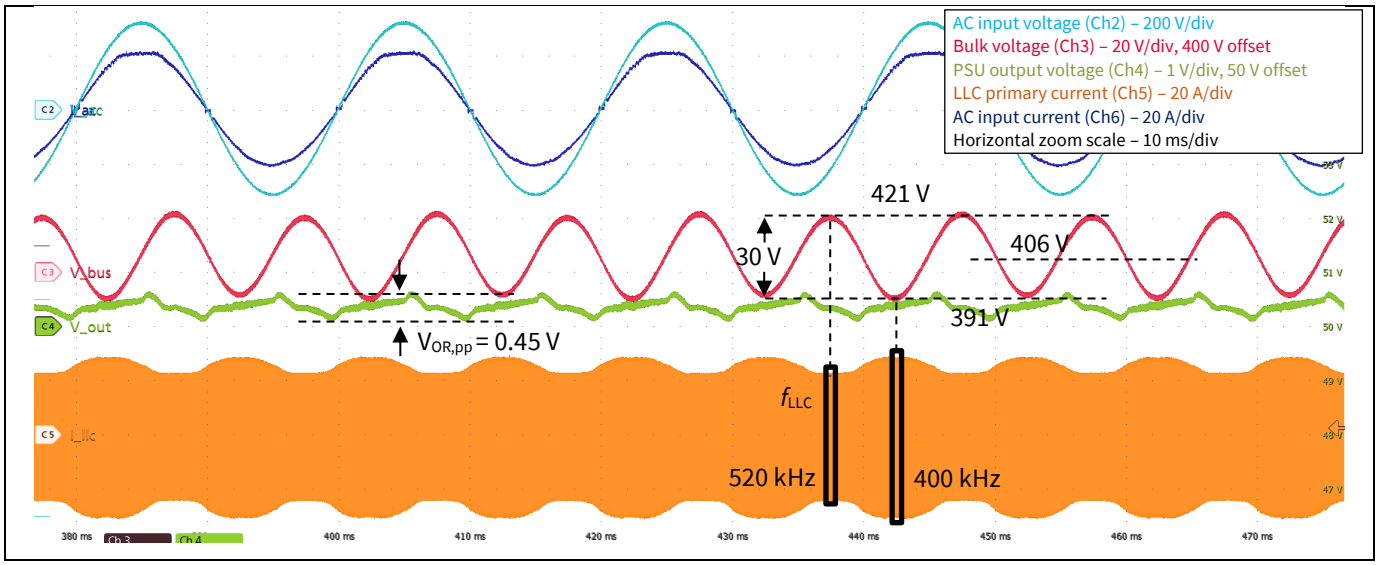



**Figure 34 Output voltage ripple for 100% load condition**

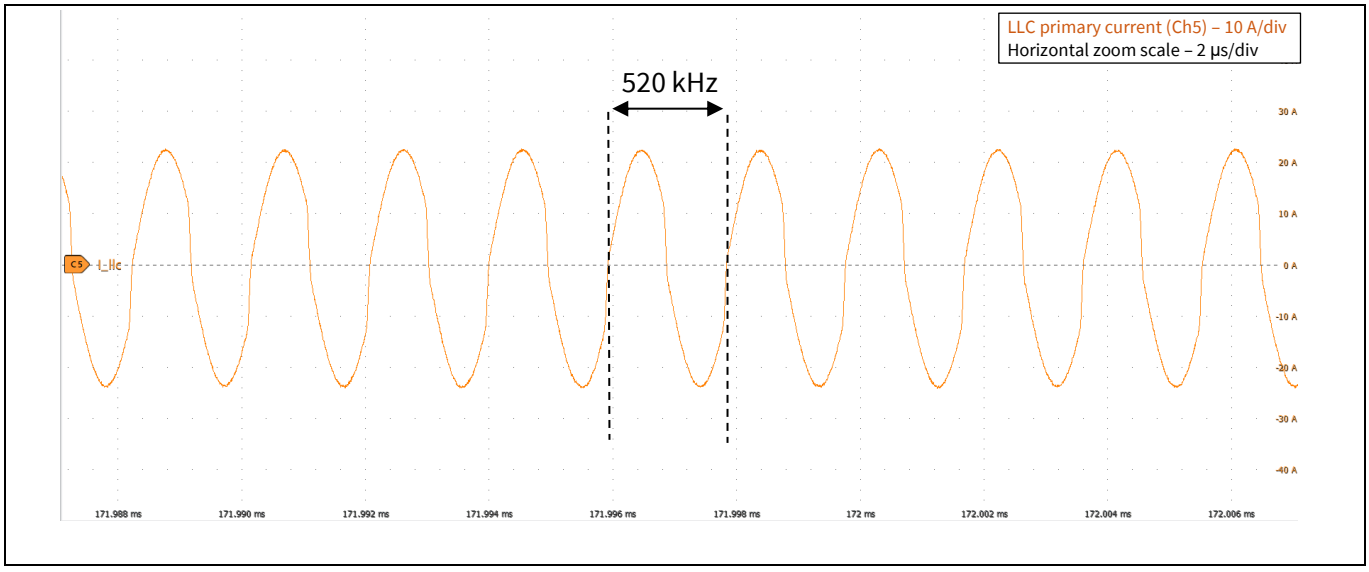



**Figure 35 LLC primary current at full-load, steady-state for maximum bulk voltage**

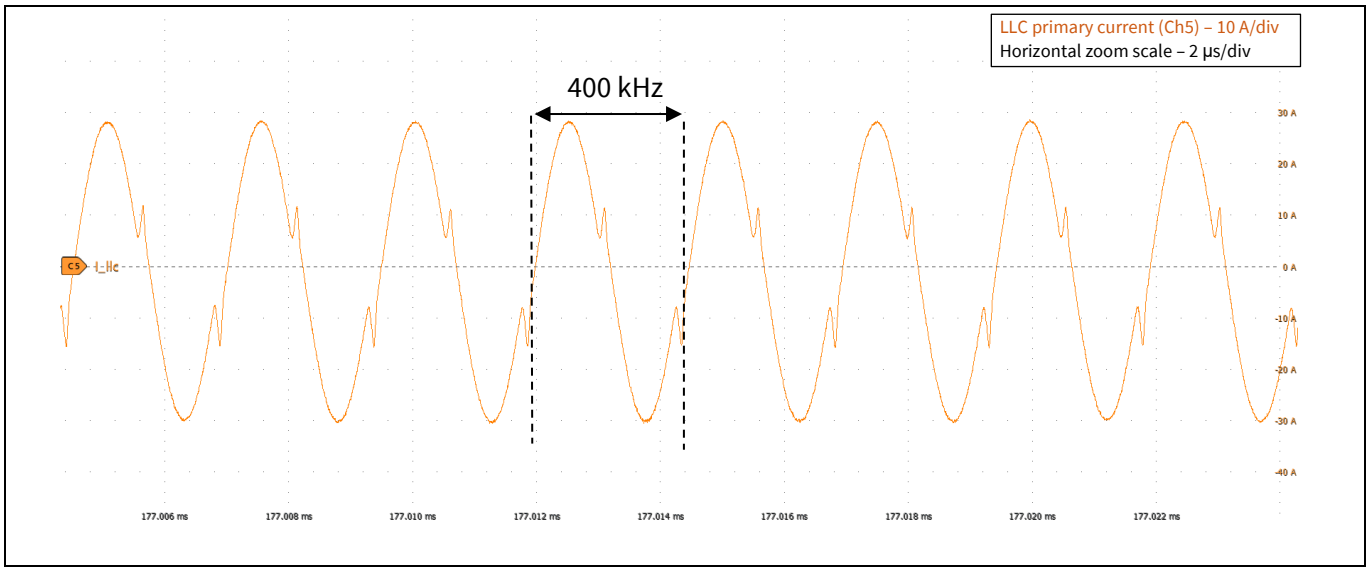



**Figure 36 LLC resonant current at full-load, steady-state for minimum bulk voltage**

Figure 37 shows that the output voltage ripple at light load conditions remains within 130 mV. The bulk voltage does not vary significantly, which means that the LLC frequency works at a narrow range of about 520 kHz.

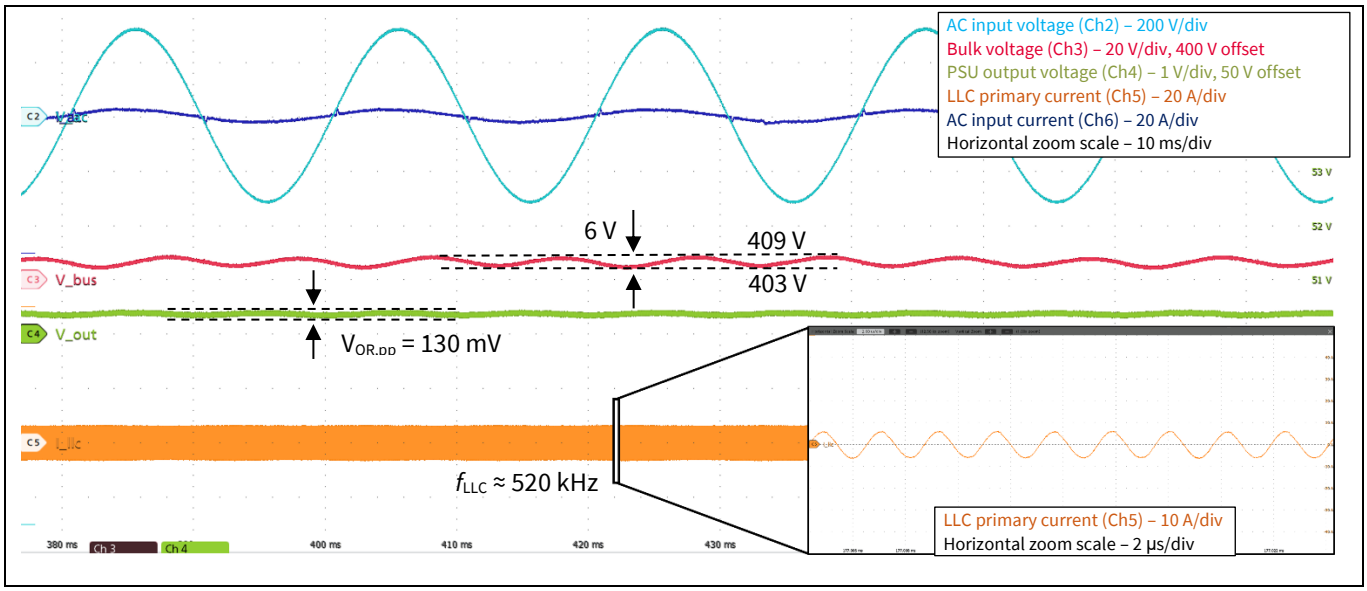



**Figure 37 Output voltage ripple for 10% load conditions**

## 4.2.3 PSU startup

When the AC is applied to the board, first the main flyback transformer begins operation to regulate the 12 V rail. After that, other rails such as the 3.3 V primary, the +9 V -3 V bias of the high-frequency leg and the secondary bias voltages raise to their nominal values. The XMC™ 4200 MCU is then initialised, and the AC line is monitored to check if the voltage is within range. If it is, the relay which shorts the NTC of the input is enabled, and the PFC synchronous rectification are enabled. The voltage of the bulk is increased by the PFC while running in open voltage loop, with a steadily increasing voltage reference until it reaches the nominal bulk voltage. At this point, the PFC side soft-start is completed and a signal is sent to the LLC controller that allows it to start.

The LLC begins the soft-start procedure by starting from a high-switching frequency and reducing it until reaching the nominal output voltage. After that, the LLC is run in normal operation, which is able to keep the output voltage steady regardless of the output power.

The sequence from the beginning of the PFC operation until the output voltage is nominal and stable takes about 60 ms, while the ramp up of the output voltage from 10% to 90% is about 7 ms at 50% of the rated load.

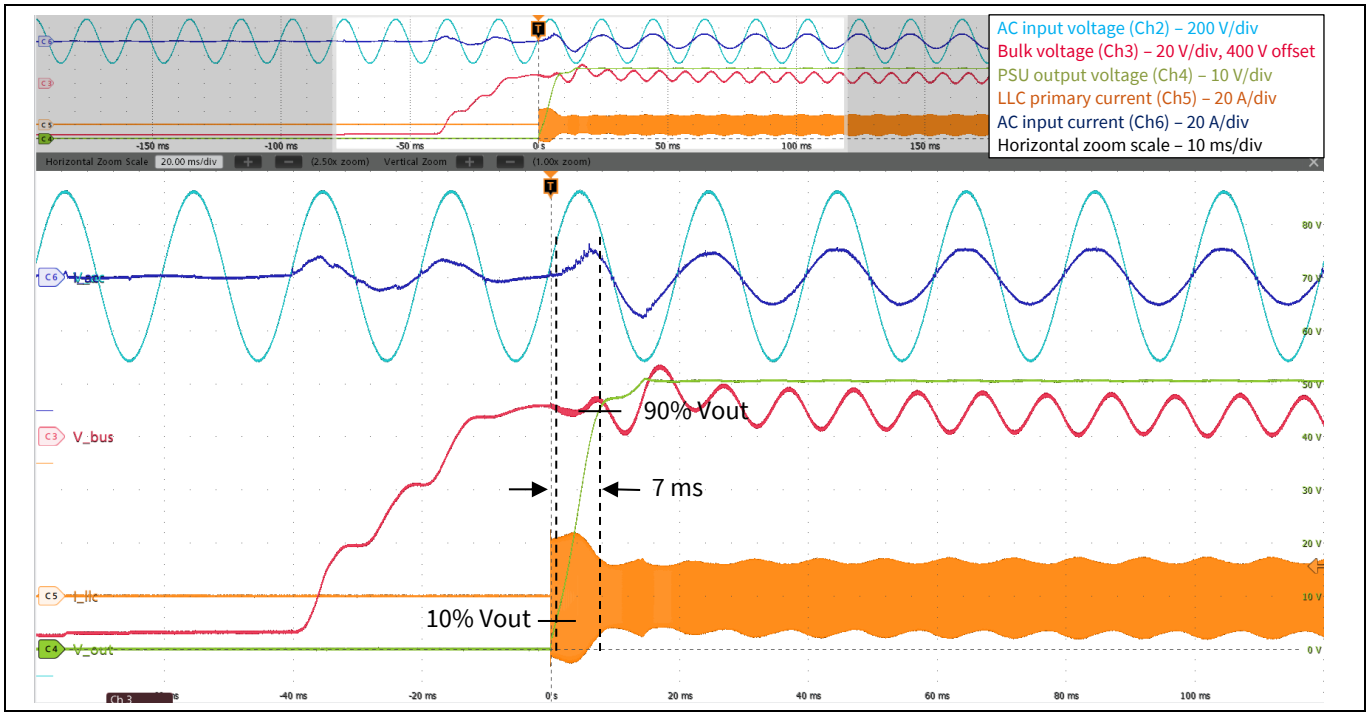



**Figure 38 PSU startup at 50% output load**

## 4.2.4 ARCP totem-pole PFC

This section presents the performance and waveforms of the AC-DC front-end converter of EVAL_3K3W_ARCP_PSU board.

### 4.2.4.1 Steady-state performance of the PFC conversion stage

Figure 39 shows the efficiency measurements for steady-state operation of only the PFC at different AC voltages. The efficiency measurements have been obtained with a WT5000 power analyzer with 5 kHz input and no output line filters at 50 Hz line voltage, excluding the fan power consumption. The fan has been powered externally at 12.4 V, and the spaces between the metal chasis and the plastic shroud have been taped in order to mimic the airflow that a steel server or data center PSU would have, as shown in Figure 48. The measurement point for the input voltage is right before the insertion of the input connector into the PCB, while the output voltage measurement point is in one of the bulk capacitor pins.

*Note: Due to production and measurement setup tolerance, worst-case efficiency variations of a maximum of ±0.1% can be observed.*

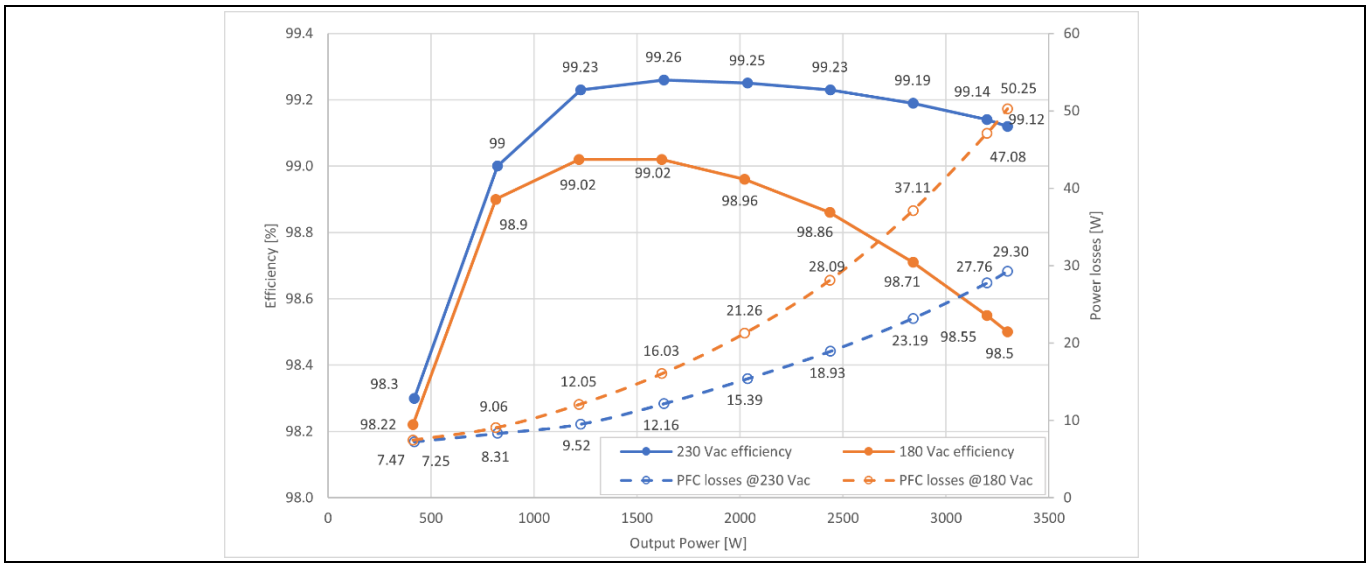



**Figure 39 Measured efficiency of the PFC standalone at different RMS input voltage and 50 Hz (no fan)**

Figure 40 depicts the total input current harmonic distortion (iTHD) and power factor measured at 230 $V_{AC}$ and 180 $V_{AC}$ line voltages at 50 Hz. The iTHD and PF measurements have been performed with the full PSU operating in steady-state conditions.

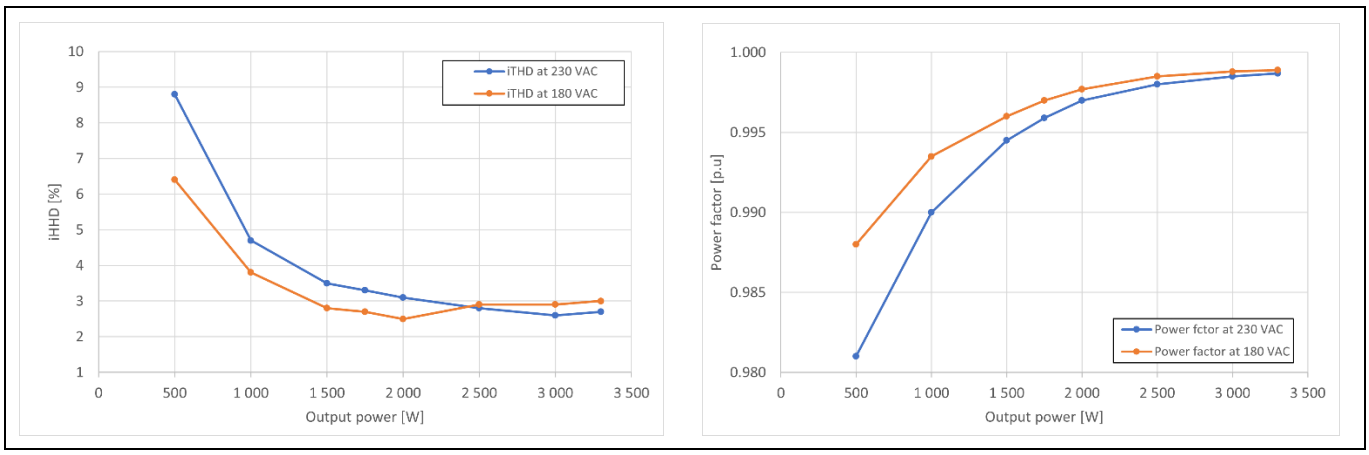



**Figure 40 Measured iTHD (a) and PF (b) at different RMS voltages for 50 Hz high-line 230 $V_{AC}$ and 180 $V_{AC}$ line voltage**

## 4.2.4.2 PFC steady-state waveforms and zero crossing

Figure 41 and Figure 42 show the key waveforms of the PFC operation at full load at 230 $V_{AC}$ and 180 $V_{AC}$ respectively. The inductor current has a sinusoidal shape while having a ripple which is highest at the peak of the AC cycle. The addition of the ARCP to the TP-PFC does not change the shape of the inductor current. At 180 $V_{AC}$, the current has a peak of 26 A plus the ripple. The drain-to-source voltage of the switches is similar to a classic TP-PFC, but the transition of diode to swich is soft-switched, as shown in Figure 44 and Figure 45.

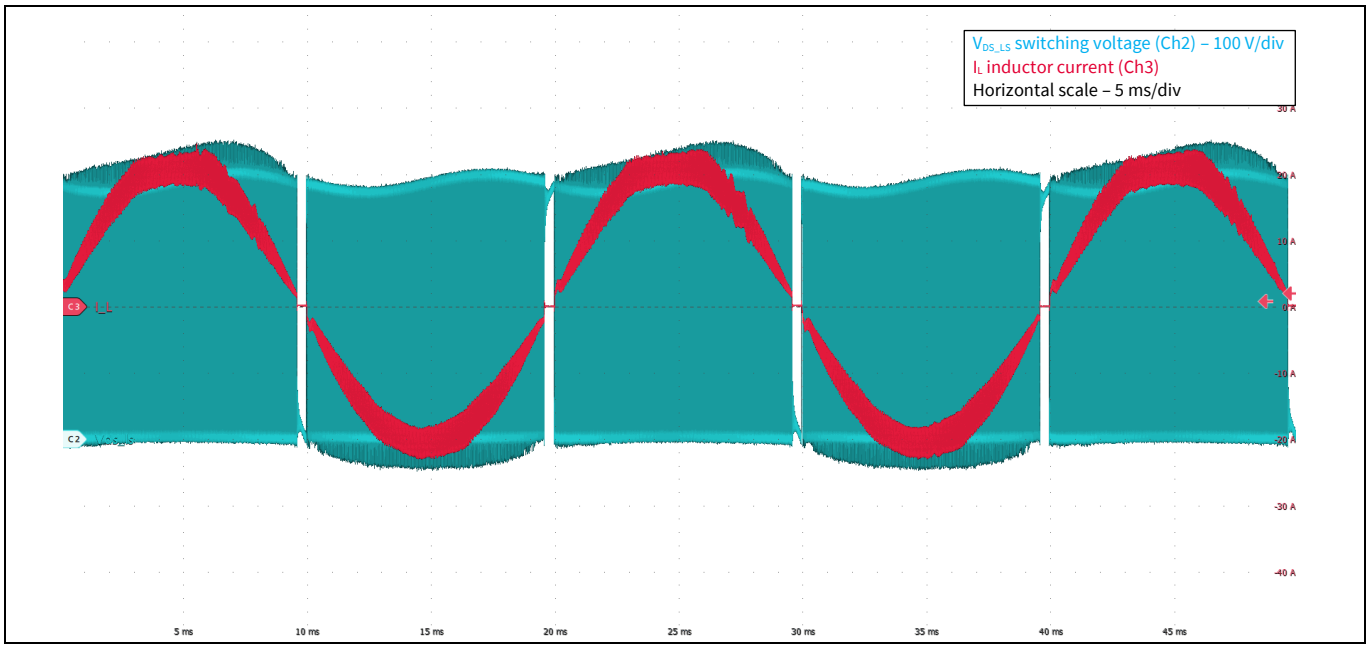



**Figure 41** **PFC steady-state operation at 230 $V_{AC}$, full-load: Current through the inductor choke and VDS_LS**

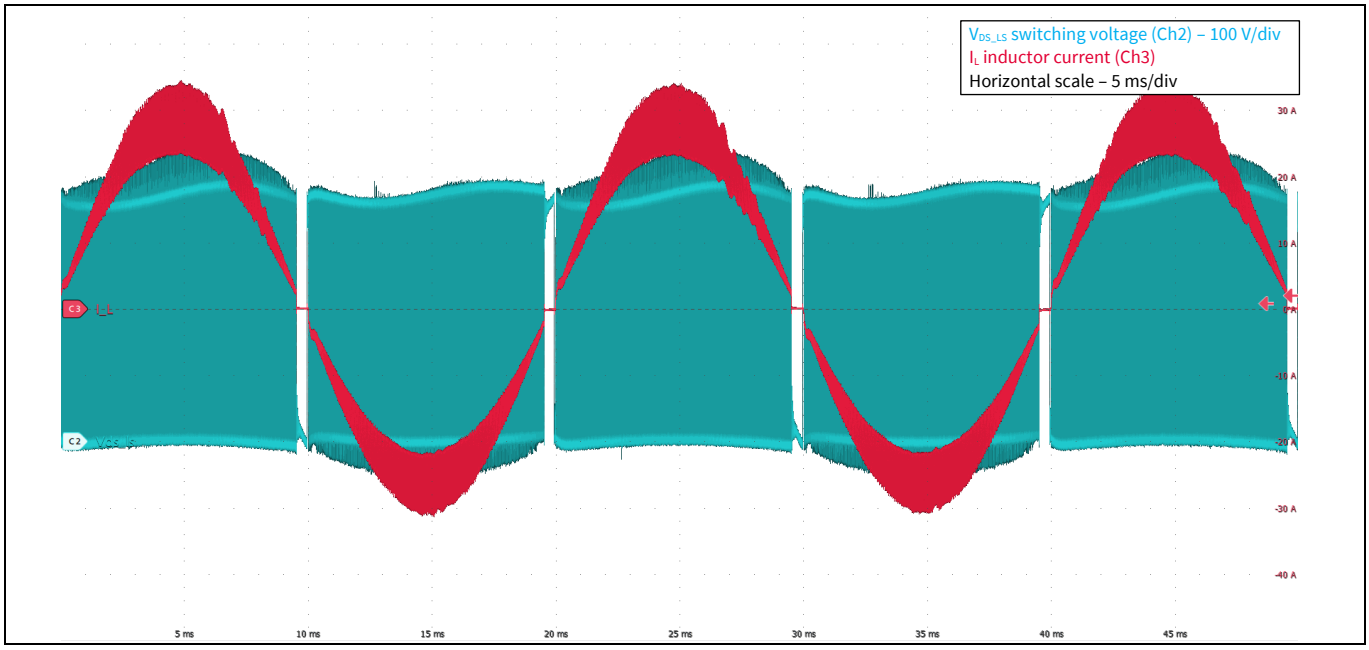



**Figure 42** **PFC steady-state operation at 180 $V_{AC}$, full-load: Current through the inductor choke VDS_LS**

Figure 43 shows the delay between PFC switching cycles when a zero crossing is detected. There are about 400 µs from the last pulse of a half-cycle until the first pulse of the next half-cycle.

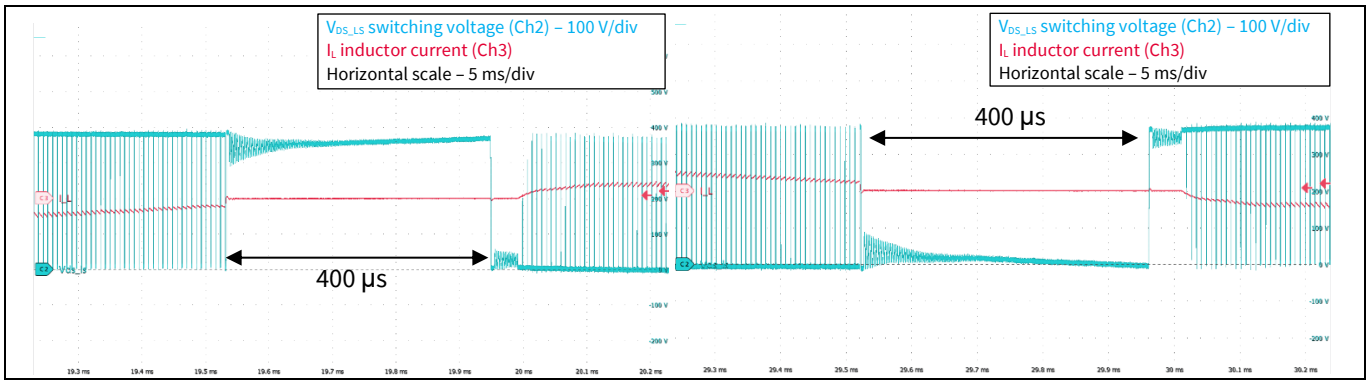



**Figure 43 Detailed waveforms of zero crossings at full-load**

The addition of the ARCP to the totem-pole enables full soft switching. If the timing of the back-to-back switches is not correct, partial hard switching can occur. This would be the case if the auxiliary pole is activated or deactivated too early or too late or for too long or short time. Figure 44 and Figure 45 show how the drain-to-source voltage of the HF half-bridge looks when the ARCP correctly assists in the soft-switching of the devices for different PFC choke currents.

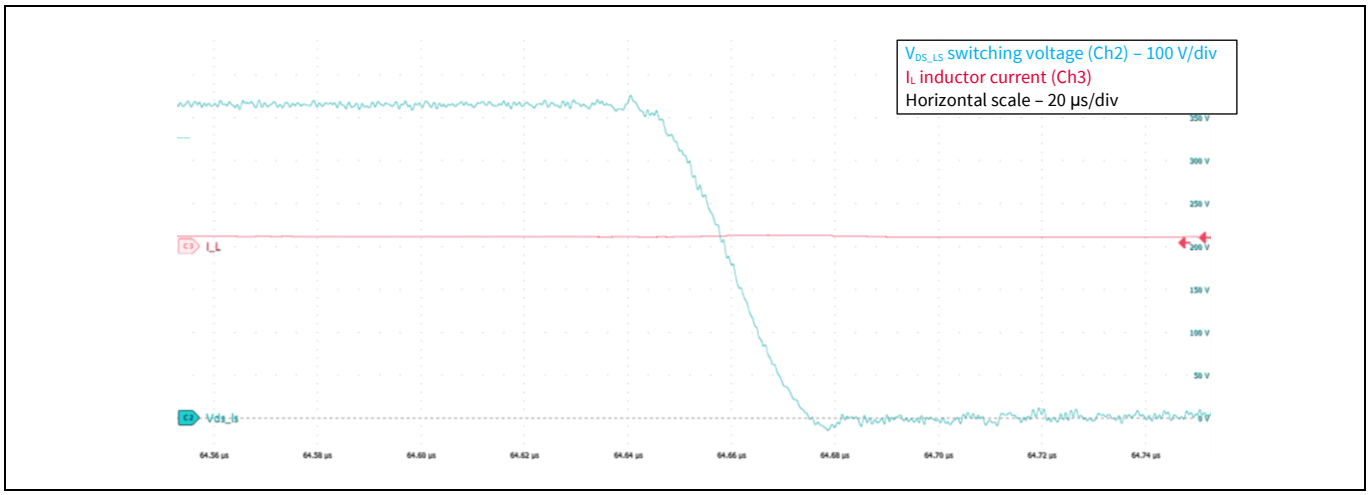



**Figure 44 Half-bridge switching node soft-switched voltage in diode to switch change at 1 A**

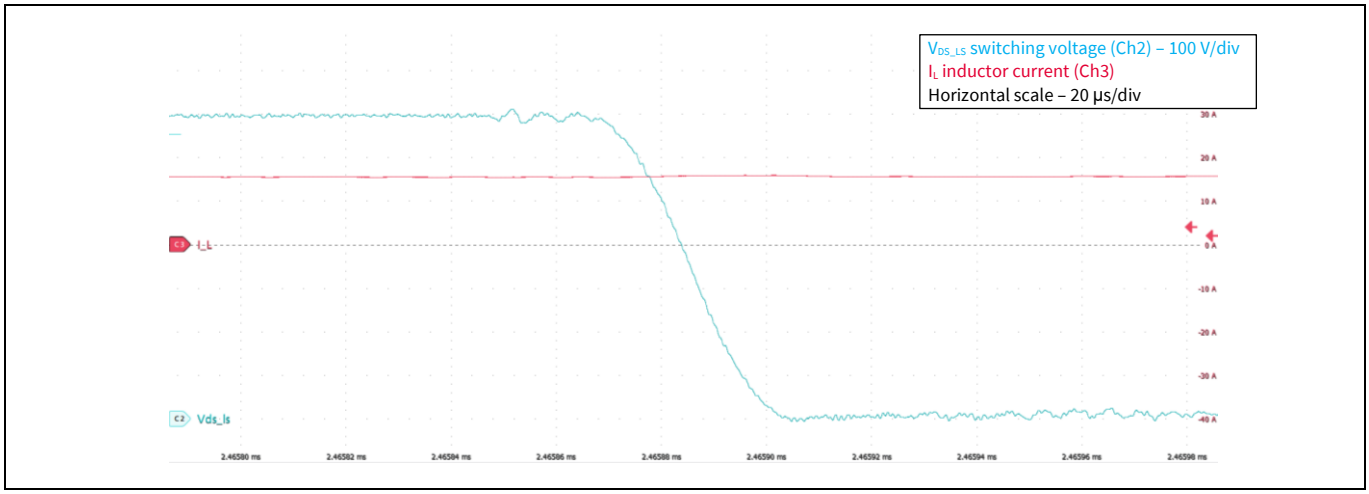



**Figure 45 Half-bridge switching node soft-switched voltage in diode to switch change at 18**

### 4.2.5 Half-bridge LLC

The half-bridge of the LLC uses CoolGaN™ IGT65R035D2 devices on the primary-side, while OptiMOS™ IQE031N08LM6CG are used for the secondary synchronous rectification. Figure 46 and Figure 47 show ZVS turn-on and the lossless turn-off of the half-bridge LLC at 100% and 50% of the rated load. The input voltage of the LLC was fixed to show the waveforms at the resonance frequency. The operation of the LLC at different frequencies and with the PFC in operation are discussed in Section 4.2.2.

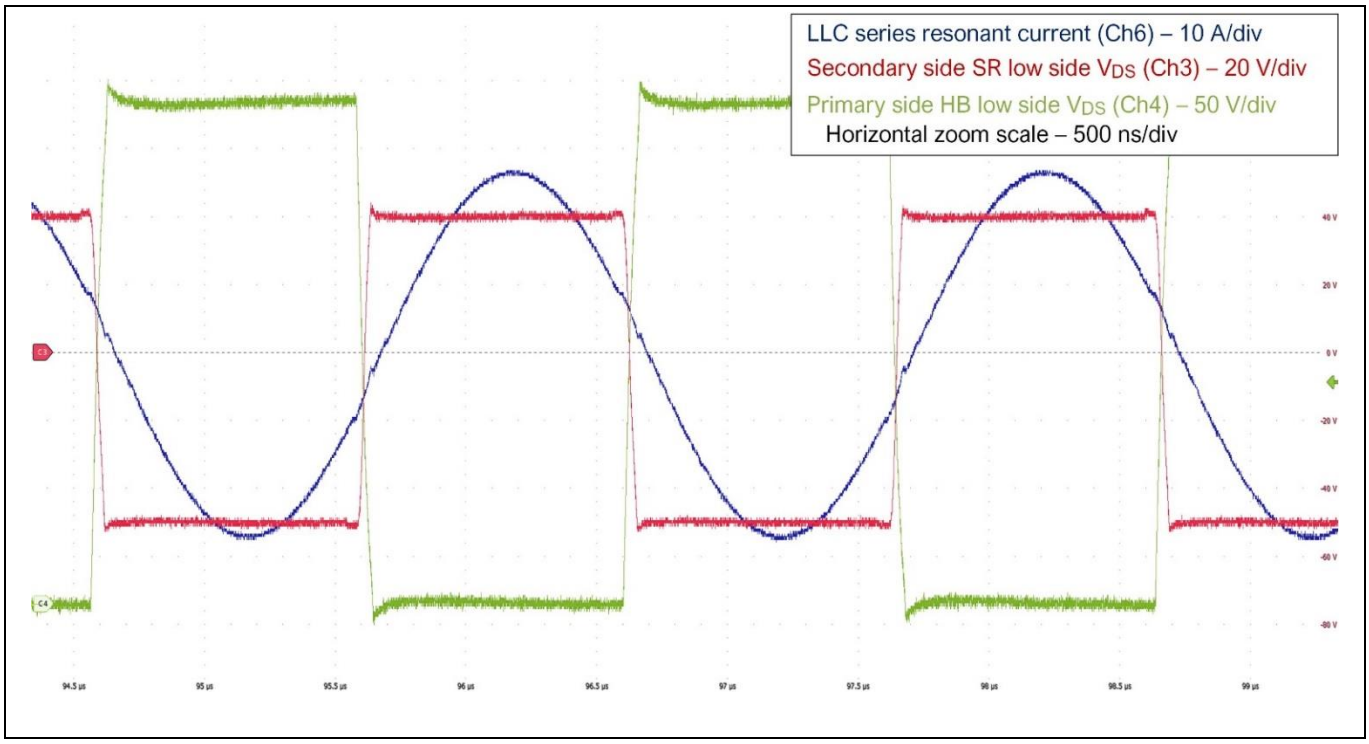



**Figure 46 LLC waveforms during steady-state operation at 100% of the rated load**

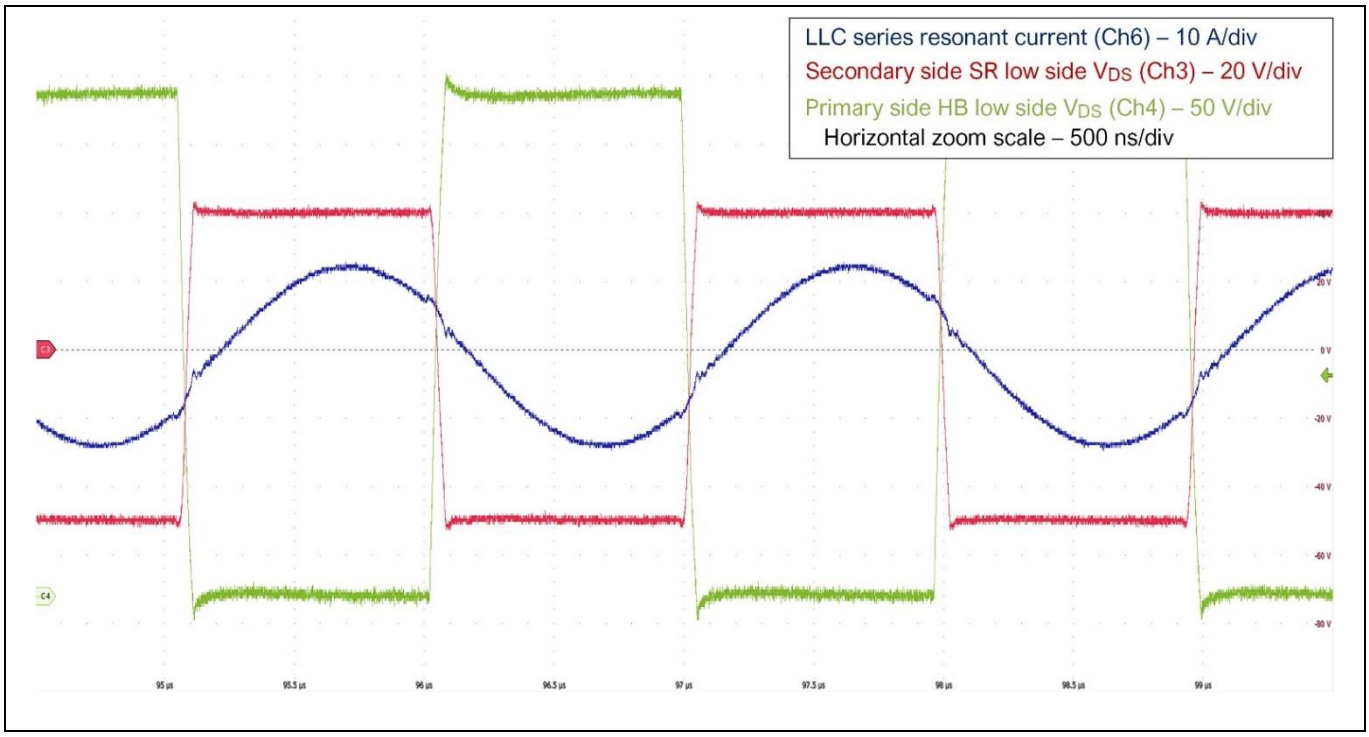



**Figure 47 LLC waveforms during steady-state operation at 50% of the rated load**

## 4.3 Thermal performance

Thermal performance of the full rectifier has been taken with Type J thermocouples, fan supplied externally, and a 25°C ambient temperature. The PSU temperature has been taken with full enclosure to provide proper cooling as the enclosure conveys the airflow through the high-temperature component through a pipe on the right-hand side of the converter. Critical hotspots such as the PFC high-frequency leg, LLC primary-side, and SR MOSFETs and drivers are shown in Figure 48.

*Note: The spaces between the metal chassis and the plastic should be taped in order to mimic the airflow that a steel server or data center PSU would have. The fan is powered internally and follows the programmed speed curve, which scales with output current and the measured temperature of the PFC and LLC NTCs.*

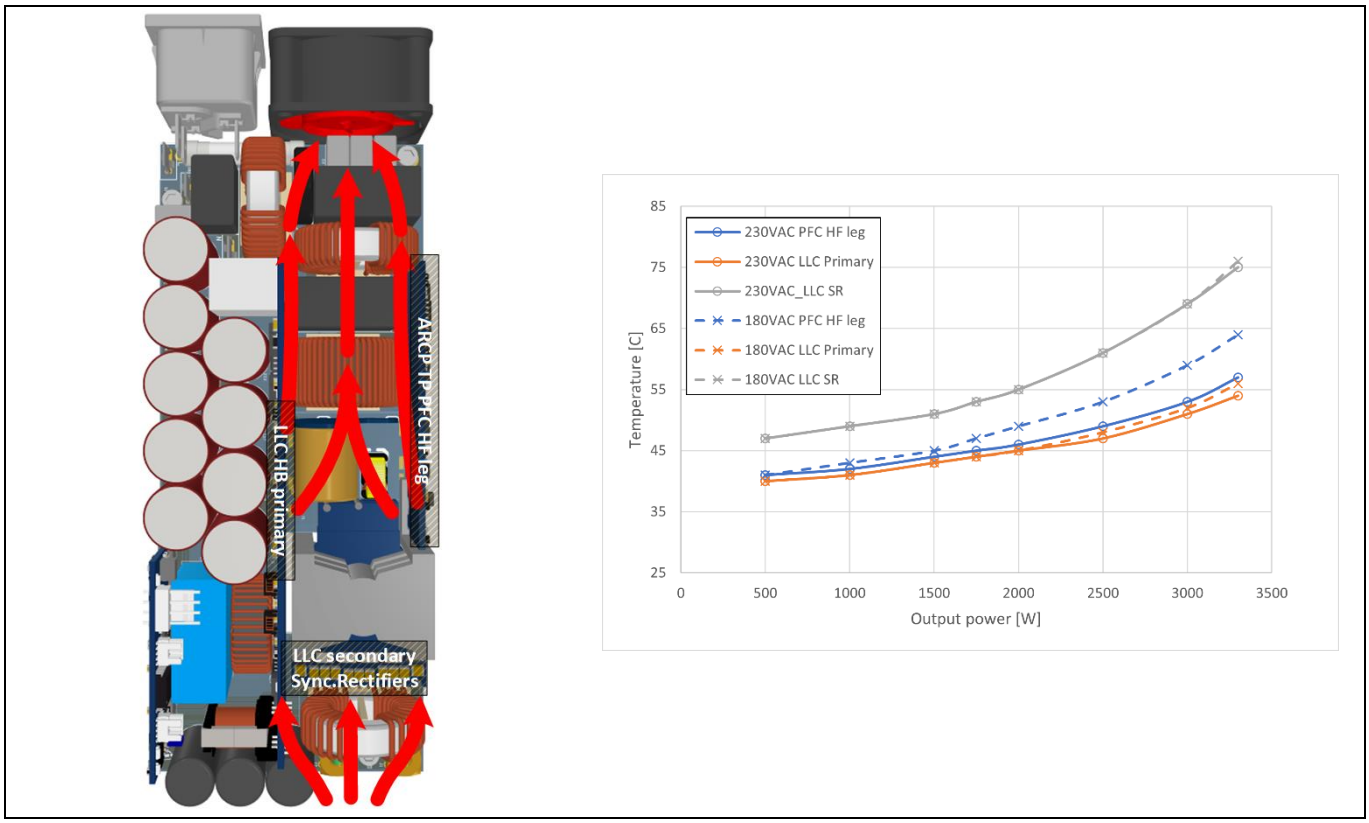



**Figure 48 PSU temperature vs. load at 180 $V_{AC}$ (dashed lines) and 230 $V_{AC}$ (solid)**

It is clear from the temperature profiles that the PSU can operate at both 230 $V_{AC}$ and 180 $V_{AC}$ input, with a maximum temperature of nearly 76°C on the LLC's synchronous rectification MOSFETs IQE031N08LM6CG. This also provides enough of a margin with respect to the maximum ambient temperature of 45°C.

## 4.4 Dynamic conditions

EVAL_3K3W_ARCP_PSU not only offers an outstanding steady-state performance as shown in the previous sections, it also complies with dynamic operation of both output load and AC input.

### 4.4.1 Load transients

The PSU has been tested for 10% to 50% and 10% to 90% load transient [1], with 1 A/µs slew rate and 20 Hz repetition-rate as shown in Figure 49 and Figure 50. Also, PSU ruggedness against zero to full-load transient and vice versa have been tested. Figure 49 and Figure 50 also show +1.0 V peak overvoltage during the 100% to 10% transient, and -0.95 V peak undervoltage during the 10% to 100% transients.

Finally, a feed-forward mechanism of the output current to the PFC voltage loop has been implemented. This allows ultra-fast recovery of the bulk voltage in less than 25 ms, which enables the PSU to withstand the transients with 20 Hz repetition-rate even without a power-buffer like the baby-boost converter, and a reduced bulk capacitance.

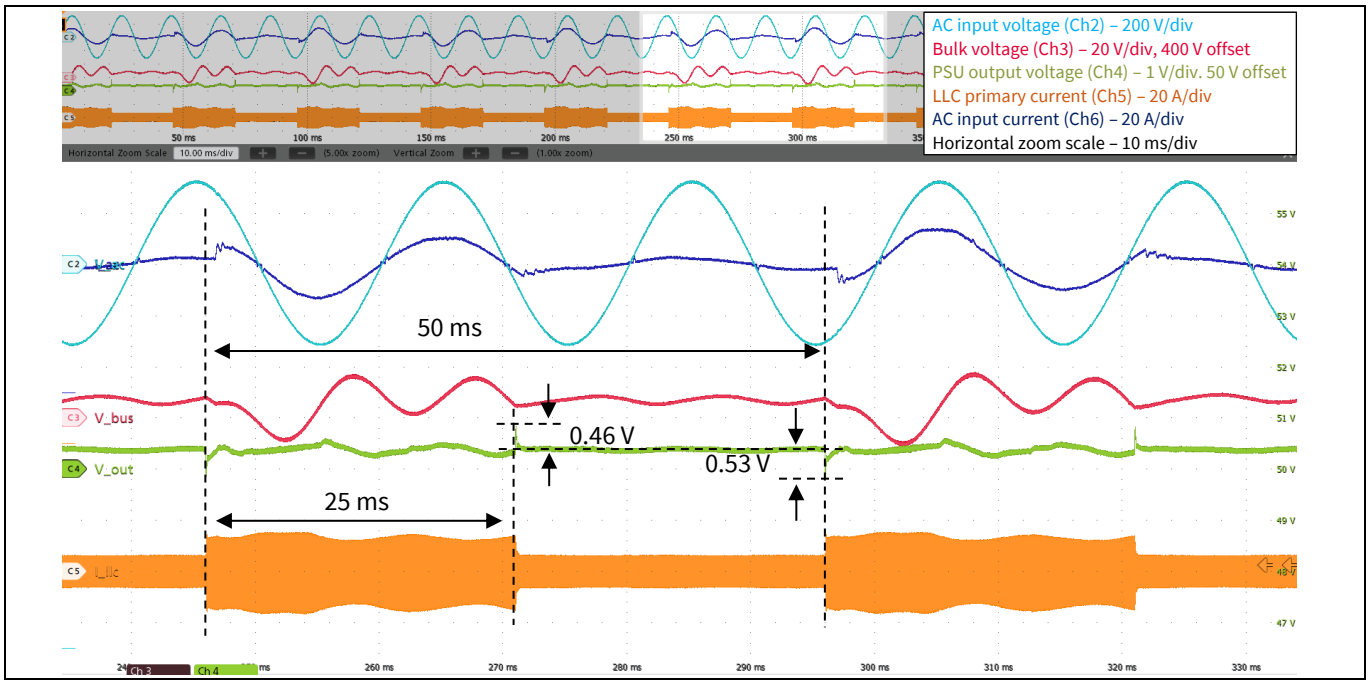



**Figure 49 10% to 50% to 10% load transients of the full PSU at 20 Hz repetition rate**

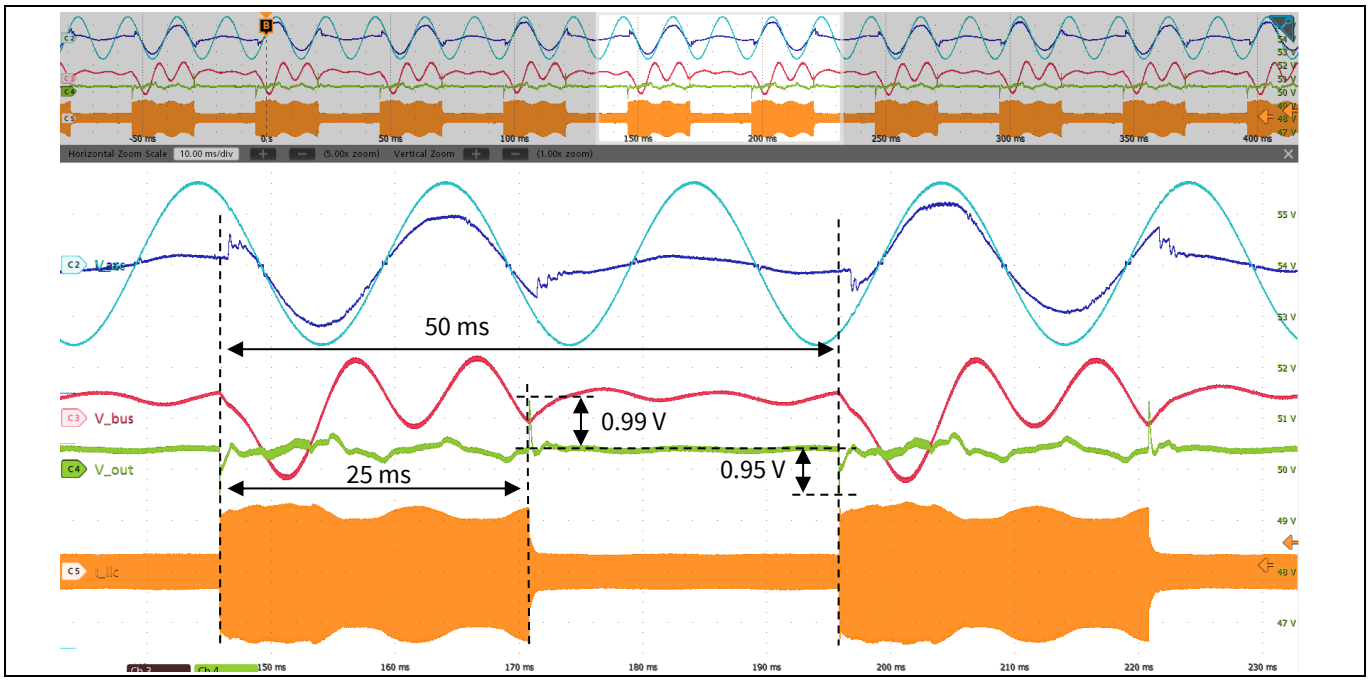



**Figure 50 10% to 90% to 10% load transients of the full PSU at 20 Hz repetition rate**

## 4.4.2 Hold-up time extension

Hold-up time extension with the baby-boost converter (see Section 3.5) has been tested within the PSU. From the steady-state operation point of view, the baby-boost stage is always disabled and triggers when a bulk voltage drop below 380 $V_{DC}$ is detected together with the absence of AC line input. At this point, the CM8 static switch opens and the voltage at the LLC input is boosted (taking the energy from a deep discharge of the bulk capacitors) until the bulk voltage achieves a cut-off threshold of 250 $V_{DC}$. Under these conditions, a minimum

hold-up time of 10 ms has been ensured at full-load until the PSU output drops, with 900 µF nominal bulk capacitance, as discussed in Section 3.5.

#### 4.4.2.1 AC line-cycle dropout

AC line cycle drop-out (LCDO) has been tested at both 50% load and full-load, with a drop of the phase voltage at both 0° and 45° (the worst condition as the bulk voltage is at the peak minimum). The LCDO is repeated ten times, each time with a 10 ms line drop, and with a period of 100 ms. The main results of the LCDO test are reported in Figure 51 to Figure 54.

During each LCDO event, the baby-boost stage is enabled as described in sections 3.5 and 4.4.2, so the bulk voltage discharges faster to a minimum voltage of 260 $V_{DC}$ during each AC line-cycle dropout (ACLDO) event. During the worst-case 100% load-abnormal condition, the output voltage remains within +/- 2.0 $V_{DC}$ of the nominal output.

The voltage of the split capacitor deviates beyond the nominal ripple seen in steady-state operation. There is no way to balance the voltage in the worst case of 0° LCDO due to the missing pulse, which either overcharges or over-discharges the capacitors. To avoid over or undervoltages and ensure the nominal operation of the PFC, the split capacitors require a way to balance the voltage. This can be achieved by the external balancing circuit, however it is space consuming.

In EVAL_3K3W_ARCP_PSU, a DC offset is added to the current reference of the input AC current – negative when the split capacitor voltage is too high and positive when it is too low. In Figure 53, the recovery of the split capacitor voltage is the most noticeable. After the AC line comes back, the voltage of the split capacitors rises above the nominal ripple, which is when the DC input current offset is enabled. The positive half-cycle currents are slightly lower than the negative ones - until the voltage returns to its nominal value - in time for the next LCDO event.

The purple waveform (M2) in the figures show the deviation of the split capacitor voltage from $V_{bulk}/2$. When the full-load LCDO occurs, the split capacitor voltage always crosses the threshold for the balancing logic, set at ±15 V. Therefore, the input current of the PFC is modified with a DC offset, which brings the voltage back to its nominal value. In the 50% load condition, however, the deviation is not always enough to trigger the balancing logic, which explains why in some cycles the voltage does not recover.

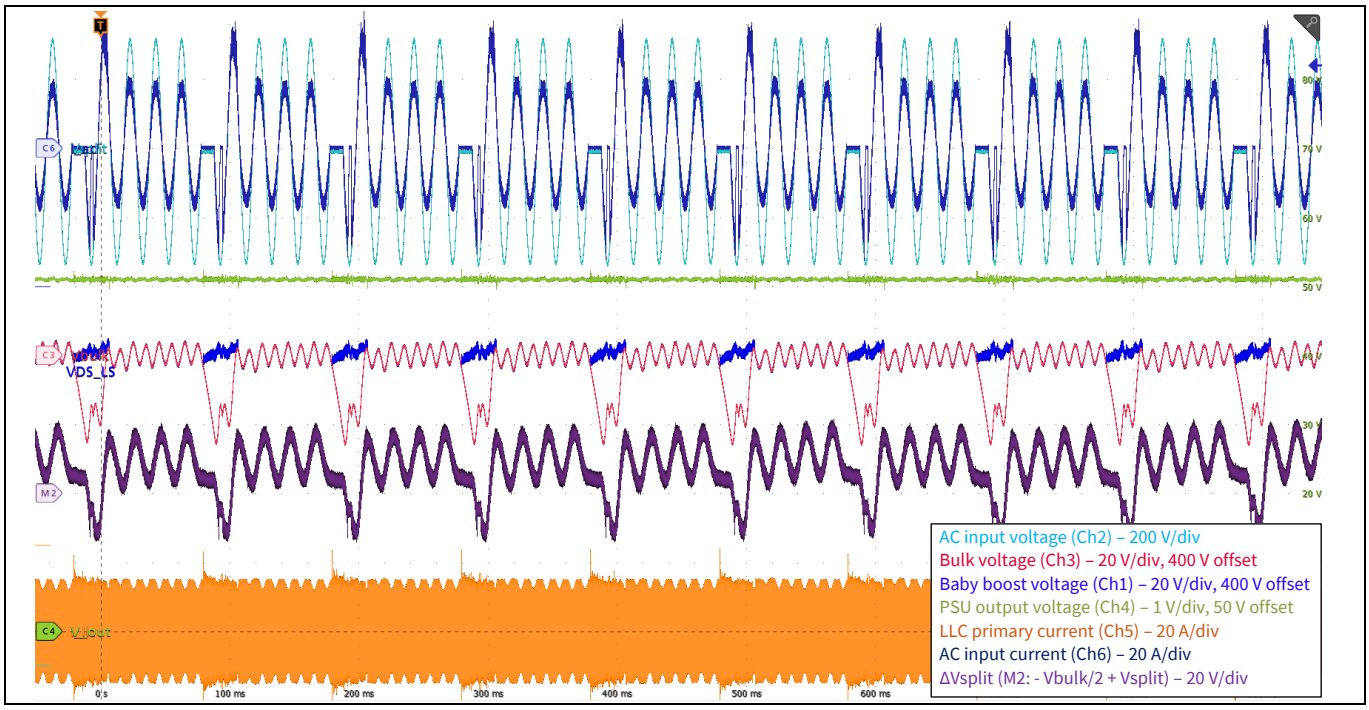



**Figure 51 ACLDO at 100% load, AC phase 0 degrees**

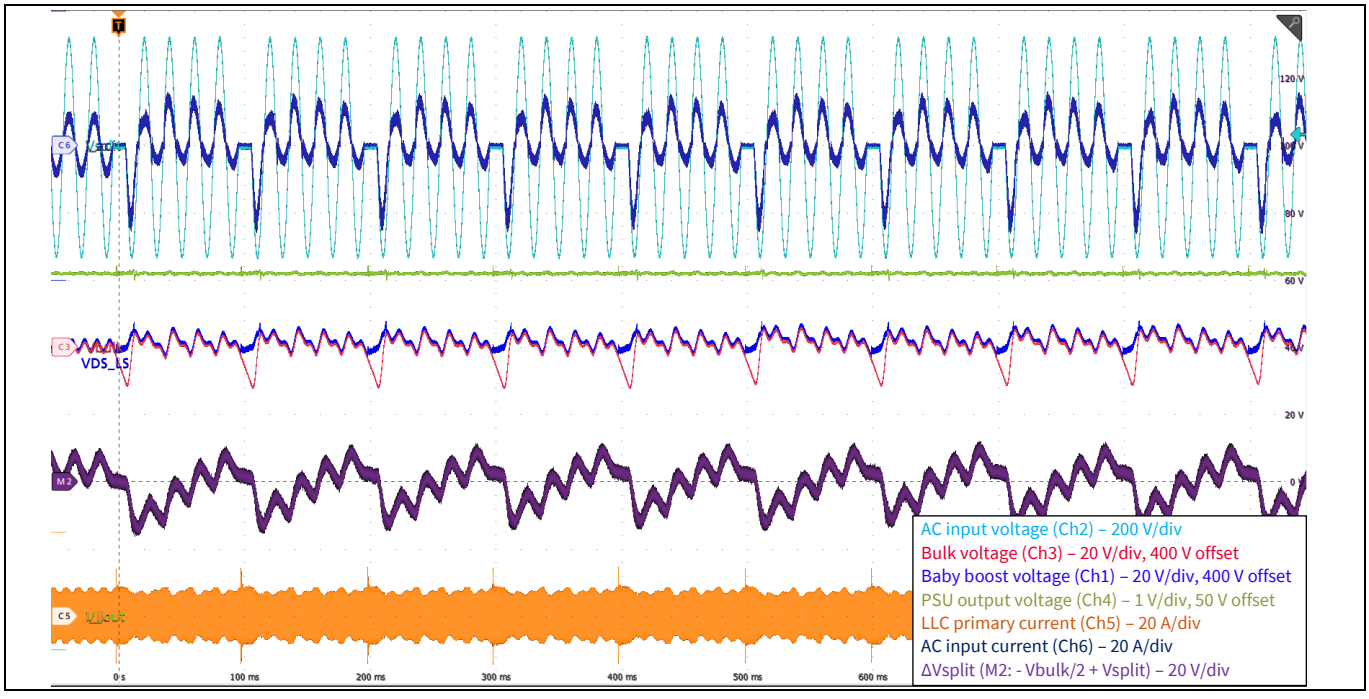



**Figure 52 ACLDO at 50% load, AC phase 0 degrees**

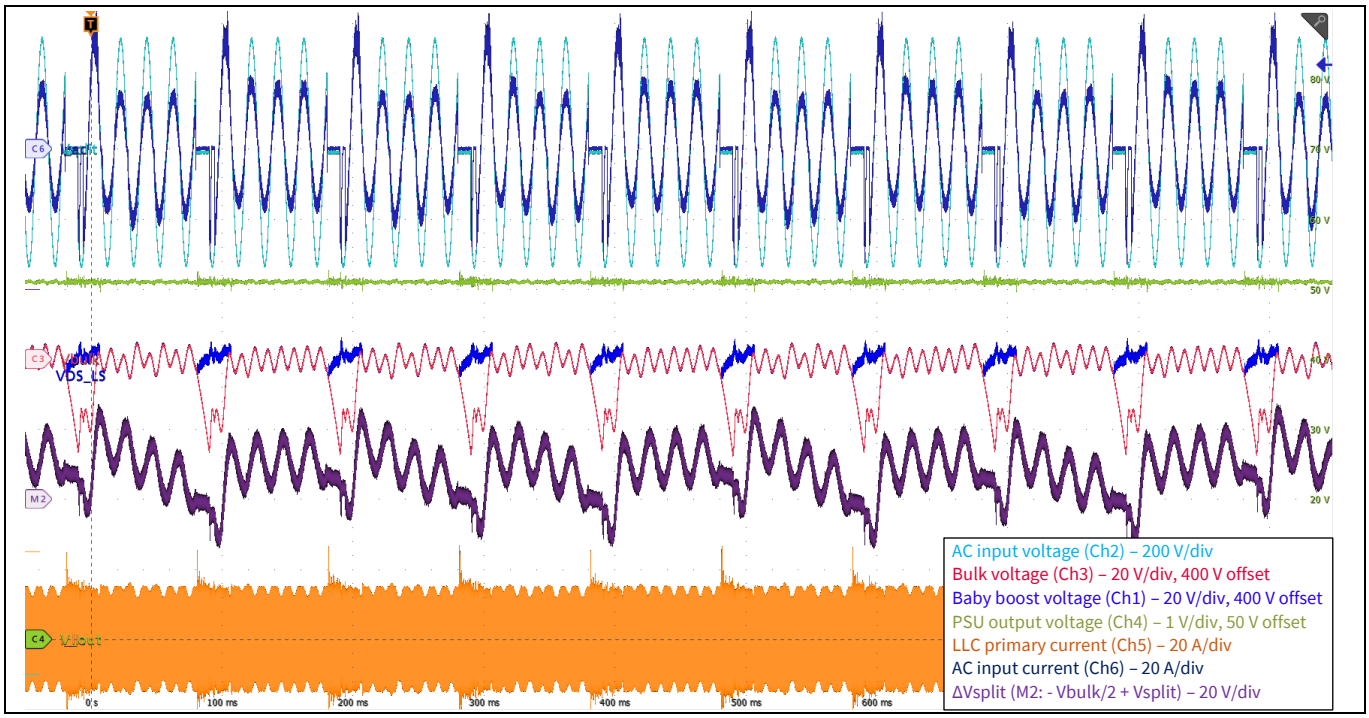



**Figure 53 ACLDO at 100% load, AC phase 45 degrees**

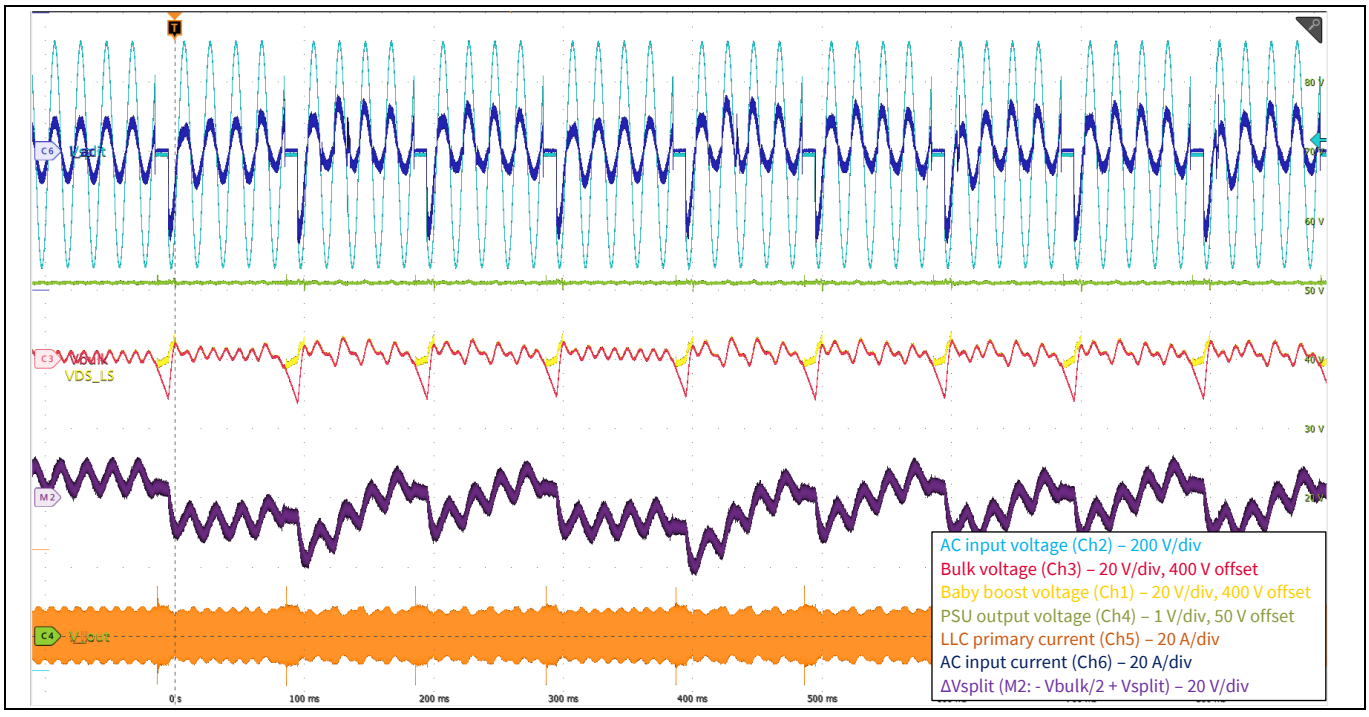



**Figure 54 ACLDO at 50% load, AC phase 45 degrees**

## 4.5 EMI measurements

The conducted electromagnetic interference (EMI) of the full PSU was measured with the setup shown in Figure 55. The AC voltage is generated by an AC source and the connection to the PFC is done with a line impedance stabilization network (LISN). The spectrum analyzer is connected to the LISN. A passive resistive load has been used for the test .

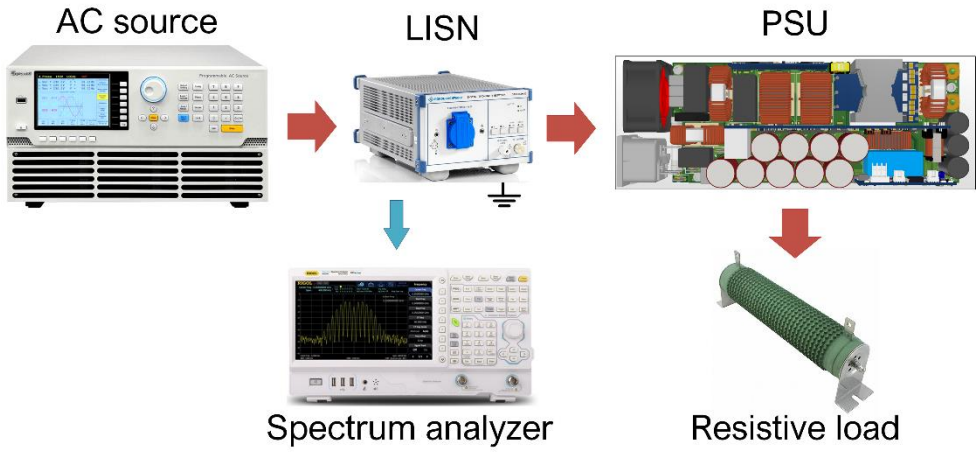



**Figure 55 Setup used for EMI test**

The EMI tests were performed for both line and neutral with an input of 230 $V_{AC}$ and 3 kW output power. Figure 56 shows the results of the average (blue) and the quasi-peak (red) measurements at 230 $V_{AC}$. The PSU is fully-compliant with Class A limits in both the peak and average measurements. Furthermore, the measured peak values represent a worst-case compared to the Quasi-peak of the Class A CISPR-22 standard. A margin of 3 dB is also always achieved.

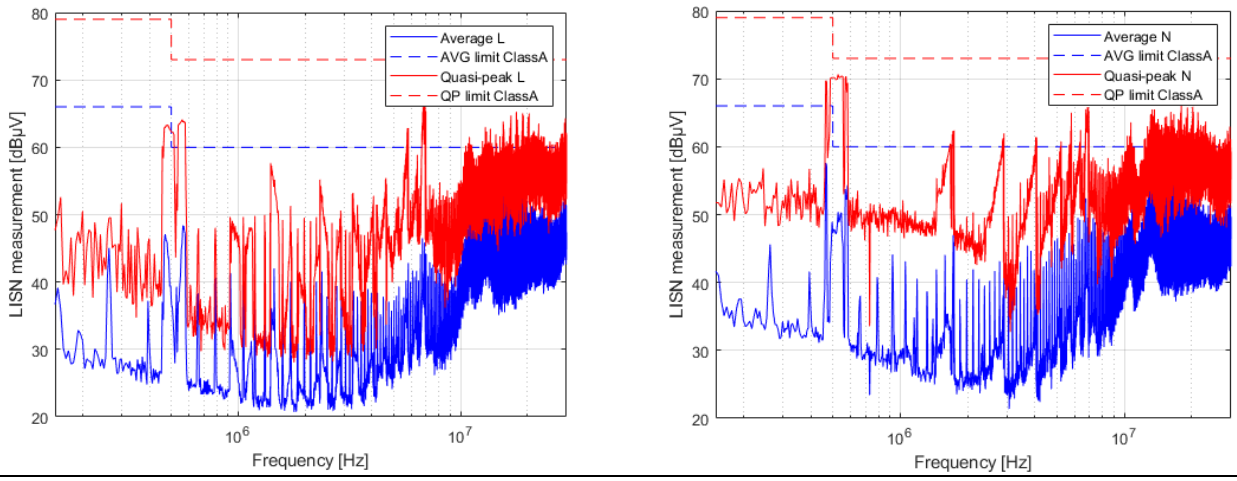



**Figure 56 AC input EMI of the PSU at 230 $V_{AC}$ input and 3 kW, and a comparison with the EN 55032 limit**

## 4.6 Efficiency comparison of EVAL_3K3W_ARCP_PSU and 3K3W_HFHD_PSU

Figure 57 shows the efficiency comparison between the EVAL_3K3W_ARCP_PSU and the EVAL_3K3_HFHD_PSU. The measurement setup is as described in Section 4.2.1. It is important to note that the efficiency test was conducted on a different bench compared to the previous measurements taken for the HDHF application note [3]. The deviation of the efficiency measurement in this setup and the efficiency reported in the application note [3] is negligible.

The figure provides a detailed comparison of the efficiency of the two boards across different AC input voltages, specifically at 180 V and 230 V. The light-load, peak, and full-load efficiency points are highlighted. EVAL_3K3W_ARCP_PSU can achieve about 0.28% higher efficiency at light load, while the peak efficiency gain is about 0.56%. At full load, the margin further increases.

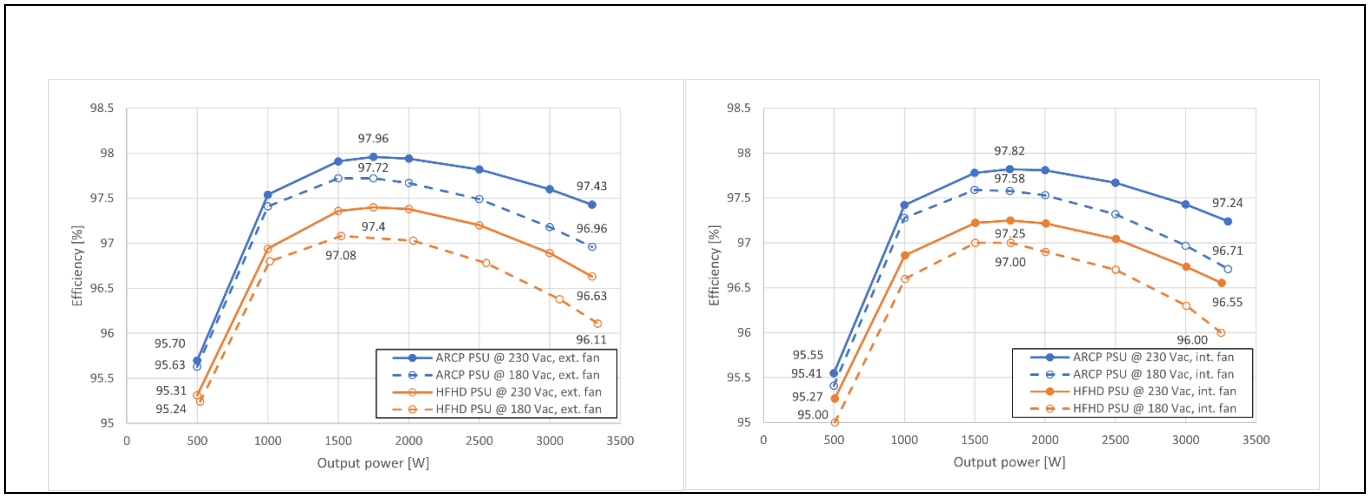



**Figure 57 PSU efficiency comparison of EVAL_3K3W_ARCP_PSU and EVAL_3K3_HFHD_PSU**

# 5 Summary

This document provides a complete system solution based on ARCP topology from Infineon designed for server PSU applications. The solution incorporates an auxiliary resonant commutated pole totem-pole PFC converter and a DC-DC isolated half-bridge LLC converter, achieving peak efficiency levels of 98% at 230 $V_{AC}$ and 97.7% at 180 $V_{AC}$, along with a power density of 98 W/in$^3$.

The EVAL_3K3W_ARCP_PSU reference board utilizes CoolGaN™ 650 V power transistors and CoolMOS™ 600 V MOSFETs in TOLL packages, and OptiMOS™ 6 in PQFN 3.3 x 3.3 package from Infineon. This combination of CoolGaN™, CoolMOS™, and OptiMOS™ MOSFETs enables high performance within a compact form factor, as detailed in this document. The ARCP PFC topology and the half-bridge LLC incorporate full digital control through an XMC™ 4000 MCU from Infineon. Using the ARCP soft-switching technique enables a considerable increase in efficiency compared to an interleaving solution (+0.36 %). The high-frequency LLC implementation with CoolGaN™ and integrated magnetic structure, including the SR OptiMOS™, significantly contributes to the overall efficiency and power density achievement.

The PSU performance excels not only in steady-state conditions, offering high efficiency, it also meets power line disturbance and hold-up time requirements with additional hold-up time boost converter, which can achieve the required 10 ms hold-up at full-load. The steady-state performance and the dynamic operation of EVAL_3K3W_ARCP_PSU is presented in this document using a programmable AC source and an electronic load.

# 6 Bill of materials

Infineon main components are marked in bold.

**Table 5 BOM for the main board M100001621**

| Designator | Value | Tolerance | Voltage | Description |
|---|---|---|---|---|
| C1, C2, C6, C7 | 4.7nF | Y2 | 300 V | Capacitor Ceramic |
| C3 | 0.82µF | X2 | 275 $V_{AC}$ | Capacitor Foil |
| C4, C5 | 2.2µF | X2 | 275 $V_{AC}$ | Capacitor Foil |
| C8, C9, C32, C33, C34, C35, C56, C57 | 10nF | 5% | 630 V | Capacitor Ceramic |
| C10 | 10uF | 10% | 450 V | Capacitor Foil |
| C11, C12, C13, C14, C15, C16, C17, C18, C29 | 100uF | 20% | 450 V | Capacitor Polarized |
| C19, C20, C21, C44, C48 | 1uF | X7R | 35 V | Capacitor Ceramic |
| C22, C23, C26, C27, C37, C43, C45, C46, C47, C49, C50, C51, C52 | 4.7uF | X8L | 100 V | Capacitor Ceramic |
| C28, C36, C38, C41, C53, C54 | 100nF | X7R | 630 V | Capacitor Ceramic |
| C30, C31, C39 | 820uF | 20% | 63 V | Capacitor Electrolyt |
| C40, C42 | 100pF | X7R | 50 V | Capacitor Ceramic |
| C55 | 100uF | X5R | 10 V | Capacitor Ceramic |
| D1, D2 | S8KCDICT | – | 800 V | Standard Diode |
| **D3** | **IDL10G65C5** | – | **650 V** | **Schottky-Diode** |
| F1 | 20A | – | – | Fuse |
| IC1, IC2 | MCR1101-50-3 | – | – | Hall Sensor |
| **IC3** | **1EDN8511B** | – | – | **Integrated Circuit** |
| **IC4** | **1EDB8275F** | – | – | **Integrated Circuit** |
| J1, J2 | 7460307 | – | – | Screw Terminal |
| L1, L2 | 1.4mH | – | – | Common Mode Choke |
| L3 | 30uH | – | – | Buffer Choke |
| L4 | 177uH | – | – | PFC-Choke |
| L6 | 32uH | – | – | Inductor |
| NTC1 | 14R | 25% | – | NTC Resistor |
| **Q2** | **IPT60R080G7** | – | **600 V** | **MOSFET** |
| **Q3** | **IPT60R016CM8** | – | **600 V** | **MOSFET** |
| R1, R17, R18, R19, R20, R21, R22, R23, R24, R29, R30, R31, R32, R33, R35, R38 | 309k | 0.1% | – | Resistor |
| R2, R6 | 10R | 1% | – | Resistor |
| R3, R4, R5, R7 | 4R7 | 1% | – | Resistor |

## Bill of materials

| Designator | Value | Tolerance | Voltage | Description |
|---|---|---|---|---|
| R8, R27 | 100R | 1% | – | Resistor |
| R9 | 10R | 1% | - | Resistor |
| R12, R13, R16, R40, R41 | R001 | 1% | – | Resistor |
| R14, R28, R34, R36, R37, R39, R42, R43, R44 | 2k7 | 1% | – | Resistor |
| R15 | 0R | 1% | – | Resistor |
| R45 | R003 | 1% | – | Resistor |
| R46, R47 | 620k | 1% | - | Resistor |
| T1 | MG500003079 | – | – | PWR Transformer |
| TR1 | MG600003070 | – | – | Current Sense Transformer |
| X1, X4, X5 | Faston Connector TE1217421-1 | – | – | Connector |
| X3 | SQW-106-01-L-D-ND | – | – | Female Header, 10 Contacts 2mm |
| X6 | 200-SQW11301LD | – | – | Female Header, 26 Contacts 2mm |

**Table 6 BOM for the ARCP TP PFC HF power card PW100001622**

| Designator | Value | Tolerance | Voltage | Description |
|---|---|---|---|---|
| C1 | 22uF | X7R | 10 V | Capacitor Ceramic |
| C2, C3 | 22nF | C0G | 25 V | Capacitor Ceramic |
| C4, C5, C6, C7, C9, C15, C19, C33, C40, C42 | 1uF | X7R | 50 V | Capacitor Ceramic |
| C8, C27, C29, C31 | 100nF | X7R | 50 V | Capacitor Ceramic |
| C12, C16, C17, C18 | 470nF | X7R | 500 V | Capacitor Ceramic |
| C21, C23, C41 | 100pF | C0G | 50 V | Capacitor Ceramic |
| C26, C28, C30, C32 | 220nF | X7R | 50 V | Capacitor Ceramic |
| C34, C35, C36, C37, C38, C39 | 3300pF | X7R | 50 V | Capacitor Ceramic |
| **D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D17, D19, D21, D23** | **BAT165** | **–** | **40 V** | **Schottky-Diode** |
| D15, D16 | ES1JAL_M3G | – | 600 V | Standard Diode |
| D18, D20, D22, D24 | BZX384-C10 | 5% | 10 V | Zenner Diode |
| IC1 | LM51571QRTERQ1 | - | - | Integrated Circuit |
| L1, L2, L3, L4 | SRF2012-361YA | – | – | Common Mode Choke |
| L5 | 744918220 | – | – | Aircore Inductor |
| L6 | SRF3225TAC-510Y | – | - | Common Mode Choke |
| **Q1, Q2, Q3, Q4** | **IGT65R035D2** | **-** | **650 V** | **GaN HEMT Transistor** |

| Designator | Value | Tolerance | Voltage | Description |
|---|---|---|---|---|
| **Q5, Q6** | **IGLD65R055D2** | **-** | **650 V** | **GaN HEMT Transistor** |
| R1 | 2.7k | 1% | – | Resistor |
| R2 | 820R | 1% | – | Resistor |
| R3, R35 | 100k | 1% | – | Resistor |
| R7, R10, R24, R27 | 22R | 1% | – | Resistor |
| R8, R11, R25, R28 | 1R | 1% | - | Resistor |
| R18 | 10R | 1% | - | Resistor |
| R12, R13, R15, R16 | 2R2 | 1% | – | Resistor |
| R9, R14 | 68R | 1% | – | Resistor |
| R17 | 10K NTC | – | – | Resistor |
| R20, R21, R26, R29 | 1k2 | 1% | - | Resistor |
| R22, R23 | 180R | 1% | - | Resistor |
| R30, R31, R32, R33 | 3R9 | 1% | - | Resistor |
| **U1, U2** | **2EDB8259Y** | **-** | **-** | **Gate Driver IC** |

**Table 7 BOM for the LLC power card PW200003075**

| Designator | Value | Tolerance | Voltage | Description |
|---|---|---|---|---|
| C2, C26 | 150uF | 20% | 16 V | Capacitor Polarized |
| C3, C7, C8, C9, C17, C18, C30 | 1uF | X7R | 35 V | Capacitor Ceramic |
| C4, C6, C10, C11 | 2n2 | X7R | 50 V | Capacitor Ceramic |
| C5, C19, C20, C23, C28 | 100pF | X7R | 50 V | Capacitor Ceramic |
| C12, C14, C15, C35, C36 | 100nF | X7R | 630 V | Capacitor Ceramic |
| C13 | 10uF | X7R | 25 V | Capacitor Ceramic |
| C16, C21, C31, C32 | 10uF | X7R | 50 V | Capacitor Ceramic |
| C24 | 100nF | X7R | 25 V | Capacitor Ceramic |
| C27 | 1nF | X7R | 50 V | Capacitor Ceramic |
| C29 | 33uF | 10% | 20 V | Capacitor Polarized |
| C34 | 330pF | X7R | 50 V | Capacitor Ceramic |
| **D1, D9, D10** | **BAT165** | **–** | **40 V** | **Schottky-Diode** |
| D2, D7, D8 | DFLS1200 | – | 200 V | Diode |
| D5 | FES1JE | – | 600 V | Diode |
| **IC1, IC4** | **1EDB8275F** | – | – | **Gate Driver IC** |
| **IC2** | **1EDN8550B** | – | – | **Gate Driver IC** |
| **IC5, IC9** | **1EDN8511B** | – | – | **Gate Driver IC** |
| IC6 | TLV431B | 0.5% | 1.24 V | TLV431B- Adjustable Precision Shunt Regulator 0.5% |
| **IC7** | **ICE2QR2280G** | – | – | **Integrated Circuit** |

## Bill of materials

| Designator | Value | Tolerance | Voltage | Description |
|---|---|---|---|---|
| IC8 | VOL617A-3 | – | – | Integrated Circuit |
| L1, L2, L3, L4 | SRF2012-361YA | – | – | Common Mode Power Line Choke |
| **Q1, Q2, Q3, Q4** | **IGT60R042D2** | – | – | **GaN HEMT Transistor** |
| **Q5, Q6, Q7, Q8** | **IPT60R016CM8** | – | **600 V** | **MOSFET** |
| **Q9, Q10** | **BSS138N** | – | **60 V** | **MOSFET** |
| R2, R5, R9, R14, R15, R16, R19, R20, R23, R24, R26, R29, R47 | 10R | 1% | – | Resistor |
| R3, R4, R27, R28 | 2R7 | 1% | – | Resistor |
| R6, R7, R46, R48 | 1k | 1% | – | Resistor |
| R8 | 150R | 1% | – | Resistor |
| R10, R13, R45 | 33k | 1% | – | Resistor |
| R11, R17, R18, R21, R22, R25, R36 | 510R | 1% | – | Resistor |
| R12 | 10K NTC | 3% | – | Resistor |
| R30, R31, R32, R33 | 270R | 1% | – | Resistor |
| R34, R35, R40 | 15k | 1% | – | Resistor |
| R37, R39 | 825R | 1% | – | Resistor |
| R38 | 3k6 | 1% | – | Resistor |
| R41 | 1k18 | 0.1% | – | Resistor |
| R42 | 1R5 | 1% | – | Resistor |
| R43 | 2K7 | 1% | – | Resistor |
| R44 | 10k | 1% | | Resistor |
| REL1 | G2RL-1A-E2-CV-HA - DC12 | – | 12 V | Relay |
| TF1 | ICE 8032.0205.024 | – | – | Transformer |
| TR1, TR3 | XT01 | – | – | Common Mode Power Line Choke |

**Table 8 BOM for the control card CD100001621**

| Designator | Value | Tolerance | Voltage | Description |
|---|---|---|---|---|
| C1, C2, C8, C18, C24, C26, C28, C31, C33, C35, C36, C42, C49, C50, C54, C59, C65, C66, C67, C68, C74, C75 | 100nF | X7R | 25 V | Capacitor Ceramic |
| C3, C4, C40, C41 | 10pF | X7R | 50 V | Capacitor Ceramic |
| C5 | 10uF | X5R | 25 V | Capacitor Ceramic |
| C6, C9, C16, C37 | 4.7uF | X7R | 50 V | Capacitor Ceramic |
| C7, C70, C72 | 100pF | X7R | 50 V | Capacitor Ceramic |

## EVAL_3K3W_ARCP_PSU

### Bill of materials

| Designator | Value | Tolerance | Voltage | Description |
|---|---|---|---|---|
| C14, C15, C17, C19, C45, C47, C57, C58, C61, C63, C64, C71 | 330pF | X7R | 50 V | Capacitor Ceramic |
| C10, C23, C25, C27, C30, C32, C34, C48, C55, C56, C69 | 10uF | X5R | 6.3 V | Capacitor Ceramic |
| C43, C52 | 47pF | X7R | 50 V | Capacitor Ceramic |
| C60, C62 | 4n7 | X7R | 50 V | Capacitor Ceramic |
| C76 | 100uF | X5R | 10 V | Capacitor Ceramic |
| D3, D7, D8, D9, D10, D12 | BAT165 | – | 40 V | Schottky-Diode |
| D5, D6, D11 | GREEN LED | – | – | LED |
| **IC1** | **4DIR1400H** | – | – | **Integrated Circuit** |
| **IC2** | **TLS4120D0EPV33** | – | – | **Synchronous Step-Down Regulator** |
| **IC3** | **TLV1391IDBVR** | – | – | **Single Differential Comparators.** |
| **IC4, IC10** | **TLV2376IDR** | – | – | **Integrated Circuit** |
| IC8 | dsPIC33CK256MP203-I/M5 | – | – | MCU |
| IC11, IC12 | LMH6642MF | – | – | Integrated Circuit |
| **IC13** | **TLS820F3ELV33XUM** | – | – | **Low Dropout Linear Voltage Regulator** |
| **IC14** | **XMC4200-Q48K256** | – | – | **Integrated Circuit** |
| L1 | 100uH | – | – | Magnetic |
| L2, L3 | Ferrite bead 60Ohm@100MHz | – | – | Magnetic |
| NTC1 | 10K | 1% | – | NTC Resistor |
| R1, R6, R12, R41, R44, R71, R72, R76, R77 | 510R | 1% | – | Resistor |
| R2, R3, R4, R5, R34, R39, R43, R60, R69 | 15k | 1% | – | Resistor |
| R7, R16, R23, R24, R26, R28, R32 | 309k | 0.1% | – | Resistor |
| R8, R9, R13, R15, R25, R33, R47, R53 | 10k | 0.1% | – | Resistor |
| R10, R30, R37, R42, R62 | 2k7 | 1% | – | Resistor |
| R14, R18, R19, R20, R45, R70 | 100R | 1% | – | Resistor |
| R21, R22, R27, R29 | 17k8 | 0.1% | – | Resistor |
| R11, R31 | 1k | 1% | – | Resistor |
| R48, R56, R57, R63, R65 | 4k99 | 0.1% | – | Resistor |
| R49, R52 | 124R | 0.1% | – | Resistor |
| R50, R54, R58 | 49k9 | 0.1% | – | Resistor |

## EVAL_3K3W_ARCP_PSU

## Bill of materials

| Designator | Value | Tolerance | Voltage | Description |
|---|---|---|---|---|
| R51, R55, R59 | 54k9 | 0.1% | – | Resistor |
| R66, R68, R73, R74 | 261R | 1% | – | Resistor |
| R75 | 1R4 | 1% | – | Resistor |
| X1, X5 | FTSH-105-01-L-DV-K | – | – | Connector |
| X2 | TMM-113-03-L-D | – | – | Pin Header, 26 Contacts |
| X3 | Fan connector | – | – | Pin Header, 4 Contacts |
| X4 | TMM-106-03-L-D | – | – | Pin Header, 26 Contacts |
| X6 | B2B-ZR | – | – | Connector |
| XTAL1 | QT325S-12.000MEEQ-T | – | – | Crystal Oscillator |

**Table 9 BOM for the secondary-side transformer PCB MG100001429**

| Designator | Value | Tolerance | Voltage | Description |
|---|---|---|---|---|
| C2, C3, C4, C5, C6, C7, C8, C9, C10 | 4.7uF | X8L | 100 V | Capacitor Ceramic |
| C13, C14, C15, C16, C17, C18 | 1uF | X7R | 35 V | Capacitor Ceramic |
| **D1, D2** | **BAT46WJ** | – | **100 V** | **Schottky Diode** |
| **IC1, IC2** | **2EDB7259K** | – | – | **Gate driver IC** |
| R1, R2 | 2R2 | 1% | – | Resistor |
| R3, R4, R5, R6, R7, R8, R9, R10 | 1R | 1% | – | Resistor |
| R11, R12 | 2k | 1% | – | Resistor |
| T1, T2, T3, T4, T5, T6, T7, T8 | IQE031N08LM6CG | – | 80 V | MOSFET |

**Table 10 BOM for the split capacitor PCB EL100001621**

| Designator | Value | Tolerance | Voltage | Description |
|---|---|---|---|---|
| C1, C2 | 56uF | 20% | 350 V | Electrolyt |

# 7 Schematics

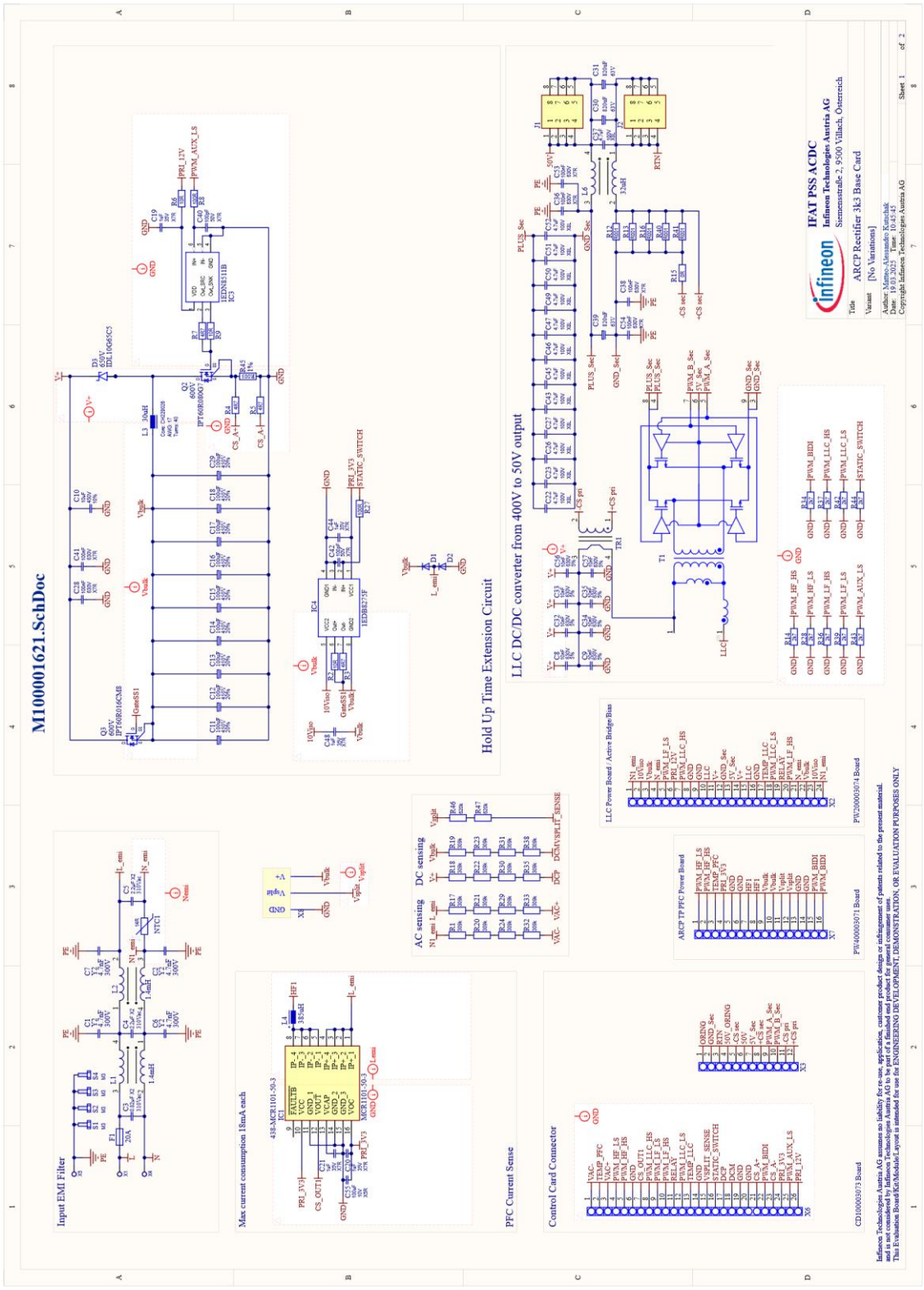



**Figure 58 Schematic diagram of the main board (M100001621)**

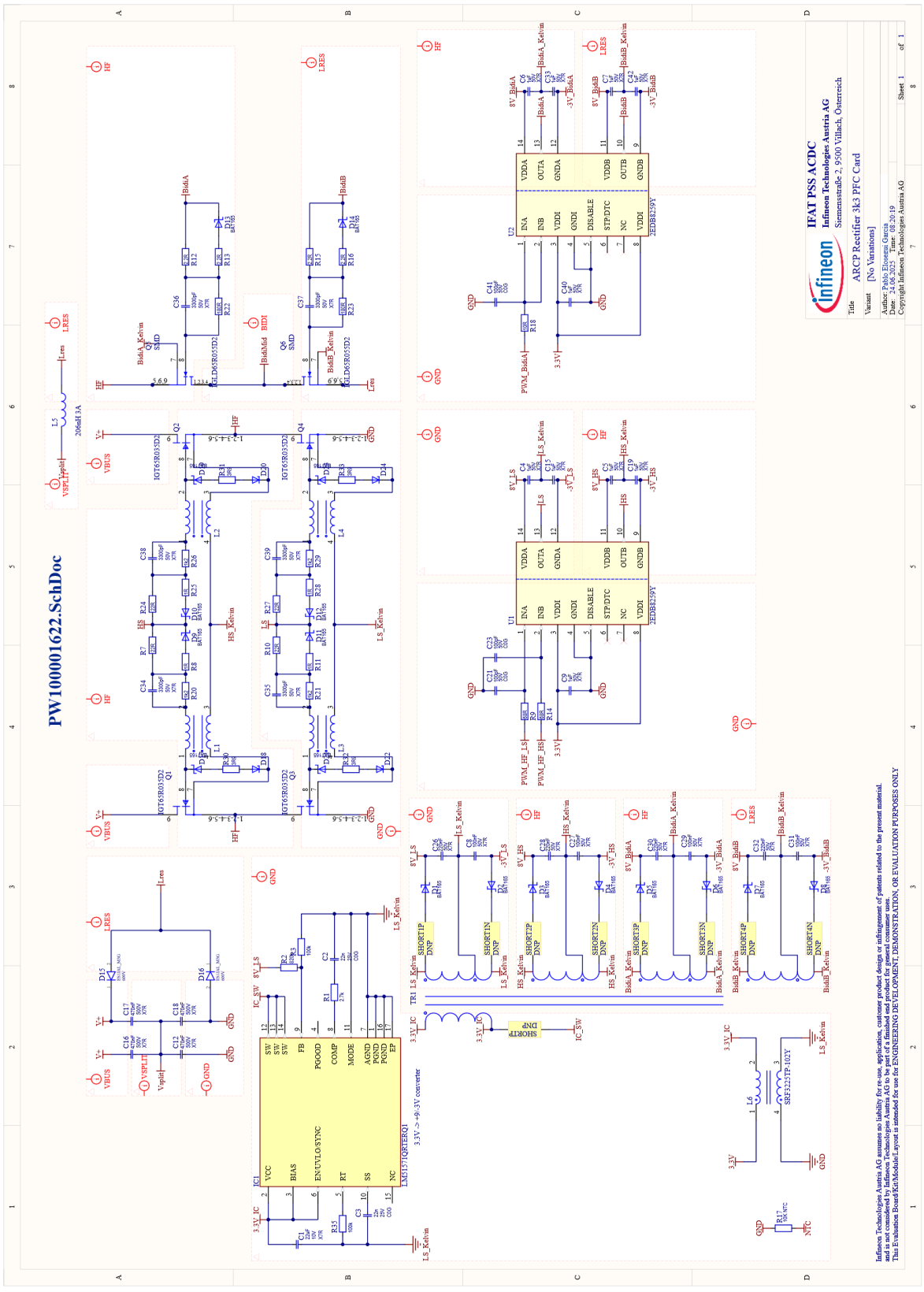



**Figure 59 Schematic diagram of the ARCP TP-PFC high-frequency board (PW100001622)**

## Schematics

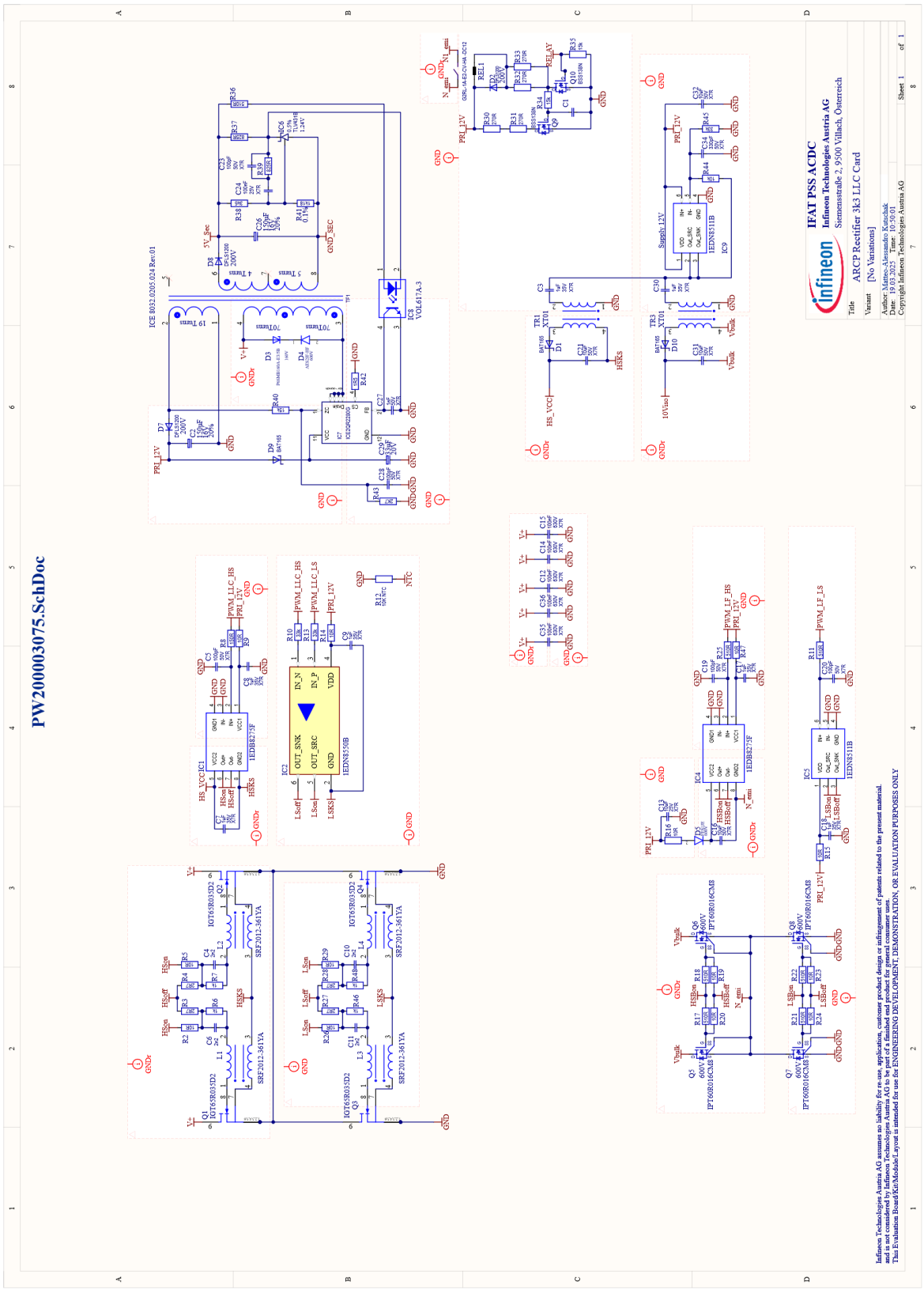



**Figure 60 Schematic diagram of the LLC and PFC SR power card (PW200003075)**

## Schematics

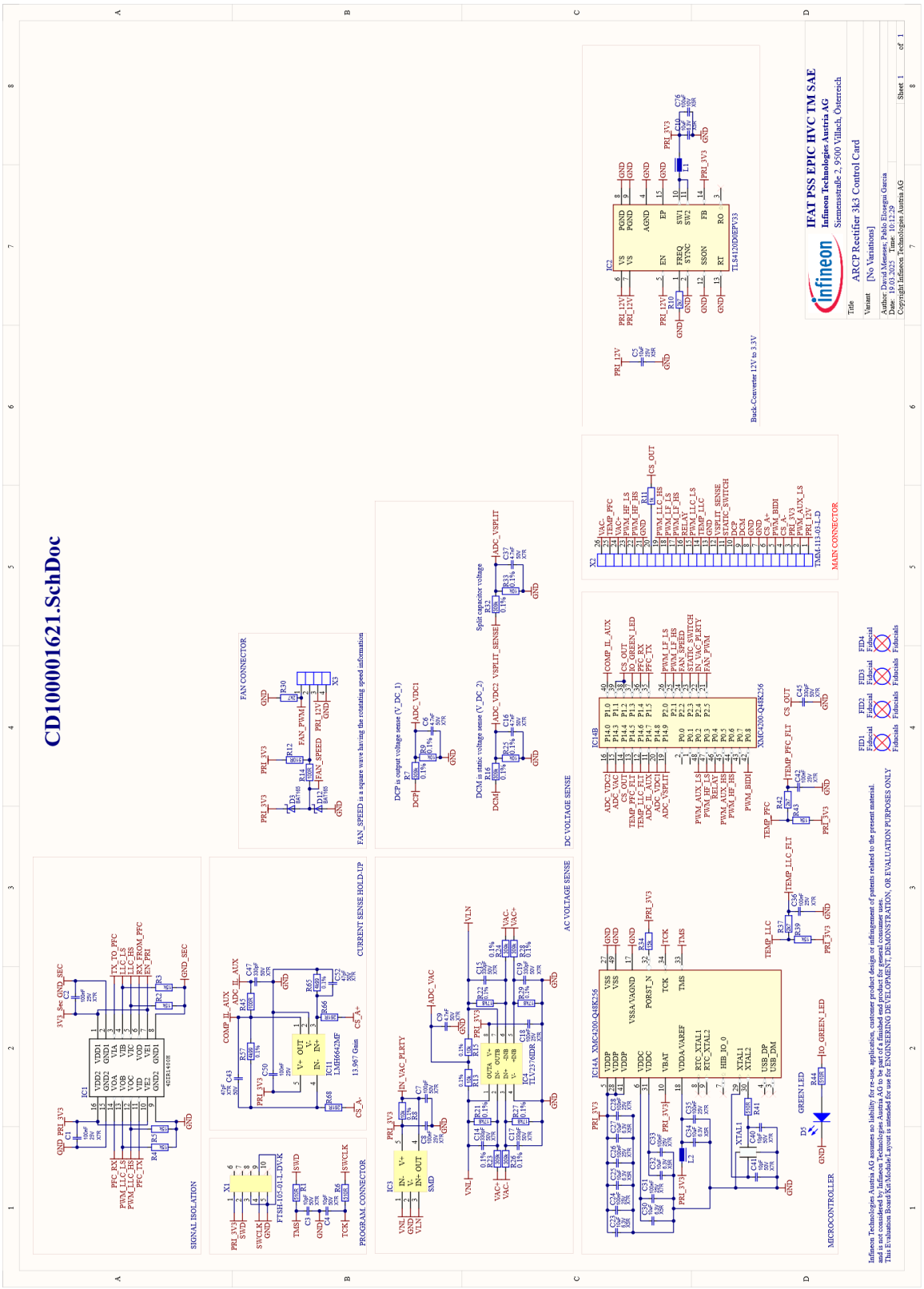



**Figure 61 Schematic diagram of the control PCBA (CD100001621) – part 1: PFC control**

## Schematics

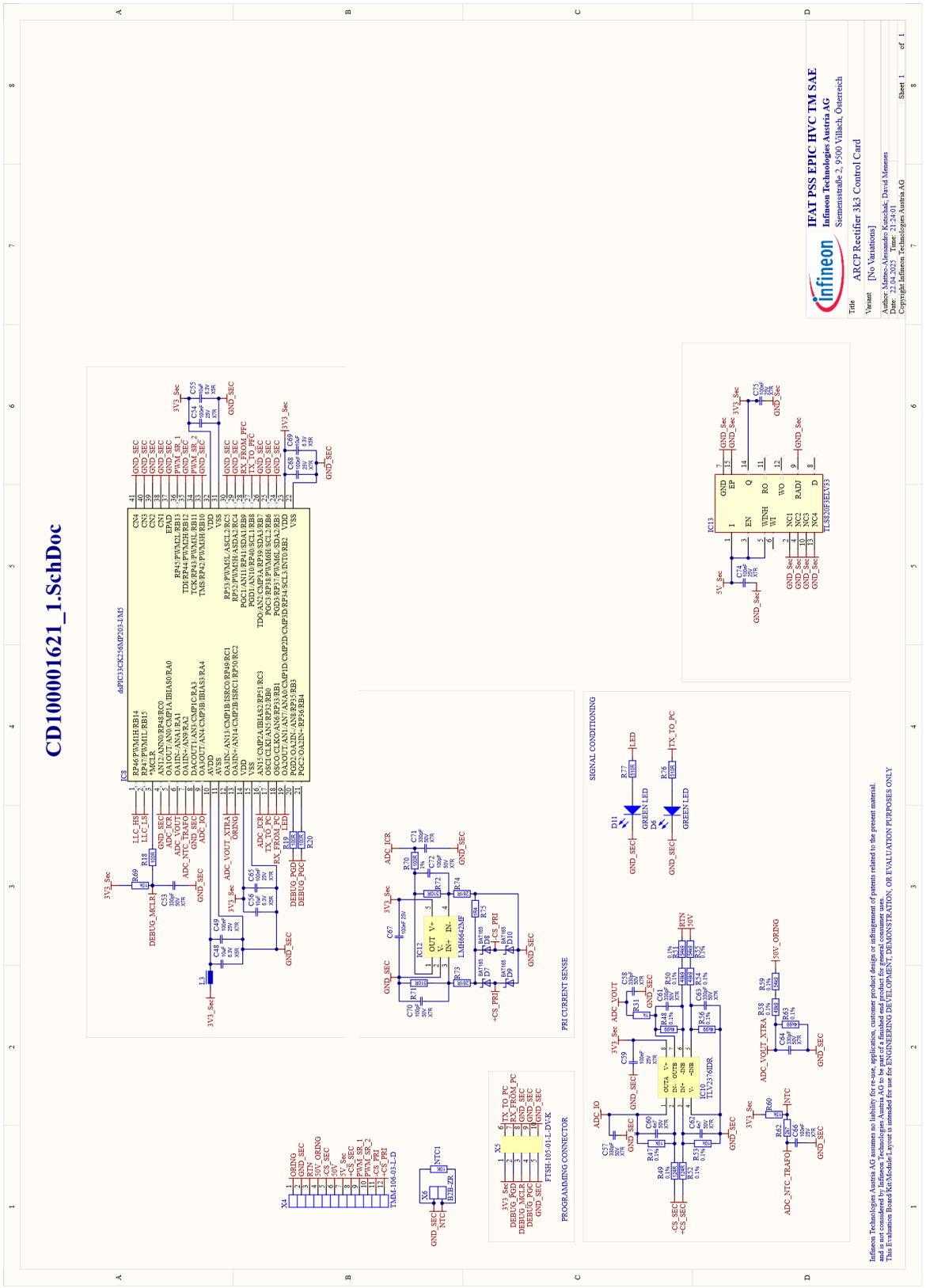



**Figure 62 Schematic diagram of the control PCBA (CD100001621) – part 2: LLC control**

## Schematics

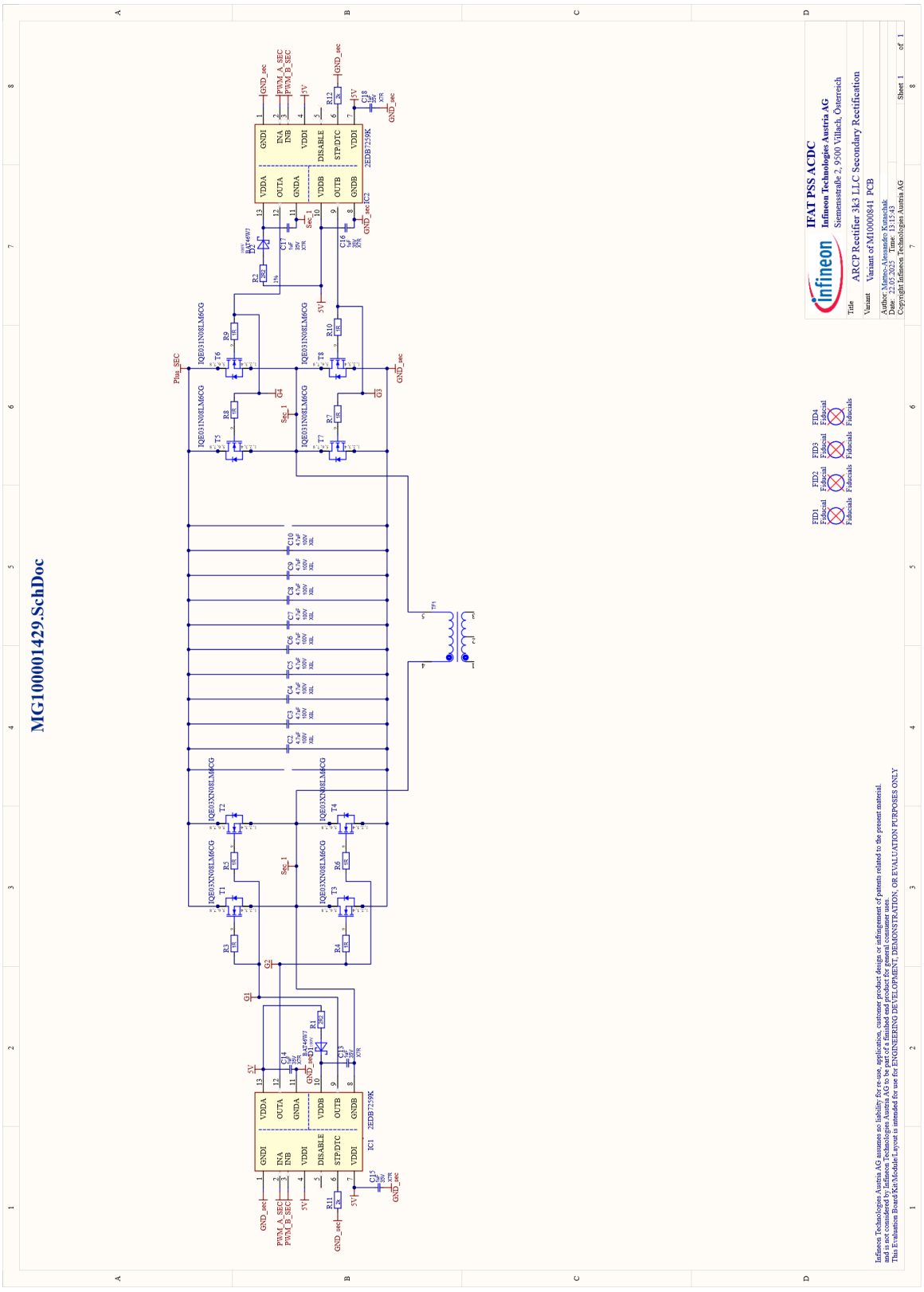



**Figure 63 Schematic diagram of the secondary PCBs (MG100001429)**

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## Acronyms/abbreviations

**Table 11 Acronyms/abbreviations**

| Acronym | Description |
|---|---|
| ARCP | Auxiliary resonant commutated pole |
| ACLDO | AC line-cycle dropout |
| BW | Bandwidth |
| BTM | Bottom |
| CCM | Continuous conduction mode |
| DFF | Duty-cycle feed-forward |
| FB | Full-bridge |
| GaN | Gallium nitride |
| HB | Half-bridge |
| HV | High voltage |
| iTHD | Input current total harmonic distortion |
| LCDO | Line cycle dropout |
| LDO | Low dropout voltage regulator |
| LLC | Series parallel resonant converter |
| OCP | Overcurrent protection |
| OVP | Overvoltage protection |
| PF | Power factor |
| PFC | Power factor correction |
| PSU | Power supply unit |
| PWM | Pulse width modulation |
| Si | Silicon |
| SMPS | Switched mode power supply |
| SR | Synchronous rectification |
| THD | Total harmonic distortion |
| UVLO | Undervoltage lockout |
| UVP | Undervoltage protection |
| WBG | Wide-bandgap |

## Revision history

| Document revision | Date | Description of changes |
|---|---|---|
| V 1.0 | 2025-09-24 | Initial release |

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