

SMM System Mode Management

AURIX™ TC4xx Microcontroller V1.0.0 2024-09

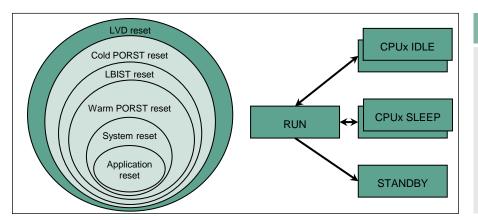


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SMM

System Mode Management





Highlights

- Different power modes provide the possibility to save power consumption
- Resets are managed by SMM to make the intended modules and RAMs to switch back to reset state

Key Features

System modes: SMM supports the transaction among various system modes like reset state, RUN0/1 Mode and IDLE/SLEEP/STANDBY mode

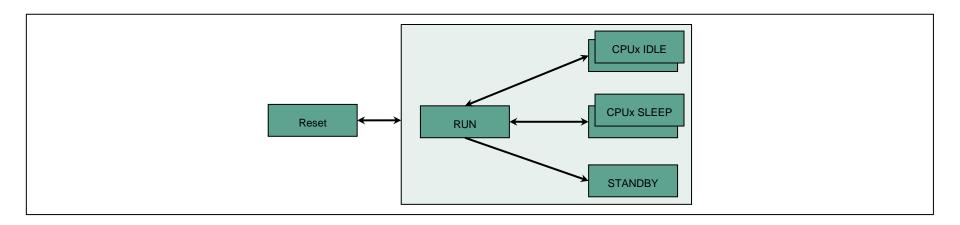
Reset types: SMM manages various reset types like Cold or Warm Power-On Reset, Application Reset, System Reset, Module (Group) Reset etc.

Customer Benefits

- Various power modes supports flexible consumption use cases
- User may choose the most proper reset type to reset necessary modules and also to achieve the optimum reset time

SMM System Modes





Supported system modes:

- RUN mode: at least one CPU is not in IDLE or SLEEP mode. CPU clock is active, and code is being executed
- IDLE mode: The CPU code execution is halted, and CPU clock is disabled in Idle state. The peripherals continue to remain active.
 CPU RAM memories are accessible to other bus masters and peripherals
- SLEEP mode: CPU code execution is halted, and CPU Idle state is entered. Peripherals are set into sleep state if so, configured in the
 respective CLCx.EDIS bit. Ports retain their earlier programmed state
- STANDBY mode: The Standby domain constituting the Standby RAM, the 8-bit standby controller, standby ports including pin wakeup logic remain actively supplied. The power to the rest of the chip is completely switched off. VDD supply rail is switched off

SMM Reset Types



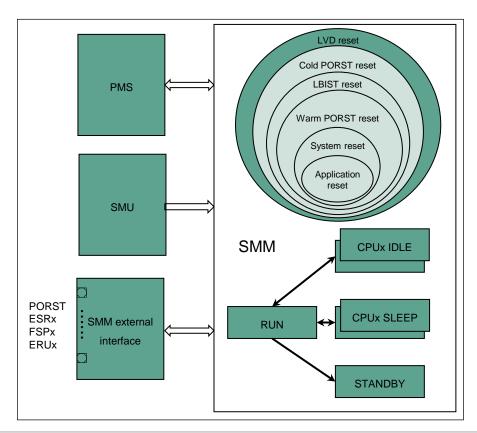
LVD reset	Effect of Reset on Device Functions						
Cold PORST reset LBIST reset Warm PORST reset System reset Application		Low Voltage Detector Resets	Cold Power-on Reset	LBIST	Warm Power-on Reset	System Reset	Application Reset
	PMS0, PMS1	Х	Not affected	Not affected	Not affected	Not affected	Not affected
	SCR	Х	configurable	Not affected	configurable	Not affected	Not affected
	PMS2, EVRC, Standby SMU	Х		Not affected	Not affected	Not affected	Not affected
	PORST pin	driven low		Not affected.	Not affected. Reset trigger	Not affected	Not affected

- Lower reset class is automatically done, when a higher reset class is triggered. For example, when user triggers a system reset, then application reset is automatically included too
- > It is important to know which domains are reset, and which domains are not affected, by which reset class. Please refer to user manual table "Effect of Reset on Device Functions"
- Reset sources could be: under or over voltage events, ESRx pin assertion, PORST pin assertion, SMU (Safety and security alarm Management Unit) Alarm, software trigger, debugger trigger etc

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System integration

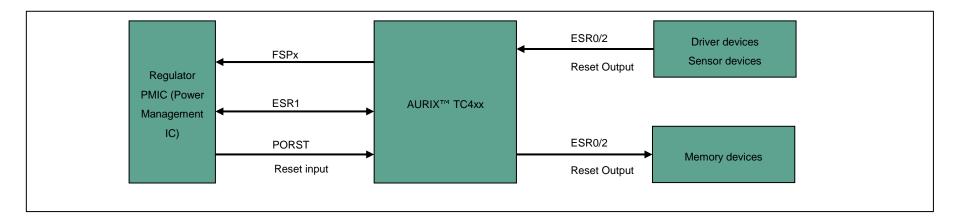




- SMM manages power modes and reset, which affect the microcontroller overall
 - It has especially close interaction with PMS (Power Management System)
 - It receives reset triggers from PMS (voltage event), SMU and other reset sources etc.
 - It provides reset information for user evaluation e.g. which triggers have triggered reset, which is the highest-class trigger of the previous reset
 - In many applications SMM also interacts with user external reset controls e.g. through ESRx pins. ERUx (External Request Unit) can also be used to trigger reset
 - FSPx (Fault Signaling Protocol) pins can be reset output indication too

Application example Reset Control





Overview

- In real applications, both AURIX™ and external user components, must be reset in a controlled manner
- The timing e.g. when a device should release its reset can be implemented with the support of SMM

Advantages

- > AURIX™ is able to react on reset input, typically from power supply IC, external watchdog or any other peripheral. Reset type is configurable for user
- As main microcontroller, AURIX™ is responsible for external component reset timing (reset output). For example, some components need longer reset time, this can be achieved by using the ESRx configurable delay feature

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