SDMMC
Secure Digital Multi-Media Card

AURIX™ TC4xx Microcontroller

V1.0.0 2024-09

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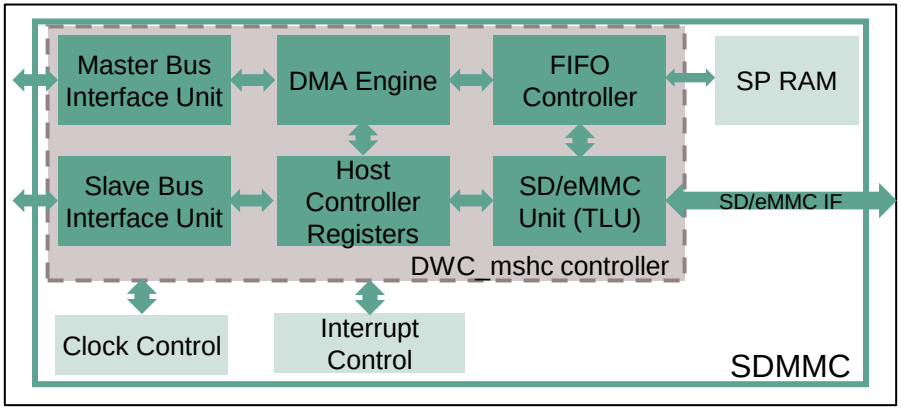
SDMMC
SD- and eMMC interface



Highlights

- The SD- and eMMC Interface (SDMMC) is used to enable communication with a single embedded (eMMC) memory device or a single SD- card
- Bandwidth up to 400 Mbits/sec for eMMC devices and up to 200 Mbits/sec for SD cards

Key Features

DMA engine
Integrated buffer memory
Interrupt support

Customer Benefits

Data transfers without CPU overload
2 x 512 bytes buffer for data transfers between core and cards
Status and error signaling

SDMMC
DMA engine

- The Mobile Storage Host Controller (DWC_mshc) contains a DMA engine for data transfer to and from the system memory
- Multiple modes are supported for different data transfer sizes:
  - Single operation DMA (SDMA) – short data transfer: only a single SD command transaction can be executed for each SDMA operation
  - Advanced DMA-2 (ADMA2) – lengthy data transfers: high data transfer speed is obtained by using the scatter gather DMA algorithm
- It supports single and burst transfers

SDMMC
Integrated buffer memory

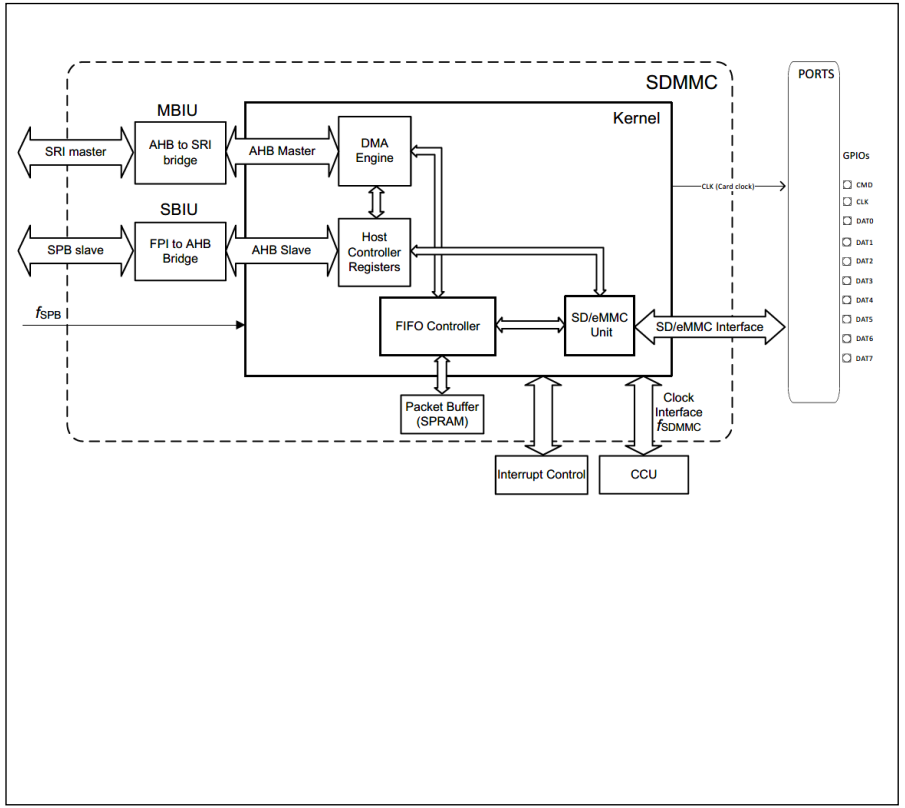
- The internal buffer in the SDMMC is configured as a double buffer (2 x 512 Bytes)
- Cards with the size less or equal to 256 GB are supported:
  - For card sizes less or equal to 2 GB, the memory addressing is using a byte addressing (32-bit field).
  - For card sizes bigger than 2 GB, the memory addressing is using sector access mode (512 B sector)
- It can also handle FIFO over and under run conditions

SDMMC
Interrupt Support

- The SDMMC has two types of service requests routed to the interrupt router:
  - Status interrupts (e.g. DMA transfer completed)
  - Error interrupts (e.g. timeouts)
- Errors in either command or data portion of the transaction can be detected by setting the Error Interrupt flag, for examples:
  - Data errors: Data Timeout Error, Data CRC Error, ADMA Error
  - Command errors: Timeout for CMD_RES, Framing Error, Header Error
- The DWC_mshc supports the Error Interrupt Status register, which captures the interrupt status

SDMMC
System integration

- The SDMMC connects to the SPB and to the SRI bus
- Access to host control registers takes place through slave interface (SPB).
- Data transfers from or to external NAND memory to or from internal system memory space takes place through an internal Direct Memory Access(DMA) engine through the master interface (SRI).
- The card clock domain runs at the peripheral frequency of fSDMMC.
- The Host controller accesses the external memory device over the GPIO pads belonging to the PORTS functional block.
  - SD mode uses 4 IOs
  - eMMC mode uses 8 IOs

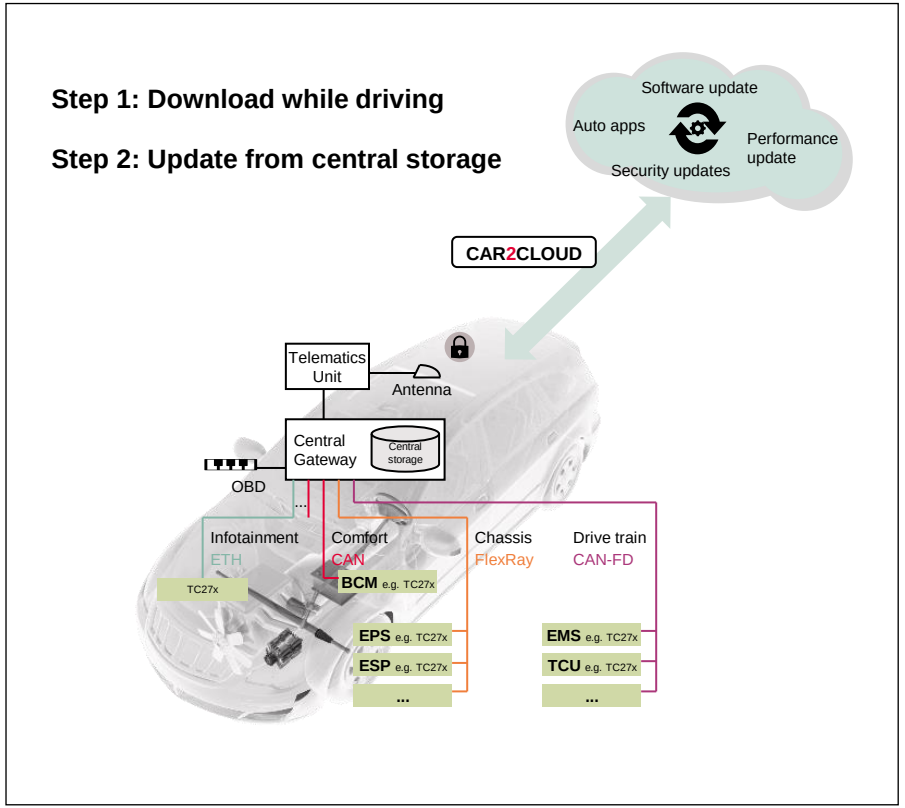


SDMMC
System Features

- The SDMMC module conforms to the following standards:
  - JEDEC eMMC 5.1 Specification - JESD84-B51, Feb 2015
  - SD Specifications Part A2 SD Host Controller Standard Specification Version 4.20, August 2015
  - SD Specifications Part 1 Physical Layer Specification Version 5.00, dated February 22, 2016
  - SD Specifications Part E1 SDIO Specification Version 4.10 Sept 2014
- With the following restrictions:
  - Maximum clock frequency (fSDMMC): 50 MHz
  - Capacity of memory up to 32GB
  - Bus speed modes
    - Default Speed mode / Legacy: 3.3V signaling, frequency up to 25MHz, up to 100Mbit/s in SD mode and up to 200Mbit/s in eMMC mode
    - High Speed mode / High Speed SDR: 3.3V signaling, frequency up to 50MHz, up to 200Mbit/s in SD mode and up to 400Mbit/s in eMMC mode

Application example
Software update Over The Air (SOTA)

- SDMMC module has many use cases like In-Vehicle infotainment, GPS and telematics, data recorder or Software update Over The Air (SOTA)
- AURIX™ TC4xx devices have the ability to receive Software updates Over The Air (SOTA)
- The flash memory is divided in banks and when SOTA is enabled, one of these bank groups can be used to read and execute from, while another group can have new code written to it



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Email: erratum@infineon.com

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