PSI5-S
Peripheral Sensor Interface with Serial Interface to PHY

AURIX™ TC4xx Microcontroller

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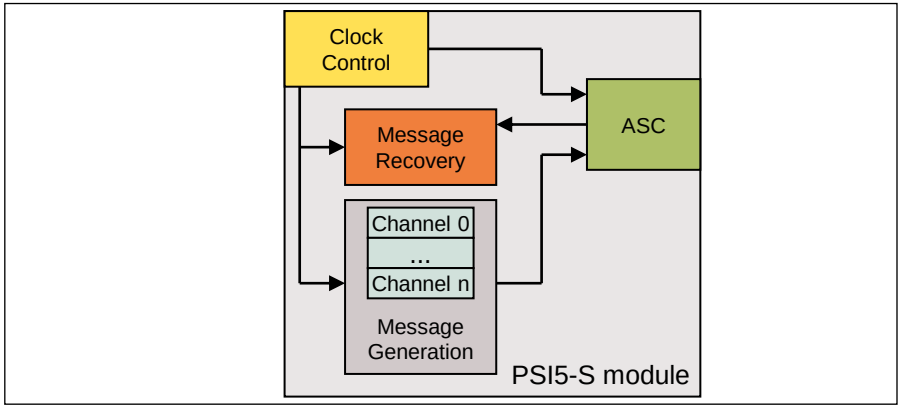
Peripheral sensor interface with serial interface to PHY



Highlights

- The Peripheral Sensor Interface is an interface for automotive sensor applications
- PSI5-S module supports PSI5 protocol specification V2.1 powertrain substandard
- Data rates of 125 kbit/s and 189 kbit/s are supported

Key Features

- 8 PSI5-S channels sharing one common ASC module
- Message recovery and generation blocks
- Error detection and handling

Customer Benefits

- Simplifies and reduces cost of integration due to reduced number of required pins
- Simplifies implementation while the message recovery is done in HW
- Reduces software overhead while the errors will be detected by the module itself

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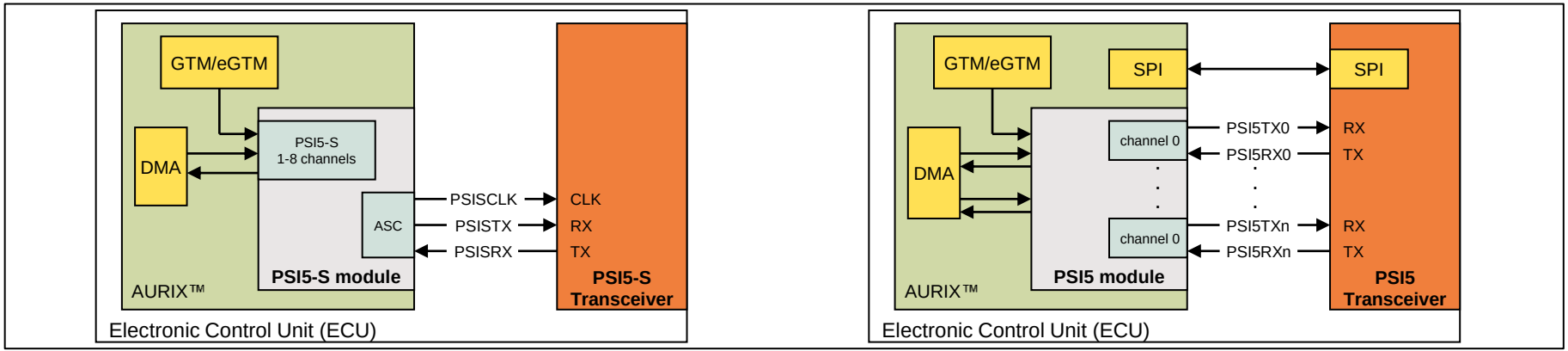
PSI5-S
8 PSI5-S channels sharing one common ASC module



- Each channel supports 6 sensor slots (allows greater bus topology flexibility)
- In comparison with PSI5 module, reduction of required pins:
  - 2 pins (TX/RX) + 1 CLK pin for up to all 1-8 channels (**PSI5-S** module)
  - 2 pins (TX/RX) per channel and optionally 4 SPI pins (PHY configuration) (**PSI5** module)
- One common ASC module consists of 3 pins (PSISTX, PSISRX, and PSISCLK)
- PSISTX and PSISRX pins act as a transmit data output and receive data input signals respectively
- PSISCLK pin provides the clock to drive the external PHY

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PSI5-S
Message recovery and generation blocks

- Message recovery block
  - ASC format 10 Bit: 1 Start Bit, 8 Data bits, 1 Stop Bit (Up Stream)
  - Each PSI5 Frame is transported in a Packet Frame consisting of 3 to 6 UART Frames transmitted back to back, i.e. with exactly one stop bit - no additional delay
  - Configurable data length 8 .. 28 bit + 3 bit PSI5 CRC or 1 bit PSI5 Parity
  - Packet Frames are separated by a programmable idle time (1-16 idle bits)
  - Two independent time bases for Time Stamp: clocked by GTM (1 out of n GTM signals is selectable) or internal periodic trigger generator (24-Bit time stamp with resolution of 1µs)
  - CRC check of received PSI5 sensor data, CRC code still transparent
- Message generation block
  - ASC format 11 Bit: 1 Start Bit, 8 Data bits, 1 Parity, 1 Stop Bit (Down Stream)
  - Downstream data transmission by 2 different ASC commands (support for both “Tooth Gap” or “Pulse Width” bit coding methods)
  - Start sequence generator for downstream data (can be switched off)
  - Bit stuffing generator for downstream data (can be switched off)
  - CRC generator (3 or 6 bit CRC) for downstream data (can be switched off)

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PSI5-S
Error detection and handling

- Each PSI5-S channel can detect and signal the following error conditions:
- Protocol Level:
  - Packet Frame CRC Error (XCRC)
  - PSI5 Frame Checksum error (CRCI)
  - Frame not sent in time / UART Frames missing (TEI)
  - Error Bits Set in Packet Frame (HDI)
  - Errors signaled by ASC Sub Module
    - parity error (PE)
    - framing error (FE)
    - overrun error (OE)
- Transfer Management Level:
  - Receive Data Buffer Overrun (RBI)
  - ECU to Sensor Data Buffer Underrun (TBI)

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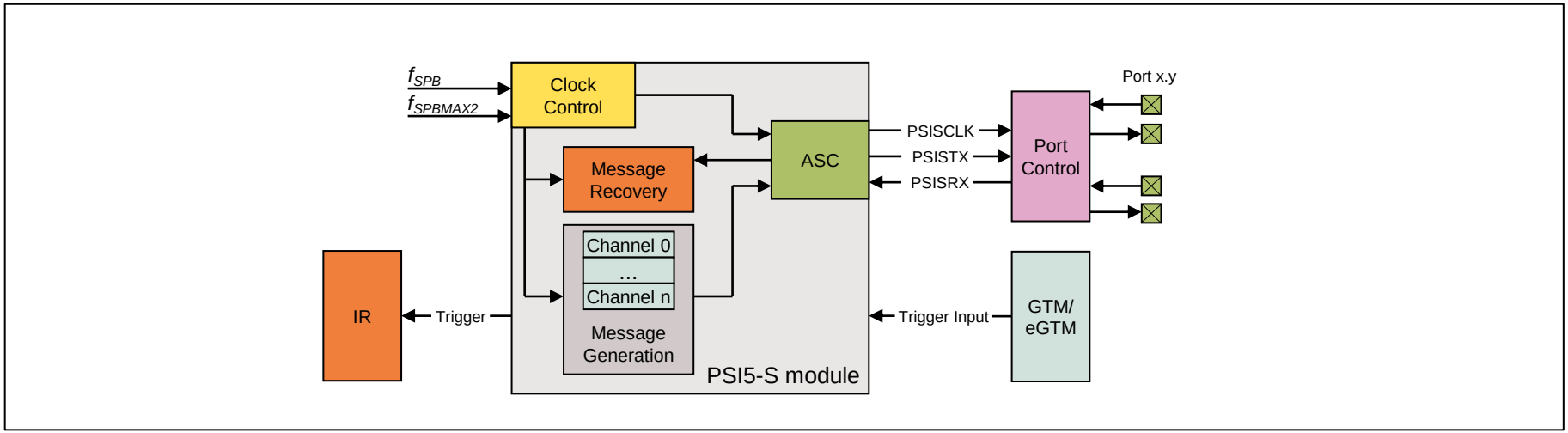
PSI5-S
System integration

PSI5-S module is connected to several external modules:

- As an input clock source for the Clock Control module, f_{SPB} or $f_{SPBMAX2}$ can be selected
- Interrupt Router: Schedules service requests coming from 8 interrupt sources available for the PSI5-S module
- Port Control: Connects the PSISTX, PSISRX, and PSISCLK pins to the external GPIO pins
- GTM/eGTM: GTM/eGTM module outputs are connected to the timer inputs to support timestamp generation



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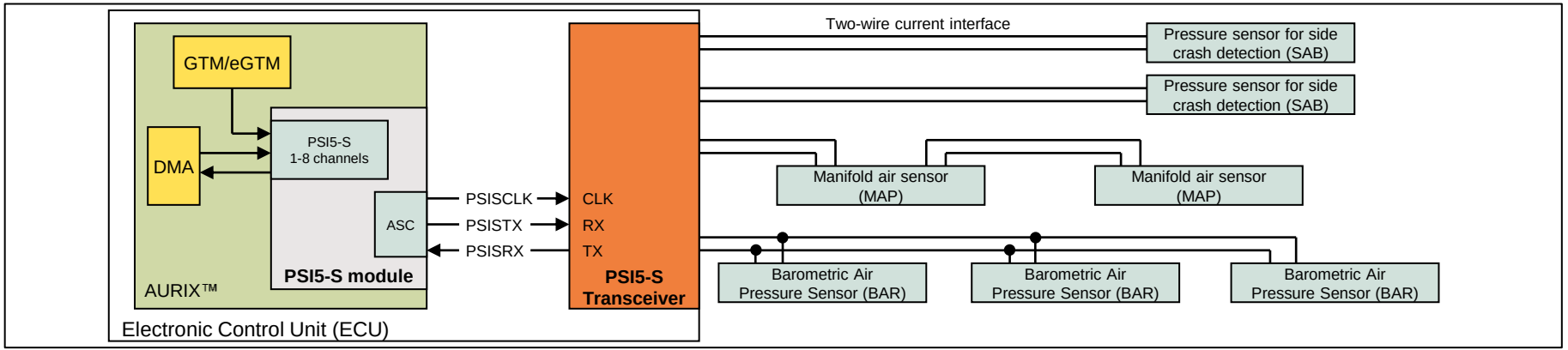
Application example
Connection of sensors to an ECU



Overview

- This application example shows typical usage of PSI5-S module in airbag or powertrain domain
- PSI5-S module is connected to the external PSI5-S transceiver module (PHY) whose role is to fulfil physical layer requirement that cannot be achieved with MCU alone

Advantages

- The sensors are connected to the ECU by just two wires, using same lines for power supply and data transmission
- This allows high reliability data transfer at lowest possible implementation overhead and cost

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