# NVM
# Non Volatile Memory

AURIX™ TC4xx Microcontroller

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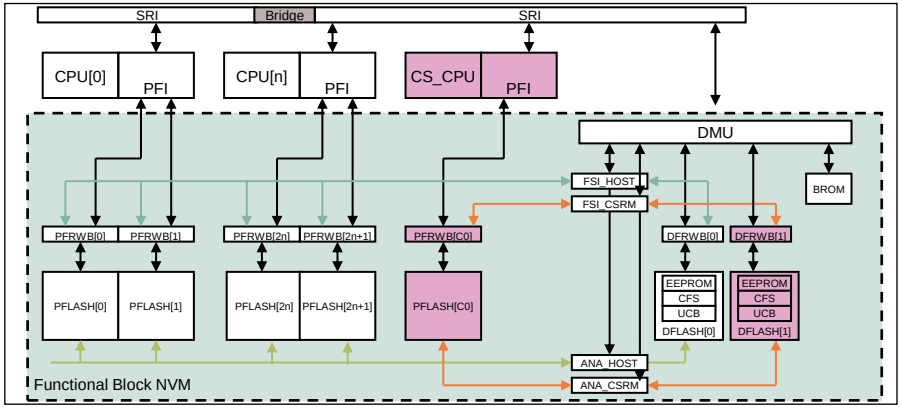
# NVM
# Non volatile memory




## Highlights

- The NVM subsystem comprises of Program and Data Flash Memory, Data Memory Unit (DMU), Program Flash Interface (PFI) and Flash Standard Interface (FSI)
- NVM enables writing to the flash memories through a command sequencer and controls the flash accesses for safety and security through protections

## Key Features

Separate Security PFlash

Two parallel PFLASH Banks per CPU

Two complete and independent command interfaces

## Customer Benefits

- Read while write
- Independent access path and no performance impact on SOTA
- Domain Separation between HOST and CSRM

# NVM
# Separate Security PFlash

- Read while write
  - reading code for security CPU is possible while HOST is doing application code updates
- Freedom of interference between HOST and CSRM SOTA updates and swaps
  - HOST program/erase operations do not interfere with CSRM program/erase operations
  - A/B Swap setting can be set independent from each other

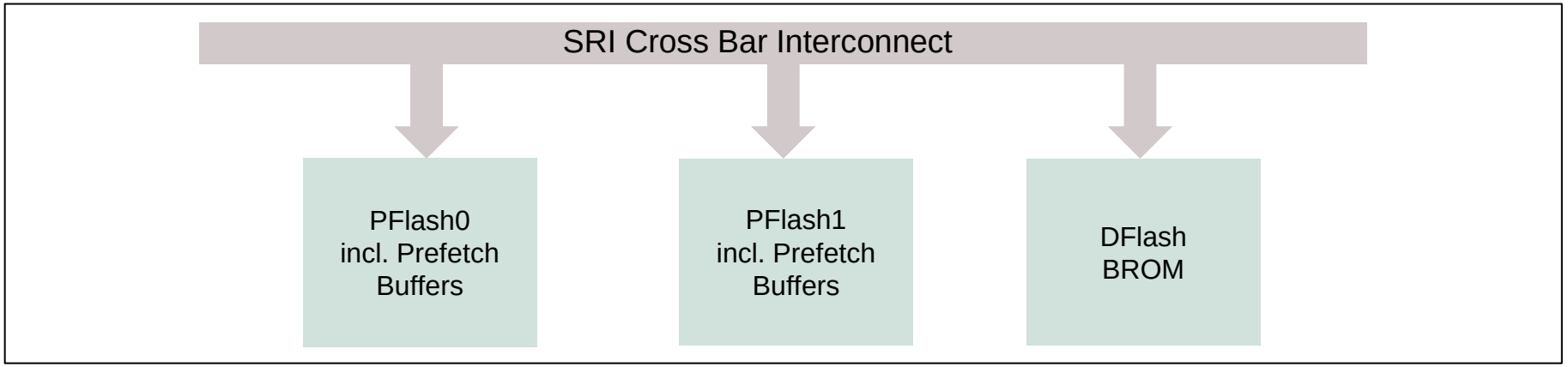
# NVM
# Two parallel PFLASH Banks per CPU

- Each PFLASH block of any Host CPU is divided in 2 banks
- Two completely independent access paths
  - read from one bank while operation is ongoing on the other bank
- When SOTA support is enabled, no more impact on program execution performance

# NVM
## Two complete and independent command interfaces

- One command interface for HOST and one for CSRM
- Each command interface has an independent digital and analog part
  - time slice for two concurrent operations is no more needed
- The allocation of NVM memory Banks to the command interfaces can be changed
  - new Bank Reallocation command

# NVM
# System integration




- All PFlash banks and DFlash/BROM can be read in parallel via dedicated SRI interface(s)
- Access control (PROT/APU) for safety and security for all assigned memories
- All PFlash banks have Prefetch Buffers implemented for improved read throughput to achieve higher system performance

# Application example
# Simplified sequence for programming

## Overview

- “Clear Status” to clear flags
- “Enter Page Mode”
- Check for Page Mode status bit or error
- Repeat “Load Page” until the page is filled
- “Write Page”
- Wait until Request Acknowledgement status bit
- Wait until Request Done status bit
- Check for Program Verification bit
- Fail if Operation/Sequence/Protection error is set

## Advantages

- Easy sequence of commands to perform all the programming steps
- Each command has a notification bit to check when the operation is completed
- Several kind of error bits to check during the sequence

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