IR
Interrupt Router

AURIX™ TC4xx Microcontroller

V1.0.0 2024-09

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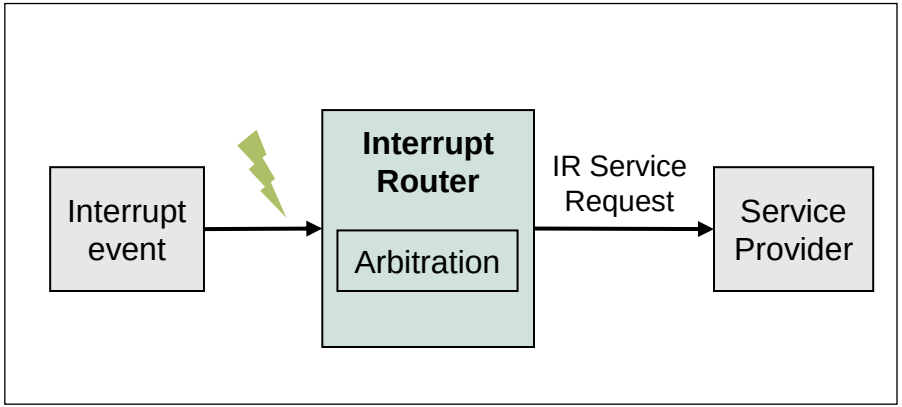
IR
Interrupt router



Highlights

- Schedules the Service Requests (SR) from external resources, internal resources and Software to Interrupt Service Providers (ISP)
- Up to 2048 Service Requests
- Up to 15 Interrupt Control Units (ICU)
- Up to 256 SR priority level per ICU
- Support for HW Virtualization mode

Key Features

Mapping Service Requests to Service Providers

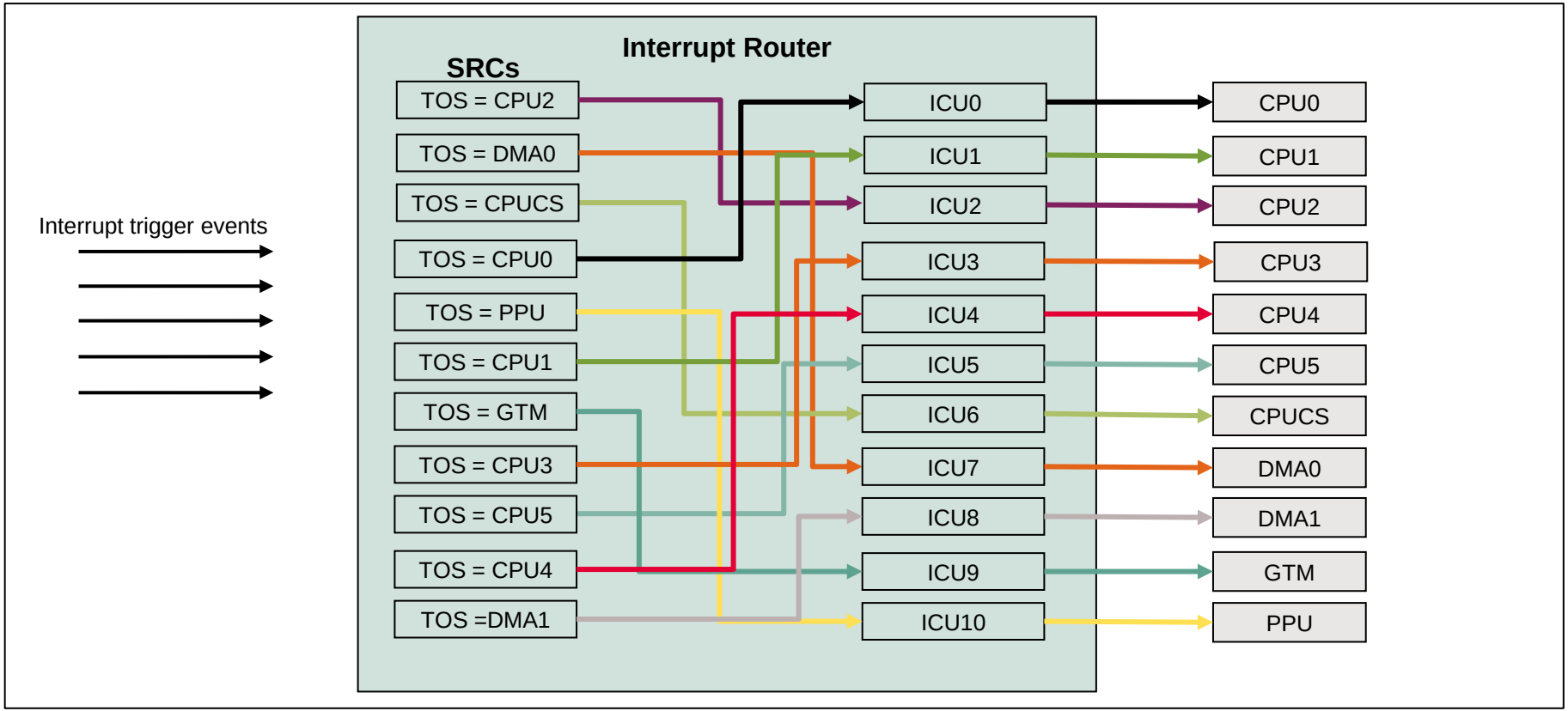
Assign a priority for each Service Request

Support of software interrupt groups

Customer Benefits

- Each interrupt could be configured to trigger one Service Provider (CPUx, PPU, GTM or DMA)
- Arbitration for pending Service Requests mapped to the same ISP
- One group of eight General Purpose Service Requests (GPSR) per CPU and for the PPU

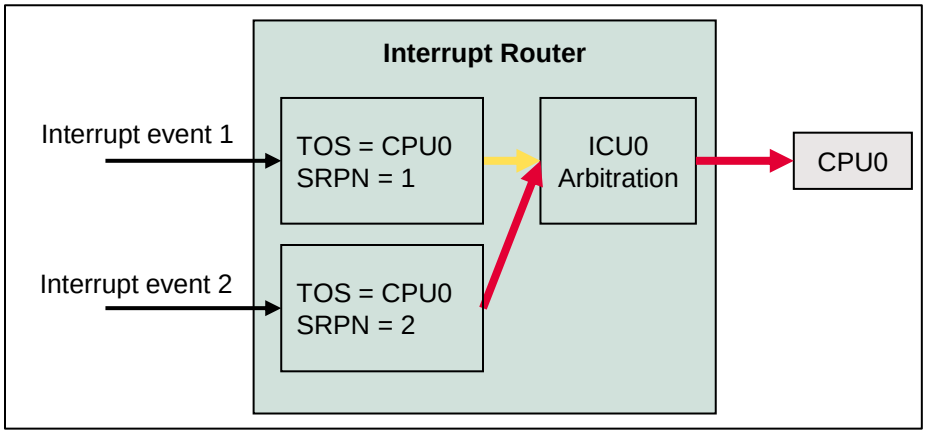
IR
Mapping service requests to service providers



IR
Assign a priority for each service request

- A Service Request Priority Number (**SRPN**) from 0 to 255 must be assigned to each service request :
  - Depending on the selected Service Provider (TOS) the SRPN represents the following:
    - **CPUx**, **GTM** or **PPU**: The interrupt priority of the related Service request (SRPN 0 is neutral)
    - **DMA**: The number of the DMA channel to be triggered

- **Arbitration**:
  - For each ISP, IR arbitrates among the group of pending Service Requests mapped to this ISP. The winner of an arbitration round is the pending SR with the highest priority (SRPN number)
  - *New:* For a CPU with hardware virtualization support, service request arbitration is performed for each active Virtual Machine individually. Following a defined sequence



IR
Support of software interrupt groups

Software Interrupts:
- One group of 8 GPRS is implemented per CPU and PPU
- Broadcast feature per GPRS group (SW compatible to TC3x)

New: Each GPSR has a software control register (SWC) including the following functionalities:
- Data bit field can be transferred from SW to ISP
- Data bit field handshake protected
- Can be used to control associated GPSR
- Disable / enable broadcast function

SW Control Register

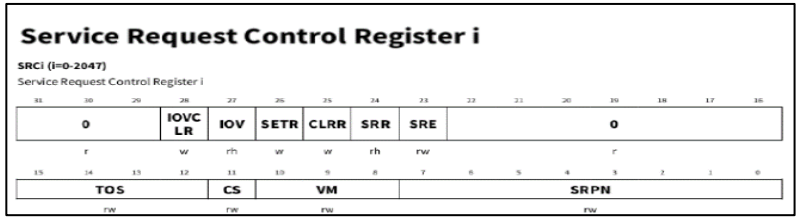
GPSRGx_SWCy (x=0-15;y=0-7) — Offset address: 0720_H+x*40_H+y*4

SW Control Register for GPSRGxSRy — Application Reset value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IOVCLR	IOV	SETR	SRR	BRDIS	0								LOCKSTAT	LOCKCLR	LOCKSET
w	rh	w	rh	rw	r								r	w	w

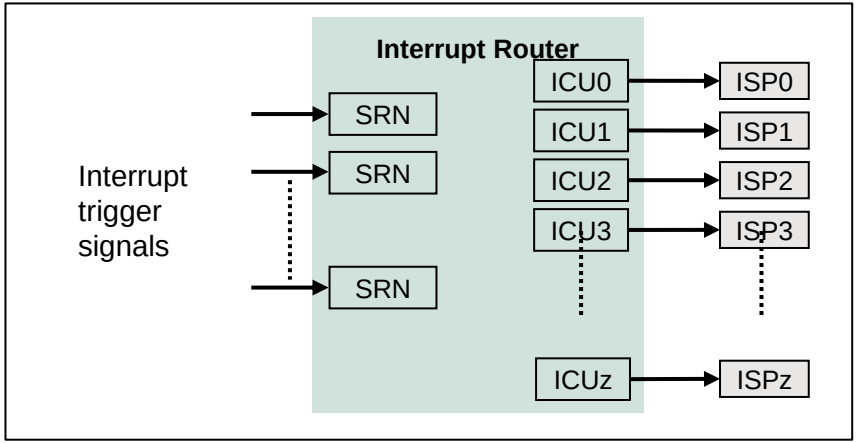
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA															
rw															

- Each peripheral interrupt has a dedicated Service Request Node (SRN) configurable through the Service request Control (SRC) Register:
  - ***TOS***: Target Interrupt Service Provider
  - ***VM***: Target Virtual Machine, if applicable
  - ***SRPN***: SR priority number
  - ***CS***: Cyber Security bit used to assign a SR to a security or non-security application



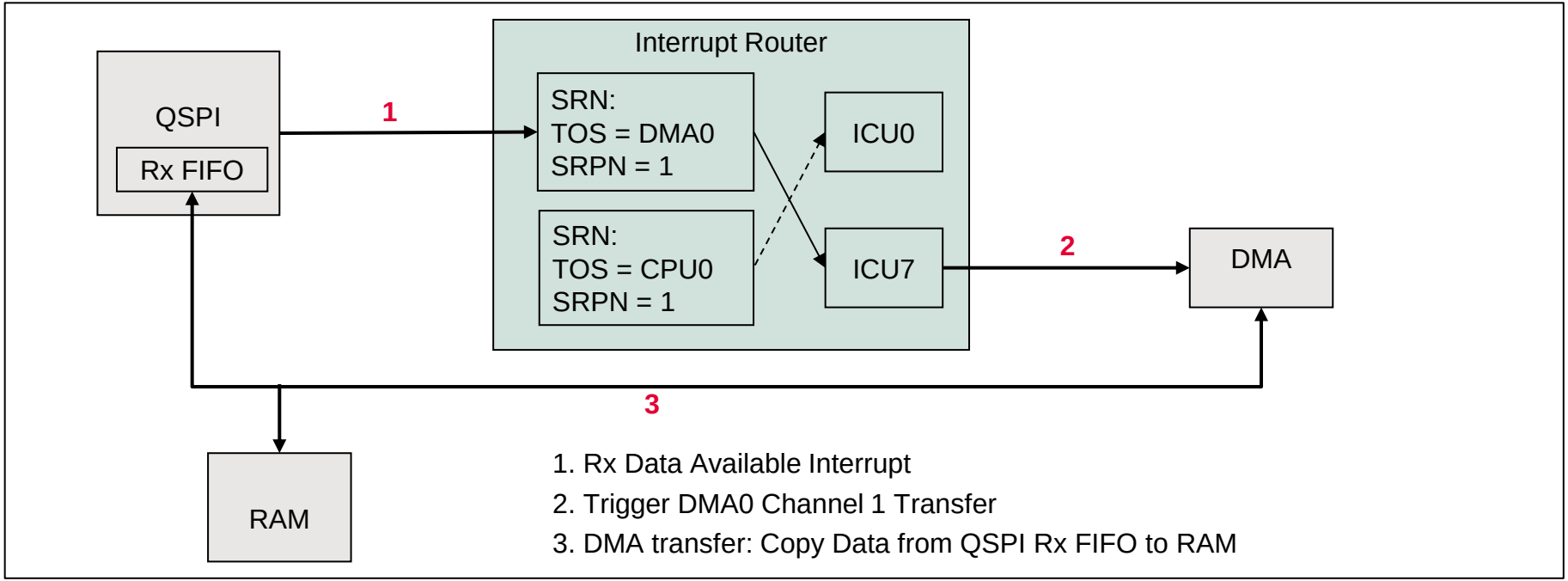
- Each Interrupt Service Provider has a dedicated Interrupt Control Unit

- Parallel and independent arbitration for pending service requests mapped to different ISPs



Application example
DMA transfer

› In this example data is transferred from the QSPI FIFO registers to internal memory without any CPU intervention



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