



DSADC

Delta-Sigma Analog-to-Digital Converter

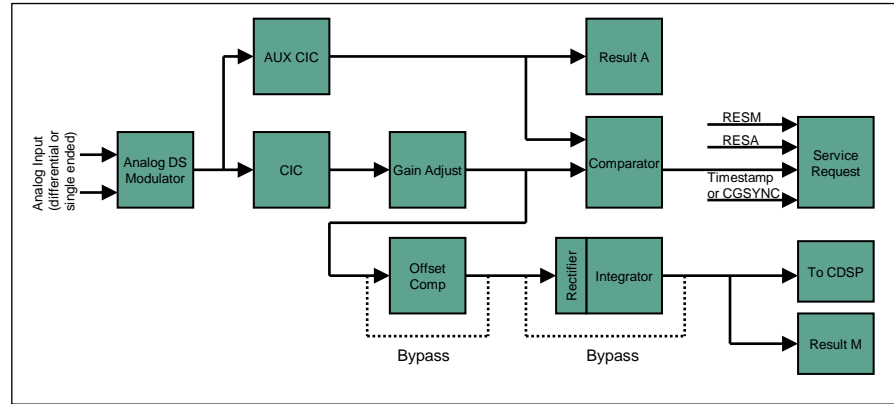
AURIX™ TC4xx Microcontroller
V1.0.0 2024-09

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DSADC

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Highlights

- › Cascaded Integrator Comb (CIC) filter decimation up to 1024
- › Gain correction and offset compensation
- › Signal rectification, carrier cancellation and integration
- › Event signaling to interrupt router and boundary flag connection to GTM and eGTM

Key Features

Up to 86 dB SNR

External Modulator support (MOD)

Customer Benefits

- › ENOB accuracy up to 14 bit (related to pass band (f_{PB}) and modulator frequency (f_{MOD}))
- › Support external isolated DSADC modulator
- › Separate pin not to waste DSADC core resource
- › Manchester decoder to save one clock signal

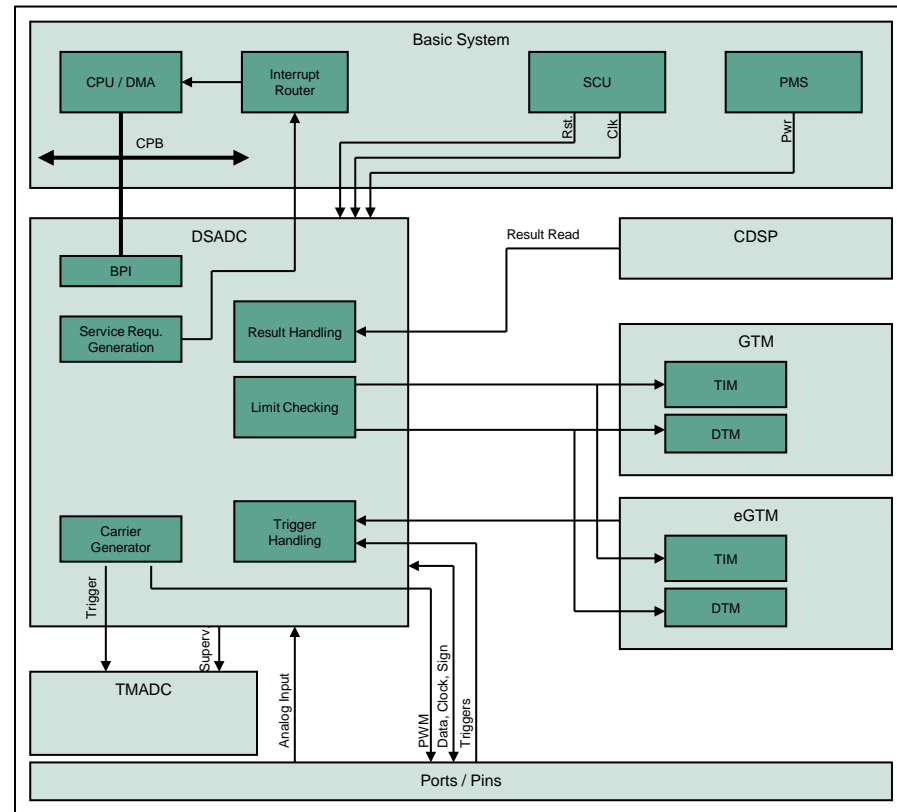
- › DSADC supports up to 40 MHz sampling rate (f_{MOD})
- › The accuracy performance depends onw:
 - which connection mode is used (differential mode is optimal)
 - If calibration is done or not
 - if all filters are enabled
 - the limitation on pass band
- › The conversion between SNR (dB) and ENoB (bit) is:
$$\text{ENoB} = (\text{SNR} - 1.76) / 6.02$$
- › In automotive industry, high accuracy ADC results are required for application like combustion engine in-cylinder pressure measurement and fuel injection control etc.

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- The block diagram illustrates the digital signal processing architecture. It begins with two 8-bit ports: 'Data' and 'Clock'. The 'Data' port feeds into a 'Digital Data Sync/Async' block, which also receives input from the 'Clock' port. The output of this block goes to a 'Manchester Decode Enable/disable' block. The output of the Manchester block feeds into a 'CIC' (Cascaded Integrator-Comb) block. The output of the CIC block goes to a 'Gain Adjust' block. The output of the Gain Adjust block feeds into a 'Comparator' block. The output of the Comparator block goes to a 'Result M' block. The output of the Gain Adjust block also feeds into a 'To CDSP' block. The output of the Gain Adjust block also feeds into a 'Result A' block. The output of the Gain Adjust block also feeds into a 'Service Request' block. The output of the Gain Adjust block also feeds into a 'Timestamp or CGSYNC' block. The output of the Gain Adjust block also feeds into a 'RESA' block. The output of the Gain Adjust block also feeds into a 'RESM' block.

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System integration

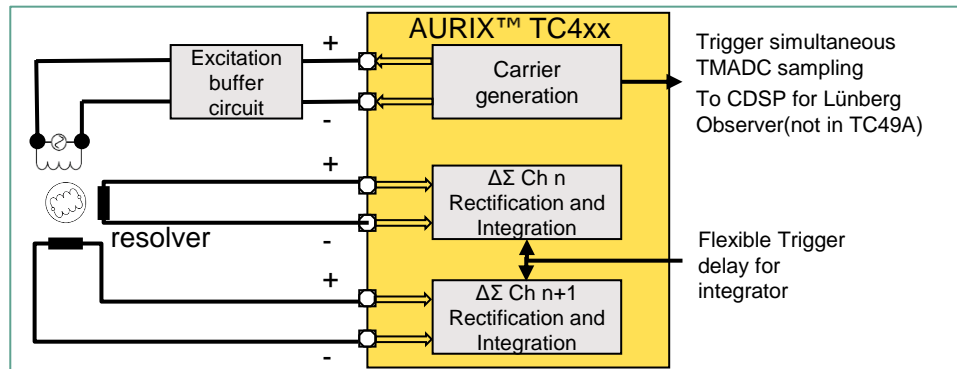
- › Carrier generator can trigger:
 - Time-Multiplexed Analog-to-Digital Converter (TMADC) on the peak values of the carrier pattern
 - Converter Digital Signal Processing (CDSP)
- › Analog Supervision signals from DSADC to input of monitoring samplers in TMADC
- › HW trigger sources are:
 - › Generic Timer Module - GTM (up to 36)
 - › Enhanced Generic Timer Module - eGTM (10)
 - › PORTS (up to 8)
 - › External Request Unit - ERU (up to 8)
 - › Carrier generator (1)
- › Boundary Flags are connected to GTM & eGTM through central ADC MUX
- › Main Result register of DSADC & EXMOD can be mapped to input of CDSP
- › Service Request going to IR



Application Example

Enhanced Resolver Support

- › The carrier generator output is differential
- › Excitation buffer converts digital signal to sinusoidal wave
- › 2 orthogonally placed coils are excited by the magnetic field of the third coil, which is connected to carrier buffer circuit
- › After integrator, carrier is cancelled. With software trigonometric computation or Lünberg Observer of CDSP, the rotary position can be determined



Overview

- › Resolver application occupies the carrier generator and 2 DSADC channels: one for sine and one for cosine signals
- › Dedicated resolver sensor can be saved to reduce system cost
- › Trigger of Integrator can be delayed
- › Simultaneously trigger TMADC sampling

Advantage

- › AURIX™ provides carrier generator and integrator, which are conventionally provided by resolver sensor
- › User just needs to implement the external excitation buffer circuit
- › Hardware delay of integrator can be compensated to improve angle calculation accuracy
- › To reach ASIL-D by the redundant path

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Edition 2024-09

**Published by
Infineon Technologies AG
81726 Munich, Germany**

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**Document reference
AURIX_3_Delta_Sigma_Analog-
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