CANXL
Controller Area Network XL interface

AURIX™ TC4xx Microcontroller

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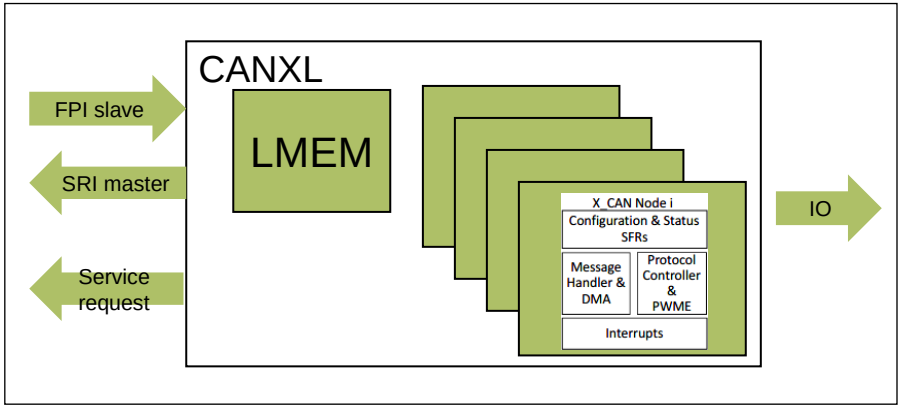
CANXL
Controller Area Network XL interface



Highlights

- Classical CAN and CAN FD communication according to ISO11898-1:2015
- CAN XL communication according to CiA 610-1
- Compatible to existing CAN, CAN FD and CAN SIC transceiver
- Up to 4 CAN XL nodes

Key Features

Local Memory (LMEM) stores up to 255 RX filter elements

8 TX FIFO Queues and one TX Priority Queue, 8 RX FIFO Queues

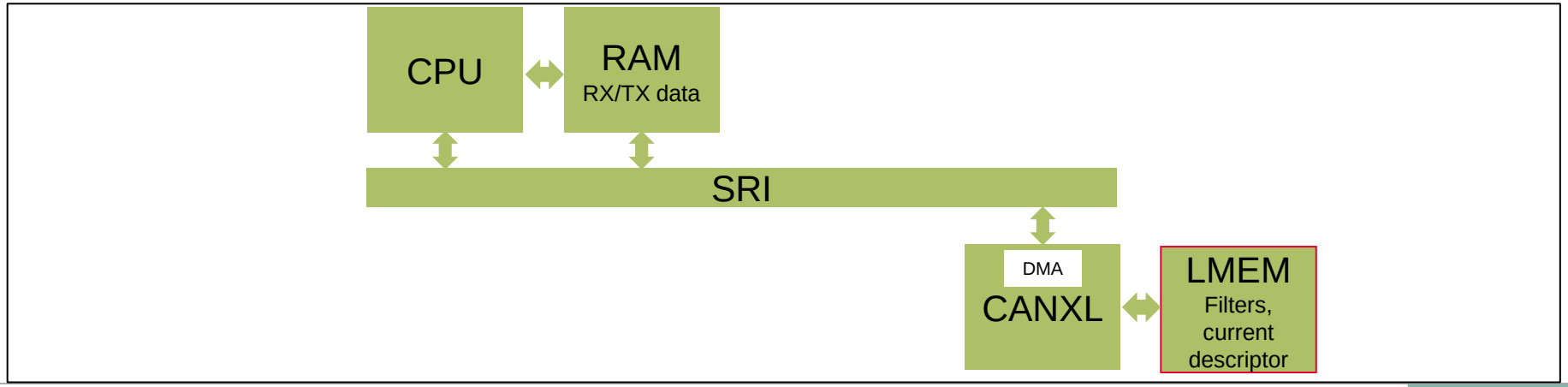
Integrated DMA for message transfers without CPU load

Customer Benefits

- Data rates up to 15Mbit/s
- Large payload up to 2048 byte enables the use of higher layer protocols and enhanced security
- Interoperability with CAN FD for mixed FD/XL networks

CANXL
Local Memory (LMEM) stores up to 255 RX filter elements

- Up to 16 Kbyte shared by the CANXL nodes
- Local RAM
  - buffers part of RX/TX messages during transfer from/to system memory
  - holds acceptance filter elements
  - holds active descriptors for DMA transfer to system memory



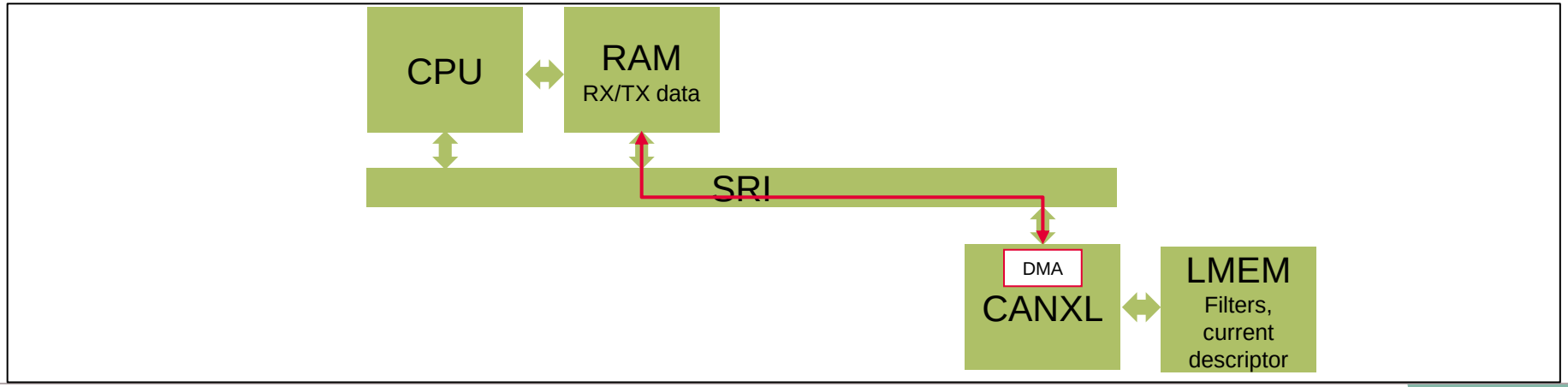
CANXL
8 TX FIFO Queues and one TX Priority Queue, 8 RX FIFO Queues

- Usage of queues makes multiple message transmission easier to manage and to prioritize
- 1 transmit priority queue with maximum of 32 slots for ID-based priority transmission of CAN frames
  - The controller will first compare the message ID value for all messages that are in the priority queue and prioritize the transmission of the message with the lowest message ID
- Maximum 8 TX FIFO queues, each with up to 1024 messages
  - The controller will transmit the messages in the order they were placed in the FIFO
- The selection of the TX message is done by looking at the queues in the following order, TX Priority Queue slots from 0 to 31, then the TX FIFO Queues are scanned from 0 to 7

- Maximum 8 RX FIFO queues, each with up to 1024 messages
  - The controller will place the received message into the appropriate RX FIFO based on the filter settings

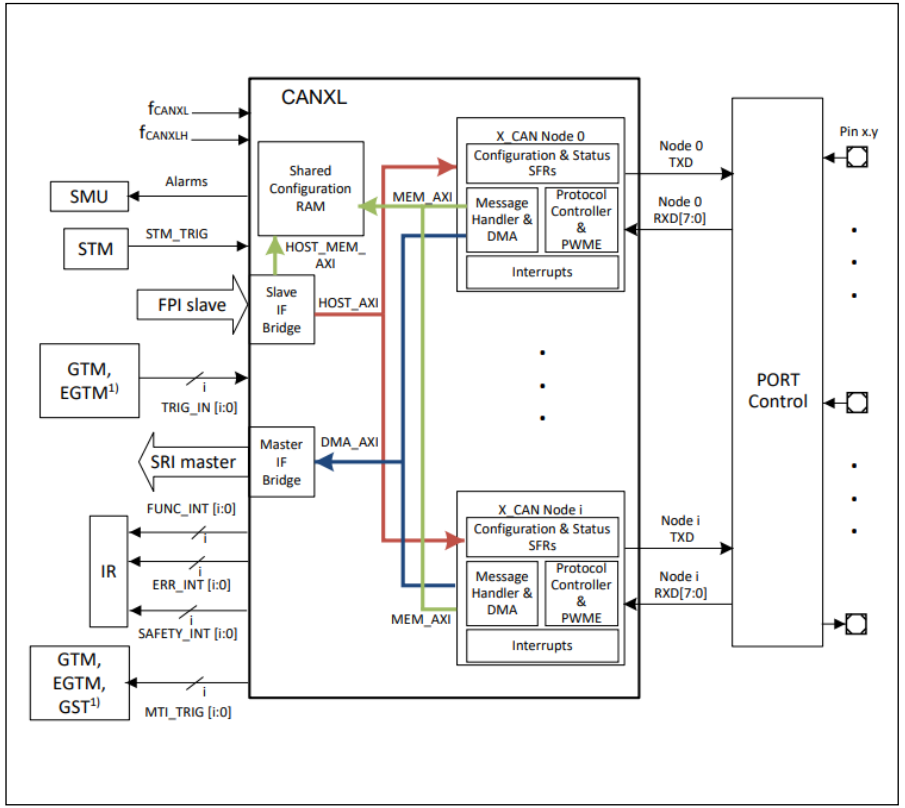
CANXL
Integrated DMA for message transfers without CPU load

- CANXL acts as DMA master in the SRI bus for message handling
- Received data and data to be transmitted is stored in system memory
  - Transfer of payload handled by DMA descriptors
  - Reduced interrupt load for processor core

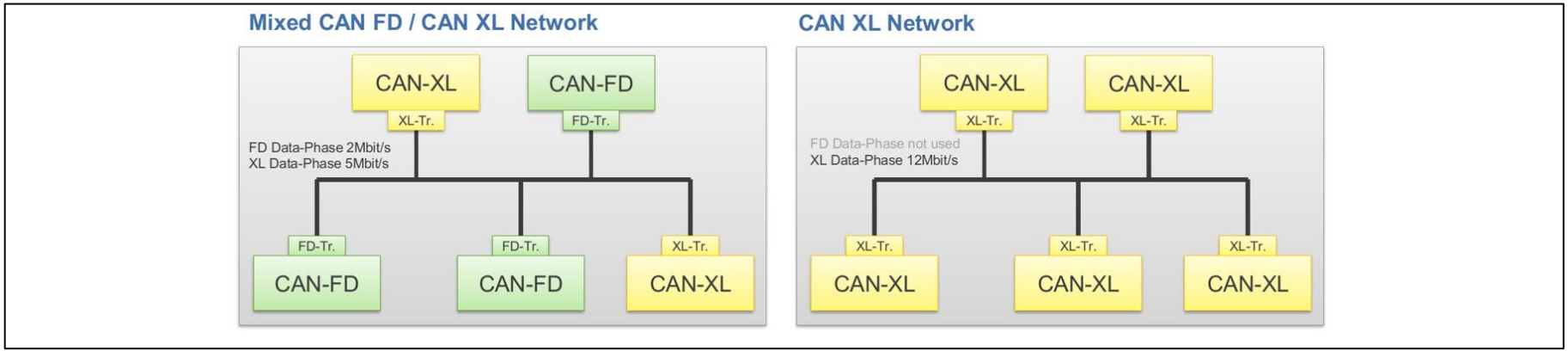


CANXL
System integration

- **Clock**
  - fCANXLH (max. fSRI/2): Clock for message handler, DMA, LMEM
  - fCANXL (max 160MHz): reference clock to configure bit timings (Protocol controller)
- **Service requests per node**
  - CANXL_IR_FUNC_INT: functional events
  - CANXL_IR_ERR_INT: error events
  - CANXL_IR_SAFETY_INT: safety error events
- **Time stamp time base clock sources**
  - fCANXLH clock, STM trigger, GTM or eGTM trigger
- **IO interface per node**
  - PORTS_CANXL_RXD[7:0]: Multiplexer selecting receive input signal of the CANXL node from available pins
  - CANXL_PORTS_TXD: Transmit output signal connected to a selection of pins



Application example
Interoperability with CAN FD for mixed FD/XL networks



Overview

- Mixed CAN FD / CAN XL Network: 2 data bit rates on the same bus
  - The CAN-XL node can receive the data of the CAN-FD nodes
  - The CAN-FD node will ignore the CAN-XL data (limited to SIC mode and Error Signaling enabled)

Advantages

- Simple migration path for existing CAN FD networks
- CANXL large payload size
- Higher speed

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