Hardware design guide for the TRAVEO™ T2G family

About this document

Scope and purpose

This application note describes how to set up a hardware environment for the TRAVEO™ T2G MCU family.

Intended audience

This application note is intended for hardware designers.

Associated part family

TRAVEO™ T2G automotive microcontroller.

Table of contents

Table of contents

Table of contents

Table of contents

1 Introduction

This document describes how to set up a hardware environment for the TRAVEO™ T2G MCU family.

Design restrictions and recommendations regarding signal wiring and the electrical power system of the MCU are considered. For details on device features and their relevant settings, see the TRAVEO™ T2G architecture technical reference manual (TRM) and the dedicated device datasheet in the Related documents section.

This application note answers most of the frequent questions. It is not intended to replace the designer's responsibility.

2 Package selection

First, decide the package you want to use for your design. The following considerations drive this decision:

- Number of I/O pins required
- PCB and product size
- PCB design rules
- Thermal and mechanical stresses

The device families have a very large selection of devices to help match your exact needs in any situation with an efficient and cost-effective solution. Packaging solutions range from the ultra-small wafer scale packages to high-pin-count ball grid array (BGA) packages. Easier to layout on lower layer counts and lower-cost PCBs are the leaded quad flat pack (LQFP). LQFP packaging options range from 48-pin devices to 176-pin devices for example.

Some of the package selection criteria are as follows:

2.1 QFN and LQFP

- Easier to route signals due to the large pitch and the open area below the part
- Less mechanical rigidity for more protection against vibration and mechanical stress
- Disadvantages include larger package size and lower thermal conduction (θ_{JA})

2.2 BGA and PBGA

- Small-scale packages offering high pin counts in larger lead pitches, which significantly reduce the manufacturing complexities for high I/O devices. BGA packages are used in applications requiring:
  - Faster circuitry speed because the terminations are much shorter and therefore less inductive and resistive
  - Better heat dissipation
- Conventional surface mount (SMT) production technologies such as stencil printing and component mounting can be used
- Robust reflow processing, due to higher pitch (1.27 mm, 0.050”, typical), better lead rigidity, and self-alignment characteristics. Self-alignment during reflow is beneficial and opens the process window considerably

Disadvantage: X-ray is needed for solder joint inspection.

3 Power supply

3.1 Power domains

MCU power system is based on separate analog and digital supplies. To define a single supply rail, all power supplies should be connected to voltages between 3.3 V and 5.0 V. If you need to apply different power supply voltages, such as 5 V to the analog system (that is, $V_{DDA} = V_{REFH}$) and 3.3 V to V_{DDIO} of the MCU port pins, see the operating conditions in the datasheet of the dedicated device.

Devices designed for applications with higher power dissipation require an external core supply source, which is controlled by dedicated MCU pins. See also Appendix A – Power supply concept.

3.2 ADC supply pins

To avoid additional leakage current, connect the ADC supply pins (V_{DDA}, V_{SSA}, V_{REFH}, and optionally V_{REFL}), even if the ADC is not used.

3.3 Power supply variants

Although separate power supplies are provided in the MCU, dependencies between each other must be considered. The power domains are independent of each other.

3.3.1 ADC

The enabled analog inputs belong to dedicated I/O domains, which means that the applied voltage level of an analog sensor is limited to the I/O domain supply level and the protection diode structure. That means, the analog supplies and the I/O domains of the selected analog inputs must have the same voltage supply level. See Clamping structure of I/O pins with shared analog functions.

3.3.2 Debug connection

Select a power supply on which both the debug HW tool and the MCU can communicate with each other. For more information on the HW connection, see Debug interface.

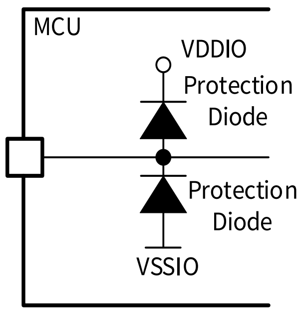


Figure 1 Protection diode structure for all I/O pins

3.4 Power ON/OFF sequence of power supply domains

Different voltage levels can be supplied to the power rails of the MCU. Therefore, the power ON/OFF sequence is not required for the power supplies of many devices. When there is no supply voltage at V_{DDD}, but the analog supply V_{DDA} is powered, a leakage current inside the MCU can occur. However, no port output will be driven. If a device needs a power sequence, see the device datasheet in the Related documents section.

3.4.1 General

- Disable monitoring features (for example, LVD, BOD, internal supply monitoring via ADC) before disabling related power domains. Otherwise, an unintended reset or fault might occur
- Disable or tie to low-output pins before disabling the power domains
- Disable input buffers before disabling the power domains
- Power sequencing requirements and power domain dependencies can differ between power modes. So, when domains need to be switched off to reduce the leakage current in power save modes, carefully consider the transition phase for entering and leaving the modes
- ECU peripherals must be in proper states during power mode transitions

3.4.2 External core supply

Devices running with external core supply have the same power ON/OFF sequence, because the MCU is starting in the internal supply mode and the external core supply must be enabled by the application. In power off transition, the external core supply is disabled by the MCU.

3.4.3 ADC

- In Active mode, leakage current occurs only when $V_{CCD} > V_{DDA\_ADC}$ in (LP) Active and Sleep power modes
- Many I/O domains with shared analog/digital inputs can be ramped up after V_{DDA_ADC}, if the ADC does not start the sampling operation of these domains
- When the I/O domain is deployed only for digital signaling, many I/O domains can also have a voltage operation range different from that of the ADC. See Clamping structure of I/O pins with shared analog functions
- Do not address analog multiplexing bus (AMUXBUS) to unpowered domains

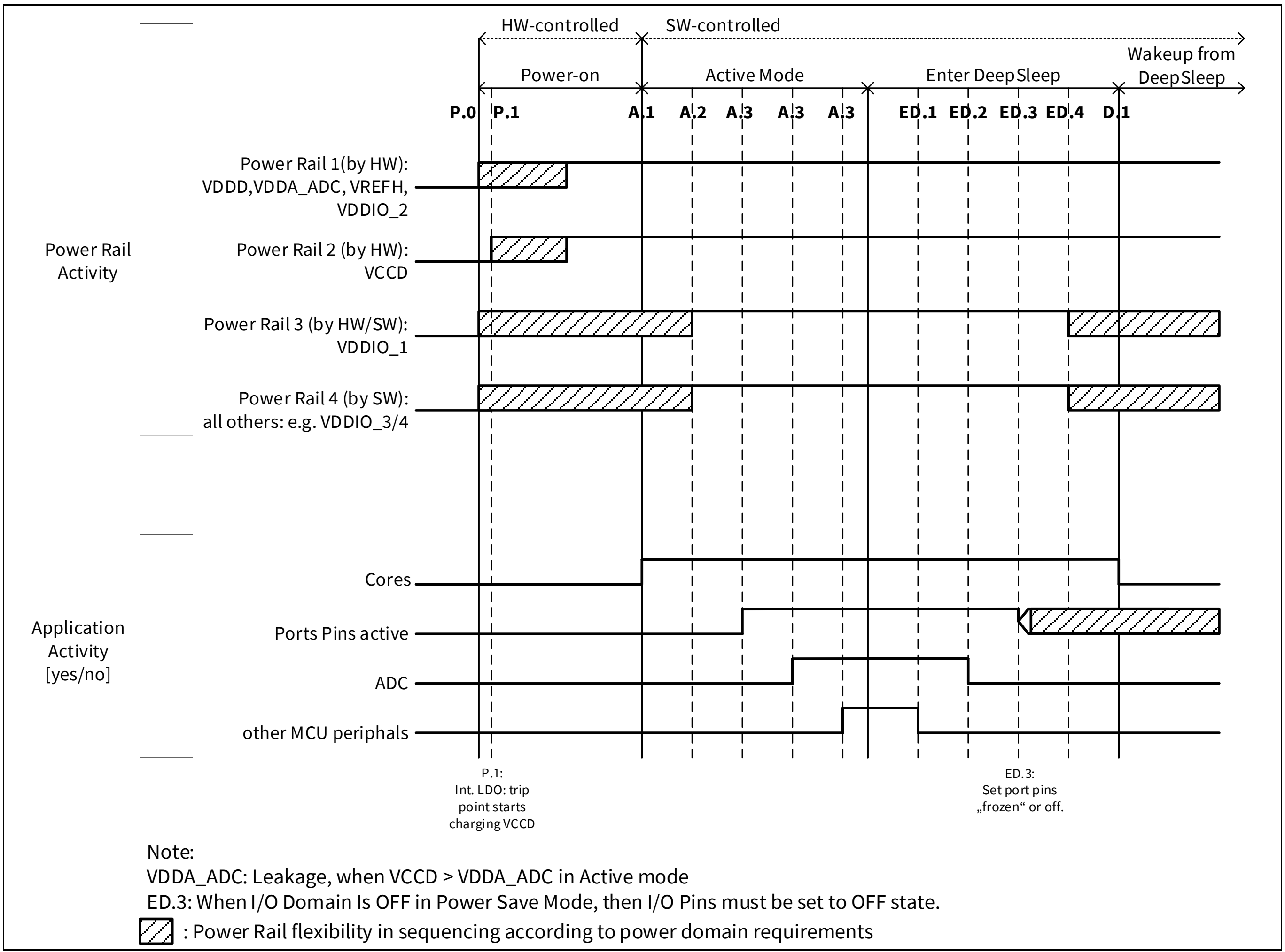


Figure 2 **CYT4B series power sequencing example**

3.5 Power supply circuit

To meet the EMC requirements for the target board, a noise-efficient supply buffering concept is needed. Therefore, the supply should be filtered. To have a minimum noise on the analog supply, it is recommended to use separate analog and digital power supplies.

Power supply concept proposals for different devices are discussed in Appendix A – Power supply concept.

3.6 External core supply control

The power supply concept description is not part of this documentation. See the application note for your device in the Related documents section.

3.7 Unused power domains

An unused power domain is usually considered as a permanent OFF state related to the power domain in the full application lifecycle. However, a temporary state of an unused domain is also possible, when some not-always-on power domains stay on in power save modes. For details on how to handle the I/O port pins of a dedicated domain, see Port input/unused pins.

In general, the following are the main classes of an unused domain:

- **Permanent unused domain:** Not required in the application
- **Temporary unused domain:** Disabled in power save mode

For details on different devices, see Appendix E – Unused power domain handling.

Note: *In principle, you can remove the big bypass capacitors and keep only small decoupling caps (decaps) left on the unused power domains that cannot be grounded. However, you must check if bypass capacitors are also used for other shared power domains in power concept.*

If you do not find information on unused power domains in the device datasheet, contact Infineon support.

4 Clock system

The MCU provides several clock sources depending on the system requirements. Table 1 lists the available clock sources for the MCU system and shows how the clock sources are connected to the MCU internal clock system.

4.1 Clock sources

Table 1 Clock sources

Clock source	Oscillator	Int/ Ext	Port pin name (ext. only)	Frequency	Trimmable	Use case
Internal main oscillator (IMO)	Yes	Int	–	8 MHz	Yes	LIN Responder[1]
Internal low-speed oscillator (ILO)	Yes	Int	–	32 kHz	Yes	–
External crystal oscillator (ECO)	Yes	Ext	ECO_IN ECO_OUT	~4 MHz to 33.33 MHz	Yes	CAN communication
Watch crystal oscillator (WCO)	Yes	Ext	WCO_IN WCO_OUT	32.768 kHz	No	Watch
Low-power external crystal oscillator (LPECO)[2]	Yes	Ext	LPECO_IN LPECO_OUT	~4 MHz to 8 MHz	No	Watch
EXT_CLK pin[3]	No	Ext	Optional on several pins	Note[4]	–	Test
Reference clock for Ethernet PHY and MAC	Yes	Ext	ETHn_REF_CLK	50 MHz	–	Ethernet: RMII
				125 MHz	–	Ethernet: GMII, RGMII

1 As per the device datasheet specification, the IMO clock can be used for a LIN responder either with synchronization or without synchronization.

2 LPECO is available only for CYT4D series.

3 This port pin is bidirectional and can be used as an external clock source for the device and as a clock observation mechanism for internal clock signals.

4 See the device datasheet for external clock input specifications.

5 PLL

With the help of the PLL, it is possible to generate higher output frequencies based on the input reference clock (F_{ref}). The principal setup of a PLL is shown in Figure 3. According to application requirements for nominal target frequency and jitter, the PLLs can have different modii[5]:

- Integer
- Fractional
- Spread spectrum clock generation (SSCG)

Depending on the selected mode, the phase detector frequency (F_{pfd}) has a permitted frequency range. This lso has an impact on the nominal frequency selection of the external clock source (for example, crystal quartz).

5.1.1 Example

Several PLLs share an external crystal quartz as the common clock source and the following modii are used:

PLL#A: Integer mode: F_{pfd} = 4–20 MHz
PLL#B: Fractional mode: F_{pfd} = 8–20 MHz

Result: The crystal quartz must be min. 8 MHz

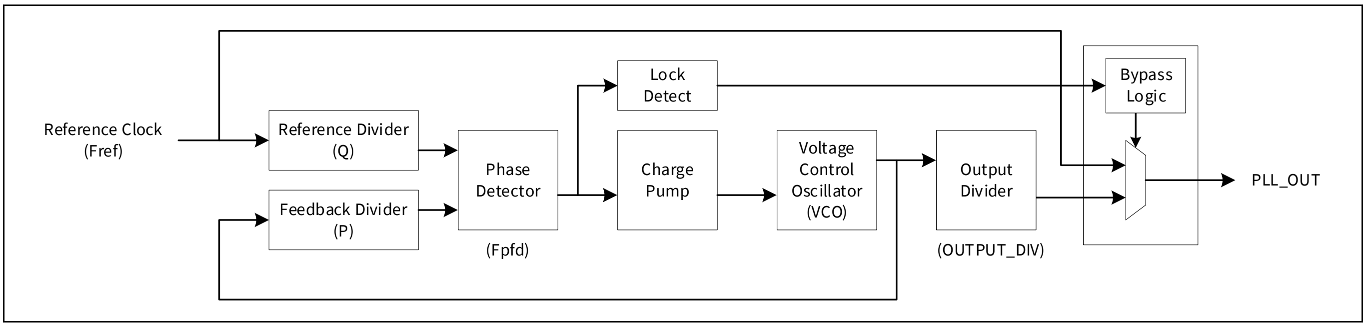


Figure 3 Principle block diagram of PLL

5 See the corresponding architecture TRM in the Related documents for details on each configuration.

6 Reset circuit

To make sure that an MCU operates within specifications, an external reset signal via the reset input pin (XRES pin) or an internal reset signal can be generated. The implementation of the internal reset circuits has several advantages over the hardware design:

- Reduced bill of material (BOM) cost as the external monitoring ICs are removed
- Detection of MCU internal out-of-range operations, which cannot be monitored externally (for example, MCU internal voltage drops)

Note that external monitoring or resetting ICs might still be needed based on the application requirements.

6.1 Reset pin (XRES)

A switch connects the reset input pin to V_{SSIO} (Ground). An internal pull-up resistor and an internal noise filter of minimum 100 ns are available to reduce the BOM cost. If an external capacitor is applied for additional filtering, make sure that the EMC requirements are fulfilled. Otherwise, the ESD test pulses might destroy the ESD protection structure inside the MCU.

For details on the reset pin, see the datasheet.

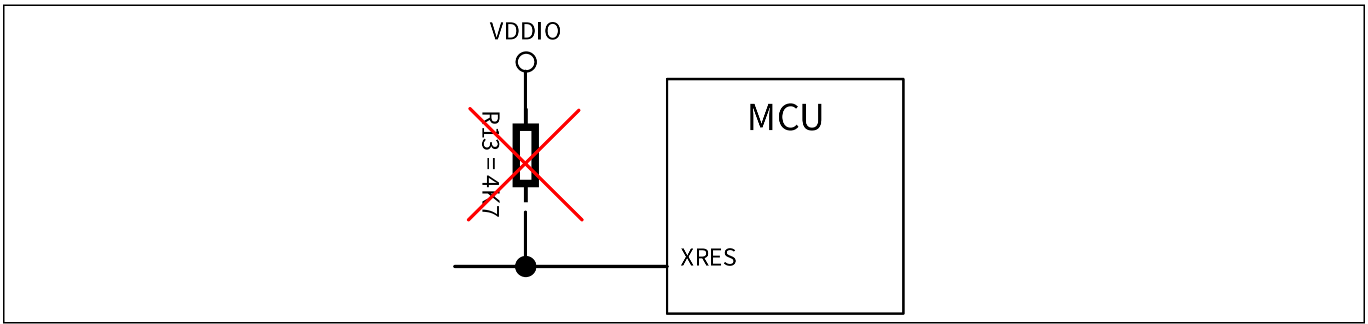


Figure 4 External reset input (XRES)

6.2 Power supply monitoring

To make sure that the MCU is not running beyond operating conditions, a broad range of power monitor circuits is provided by the MCU. For details, see the device architecture TRM and datasheet listed in the Related documents section.

6.2.1 Power-on reset (POR)

Power-on reset (POR) circuits provide a reset pulse during the initial power ramp. Here, only the V_{DDD} power supply rail is observed.

6.2.2 Brown-out detection (BOD)

The brown-out detection (BOD) circuit protects the operating or retaining logic from possibly unsafe supply conditions by applying a reset to the device. BOD circuits for the V_{DDD}, V_{DDA}, and V_{CCD} power supply rails are provided. A reset is generated when one of the monitored operating ranges is undercut. This circuit is required to detect a sneaking voltage drop of the battery power supply.

6.2.3 Low-voltage detection (LVD) and high-voltage detection (HVD)

Before the BOD level threshold generates a reset, you might be warned by the configurable circuit for low-voltage detection (LVD) and high-voltage detection (HVD) use cases. You can configure the trip point (detection level), which creates an interrupt for possible safety measures. This circuit can oversee faster transitions.

6.2.4 Overvoltage detection (OVD)

Overvoltage detection (OVD) circuit applies a device reset when the V_{CCD}, V_{DDD}, or V_{DDA} supply goes above the maximum allowed voltage. This concept is a reverse of the BOD circuit.

6.2.5 Overcurrent detection (OCD)

The overcurrent detection circuit monitors the current of the V_{CCD} power supply rail and detects whether the load current of a regulator is higher than expected. If the current is over the regulator limit, the OCD circuit generates a reset to protect the device.

6.2.6 Power domain voltage monitoring by the ADC

The ADC provides the opportunity to monitor several power supply and ground pads. Instead of a reset, only an interrupt is generated by the corresponding ADC unit. To keep the CPU load low, the range detection feature can be enabled to generate only an interrupt when a critical range is entered. The pads can be selected by a complex multiplexer structure as shown in Figure 5. For details on this feature, see the *Analog subsystem* > *SAR ADC* > *Reference buffer* and *Resources subsystem (SRSS)* > *Voltage monitoring* > *Voltage monitoring by ADC* chapters in the architecture TRM listed in the Related documents section.

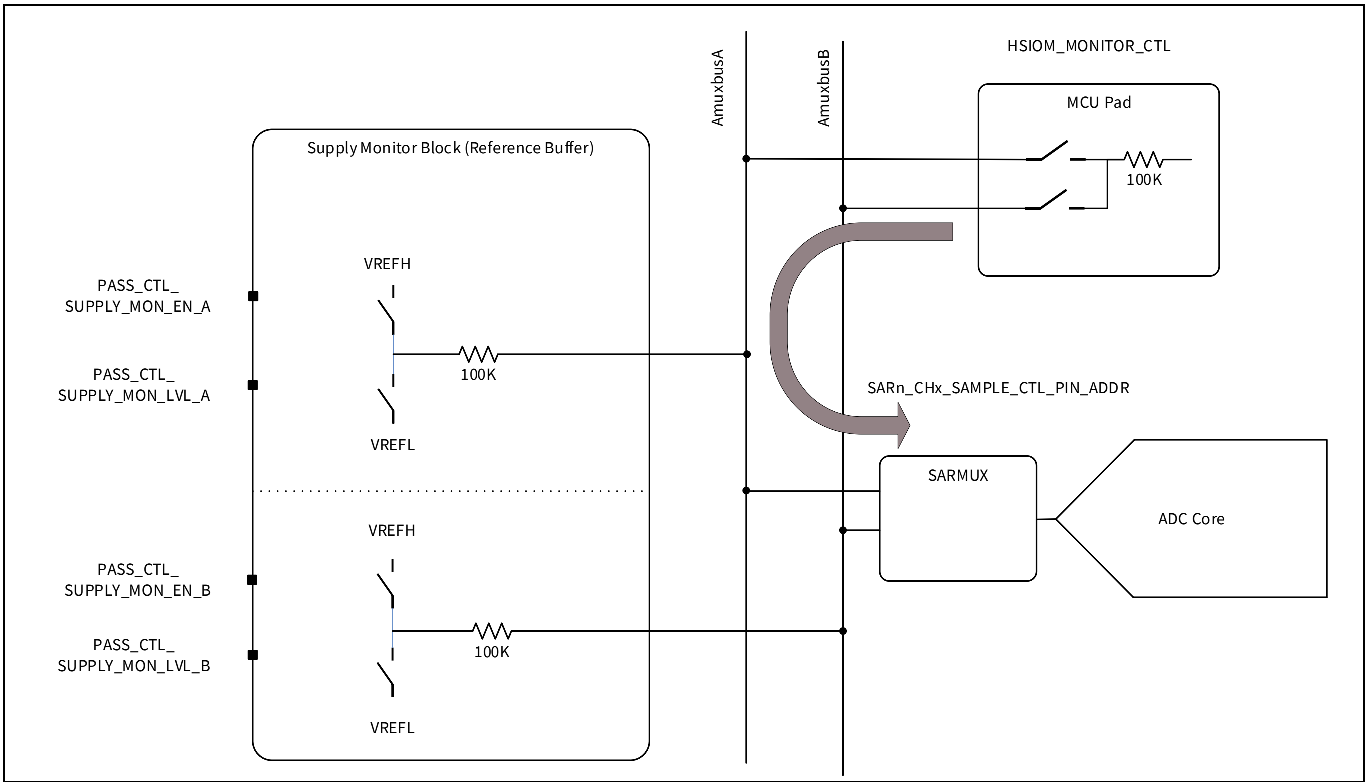


Figure 5 Block diagram of voltage monitoring by ADC

6.3 Watchdog reset

An internal watchdog timer (WDT) within the MCU supports a wide range of capabilities. This WDT circuit can also run in the Hibernate power mode (Refer to “Device power modes” in the architecture TRM listed in the Related documents section).

7 Ports and non-power pins

7.1 Port input/unused pins: General considerations

This section explains the different methods to handle unused pins and the advantages and disadvantages with respect to the MCU operation. In general, the risk of unused pins is floating inputs and a latch-up effect within the pin structure.

7.1.1 Open pin connection

During and after POR, by default, the I/O pins are in a high-impedance (High-Z) analog state with disabled input buffers. The advantage of this method is that the current consumption of the MCU is lower when compared to the use of a terminal resistor, and the BOM cost is reduced. The disadvantage is that during an assembly option, a long signal trace is routed to the pin; the signal trace can take effect as an antenna and a captured noise can cause a latch-up at the pin.

7.1.2 Direct connection to GND or power supply

Do not connect the I/O pins directly to GND or to the power supply as the power supply traces can take effect as an antenna to the pin and the captured noise can cause a latch-up effect.

7.1.3 Internal pull-up/down resistor as termination

When there is a risk of a latch-up effect at an unused pin due to the board design (long traces of optional features), terminate the input pin using internal pull-up or pull-down resistors.

The advantage is low current consumption and BOM cost reduction compared to using external termination resistors. The disadvantage is that you must configure the port pin state after a reset. Therefore, during a reset caused by any disturbance (supply, clock issues, and so on), the internal termination is not available and the system is again vulnerable against a latch-up effect.

You can choose this method if there are unused pins without a long trace. In general, it must be considered that the pin state (enabled pull-up or pull-down resistor) must be unchanged when a low-power mode is entered. The reason is that for an external resistor, the internal termination must be available all the time.

7.1.4 External pull-up/down resistor as termination

An external termination resistor can be placed next to the unused I/O pin instead of using the internal ones. In the case of an open signal line routed to the pin, any injected noise can be safely terminated even during a device reset. A resistor value between 2.2 kΩ and 10 kΩ can be used. However, do not connect several unused pins to one common termination resistor because if unused I/O pins unintentionally drive different output levels against each other, the I/O pins might be permanently damaged.

7.2 Dedicated port pins

For dedicated MCU peripherals, the unused I/O handling is explicitly considered. In most of these cases, the entire MCU peripheral including the power domain pins must be considered to avoid the risk of latch-up (LU). For details on power domain pins, see Unused power domains.

Table 2 Handling of unused dedicated I/O pins

MCU peripheral	Power domain	I/O pin	I/O function [IN/OUT]	Pin I/O handling (Connect to …)
MIPI	VDDA_MIPI	MIPI_DPx x: 0/1/2/3	IN	Open pin connection
	VDDA_MIPI	MIPI_DNx x: 0/1/2/3	IN	Open pin connection
	VDDA_MIPI	REXT	IN	Open pin connection (external 15 kΩ removed)
FPD	VDDA_FPD	FPD_TxP x: A/B/C/D	OUT	Open pin connection
	VDDA_FPD	FPD_TxN x: A/B/C/D	OUT	Open pin connection
Audio-DAC	VDDA_DAC	C_L, C_R	IN	GND (when Mono sound: Open pin connection of the unused part)
		DAC_L, DAC_R	OUT	
REGHC/PMIC Controller	VDDD (always-on)	DRV_OUT	OUT	Open pin connection

7.3 Port pin configuration in AUTOSAR MCAL

The microcontroller abstraction layer (MCAL) of AUTOSAR is a low-level driver for the microcontroller, which is used in the software developed for automotive applications. So, the port pin configuration with the PORT module is part of the MCAL.

The following are the possible risks if there is a wrong port pin setting to the MCU:

- I/O structure being destroyed
- Additional leakage current in power save modes
- Latch-up effect

Therefore, especially with regard to the latch-up risk, keep the software port pin configuration always compliant with the HW concept for unused I/O pins (see Port input/unused pins) and unused I/O power domains (see Unused power domains). This is also relevant for the SOFTWARE-controlled power sequencing procedure in which unpowered I/O domains must be considered as unused power domains.

In the MCAL PORT module, you can configure port pins depending on different use cases within the corresponding application cycles, each time in a PortContainer. All port pins, which are not explicitly configured by the dedicated PortContainer will be implicitly configured according to the PortDefaultContainer. The `Port_Init()` API sets all pins of the derivative device either according to the explicit configuration in PortContainer (if the pin was configured) or the implicit configuration in PortDefaultContainer (if the pin was not configured in PortContainer).

The `PortPinDirection=PORT_PIN_IN` setting sets the pin as an input and enables the input buffer. If a pin is not needed (that is, no output and no input required), the pin should be configured to `PortPinDirection=PORT_PIN_OUT`, `PortPinOutputDrive=PORT_PIN_OUT_MODE_HIGHZ`, and `PortPinOutputInBufEnable=FALSE`. This is the only recommended setting for PortDefaultContainer, but the key is to be compliant with the latch-up HW requirements to I/O pins.

7.4 Pins in low-power mode

To achieve the lowest possible quiescent current in a low-power mode, the current consumption of I/O pins must be considered. Depending on the low-power mode, the configuration state and the last output state are frozen. In the case of input pins, it is forbidden to have floating input levels because the quiescent current of the MCU increases dramatically. When an input pin is used as a wake-up pin, do not change the configuration under the assumption that the pin has an internal or external pull-up or pull-down resistor for termination. When an input pin is not required in a low-power mode, it can be configured as a High-Z input with a disabled input buffer. For details on different low-power modes, see the architecture TRM and the corresponding application note listed in Related documents.

7.5 Latch-up considerations (Switch)

Pressed switches usually cause a bouncing signal, which can damage the MCU port pin. As a countermeasure, debounce capacitors are deployed. Exercise caution with external switches to V_{CC} or ground together with debounce capacitors connected to port pins.

A usual configuration is shown in Figure 6.

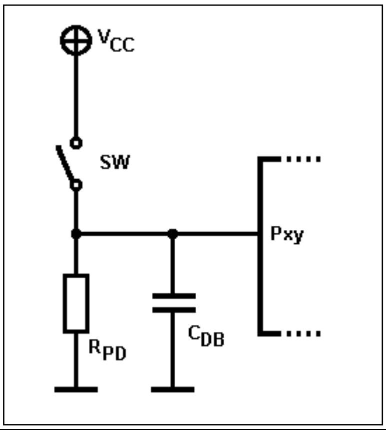


Figure 6 Principle switch circuit

R_{PD} is a pull-down resistor and C_{DB} a debounce capacitor. If the switch software is open, a “0” is read from the port pin Pxy. When the switch is closed, the input changes to “1”.

From the physical aspect, it needs to be considered that the switch is often placed at a distance from the MCU by cable, wire, or circuit path. The longer the circuit path is, the higher is its inductivity LX (and capacity CX).

An equivalent circuit diagram is shown in Figure 7.

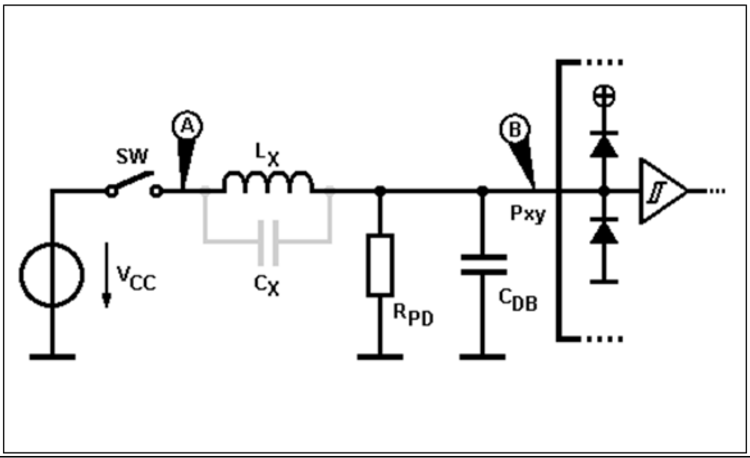


Figure 7 **Equivalent circuit of the principle switch circuit**

By closing the switch software at time t_0, as shown in Figure 8, the voltage can be measured at point (A).

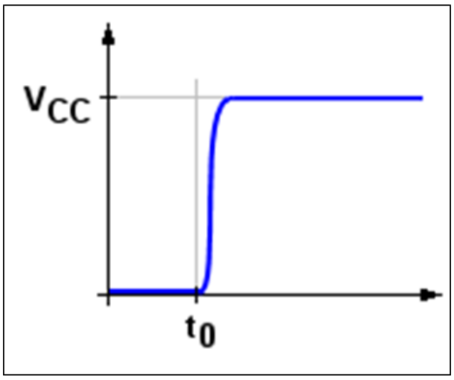


Figure 8 **Signal rise after closing the switch at Point (A).**

However, at the port pin Pxy on Point (B), as shown Figure 9, voltage can be measured.

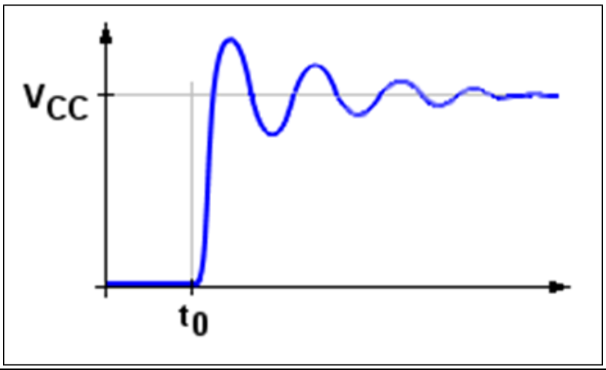


Figure 9 **Signal rise after closing the switch at Point (B)**

By closing the switch software, the circuit becomes a parallel oscillator with the wire inductivity L_x, the debounce capacitance C_x, and the damping R_{PD} of the pull-down resistor (It is assumed that it is an ideal power supply, that is, it has no internal resistance).

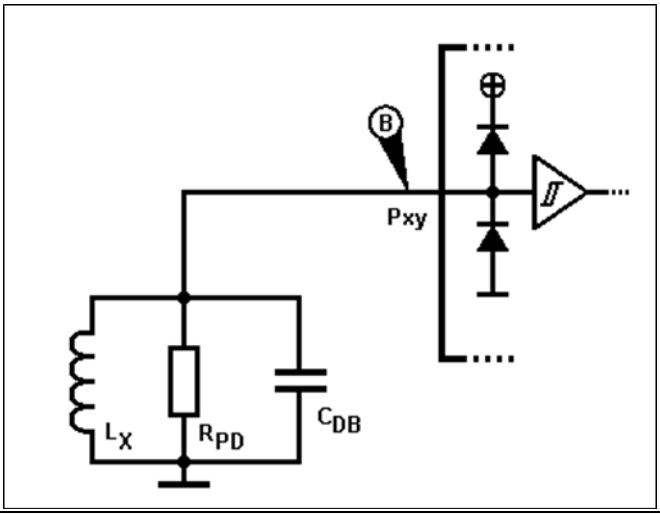


Figure 10 Equivalent circuit during closed switch

R_{PD} is often chosen high (> 50 kΩ), and so its damping effect is weak.

This (weakly) attenuated oscillator causes voltage overshoots on the port pin (Point (B)), as shown in red in Figure 11.

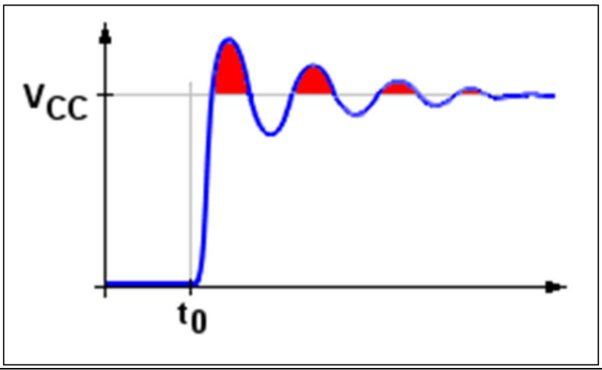


Figure 11 Signal overshoots on the port pin after closing the switch

These overshoots may cause an internal latch-up on the port pin, as the internal clamping diode connected to the internal power supply becomes conductive. Similar is the effect if the switch software is opened. In this case, there are undershoots on the port pin.

The frequency of the oscillation can be calculated by:

$$f_{OSC} = \frac{1}{2\pi\sqrt{L_X C_{DB}}}$$

Equation 1

The inductivity (LX) is an unknown value and depends on the PCB, its routing, and the wire length.

There are two counter measures to prevent a latch-up.

7.5.1 Solution A

Decrease the capacitance of the debounce capacitor. This increases the oscillation frequency, which causes the overall energy of the overshoots to be smaller.

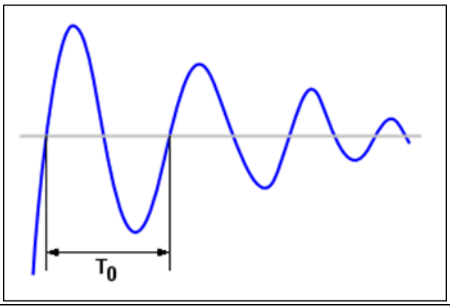


Figure 12 Bounce signal on the pin with a large capacitance

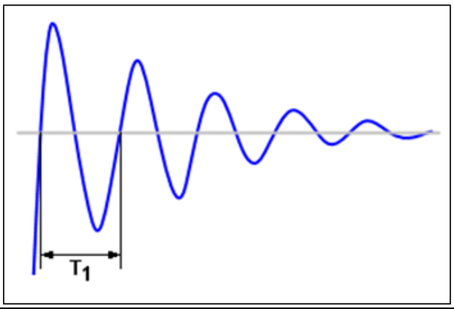


Figure 13 Bounce signal on the pin with a small capacitance

This solution has two disadvantages: the debounce effect decreases and there is no guarantee that the latch-up condition is eliminated.

7.5.2 Solution B (recommended)

Use a series resistor (R_S) at the port pin as shown Figure 14.

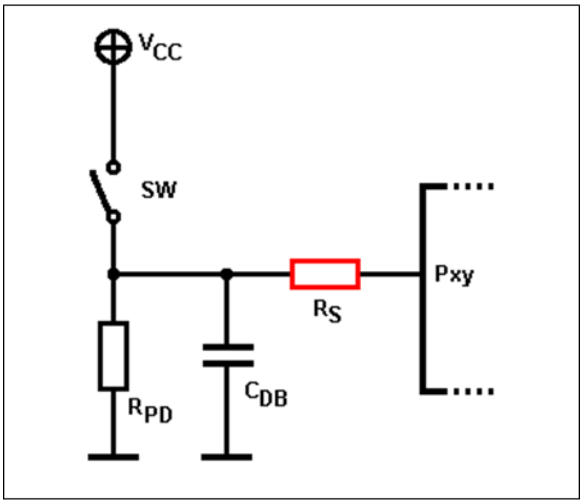


Figure 14 Recommended switch circuit with series resistor

The series resistor R_S reduces the amplitude of the oscillation and decreases the voltage offset at first. Do not choose too high a resistor value. Otherwise, the port pin input voltage (V_P) will be below the high input level threshold of the dedicated port pin (for example, CMOS/TTL/Automotive level).

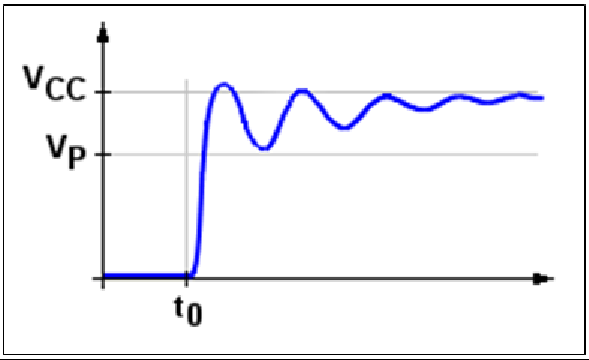


Figure 15 Reduction of the signal bouncing on the pin due to the series resistor

7.6 5-V-tolerant input pins

The MCU does not have 5-V-tolerant input pins if the corresponding I/O domain has a smaller voltage supply (for example, 3.3 V). In the case of the deployment of an I^2C bus system with 5 V, and if V_{DDIO} is supplied with 3.3 V, an external level shifter must be added to avoid the latch-up effect on the MCU pin.

7.7 Reset behavior of I/O port pins

During and after the power-on reset (POR), all GPIOs are in high-impedance analog state and the input buffers are disabled. During runtime, GPIOs can be configured by writing to the associated registers. The Debug Access Port (DAP) connection can be disabled or reconfigured for general-purpose use only after the code execution starts.

7.8 Glitch filtering

The MCU provides the option of internal glitch filtering. As the glitch filters are not available on every port pin, the assignment of wakeup pins must be done with caution. Before assigning wakeup pins, check the number of available glitch filters in the device datasheet.

7.8.1 Analog filter

Every port group has one analog filter, which also works in DeepSleep mode. For details on AC characteristics, see the device datasheet.

7.8.2 Digital-based filter

The smart I/O module in the I/O system can implement one digital-based filter in dedicated ports. In the DeepSleep mode, either the internal low-speed oscillator (ILO) or the external crystal oscillator (ECO) clock can be selected as the clock source (see Clock system). This means that the minimum filter period is ~30 µs. Additionally, the current consumption increases because a clock is running. For more information, see "smart I/O, I/O system" in the architecture technical reference manual (TRM) listed in the Related documents section.

See Latch-up considerations (Switch) for the latch-up considerations regarding deployed external filters.

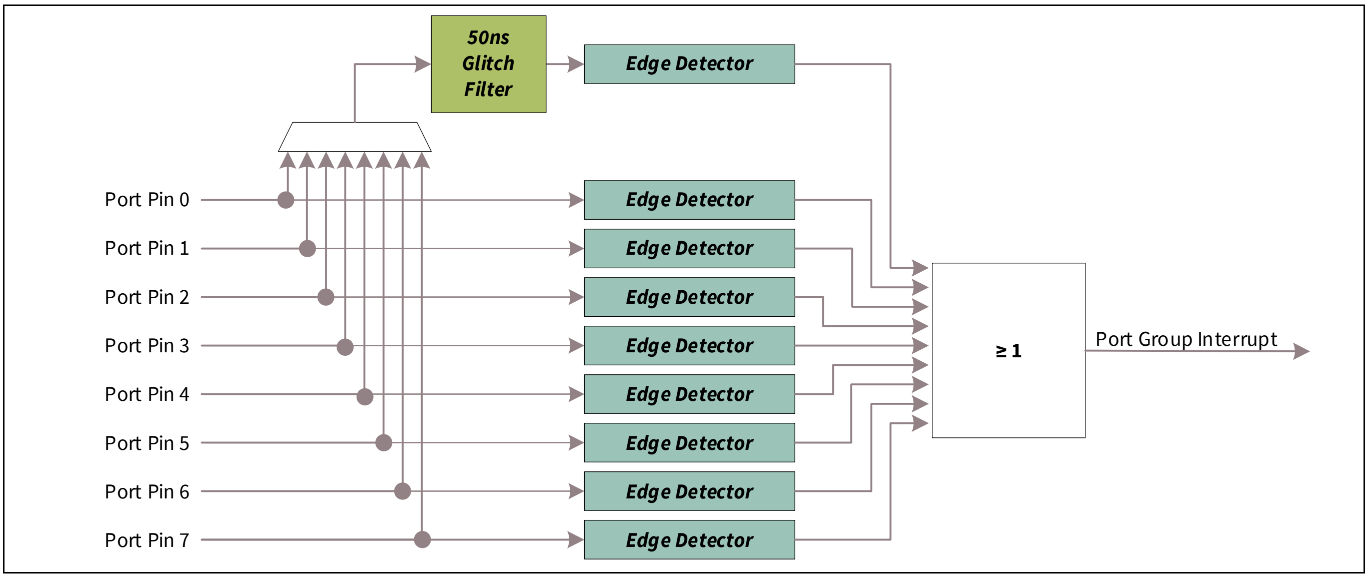


Figure 16 Port glitch filter and interrupt structure

7.9 Mode pin

A dedicated Mode pin is not required to enter the MCU into programming or normal run mode.

7.10 External interrupt input pins

In general, an external interrupt can be captured by edge detection on every general-purpose I/O (GPIO) port pin. See Glitch filtering to learn how to use glitch filtering.

Table 3 lists the wakeup sources in the different power modes. For more details on the power modes, see the "System resources subsystem (SRSS)" and "Device power modes" sections in the corresponding TRM.

Table 3 External interrupt/wakeup support in power modes

	External interrupt/wakeup in power mode			
Port pin function	**Active**	**Sleep**	**DeepSleep**	**Hibernate**
GPIO	Yes	Yes	Yes	–
Dedicated peripherals[6]	Yes	Yes	Yes	Yes
WAKEUP[7]	–	–	–	Yes

[6] See the architecture TRM, device datasheet, or both in the Related documents.

[7] The WAKEUP function is supported only on a few pins.

7.11 Clamping structure of I/O pins with shared analog functions

It is important to identify the power supply domains that must have a common supply level in each application. Figure 18 and Appendix G – Clamping structure of I/O pins with shared analog functions provide the overview of the clamping structure and the consequences when the analog input function is used on dedicated power domains. When any port pin of a dedicated power domain (PD) is applied as an analog input, the domain must have the same voltage level or lower than the analog supply (VDDA_ADC). Appendix G – Clamping structure of I/O pins with shared analog functions lists the special use cases.

As soon as the ADC unit is in use, the deployed SARMUX must also be powered. For example, when an analog input AN[1]_x of SARMUX[1] is used by the ADC[0] unit, the I/O power domain of SARMUX[0] is not relevant. Note that the SARMUX supplies the external (for example, AN[x]) pins and internal analog sensing (for example, VCCD) paths; as a result, the corresponding I/O power domain should have the same voltage level as VDDA_ADC.

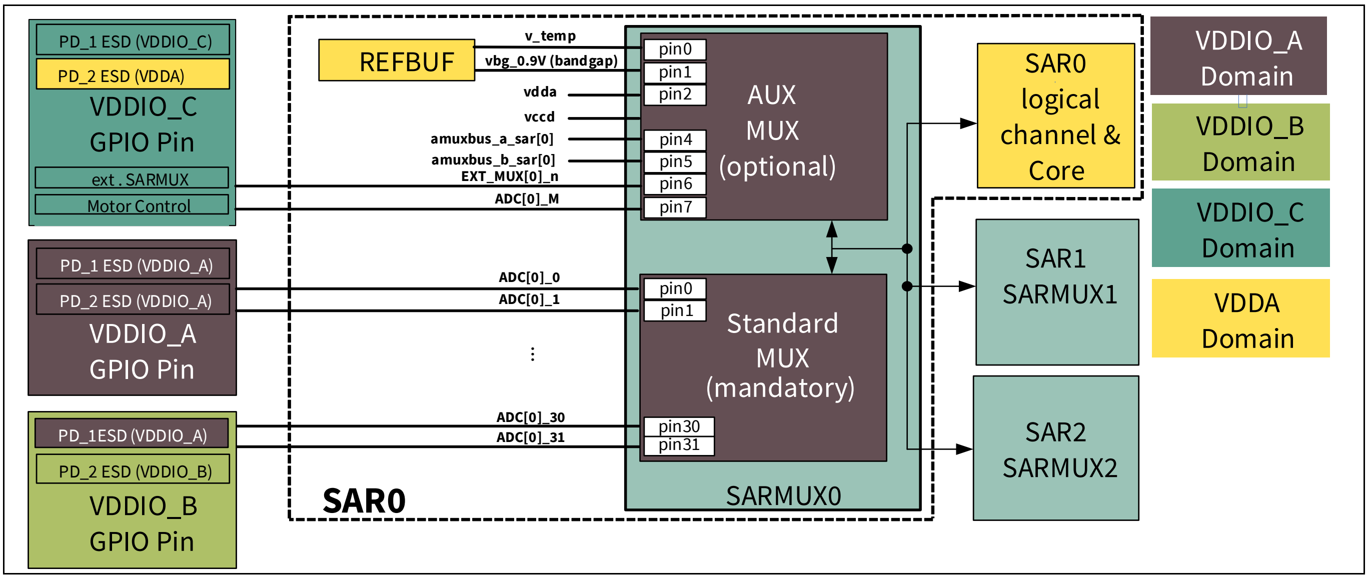


Figure 17 **Power domains**

General

- Usually the I/O domain, PD_1, deployed is also the same as PD_2, but in some cases there are exceptions for PD_2
- The power domain dependency PD_1 ≤ PD_2 is especially relevant when PD_1 is a different power domain when compared to PD_2
- When VDDA_ADC is only on PD_3 and if the pin input has not started to operate as an analog input, PD_1 and PD_2 can be greater than VDDA_ADC. See also Power ON/OFF sequence of power supply domains

Note: *The implementation of power rail voltage levels for the dedicated I/O domains and the ADC supply must be compliant with the other power sequencing requirements mentioned in the device datasheet.*
Also for the I/O power domain of each SARMUX must be taken care when analog function is used. The device datasheet explains which power domains supply to SARMUX; refer to the "Absolute Maximum Ratings", "Device-level specifications, or "Analog peripherals" sections. It is usually specified in the following manner: "VDDIO_1 must be greater than 0.8 × VDDA when ADC[0] is

enabled", that is, VDDD is the SARMUX0 I/O power domain."VDDIO_GPIO >= 0.8 x VDDA when SARMUX0 enabled".

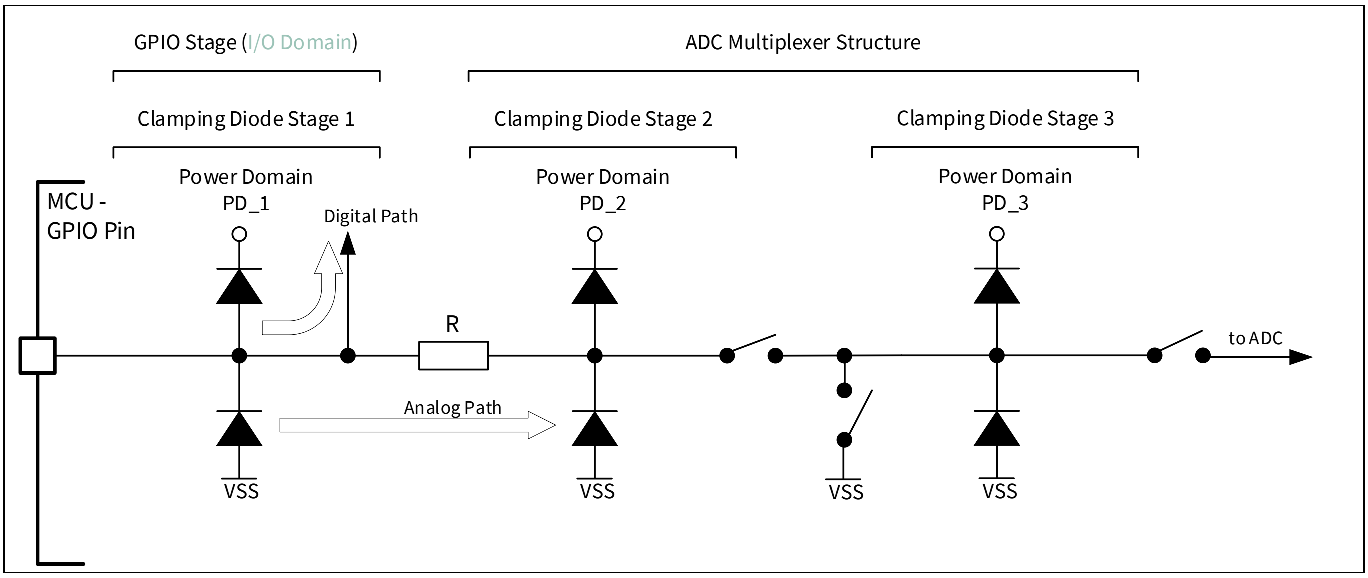


Figure 18 Clamping structure of I/O pins with shared analog functions

See Appendix G – Clamping structure of I/O pins with shared analog functions for device-specific information.

7.12 External supply for the core voltage

7.12.1 Requirements

- Applications with < 300 mA core current consumption can run with the MCU-internal LDO
- Applications with > 300 mA core current consumption need an external supply for the core voltage

For the technical requirements of the DC-DC Converter and details on how to use it, see AN226698 listed in Related documents.

Note: *In AN226698, DC-DC Converters are termed as PMIC, although only the core voltage regulation handling is considered.*

7.12.2 Drive output current of "Enable" control pin

To control the Enable (EN) input pin of the external DC-DC Converter, a dedicated output control pin on the MCU is available. Compared to a standard GPIO pin, the absolute maximum drive current is extremely limited. Therefore, for current limitation, a series resistor is necessary. Otherwise, this MCU control pin might be permanently damaged. For electrical specification, see the device datasheet in the Related documents.

8 Flash programming connection

Flash programming can be done with the JTAG/SWD connection. Due to this fact, no mode pins are available to switch the device into a programming mode after a power-on reset. See Debug interface for information on the debug connections. There is also the option to use dedicated LIN and the CAN channels for mass production programming as an integrated part of a Flash bootloader. For details, see AN227076 in Related documents.

9 Debug interface

There are several options to connect the debug system to the MCU depending on the debug requirements and the tool chain support. The following are the debug connectors:

- Legacy 20-pin IDC JTAG connector
- 10-pin Cortex® debug connector
- 20-pin Cortex® debug + ETM connector

In all these connectors, the JTAG and SWD signals are shared. The differences are indicated by marking the serial wire debug (SWD) protocol signals in blue. For more information on the interface signals, see Chapter 11 of the CoreSight Components Technical Reference Manual . A short overview is given in Table 4.

Note: For the power domain to which the Debug/Boundary Scan pins of each product belong, please refer to the following Appendix pages.
The power domains to which Debug/Boundary Scan pins belong of CYT2B series
The power domains to which Debug/Boundary Scan pins belong of CYT3B/4B/6B series
The power domains to which Debug/Boundary Scan pins belong of CYT3D series
The power domains to which Debug/Boundary Scan pins belong of CYT4E series
The power domains to which Debug/Boundary Scan pins belong of CYT4D series
The power domains to which Debug/Boundary Scan pins belong of CYT2C series

Table 4 Overview of SWD and JTAG interfaces

Item	JTAG	SWD
Pin count	4	2
Functionalities	Programming Debugging Boundary scan	Programming Debugging
Topology	Daisy-chained	Star
Extra features	N/A	Print out debug info

9.1 Legacy 20-pin IDC JTAG connector

The legacy JTAG interface is used for flash programming and debugging. The RTCK JTAG signal is not available on the MCU. Additionally, the SWD signals can be shared.

Note: The JTAG interface terminates in a 20-way, 2.54-mm-pitch IDC connector (for example, Hirose HIF3FC-20PA-2.54DSA).

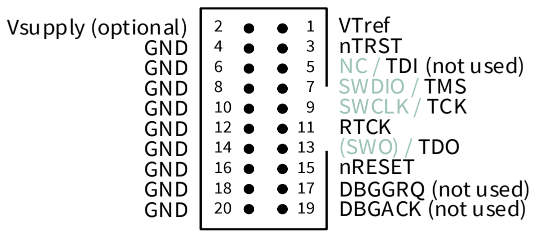


Figure 19 Legacy 20-pin IDC JTAG connector

9.2 10-pin Cortex® debug connector

To use the SWD debug interface, a 10-pin MIPI connector is defined with the minimum number of signals, which are required for debugging. The JTAG interface signals are replaced by the bidirectional data signal (SWDIO) and the clock signal (SWCLK). The freed-up TDO signal can be reused as a system trace data output serial wire output (SWO).

Note:

1. *For the SWD debugging a 10-way connector with 1.27-mm pitch is applied (for example, Samtech FTSH-105-01-L-DV-K)*
2. *Position 7 (KEY) has no pin and serves only as a key to properly orient the connector*

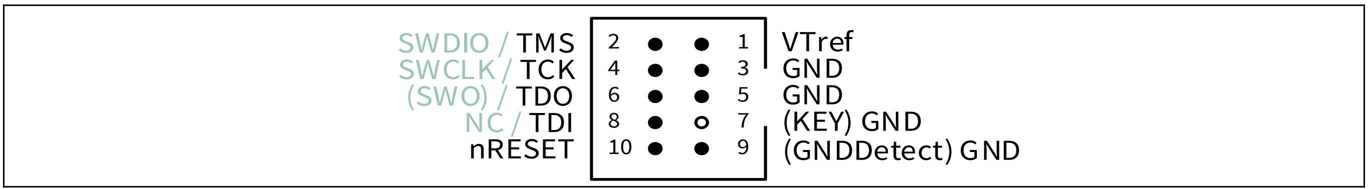


Figure 20 10-pin Cortex® debug connector

9.3 20-pin Cortex® debug + ETM connector

Beside JTAG debugging and SWD debugging, this connector is used to connect a signal trace probe for the embedded trace macrocell (ETM) instruction trace operations.

Note:

1. *As a connector, a 20-way 1.27-mm-pitch IDC-connector is applied (for example, Samtech FTSH-110-01-L-DV-K)*
2. *Position 7 (KEY) has no pin and serves only as a key to properly orient the connector*

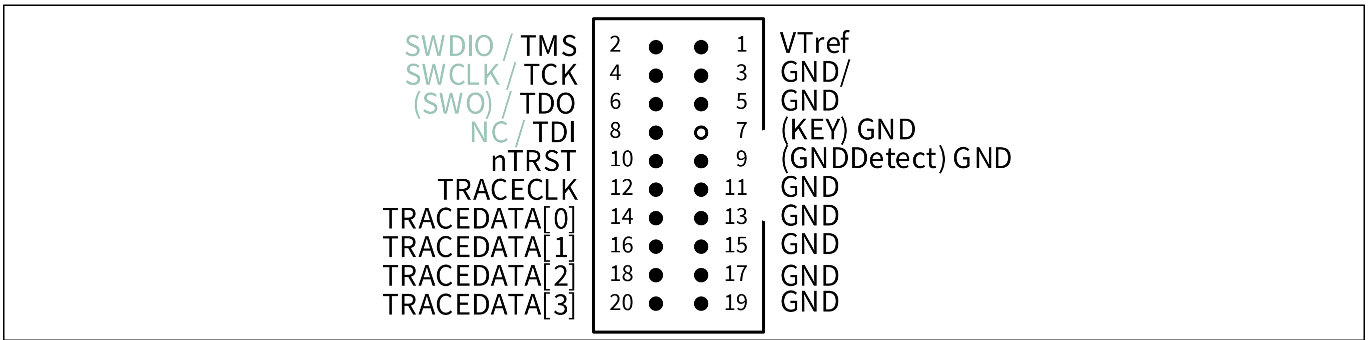


Figure 21 20-pin Cortex® debug + ETM connector

9.4 Termination resistors

In general, the debug connection needs termination resistors for a proper communication. External termination resistors should not be required for this MCU, because after POR, by default, the JTAG interface is enabled in the boot ROM. If externals are applied on the board, each external signal termination must be in the same direction as it is done in the device implementation. Although the JTAG interface is enabled by after reset, the SWD mode can be enabled afterward by establishing the SWD connection.

Table 5 Termination resistor for debug interface

JTAG mode	SWD mode	Signal	Required termination resistor (if N/A in the MCU)	MCU implementation
TCK	SWCLK	Clock into debug core	10 k–100 kΩ pull-down resistor to GND	Pull-down resistor
TDI	–	JTAG test data input	10 k–100 kΩ pull-up resistor to V_{DDIO}	Pull-up resistor
TDO	SWO (optional)	JTAG test data output, SWV trace data output	10 k–100 kΩ pull-up resistor to V_{DDIO}	None. Termination, push-pull driver implemented.
TMS	SWDIO	JTAG test mode select, SWD data in/out	10 k–100 kΩ pull-up resistor to V_{DDIO}	Pull-up resistor
nTRST	–	JTAG TAP reset (active LOW)	10 k–100 kΩ pull-up resistor to V_{DDIO}	Pull-up resistor
GND	GND	Connection to the system ground	–	–

Figure 22 and Figure 23 show how to connect the debug connector to the MCU. In general, it is recommended to place a series resistor (R16) closer to the connector to avoid reflections and ringing of the debug clock signal. Otherwise, with strong oscillations during level settlement, the debug interface can interpret the wrong data. It must be considered that due to the internal termination resistor, a possible voltage divider in the debug clock signal might be created.

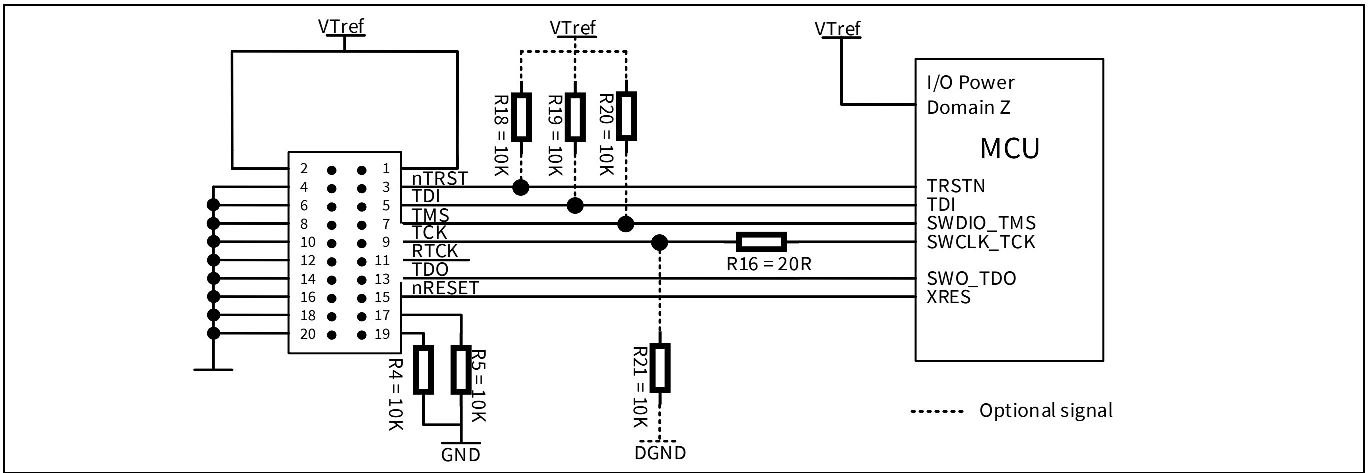


Figure 22 JTAG debug connection to the MCU with a 20-pin IDC connector

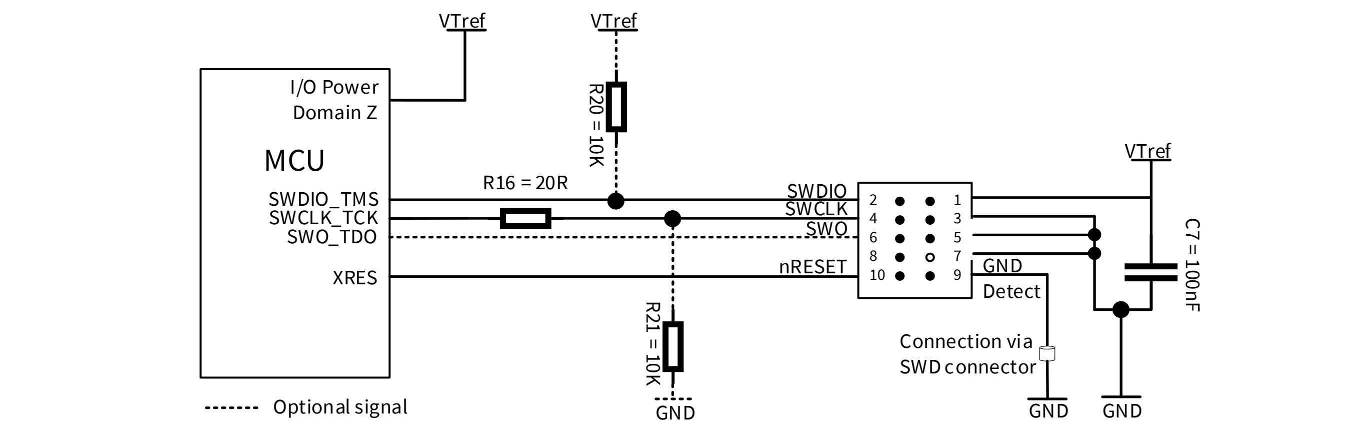


Figure 23 SWD debug connection to the MCU with 10-pin MIPI SWD debug connector

Note:

1. *When SWD is used as the debug interface instead of JTAG, there is a time slot after reset and in between boot ROM and user pin configuration in which unused JTAG pins are configured according to JTAG communication. When these unused JTAG pins are used in an application, make sure that the peripherals on the ECU are not negatively affected*
2. *Check the debug connection that is supported by the vendors for flash programming and debugging. Also, check for the target board supply and the supported power supply level of the vendor's hardware. In the case of a power supply mismatch, an adapter is required*
3. *Boundary-scan is supported only on the JTAG interface, not on SWD*

9.5 Trace width

The trace signals are identified by the function names `TRACE_DATA_x(0)` and `TRACE_DATA_x (1)`. The number in parentheses denotes the relocation set. Other than that, they are functionally identical. Nevertheless, you should only use the signals from the same relocation set; that is, only (0) signals or only (1) signals.

If all trace signals are not used, the ones with the higher numbers can be omitted. Your debugger tool should allow you to select the actual trace port width.

Possible trace width combinations

Trace signal	8-bit width	4-bit width	2-bit width
Variant A	TRACE_CLOCK (0) TRACE_DATA_0-7 (0)	TRACE_CLOCK (0) TRACE_DATA_0-3 (0)	TRACE_CLOCK (0) TRACE_DATA_0-1 (0)
Variant B	TRACE_CLOCK (1) TRACE_DATA_0-7 (1)	TRACE_CLOCK (1) TRACE_DATA_0-3 (1)	TRACE_CLOCK (1) TRACE_DATA_0-1 (1)

10 Clock output function

You might need to cross-check the MCU internal clock signals for evaluation purposes. You can cross-check with the following options:

- EXT_CLK port pin
- Alternate output function pin

10.1 Using the EXT_CLK port pin

Internal clocks can be routed through a divider to the alternate function port pin EXT_CLK as the clock output function. It must be taken into consideration that the event generator macro (EVTGEN) and EXT_CLK are driven by the same internal clock signal (CLK_HF1). Therefore, when the divided ECO signal should be observed at the EXT_CLK pin, the EVTGEN macro is also driven with the ECO clock accordingly. This may have an impact on the application. The EXT_CLK pin is a bidirectional pin and can also be used as an external clock source. See Clock system for more information about this pin.

As the MCU clock output functionality drives the fast digital signal, this signal must be routed far away from the analog input and the analog voltage reference signals.

10.2 Using the alternate function pin

The system clocks can be implicitly observed by using a PWM signal coming from a TCPWM output channel for instance. It must be taken into consideration that each TCPWM channel input clock is derived by a dedicated clock divider of the peripheral clock. See the “Clocking system” chapter in the TRM for details on the clock tree.

11 Layout and electromagnetic compatibility

11.1 General

To avoid ESD problems and noise emission of the system, consider some rules for the layout design.

The most critical point is the VCCD pin, as this is the connection to the internal supply for the MCU core. The required decoupling capacitors (decaps) must be placed as close as possible to this pin. Usually, a bigger buffer or bypass capacitor of µF range is added to the dedicated power domain to bypass the period of time until the capacitors are recharged again. Otherwise, decaps and finally the system fall below the power supply operating range.

As the MCU has different digital supply rails, route the power supply traces carefully. Route the supply traces in a star shape or as a digital plane in the middle layer. A digital ground plane in the middle layer or on the mounting side just under the MCU is recommended. Assemble the decoupling capacitors as near as possible to the related pins. If these capacitors are placed too far away, their functionality is diminished.

If possible, all decoupling capacitors should be placed on the same mounting side as the MCU. Alternatively, the decaps could be placed on the bottom layer below the paired power supply pins (for example, VDD/VSS pair).

The analog supply should be decoupled from the digital supply and a common-ground star point should be placed as far as possible from the MCU. In the hardware design, make sure that no latch-up effect between the digital and analog supply or between analog and digital ground can occur. Therefore, the impedance between the different VSS pins and between analog ground and analog reference input must be as low as possible.

11.2 Power supply pins

For proper operation of the MCU, decaps and bypass capacitors are needed for the power supply pins. See General regarding recommendations about the placement of the decaps.

11.3 Ground and power supply

For a multilayer PCB, the power supply rails and ground should be routed as a plane in the inner layers of the PCB. Considering a layer stack with several power supply planes, these planes should not overlap to avoid noise coupling.

Here are some recommendations for good EMC behavior:

- Use a multilayer PCB
- Use power supply planes (ground and power) in the inner layer of the PCB layer stack
- Place one or two decoupling capacitors close to each corresponding supply pin pair to reduce possible radiation
- Use capacitor groups to match the frequency behavior of power supply decoupling. The decoupling capacitors can have values between 1 nF and 10 µF
- Make sure that only one common star point connects analog and digital ground planes to each other. To have less noise on the analog part, place the star point far from the MCU and close to the voltage regulator capacitor, with respect to the electronic control unit (ECU) connector
- Make sure that the digital and analog planes do not overlap and interfere. Furthermore, there should be no signal plane between these planes
- Shield the analog input signals by the analog ground as much as possible

- Avoid ground loops
- Make sure that the supply traces with a layer changeover have at least two vias

Figure 24 shows an example of a bad PCB layer stack, as there might be crosstalk between different power supply planes. However, Figure 25 is an example of a well-designed PCB layer stack in which the analog and digital supply planes are separated in the common layer. Thus, the EMC behavior of the board is already improved.

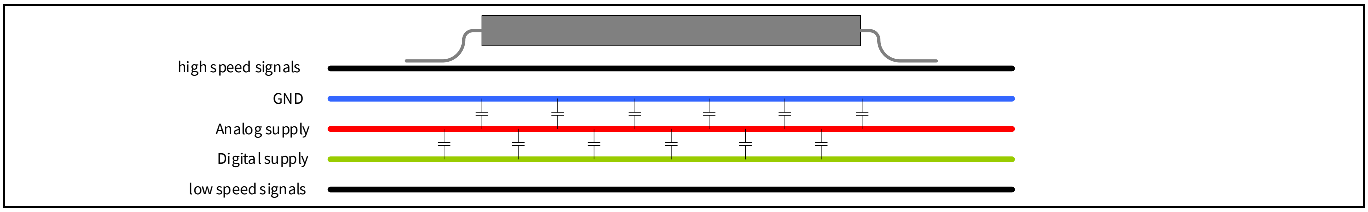


Figure 24 Example of a bad PCB layer stack

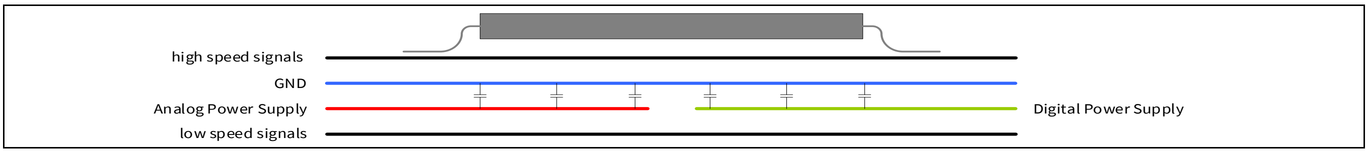


Figure 25 Example of a good PCB layer stack

11.4 Power supply decoupling

11.4.1 Placement

In general, the decaps should be placed as close as possible to the MCU. When a small ceramic capacitor is used together with a large electrolytic capacitor for decoupling, place the ceramic capacitor closer to the MCU power supply rail than the electrolytic capacitor.

Decaps for the power supply must be placed within the current flow. If not, they provide no benefit as their function becomes less efficient as shown in Figure 26. As the description is valid for generic use, as shown in Figure 26 to Figure 28, the generic naming convention for power supply pins is VCC; for ground pins, it is VSS.

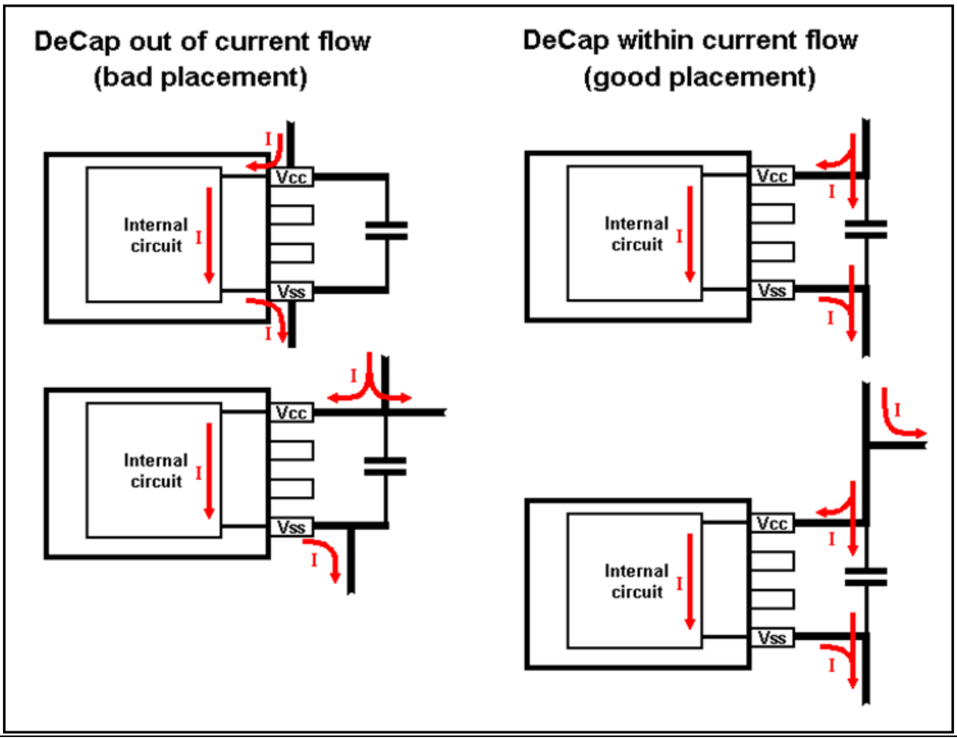


Figure 26 **Power supply decoupling capacitor placement**

Usually, the noise current should flow through the soldering pad of the decoupling capacitor CB. Figure 27 shows the recommended routing and placement on the boards.

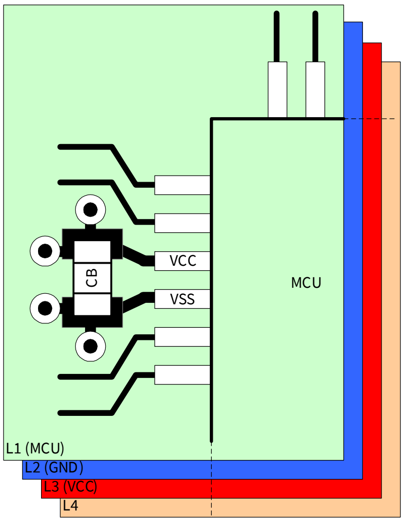


Figure 27 **Recommended power supply decoupling on boards**

Figure 28 shows an alternate but not recommended routing and placement. Note that the capacitor is placed on the opposite PCB side like the MCU. This solution works best for high-density board assembly.

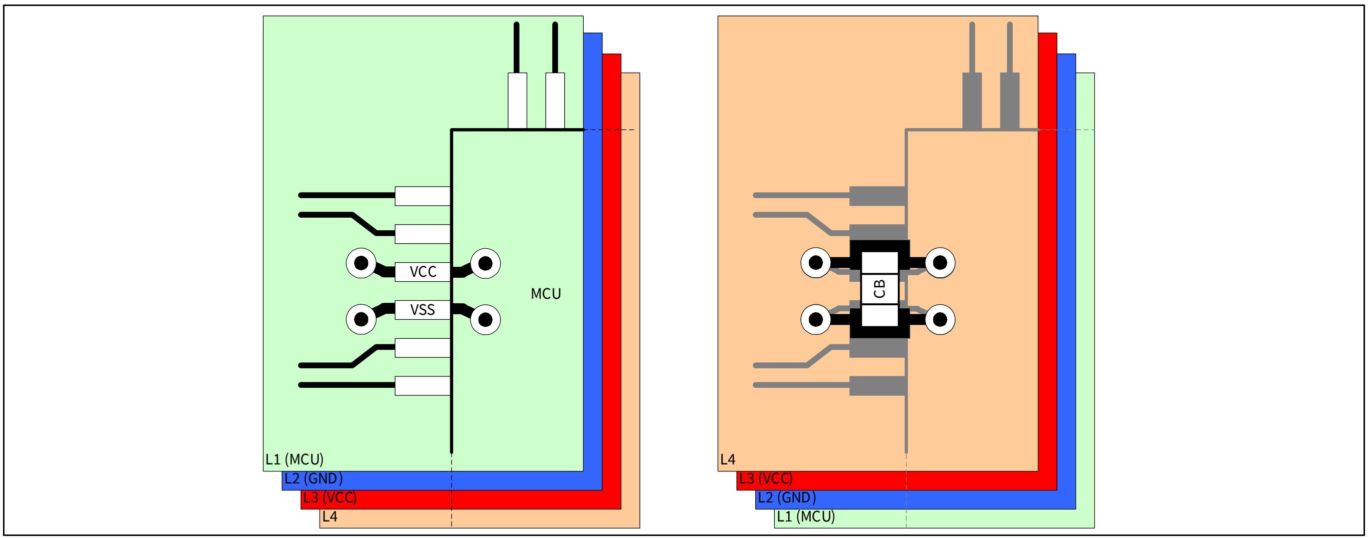


Figure 28 Alternate power supply decoupling on boards

11.4.2 I/O domains

The dimensioning of the decaps and bypass capacitors for the I/O domain is application specific. The following are some points to be considered while dimensioning:

- How is the switching behavior (periodic or random) of the output stages and what is the transition requirement?
- How many outputs have the same transition at the same time during the running operation or after any wakeup or reset?
- How big is the capacitive load at one output pin?
- Which driver strength configuration is selected?
- Is there any DC current caused by resistors, which might be also buffered by a big bypass capacitor?

It is strongly recommended to make either a power distribution network (PDN) analysis with an according model (IBIS or lumped model) or test on the PCB. A simplified consideration about the decoupling is provided in the SRAM board design guidelines.

11.5 Quartz crystal placement and signal routing

The MCU provides two Pierce oscillators implementations with an embedded feedback resistor (Rf) for the ECO and external watch oscillator (WCO). You can enable both oscillators by software. It means that the MCU starts the boot process from an internal clock source.

Note: *Figure 30 to Figure 32 show the implementation of oscillators in the MCU family and the trimming features discussed in this application note might differ from the dedicated device architecture TRM (see Related documents). Due to different trimming features, the external BOM cost can be reduced in the ECU design.*

11.5.1 Setup

Figure 29 shows the principle of an external oscillator circuit. The feedback resistor (Rf) is required to act is necessary for the inverter to act as an amplifier. Optionally, a damping resistor (Rd) is required for drive-level

(DL) reduction. If the DL is too strong, the crystal can be damaged over the lifetime. The load capacitance C_L is the terminal capacitance and is connected to the crystal. Thus, C_L includes the external capacitors C1 and C2 and the stray capacitance C_S. C_S comes from the PCB layout, manufacturing tolerances, and the oscillator MCU pins. As the stray capacitance is usually ~4 pF for each signal line, the value of both load capacitors (C1 and C2) should be determined with a crystal matching test. This test must always be done by the crystal manufacturer when there is any change on the target board affecting the oscillator circuit.

Load capacitance (C_L)

$$C_L = \frac{C1 \times C2}{C1 + C2} + C_S$$

Equation 2

Note:

1. *The oscillator pins are shared with standard GPIO pins, which automatically leads to additional load capacitance in the oscillator circuit. This must be considered with regards to external load capacitors*
2. *For details on crystal trimming, see AN230194*

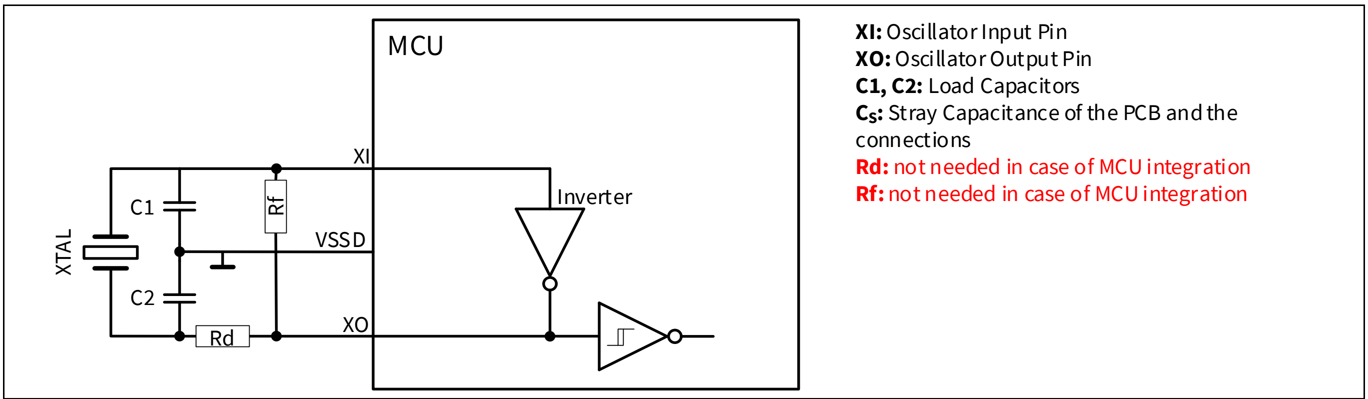
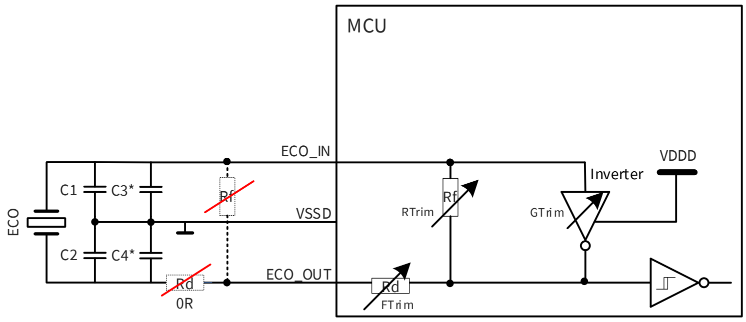


Figure 29 Standard setup of an external oscillator circuit (different from TRAVEO™ implementation)

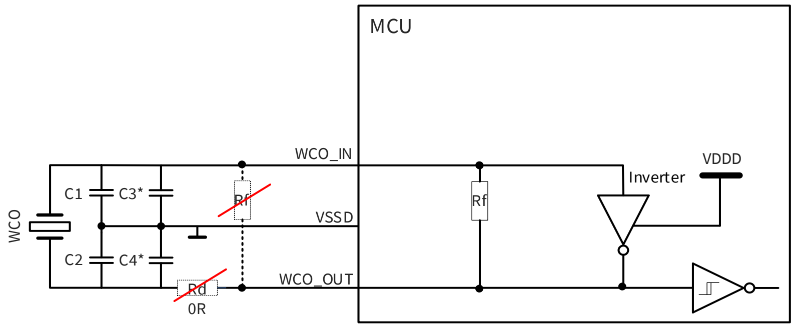
The ECO design is optimized for BOM cost reduction (see Figure 30). This is realized by a scalable DL and an embedded Rf implementation. By trimming features, a broad crystal frequency range can be supported. For details, see the “Clock sources” section in the architecture TRM listed in Related documents.



ECO_IN: External crystal oscillator input pin
ECO_OUT: External crystal oscillator output pin
C1, C2: Load Capacitors
C3*, C4*: Stray Capacitance of the PCB
Rd: external to be removed due to MCU integrated. Even no 0R needed as placeholder
Rf: external incl. path to be removed due to MCU integration

Figure 30 ECO circuit scheme[8] (main crystal oscillator)

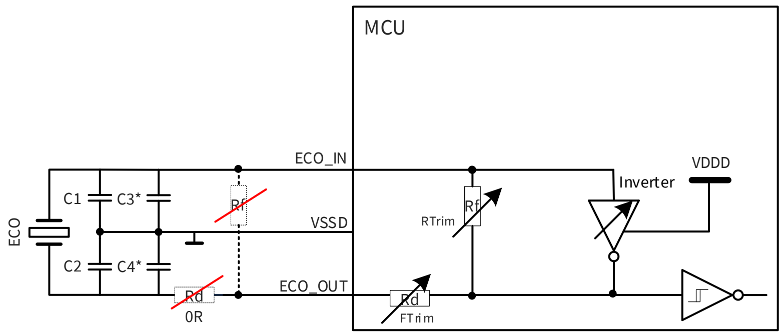
The WCO implementation scheme is shown in Figure 31. Like in the ECO, Rf is embedded to reduce the external BOM cost. An external Rd might be required to avoid damage of the external watch crystal.



WCO_IN: Watch crystal oscillator input pin
WCO_OUT: Watch crystal oscillator output pin
C1, C2: Load Capacitors
C3*, C4*: Stray Capacitance of the PCB
Rd: external to be removed. Even no 0R needed as placeholder
Rf: external incl. path to be removed due to MCU integration

Figure 31 WCO circuit scheme[8] (watch crystal oscillator)

The LPECO design is optimized for BOM cost reduction (see Figure 32). This is realized by a scalable DL and an embedded Rf implementation.



LPECO_IN: External crystal oscillator input pin
LPECO_OUT: External crystal oscillator output pin
C1, C2: Load Capacitors
C3*, C4*: Stray Capacitance of the PCB
Rd: external to be removed due to MCU integrated. Even no 0R needed as placeholder
Rf: external incl. path to be removed due to MCU integration

Figure 32 LPECO circuit scheme[8] (low-power main oscillator)

Table 6 shows the resulting external BOM based on the feature set in each oscillator implementation.

[8] Figure might differ from dedicated architecture TRM. Trimming features are not covered 100%.

Table 6 BOM overview of crystal oscillator implementations

Ext. component	ECO (main oscillator)	LPECO[9] (low-power main oscillator)	WCO (watch crystal oscillator)
XTAL	Mandatory	Mandatory	Mandatory
C1, C2	Mandatory	Mandatory	Mandatory
Rd[10]	Remove	Remove	Remove
Rf	Remove	Remove	Remove

11.5.2 PCB design

To reduce the impact of EMI, the placement of the external oscillator components and the signal routing must be done carefully. The following should be considered during PCB layouts. Due to design constraints, it might be required to make a tradeoff between the items.

- Stable frequency
  - Place the external oscillator components on the MCU layer
  - Place the external oscillator components as close as possible to the MCU
  - Make sure that the connection of load capacitors C1 and C2 to the oscillator ground is in a common star point
  - Make sure that there is no signal line between both the capacitor ground connections
  - Do not use vias for ground signal routing
- Noise injection
  - Use a ground layer directly below the MCU
  - Use a ground shield in the MCU layer and use the neighbor layer as the ground layer
  - Shield the area of oscillator bonding wires
  - Do not use the ground shield as the oscillator ground signal
  - Avoid ground loops. The oscillator ground signal must be connected at first to VSSD before connecting to the system ground
  - Make sure that the routing of the oscillator ground to VSSD is as short as possible
  - Do not route signals with strong pulses close to the oscillator. This is also valid for the neighbor layer

Connect the silent ground of the oscillator to the system ground after passing the silent VSSD MCU pin to ensure a stable current return path. So, the via to the system ground will be usually below the MCU package and not between the oscillator and the silent MCU VSSD pin. See Figure 60 as an example.

- Noise emission
  - Do not route sensitive signals close to the oscillator signals (example: analog sensor signals)

11.5.3 Crystal matching test

For each device package and ECU variant, a crystal matching test must be done by the crystal vendor. The oscillator MCU module must be configured according to the oscillator circuit. See AN230194 to learn how to configure the ECO module.

---

[9] Not available on each device. When available, then same pins might be shared with WCO.

[10] Rd not needed due to low power oscillator implementation

To reduce the iterations of matching activities between the customer and crystal vendor, a crystal matching test software is provided on demand. It can be directly used by the vendor to modify the preconfigured crystal setting from the customer for optimization. By default, a UART interface with a PC terminal is used. Due to the availability of the source code, another UART channel or even interface can be used.

11.6 Component placement

- Place analog components in such a way that the ground connection is on a common partition area. Do the same for digital components. Place the analog voltage reference regulator over the analog plane and the digital voltage regulator accordingly over the digital plane
- Components with a common power supply should be located as centrally as possible to each other
- Place the MCU and other mixed signal components on the PCB as a bridge between the analog and digital partitions

11.7 Signal routing

- Route the digital power and signal traces over the digital ground planes and route the analog power and signal traces over the analog ground plane
- To isolate analog signals traces, fill the areas around the traces that are connected to the analog ground plane with copper. Accordingly, the same recommendation is also valid for areas with digital signal traces
- Do not route traces near to or parallel to other noisy and sensitive traces
- Keep the trace lengths as short as possible

Furthermore, when designing an application, study the following areas to improve the EMC performance:

- Noisy signals, for example, signals with fast edge times
- Sensitive and high-impedance signals
- Signals that capture events, such as interrupts and strobe signals

12 Thermal considerations

Once an indication of the MCU total power requirement is known, it is very important to understand whether the system design can properly dissipate this power into the ambient air efficiently enough. This determines whether further action or significant heat sinking and PCB design choices are required.

The MCUs cover a wide range of products from very low power devices to MCUs with very fast complex logic requiring higher power needs. Under certain conditions, MCUs may dissipate more than 1 watt of power including the core, peripheral, and I/O currents. With a lot of power in a device, necessary steps must be considered to avoid it from overheating.

Before a design is finalized, a complete thermal review should be done. Items such as the amount of airflow through the system, nearby heat sources, and PCB construction should be reviewed. The examples given below are the first steps to determine whether the preliminary design objectives can be met by taking the equation.

Calculation of junction temperature

$$T_J = T_A + \Theta_{\mathrm{JA}} \times P_D$$

Equation 3

- **T_J:** Junction temperature
- **T_A:** Ambient temperature
- **Θ_{JA}:** Thermal resistance from junction to ambient
- **P_D:** Power dissipation

For a first-order approximation, first check the datasheet for the thermal resistance from junction to ambient (θ_{JA}) for the target device package. θ_{JA} is expressed in units of °C/watt. These values are estimated with a 2s2p PCB per JESD51-9.

For example, the θ_{JA} for an LQFP 120-pin is 38°C/watt. For the same device in an LQFP 120-pin package with an exposed pad on the bottom side correctly mounted, the θ_{JA} is reduced to 18°C/watt, allowing a much higher total device power usage or a higher ambient operating temperature.

The maximum temperature difference between the device junction and the ambient air surrounding the device is θ_{JA} times the maximum power, or as in the first case above, 38°C/watt x 1.0 watt = 38°C. Because the specified maximum operating junction temperature of the device is 125°C, the maximum allowable ambient air temperature is 125 – 38 = 87°C. If you use the exposed pad version of the package, which has a lower thermal resistance θ_{JA} of 18°C/watt if implemented with proper PCB to pad design, the maximum allowable ambient air temperature is 125°C – 18°C = 107°C. This allows a 20°C increase in ambient operating temperature or the possibility to drive more power from the device I/O or core.

Each datasheet for a device series contains a table showing package thermal resistance and maximum permissible power. This allows you to quickly see the amount of power that can practically be consumed by a device in a specific package. In the DS, a recommended minimal PCB construction might be given. So, for example, a four-layer PCB has a better power dissipation characteristic than a two-layer PCB, because the inner plane layers help to dissipate heat. Ensuring good contact between package-exposed pad and leads with copper pads on the PCB would improve the heat dissipation from the package to the PCB and improve the junction temperature.
The need to use airflow and other cooling solutions must be determined on each case with the customer's own simulations.

Note: *The datasheet specifications for Θ_{JA} are typical. The ambient air temperature should be much less than the allowable maximum for the product design.*

Note: *With the above calculation, if the Θ_{JA} or the power dissipated is high, the maximum allowable ambient air temperature could theoretically approach the 125°C junction temperature limit. However, the product's commercial-range ambient air temperature limit of 85°C or the industrial-range ambient air temperature limit of 105°C still applies. In the example above, the first example would be unacceptable for operating a consumer grade (85°C) device. In the second example, a consumer grade or industrial grade device would be well suited depending on the choice of operating conditions of the final product.*

MCUs offered in BGA or QFN packages have a reduced available surface area for thermal conduction. Due to the small package size; these packages must be thoroughly reviewed for power applications.

Detailed information is provided in the application notes AN72845, AN202751, and AN79938 listed in Related documents.

13 ADC

This section considers ADC and its analog input (AN) circuit for highly accurate sampling of the analog sensor level and other potential issues.

13.1 Filter design considerations for analog inputs

13.1.1 Principle of acquisition

The full period of sampling the analog value and then the conversion into a digital value is called acquisition time (t_{ACQ}). The voltage level of the analog input is sampled by an internal sample capacitor (C_{VIN}) within a configurable sample time (t_S); the conversion time (t_{CNV}) is implicitly configurable by the ADC clock input.

Figure 33 shows a principal circuit between the sensor, the analog source V_0, and the analog input.

$$t_{ACQ} = t_S + t_{CNV}$$

Equation 4

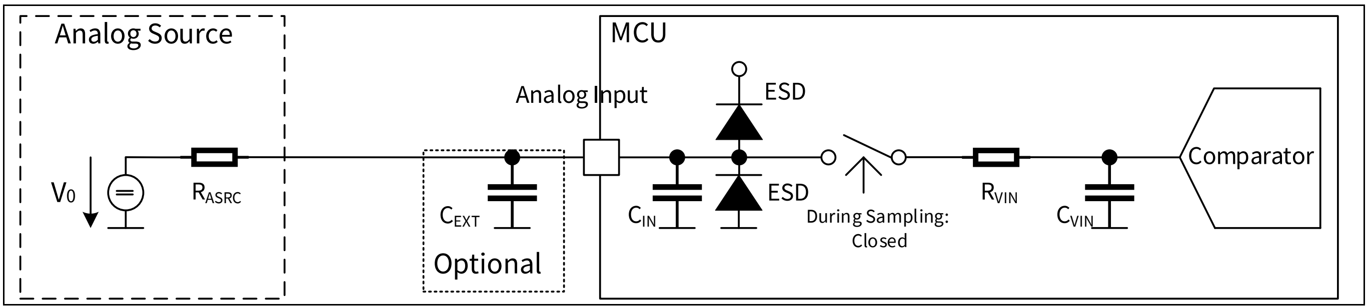


Figure 33 Analog input with optional external buffer capacitor

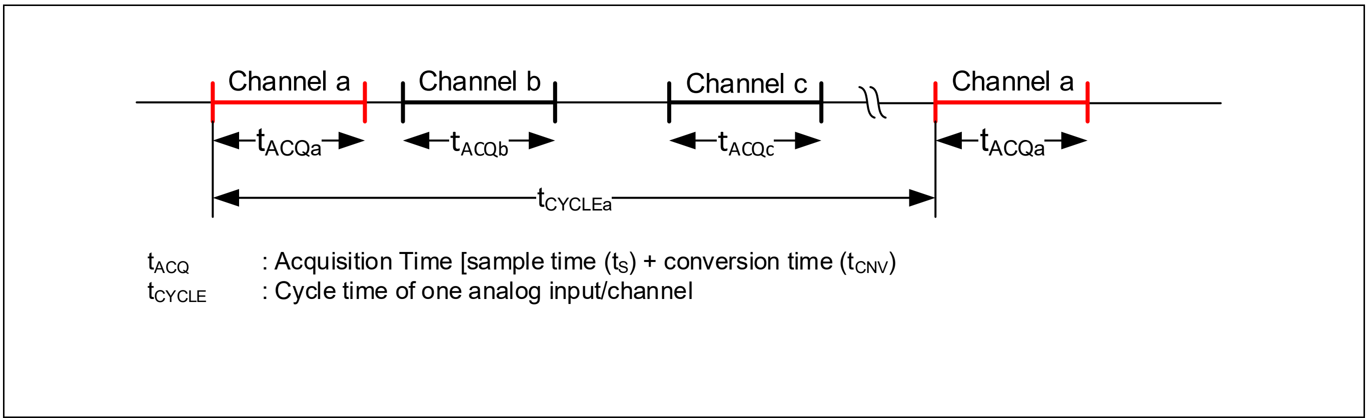


Figure 34 Cycle time of analog channels

13.1.2 Accuracy at sample time

The sample time (t_S) must be long enough for charging C_{VIN} at the same level as the analog source, which means that the internal resistance of the analog source (R_{ASRC}) should be small enough. When R_{ASRC} is too high, either the sample time must be longer, which has an impact on the total sample rate of all channels, or the cycle time

(t_{CYCLE}), the period between two acquisitions of a channel, must be longer accordingly (see Figure 33). After the cycle time, there should be either no or a neglectable voltage difference between the analog source V_0 and the analog input (AN) before the next acquisition. When a channel is sampled twice or more directly one after the other, the following equation must be fulfilled: $t_{CYCLE} \leq t_{ACQ}$.

The following are the assumptions to be considered while calculating the cycle time t_{CYCLE}:

- The analog input must be reloaded to a new source level, V_0, with a remaining voltage difference, V_R, depending on the required resolution 2^r. V_R should be smaller than the sampled error
- The reloading from the external capacitor C_{EXT} to the internal sample capacitor C_{VIN} during the sample time extends the cycle time

$$t_{CYCLE} = t_S + k \times \tau = t_S + ln\left(\frac{2^r}{V_{R,LSB}}\right) \times (R_{ASRC} \times (C_{EXT} + C_{IN}))$$

Equation 5

Example:

- **Resolution:** 12-bit
- **$V_{R,LSB}$:** 0.25 LSB = 0.25 x $(1/2^{12})$

$$t_{CYCLE} = t_S + k \times \tau = t_S + ln\left(\frac{2^{12}}{0.25}\right) \times (R_{ASRC} \times (C_{EXT} + C_{IN})) = t_S + 9.7 \times \tau$$

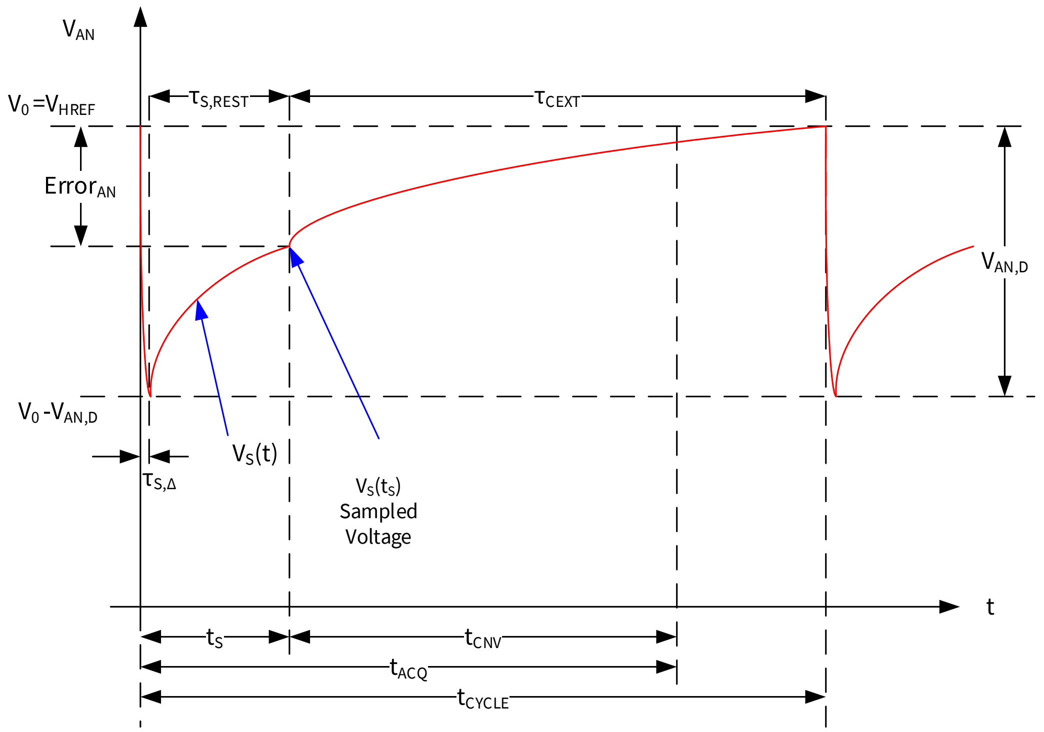
Equation 6

13.1.3 Sample time charging process

During the sample phase, the sample capacitor CVIN is charged by the external capacitor CEXT until both reach a common voltage (charge balancing). After that, both capacitors are charged to the analog source level V_0 via the source resistance.

So, different time constants must be considered:

- **$T_{S,\Delta}$:** Time constant at the beginning of the sample time for the charge balancing between C_{EXT} and C_{VIN}
- **$T_{S,REST}$:** Time constant during the sample time, after charge balancing, to charge close to V_0 with an acceptable error
- **T_{CEXT}:** Time constant, starting from the conversion time and ending with the next sample phase of the analog input



t_s : Sample time (t_S)
t_{ACQ} : Acquisition time
t_{CYCLE} : Cycle time of one analog input/channel
$\tau_{S,D}$: Time constant for the charge balancing between C_{EXT} and C_{VIN} causing a voltage drop during sample time
$\tau_{S,REST}$: Time constant for charging C_{EXT} and C_{VIN} by analog source V_0 for the rest of the sample time
τ_{CEXT} : Time constant for C_{EXT} only after sample time
V_0 : Voltage of the analog source
$V_S(t)$: Voltage level at analog input during sample time
t_{CNV} : Conversion time
$V_{AN,D}$: Voltage drop caused at analog input due to the charge balancing during the sample time
$Error_{AN}$: Voltage error between sample voltage and analog source voltage level

Figure 35 Charging curve of the analog input during acquisition time

13.1.4 Charge balancing between C_{EXT} and C_{VIN}

Depending on the ADC macro implementation, the sample capacitor can be precharged to a target level ($C_{VIN, PRE}$) before starting the sample phase. If this feature is not deployed, C_{VIN} will have the voltage level of the previous acquisition, which means that in the worst case, the maximum voltage difference ($\Delta V_{CVIN, PRE}$) between C_{VIN} and the external capacitor C_{EXT} corresponds to the analog reference voltage V_{REFH}. When the sample switch is closed, charge balancing between the external capacitor C_{EXT} and the sample capacitor C_{VIN} causes a voltage drop at the analog input $V_{AN, D}$.

$$V_{AN,D} = \frac{Q_{VIN}}{(C_{IN}+C_{EXT})+C_{VIN}} = \frac{C_{VIN}\times(V_0-V_{VIN,PRE})}{(C_{IN}+C_{EXT})+C_{VIN}} = \frac{C_{VIN}\times\Delta V_{VIN,PRE}}{(C_{IN}+C_{EXT})+C_{VIN}}$$

Equation 7

In a simplified consideration of the analog input and the analog source have the same voltage level $V_{AN} = V_0$, resulting in:

$$V_{AN,D} = \frac{Q_{VIN}}{(C_{IN}+C_{EXT})+C_{VIN}} = \frac{C_{VIN}\times(V_0-V_{VIN,PRE})}{(C_{IN}+C_{EXT})+C_{VIN}}$$

Equation 8

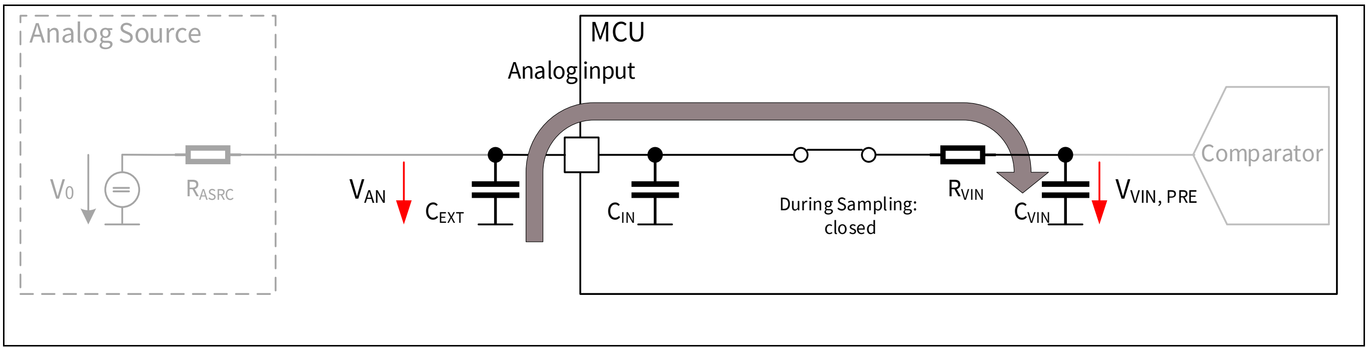


Figure 36 **Charge balancing during ADC sample time**

While this charge balancing happens, it is assumed that R_{ASRC} >> $R_{VIN,}$ and therefore R_{ASRC} has no impact during that phase. This results in the following time constant $\tau_{S,\Delta}$ for charging the capacitor:

$$\tau_{S,D} = R_{VIN} \times C_{SUM} = R_{VIN} \times \left(\frac{1}{1/(C_{EXT}+C_{IN})+1/C_{VIN}}\right)$$

Equation 9

Thus, in the worst-case scenario for the maximum voltage difference between the analog input and the sample capacitor after 9.7*$\tau_{S,D}$, the voltage error of the analog input is less than 0.25 LSB_{12}.

13.1.5 Charging the analog input by the analog source V_0

Depending on the dimensioning of the external capacitor C_{EXT}, charge balancing between C_{EXT} and C_{VIN} causes a huge voltage difference in the analog input in relation to the analog source V_0. The analog input must be charged by V_0 itself directly. In this case, the analog source resistance R_{ASRC} has a relevant influence for the charging curve.

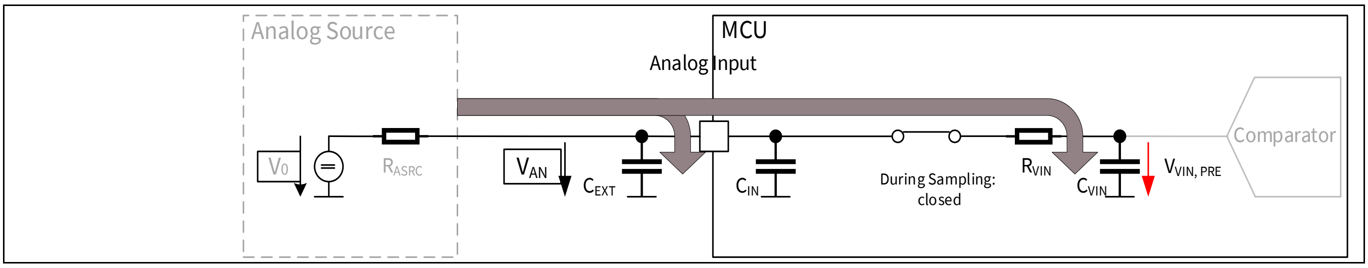


Figure 37 Charging of the analog input during the sample time by the analog source V_0

Thus, for the rest of the sample time, the time constant $\tau_{S,REST}$ is calculated as follows:

$$\tau_{S,REST} = (R_{VIN} + R_{ARSC}) \times C_{VIN} + R_{ARSC} \times (C_{EXT} + C_{IN})$$

Equation 10

13.1.6 Filter case: $C_{EXT} > 2^r * C_{VIN}$

When the analog source impedance is too high, the sampling period for analog voltages may be insufficient, especially when all analog input needs to be sampled with a common high sample rate (for example, 1 MS/s). If the cyclic sampling of the dedicated analog input, the cycle time (t_{CYCLE}), can be much longer, a big external buffer capacitor C_{EXT} can be deployed. The dimensioning considers the maximal target error at the sampled analog input $Error_{AN}$.

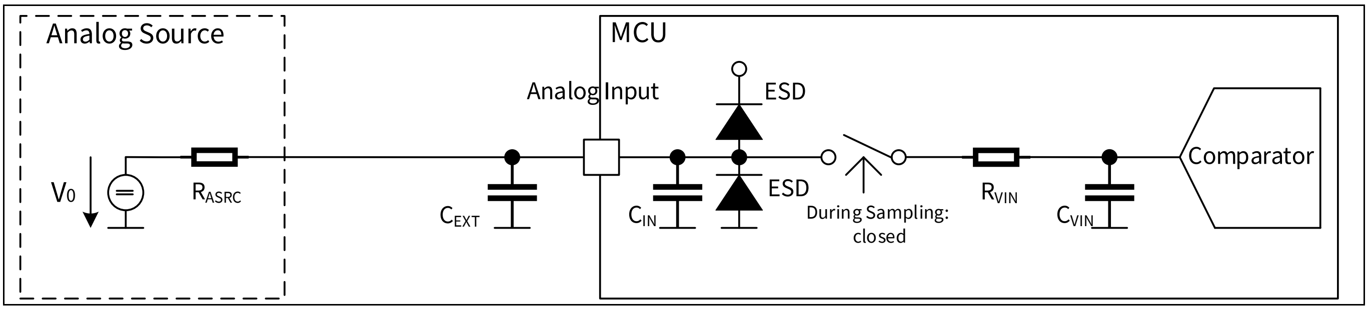


Figure 38 Analog input with decoupling capacitor against internal switching noise

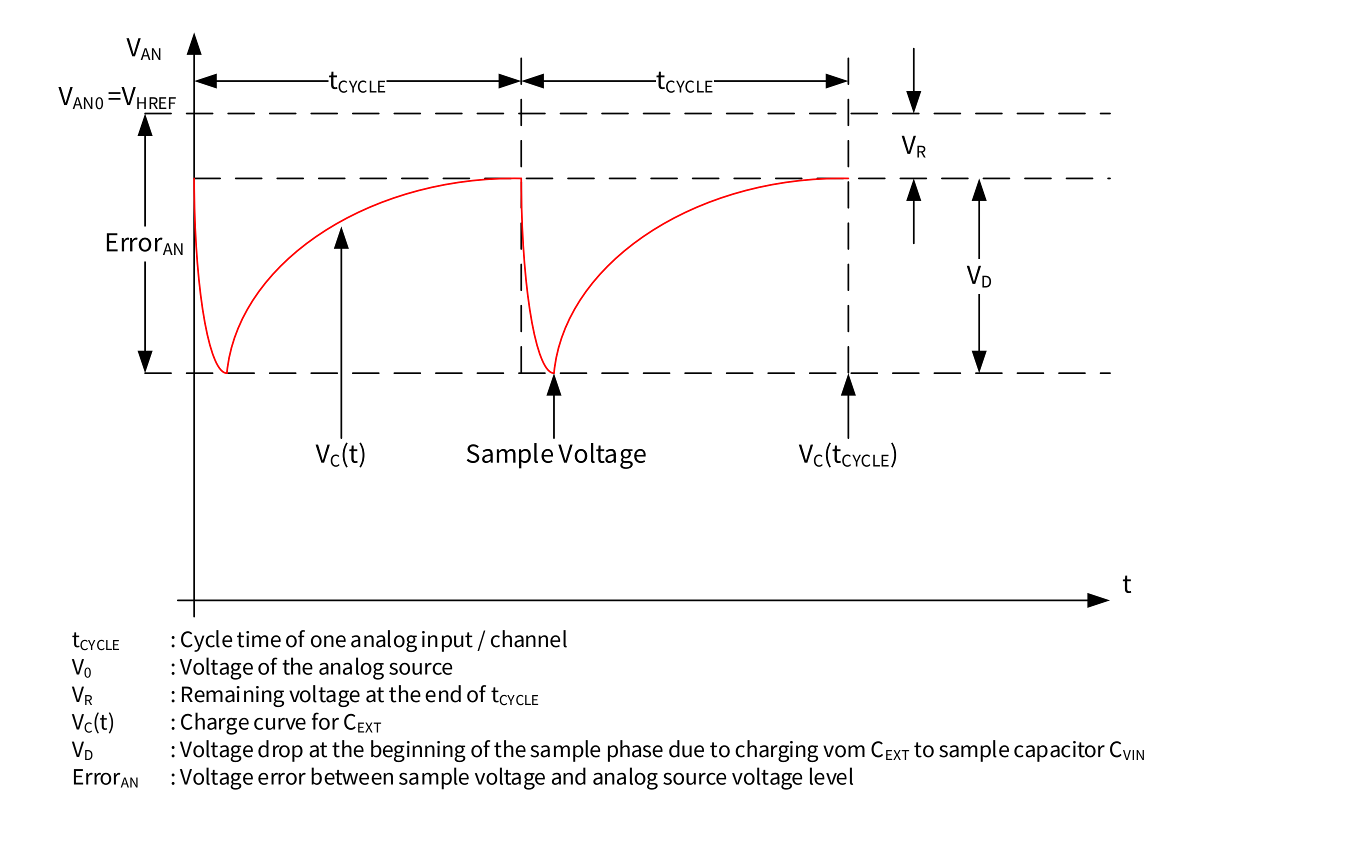


Figure 39 Simplified cyclic charge Curve of C_{EXT} for use case C_{EXT} > 2r * C_{VIN}

At first, the maximum permitted error $Error_{AN}$ must be defined as shown in:

$$Error_{AN} = 1/2^{E} \times LSB_{r}$$

Equation 11

With:

r = 12: 12-bit resolution E = 0; ErrorAN = 1 LSBr/4/2

r = 12: 12-bit resolution E = 1; ErrorAN = LSBr/2

r = 12: 12-bit resolution E = 2; ErrorAN = LSBr/4

$$C_{EXT} = 2^{r+E} \times C_{VIN}$$

Equation 12

To achieve a sampling error of less than 0.25 LSB (E = 2) at 12-bit resolution (r = 12), the minimum external filter capacitor C_{EXT} is as shown in:

$$C_{EXT,0.25LSB} \geq 2^{r+E} \times C_{VIN} = 2^{12+2} \times C_{VIN}$$

Equation 13

Due to the selection of $C_{EXT} > 2^r * C_{VIN,}$ the sample time t_S can be selected independently of the analog source R_{ASRC}. Nevertheless, R_{ASRC} has a direct impact to the cycle time t_{CYCLE}.

13.1.7 Discrete RC filter

If an extended sample time is insufficient to filter the noise on the analog signal input, you can use an external low-pass filter (RC filter) to the analog input pin (see Figure 40). Cross-check the possible sample period with the cut-off frequency of the RC filter. Furthermore, the voltage drop at R_{EXT} due to the complete leakage current of the analog input must not be higher than the required accuracy of the measured analog signal.

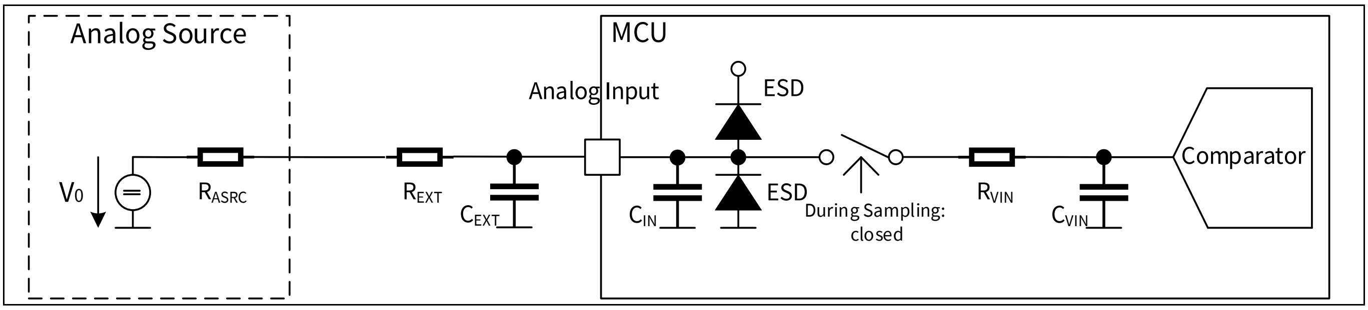


Figure 40 Analog input with low-pass filter

14 Assembly and package-related PCB design

The application notes AN202751 and AN79938 provided guidelines on surface mount assembly for different BGA packages, related PCB design, surface mount process flow, and final joint inspection methods.

15 Video interface

15.1 FPD-link

15.1.1 Signal pin configuration

The FPD differential data output signal pairs FPDx_TyP/N can be freely configured. This provides the advantage of avoiding signal pair crossing by changing the PCB layers for signal routing to the display connector. However, the FPD clock signal pair is on fixed pins.

15.1.2 Power domain VDD_PLL

The PLL power domain, VDD_PLL, of the FPD-Link is very noise sensitive, which can result in erroneous FPD-Link communication due to jitter. Thus, the following countermeasures are required to fulfill a silent power supply input:

- External filter
- Nearby signals that do not cause crosstalk (for example, I/O signals)

Note: *In the CYT3DL 216-TEQFP package, when in parallel, FPD-Link and port pins P.16.5 and P16.6 are used. Both pins must be only for noiseless I/O function (for example, a control signal with low driver strength).*

15.1.3 Unused port pin handling

See Dedicated port pins.

15.1.4 Unused power domain handling

See Unused power domains for generic information, and then refer to the device-specific information in the appendix.

15.2 The PLL power RGB interface

15.2.1 Signal pin configuration

As the pin names of the RGB interface are not 100% clear about the functional assignment, Figure 41 shows the flexibility in functional assignment for the bypass mode, the "standard" GPU display mode. In the following sections, the signal group routing is described.

Pixel clock: The pixel clock is routed directly to the TTL_DSPx_CLOCK pins.

Frame timing signals (HSYNC, VSYNC, DE): Each signal is routed through the signal generator of the GPU to several TTL_DISPx_CONTROL[y] pins. This provides additional flexibility and is the recommended for approach for the functional pin assignment.

If instead of 24-bit RGB only 18-bit RGB is in use, it is also possible to map the control signals via the map bit (MB) MUXer to one of the TTL_DISPx_DATA0/1[y] pins. This option is only available, because the MB MUXer is responsible for the bit mapping of all RGB signals for FPD-Link, which is not part of this chapter.

RGB color signals: The color signals can be routed freely to TTL_DISPx_DATA0/1[y]. This flexible pin assignment provides the chance to avoid signal crossing on the PCB to the display connector.

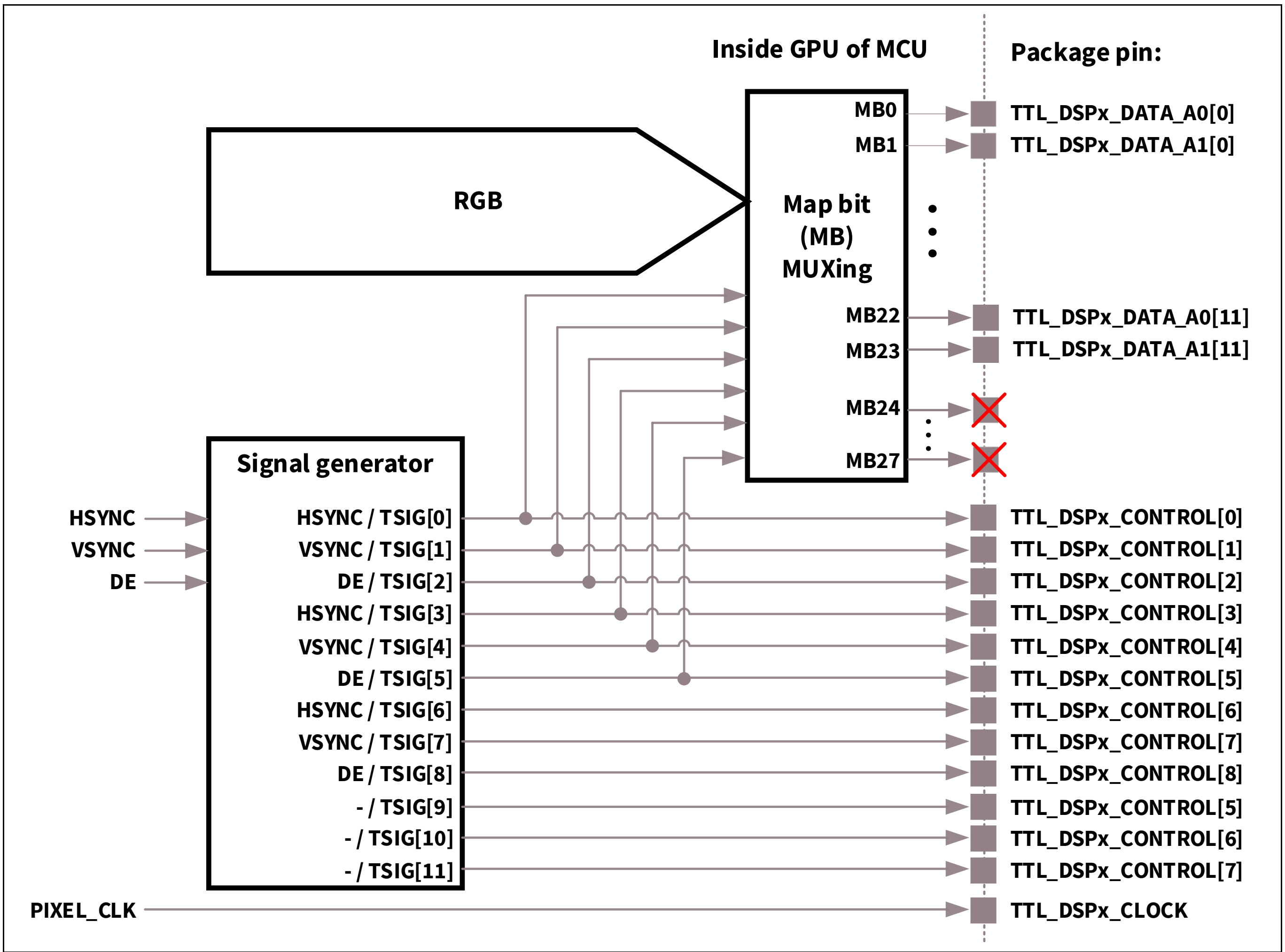


Figure 41 **Internal RGB signal routing from GPU to package pins**

15.3 MIPI

15.3.1 Signal pin configuration

The function of MIPI pins does not need to be explicitly configured like on standard GPIO pins, because these pins are dedicated to MIPI. Therefore, this is done implicitly by MIPI itself.

MIPI_REXT: Connect an external 15 kΩ 1% pull-down resistor to the MIPI_REXT pin.

Termination: Use the internal 100 Ω -20/+25% termination resistor and then use the calibration feature.

15.3.2 Unused port pin handling

See Dedicated port pins.

15.3.3 Unused power domain handling

See Unused power domains for generic information and then refer to the device-specific information in the appendix.

16 Audio-DAC

16.1.1 Implementation and features

The audio digital-to-analog converter (DAC) is an analog audio block inside the MCU and supports internal CIC filter, FIR filter, interpolation filter, and delta-sigma modulator for 10-bit resolution. Both OUT signals (DAC_L and DAC_R) are intended to connect with an external audio amplifier with an external output load resistance > 20 kΩ and load capacitance < 100 pF.

The DAC block consists of several internal power domains. The cut-off frequency of the third-order low-pass filter is 90 kHz. The noise-critical circuitry of the DAC is the analog part VDDA. The DC bias output voltage is determined by the internal voltage divider 131.6k/131.6k and an external smoothing capacitor at the COM pin (C_{COM}), shown below.

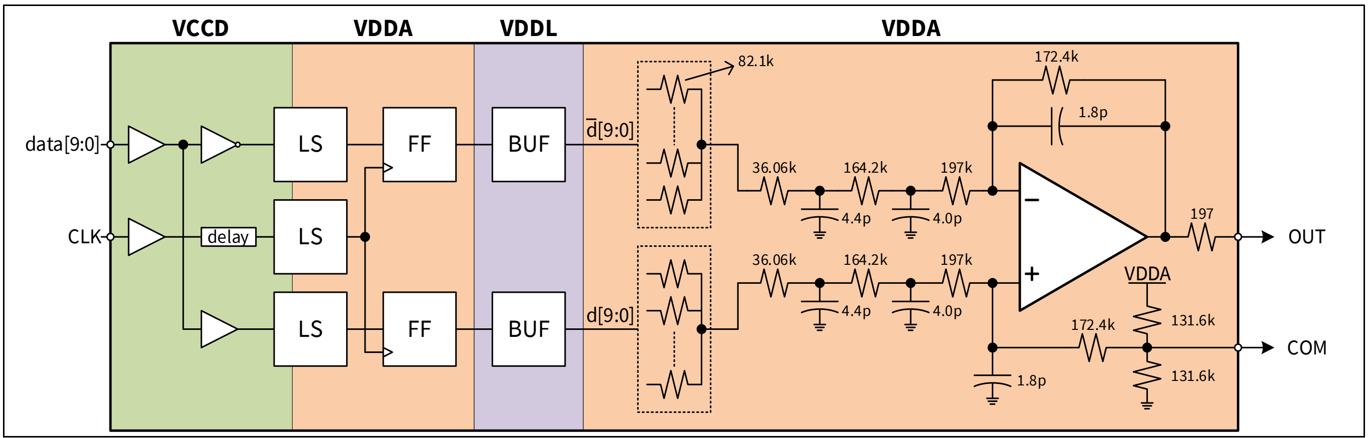


Figure 42 Block diagram of the audio-DAC output

As Figure 43 shows, the startup time depends on the selected smoothing capacitor (C_{COM}) value and should be configured with the integrated fast startup timer to 70 ms at 2.2 µF (low ESR). If a capacitor larger than 2.2 µF is needed, adjust the timer setting for the *FastRampCount* period and the *CompRampCount* period based on this reference value from the datasheet.

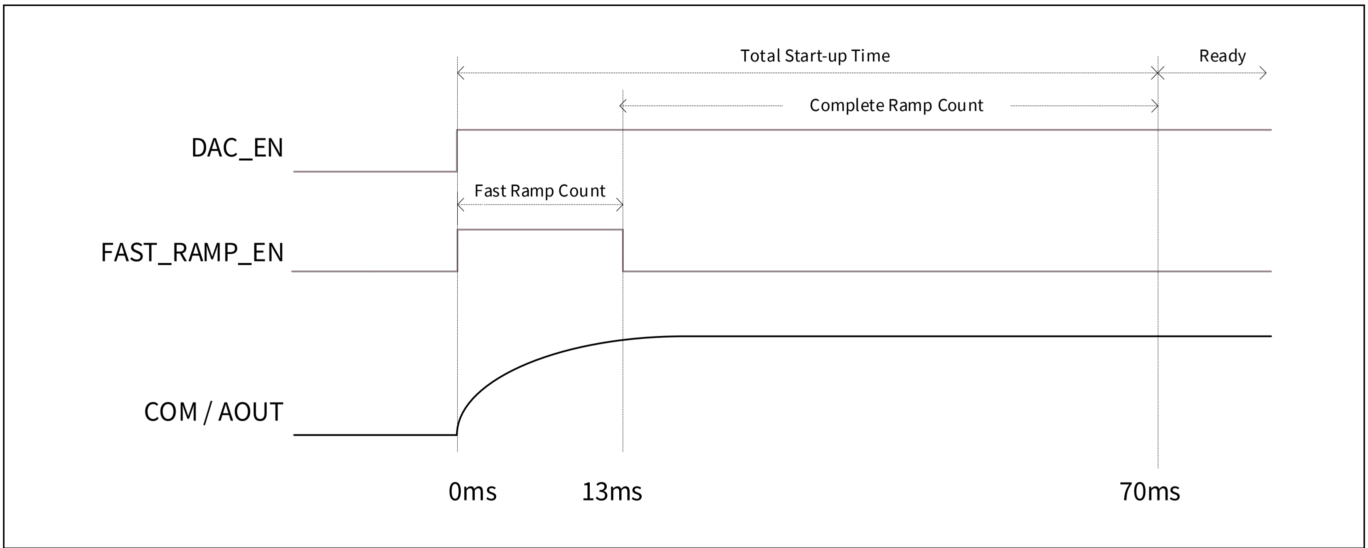


Figure 43 Audio-DAC startup time

During the audio-DAC startup time, the external amplifier must be either powered down or in mute mode (if mute mode is available). The typical COM capacitor value is 2.2 µF. For the typical case, the fast startup timer must be set to 13 ms to ensure that the audio-DAC is ready in 70 ms. The maximum supported COM capacitor is 10 µF. For this case, the fast startup timer must be set to 60 ms. Figure 43 shows the relationship between DAC_EN, FAST_RAMP_EN, and how the COM output behaves during startup.

16.1.2 Power domain filter

The analog block of the Audio-DAC, which corresponds to the internal VDDA block in Figure 42, is very noise-sensitive. Each noise on its supply can be heard directly on the audio output. Therefore, either of the following possibilities is recommended to create a silent supply at the VDDA_DAC/VSSA_DAC power domain pins:

- LDO linear regulator
- Low-pass filter (LPF) for the 3.3 V supply

If using a common 3.3-V supply for digital and analog parts of the application, it is necessary to consider the potential noise sources as listed in Table 7. In this case, a power supply filter in Figure 44 is recommended for the 3V3 audio power domain.

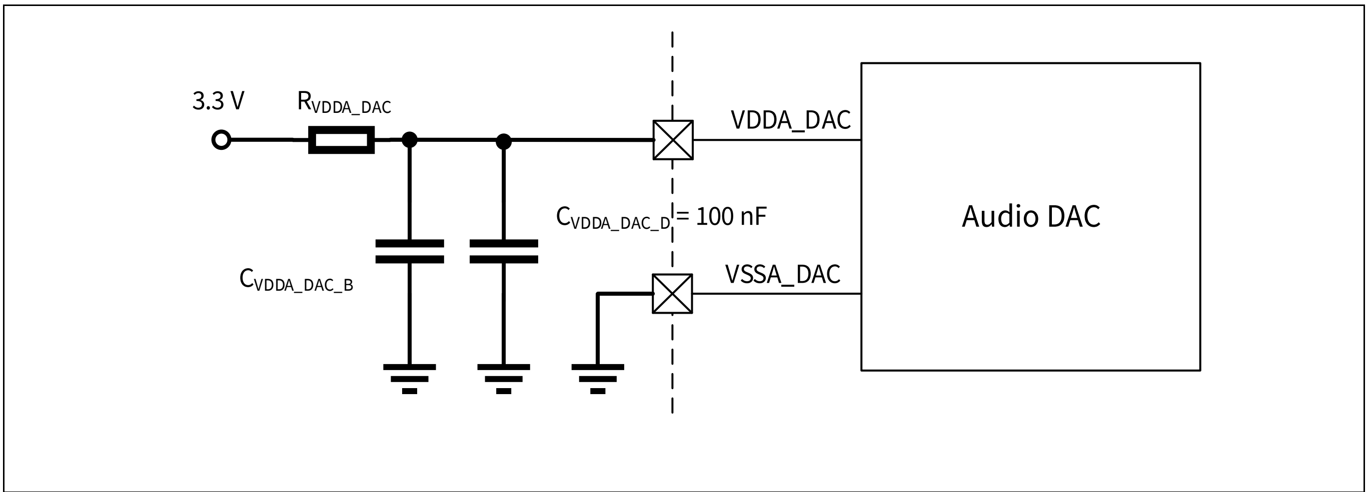


Figure 44 Power supply filter (LPF) for audio-DAC

Table 7 Potential noise sources on 3V3 audio power domain

Domain	Frequency range	Comment
Audio	100 Hz ... 20 kHz	Audio
DC-DC converter (switching regulator)	300 kHz ... 2.2 MHz	Switching frequency
	< 100 kHz	Response time
FPD-Link (I/O domain)	32 MHz … 110 MHz	Bus speed; equivalent frequency range of transitions are not considered
Memory interface	50 MHz … 133 MHz	
Ethernet	50 MHz … 125 MHz	
Communication interface	1 MHz … 10 MHz	

16.1.2.1 Low-pass filter calculation

The following diagram shows a simple RC LPF for the power supply of the audio-DAC, which is the responsibility of the user.

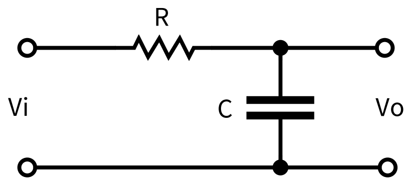


Figure 45 RC low-pass filter (RC LPF)

The cut-off frequency of the filter can be calculated by the following equation:

$$a = \frac{Vi}{Vo} = \frac{1}{\sqrt{1+(2\pi f RC)^2}}$$

$$fc = \frac{1}{2\pi RC}$$

Equation 14

Note: RC-filter −6 dB per octave corresponds to 20 dB per decade.

The following equation shows an example calculation for the RC-low-pass filter:

$$fc(-3\ dB) = \frac{1}{2\pi * 10\ \Omega * 10\ uF} = \ 1.592\ \text{kHz}$$

Equation 15

The following table shows the calculated cut-off frequency of LPF. Default values: C =2.2 µF and R = 10 Ω.

Table 8 LPF cut-off frequency

R[Ω]	10	1	0.3
C[µF]	f3dB[kHz]	f3dB[kHz]	f3dB[kHz]
10	1.59	15.9	53.1
4.7	3.39	33.9	112.9
2.2	7.2	72.3	241.1
1	15.92	159.2	530.5
0.47	33.96	338.6	1128.8
0.22	72.34	723.4	2411.4
0.1	159.15	1591.5	5305.2

There is an estimated IR drop on the power domain pin, VDDA DC, as shown in the following table, due to the series resistor (Rfilter). The reduction of the series resistor (Rfilter) of the LPF impacts the cut-off frequency. As an alternate for the resistor, a ferrite bead with Rdc ≤ 300 mΩ is recommended. See the example in Table 34.

Table 9 LPF DC-power power drop estimation

IDD[mA] (SID1318)	R[Ω]	Vdc[mV]
3.2	10	32
	4.7	15.04
	2.2	7.04
	1	3.2
	0.8	2.56
	0.5	1.6
	0.3	0.96
	0.1	0.32

Note: *In the application, to connect to the speakers, small series capacitors are added to the output pins DAC_L/R, as shown in Figure 47. This HW setup is not in contradiction to the parameters RL and CL of SID1300 (see the following table). These parameters belong to the test circuit as shown in Figure 46.*

Note: *For the correct values, see the device datasheet.*

Table 10 Audio-DAC output load and C_{COM} specification

SID1300	**f_{CLKDAO}**	**System clock frequency**	**2.048**	**–**	**18.432**	**MHz**	**All parameters specified f_S = 44.1 kHz, system clock 256 x f_S and 16-bit data, R_L = 20 kΩ, CL = 100 pF, unless otherwise noted**
SID1301	f_S	Sampling clock	8	–	48	kHz	–
SID1302	R_L	Analog output load resistance	20	–	–	kΩ	DAC_L, DAC_R
SID1303	C_L	Analog output load capacitance	–	–	100	pF	DAC_L, DAC_R
SID1304	C_{COM}	Com Capacitance	2.2	–	10	µF	C_L, C_R
SID1305	V_{OUT_MAX}	Analog outputsingle-end output range (±full scale)	0.655 x V_{DDA_DAC}	0.673 x V_{DDA_DAC}	0.690 x V_{DDA_DAC}	V_{P-P}	DAC_L, DAC_R, RL = 20 kΩ, CL = 100 pF
SID1306	V_{OUT_ZERO}	Analog output voltage (zero)	0.49 x V_{DDA_DAC}	0.5 x V_{DDA_DAC}	0.51 x V_{DDA_DAC}	V	DAC_L, DAC_R

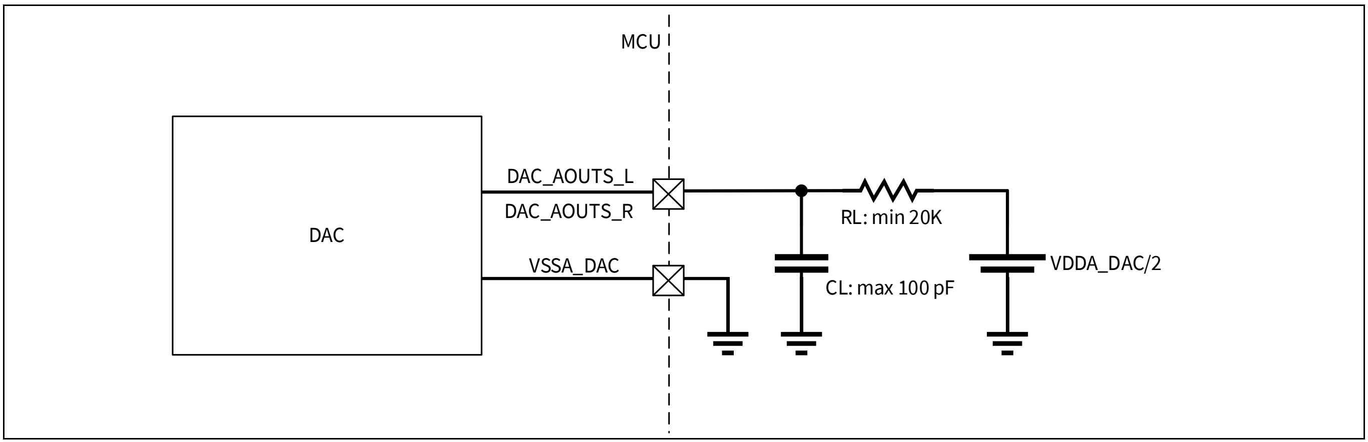


Figure 46 **DC coupling connected to VDDA_DAC/2 (test circuit)**

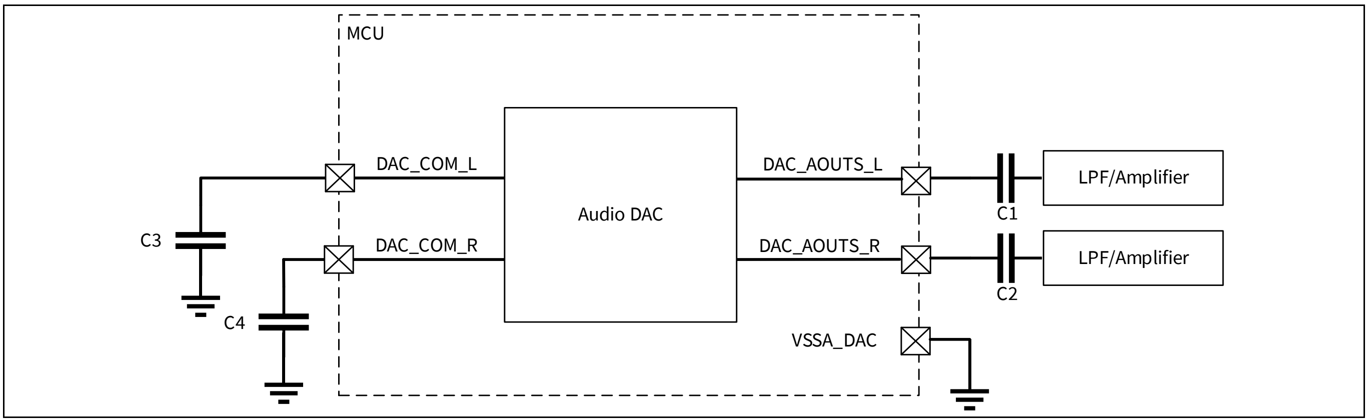


Figure 47 **AC coupling connected to LPF and amplifier (application example)**

Capacitors:

- **C1, C2:** 10-nF – 10-µF AC coupling capacitor
- **C3, C3:** 2.2-µF -10-µF low-ESR capacitors

16.1.3 Unused audio-DAC

When the audio-DAC is not used in the target system or is used only as mono sound output, the related audio-DAC pins are handled as described in Unused power domains and Dedicated port pins.

16.1.4 Avoiding the pop noise at the speaker output

The audio-DAC and external amplifier generates a pop noise when a transition from high-to-low or low-to-high occurs on the DAC_EN bit of the DAC0_IF_CTL register during power up or power down.

An external circuitry is recommended, as shown in the following diagrams, to suppress such pop noises if necessary. During audio-DAC start-up, the external amplifier must be either powered down, or in mute mode (if mute mode is available). These diagrams show examples for audio-DAC use cases.

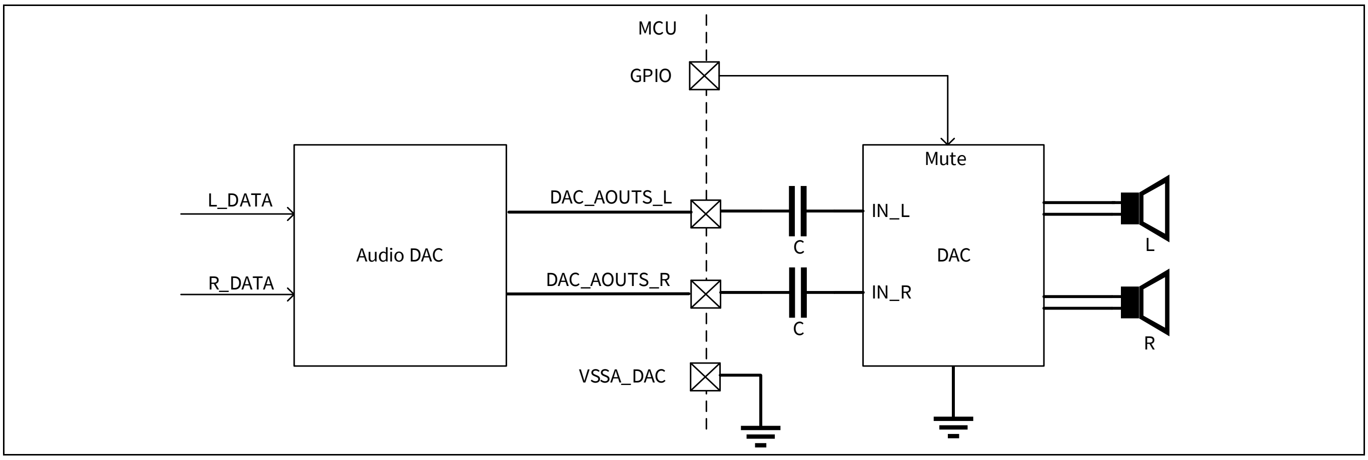


Figure 48 **Audio-DAC with single-end mono/stereo output**

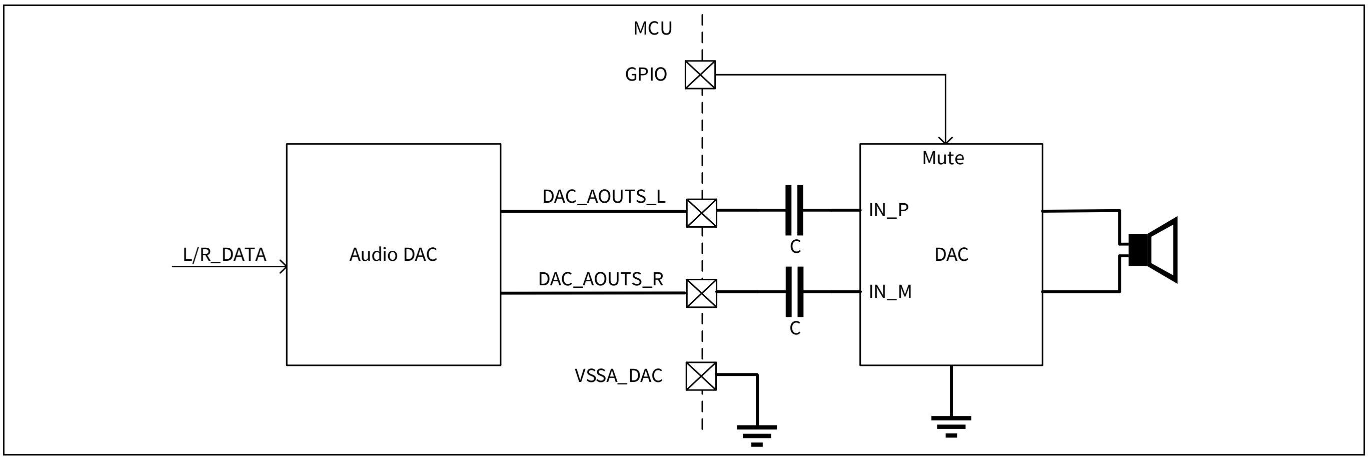


Figure 49 **Audio-DAC with differential mono output**

17 Summary

The application note described how to set up a minimum MCU system. The application note also provided hints on how to handle different use cases at MCU pins and how to make a proper PCB layout design.

18 Abbreviations

Abbreviation	Description
ADC	A/D converter
ALT	alternate
AN	analog input
BOD	brown-out detection
BOM	bill of material
Cap	capacitor
DAP	debug access port
decap	decoupling capacitor
DDR	double data rate. Data sampled twice within a clock cycle. fDATA = fCLK
DE	display enable
DS	datasheet
DUT	device under test
ECU	electronic control unit
ETM	embedded trace macrocell
Ext	external
GND	electrical ground
GPIO	general-purpose I/O
HVD	high-voltage detection
HSYNC	horizontal synchronization
IC	integrated circuit
IF	interface
Int	internal
IO	input output
JTAG	Joint Test Action Group is the common name for the IEEE 1149.1 Standard Test Access Port, Boundary-Scan Architecture, and interface for debug tools for on-chip debugging inside the target MCU
LDO	low drop-out line regulator
LPF	low-pass filter
LVD	low-voltage detection
LU	latch-up
MAC	media access control. Component independent from communication medium.
MB	map bit
MCU	microcontroller
MCU	microcontroller unit
PDN	power distribution network
PHY	PHYsical layer. Electrical component for data coding and decoding between pure digital and modulated channel

Abbreviation	Description
PMIC	power management IC
SDR	single data rate. Data sampled only once within a clock cycle. fDATA = ½ x fCLK
S/s	samples per second
NC	not connected
OCD	overcurrent detection
OVD	overvoltage detection
PCB	printed circuit board
POR	power-on reset
Rd	damping resistor
Rf	feedback resistor
STP	shielded twisted pair
SWD	serial wire debug
TRM	technical reference manual
VCC	Generic naming convention for power supply pin
Voltage droop	transient voltage drop
VSS	Generic naming convention for ground pin
VSYNC	vertical synchronization
WDT	watchdog timer

19 Appendix A – Power supply concept

19.1 Introduction

The appendix provides the MCU-specific proposals for a power supply concept including decoupling capacitors for the MCU power supply.

Note: The deployment of decoupling caps and the bypass capacitors depend on the application and is in full responsibility on the customer side. The bypass capacitors usually do not suffice to cover a PMIC load response. This is especially valid for I/O supplies. For more information, see I/O domains.

Note: By default, capacitors with X7R temperature characteristic should be used.

19.2 Definitions

- **f_{CLK}:** Clock signal frequency
- **f_{DATA}:** Data signal frequency
- **SDR:** Single data rate. Data sampled only once within a clock cycle. f_{DATA} = ½ x f_{CLK}
- **DDR:** Double data rate. Data sampled twice within a clock cycle. f_{DATA} = f_{CLK}
- **'Pin':** Synonym for the original pin name
- **Domain:** Power domain. One power domain can have one or more power pins (for example, VDDD has several pins)
- **Voltage drop:** Transient voltage drop

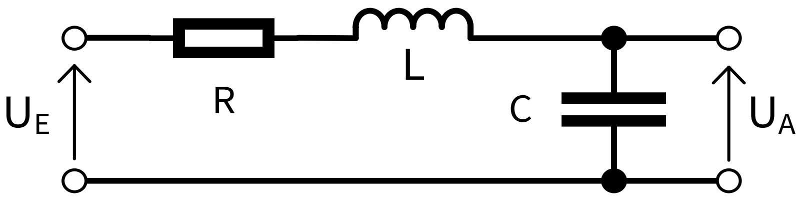


Figure 50 Equivalent RLC low-pass filter composition

19.3 CYT2B series with QFN and LQFP

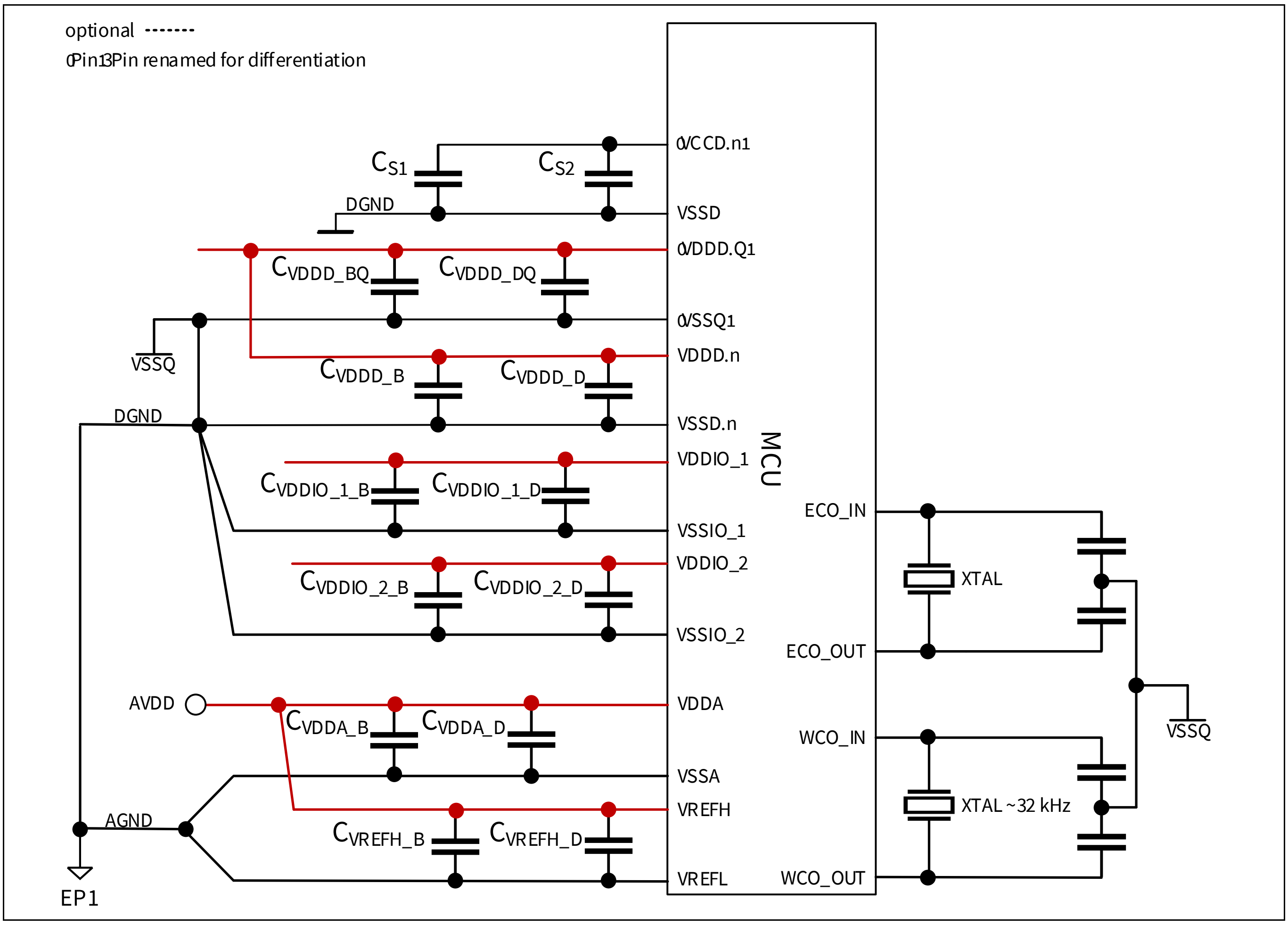


Figure 51 Power supply concept example for CYT2B series

Table 11 External component integration example for CYT2B series

Symbol	Parameter	Package	
		Value	**Remark**
C_{S1}	Bypass/smoothing capacitor for core power supply domain VCCD	X7R type	Value in the datasheet Close to the pin pair according to the device DS specification with respect to ‘VCCD.CS1’ 1 capacitor per domain ESR ≤ 100 mΩ, ESL ≤ 4 nH in total per capacitor and including the board track to all VCCD pins with priority on pin ‘VCCD.CS1’ with I_{DD}[11] ≤ 150 mA by active regulator Low impedance plane recommended

[11] I_{DD}: input current definition of VDDD in CYT2B datasheet

Symbol	Parameter	Package	
		Value	Remark
C_{S2}	Decoupling capacitor for core power supply domain VCCD	100 nF X7R ALT: 47 nF X7R	Optional: 1 capacitor on affected power domain pin, having risk of EMC issues due to PCB parasitic between C_{S1} and power domain pin
C_{VDDD_BQ}	Bypass capacitor for VDDD domain IPs	4.7 µF X7R	Also used for low-frequency decoupling and MCU inrush current For PCB-specific capacitor dimensioning, consider the inrush current from active regulator in spec ID SID603 mentioned in the datasheet and Appendix D – Active regulator inrush current ESR ≤ 100 mΩ, ESL ≤ 4 nH including board track
C_{VDDD_DQ}	Decoupling capacitor for VDDD domain IPs	100 nF X7R	Voltage drop greater than 300 mV must be avoided to keep the stability of the internal LDO and to reset assertion trip points Pin 'VDDD.Q' (Quiet Supply) not shared with I/O domain, but for oscillator among others
C_{VDDD_B}	Bypass capacitor for VDDD domain IPs and I/O	–	Required only if C_{VDDD_BQ} is not sufficient for bypassing the power rail supply
C_{VDDD_D}[12], [13]	Decoupling capacitor VDDD domain logic and I/O	100 nF X7R	1 capacitor per domain pin Decoupling conditions are valid per pin; all toggling groups should toggle asynchronously to each other
$C_{VDDIO\_1\_B}$[14]	Bypass capacitor for I/O domain VDDIO_1	1 µF X7R	Optional. Depending on the power supply inductance
$C_{VDDIO\_1\_D}$[15], [16]	Decoupling capacitor for I/O domain VDDIO_1	100 nF X7R	1 capacitor per domain pin Decoupling condition is valid for the whole domain
$C_{VDDIO\_2\_B}$	Bypass capacitor for I/O domain VDDIO_2	–	–

[12] VDDD: 5 V, 4% voltage drop, f_{DATA}: 2 MHz, 4x parallel transition: 20 ns, C_L/pin: 47 pF, no consideration of device internal impedance

[13] VDDD: 5 V, 4% voltage drop, f_{DATA}: 0.1 MHz, 4x parallel transition: 20 ns, C_L/pin: 47 pF, no consideration of device internal impedance

[14] VDDIO_1: PMIC load response > 300 kHz

[15] VDDIO_1: 5 V, 4% voltage drop, f_{DATA}: 2 MHz, 5x parallel transition: 20 ns, C_L/pin: 47 pF, no consideration of device internal impedance

[16] VDDIO_1: 5 V, 4% voltage drop, f_{DATA}: 0.1 MHz, 5x parallel transition: 100 ns, C_L/pin: 47 pF, asynchronous to footnote 15, no consideration of device internal impedance

Symbol	Parameter	Package	
		Value	Remark
$C_{VDDIO\_2\_D}$[17]	Decoupling capacitor for I/O domain VDDIO_2	100 nF X7R	1 capacitor per domain pin Decoupling condition is valid for the whole domain *Note:* *Voltage drop at VDDIO_2 must fulfill the requirement VDDA – 0.3 V ≤ VDDIO_2 ≤ VDDA*
C_{VDDA_B}[18]	Bypass capacitor for ADC VDDA	2.2 µF X7R	–
C_{VDDA_D}	Decoupling capacitor for ADC VDDA	100 nF X7R	1 capacitor per domain pin
C_{VREFH_B}	Bypass capacitor for ADC VREFH	2.2 µF X7R	Optional. Required only if a separate analog reference supply is used Silent supply is required. If the supply is not sufficient, LPF is required
C_{VREFH_D}	Decoupling capacitor for ADC VREFH	100 nF X7R	–

Table 12 Special power domain pins for CYT2B series

Name	Package pin number (original pin name)						Comment
	48-QFN	64-LQFP	80-LQFP	100-LQFP	144-LQFP	176-LQFP	
VDDD.Q	41 (VDDD)	55 (VDDD)	69 (VDDD)	86 (VDDD)	124 (VDDD)	153 (VDDD)	Quiet Supply Not shared with the I/O domain
VSSQ	42 (VSSD)	56 (VSSD)	70 (VSSD)	87 (VSSD)	125 (VSSD)	154 (VSSD)	Quiet Ground for the oscillator
VCCD.CS1	44 (VCCD)	58 (VCCD)	72 (VCCD)	89 (VCCD)	127 (VCCD)	156 (VCCD)	–

[17] VDDIO_2: 5 V, 4% voltage drop, f_{CLK}: 2 MHz, SDR, 10 x parallel transition: 20 ns, C_L/pin: 47 pF, no consideration of device internal impedance

[18] Connection of C_{VDDA_B} to both ADC DeCaps for low-noise environment. Three ADC units run simultaneously, not asynchronously and no use of the precondition feature. Power rails and ground parasitic for the analog supply should not exceed the following values according to Figure 59: R_{AVDD} ≤ 100 mΩ, L_{AVDD} ≤ 15 nH, R_{AGND} ≤ 100 mΩ, L_{AGND} ≤ 15 nH, L1 ≤ 1 nH, L2 ≤ 1 nH

19.4 CYT3B/4B/6B series with TEQFP package

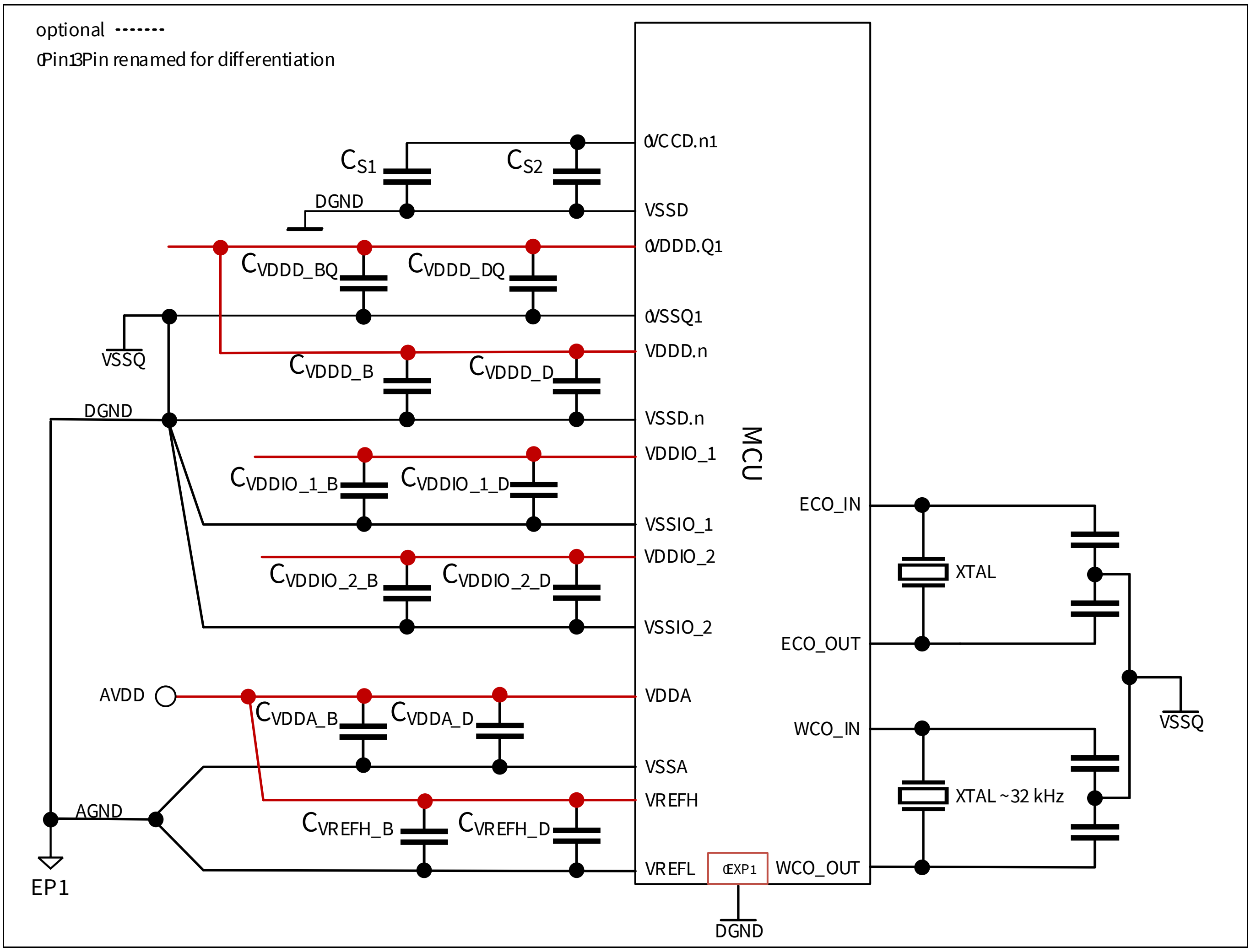


Figure 52 Power supply concept example for CYT3B/4B/6B series with TEQFP package

Table 13 External component integration example for CYT3B/4B/6B series with TEQFP package

Symbol	Parameter	Package	
		Value	**Remark**
C_{S1}	Bypass/smoothing capacitor for the core power supply domain VCCD	X7R Type	Value in the datasheet Close to pin pair according to the device DS specification with respect to 'VCCD.CS1' 2 capacitors per power domain ESR ≤ 100 mΩ, ESL ≤ 4 nH in total per capacitor including board track to all VCCD pins with priority on pin 'VCCD.CS1' with I_{DD_VDDD}[19] ≤ 300 mA by the active regulator Values do not cover higher load transition cases like wakeup from DeepSleep with permanent supply from an external PMIC
C_{S2}	Decoupling capacitor for core power supply domain VCCD	100 nF X7R ALT: 47 nF X7R	1 capacitor per domain pin group. For VCCD pin group definition, see Table 14
C_{VDDD_BQ}	Bypass capacitor for VDDD domain IPs	> 22 µF X7R	Also, used for low-frequency decoupling and MCU inrush current. For PCB-specific capacitor dimensioning, consider the inrush current from the active regulator in spec ID SID603 mentioned in the datasheet and Appendix D – Active regulator inrush current ESR ≤ 50 mΩ, ESL ≤ 2 nH in total including board track. In total 2 pcs recommended due to impedance
C_{VDDD_DQ}	Decoupling capacitor for VDDD domain IPs	100 nF X7R	Voltage drop greater than 300 mV must be avoided to keep the stability of the internal LDO and reset assertion trip points. Pin 'VDDD.Q' (Quiet Supply) is not shared with the I/O domain, but with oscillator among others
C_{VDDD_B}	Bypass capacitor for VDDD domain IPs and I/O	–	Only required if C_{VDDD_BQ} is not sufficient for bypassing power rail supply

[19] I_{DD_VDDD}: input current definition of VDDD in internal supply mode in CYT3B/4B/6B datasheet.

Symbol	Parameter	Package	
		Value	Remark
C_{VDDD_D} [20], [21]	Decoupling capacitor VDDD domain logic and I/O	100 nF X7R	1 capacitor per domain pin. Decoupling conditions are valid per pin; all toggling groups should toggle asynchronously with each other
$C_{VDDIO\_1\_B}$ [22]	Bypass capacitor for I/O domain VDDIO_1	1 µF X7R	Optional; depends on the power supply inductance
$C_{VDDIO\_1\_D}$ [23], [24}	Decoupling capacitor for I/O domain VDDIO_1	100 nF X7R	1 capacitor per domain pin Decoupling condition is valid for the whole domain
$C_{VDDIO\_2\_B}$	Bypass capacitor for I/O domain VDDIO_2	–	–
$C_{VDDIO\_2\_D}$ [25]	Decoupling capacitor for I/O domain VDDIO_2	100 nF X7R	1 capacitor per domain pin Decoupling condition is valid for the whole domain *Note:* *Voltage drop at VDDIO_2 must fulfill the requirement VDDA – 0.3 V ≤ VDDIO_2 ≤ VDDA*
C_{VDDA_B} [26]	Bypass capacitor for ADC VDDA	2.2 µF X7R	–
C_{VDDA_D}	Decoupling capacitor for ADC VDDA	100 nF X7R	1 capacitor per domain pin
C_{VREFH_B}	Bypass capacitor for ADC VREFH	2.2 µF X7R	Optional. Required only if a separate analog reference supply is used Silent supply is required. If the supply is not sufficient, LPF is required
C_{VREFH_D}	Decoupling capacitor for ADC VREFH	100 nF X7R	–

[20] VDDD: 5 V, 4% voltage drop, f_{DATA}: 2 MHz, 4x parallel transition: 20 ns, C_L/pin: 47 pF, no consideration of device internal impedance

[21] VDDD: 5 V, 4% voltage drop, f_{DATA}: 0.1 MHz, 4x parallel transition: 20 ns, C_L/pin: 47 pF, no consideration of device internal impedance

[22] VDDIO_1: PMIC load response > 300kHz

[23] VDDIO_1: 5 V, 4% voltage drop, f_{DATA}: 2 MHz, 5x parallel transition: 20 ns, C_L/pin: 47 pF, no consideration of device internal impedance

[24] VDDIO_1: 5 V, 4% voltage drop, f_{DATA}: 0.1 MHz, 5x parallel transition: 100 ns, C_L/pin: 47 pF, asynchronous to footnote 23, no consideration of device internal impedance

[25] VDDIO_2: 5 V, 4% voltage drop, f_{CLK}: 2 MHz, SDR, 10 x parallel transition: 20 ns, C_L/pin: 47 pF, no consideration of device internal impedance

[26] Connection of C_{VDDA_B} to both ADC DeCaps for low-noise environment. Three ADC units run simultaneously, not asynchronously and no use of the precondition feature. Power rails and ground parasitic for the analog supply should not exceed the following values according to Figure 59: R_{AVDD} ≤ 100 mΩ, L_{AVDD} ≤ 15 nH, R_{AGND} ≤ 100 mΩ, L_{AGND} ≤ 15 nH, L1 ≤ 1 nH, L2 ≤ 1 nH

Table 14 Special power domain pins for CYT3B/4B/6B series with TEQFP package

Name	Package pin number (original pin name)					Remark
	64-TEQFP	80-TEQFP	100-TEQFP	144-TEQFP	176-TEQFP	
VDDD.Q	Package(s) not available		86 (VDDD)	124 (VDDD)	153 (VDDD)	Quiet Supply Not shared with the I/O domain
VSSQ			87 (VSSD)	125 (VSSD)	154 (VSSD)	Quiet Ground for the oscillator
VCCD.CS2.A			27 (VCCD) 28 (VCCD)	38 (VCCD) 39 (VCCD)	46 (VCCD) 47 (VCCD)	One decap C_{S2} on the pin group Two decaps if the pin group has 3-pins
VCCD.CS2.B			64 (VCCD) 65 (VCCD)	92 (VCCD) 93 (VCCD)	111 (VCCD) 112 (VCCD) 113 (VCCD)	One decap C_{S2} on the pin group Two decaps if the pin group has 3-pins
VCCD.CS2.C			89 (VCCD)	127 (VCCD)	156 (VCCD)	One decap C_{S2} on the pin group Two decaps if the pin group has 3-pins
VCCD.CS2.D* (*only CYT6B series)			–	–	61 (VCCD) 62 (VCCD)	One decap C_{S2} on the pin group Two decaps if the pin group has 3-pins
EXP	N/A	N/A	Yes	Yes	Yes	Exposed pad

19.5 CYT3B/4B/6B series with BGA package

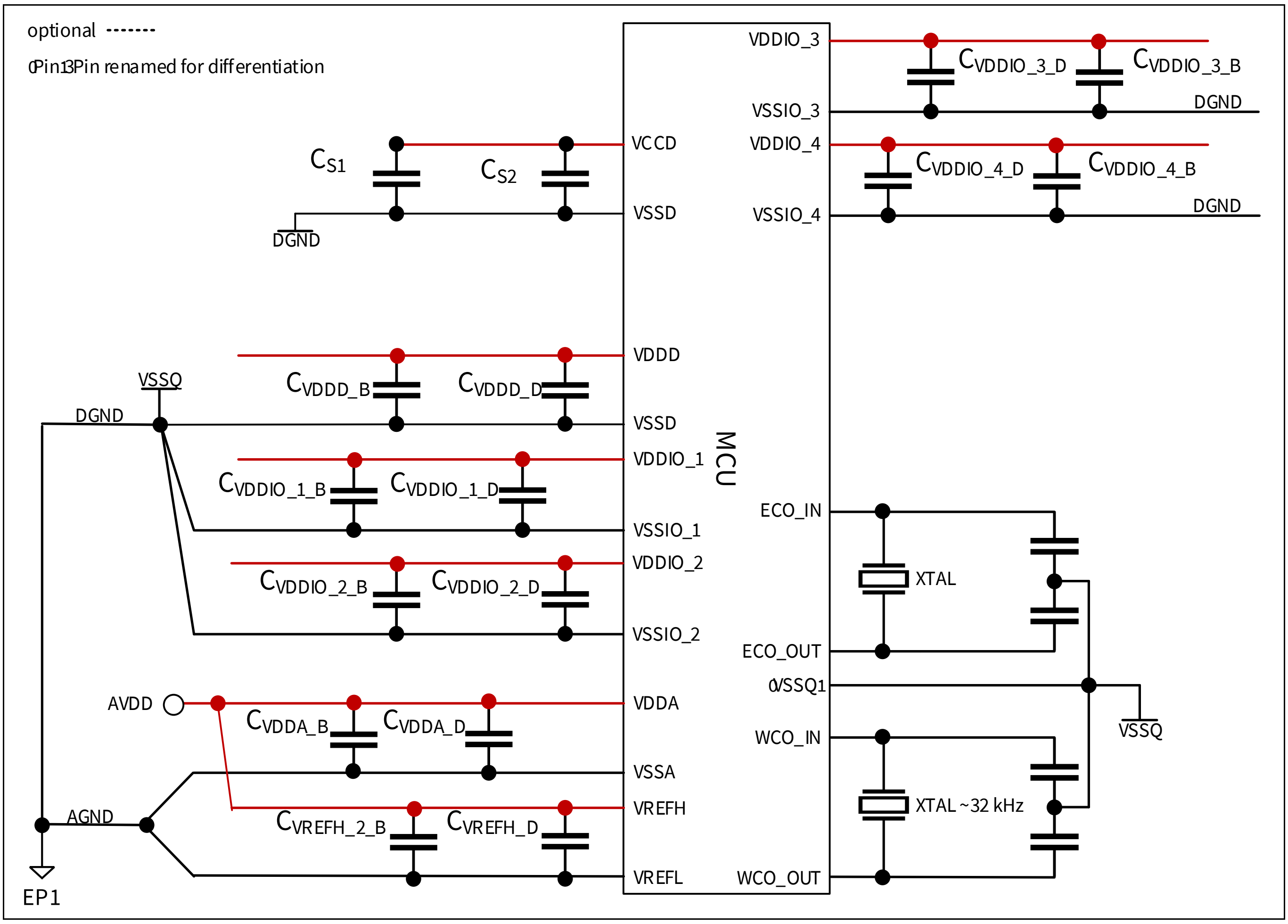


Figure 53 MCU power supply concept example for CYT3B/4B/6B series with BGA package

Table 15 External component integration example for CYT3B/4B/6B series BGA package

Symbol	Parameter	Package	
		Value	Remark
C_{S1}	Bypass/Smoothing capacitor for core power supply domain VCCD	X7R Type	Value in the datasheet Close to pin pair according to the device datasheet specification with respect to 'VCCD.CS1' Two capacitors per power domain ESR ≤ 100 mΩ, ESL ≤ 4 nH in total per capacitor including board track to all VCCD pins with priority on the 'VCCD.CS1' pin with I_{DD_VDDD}[27] ≤ 300 mA by the active regulator Values do not cover higher load transition cases like wakeup from

[27] I_{DD_VDDD}: Input current definition of VDDD in internal supply mode in CYT3B/4B/6B datasheet (see Related documents).

Symbol	Parameter	Package	
		Value	Remark
			DeepSleep with permanent supply from an external PMIC
C_{S2}	Decoupling capacitor for core power supply domain VCCD	100 nF X7R ALT: 47 nF X7R	1 capacitor per domain pin
C_{VDDD_B}	Bypass capacitor for VDDD domain IPs and I/O	> 22 µF X7R	Required for internal LDO For PCB-specific capacitor dimensioning, consider the inrush current from the active regulator in spec ID SID603 mentioned in the datasheet and Appendix D – Active regulator inrush current ESR ≤ 50 mΩ, ESL ≤ 2 nH in total including board track In total 2 pcs recommended due to impedance
C_{VDDD_D}	Decoupling capacitor VDDD domain logic and I/O	100 nF X7R	1 capacitor per domain pin Voltage drop greater than 300 mV must be avoided due to internal LDO and reset assertion trip points Number of parallel transitions should be reduced as much as possible
$C_{VDDIO\_1\_B}$[28]	Bypass capacitor for I/O domain VDDIO_1	1 µF X7R	1 capacitor per domain
$C_{VDDIO\_1\_D}$[25]	Decoupling capacitor for I/O domain VDDIO_1	100 nF X7R	1 capacitor per domain pin. Minimum two pieces are required
$C_{VDDIO\_2\_B}$	Bypass capacitor for I/O domain VDDIO_2	–	–
$C_{VDDIO\_2\_D}$[29]	Decoupling capacitor for I/O domain VDDIO_2	100 nF X7R	1 capacitor per domain pin *Note:* *Voltage drop at VDDIO_2 must fulfill the requirement VDDA – 0.3 V ≤ VDDIO_2 ≤ VDDA.*
$C_{VDDIO\_3\_B}$	Bypass capacitor for I/O domain VDDIO_3	1 µF X7R	1 capacitor per domain Equivalent power rail inductance: 20 nH

[28] VDDIO_1: 3.3 V, 5% voltage drop at capacitors(s), f_{CLK}: 25 MHz, DDR, 9 x parallel transition: 3 ns, C_L/pin: 20 pF, no consideration of device internal impedance

[29] VDDIO_2: 5 V, 4% voltage drop at capacitor(s), f_{DATA}: 2 MHz, 10 x parallel transition: 20 ns, C_L/pin: 47 pF, no consideration of device internal impedance

Symbol	Parameter	Package	
		Value	Remark
$C_{VDDIO\_3\_D}$[30]	Decoupling capacitor for I/O domain VDDIO_3	100 nF X7R 10 nF X7R	1 capacitor for domain 1 capacitor for domain
$C_{VDDIO\_4\_B}$	Bypass capacitor for I/O domain VDDIO_4	1 µF X7R	1 capacitor per domain Equivalent power rail inductance: 20 nH
$C_{VDDIO\_4\_D}$[31]	Decoupling capacitor for I/O domain VDDIO_4	100 nF X7R 10 nF X7R	1 capacitor for domain 1 capacitor for domain
C_{VDDA_B}[32]	Bypass capacitor for ADC VDDA	2.2 µF X7R	–
C_{VDDA_D}	Decoupling capacitor for ADC VDDA	100 nF X7R	1 capacitor per domain pin
$C_{VREFH\_2\_B}$	Bypass capacitor for ADC VREFH	2.2 µF X7R	Optional. Required only if a separate analog reference supply is used
C_{VREFH_D}	Decoupling capacitor for ADC VREFH	100 nF X7R	–

Table 16 Special power domain pins for CYT3B/4B series with BGA package

Name	Package pin number (original pin name)		Remark
	272-BGA	320-BGA	
VSSQ	L11 (VSSD_1)	N13 (VSSD_1)	Quiet Ground for the oscillator

Conditions:

[30] VDDIO_3: 3.3 V, 7% voltage drop at capacitors, f_{CLK}: 100 MHz, DDR, 9 x parallel transition: 1.5 ns, C_L/pin: 15 pF, no consideration of device internal impedance

[31] VDDIO_4: 3.3 V, 7% voltage drop at capacitors, f_{CLK}: 125 MHz, SDR, 9 x parallel transition: 0.75 ns, C_L/pin: 10 pF, no consideration of device internal impedance

[32] Connection of C_{VDDA_B} to both ADC DeCaps for low-noise environment. Three ADC units run simultaneously, not asynchronously and no use of the precondition feature. Power rails and ground parasitic for the analog supply should not exceed the following values according to Figure 59: $R_{AVDD} \leq 100$ mΩ, $L_{AVDD} \leq 15$ nH, $R_{AGND} \leq 100$ mΩ, $L_{AGND} \leq 15$ nH, L1 ≤ 1 nH, L2 ≤ 1nH

19.6 CYT3D series with TEQFP package

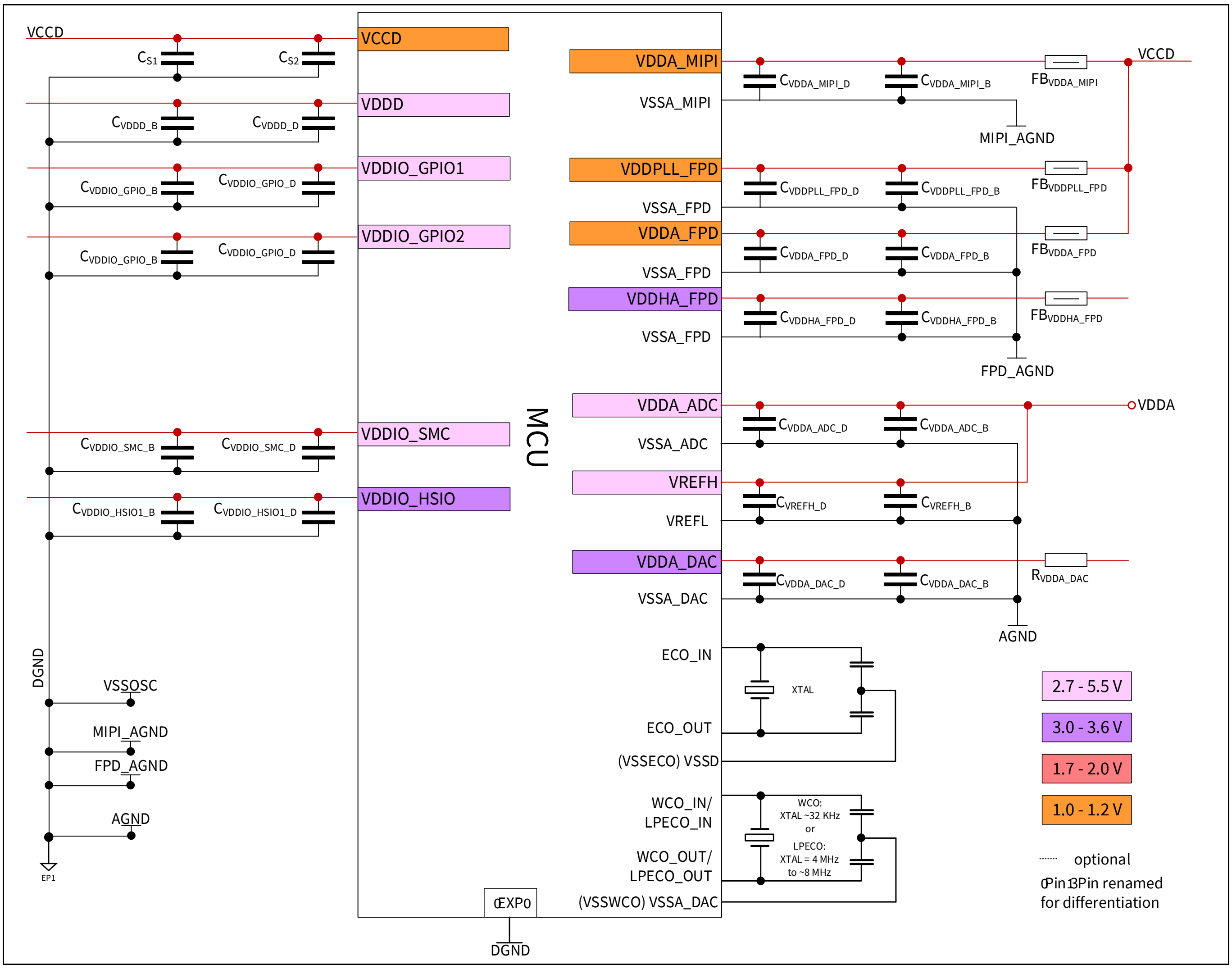


Figure 54 MCU power supply concept example for CYT3D series with TEQFP package

Table 17 External component integration example for CYT3D series TEQFP package[33], [34]

Symbol	Parameter	Package	
		Value	Remark
C_{S1}	Bypass/Smoothing capacitor for core power supply domain VCCD	X7R Type	Value in the datasheet 2 capacitors for domain. Close to the pin pair according to the device datasheet specification Check capacitor value and placement requirements between the MCU and PMIC depending on the core VCCD power rail concept[35],

[33] Device internal impedance and resonance frequencies are not considered.

[34] Dimensioning of bypass capacitors does not consider slow response time of PMICs in kHz range, especially for fast signal domains.

[35] Under clarification, if MIPI and FPD-link filter caps must be considered for total C_{S1} range.

Symbol	Parameter	Package	
		Value	**Remark**
C_{S2}	Decoupling capacitor for core power supply domain VCCD	100 nF X7R	1 capacitor per domain pin
C_{VDDD_B}	Bypass capacitor for VDDD domain IPs and I/O	> 22 µF X7R	Required for internal LDO For PCB-specific capacitor dimensioning, consider the inrush current from active regulator in spec ID SID603 mentioned in the datasheet, Appendix D – Active regulator inrush current, and all bypass capacitors for the core supply ESR ≤ 50 mΩ, ESL ≤ 2 nH in total including board track In total 2 pcs recommended due to impedance
C_{VDDD_D}	Decoupling capacitor VDDD domain logic and I/O	100 nF X7R	1 capacitor per domain pin Voltage drop greater than 300 mV must be avoided due to internal LDO and reset assertion trip points Number of parallel transitions should be reduced as much as possible
$C_{VDDIO\_GPIO1\_B}$	Bypass capacitor for I/O domain GPIO	1 µF X7R	1 capacitor for domain
$C_{VDDIO\_GPIO1\_D}$	Decoupling capacitor for I/O domain GPIO	100 nF X7R	1 capacitor per domain pin
$C_{VDDIO\_GPIO2\_B}$	Bypass capacitor for I/O domain GPIO	1 µF X7R	1 capacitor for domain
$C_{VDDIO\_GPIO2\_D}$	Decoupling capacitor for I/O domain GPIO	100 nF X7R	1 capacitor per domain pin
$C_{VDDIO\_SMC\_B}$	Bypass capacitor for I/O domain SMC	2.2 µF X7R	1 capacitor per domain. Required only when SMC control is in use.
$C_{VDDIO\_SMC\_D}$	Decoupling capacitor for I/O domain SMC	100 nF X7R	1 capacitor per 2 domain pins
$C_{VDDIO\_HSIO1\_B1}$	Bypass capacitor for I/O domain HSIO1	1 µF X7R	1 capacitor per SMIF ch
$C_{VDDIO\_HSIO1\_B2}$	Bypass capacitor for I/O domain HSIO1	470 nF X7R	1 capacitor per ETH ch
$C_{VDDIO\_HSIO1\_D}$	Decoupling capacitor for I/O domain HSIO1	100 nF X7R	1 capacitor per 2 domain pins
$C_{VDDA\_ADC\_B}$	Bypass capacitor for ADC VDDA	4.7 µF X7R	1 capacitor per domain

C_{S1} Datasheet specification excludes C_{VDDA_FPD} and C_{VDDA_MIPI} capacitance

Symbol	Parameter	Package	
		Value	Remark
$C_{VDDA\_ADC\_D}$	Decoupling capacitor for ADC VDDA	100 nF X7R	1 capacitor per domain pin
C_{VREFH_B}	Bypass capacitor for ADC VREFH	2.2 µF X7R	1 capacitor per domain. Optional Required only if a separate analog reference supply is used Silent supply required. If not sufficient, a low-pass filter (LPF) required
C_{VREFH_D}	Decoupling capacitor for ADC VREFH	100 nF X7R	1 capacitor per 2 domain pins
$C_{VDDA\_DAC\_B}$	Bypass capacitor for DAC VDDA	2.2 µF X7R	1 capacitor per domain
$C_{VDDA\_DAC\_D}$	Decoupling capacitor for DAC VDDA	100 nF X7R	1 capacitor per domain
$C_{VDDPLL\_FPD\_B}$	Bypass capacitor for FPD VDDPLL	10 µF X7R	1 capacitor per domain
$C_{VDDPLL\_FPD\_D}$	Decoupling capacitor for FPD VDDPLL	1.5 nF X7R	1 capacitor per 2 domain pins
F_{VDDPLL_FPD}	Ferrite bead for FPD VDDPLL	MPZ1608B471ATA00	1 ferrite bead per domain. Silent supply must be ensured In total, 2 Ω in series as RLC filter[36], [37] against the resonance frequency < 100 kHz from the PMIC
$C_{VDDA\_FPD\_B}$	Bypass capacitor for FPD VDDA	10 µF X7R	1 capacitor per domain
$C_{VDDA\_FPD\_D}$	Decoupling capacitor for FPD VDDA	1.5 nF X7R	4 capacitors per domain
F_{VDDA_FPD}	Ferrite bead for FPD VDDA	MPZ1608B471ATA00	1 ferrite bead per domain. Silent supply must be ensured In total, 2 Ω DC in series as RLC filter[36], [37] against the resonance frequency< 100 kHz from the PMIC
$C_{VDDA\_MIPI\_B}$	Bypass capacitor for MIPI VDDA	10 µF X7R	1 capacitor for domain
$C_{VDDA\_MIPI\_D}$	Decoupling capacitor for MIPI VDDA	100 nF X7R, 1 nF X7R	1 capacitor per domain, 1 capacitor per domain
F_{VDDA_MIPI}	Ferrite bead for MIPI VDDA	MPZ1608B471ATA00	1 ferrite bead per domain. Silent supply must be ensured

[36] Equivalent RLC filter type as shown in Figure 50.

[37] The IR drop of the optional series resistor in the ferrite filter can violate the min. operation specification of the dedicated power domain. The resistor serves as countermeasure for the resonance frequency range. This filter combination was characterized with following DC level applied in front of the filter (LV domain: 1.09V, HV domain: 3.0V).

Symbol	Parameter	Package	
		Value	Remark
			Optional: In total, 2 Ω DC in series as RLC filter[36], [37] against the resonance frequency< 100 kHz from the PMIC
$C_{VDDHA\_FPD\_B}$	Bypass capacitor for FPD VDDHA	10 µF X7R	1 capacitor per domain
$C_{VDDHA\_FPD\_D}$	Decoupling capacitor for FPD VDDHA	100 nF X7R 10 nF X7R 1.5 nF X7R	1 capacitor per domain 1 capacitor per domain 1 capacitor per domain
F_{VDDHA_FPD}	Ferrite bead for FPD VDDA	MPZ1608B471ATA00	1 ferrite bead per domain. Silent supply must be ensured Optional: In total, 2 Ω DC in series as RLC filter[36], [37] against the resonance frequency< 100 kHz from the PMIC

Table 18 Special power domain pins for CYT3D series with TEQFP packages

Name	Package pin number (original pin name)		Remark
	208-TEQFP	216-TEQFP	
(VSSECO) VSSD	138 (VSSD)	142 (VSSD)	Quiet ground for ECO oscillator shielding shared with other SRSS IPs
(VSSWCO) VSSA_DAC	131 (VSSD_DAC)	135 (VSSD_DAC)	Quiet ground for WCO/LPECO oscillator shielding shared with analog IP
'EXP'	N/A	N/A	Exposed pad

19.7 CYT4D series with BGA package

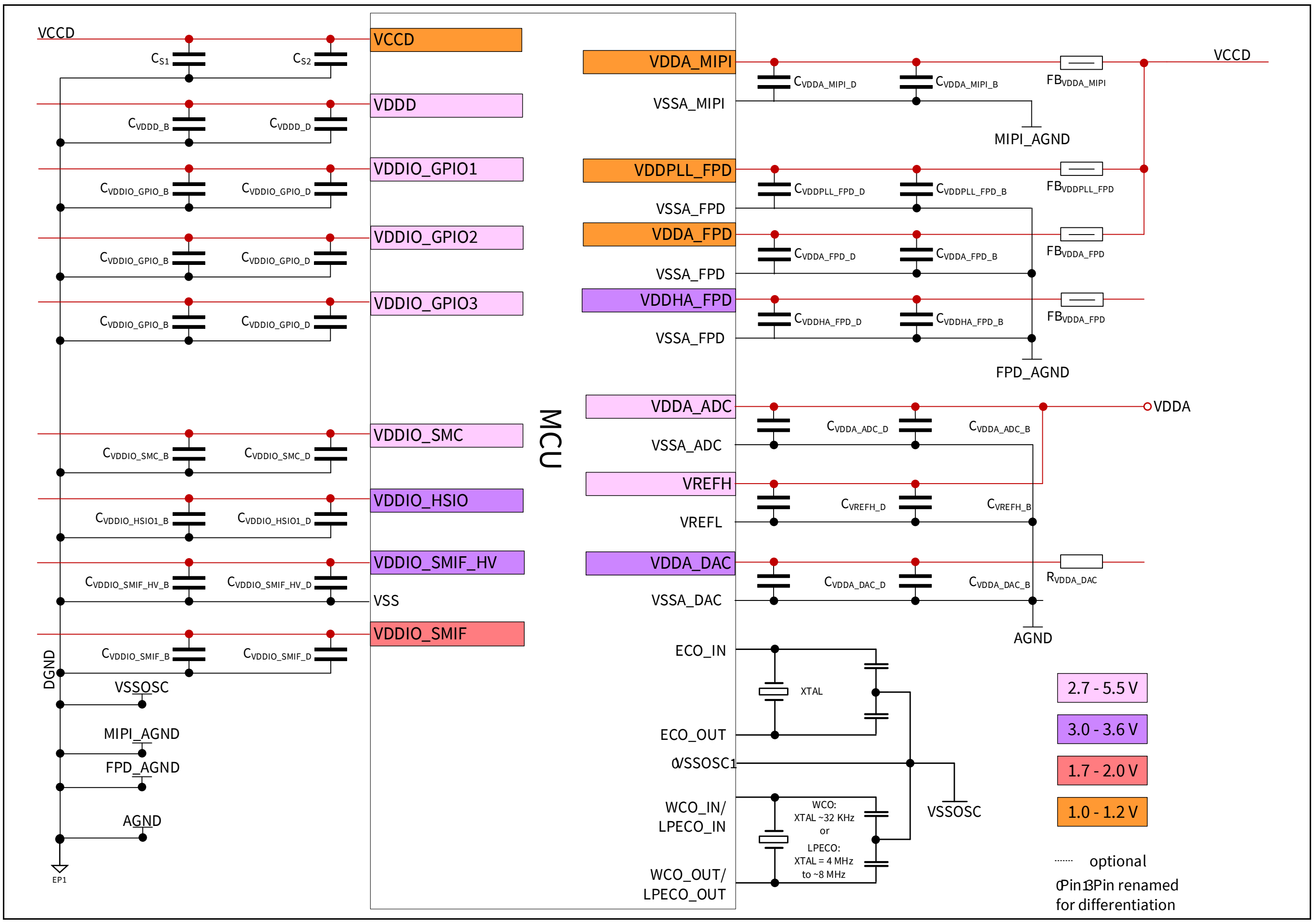


Figure 55 MCU power supply concept example for CYT4D series with BGA package

Table 19 External component integration example for CYT4D series with BGA package[38], [39]

Symbol	Parameter	Package	
		Value	**Remark**
C_{S1}	Bypass/Smoothing capacitor for core power supply domain VCCD	X7R type	Value in the datasheet 2 capacitors for domain. Close to the pin pair according to the device datasheet specification Check the capacitor value and placement requirements between the MCU and PMIC depending on the core VCCD power rail concept[40]

[38] Device internal impedance and resonance frequencies are not considered.

[39] Dimensioning of bypass capacitors does not consider slow response time of PMICs in kHz range, especially for fast signal domains.

[40] Under clarification, if MIPI and FPD-link filter caps must be considered for total C_{S1} range.
C_{S1} Datasheet specification excludes C_{VDDA_FPD} and C_{VDDA_MIPI} capacitance

Symbol	Parameter	Package	
		Value	Remark
C_{S2}	Decoupling capacitor for core power supply domain VCCD	100 nF X7R	1 capacitor per domain pin
C_{VDDD_B}	Bypass capacitor for VDDD domain IPs and I/O	> 22 µF X7R	Required for internal LDO For PCB-specific capacitor dimensioning, consider the inrush current from the active regulator in spec ID SID603 mentioned in the datasheet, Appendix D – Active regulator inrush current, and all bypass capacitors for the core supply ESR ≤ 50 mΩ, ESL ≤ 2 nH in total including board track In total 2 pcs recommended due to impedance
C_{VDDD_D}	Decoupling capacitor VDDD domain logic and I/O	100 nF X7R	1 capacitor per domain pin Voltage drop greater than 300 mV must be avoided due to internal LDO Number of parallel transitions should be reduced as much as possible
$C_{VDDIO\_GPIO1\_B}$	Bypass capacitor for I/O domain GPIO	1 µF X7R	1 capacitor for domain
$C_{VDDIO\_GPIO1\_D}$	Decoupling capacitor for I/O domain GPIO	100 nF X7R	1 capacitor per domain pin
$C_{VDDIO\_GPIO2\_B}$	Bypass capacitor for I/O domain GPIO	1 µF X7R	1 capacitor for domain
$C_{VDDIO\_GPIO2\_D}$	Decoupling capacitor for I/O domain GPIO	100 nF X7R	1 capacitor per domain pin
$C_{VDDIO\_GPIO3\_B}$	Bypass capacitor for I/O domain GPIO	1 µF X7R	1 capacitor for domain
$C_{VDDIO\_GPIO3\_D}$	Decoupling capacitor for I/O domain GPIO	100 nF X7R	1 capacitor per domain pin
$C_{VDDIO\_SMC\_B}$	Bypass capacitor for I/O domain SMC	2.2 µF X7R	1 capacitor per domain
$C_{VDDIO\_SMC\_D}$	Decoupling capacitor for I/O domain SMC	100 nF X7R	1 capacitor per 2 domain pins
$C_{VDDIO\_HSIO1\_B}$	Bypass capacitor for I/O domain HSIO1	2.2 µF X7R	1 capacitor per domain
$C_{VDDIO\_HSIO1\_D}$	Decoupling capacitor for I/O domain HSIO1	100 nF X7R	1 capacitor per 2 domain pins
$C_{VDDIO\_SMIF\_B}$	Bypass capacitor for I/O domain SMIF	2.2 µF X7R	1 capacitor per domain

Symbol	Parameter	Package	
		Value	Remark
$C_{VDDIO\_SMIF\_D}$	Decoupling capacitor for I/O domain SMIF	100 nF + 2.2 nF or 2x 100 nF	1 capacitor per 2 domain pins
$C_{VDDIO\_SMIF\_HV\_B}$	Bypass capacitor for I/O domain SMIF_HV	2.2 µF X7R	No capacitor per domain
$C_{VDDIO\_SMIF\_HV\_D}$	Decoupling capacitor for I/O domain SMIF_HV	100 nF	1 capacitor per domain
$C_{VDDA\_ADC\_B}$	Bypass capacitor for ADC VDDA	4.7 µF X7R	1 capacitor per domain
$C_{VDDA\_ADC\_D}$	Decoupling capacitor for ADC VDDA	100 nF X7R	1 capacitor per domain pin
$C_{VDDA\_DAC\_B}$	Bypass capacitor for DAC VDDA	2.2 µF X7R	1 capacitor per domain
$C_{VDDA\_DAC\_D}$	Decoupling capacitor for DAC VDDA	100 nF X7R	1 capacitor per domain
C_{VREFH_B}	Bypass capacitor for ADC VREFH	2.2 µF X7R	1 capacitor per domain. Optional. Required only if a separate analog reference supply is used
C_{VREFH_D}	Decoupling capacitor for ADC VREFH	100 nF X7R	1 capacitor per 2 domain pins
$C_{VDDPLL\_FPD\_B}$	Bypass capacitor for FPD VDDPLL	10 µF X7R	1 capacitor per domain
$C_{VDDPLL\_FPD\_D}$	Decoupling capacitor for FPD VDDPLL	1.5 nF X7R	1 capacitor per domain
F_{VDDPLL_FPD}	Ferrite bead for FPD VDDPLL	MPZ1608B471ATA00	1 ferrite bead per domain. Silent supply must be ensured In total, 2 Ω DC in series as RLC filter[41], [42] against the resonance frequency< 100 kHz from the PMIC
$C_{VDDA\_FPD\_B}$	Bypass capacitor for FPD VDDA	10 µF X7R	1 capacitor per domain
$C_{VDDA\_FPD\_D}$	Decoupling capacitor for FPD VDDA	1.5 nF X7R	1 capacitor per domain
F_{VDDA_FPD}	Ferrite bead for FPD VDDA	MPZ1608B471ATA00	1 ferrite bead per domain. Silent supply must be ensured Optional: In total, 2 Ω DC in series as RLC filter[41], [42] against the resonance frequency< 100 kHz from the PMIC

[41] Equivalent RLC filter type as shown in Figure 50.

[42] The IR drop of the optional series resistor in the ferrite filter can violate the min. operation specification of the dedicated power domain. The resistor serves as countermeasure for the resonance frequency range. This filter combination was characterized with following DC level applied in front of the filter (LV domain: 1.09V, HV domain: 3.0V).

Symbol	Parameter	Package	
		Value	Remark
$C_{VDDA\_MIPI\_B}$	Bypass capacitor for MIPI VDDA	10 µF X7R	1 capacitor for domain
$C_{VDDA\_MIPI\_D}$	Decoupling capacitor for MIPI VDDA	100 nF X7R, 1nF X7R	1 capacitor per domain, 1 capacitor per domain
F_{VDDA_MIPI}	Ferrite bead for MIPI VDDA	MPZ1608B471ATA00	1 ferrite bead per domain. Silent supply must be ensured In total, 2 Ω DC in series as RLC filter[41], [42] against the resonance frequency< 100 kHz from the PMIC
$C_{VDDHA\_FPD\_B}$	Bypass capacitor for FPD VDDHA	10 µF X7R	1 capacitor per domain
$C_{VDDHA\_FPD\_D}$	Decoupling capacitor for FPD VDDHA	100 nF X7R, 10 nF X7R, 1.5 nF X7R	1 capacitor per domain, 1 capacitor per domain, 1 capacitor per domain
F_{VDDHA_FPD}	Ferrite bead for FPD VDDA	MPZ1608B471ATA00	1 ferrite bead per domain. Silent supply must be ensured In total, 2 Ω DC in series as RLC filter[41], [42] against the resonance frequency< 100 kHz from the PMIC

Table 20 Special power domain pins for CYT4D series with BGA packages

Name	Package pin number (original pin name)		Comment
	327-BGA rev. A0	500-BGA rev. A0	
VSSOSC	E20, F19, G20	H25, H26, K25, K26 (VSS)	Quiet ground for oscillator shielding

19.8 CYT4E series with BGA package

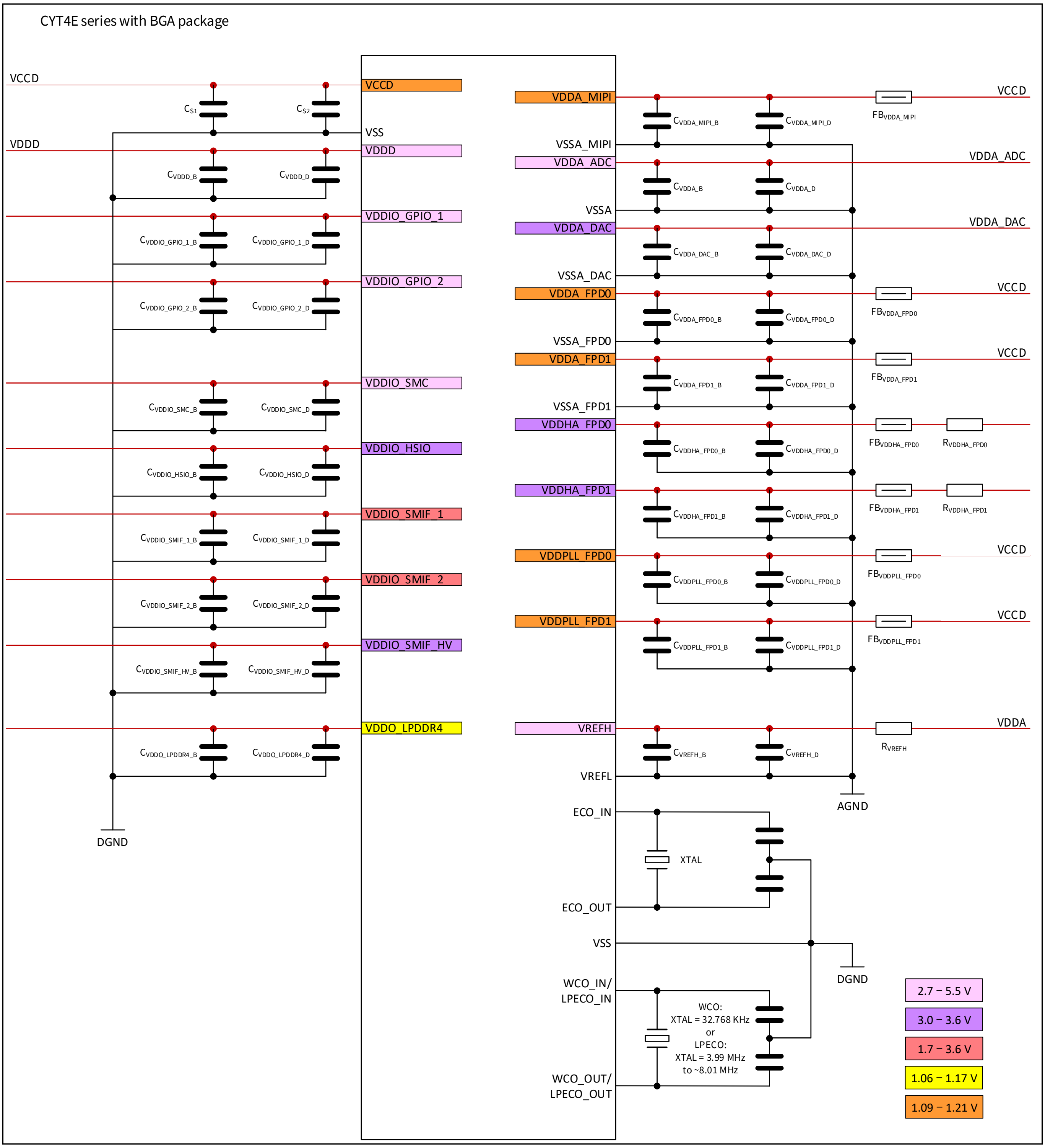


Figure 56 MCU power supply concept example for CYT4E series with BGA package

Table 21 External component integration example for CYT4E series with BGA package[43], [44]

Symbol	Parameter	Package	
		Value	Remark
C_{S1}	Bypass/Smoothing capacitor for core power supply domain VCCD	X7R type	Value in the datasheet 2 capacitors for domain. Close to the pin pair according to the device datasheet specification Check the capacitor value and placement requirements between the MCU and PMIC depending on the core VCCD power rail concept[45]
C_{S2}	Decoupling capacitor for core power supply domain VCCD	100 nF X7R	1 capacitor per domain pin
C_{VDDD_B}	Bypass capacitor for VDDD domain IPs and I/O	> 22 µF X7R	Required for internal LDO For PCB-specific capacitor dimensioning, consider the inrush current from the active regulator in spec ID SID603 mentioned in the datasheet, Appendix D – Active regulator inrush current, and all bypass capacitors for the core supply. ESR ≤ 50 mΩ, ESL ≤ 2 nH in total including board track In total 2 pcs recommended due to impedance
C_{VDDD_D}	Decoupling capacitor VDDD domain logic and I/O	100 nF X7R	1 capacitor per domain pin Voltage drop greater than 300 mV must be avoided due to internal LDO Number of parallel transitions should be reduced as much as possible
$C_{VDDIO\_GPIO1\_B}$	Bypass capacitor for I/O domain GPIO	1 µF X7R	1 capacitor for domain
$C_{VDDIO\_GPIO1\_D}$	Decoupling capacitor for I/O domain GPIO	100 nF X7R	1 capacitor per domain pin
$C_{VDDIO\_GPIO2\_B}$	Bypass capacitor for I/O domain GPIO	1 µF X7R	1 capacitor for domain
$C_{VDDIO\_GPIO2\_D}$	Decoupling capacitor for I/O domain GPIO	100 nF X7R	1 capacitor per domain pin
$C_{VDDIO\_SMC\_B}$	Bypass capacitor for I/O domain SMC	2.2 µF X7R	1 capacitor per domain

[43] Device internal impedance and resonance frequencies are not considered.

[44] Dimensioning of bypass capacitors does not consider slow response time of PMICs in kHz range, especially for fast signal domains.

[45] Under clarification, if MIPI and FPD-link filter caps must be considered for total C_{S1} range.

Symbol	Parameter	Package	
		Value	Remark
$C_{VDDIO\_SMC\_D}$	Decoupling capacitor for I/O domain SMC	100 nF X7R	1 capacitor per 2 domain pins
$C_{VDDIO\_HSIO\_B}$	Bypass capacitor for I/O domain HSIO	2.2 µF X7R	1 capacitor per domain
$C_{VDDIO\_HSIO\_D}$	Decoupling capacitor for I/O domain HSIO	100 nF X7R	1 capacitor per 2 domain pins
$C_{VDDIO\_SMIF\_0\_B}$	Bypass capacitor for I/O domain SMIF	2.2 µF X7R	1 capacitor per domain
$C_{VDDIO\_SMIF\_0\_D}$	Decoupling capacitor for I/O domain SMIF	100 nF + 2.2 nF or 2x 100nF	1 capacitor per 2 domain pins
$C_{VDDIO\_SMIF\_1\_B}$	Bypass capacitor for I/O domain SMIF	2.2 µF X7R	1 capacitor per domain
$C_{VDDIO\_SMIF\_1\_D}$	Decoupling capacitor for I/O domain SMIF	100 nF + 2.2 nF or 2x 100nF	1 capacitor per 2 domain pins
$C_{VDDIO\_SMIF\_HV\_B}$	Bypass capacitor for I/O domain SMIF_HV	2.2 µF X7R	No capacitor per domain
$C_{VDDIO\_SMIF\_HV\_D}$	Decoupling capacitor for I/O domain SMIF_HV	100 nF	1 capacitor per domain
$C_{VDDA\ B}$	Bypass capacitor for VDDA	4.7 µF X7R	1 capacitor per domain
$C_{VDDA\ D}$	Decoupling capacitor for VDDA	100 nF X7R	1 capacitor per domain pin
$C_{VDDA\_DAC\_B}$	Bypass capacitor for DAC VDDA	2.2 µF X7R	1 capacitor per domain
$C_{VDDA\_DAC\_D}$	Decoupling capacitor for DAC VDDA	100 nF X7R	1 capacitor per domain
C_{VREFH_B}	Bypass capacitor for ADC VREFH	2.2 µF X7R	1 capacitor per domain. Optional Required only if a separate analog reference supply is used
C_{VREFH_D}	Decoupling capacitor for ADC VREFH	100 nF X7R	1 capacitor per 2 domain pins
$C_{VDDA\_FPD\_0\_B}$	Bypass capacitor for FPD_0 VDDA	10 µF X7R	1 capacitor per domain
$C_{VDDA\_FPD\_0\_D}$	Decoupling capacitor for FPD_0 VDDA	1.5 nF X7R	1 capacitor per domain
$F_{VDDA\_FPD\_0}$	Ferrite bead for FPD_0 VDDA	MPZ1608B471ATA00	1 ferrite bead per domain. Silent supply must be ensured Optional: In total, 2 Ω DC in series as RLC filter[41], [42] against the resonance frequency< 100 kHz from the PMIC
$C_{VDDA\_FPD\_1\_B}$	Bypass capacitor for FPD_1 VDDA	10 µF X7R	1 capacitor per domain

Symbol	Parameter	Package	
		Value	Remark
$C_{VDDA\_FPD\_1\_D}$	Decoupling capacitor for FPD_1 VDDA	1.5 nF X7R	1 capacitor per domain
$F_{VDDPLL\_FPD\_1}$	Ferrite bead for FPD_1 VDDA	MPZ1608B471ATA00	1 ferrite bead per domain. Silent supply must be ensured Optional: In total, 2 Ω DC in series as RLC filter[41], [42] against the resonance frequency< 100 kHz from the PMIC
$C_{VDDA\_MIPI\_B}$	Bypass capacitor for MIPI VDDA	10 µF X7R	1 capacitor for domain
$C_{VDDA\_MIPI\_D}$	Decoupling capacitor for MIPI VDDA	100 nF X7R, 1nF X7R	1 capacitor per domain, 1 capacitor per domain
F_{VDDA_MIPI}	Ferrite bead for MIPI VDDA	MPZ1608B471ATA00	1 ferrite bead per domain. Silent supply must be ensured In total, 2 Ω DC in series as RLC filter[41], [42] against the resonance frequency< 100 kHz from the PMIC
$C_{VDDHA\_FPD\_0\_B}$	Bypass capacitor for FPD_0 VDDHA	10 µF X7R	1 capacitor per domain
$C_{VDDHA\_FPD\_0\_D}$	Decoupling capacitor for FPD_0 VDDHA	100 nF X7R, 10 nF X7R, 1.5 nF X7R	1 capacitor per domain, 1 capacitor per domain, 1 capacitor per domain
$F_{VDDHA\_FPD\_0}$	Ferrite bead for FPD_0 VDDHA	MPZ1608B471ATA00	1 ferrite bead per domain. Silent supply must be ensured In total, 2 Ω DC in series as RLC filter[41], [42] against the resonance frequency< 100 kHz from the PMIC
$C_{VDDHA\_FPD\_1\_B}$	Bypass capacitor for FPD_1 VDDHA	10 µF X7R	1 capacitor per domain
$C_{VDDHA\_FPD\_1\_D}$	Decoupling capacitor for FPD_1 VDDHA	100 nF X7R, 10 nF X7R, 1.5 nF X7R	1 capacitor per domain, 1 capacitor per domain, 1 capacitor per domain
$F_{VDDHA\_FPD\_1}$	Ferrite bead for FPD_1 VDDHA	MPZ1608B471ATA00	1 ferrite bead per domain. Silent supply must be ensured In total, 2 Ω DC in series as RLC filter[41], [42] against the resonance frequency< 100 kHz from the PMIC
$C_{VDDO\_LPDDR4\_B}$	Bypass capacitor for VDDO_LPDDR4	[46]	–

[46] See AN236076 - LPDDR4 design guidelines for TRAVEO™ T2G Automotive Cluster 2D family MCUs (Doc. No. 002-36076)

Symbol	Parameter	Package	
		Value	Remark
$C_{VDDO\_LPDDR4\_B}$	Decoupling capacitor for VDDO_LPDDR4	[47]	–

[47] See AN236076 - LPDDR4 design guidelines for TRAVEO™ T2G Automotive Cluster 2D family MCUs (Doc. No. 002-36076)

19.9 CYT2C series with LQFP package

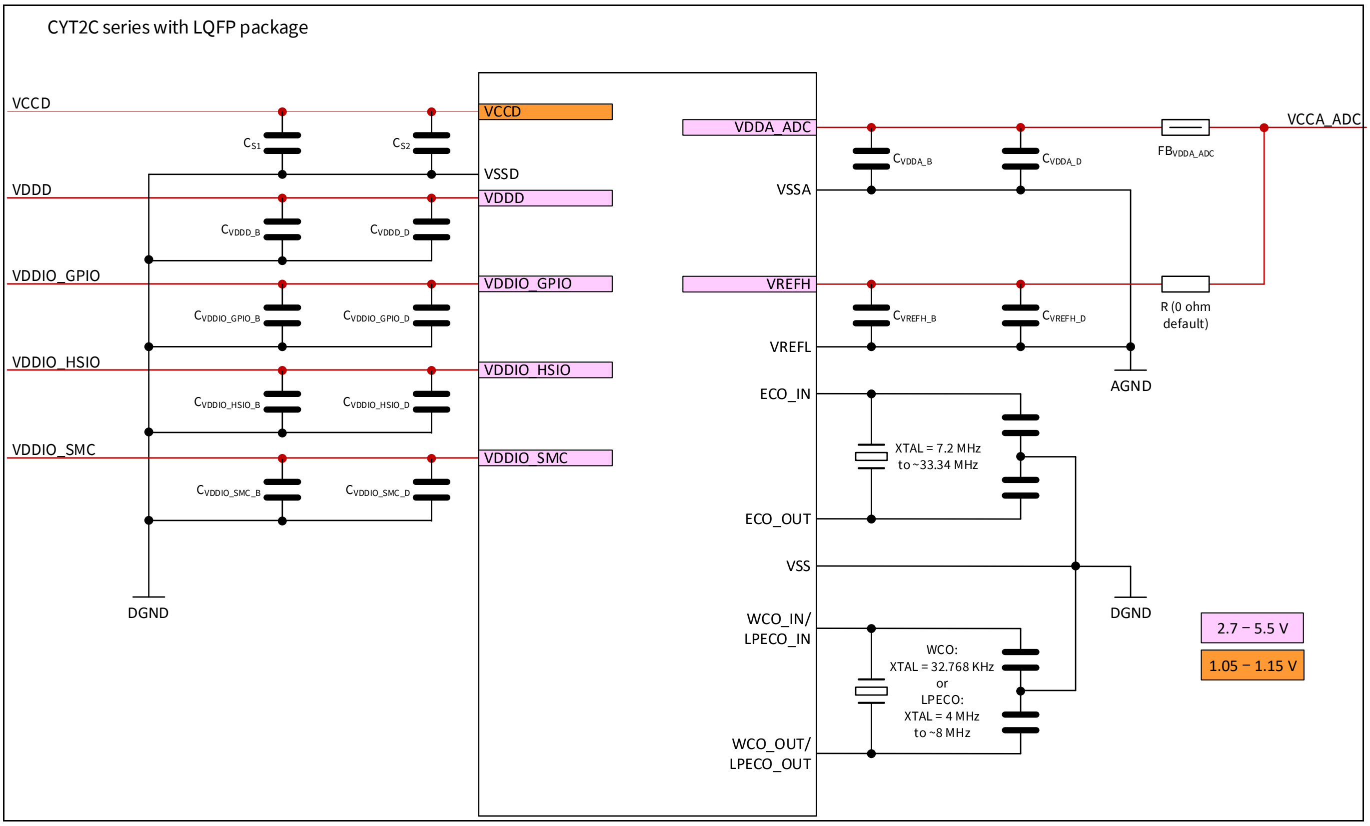


Figure 57 MCU power supply concept example for CYT2C series with LQFP package

Table 22 External component integration example for CYT2C series with LQFP package

Symbol	Parameter	Package	
		Value	Remark
C_{S1}	Bypass/Smoothing capacitor for core power supply domain VCCD	X7R type	Value in the datasheet 2 capacitors for domain. Close to the pin pair according to the device datasheet specification Check the capacitor value and placement requirements between the MCU and PMIC depending on the core VCCD power rail concept
C_{S2}	Decoupling capacitor for core power supply domain VCCD	100 nF X7R	1 capacitor per domain pin
C_{VDDD_B}	Bypass capacitor for VDDD domain IPs and I/O	> 22 µF X7R	Required for internal LDO For PCB-specific capacitor dimensioning, consider the inrush current from the active regulator in spec ID SID603 mentioned in the datasheet, Appendix D – Active regulator inrush current, and all bypass capacitors for the core supply

Symbol	Parameter	Package	
		Value	Remark
			ESR ≤ 50 mΩ, ESL ≤ 2 nH in total including board track In total 2 pcs recommended due to impedance
C_{VDDD_D}	Decoupling capacitor VDDD domain logic and I/O	100 nF X7R	1 capacitor per domain pin Voltage drop greater than 300 mV must be avoided due to internal LDO Number of parallel transitions should be reduced as much as possible
$C_{VDDIO\_GPIO\_B}$	Bypass capacitor for I/O domain GPIO	1 µF X7R	1 capacitor for domain
$C_{VDDIO\_GPIO\_D}$	Decoupling capacitor for I/O domain GPIO	100 nF X7R	1 capacitor per domain pin
$C_{VDDIO\_SMC\_B}$	Bypass capacitor for I/O domain SMC	2.2 µF X7R	1 capacitor per domain
$C_{VDDIO\_SMC\_D}$	Decoupling capacitor for I/O domain SMC	100 nF X7R	1 capacitor per 2 domain pins
$C_{VDDIO\_HSIO\_B}$	Bypass capacitor for I/O domain HSIO	2.2 µF X7R	1 capacitor per domain
$C_{VDDIO\_HSIO\_D}$	Decoupling capacitor for I/O domain HSIO	100 nF X7R	1 capacitor per 2 domain pins
$C_{VDDA\ B}$	Bypass capacitor for VDDA	4.7 µF X7R	1 capacitor per domain
$C_{VDDA\ D}$	Decoupling capacitor for VDDA	100 nF X7R	1 capacitor per domain pin
C_{VREFH_B}	Bypass capacitor for ADC VREFH	2.2 µF X7R	1 capacitor per domain. Optional Required only if a separate analog reference supply is used
C_{VREFH_D}	Decoupling capacitor for ADC VREFH	100 nF X7R	1 capacitor per 2 domain pins
F_{VDDA_ADC}	Ferrite bead for FPD VDDA	742792645	1 EMI suppression ferrite bead Optional: In total, 470 Ω DC in series

20 Appendix B – Analog supply

Figure 58 and Figure 59 show the difference between an ideal analog supply without any parasitic elements and a real analog supply with the parasitic elements in the power rail and in the filter capacitors.

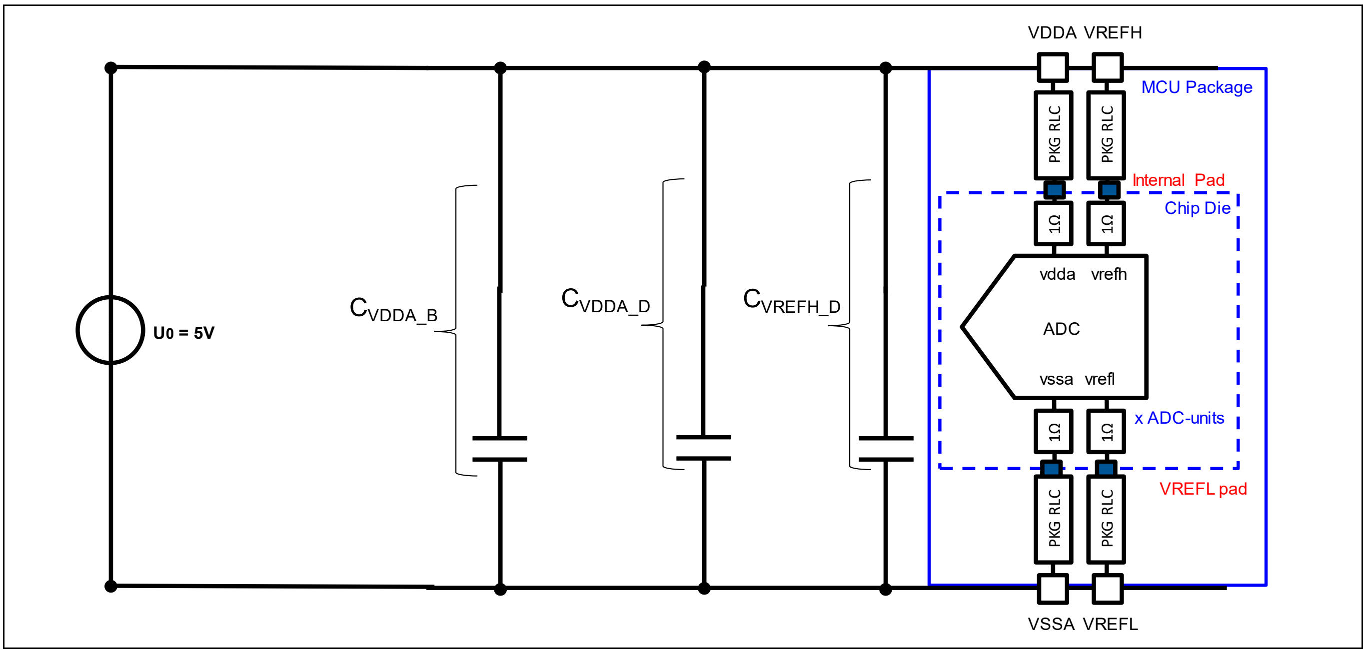


Figure 58 Ideal analog power supply

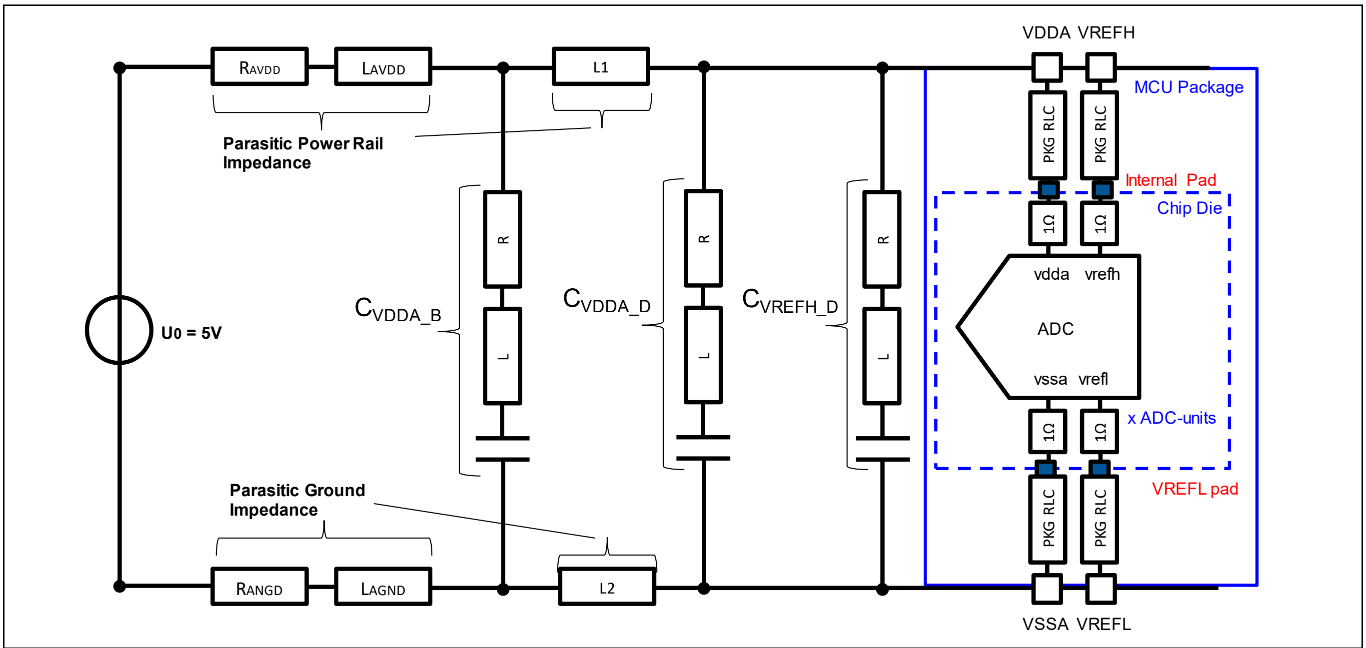


Figure 59 Real analog power supply

21 Appendix C – Oscillator layout

Generic oscillator layout proposals are given for several packages.

Note: *The recommendations for layout design do not guarantee the correct component ratio or follow any PCB design rules. You may need to make changes for different packages.*

21.1 QFP packages

A generic proposal for an oscillator layout with the QFP package is shown in Figure 60.

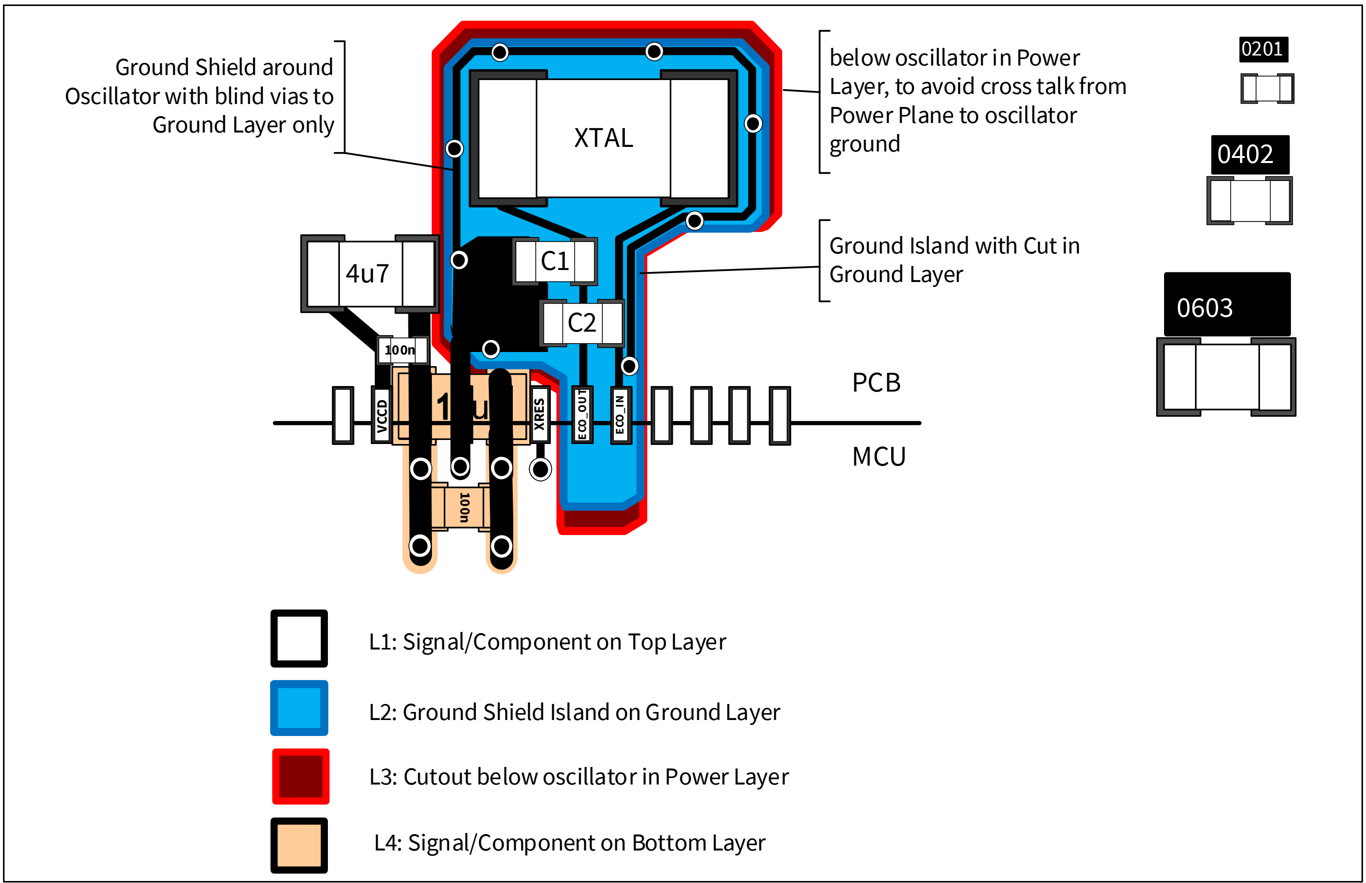


Figure 60 Oscillator layout proposal for CYT2B, CYT3B, and CYT4B series QFP packages

21.2 BGA packages

Figure 61 shows a recommended oscillator layout with the BGA package.

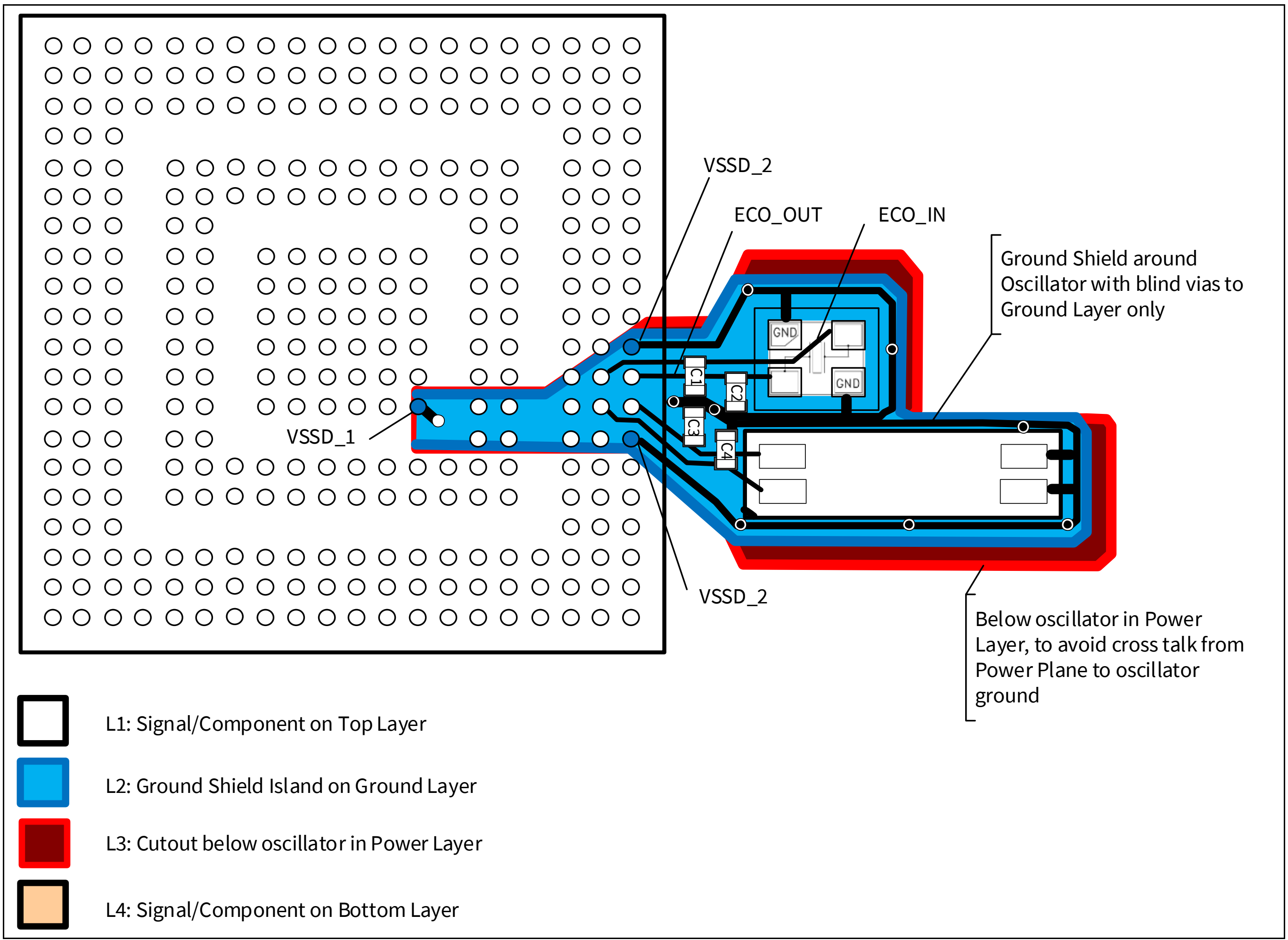


Figure 61 Oscillator layout proposal for BGA packages (based on CYT4B series 320-BGA package)

22 Appendix D – Active regulator inrush current

As a part of the dimensioning of bypass capacitors at the VDDD domain, the external voltage regulator, the PCB parasitic (ESR and ESL) of that power rail, and the maximum current consumption of the active regulator (internal LDO) must be considered. The fastest inrush current transient into the active regulator is shown for:

- MCUs with a maximum of 150-mA internal LDO operation current (CYT2)
- MCUs with a maximum of 300-mA internal LDO operation current (CYT3/CYT4/CYT6)

Note: If the max. DC current is too small, check the max. overcurrent limitation and/or cover the rest with bypass capacitors.

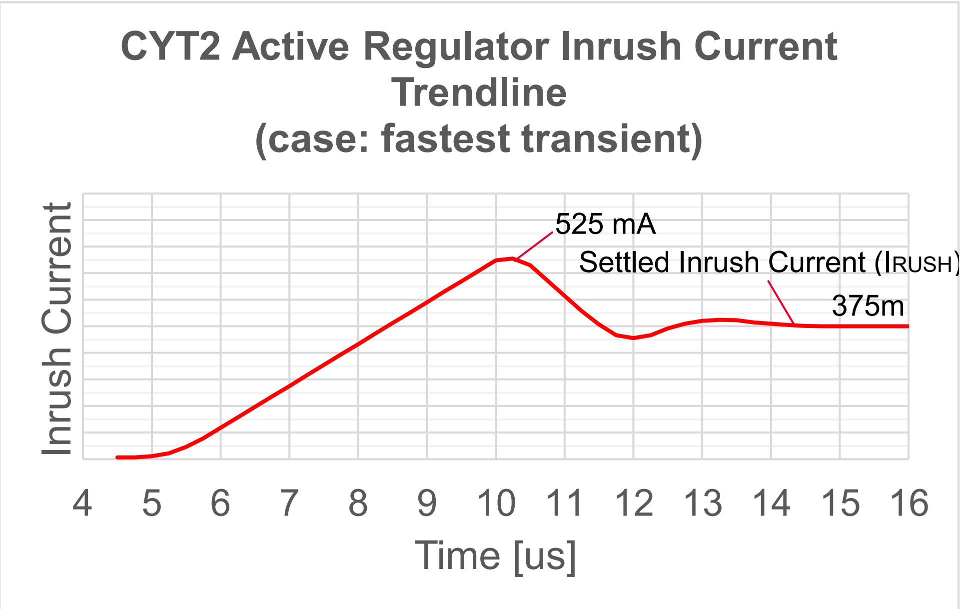


Figure 62 CYT2 active regulator inrush current in the worst-case scenario

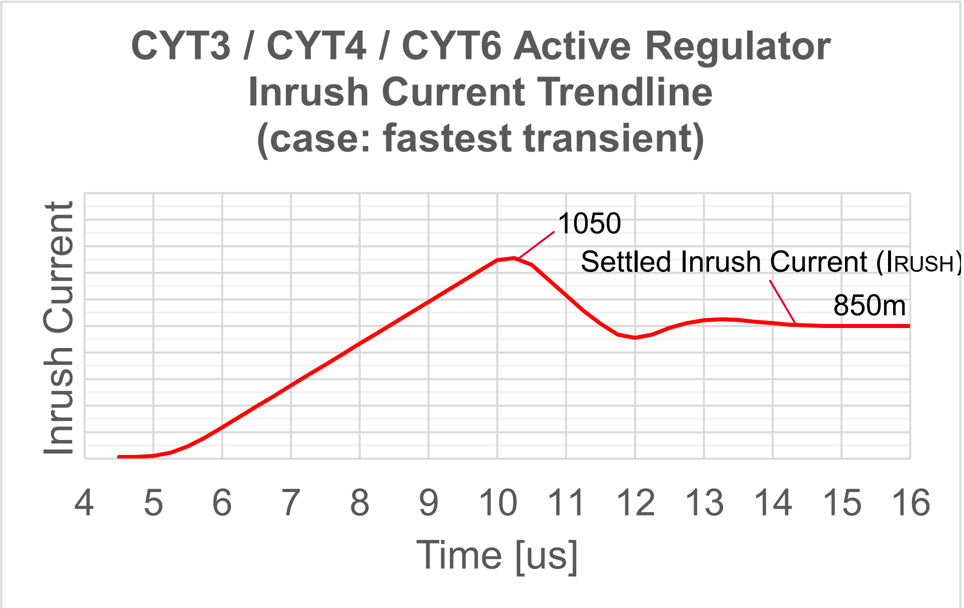


Figure 63 **CYT3/CYT4/CYT6 active regulator inrush current in the worst-case scenario**

23 Appendix E – Unused power domain handling

23.1 Introduction

This section explains how to handle unused power domains and their I/O port pins. It does not consider the transition requirements for different power modes, that is, the power ON/OFF sequencing. With reference to I/O port pin handling, make sure that the ECU peripherals are in proper states during power mode transitions. See Unused power domains to learn how to handle permanently unused power domains that cannot be grounded. See Port input/unused pins: for details on I/O pin handling.

23.2 CYT2B series

Table 23 Unused domain handling of CYT2B series

Power domain	Voltage operation range	Permanent unused domain (active mode)				DeepSleep mode			Hibernate		
		Can be switched OFF? [Yes/No]	Power pin handling[48]	I/O pin handling[48]	Remarks	Can be switched OFF? [Yes/No]	I/O pin handling[48]	Remarks	Can be switched OFF? [Yes/No]	I/O pin handling[48]	Remarks
VDDD (always-on)	2.7 - 5.5 V	No	–	–	–	No	–	–	No	–	–
VCCD	1.09 - 1.21 V	No	–	–	–	No	–	–	–	–	–
VDDA_ADC	2.7 - 5.5 V	No	–	–	–	Yes	–	Disable BOD reset before DeepSleep	Yes	–	–
VDDA_VREFH	2.7 - 5.5 V	Yes	Tie to GND	–	–	Yes	–	–	Yes	–	–
VDDIO_1	2.7 - 5.5 V	No	–	–	–	No	–	–	No	Disable	–
VDDIO_2	2.7 - 5.5 V	No	–	–	–	Yes	Disable	–	Yes	Disable	–

[48] Explanation on pin handling (for details on unused I/O port pins, see Port input/unused pins):

- Tie to GND: Direct connection to GND. Floating levels must be avoided due to Latch-up (LU) risk.
- Open pin: Pin stays open, no wiring. Exception in power save modes.
- Pull Down: External resistor pulled down to GND.
- Disable: Disable the input buffer and disable the output.
- "-": N/A

Table 24 The power domains to which Debug/Boundary Scan pins belong of CYT2B series

Debug pin name	64-LQFP	80-LQFP	100-LQFP	144-LQFP	176-LQFP
SWJ_TRSTN	VDDD	VDDD	VDDD	VDDD	VDDD
SWJ_SWO_TDO	VDDD	VDDD	VDDD	VDDD	VDDD
SWJ_SWCLK_TCLK	VDDD	VDDD	VDDD	VDDD	VDDD
SWJ_SWDIO_TMS	VDDD	VDDD	VDDD	VDDD	VDDD
SWJ_SWDOE_TDI	VDDD	VDDD	VDDD	VDDD	VDDD

23.3 CYT3B/4B/6B series

Table 25 Unused domain handling of CYT3B/4B/6B series

Power domain	Voltage operation range	Permanent unused domain (active mode)				DeepSleep mode			Hibernate		
		Can be switched OFF? [Yes/No]	Power pin handling[49]	I/O pin handling [49]	Remarks	Can be switched OFF? [Yes/No]	I/O pin handling [49]	Remarks	Can be switched OFF? [Yes/No]	I/O pin handling [49]	Remarks
VDDD (always-on)	2.7 - 5.5 V	No	–	–	–	No	–	–	No	–	–
VCCD	1.09 - 1.21 V	No	–	–	–	No	–	–	–	–	–
VDDA_ADC	2.7 - 5.5 V	No	–	–	–	Yes	–	Disable BOD reset before DeepSleep	Yes	–	–
VDDA_VREFH	2.7 - 5.5 V	Yes	Tie to GND	–	–	Yes	–	–	Yes	–	–
VDDIO_1	2.7 - 5.5 V	Yes	Tie to GND	Tie to GND, open pin	–	Yes	Disable	–	Yes	Disable	–

[49] Explanation on pin handling (for details on unused I/O port pins, see Port input/unused pins):

- Tie to GND: Direct connection to GND. Floating levels must be avoided due to latch-up (LU) risk.
- Open pin: Pin stays open, no wiring. Exception in power save modes.
- Pull Down: External resistor pulled down to GND.
- Disable: Disable the input buffer and disable the output.
- "-": N/A

Power domain	Voltage operation range	Permanent unused domain (active mode)				DeepSleep mode			Hibernate		
		Can be switched OFF? [Yes/No]	Power pin handling[49]	I/O pin handling [49]	Remarks	Can be switched OFF? [Yes/No]	I/O pin handling [49]	Remarks	Can be switched OFF? [Yes/No]	I/O pin handling [49]	Remarks
VDDIO_2	2.7 - 5.5 V	No	–	-	–	Yes	Disable	–	Yes	Disable	–
VDDIO_3	2.7 - 3.6 V	Yes	Tie to GND	Tie to GND, open pin	–	Yes	Disable	–	Yes	Disable	–
VDDIO_4	2.7 - 3.6 V	Yes	Tie to GND	Tie to GND, open pin	N/A in all packages	Yes	Disable	–	Yes	Disable	–

Table 26 The power domains to which Debug/Boundary Scan pins belong of CYT3B/4B/6B series

Debug pin name	100-TEQFP	144-TEQFP	176-TEQFP	272-BGA	320-BGA
SWJ_TRSTN	VDDD	VDDD	VDDD	VDDD	VDDD
SWJ_SWO_TDO	VDDD	VDDD	VDDD	VDDD	VDDD
SWJ_SWCLK_TCLK	VDDD	VDDD	VDDD	VDDD	VDDD
SWJ_SWDIO_TMS	VDDD	VDDD	VDDD	VDDD	VDDD
SWJ_SWDOE_TDI	VDDD	VDDD	VDDD	VDDD	VDDD

23.4 CYT3D Series

Table 27 Unused domain handling of CYT3D series

Power domain	Voltage operation range	Permanent unused domain (active mode)				DeepSleep mode			Hibernate		
		Can be switched OFF? [Yes/No]	Power pin handling[50]	I/O pin handling [50]	Remarks	Can be switched OFF? [Yes/No]	I/O pin handling [50]	Remarks	Can be switched OFF? [Yes/No]	I/O pin handling [50]	Remarks
VDDD (always-on)	2.7 - 5.5 V	No	–	–	–	No	–	–	No	–	–

[50] Explanation on pin handling (for details on unused I/O port pins, see Port input/unused pins):

- Tie to GND: Direct connection to GND. Floating levels must be avoided due to latch-up (LU) risk.
- Open pin: Pin stays open, no wiring. Exception in power save modes.

Power domain	Voltage operation range	Permanent unused domain (active mode)				DeepSleep mode			Hibernate		
		Can be switched OFF? [Yes/No]	Power pin handling[50]	I/O pin handling [50]	Remarks	Can be switched OFF? [Yes/No]	I/O pin handling [50]	Remarks	Can be switched OFF? [Yes/No]	I/O pin handling [50]	Remarks
VCCD	1.09 - 1.21 V	No	–	–	–	No	–	–	–	–	–
VDDA_FPD	1.09 - 1.21 V	No	–	Dedicated port pins	–	No	Disable IP	–	–	Disable IP	–
VDDPLL_FPD	1.09 - 1.21 V	No	–	Dedicated port pins	–	No	Disable IP	–	–	Disable IP	–
VDDA_MIPI	1.09 - 1.21 V	Yes	Tie to GND	Dedicated port pins	–	Yes	Disable IP	–	Yes	Disable IP	–
VDDHA_FPD	3.0 – 3.6 V	No	–	–	–	Yes	Disable IP	–	Yes	Disable IP	–
VDDIO_HSIO	3.0 – 3.6 V	Yes	Tie to GND	Tie to GND, open pin, pull down	–	Yes	Disable	–	Yes	Disable	–
VDDA_DAC	3.0 – 3.6 V	Yes	Tie to GND	Dedicated port pins	–	Yes	Disable IP	–	Yes	Disable IP	–
VDDA_ADC	2.7 - 5.5 V	No	–	–	–	Yes	–	Disable BOD reset before DeepSleep	Yes	–	–
VDDA_VREFH	2.7 - 5.5 V	Yes	–	–	–	Yes	–	–	Yes	–	–
VDDIO_GPIO1	2.7 - 5.5 V	Yes	Tie to GND	Tie to GND, open pin, pull down	–	Yes	Disable	–	Yes	Disable	–
VDDIO_GPIO2	2.7 - 5.5 V	Yes	Tie to GND	Tie to GND, open pin, pull down	–	Yes	Disable	–	Yes	Disable	–

- Pull Down: External resistor pulled down to GND.
- Disable: Disable the input buffer and disable the output.
- "-": N/A

Power domain	Voltage operation range	Permanent unused domain (active mode)				DeepSleep mode			Hibernate		
		Can be switched OFF? [Yes/No]	Power pin handling[50]	I/O pin handling [50]	Remarks	Can be switched OFF? [Yes/No]	I/O pin handling [50]	Remarks	Can be switched OFF? [Yes/No]	I/O pin handling [50]	Remarks
VDDIO_SMC	2.7 - 5.5 V	Yes	Tie to GND	Tie to GND, open pin, pull down	–	Yes	Disable	–	Yes	Disable	–

Table 28 The power domains to which Debug/Boundary Scan pins belong of CYT3D series

Debug pin name	216-TEQFP	272-BGA
SWJ_TRSTN	VDDIO_GPIO_1	VDDIO_GPIO_1
SWJ_SWO_TDO	VDDIO_GPIO_1	VDDIO_GPIO_1
SWJ_SWCLK_TCLK	VDDIO_GPIO_1	VDDIO_GPIO_1
SWJ_SWDIO_TMS	VDDIO_GPIO_1	VDDIO_GPIO_1
SWJ_SWDOE_TDI	VDDIO_GPIO_1	VDDIO_GPIO_1

23.5 CYT4D Series

Table 29 Unused domain handling of CYT4D series

Power domain	Voltage operation range	Permanent unused domain (active mode)				DeepSleep mode			Hibernate		
		Can be switched OFF? [Yes/No]	Power pin handling[51]	I/O pin handling [51]	Remarks	Can be switched OFF? [Yes/No]	I/O pin handling[51]	Remarks	Can be switched OFF? [Yes/No]	I/O pin handling [51]	Remarks
VDDD (always-on)	2.7 - 5.5 V	No	–	–	–	No	–	–	No	–	–
VCCD	1.09 - 1.21 V	No	–	–	–	No	–	–	–	–	–
VDDA_FPD	1.09 - 1.21 V	No	–	Dedicated port pins	–	No	Disable IP	–	–	Disable IP	–
VDDPLL_FPD	1.09 - 1.21 V	No	–	Dedicated port pins	–	No	Disable IP	–	–	Disable IP	–
VDDA_MIPI	1.09 - 1.21 V	Yes	Tie to GND	Dedicated port pins	–	Yes	Disable IP	–	Yes	Disable IP	–
VDDHA_FPD	3.0 – 3.6 V	No	–	–	–	Yes	Disable IP	–	Yes	Disable IP	–
VDDIO_HSIO	3.0 – 3.6 V	Yes	Tie to GND	Tie to GND, open pin, pull down	–	Yes	Disable	–	Yes	Disable	–
VDDA_DAC	3.0 – 3.6 V	Yes	Tie to GND	Dedicated port pins	–	Yes	Disable IP	–	Yes	Disable IP	–

[51] Explanation on pin handling (for details on unused I/O port pins, see Port input/unused pins):

- Tie to GND: Direct connection to GND. Floating levels must be avoided due to latch-up (LU) risk.
- Open pin: Pin stays open, no wiring. Exception in power save modes.
- Pull Down: External resistor pulled down to GND.
- Disable: Disable the input buffer and disable the output.
- "-": N/A

Power domain	Voltage operation range	Permanent unused domain (active mode)				DeepSleep mode			Hibernate		
		Can be switched OFF? [Yes/No]	Power pin handling[51]	I/O pin handling [51]	Remarks	Can be switched OFF? [Yes/No]	I/O pin handling[51]	Remarks	Can be switched OFF? [Yes/No]	I/O pin handling [51]	Remarks
VDDA_ADC	2.7 - 5.5 V	No	–	–	–	Yes	–	Disable BOD reset before Deep-Sleep	Yes	–	–
VDDA_VREFH	2.7 - 5.5 V	Yes	–	–	–	Yes	–	–	Yes	–	–
VDDIO_GPIO1	2.7 - 5.5 V	Yes	Tie to GND	Tie to GND, open pin, pull down	–	Yes	Disable	–	Yes	Disable	–
VDDIO_GPIO2	2.7 - 5.5 V	Yes	Tie to GND	Tie to GND, open pin, pull down	–	Yes	Disable	–	Yes	Disable	–
VDDIO_SMC	2.7 - 5.5 V	Yes	Tie to GND	Tie to GND, open pin, pull down	–	Yes	Disable	–	Yes	Disable	–
VDDIO_SMIF_HV	3.0 – 3.6 V	Yes	Tie to GND	–	–	Yes	-	See DS > SID40D/DA.	Yes	–	See DS > SID40D/DA
VDDIO_SMIF	1.7- 2.0 V	Yes	Tie to GND	Tie to GND, open pin, pull down	–	Yes	Disable		Yes	Disable	

Table 30 The power domains to which Debug/Boundary Scan pins belong of CYT4D series

Debug pin name	327-BGA
SWJ_TRSTN	VDDIO_GPIO_1
SWJ_SWO_TDO	VDDIO_GPIO_1
SWJ_SWCLK_TCLK	VDDIO_GPIO_1
SWJ_SWDIO_TMS	VDDIO_GPIO_1
SWJ_SWDOE_TDI	VDDIO_GPIO_1

23.6 CYT4E Series

Table 31 Unused domain handling of CYT4E series

Power domain	Voltage operation range	Permanent unused domain (active mode)				DeepSleep mode			Hibernate		
		Can be switched off? [Yes/No]	Power pin handling [51]	I/O pin handling [52]	Remarks	Can be switched off? [Yes/No]	I/O pin handling [51]	Remarks	Can be switched off? [Yes/No]	I/O pin handling [51]	Remarks
VDDD (always-on)	2.7 - 5.5 V	No	–	–	–	No	–	–	No	–	–
VCCD	1.09 - 1.21 V	No	–	–	–	No	–	–	–	–	–
VDDA_FPD0	1.09 - 1.21 V	No	–	Dedicated port pins	–	No	Disable IP	–	–	Disable IP	–
VDDA_FPD1	1.09 - 1.21 V	No	–	Dedicated port pins	–	No	Disable IP	–	–	Disable IP	–
VDDPLL_FPD 0	1.09 - 1.21 V	No	–	Dedicated port pins	–	No	Disable IP	–	–	Disable IP	–
VDDPLL_FPD 1	1.09 - 1.21 V	No	–	Dedicated port pins	–	No	Disable IP	–	–	Disable IP	–
VDDA_MIPI	1.09 - 1.21 V	Yes	Tie to GND	Dedicated port pins	–	Yes	Disable IP	–	Yes	Disable IP	–
VDDHA_FPD0	3.0 – 3.6 V	No	–	–	–	Yes	Disable IP	–	Yes	Disable IP	–
VDDHA_FPD1	3.0 – 3.6 V	No	–	–	–	Yes	Disable IP	–	Yes	Disable IP	–

[52] Explanation on pin handling (for details on unused I/O port pins, see Port input/unused pins):

- Tie to GND: Direct connection to GND. Floating levels must be avoided due to latch-up (LU) risk.
- Open pin: Pin stays open, no wiring. Exception in power save modes.
- Pull Down: External resistor pulled down to GND.
- Disable: Disable the input buffer and disable the output.
- “-“: N/A

Power domain	Voltage operation range	Permanent unused domain (active mode)				DeepSleep mode			Hibernate		
		Can be switched off? [Yes/No]	Power pin handling [51]	I/O pin handling [52]	Remarks	Can be switched off? [Yes/No]	I/O pin handling [51]	Remarks	Can be switched off? [Yes/No]	I/O pin handling [51]	Remarks
VDDIO_HSIO	3.0 – 3.6 V	Yes	Tie to GND	Tie to GND, open pin, pull down	–	Yes	Disable	–	Yes	Disable	–
VDDA_DAC	3.0 – 3.6 V	Yes	Tie to GND	Dedicated port pins	–	Yes	Disable IP	–	Yes	Disable IP	–
VDDA	2.7 - 5.5 V	No	–	–	–	Yes	–	Disable BOD reset before Deep-Sleep	Yes	–	–
VREFH	2.7 - 5.5 V	Yes	–	–	–	Yes	–	–	Yes	–	–
VDDIO_GPIO1	2.7 - 5.5 V	Yes	Tie to GND	Tie to GND, open pin, pull down	–	Yes	Disable	–	Yes	Disable	–
VDDIO_GPIO2	2.7 - 5.5 V	Yes	Tie to GND	Tie to GND, open pin, pull down	–	Yes	Disable	–	Yes	Disable	–

Power domain	Voltage operation range	Permanent unused domain (active mode)				DeepSleep mode			Hibernate		
		Can be switched off? [Yes/No]	Power pin handling [51]	I/O pin handling [52]	Remarks	Can be switched off? [Yes/No]	I/O pin handling [51]	Remarks	Can be switched off? [Yes/No]	I/O pin handling [51]	Remarks
VDDIO_SMC	2.7 - 5.5 V	Yes	Tie to GND	Tie to GND, open pin, pull down	–	Yes	Disable	–	Yes	Disable	–
VDDIO_SMIF_HV	3.0 – 3.6 V	Yes	Tie to GND	–	–	Yes	–	See DS > SID40D/DA.	Yes	–	See DS > SID40D/DA
VDDIO_SMIF_1	1.7 - 1.95 V, 3.0 - 3.6 V	Yes	Tie to GND	Tie to GND, open pin, pull down	–	Yes	Disable		Yes	Disable	
VDDIO_SMIF_2	1.7 - 1.95 V, 3.0 - 3.6 V	Yes	Tie to GND	Tie to GND, open pin, pull down	–	Yes	Disable		Yes	Disable	
VDDO_LPDDR4	1.06 – 1.17 V (typical 1.1 V)	No	–	–	–	No	–	–	No	–	–

Table 32 The power domains to which Debug/Boundary Scan pins belong of CYT4E series

Debug pin name	500-BGA
SWJ_TRSTN	VDDIO_GPIO_2
SWJ_SWO_TDO	VDDIO_GPIO_2
SWJ_SWCLK_TCLK	VDDIO_GPIO_2
SWJ_SWDIO_TMS	VDDIO_GPIO_2
SWJ_SWDOE_TDI	VDDIO_GPIO_2

23.7 CYT2C Series

Table 33 Unused domain handling of CYT2C series

Power domain	Voltage operation range	Permanent unused domain (active mode)				DeepSleep mode			Hibernate		
		Can be switched OFF? [Yes/No]	Power pin handling [51]	I/O pin handling [53]	Remarks	Can be switched off? [Yes/No]	I/O pin handling [51]	Remarks	Can be switched off? [Yes/No]	I/O pin handling [51]	Remarks
VDDD (always-on)	2.7 - 5.5 V	No	–	–	–	No	–	–	No	–	–
VCCD	1.05 - 1.15 V	No	–	–	–	No	–	–	–	–	–
VDDIO_HSIO	3.0 – 3.6 V	Yes	Tie to GND	Tie to GND, open pin, pull down	–	Yes	Disable	–	Yes	Disable	–

[53] Explanation on pin handling (for details on unused I/O port pins, see Port input/unused pins):

- Tie to GND: Direct connection to GND. Floating levels must be avoided due to latch-up (LU) risk.
- Open pin: Pin stays open, no wiring. Exception in power save modes.
- Pull Down: External resistor pulled down to GND.
- Disable: Disable the input buffer and disable the output.
- "-": N/A

Power domain	Voltage operation range	Permanent unused domain (active mode)				DeepSleep mode			Hibernate		
		Can be switched OFF? [Yes/No]	Power pin handling [51]	I/O pin handling [53]	Remarks	Can be switched off? [Yes/No]	I/O pin handling [51]	Remarks	Can be switched off? [Yes/No]	I/O pin handling [51]	Remarks
VDDA_ADC	2.7 - 5.5 V	No	–	–	–	Yes	–	Disable BOD reset before Deep-Sleep	Yes	–	–
VDDA_VREFH	2.7 - 5.5 V	Yes	–	–	–	Yes	–	–	Yes	–	–
VDDIO_GPIO	2.7 - 5.5 V	Yes	Tie to GND	Tie to GND, open pin, pull down	–	Yes	Disable	–	Yes	Disable	–
VDDIO_SMC	2.7 - 5.5 V	Yes	Tie to GND	Tie to GND, open pin, pull down	–	Yes	Disable	–	Yes	Disable	–

Table 34 The power domains to which Debug/Boundary Scan pins belong of CYT2C series

Debug pin name	144-LQFP	176-LQFP
SWJ_TRSTN	VDDIO_GPIO	VDDIO_GPIO
SWJ_SWO_TDO	VDDIO_GPIO	VDDIO_GPIO
SWJ_SWCLK_TCLK	VDDIO_GPIO	VDDIO_GPIO
SWJ_SWDIO_TMS	VDDIO_GPIO	VDDIO_GPIO
SWJ_SWDOE_TDI	VDDIO_GPIO	VDDIO_GPIO

24 Appendix F – Power supply filter characteristics

As part of a second-order LPF, a ferrite bead is deployed instead of an inductor. This appendix shows a ferrite bead specification example.

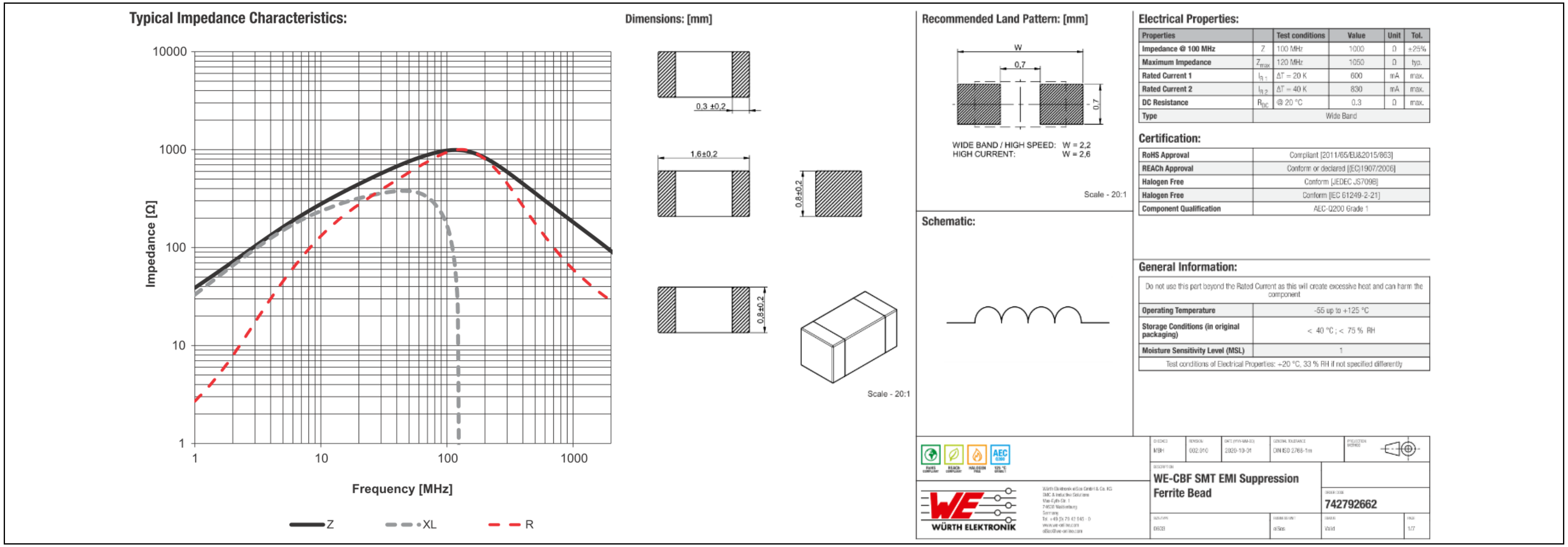


Figure 64 **Ferrite bead specification example**

25 Appendix G – Clamping structure of I/O pins with shared analog functions

As described in Clamping structure of I/O pins with shared analog functions, the clamping structure for different I/O domains with shared analog function are different. Power dependencies and power sequencing are not considered here.

25.1 Introduction

The tables below consider following:

- I/O domain supply requirement of the SARMUX[x] of an ADC unit
- the clamping structure of the I/O domains port pins with shared analog functions

The number of SARMUXes is independent of the ADC units. Therefore, it is possible in principle, to sense analog sources via other SARMUXes, instead via the one within the same ADC unit. The SARMUX[x] I/O domain should be powered with the same voltage level as the ADC, as soon as one of the case variants (one-of-x) is fulfilled. The same consideration (one-of-x) must be done for the I/O pin supplies PD_1 and PD_2. Hereby it is helpful to make use of sorting the table accordingly, because the case variants are sorted to SARMUX[x].

25.2 CYT2B and CYT3B/4B/6B series

Table 35 Clamping structure of I/O pins with shared analog functions within CYT2B and CYT3B/4B/6B[54]

Case	SARMUX[x]:		Used analog sensing path: (input range: 0 V – VDDA)	Clamping diode stages of Power Domain:			Power Pin Requirement "same as" VDDA_ADC[55]:	
	Instance	Domain		PD_1 (GPIO stage)	PD_2 (ADC MUX stage)	PD_3 (SAR MUX stage)	PD_1, PD_2 Domain	SARMUX[x] Domain
1.1.A	0	VDDIO_1	No port pin (only digital)	VDDIO_1	–	VDDA	No	No
1.1.B	0	VDDIO_1	ADC[0]_M pins	VDDIO_1	–	VDDA	Yes	Yes
1.1.C	0	VDDIO_1	ADC[0]_M pin (P11) via AUXMUX	VDDIO_2	VDDA	VDDA	Yes	Yes
1.2	0	VDDIO_1	Internal via AUXMUX (except ADC[x]_M)	–	–	VDDA	–	Yes
2.1.A	1	VDDIO_2	PD_1 I/O pins except P11: No port pin (only digital) (P11: unused Pins -> open)	VDDIO_2	–	VDDA	No	No
2.1.B	1	VDDIO_2	PD_1 I/O pins except P11: ADC[1]_M (P11: unused Pins -> open)	VDDIO_2	–	VDDA	Yes	Yes
2.1.B	1	VDDIO_2	P11 (ADC[x]_M): No port pin (only digital)	VDDIO_2	VDDA	VDDA	No	No
2.1.C	1	VDDIO_2	ADC[1]_M (P11) via AUXMUX	VDDIO_2	VDDA	VDDA	Yes	Yes
2.2	2	VDDIO_2	Internal via AUXMUX (except ADC[x]_M)	–	–	VDDA	–	Yes
3.1.A	2	VDDD	No port pin (digital only)	VDDD	–	VDDA	No	No
3.1.B	2	VDDD	ADC[2]_M pins	VDDD	–	VDDA	Yes	Yes
3.1.C	2	VDDD	ADC[2]_M pin (P11)	VDDIO_2	VDDA	VDDA	Yes	Yes

54 The I/Os in VDDIO_1 domain are referred to the VDDD domain in 64-LQFP package.

55 Implementation of power rail voltage levels for the dedicated I/O domains and the ADC supply must be compliant with the other power sequencing requirements mentioned in the device datasheet.

Case	SARMUX[x]:		Used analog sensing path: (input range: 0 V – VDDA)	Clamping diode stages of Power Domain:			Power Pin Requirement "same as" VDDA_ADC[55]:	
	Instance	Domain		PD_1 (GPIO stage)	PD_2 (ADC MUX stage)	PD_3 (SAR MUX stage)	PD_1, PD_2 Domain	SARMUX[x] Domain
3.2	2	VDDD	Internal via AUXMUX (except ADC[x]_M)	–	–	VDDA	–	Yes

25.3 CYT3D series

Table 36 Clamping structure of I/O pins with shared analog functions within CYT3D

Case	SARMUX[x]:		Used analog sensing path: (input range: 0 V – VDDA)	Clamping diode stages of Power Domain:			Power Pin Requirement "same as" VDDA_ADC[56]:	
	Instance	Domain		PD_1 (GPIO stage)	PD_2 (ADC MUX stage)	PD_3 (SAR MUX stage)	PD_1, PD_2 Domain	SARMUX[x] IO Domain
1.1.A	0	VDDIO_GPIO1	No port pin (only digital)	VDDIO_GPIO1	–	VDDA	No	No
1.1.B	0	VDDIO_GPIO1	ADC[0]_M pins	VDDIO_GPIO1	–	VDDA	Yes	Yes
1.2.A	0	VDDIO_GPIO1	No port pin (only digital)	VDDIO_GPIO2	VDDIO_GPIO1	VDDA	No	No
1.2.B	0	VDDIO_GPIO1	ADC[0]_M pins	VDDIO_GPIO2	VDDIO_GPIO1	VDDA	Yes	Yes
1.3	0	VDDIO_GPIO1	Internal via AUXMUX	–	–	VDDA	–	Yes
2.1.A	1	VDDIO_SMC	No port pin (only digital)	VDDIO_SMC	–	VDDA	No	No
2.2.B	1	VDDIO_SMC	ADC[1]_M pins	VDDIO_SMC	–	VDDA	Yes	Yes

[56] Implementation of power rail voltage levels for the dedicated I/O domains and the ADC supply must be compliant with the other power sequencing requirements mentioned in the device datasheet.

25.4 CYT4D series

Table 37 Clamping structure of I/O pins with shared analog functions within CYT4D

Case	SARMUX[x]:		Used analog sensing path: (input range: 0V – VDDA)	Clamping diode stages of Power Domain:			Power Pin Requirement “same as” VDDA_ADC[57]:	
	Instance	Domain		PD_1 (GPIO stage)	PD_2 (ADC MUX stage)	PD_3 (SAR MUX stage)	PD_1, PD_2 Domain	SARMUX[x] IO Domain
1.1.A	0	VDDIO_GPIO2	No port pin (only digital)	VDDIO_GPIO2	–	VDDA	No	No
1.1.B	0	VDDIO_GPIO2	ADC[0]_M pins	VDDIO_GPIO2	–	VDDA	Yes	Yes
1.2.A	0	VDDIO_GPIO2	No port pin (only digital)	VDDIO_GPIO1	VDDIO_GPIO2	VDDA	No	No
1.2.B	0	VDDIO_GPIO2	ADC[0]_M pins	VDDIO_GPIO1	VDDIO_GPIO2	VDDA	Yes	Yes
1.3	0	VDDIO_GPIO2	Internal via AUXMUX	–	–	VDDA	Yes	Yes
1.3.A	1	VDDIO_SMC	No port pin (digital only)	VDDIO_SMC	–	VDDA	No	No
1.3.B	1	VDDIO_SMC	ADC[1]_M pins	VDDIO_SMC	–	VDDA	Yes	Yes

[57] Implementation of power rail voltage levels for the dedicated I/O domains and the ADC supply must be compliant with the other power sequencing requirements mentioned in the device datasheet.

25.5 CYT4E series

Table 38 Clamping structure of I/O pins with shared analog functions within CYT4E

Case	SARMUX[x]:		Used analog sensing path: (input range: 0V – VDDA)	Clamping diode stages of Power Domain:			Power Pin Requirement “same as” VDDA_ADC[58]:	
	Instance	Domain		PD_1 (GPIO stage)	PD_2 (ADC MUX stage)	PD_3 (SAR MUX stage)	PD_1, PD_2 Domain	SARMUX[x] IO Domain
1.1.A	0	VDDIO_GPIO2	No port pin (only digital)	VDDIO_GPIO2	–	VDDA	No	No
1.1.B	0	VDDIO_GPIO2	ADC[0]_M pins	VDDIO_GPIO2	–	VDDA	Yes	Yes
1.2.A	0	VDDIO_GPIO2	No port pin (only digital)	VDDIO_GPIO1	VDDIO_GPIO2	VDDA	No	No
1.2.B	0	VDDIO_GPIO2	ADC[0]_M pins	VDDIO_GPIO1	VDDIO_GPIO2	VDDA	Yes	Yes
1.3	0	VDDIO_GPIO2	Internal via AUXMUX	–	–	VDDA	Yes	Yes
1.3.A	1	VDDIO_SMC	No port pin (digital only)	VDDIO_SMC	–	VDDA	No	No
1.3.B	1	VDDIO_SMC	ADC[1]_M pins	VDDIO_SMC	–	VDDA	Yes	Yes

[58] Implementation of power rail voltage levels for the dedicated I/O domains and the ADC supply must be compliant with the other power sequencing requirements mentioned in the device datasheet.

25.6 CYT2C series

Table 39 Clamping structure of I/O pins with shared analog functions within CYT2C

Case	SARMUX[x]:		Used analog sensing path: (input range: 0V – VDDA)	Clamping diode stages of Power Domain:			Power Pin Requirement "same as" VDDA_ADC[59]:	
	Instance	Domain		PD_1 (GPIO stage)	PD_2 (ADC MUX stage)	PD_3 (SAR MUX stage)	PD_1, PD_2 Domain	SARMUX[x] IO Domain
1.1.A	0	VDDIO_GPIO	No port pin (only digital)	VDDIO_GPIO	–	VDDA	No	No
1.1.B	0	VDDIO_GPIO	ADC[0]_M pins	VDDIO_GPIO	–	VDDA	Yes	Yes
1.2	0	VDDIO_GPIO	Internal via AUXMUX	–	–	VDDA	–	Yes
2.1.A	1	VDDIO_SMC	No port pin (only digital)	VDDIO_SMC	–	VDDA	No	No
2.1.B	1	VDDIO_SMC	ADC[1]_M pins	VDDIO_SMC	–	VDDA	Yes	Yes

[59] Implementation of power rail voltage levels for the dedicated I/O domains and the ADC supply must be compliant with the other power sequencing requirements mentioned in the device datasheet.

26 Related documents

- AN227076 – TRAVEO™ T2G bootloader
- AN234261 – Ethernet design guide for TRAVEO™ T2G family
- AN230194 – Setting ECO parameters
- AN224153 – Design and layout guide for SEMPER™ NOR flash memory
- AN233447 – Power filter options for FPD-Link interfaces for the TRAVEO™ T2G family
- AN79938 – Design guidelines for Infineon® ball grid array (BGA) packaged devices
- AN202751 – Surface mount assembly recommendations for Infineon FBGA packages
- AN213250 – Power filter options for FPD-Link interfaces
- AN226698 – TRAVEO™ T2G: External power supply design guide
- AN220118 – Getting started with TRAVEO™ T2G family MCUs
- AN72845 – Design guidelines for QFN packaged devices
- AN89611 – PSOC™ 3 and PSoC™ 5LP getting started with chip scale packages
- AN80994 – Design considerations for electrical fast transient (EFT) immunity
- AN57821 – PSOC™ 3, PSOC™ 4, and PSOC™ 5LP mixed signal circuit board layout considerations
- AN220222 – Low-power mode procedure in the TRAVEO™ T2G family
- ARM_Link_01 – CoreSight components technical reference manual (Cortex® debug connector detailed specification in Appendix C)
- ARM_Link_02 – Cortex®-M debug connectors
- SRAM board design guidelines
- Device datasheet
  - CYT2B6 datasheet 32-bit Arm® Cortex®-M4F microcontroller TRAVEO™ T2G family
  - CYT2B7 datasheet 32-bit Arm® Cortex®-M4F microcontroller TRAVEO™ T2G family
  - CYT2B9 datasheet 32-bit Arm® Cortex®-M4F microcontroller TRAVEO™ T2G family
  - CYT2BL datasheet 32-bit Arm® Cortex®-M4F microcontroller TRAVEO™ T2G family
  - CYT2CL datasheet 32-bit Arm® Cortex®-M4F microcontroller TRAVEO™ T2G family
  - CYT3BB/4BB datasheet 32-bit Arm® Cortex®-M4F microcontroller TRAVEO™ T2G family
  - CYT3DL datasheet 32-bit Arm® Cortex®-M4F microcontroller TRAVEO™ T2G family
  - CYT4BF datasheet 32-bit Arm® Cortex®-M7 microcontroller TRAVEO™ T2G family
  - CYT4DN datasheet 32-bit Arm® Cortex®-M7 microcontroller TRAVEO™ T2G family
  - CYT4EN datasheet 32-bit Arm® Cortex®-M7 microcontroller TRAVEO™ T2G family
  - CYT6BJ datasheet 32-bit Arm® Cortex®-M7 microcontroller TRAVEO™ T2G family
- Technical reference manual for body controller entry family
  - TRAVEO™ T2G automotive body controller entry family architecture technical reference manual (TRM)
  - TRAVEO™ T2G automotive body controller entry registers technical reference manual (TRM) for CYT2B7
  - TRAVEO™ T2G automotive body controller entry registers technical reference manual (TRM) for CYT2B9
- Technical reference manual for body controller high family
  - TRAVEO™ T2G automotive body controller high family architecture technical reference manual (TRM)
  - TRAVEO™ T2G automotive body controller high registers technical reference manual (TRM) for CYT3BB/4BB

Related documents

  - TRAVEO™ T2G automotive body controller high registers technical reference manual (TRM) for CYT4BF
- Technical reference manual for cluster 2D family
  - TRAVEO™ T2G automotive cluster 2D family architecture technical reference manual (TRM)
  - TRAVEO™ T2G automotive cluster 2D registers technical reference manual (TRM) for CYT3DL
  - TRAVEO™ T2G automotive cluster 2D registers technical reference manual (TRM) for CYT4DN
  - TRAVEO™ T2G automotive cluster 2D registers technical reference manual (TRM) for CYT4EN (Doc. No. 002-32087)
- Technical reference manual for cluster entry family
  - TRAVEO™ T2G automotive cluster entry family architecture technical reference manual (TRM)
  - TRAVEO™ T2G automotive cluster entry registers technical reference manual (TRM) for CYT2CL

Contact Technical support to obtain TRAVEO™ T2G family series datasheets and technical reference manuals.

Revision history

Document revision	Date	Description of changes
**	2017-11-27	New application note.

*A	2019-08-19	• Remove section Minimum System
		• Removed Figure 1
		• Replaced Figure 23, Figure 24, and Figure 42
		• Updated Section 6.2 Power supply monitoring
		• Changed 19 from Minimum Device System to Power Supply Concept
		• Added 20 and 21
		• Moved Oscillator Design Proposal to 21
		• Add CYT4D series Parts Number
		  – Updated Table 1, Table 2, and Table 3
		  – Updated Figure 27 to Figure 29
		  – Added Figure 30 to Figure 42
		  – Added Table 15
		• Deleted CYT3B series Parts Number
		Deleted 6.1 Analog Input Pins

*B	2019-12-18	• Updated External core supply control, 5-V-tolerant input pins, Related documents • Updated Appendix 19.4, A.1 • Corrected Table 13 • Updated Figure 28 • Added section Clamping structure of I/O pins with shared analog functions Added Section 13 ADC
*C	2020-05-28	• Updated Appendix: all "*External Component Integration*" tables, A.1 • New linked documents in Related documents • Added section: Assembly and package-related PCB design, Appendix D – Active regulator inrush current, Unused power domains • Updated section: Power ON/OFF sequence of power supply domains
*D	2020-12-18	• Added sections: Unused power domains, Appendix E – Unused power domain handling, FPD-link • Updated sections: Power ON/OFF sequence of power supply domains, Debug interface, Port input/unused pins, Clamping structure of I/O pins with shared analog functions • Updated: Figure 20, Figure 21, and Figure 43
*E	2021-04-27	• Updated to Infineon template • Minor changes: ADC, • Charge balancing between CEXT and CVIN • Updated:

Revision history

Document revision	Date	Description of changes
		– Figure 18, Figure 42, Figure 43, Figure 44 – Table 8, Table 13, Table 15 – Clamping structure of I/O pins with shared analog functions – Quartz crystal placement and signal routing, Related documents, Appendix D – Active regulator inrush current, Appendix E – Unused power domain handling, Ground and power supply, Clock system Added: Table 7, Audio-DAC, CYT3D series with TEQFP package, FPD-link, Port pin configuration in AUTOSAR MCAL, Table 32, Table 34 •
*F	2021-10-21	• Minor changes: CYT3B/4B/6B series with TEQFP package, Quartz crystal placement and signal routing, and changed from upper case to lower case in whole document • Updated: – Abbreviations, Appendix A – Power supply concept, Appendix E – Unused power domain handling, Clamping structure of I/O pins with shared analog functions, Clock system, Ground and power supply, Related documents, RGB interface, Power domains • Added: Video interface, Appendix G – Clamping structure of I/O pins with shared analog functions
*G	2022-03-09	• Minor changes: – CYT3B/4B/6B series with BGA package, Power supply variants, Table 11, Table 13, Table 25 • Update: – ADC, Appendix A – Power supply concept, Appendix E – Unused power domain handling, Clamping structure of I/O pins with shared analog functions, Dedicated port pins, FPD-link, Related documents, Quartz crystal placement and signal routing, Thermal considerations, Table 15, Table 19, Table 27 • Added: – MIPI, Trace width, Table 29 • Restructured/moved: • Audio-DAC
*H	2023-02-22	• Updated: • Appendix A – Power supply concept, Appendix E – Unused power domain handling, Appendix G – Clamping structure of I/O pins with shared analog functions
*I	2023-07-03	• Minor updates
*J	2023-08-17	• Added support for CYT6B series:

Revision history

Document revision	Date	Description of changes
		• Appendix A – Power supply concept, Appendix E – Unused power domain handling, Appendix G – Clamping structure of I/O pins with shared analog functions
*K	2024-03-11	• Common filter proposal including footnote update for: F_{VDDA_FPD}, F_{VDDPLL_FPD}, F_{VDDHA_FPD}, F_{VDDA_MIPI} • Typo correction: $F_{BVDDPLL\_FPD}$ -> F_{VDDPLL_FPD} • Appendix G – Clamping structure of I/O pins with shared analog functions • EXT_MUX removed, because itself no analog function
*L	2024-07-26	• Added support for CYT6B series: – Appendix D – Active regulator inrush current – Added CYT6 series • Added support for CYT2C series: – Appendix A – Power supply concept - Added section 20.9 CYT2C series with BGA package – Appendix E – Unused power domain handling - Added section 24.7 CYT2C Series – Appendix G – Clamping structure of I/O pins with shared analog functions • Added Section 26.6 CYT2C Series • Updated Related documents section
*M	2025-04-15	• Added a note and page links in "9. Debug Interface" • Fixed garbled characters in notes in "12. Thermal considerations" • Fixed table format about Table 10. Audio-DAC output load and C_{COM} specification • Added below tables in "23. Appendix E - Unused power domain handling" – Table 24. The power domains to which Debug/Boundary Scan pins belong of CYT2B series – Table 26. The power domains to which Debug/Boundary Scan pins belong of CYT3B/4B/6B series – Table 28. The power domains to which Debug/Boundary Scan pins belong of CYT3D series – Table 30. The power domains to which Debug/Boundary Scan pins belong of CYT4D series – Table 32. The power domains to which Debug/Boundary Scan pins belong of CYT4E series – Table 34. The power domains to which Debug/Boundary Scan pins belong of CYT2C series • Added a sentence to notes 34 and 39
*N	2025-12-17	• Added 48-QFN package in sections 2.1, 19.3, and Table 12 • Replaced LIN with LIN responder and added footnote [1] in Table 1

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

PSOC™, formerly known as PSoC™, is a trademark of Infineon Technologies. Any references to PSoC™ in this document or others shall be deemed to refer to PSOC™.

Edition 2025-12-17

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference

002-20270 Rev. *N