240 W USB-PD evaluation board with PFC + hybrid flyback combo IC XDP™ XDPS2222

EVAL_XDPS2222_240W1

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Scope and purpose

This document presents information about the 240 W USB-PD (power delivery) evaluation board, using a novel XDP™ digital power XDPS2222 for power factor correction (PFC) + hybrid-flyback (HFB), a CoolGaN™ device IGLD60R190D1 as the main switch, a CoolMOS™ device IPP60R070CFD7 as the PFC switch, and EZ-PD™ CCG3PA CYPD3175 for USB-PD extended power range (EPR) control. The document includes the key waveforms and performance data.

Intended audience

Users of the 240 W evaluation board, design engineers of PFC + HFB converters using the XDP™ XDPS2222.

Keywords

XDP™ digital power, PFC + HFB, combo controller, XDP™ XDPS2222, CoolGaN™, CoolMOS™, IGLD60R190D1, IPP60R070CFD7, EZ-PD™ CCG3PA CYPD3175, USB-PD controller, charger, adapter.

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Table 1 Safety precautions

	Warning: *The DC-link potential of this board is up to 1000 V DC. When measuring voltage waveforms by oscilloscope, high-voltage differential probes must be used. Failure to do so may result in personal injury or death.*
	Warning: *The evaluation or reference board contains DC bus capacitors, which take time to discharge after removal of the main supply. Before working on the drive system, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	Warning: *The evaluation or reference board is connected to the grid input during testing. Hence, high-voltage differential probes must be used when measuring voltage waveforms by oscilloscope. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	Warning: *Remove or disconnect power from the drive before you disconnect or reconnect wires, or perform maintenance work. Wait five minutes after removing power to discharge the bus capacitors. Do not attempt to service the drive until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.*
	Caution: *The heatsink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	Caution: *Only personnel familiar with the drive, power electronics and associated machinery should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	Caution: *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with ESD control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	Caution: *A drive that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as undersizing the motor, supplying an incorrect or inadequate AC supply, or excessive ambient temperatures may result in system malfunction.*
	Caution: *The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

Table of contents

1 XDP™ XDPS2222 overview

The XDP™ XDPS2222 controller is a highly integrated device including the valley-switching PFC controller, the HFB (hybrid-flyback) controller and three gate drivers for the main switches. The internal handshaking between the PFC and HFB controller and the adaptive bus voltage setting make this controller perfect for applications with wide AC input and very wide output voltage range, such as USB-PD adapters and battery chargers with an output voltage from 5 to 48 V. Detailed information about this control IC can be found in the datasheet [1], but here is a short summary of the product, its main features, the IC pin layout and the main benefits for the customer.

1.1 Product highlights

- Digital combo controller for PFC boost and DC-DC hybrid-flyback in DSO-14 (150 mil) package
- Novel zero voltage switching (ZVS) hybrid-flyback (asymmetrical half-bridge) topology for ultra-high system efficiency
- Integrated gate drivers supporting GaN and Si switches
- 600 V high-voltage start-up cell for fast V_{CC} charging
- Burst mode operation for lowest no-load standby power
- Adaptive PFC bus voltage and PFC enable/disable control to maximize average and light-load efficiency
- Supports extra-wide output voltage range system designs
- Configurable parameters for protection modes and system performance
- Pb-free lead plating, halogen-free (according to IEC61249-2-21), RoHS compliant

1.2 PFC control

- Configurable PFC QRM operation for improved average efficiency
- Pulse skipping for improved light-load efficiency
- Automatic PFC disable/enable control depending on operating conditions
- Adaptive PFC bus voltage level following operating conditions

1.3 Hybrid-flyback control

- Peak current mode control for robust and fast input and load control
- ZVS operation of high-side and low-side switch (with ZVS pulse insertion in DCM)
- Configurable multimode operation for improved average and light-load efficiency

1.4 IC pin layout

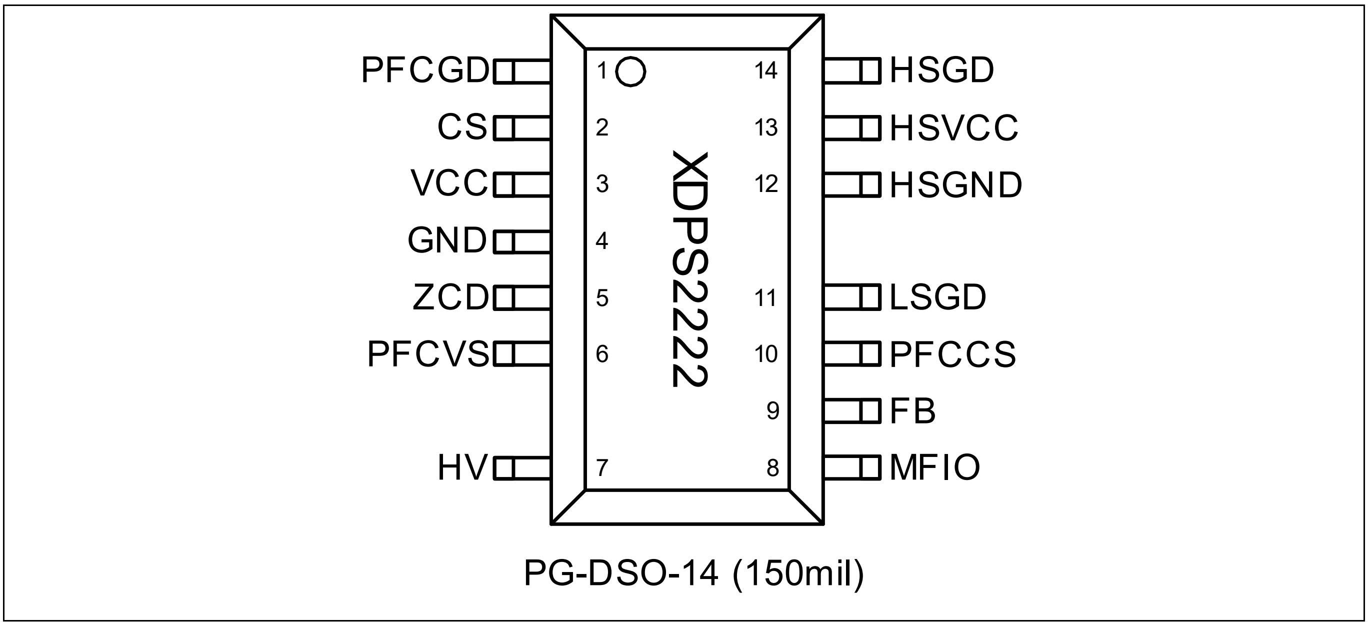


Figure 1 XDP™ XDPS2222 pin layout

1.5 Main customer benefits

1.5.1 Low bill of materials

- PFC + HFB control with gate drivers in one 14-pin DSO package
- Integrated gate drivers for direct driving of both CoolMOS™ and CoolGaN™
- Integrated start-up cell for V_{CC} initial charge-up
- Potential transformer size reduction compared to other flyback topologies

1.5.2 High system performance

- High system efficiency
- High power density design
- Low standby power

1.5.3 Unique controller in the market

- The most suitable controller for applications with wide AC input and wide output voltage range, such as USB-PD EPR adapters and battery chargers
- Embedded digital core supporting configurable parameters for optimum system performance
- Ease of design, enabling platform design approach by using one controller for multiple designs and applications

2 Board hardware

2.1 Overview

The 240 W USB-PD power charger evaluation board EVAL_XDPS2222_240W1 uses the XDP™ digital combo controller XDPS2222, CoolGaN™ device IGLD60R190D1, CoolMOS™ device IPP60R070CFD7 and the EZ-PD™ controller CCG3PA CYPD3175. It targets applications of USB-PD charger adapters, such as smartphones and mobile computers, with a very wide input range and a very wide output voltage range. Figure 2 shows the top view of the complete board system, consisting of a main power board, a half-bridge daughter board, V_{CC} daughter board, synchronous rectification (SR) daughter board and an EPR board. The AC input connection point is the connector at the bottom-left corner, while the board output is the Type-C connector located on the EPR board at the upper-right corner.

For ease of use and further experiments an evaluation board approach which offers highest flexibility and optional assembly variants is used. The evaluation board is not optimized to achieve highest performance, and there is still further room for improvement in the system performance through proper design enhancement.

Figure 2 Evaluation board with daughter boards

2.1.1 Input specifications

Table 2 lists the board input specifications.

Table 2 Electrical requirements: AC input

Parameter	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
AC voltage	V AC	90		264	V_{RMS}	Maximum range
		100		240	V_{RMS}	Operating range
AC frequency	f_{AC}	47		63	Hz	
Power factor			0.98			At 115 V AC, full load
			0.97			At 230 V AC, full load
Brown-in			88		V	
Brown-out			76		V	
X-capacitor discharge time				2	s	

2.1.2 Output specifications

Table 3 lists the board output specifications.

Table 3 Electrical requirements: output specifications

Parameter	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
Output voltage	V_{out}		5		V	Mean value of the standard fixed USB-PD EPR voltages, at 115 and 230 V AC input
			9		V	
			15		V	
			20		V	
			28		V	
			36		V	
			48		V	
Output current	I_{out}	0	3		A	V_{out} = 5 V
		0	5		A	V_{out} greater than 5 V
Start-up time				1.5	s	5 V V_{out} at cold start-up

2.1.3 Key components

The following Infineon components are used on the board.

Table 4 Key components

Item	Component
PFC + HFB controller	XDP™ XDPS2222
USB-PD controller	EZ-PD™ CCG3PA CYPD3175
PFC switch	IPP60R070CFD7
HFB switches	IGLD60R190D1
SR MOSFET	BSC074N15NS5
USB load switch	IPB110P06LM
V_{CC} regulator switch	BSS169

2.1.4 Board and PCB information

Board and PCB information is summarized in Table 5.

Table 5 Board dimensions and power density

Item	Value	Unit
Dimensions	200 x 65 x 24	mm
PCB	2	Layers

2.2 Evaluation board system

The system consists of the main power board, a half-bridge daughter board, V_{CC} supply daughter board, SR daughter board and the USD-PD EPR 48 V daughter board. Both the PFC and HFB stages are controlled by the combo controller XDP™ XDPS2222, one of Infineon's XDP™ digital controllers. At the output side, Infineon's USB-PD EZ-PD™ controller CCG3PA CYPD3175 is used for the communication with the end device and output voltage management. In the following sub-chapters, the schematic of these boards is introduced, while the bills of materials (BOMs) of the boards can be found in Chapter 4.1.

2.2.1 Main power board

The schematic and PCB layout of the main board are shown in Figure 3 to Figure 6. It can be seen that the evaluation board allows for further optimization by providing assembly variants. Not-assembled parts are grayed out in the schematics.

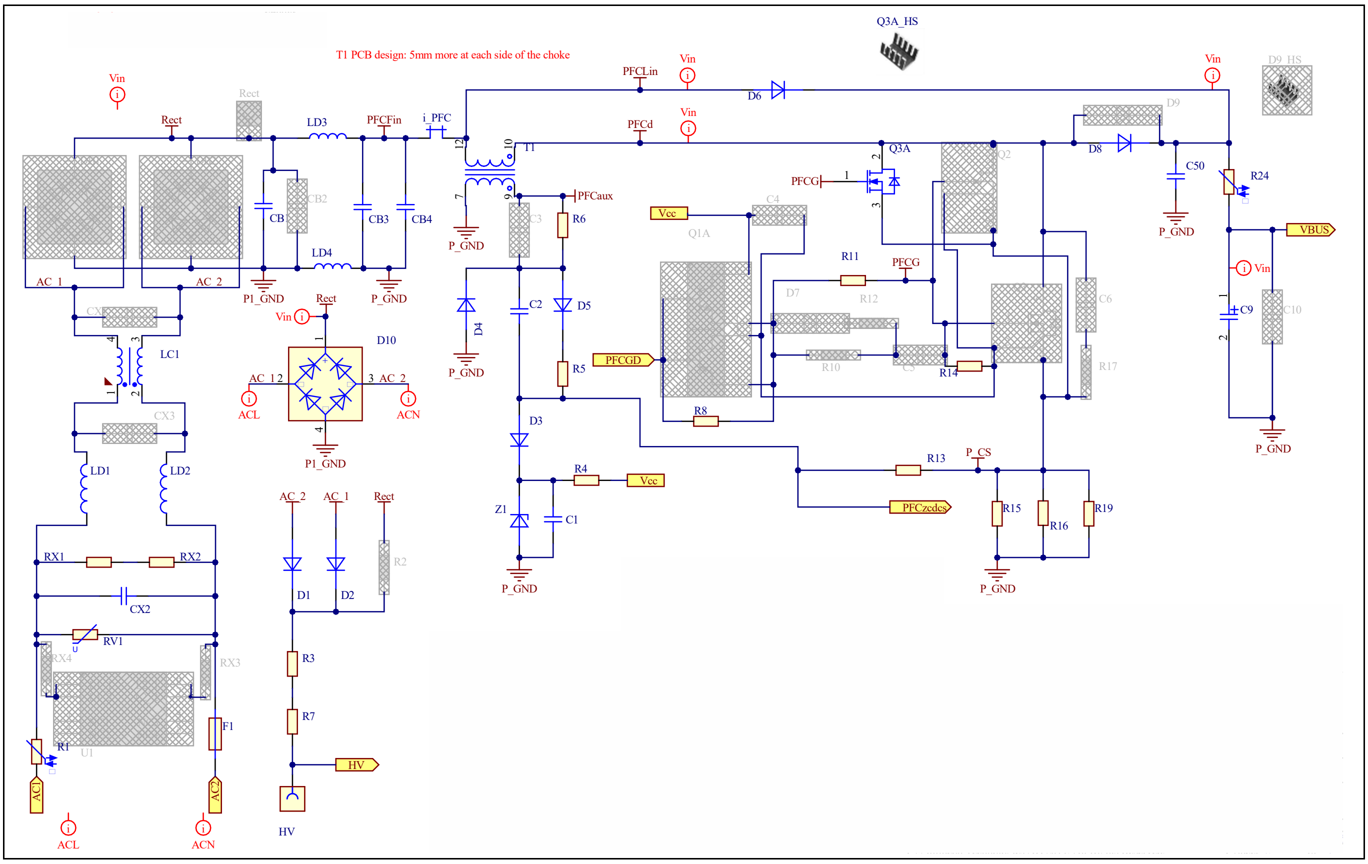


Figure 3 PFC stage schematic

Figure 3 shows the power circuitry of the AC input and PFC stage, including the input protection and EMI filter (RV1, CX2, LC1, D10, CB1, CB2, LD3, LD4, CB3 and CB4; devices LD1 and LD2 are shorted with a wire and therefore shown as "fitted"), and the start-up cell external circuit (D1, D2, R3 and R7). The PFC zero-crossing detection (ZCD) and current sensing (CS) signals are combined into a single signal, PFC_{zcdcs}, which is connected to IC pin PFCCS. The voltage at the PFC auxiliary winding, which is coupled to the PFC main inductance (T1), is processed by the devices R6, D4, D5, R5, C2, D3, Z1, C1 and R4 to generate the ZCD signal, where D4 is for the negative clamping, and the network D3, Z1, C1 and R4 limits the positive voltage of the ZCD signal. Per resistor R13, the ZCD signal is effectively de-coupled from the PFC CS resistors R15, R16 and R19, which provide the CS signal to the control IC. A CoolMOS™ device with attached heatsink is used as the PFC main switch, Q3A, and it is driven directly by the XDP™ XDPS2222 from the PFCGD pin with the external resistor R11.

Note: The grayed-out devices in the schematic are not assembled on the board. In addition, some 0 Ω resistors are prepared for easy component selection.

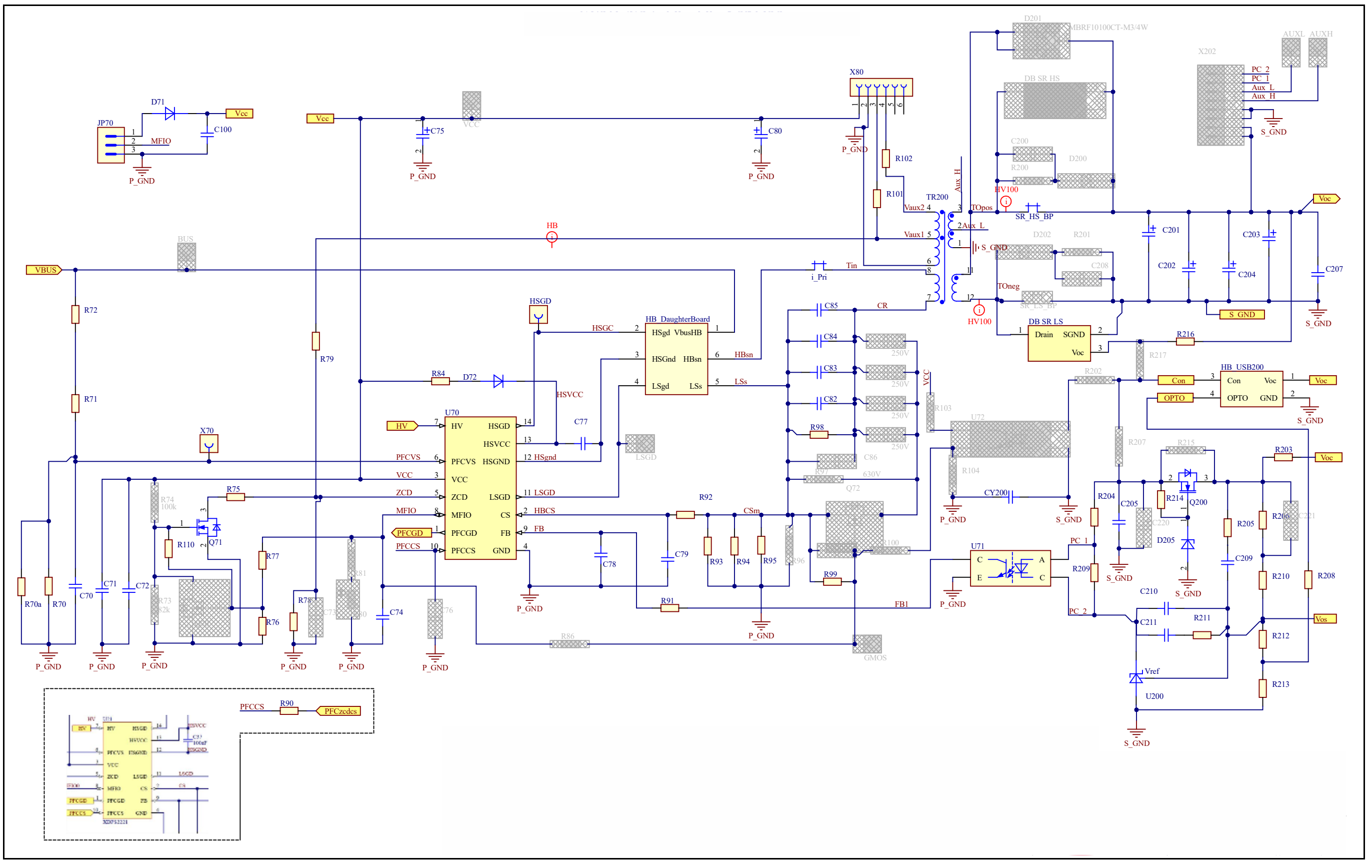


Figure 4 HFB stage schematic

The HFB is based on a half-bridge structure, which is shown in Figure 7. The transformer's TR200 primary winding is connected to the half-bridge switching node at one end and to the resonant capacitors (C82 to C90) at the other end. The shunt resistors (R93 to R95) are used to sense the current through the transformer primary winding for HFB peak current regulation. For accurate switching timing, the signal from the auxiliary winding (Vaux1) is used. It generates a ZCD signal using devices R79 and R78. In case of the given extra-wide output voltage design the ZCD divider ratio is changed during operation depending on the sensed output voltage using devices R110, Q71 and R75. The resistors R70, R70a, R71 and R72 are used for the PFC voltage sensing. Via the connector X80, both voltages from the auxiliary windings Aux1 and Aux2 are provided to the V_{CC} daughter board. The connector JP70 is used for the parameter configuration via UART communication. Figure 7 shows the schematic of the half-bridge including the gate RC network to drive the GaN switches.

To keep system costs low, two-layer PCBs are used for all boards except the USB-PD EPR-board. Figure 5 and Figure 6 show the PCB layout of the main board.

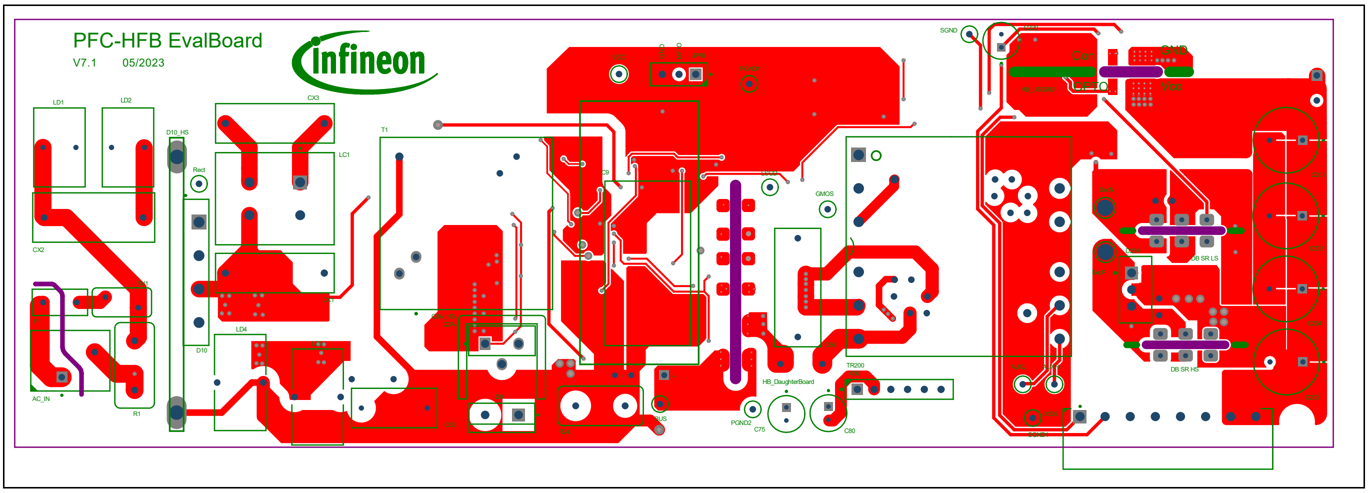


Figure 5 Main board PCB: top side

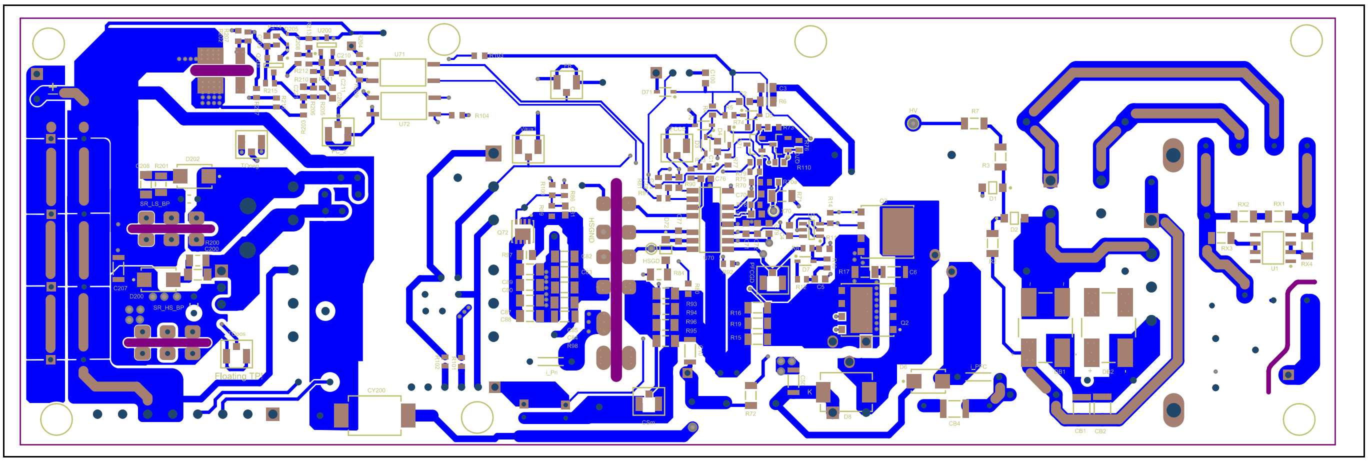


Figure 6 Main board PCB: bottom side

2.2.2 Half-bridge board

The half-bridge is located on a separate daughter board. With this approach, it is easy to evaluate the performance of CoolGaN™ and CoolMOS™ devices by simply exchanging the daughter board. By default, the half-bridge as well as the driver circuit is assembled for CoolGaN™ devices.

The schematic of the half-bridge daughter board is shown in Figure 7.

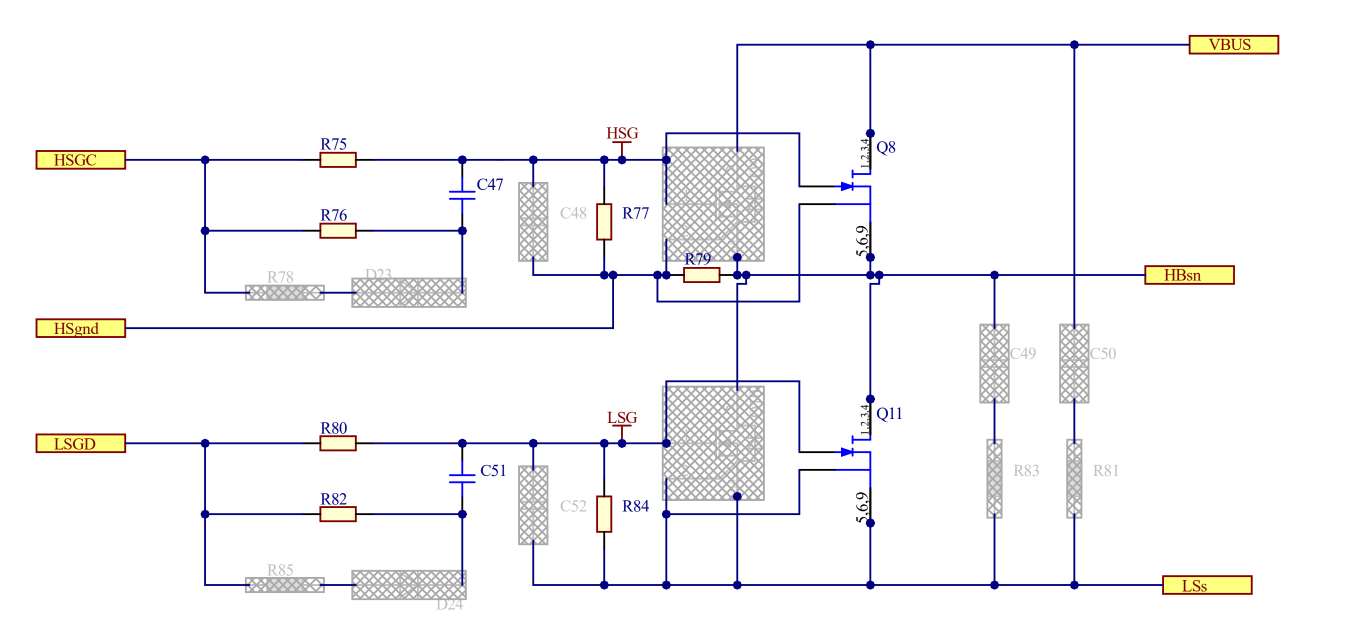


Figure 7 Half-bridge and gate RC network schematic

The PCB design for this board is shown in Figure 8.

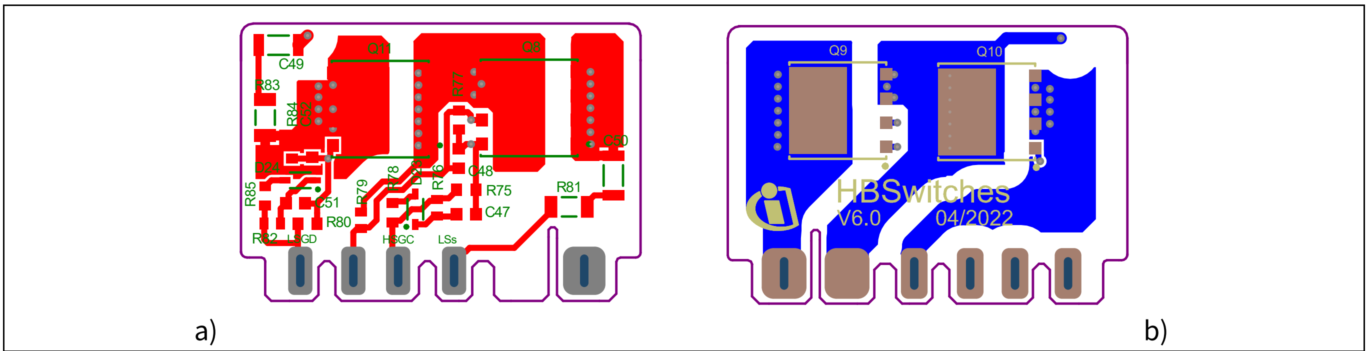


Figure 8 PCB of the half-bridge board: a) top side and b) bottom side

2.2.3 V_{CC} board

At cold start-up, the V_{CC} supply is provided via the resistors connected to the HV pin. The charging current is controlled by the start-up cell. During normal operation, the V_{CC} supply is ensured by the V_{CC} daughter board. Figure 9 shows the schematic of the V_{CC} board.

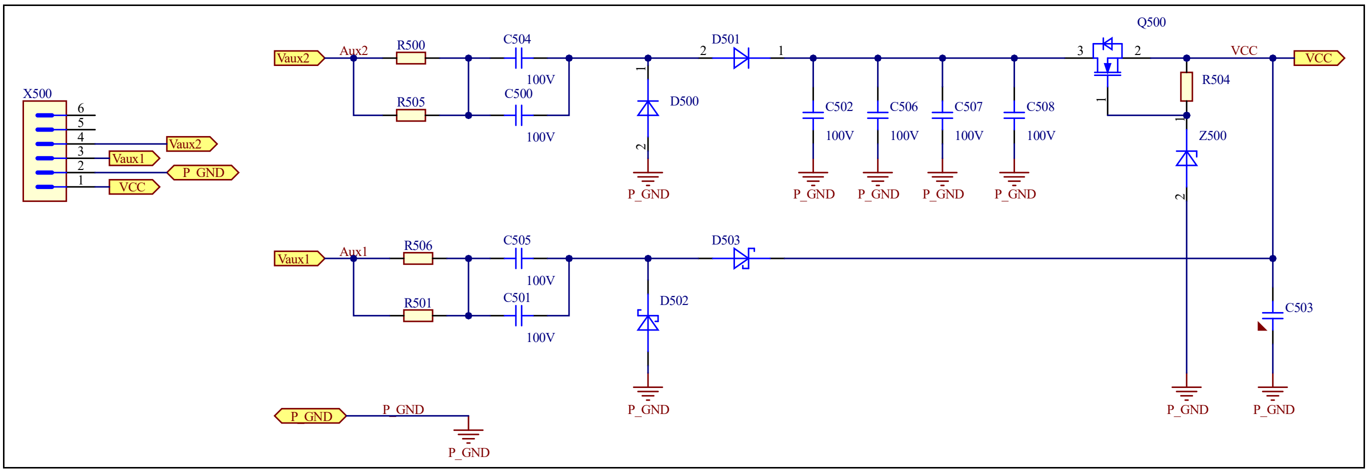


Figure 9 V_{CC} **board schematic**

The V_{CC} supply circuit is based on the charge-pump concept. With this concept, the IC supply is coupled to the HFB input voltage, but independent of the HFB output voltage. For efficient V_{CC} generation, two auxiliary windings are implemented. At high HFB input voltage, energy is transferred from Vaux1, while at low HFB input voltage Vaux2 is used. The PCB design for this board is shown in Figure 10.

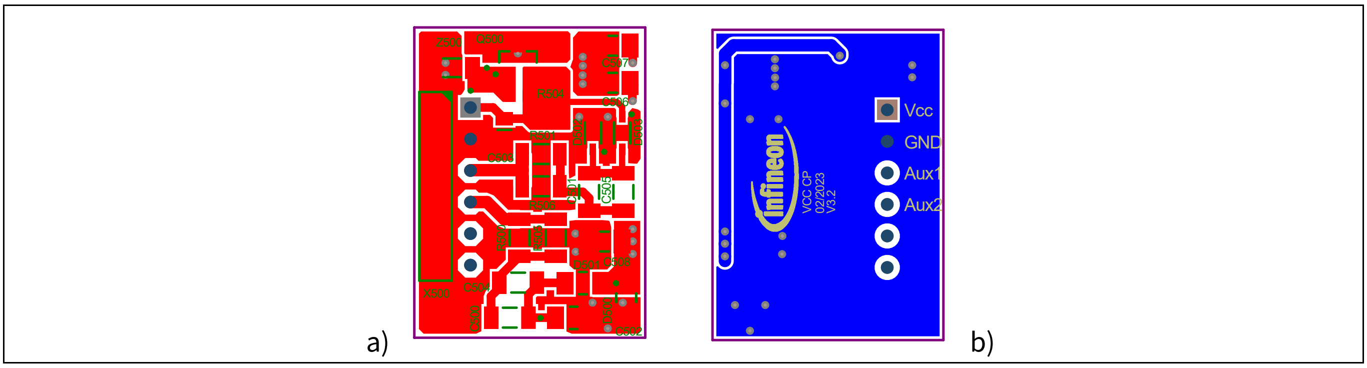


Figure 10 **PCB of the** V_{CC} **board: a) top side and b) bottom side**

2.2.4 Synchronous rectification board

At the secondary side, the output voltage is rectified by the SR circuitry, while the USB-PD daughter board controls the shunt regulator (U200) reference voltage and therefore the output voltage. The schematic of the SR daughter board is shown in Figure 11. The PCB design for this board is shown in Figure 12.

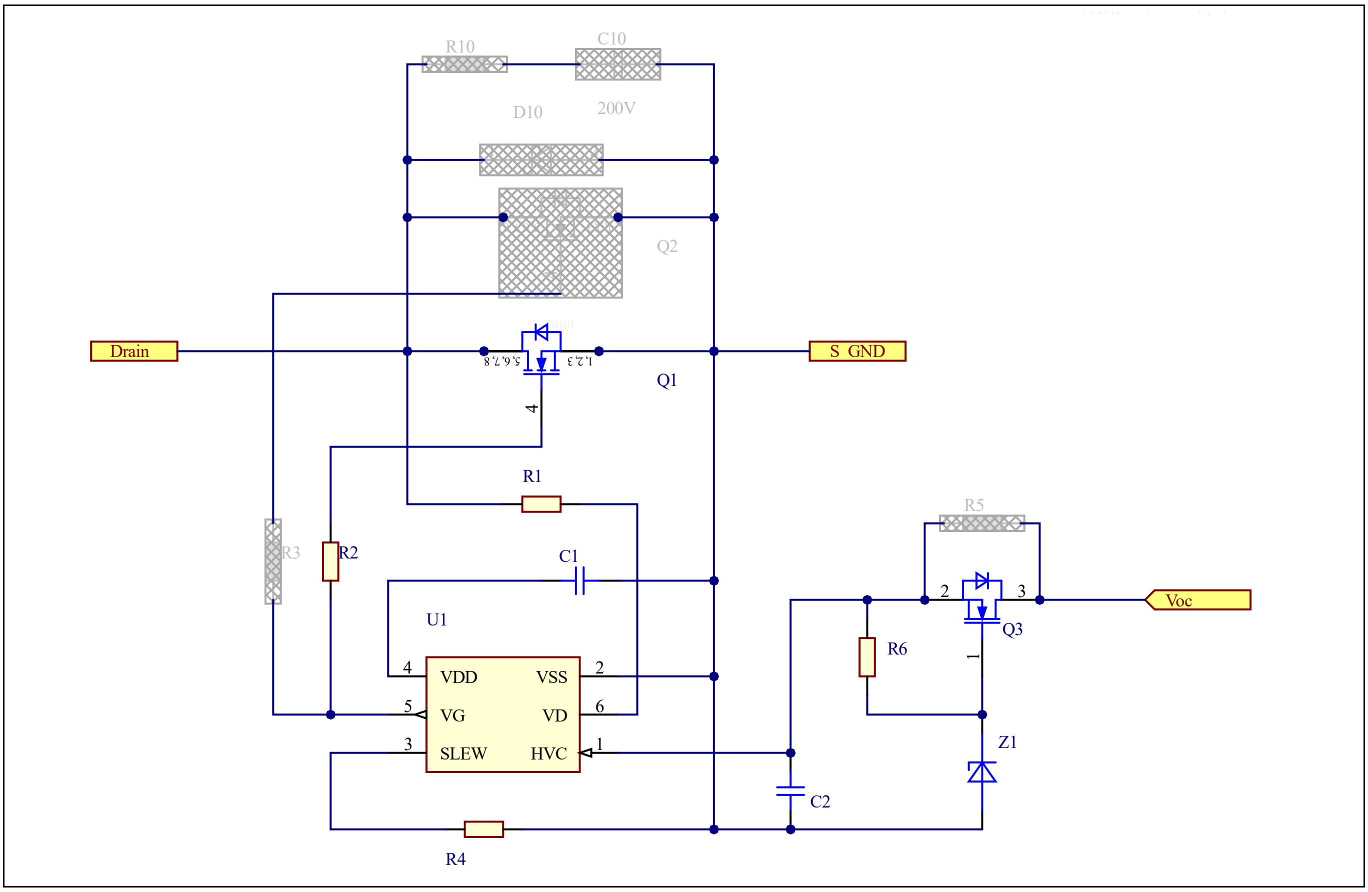


Figure 11 SR schematic

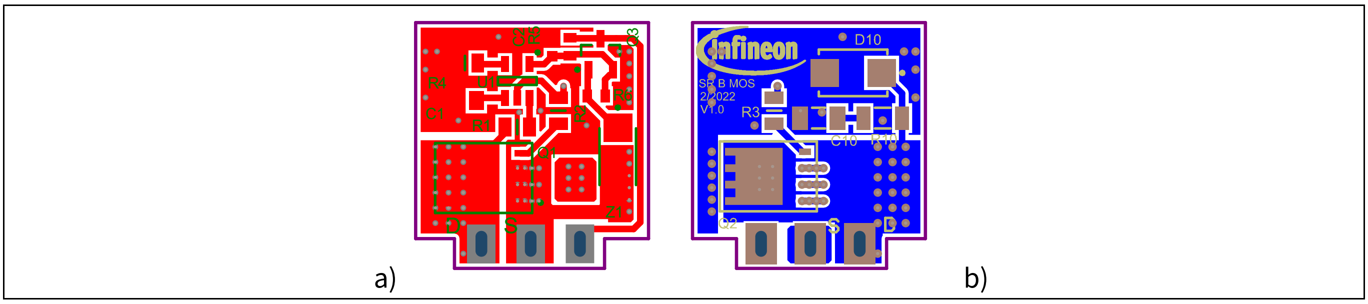


Figure 12 PCB of the V_{CC} board: a) top side and b) bottom side

2.2.5 EPR board

The EPR board is based on the EZ-PD™ controller CYPD3175, as shown in Figure 13.

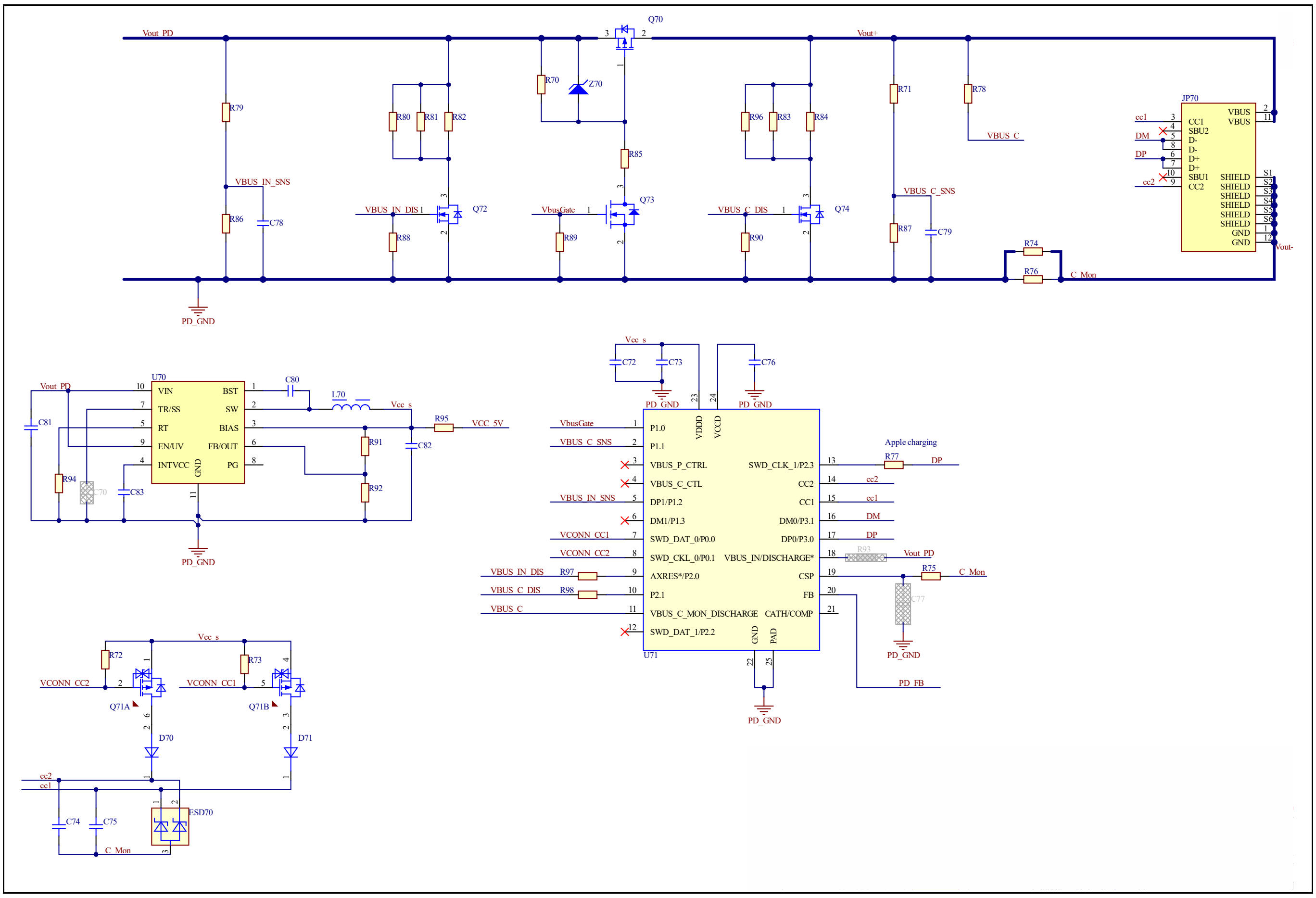


Figure 13 EPR board schematic

A buck converter (U70) is used to generate the required supply voltage for the controller CYPD3175. The circuit consisting of Q71A, Q71B, D70, D71, R72 and R73 provides the required voltage at the communication lines CC1 and CC2. The controller CYPD3175 senses both the input voltage V_{out_PD} (V_{BUS_IN} from the point of view of the EPR board) and output voltage (V_{OUT+}), where the "on" or "off" of the output voltage at the Type-C connector is controlled by the load switch Q70. The output current at the Type-C connector is sensed by shunt resistors R74 and R76, filtered by the elements of R75 and C77, and then fed to the PD control IC. The controller CYPD3175 communicates with the end device via the communication lines CC1 and CC2, sets the output voltage level of the HFB accordingly through the signal PD_FB, and controls the load switch Q70 for supplying the end device. For the output voltage falling transition, the bus discharge paths before and after the safety switch (R80, R81, R82, Q72 and R83, R84, R96, Q74) may be activated by the PD controller. The PCB layout of the EPR board is shown in Figure 14.

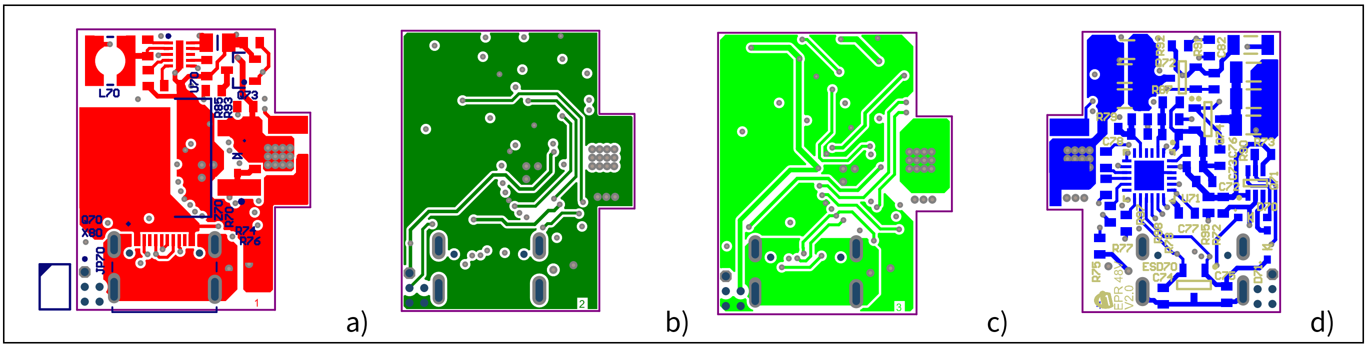


Figure 14 EPR board PCB: a) top side, b) inner top, c) inner bottom, d) bottom side

3 System performance

In the following sub-chapters, test equipment and key measurement results are illustrated.

3.1 Test equipment

The following equipment was used for the measurements:

- Oscilloscope: Yokogawa
- AC power source: Chroma 61504
- Electronic load: Chroma 6314A
- Digital power meter: WT3000

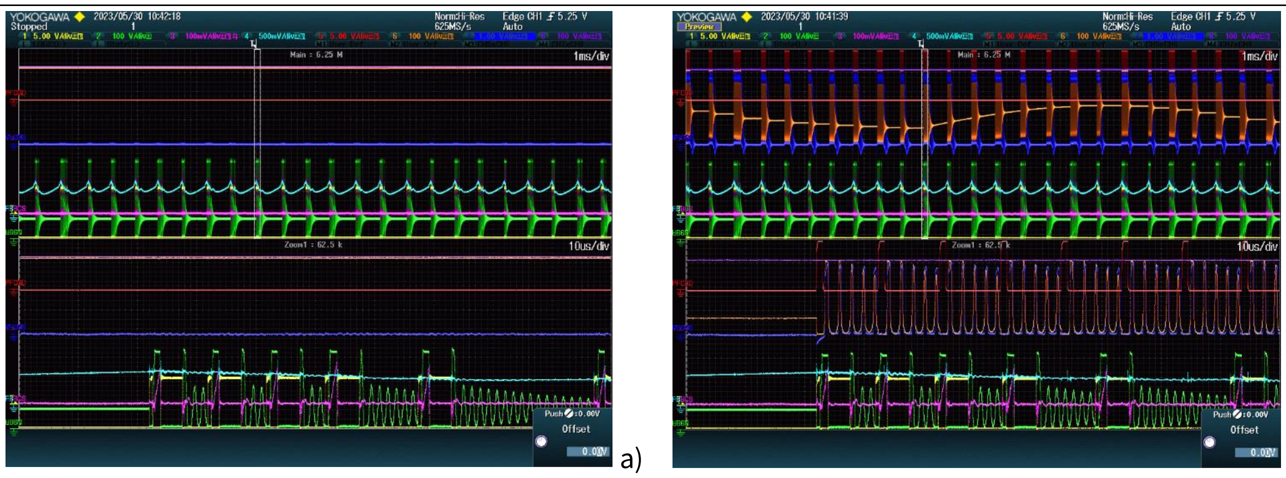
3.2 Key waveforms

Depending on the input and output conditions, the system operates in different modes, controlled by the controller XDP™ XDPS2222, namely:

- Burst mode
- Continuous operation

where burst mode applies only at very low load conditions.

In burst mode, depending on the output voltage and power level, the PFC stage may be kept disabled or enabled, while the HFB stage is always running in ZV-RVS mode. If PFC is enabled, it runs synchronously with the HFB. Figure 15 a) and b) shows two typical waveforms in burst mode operation.

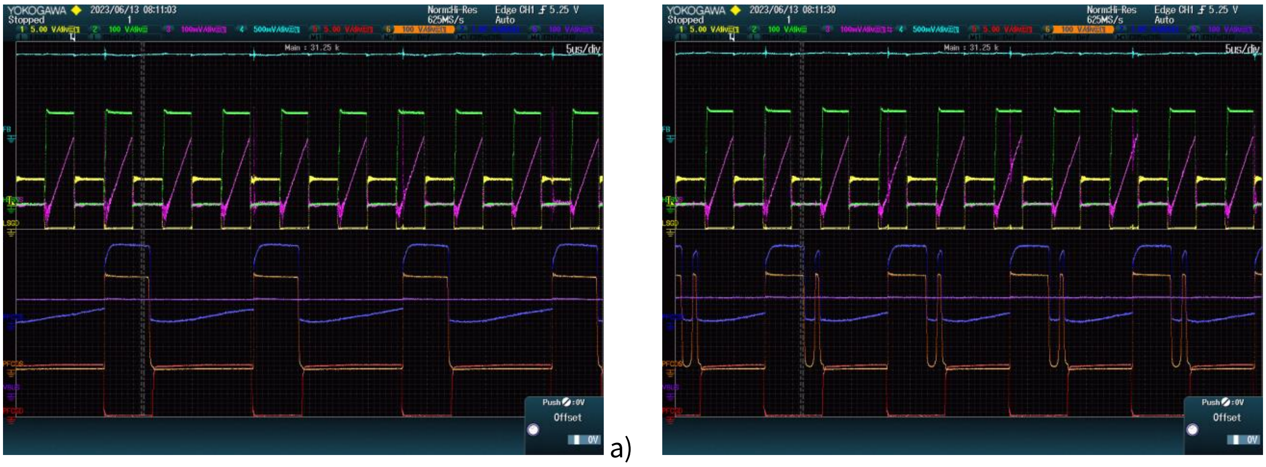


a) b)

Ch1: HFB LSGD, Ch2: HB switching node (HBSN), Ch3: HFB_{cs} (CSm), Ch4: HFB_{fb}, Ch5: PFC_{gate} (PFCGD), Ch6: PFC_{drain}, Ch7: PFC_{zcdcs}, Ch8: V_{bus}

Figure 15 Waveforms in burst mode operation: HFB in ZV-RVS with a) PFC disabled at 230 V input and 20 V, 0.15 A output, and b) PFC enabled at 115 V input and 20 V, 0.15 A output

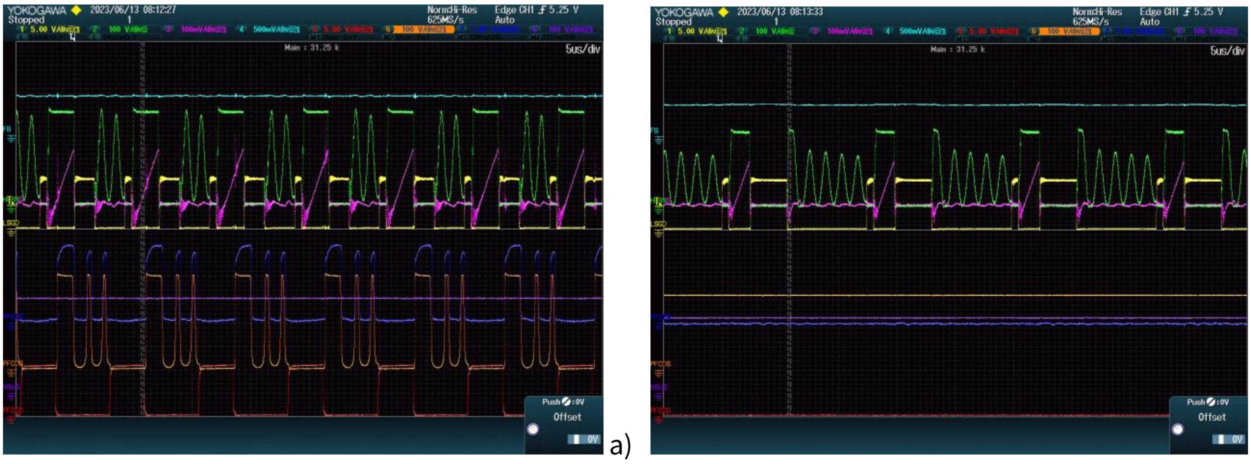
Once the system exits burst mode operation, the system runs in continuous operation mode. The operation of the PFC stage depends on the input and output conditions. The HFB runs either in CRM or ZV-RVS mode depending on the output voltage and/or power. The following figures show some of the typical waveforms in continuous operation.



a) b)

Ch1: HFB LSGD, Ch2: HB switching node (HBSN), Ch3: HFB_{cs} (CSm), Ch4: HFB_{fb}, Ch5: PFC_{gate} (PFCGD), Ch6: PFC_{drain}, Ch7: PFC_{zcdcs}, Ch8: V_{bus}

Figure 16 **Continuous operation mode with HFB in CRM at 48 V, 5 A output: a) PFC switching at first valley at 90 V input, and b) PFC switching at second valley at 115 V input**



a) b)

Ch1: HFB LSGD, Ch2: HB switching node (HBSN), Ch3: HFB_{cs} (CSm), Ch4: HFB_{fb}, Ch5: PFC_{gate} (PFCGD), Ch6: PFC_{drain}, Ch7: PFC_{zcdcs}, Ch8: V_{bus}

Figure 17 **Continuous operation mode with HFB in ZV-RVS mode: a) PFC switching at third valley at 115 V input and 48 V 2 A output, and b) PFC disabled at 230 V, 28 V 1 A output**

3.3 PFC performance

Table 6 shows the PFC performance at 48 V output voltage, 100 percent and 50 percent of full-load current. High power factor is achieved as shown in the measurement.

Table 6 **Power factor measurement**

V AC [V] / I_{out}	115	230
50 percent	0.98	0.95
100 percent	0.98	0.98

At the same time, low harmonics current is achieved, as shown in Figure 18.

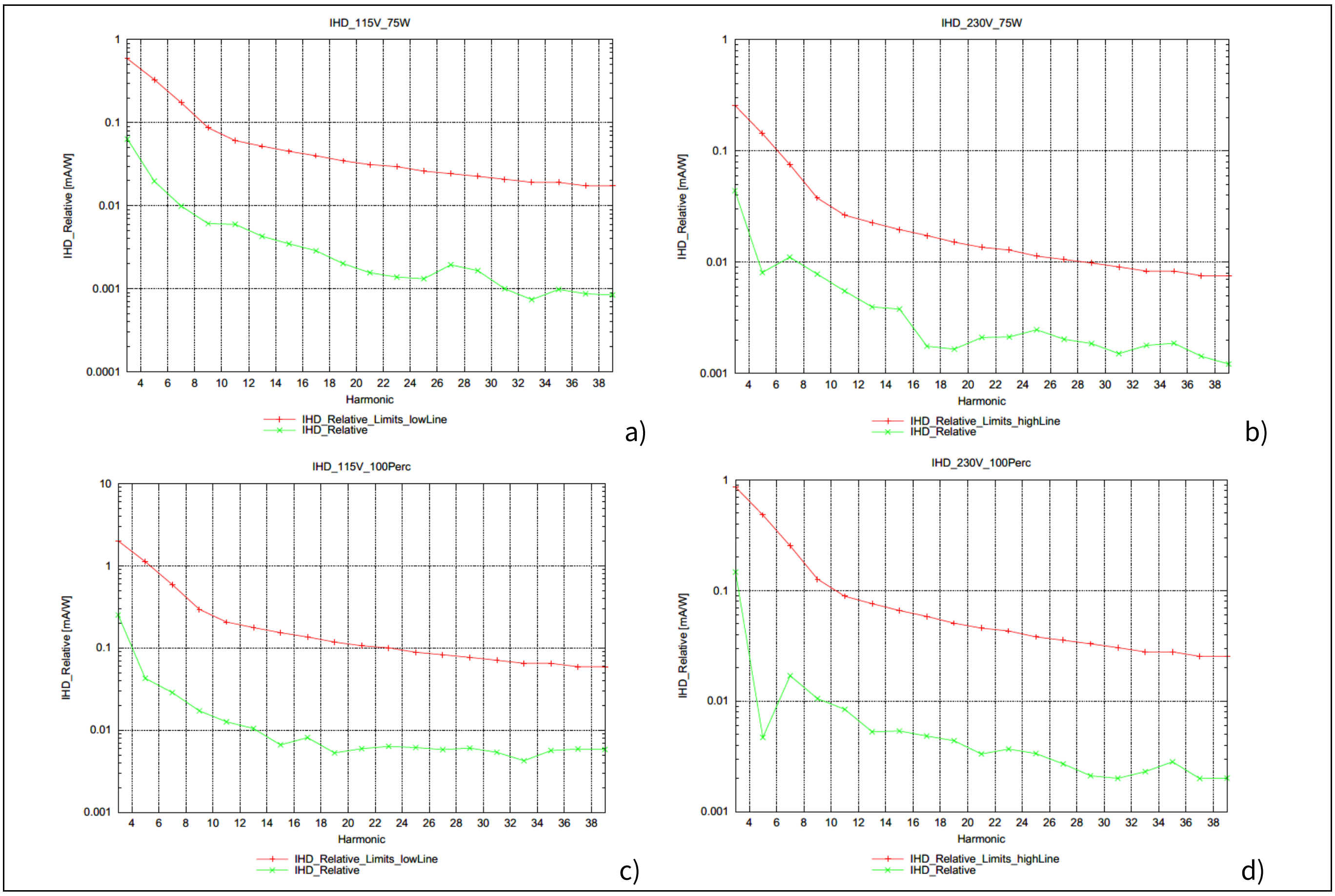


Figure 18 Harmonics current (green line) and its limit from IEC 61000-3-2 (red line): a) 115 V AC, 75 W, b) 230 V AC, 75 W, c) 115 V AC, 240 W and d) 230 V AC, 240 W

Controller XDP™ XDPS2222 has internal handshaking between the PFC and HFB controller and optimized bus voltage control for optimum performance. As shown in the previous waveforms (Figure 15 to Figure 17), PFC operation (activation/deactivation, number of switching valley) depends on the AC input voltage, the output voltage and the power level. This resulting behavior is shown in Figure 19. Here, output voltage and current were varied – beginning with low voltage (see bottom line) to high voltage (see upper line) and from low to high load (see left side to right side in each line). The results show that the PFC operation can be different even with the same output condition and input condition, since it also depends on history due to some hysteresis effects.

a)

Vout [V] \ Iout	25%	50%	75%	100%
5	ON	ON	ON	ON
9	ON	ON	ON	ON
15	ON	ON	ON	ON
20	ON	ON	ON	ON
28	ON	ON	ON	ON
36	ON	ON	ON	ON
48	ON	ON	ON	ON
36	ON	ON	ON	ON
28	ON	ON	ON	ON
20	ON	ON	ON	ON
15	OFF	OFF	OFF	ON
9	OFF	OFF	OFF	OFF
5	OFF	OFF	OFF	OFF

b)

Vout [V] \ Iout	25%	50%	75%	100%
5	OFF	OFF	OFF	OFF
9	OFF	OFF	OFF	OFF
15	OFF	OFF	OFF	ON
20	OFF	OFF	ON	ON
28	ON	ON	ON	ON
36	ON	ON	ON	ON
48	ON	ON	ON	ON
36	OFF	ON	ON	ON
28	OFF	OFF	ON	ON
20	OFF	OFF	ON	ON
15	OFF	OFF	OFF	ON
9	OFF	OFF	OFF	OFF
5	OFF	OFF	OFF	OFF

Figure 19 PFC enable/disable depending on AC input voltage, output voltage and power: a) 115 V AC and b) 230 V AC

3.4 HFB performance

Figure 20 (a to d) and Figure 21 (e to g) show the measured output voltage levels (overlapping lines in the middle) and its limits (black lines) during steady-state operation depending on the input and output conditions. The output voltage is well regulated within its limits under all conditions.

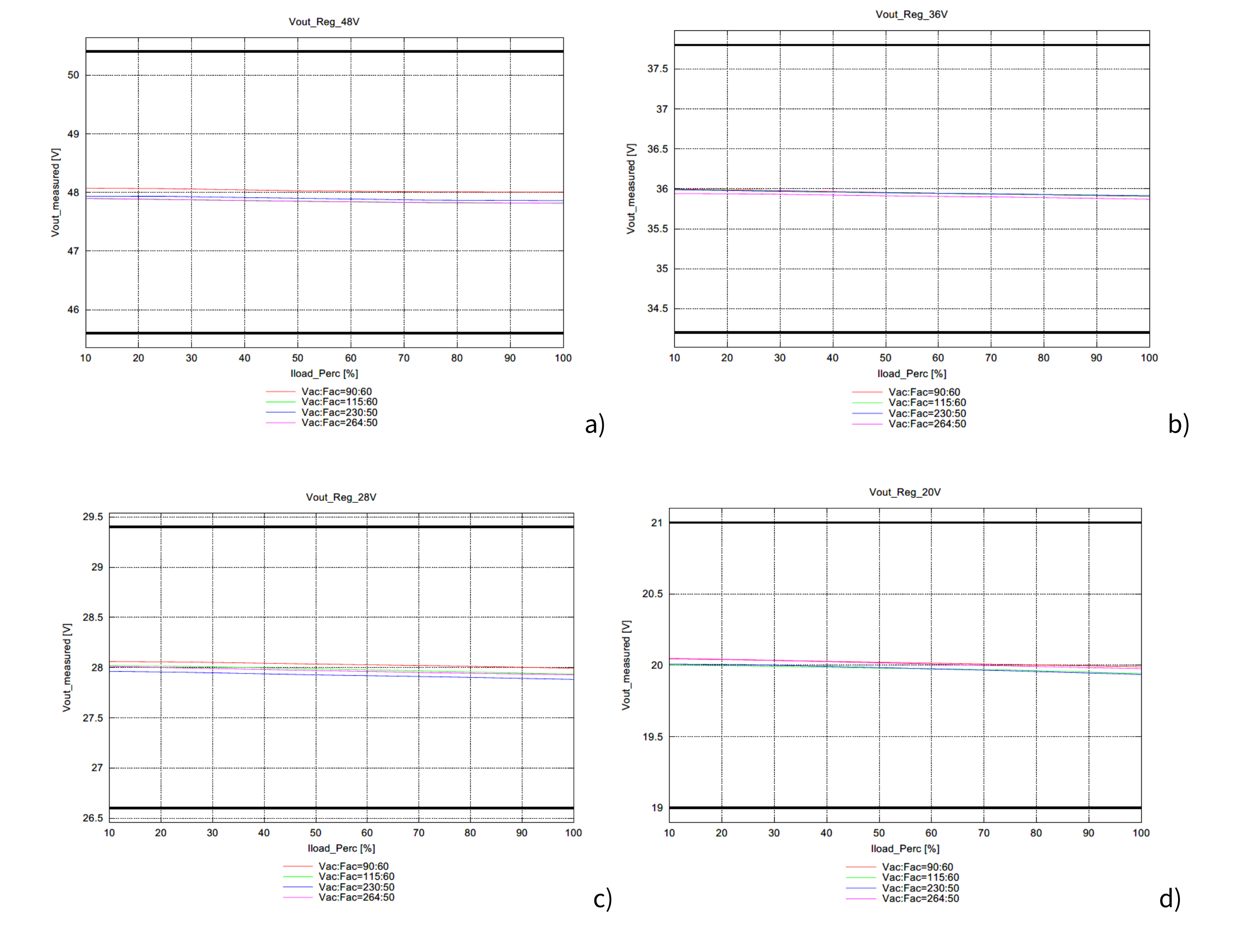


Figure 20 Output voltage in steady-state operation measured at the Type-C connector: a) 48 V, b) 36 V, c) 28 V, d) 20 V

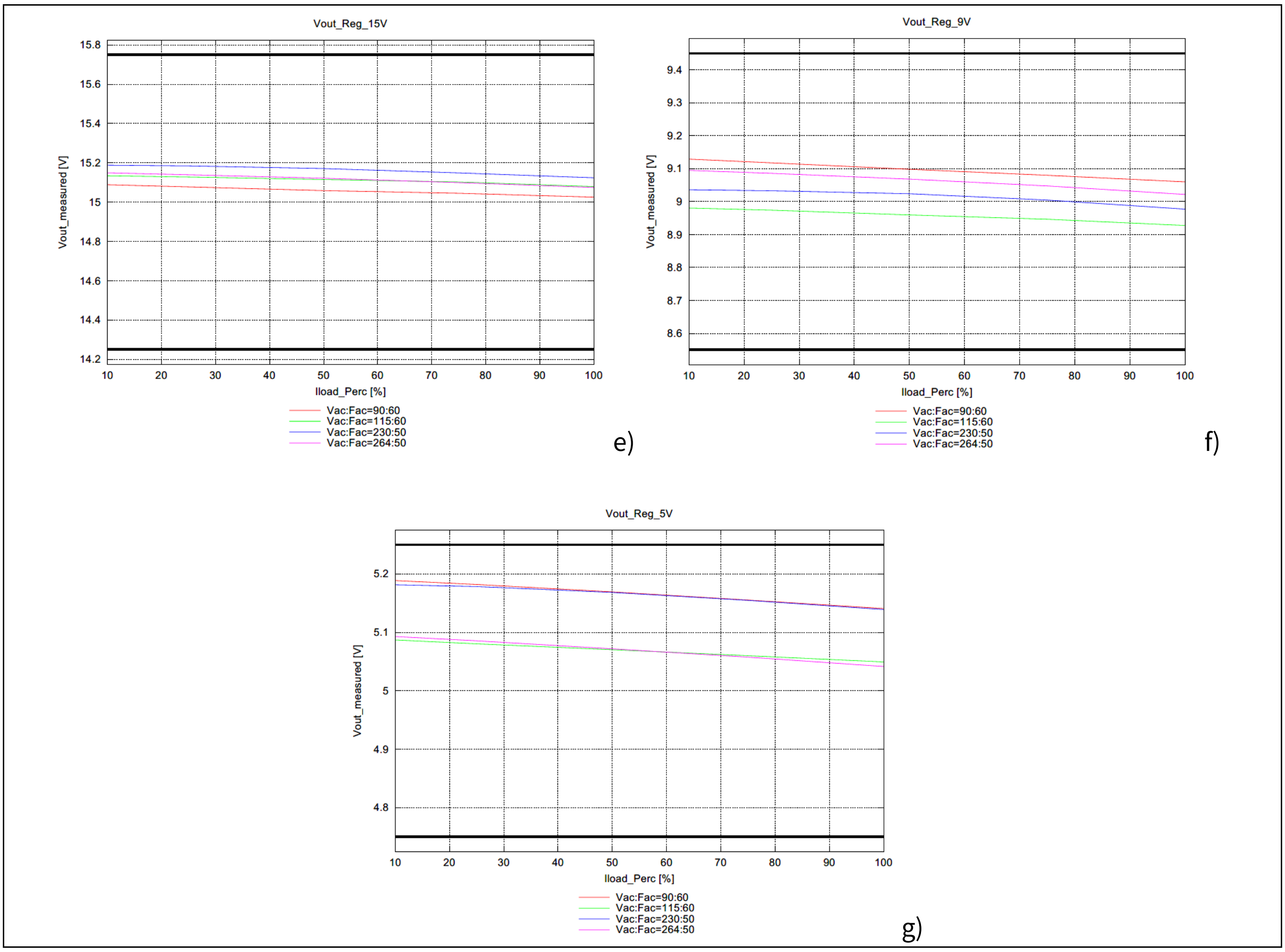


Figure 21 Output voltage in steady-state operation measured at the Type-C connector: e) 15 V, f) 9 V and g) 5 V

[Figure 22](#) (a to d) and [Figure 23](#) (e to g) show the output voltage at dynamic load depending on the input and output conditions. It shows very high dynamic response of the HFB stage under all conditions, and the output voltage is well regulated within its limits under all conditions.

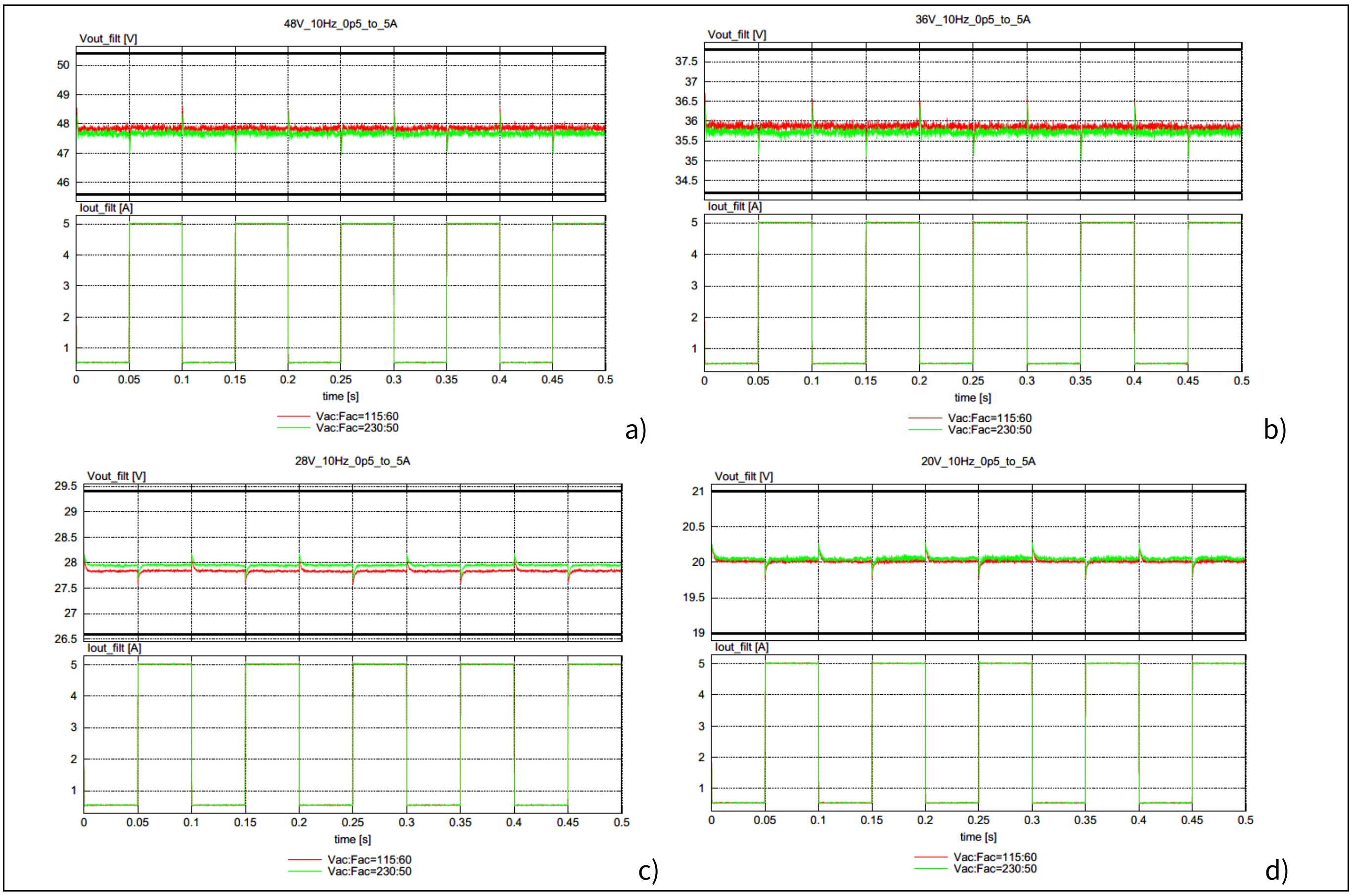


Figure 22 Output voltage at dynamic load current between 10 percent and 100 percent, measured at the Type-C connector: a) 48 V, b) 36 V, c) 28 V, d) 20 V

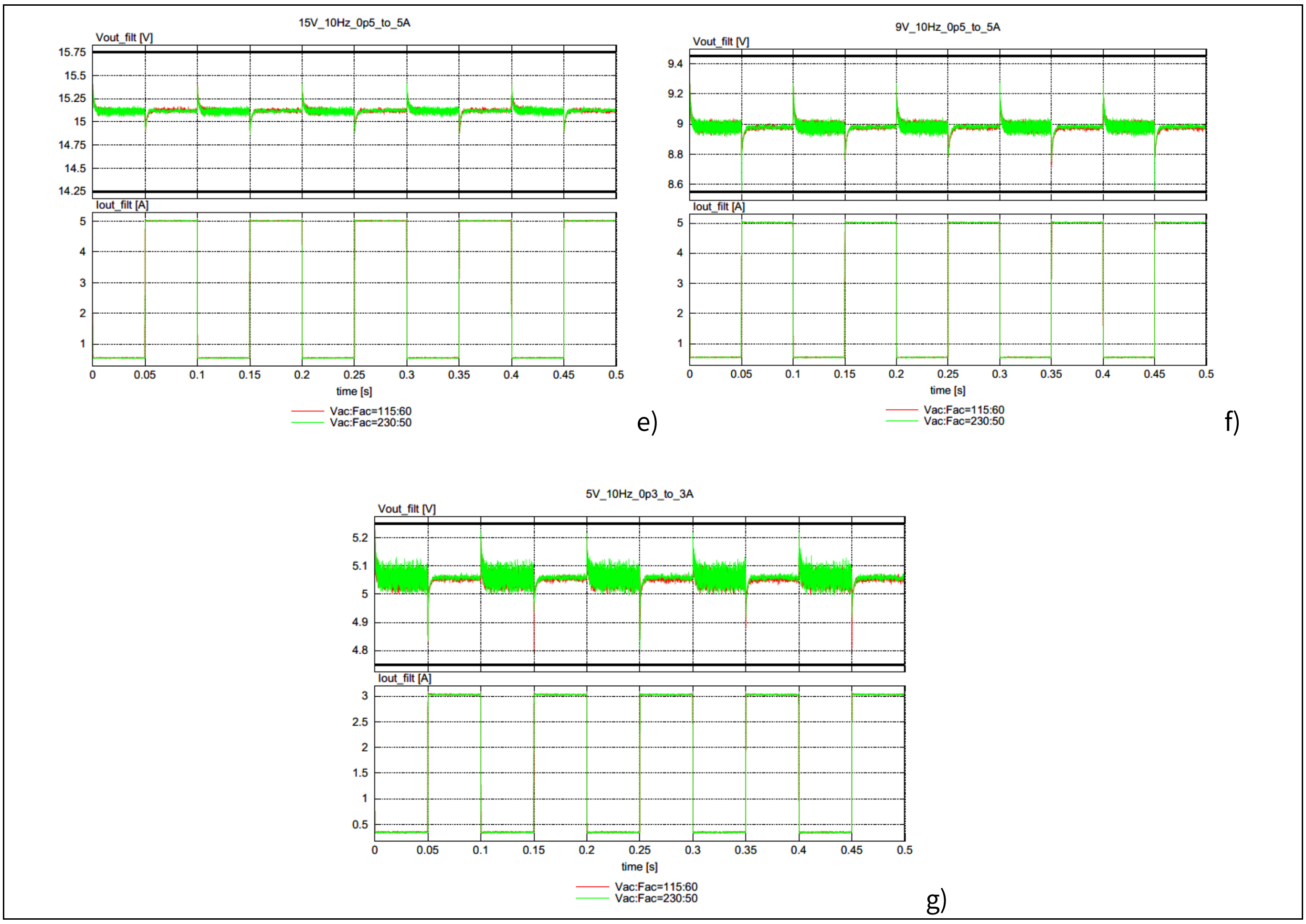


Figure 23 Output voltage at dynamic load current between 10 percent and 100 percent, measured at the Type-C connector: e) 15 V, f) 9 V and g) 5 V

The output voltage transition between 5 V and 48 V at different input and load currents is shown in Figure 24, while the rise time from 5 V to other voltage levels is shown in Figure 25 and fall time from other voltage levels to 5 V is shown in Figure 26. Smooth voltage transition is shown, and the transition time is within the USB-PD requirements.

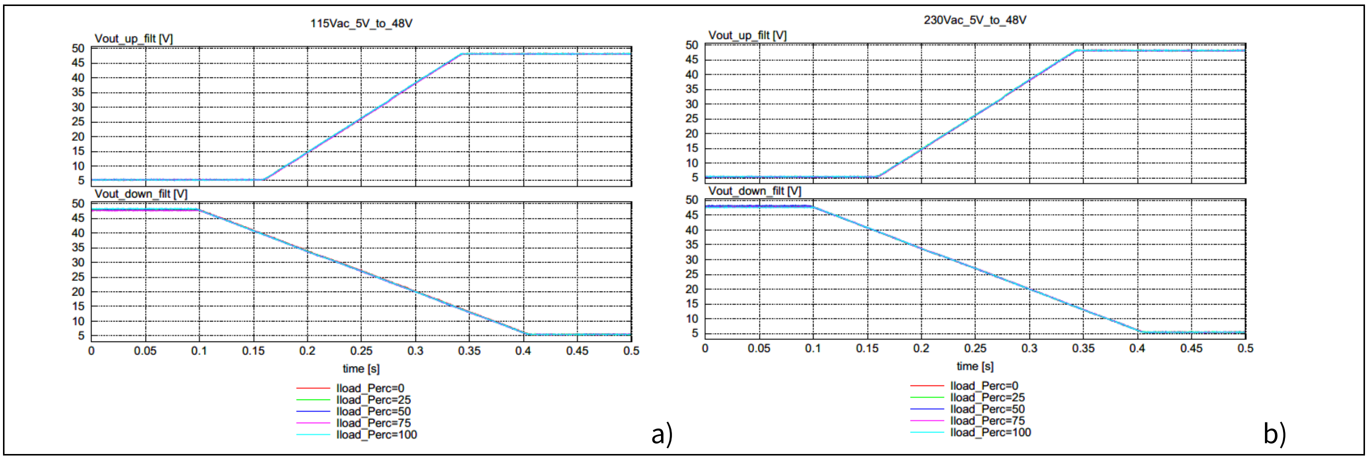


Figure 24 Output voltage transition between 5 V and 48 V: a) 115 V AC and b) 230 V AC

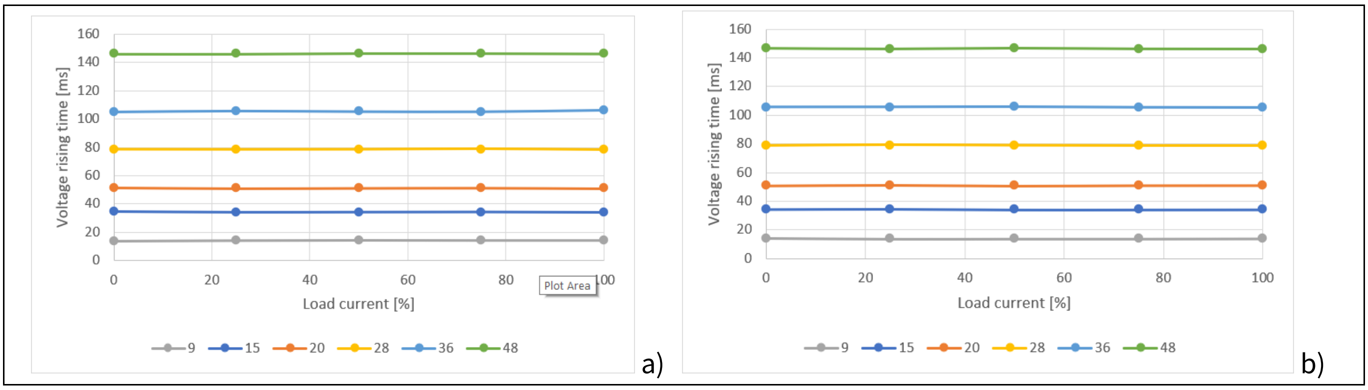


Figure 25 Output voltage rise time from 5 V to other voltage levels: a) 115 V AC and b) 230 V AC

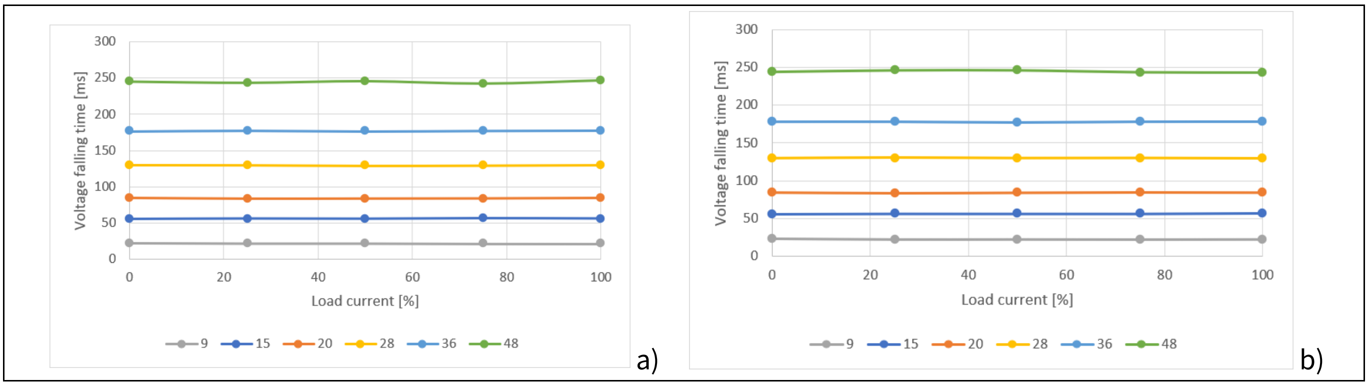


Figure 26 Output voltage fall time from other voltage levels to 5 V: a) 115 V AC and b) 230 V AC

Output voltage ripple at different conditions is shown in Figure 27.

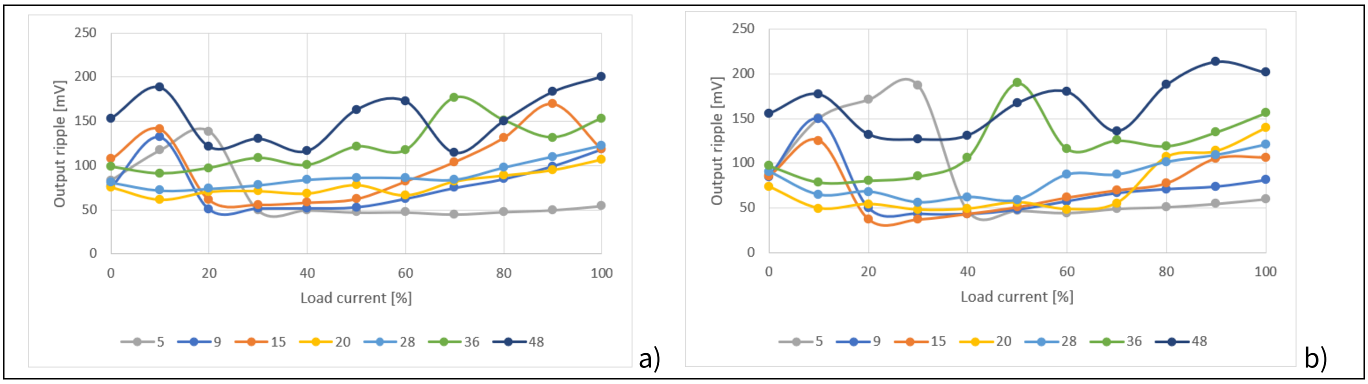


Figure 27 Output ripple measured at the Type-C connector: a) 115 V AC and b) 230 V AC

3.5 System performance

3.5.1 Efficiency and standby power

Efficiency of the board measured at the Type-C connector is shown in Table 7.

Table 7 Efficiency as a percentage, measured at the Type-C connector

V AC [V]	I_{out} / V_{out} [V]	100 percent	75 percent	50 percent	25 percent
115	5	84.01	82.25	81.43	78.89
	9	88.93	88.81	87.22	84.73
	15	91.41	91.94	91.58	88.98
	20	92.34	92.69	92.03	89.30
	28	92.68	92.92	92.13	89.51
	36	92.84	93.11	92.42	89.58
	48	93.01	93.38	91.93	90.50
230	5	89.43	89.09	88.21	87.03
	9	92.41	92.95	92.96	91.78
	15	91.89	93.93	94.63	93.48
	20	92.67	92.66	94.69	93.57
	28	93.96	93.87	92.90	92.01
	36	94.43	94.41	93.53	90.84
	48	94.92	94.94	92.99	91.44

These results are illustrated in Figure 28.

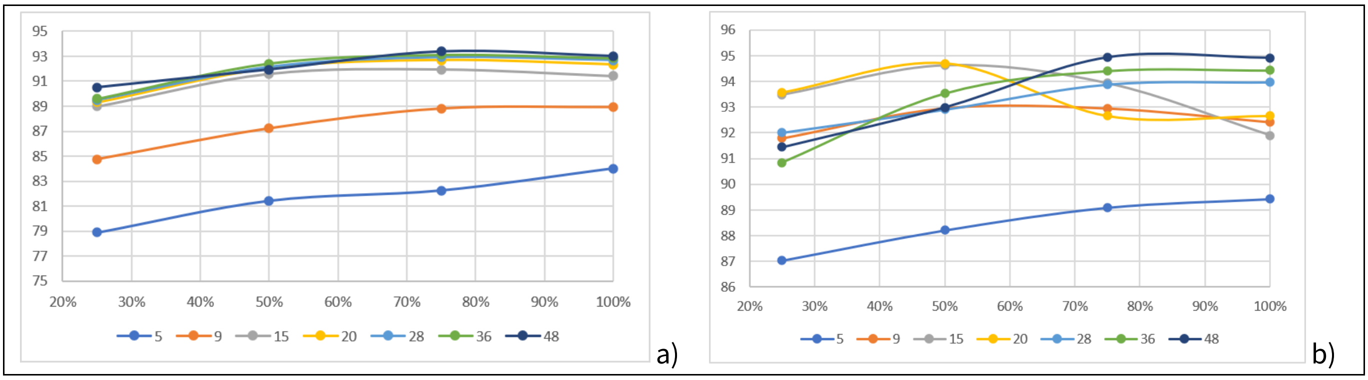


Figure 28 Efficiency measured at the Type-C connector: a) 115 V AC and b) 230 V AC

System average efficiency measured at the Type-C connector is shown in Table 8 and illustrated in Figure 29.

Table 8 Average efficiency as a percentage, measured at the Type-C connector

V AC [V] / V_{out} [V]	115	230
5	81.64	88.44
9	87.42	92.53
15	90.98	93.48
20	91.59	93.40
28	91.81	93.18
36	91.98	93.30
48	92.21	93.57

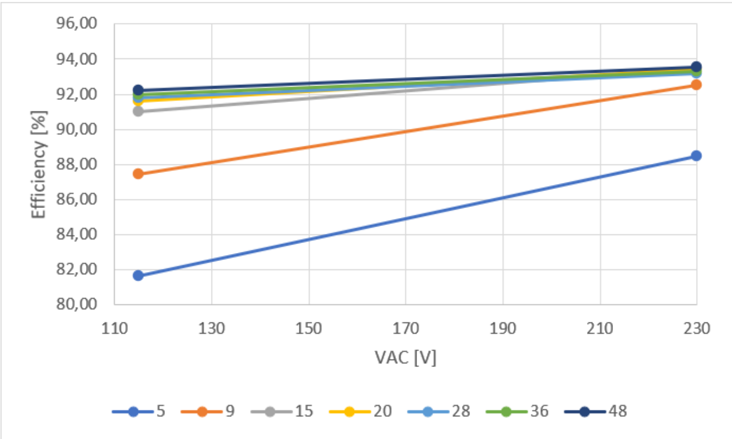


Figure 29 Average efficiency measured at the Type-C connector

System standby input power is measured, and the results are shown in Table 9. This measurement does not include the power loss on the X-capacitor discharge resistors RX1 and RX2.

Table 9 Input standby power measurements

V AC [V] / Pin	115 V	230 V
Total standby losses	54.6 mW	101.0 mW
Losses of X-capacitor discharge resistor	5.5 mW	22.0 mW
Standby losses without X-capacitor discharge resistor	49.1 mW	79.0 mW

The total standby losses can be reduced by replacing the X-capacitor discharge resistors with an active discharge controller.

3.5.2 Thermal measurement

The following images in Figure 30 and Figure 31 are the thermal images of the board at full load. The measurements were done at 25°C ambient temperature.

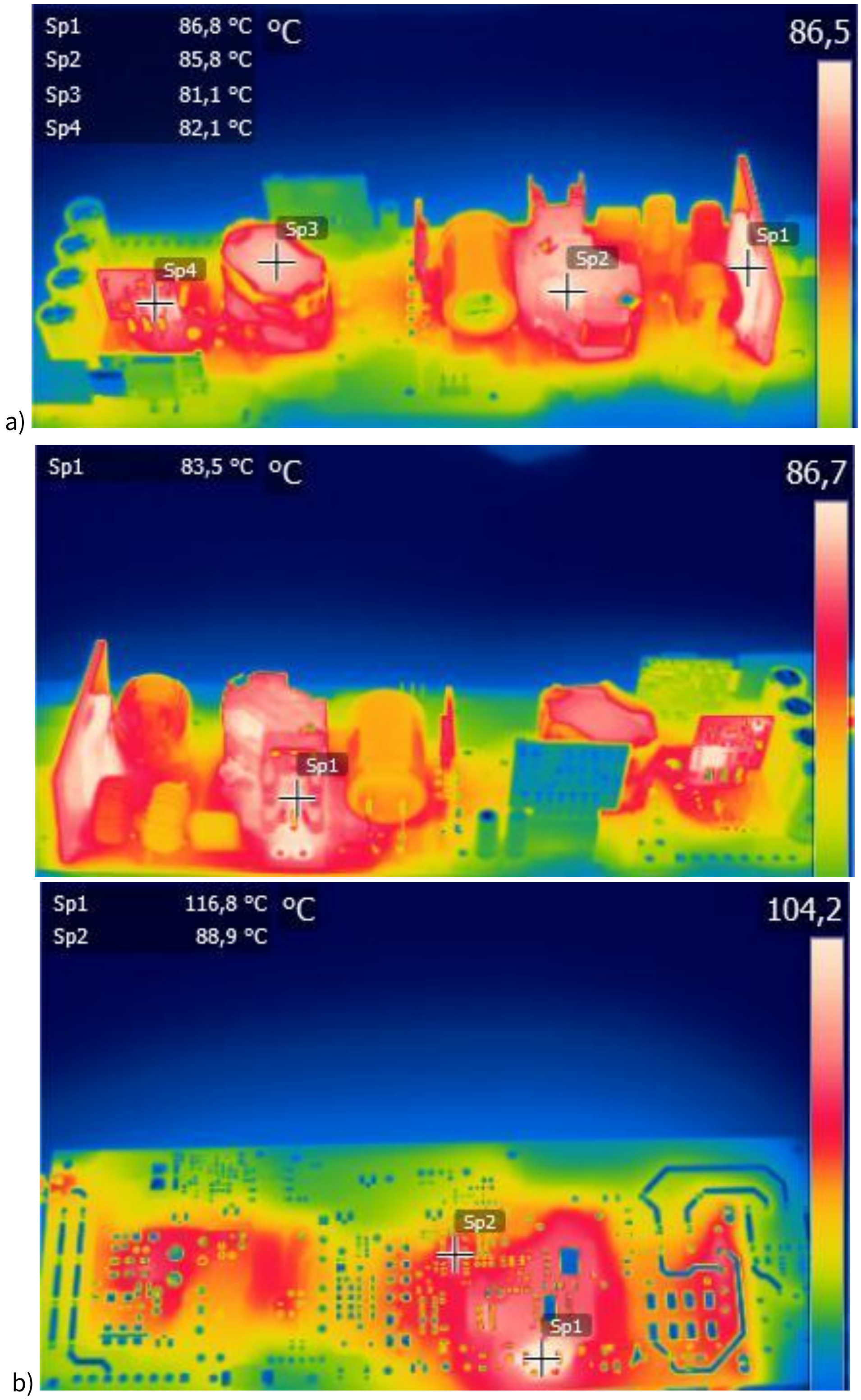


Figure 30 Thermal measurement: a) top side at 115 V AC, b) bottom side at 115 V AC

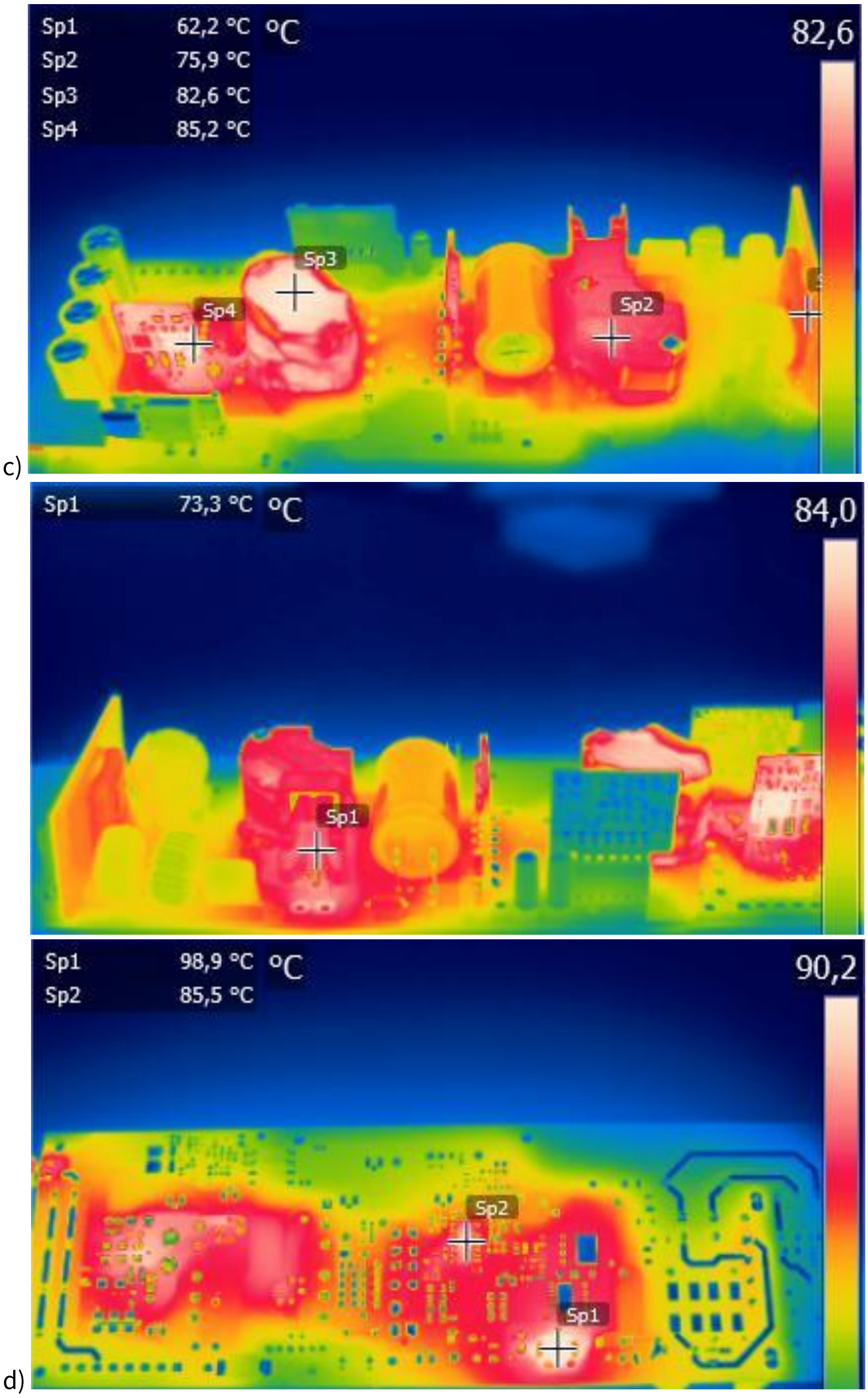


Figure 31 Thermal measurement: c) top side at 230 V AC and d) bottom side at 230 V AC

The measurements show that the device with the highest temperature captured on the board is the PFC diode at 115 V AC and full load, reaching a temperature of 116.8°C. If this temperature can not be accepted in the application, a through-hole mounted diode D9 with optional heatsink D9_HS may be used instead of the surface mounted diode D8.

4 Appendices

The chapter presents the following information:

- BOMs of the boards
- Information on the magnetic devices

4.1 Bills of materials of the boards

In this sub-chapter, BOMs of the three boards are given. While the given component voltage class shows its required operating voltage, some components on the board may have higher specification values due to component availability. Unless otherwise indicated in the BOM, 5 percent or better tolerance applies to the standard SMD resistors, and X7R or better or higher voltage class applies to the standard ceramic capacitors.

Table 10 BOM of the main power board

No.	Quantity	Designator	Description
1	1	AC_IN	Connector Würth Elektronik, 691412320002
2	1	C1	3.3 nF, 25 V, 0603
3	1	C2	47 pF, 50 V, 0603
4	1	C9	82 µF, 450 V, Würth Elektronik, 861221483002
5	1	C50	100 nF, 450 V, 1206
6	1	C70	330 pF, 50 V, 0603
7	2	C71, C77	100 nF, 50 V, 0603
8	2	C72, C100	1 µF, 25 V, 0603
9	1	C74	100 pF, 50 V, 0603
10	2	C75, C80	22 µF, 25 V, Nichicon, UVR1E220MDD
11	1	C78	150 pF, 50 V, 0603
12	1	C79	22 pF, 50 V, 0603
13	2	C82, C83	220 nF, 250 V, 1206
14	2	C84, C85	150 nF, 250V, 1206
15	4	C201, C202, C203, C204	220 µF, 63 V, Kemet, A759MY227M1JAAE45
16	1	C205	1 µF, 50 V, 0603
17	1	C207	10 µF, 63 V, 1206
18	1	C209	1 nF, 50 V, 0603
19	1	C210	470 pF, 50 V, 0603
20	1	C211	2.2 nF, 25 V, 0603
21	2	CB1, CB4	220 nF, 450 V, 1210
22	1	CB3	470 nF, 450 V, Panasonic, ECW-FD2W474P1
23	1	CX2	330 nF, 275 V, Kemet, R46KI333040P0M
24	1	CY200	470 pF, Murata, DK1E3EA102M86RBH01
25	2	D1, D2	US1MFA, SOD-23FL
26	4	D3, D4, D5, D71	1N4148WS-7-F, SOD-323
27	1	D6	RS3JB-13-F, SMB

No.	Quantity	Designator	Description
28	1	D8	MUR560J, 600 V, SMD
29	1	D10	GBU8K, SIP-4
30	1	D10_HS	Heatsink, mechanical connection with thermal paste, 13.21 mm L x 12.70 mm W x 19.05 mm H
31	1	D72	ES1GL, SMA
32	1	D205	30 V, SOD-523
33	1	DB SR LS	SR daughter board
34	1	F1	3.15 A, 63 V, THT
35	1	HB_DaughterBoard	Half-bridge daughter board
36	1	HB_USB200	EPR daughter board
37	2	i_PFC, i_Pri	Connector JL-250-25-T
38	1	JP70	Connector HTSW-103-07-G-S, CON-THT-2.54-3-1-8.38
39	1	LC1	5 mH, THT, Würth Elektronik, 7448023005
40	2	LD1, LD2	Short, THT
41	2	LD3, LD4	60 µH, THT, Würth Elektronik, 7447023
42	1	Q3A	IPP60R070CFD7, PG-TO220-3, Infineon
43	1	Q3A_HS	Heatsink, TO-220, 13.21 mm L x 12.70 mm W x 19.05 mm H, Fischer Elektronik, 10006497
44	1	Q71	2PD601ART, 50 V, PG-SOT-23
45	1	Q200	BSS159N, SOT-23-3, Infineon
46	1	R1	Short, wire 7.5 mm insulated
47	1	R3	24 k, 200 V, 1206
48	1	R4	47 k, 75 V, 0603
49	11	R5, R8, R90, R101, R102, R110, R203, R208, R210, R212, R217	0 R, 75 V, 0603
50	1	R6	9.1 k, 150 V, 0805
51	1	R7	27 k, 200 V, 1206
52	1	R11	10 R, 50 V, 0603
53	1	R13	18 k, 75 V, 0603
54	1	R14	33 k, 75 V, 0603
55	3	R15, R16, R19	220 mR, 1206
56	1	R24	Short
57	1	R70	150 k, 75 V, 0603
58	1	R70a	750 k, 75 V, 0603,
59	2	R71, R72	10 MEG, 200 V, 1206
60	1	R75	18 k, 75 V, 0603
61	1	R76	100 k, 75 V, 0603
62	1	R77	1 k, 75 V, 0603

No.	Quantity	Designator	Description
63	2	R78, R79	36 k, 75 V, 0603
64	1	R84	3.3 R, 200 V, 1206
65	1	R91	100 R, 75 V, 0603
66	1	R92	1 k, 75 V, 0603
67	3	R93, R94, R95	270 mR, 675 V, 1206
68	1	R98	4.7 MEG, 400 V, 1206
69	1	R99	10 k, 75 V, 0603
70	1	R204	2.2 k, 75 V, 0603
71	1	R205	10 k, 75 V, 0603
72	2	R206, R213	470 k, 75 V, 0603
73	1	R209	6.8 k, 75 V, 0603
74	1	R211	22 k, 75 V, 0603
75	1	R214	47 k, 75 V, 0603
76	1	RV1	TVS 275 V AC, THT
77	2	RX1, RX2	1.2 MEG, 200 V, 1206
78	1	SR_HS_BP	Connector JL-100-25-T, JP-THT-JL-100-25-T
79	1	T1	110 µH, Np:Naux = 36:7, RM10, 3C95, ICE Transformers, 8017.0802.021, see Figure 32
80	1	TR200	120 µH, Np:Ns:Na1:Na2 = 20:5:1:2, RM10, ICE Transformers, 8045.0804.051, see Figure 33
81	1	U70	XDPS2222, DSO-14, Infineon
82	1	U71	TCLT1003, SOP4L
83	1	U200	ATL432LIBQDBZRQ1, SOT-23(3)
84	1	X80	V_{CC} daughter board
85	1	Z1	2.7 V, SOD-323
86	0	AUXH, AUXL, BUS, GMOS, LSGD, PGND1, Rect, SGND, SGND1, VCC	
87	0	C3	
88	0	C4	
89	0	C5	
90	0	C6	
91	0	C10	
92	0	C73	
93	0	C76	
94	0	C81	
95	0	C86	
96	0	C87, C88, C89, C90	
97	0	C200, C208	

No.	Quantity	Designator	Description
98	0	C220	
99	0	C221	
100	0	CB2	
101	0	CSm, FB, PC_2, PFCCS, PFCGD, TOneg, TOpos, Vaux1	
102	0	CX1, CX3	
103	0	D7	
104	0	D9	
105	0	D9_HS	
106	0	D200, D202	
107	0	D201	
108	0	DB1, DB2	
109	0	DB SR HS	
110	0	MP1, MP2, MP3, MP4, MP5, MP6, MP8	
111	0	Q1	
112	0	Q2	
113	0	Q3	
114	0	Q70	
115	0	Q72	
116	0	R2	
117	0	R10	
118	0	R12	
119	0	R17	
120	0	R73	
121	0	R74	
122	0	R80	
123	0	R81	
124	0	R86	
125	0	R96	
126	0	R97	
127	0	R100, R103, R104, R202	
128	0	R200, R201	
129	0	R207, R216	
130	0	R215	
131	0	RX3, RX4	
132	0	SR_LS_BP	
133	0	U1	

No.	Quantity	Designator	Description
134	0	U72	
135	0	X202	

Table 11 BOM of the half-bridge board

No.	Quantity	Designator	Description
1	2	C47, C51	3.3 nF, 25 V, 0603
2	2	Q8, Q11	IGLD60R190D1, PG-LSON-8-1, Infineon
3	2	R75, R80	1.5 k, 75 V, 0603
4	2	R76, R82	39 R, 75 V, 0603
5	2	R77, R84	22 k, 75 V, 0603
6	1	R79	0 R, 75 V, 0603
7	0	C48, C52	
8	0	C49, C50	
9	0	D23, D24	
10	0	Q9, Q10	
11	0	R78, R85	
12	0	R81, R83	

Table 12 BOM of the V_{CC} board

No.	Quantity	Designator	Description
1	4	C500, C501, C504, C505	470 nF, 100 V, 1206
2	4	C502, C506, C507, C508	4.7 µF, 100 V, 1206
3	1	C503	1 µF, 50 V, 0805
4	2	D500, D501	SS28L, SOD-123F-2
5	2	D502, D503	PMEG4010BEA, 115
6	1	Q500	BSS169, PG-SOT-23, Infineon
7	2	R500, R505	3.6 R, 200 V, 1206
8	2	R501, R506	0 R, 1206
9	1	R504	47 k, 75 V, 0603
10	1	X500	6-pin header, 2.54 mm
11	1	Z500	BZT52-B10J, 10V, SOD-123

Table 13 BOM of the SR board

No.	Quantity	Designator	Description
1	1	C1	1 µF, 25 V, 0805
2	1	C2	100 nF, 50 V, 0603
3	1	Q1	BSC074N15NS5, PG-TSON-8-3, Infineon
4	1	Q3	BSS169, PG-SOT-23, Infineon
5	1	R1	510 R, 150 V, 0805

No.	Quantity	Designator	Description
6	1	R2	5.1 R, 150 V, 0805
7	1	R4	100 k, 150 V, 0805
8	1	R6	47 k, 75 V, 0603
9	1	U1	MP6951GJ-P, TSOT23-6, MPS
10	1	Z1	18 V, DO-214AC
11	0	C10	
12	0	D10	
13	0	Q2	
14	0	R3, R5	
15	0	R10	

Table 14 BOM of the EPR board

No.	Quantity	Designator	Description
1	2	C72, C83	1 µF, 50 V, 0603
2	4	C73, C76, C78, C79	100 nF, 16 V, 0603
3	2	C74, C75	390 pF, 50 V, 0603
4	1	C80	47 nF, 50 V_{min}, 0603
5	1	C81	1 µF, 100 V, 0805
6	1	C82	22 µF, 10 V, 1206
7	2	D70, D71	1N4148WS-7-F, SOD-323
8	1	ESD70	ESDA25L, SOT-23
9	1	JP70	USB Type-C connector, JAE, DX07S016JA1R1500
10	1	L70	33 µH, 0.42 A, Würth Electronik, 744031330
11	1	Q70	IPB110P06LM, PG-TO263-3-2, Infineon
12	1	Q71	DMP2200UDW-7
13	2	Q72, Q74	IRLML2060TRPBF, SOT-23, Infineon
14	1	Q73	2N7002, SOT-23-2, Infineon
15	1	R70	330 k, 75 V, 0603
16	2	R71, R79	200 k, 75 V, 0603
17	2	R72, R73	100 k, 75 V, 0603
18	2	R74, R76	10 mR, 0805
19	1	R75	1 k, 75 V, 0603
20	1	R77	18 k, 75 V, 0603
21	1	R78	2.4 M, 0603
22	6	R80, R81, R82, R83, R84, R96	330 R, 200 V, 1206
23	4	R85, R88, R89, R90	33 k, 0603
24	2	R86, R87	20 k, 75 V, 0603
25	1	R91	1 M, 0603
26	1	R92	187 k, 0603

No.	Quantity	Designator	Description
27	1	R94	18 k, 0603
28	1	R95	0 R, 75 V, 0603
29	2	R97, R98	100 R, 75 V, 0603
30	1	U70	LT8618
31	1	U71	CYPD3175, QFN24, Infineon
32	1	Z70	TDZ15J, SOD323_d
33	0	C70	
34	0	C77	
35	0	R93	

4.2 Information on the magnetic devices

Information about the PFC choke and the HFB transformer is shown in Figure 32 and Figure 33.

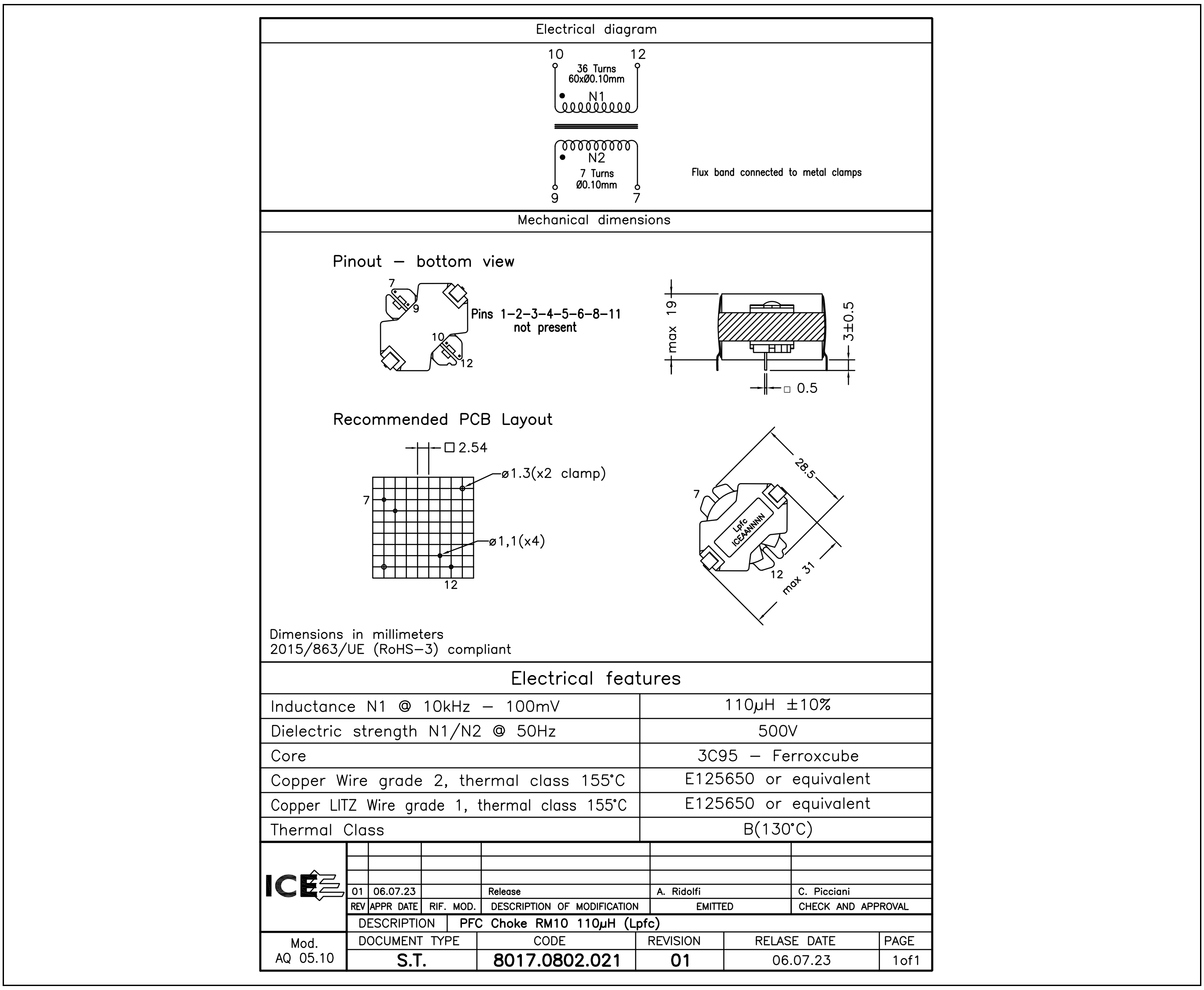
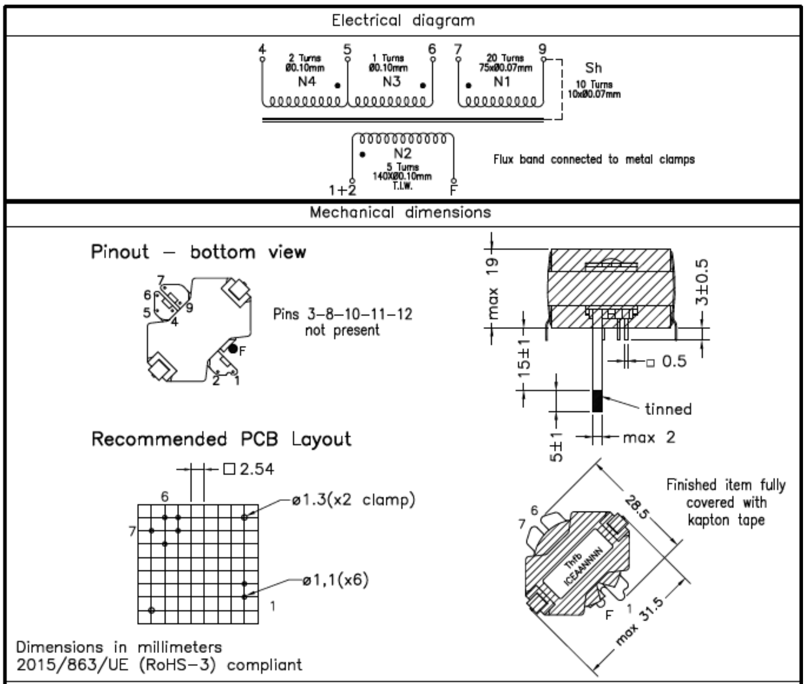


Figure 32 **PFC choke 8017.0802.021.01**



Electrical features	
Inductance N1 @ 100kHz – 100mV	120µH ±10%
Dielectric strength N1/N2 @ 50Hz	3000V
Dielectric strength N1/N3+N4 @ 50Hz	1500V
Dielectric strength N2/N3+N4 @ 50Hz	500V
Dielectric strength N1+N2+N3+N4/core @ 50Hz	500V
Core	3C95 – Ferroxcube
Copper Wire grade 2, thermal class 155°C	E125650 or equivalent
Copper LITZ Wire grade 1, thermal class 155°C	E125650 or equivalent
Copper LITZ Wire Triple Insulation; thermal class 155°C	E227175

REV	APPR DATE	RIF. MOD.	DESCRIPTION OF MODIFICATION	EMITTED	CHECK AND APPROVAL
02	27.07.23		Modified dielectric strength tests	A. Ridolfi	C. Picciani
01	06.07.23		Release	A. Ridolfi	C. Picciani

DESCRIPTION: Flyback transformer RM10 (Thfb)

Mod.	DOCUMENT TYPE	CODE	REVISION	RELASE DATE	PAGE
AQ 05.10	S.T.	8045.0804.051	02	06.07.23	1of1

Figure 33 HFB transformer 8045.0804.051.02

References

[1] Infineon Technologies AG: XDPS2222 PFC + hybrid flyback – combo controller, Datasheet (Rev. 1.0); 2023-03-29; Available online.

Revision history

Document version	Date	Description of changes
V 1.0	2023-09-15	Initial release

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