

# Infineon New CCM PFC Solution ICE3PCS01G

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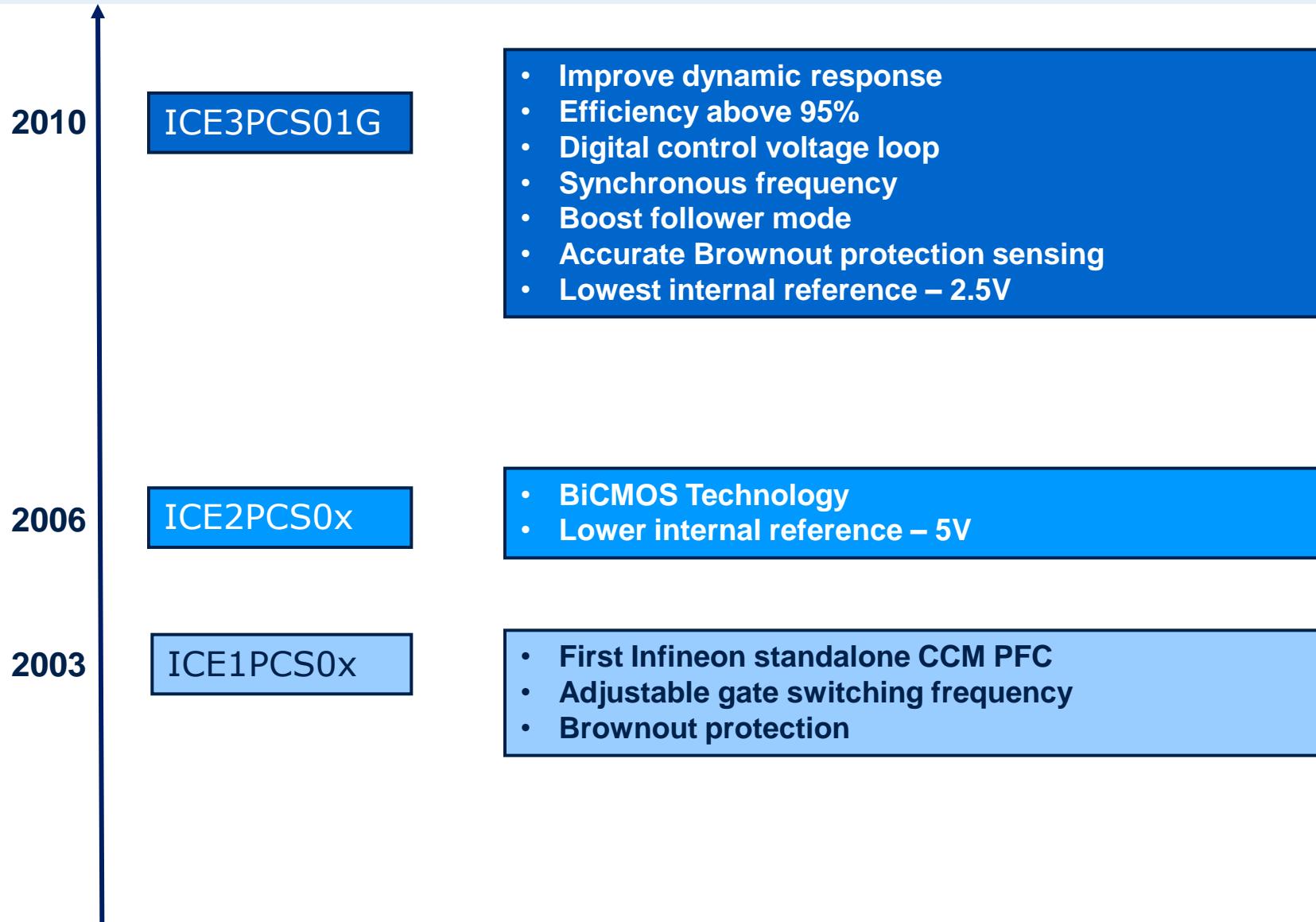


# Outline

## Infineon CCM PFC family

- 3<sup>rd</sup> Generation Infineon CCM PFC
  - Features
  - Functionality
  - 300Watt demo board results

# Infineon CCM PFC controller History

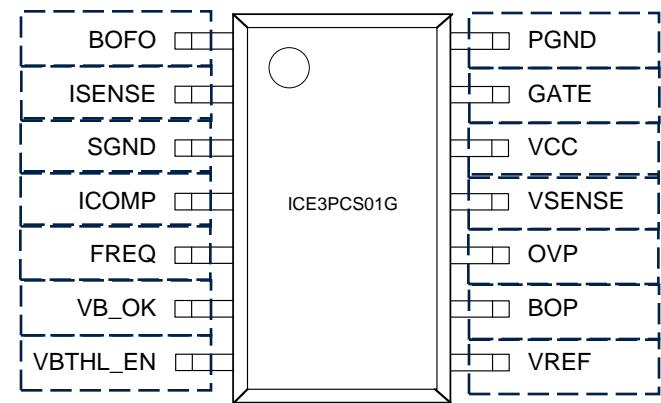


# Outline

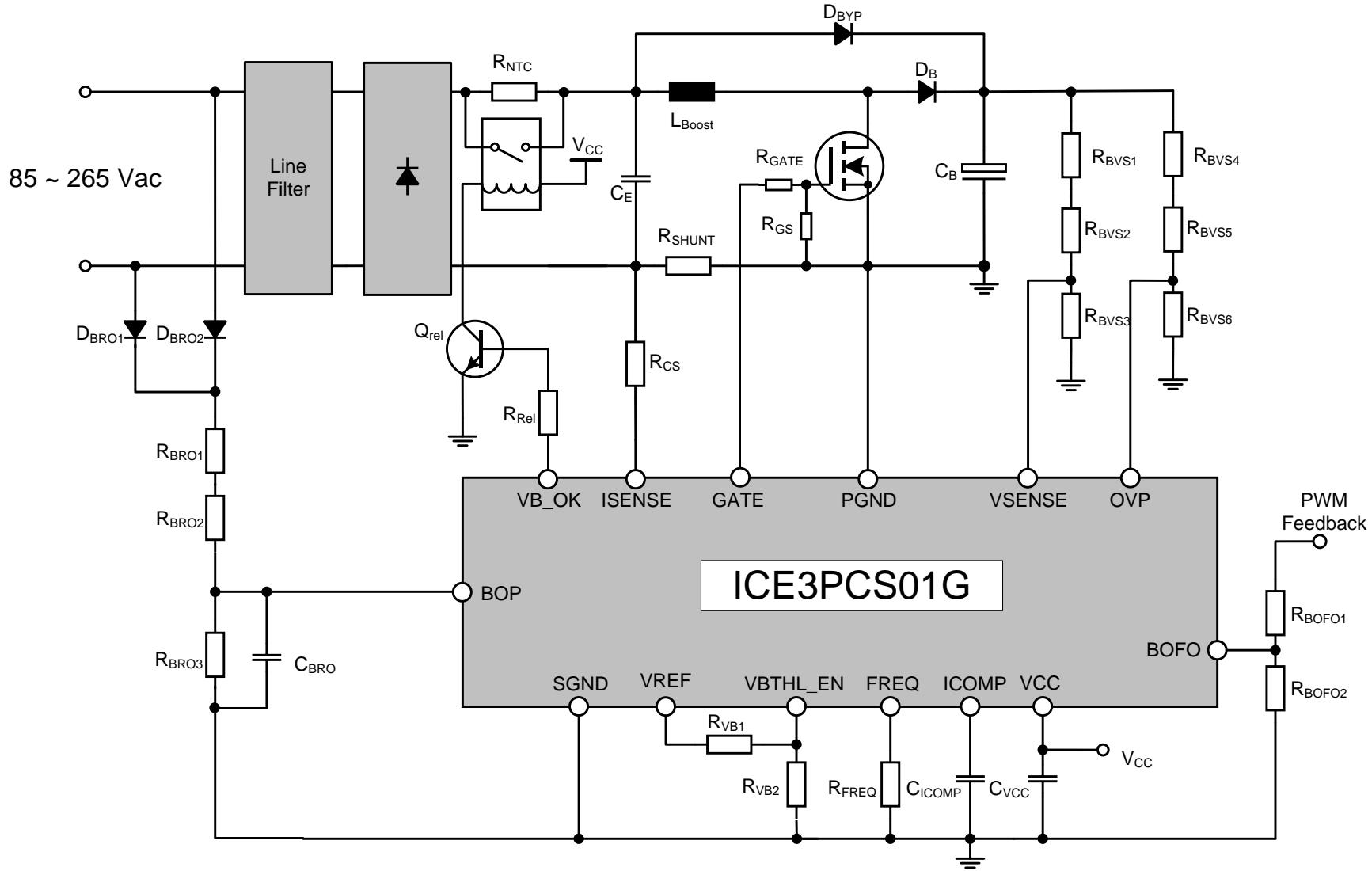
- Infineon CCM PFC family
- 3<sup>rd</sup> Generation Infineon CCM PFC
  - Features
  - Functionality
  - 300Watt demo board results

# Pin Layout ICE3PCS01G

- Pin1 =Boost Follower Setting (BOFO)
- Pin2 =Current Sense Input (ISENSE)
- Pin3 =Signal Ground (SGND)
- Pin4 =Current Loop Compensation (ICOMP)
- Pin5 =Switching Frequency Setting (FREQ)
- Pin6 =Bulk Voltage OK Signal
- Pin7 =PFC Enable Function (VBTHL\_EN)
- Pin8 =Voltage reference (VREF)
- Pin9 =Brownout Protection (BOP)
- Pin10 =Over Voltage Protection (OVP)
- Pin11 =Bulk Voltage Sense (VSENSE)
- Pin12 =IC Supply Voltage (VCC)
- Pin13 =Gate Drive (GATE)
- Pin14 =Power Ground (PGND)



# Typical Application Circuit



# Outline

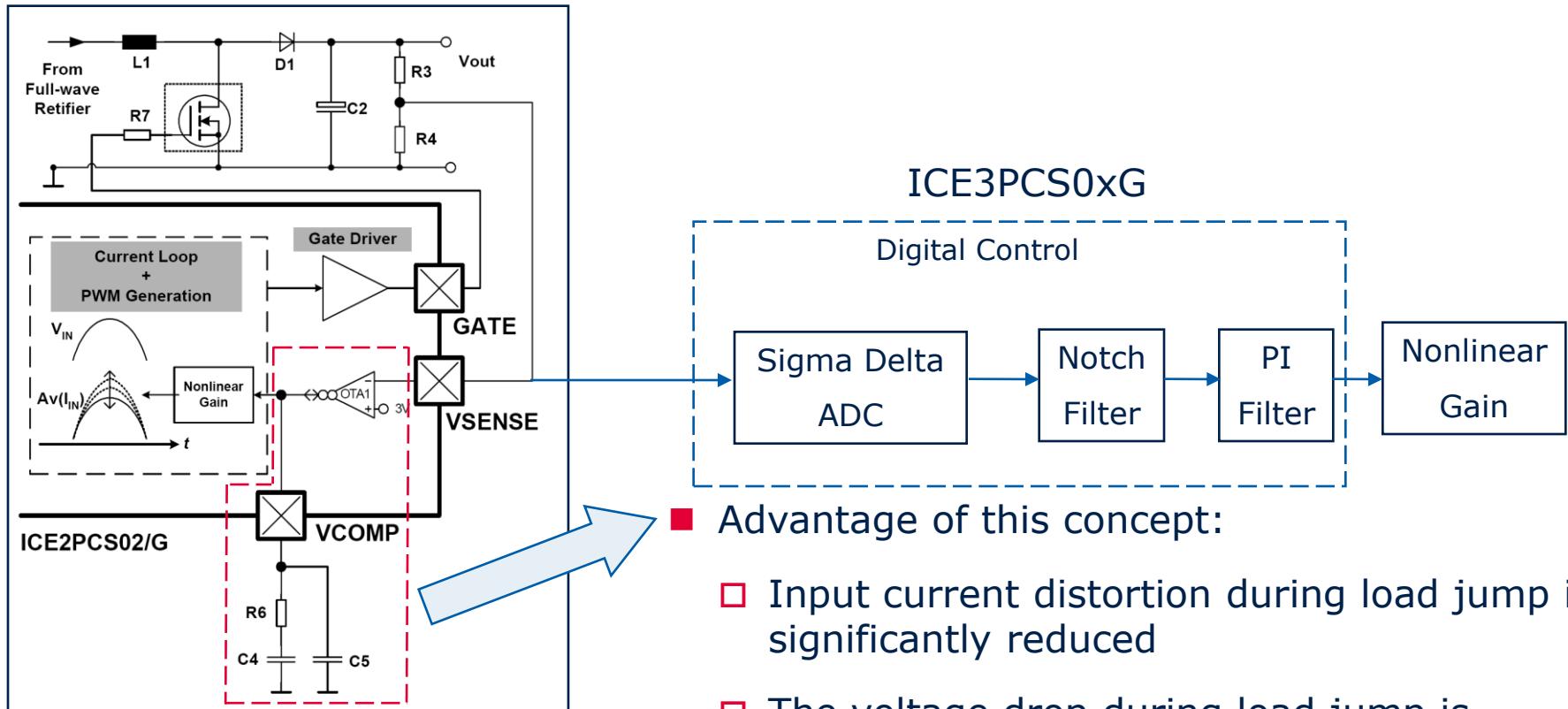
- Power Factor Correction Continuous Conduction Mode Converter
- Infineon CCM PFC family
- 3<sup>rd</sup> Generation Infineon CCM PFC
  - Features
  - Functionality
  - 300Watt Demoboard results

- Low Peak Current Limit (0.2V)
- Average current control without direct sinewave reference signal sensing
- Adjustable operating frequency (20kHz - 250kHz)
- Synchronous frequency (50kHz – 150kHz)
- Boost Follower Mode with adjustable bulk voltage at low step
- Accurate Brown Out protection
- Second Over Voltage protection (OVP2)
- PFC enable function
- Enhanced dynamic response without current distortion
- Digital Control Voltage Loop
- Simple and easy design with very few external components reduces system and assembling cost.
- Supports the trends: High efficiency, High power factor, High Power Density and Low System Cost
- Target Applications: PC, Server, TV, gaming console, Adapter

# Outline

- Power Factor Correction Continuous Conduction Mode Converter
- Infineon CCM PFC family
- 3<sup>rd</sup> Generation Infineon CCM PFC
  - Features
  - Functionality and 300Watt demo board results

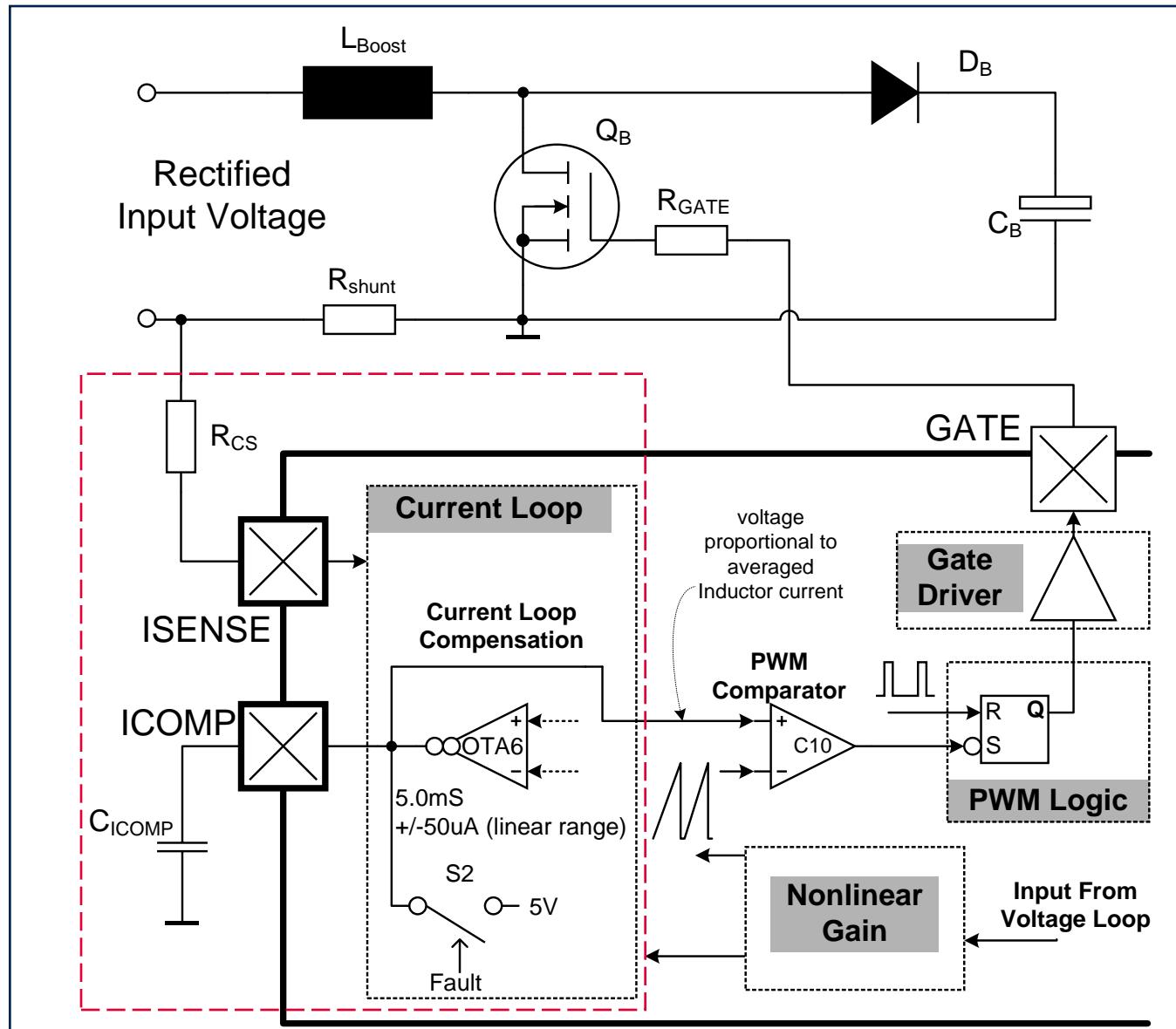
# Voltage Loop Control



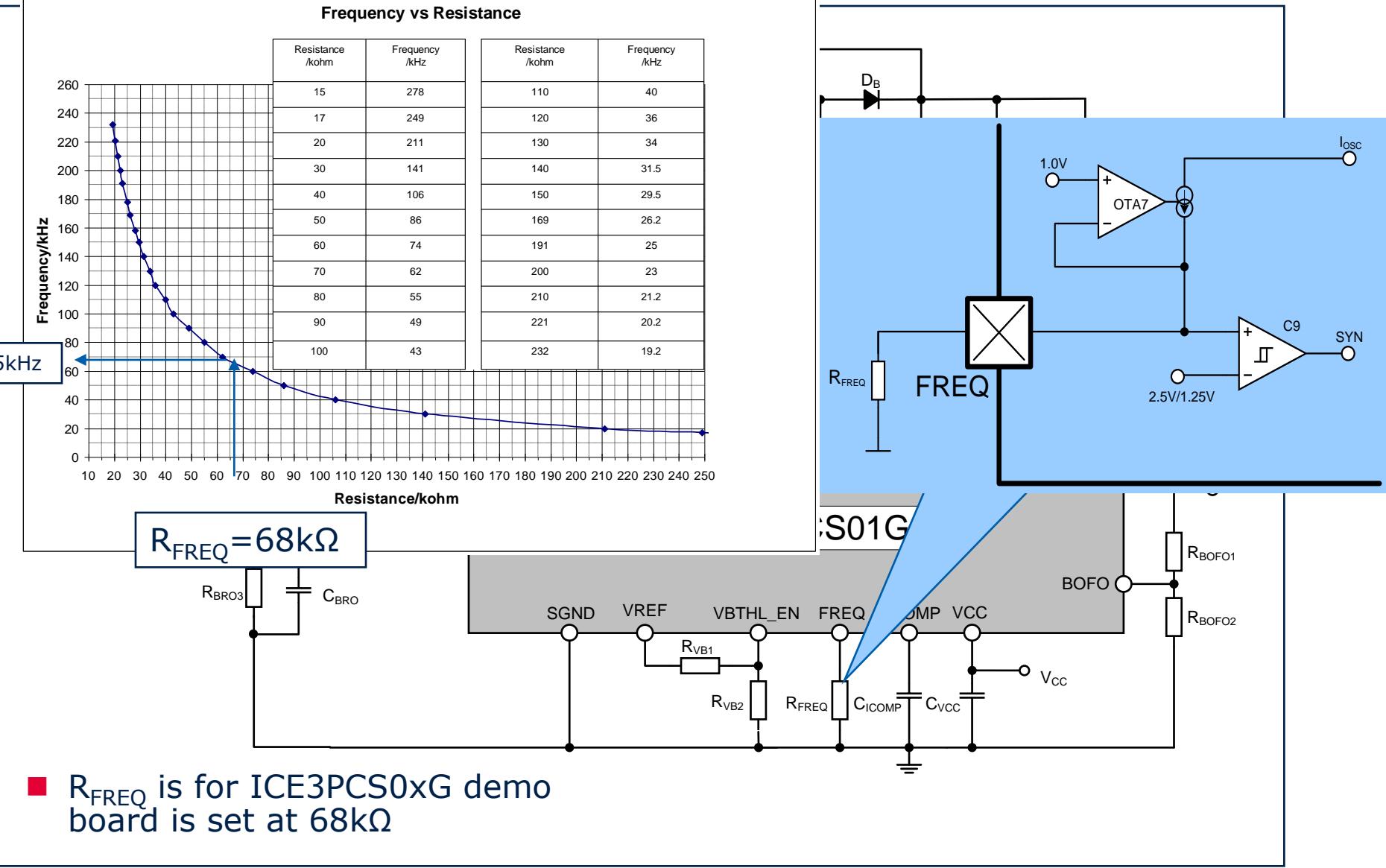
- Example of voltage loop compensation for ICE2PCS0X.

- Advantage of this concept:
  - Input current distortion during load jump is significantly reduced
  - The voltage drop during load jump is reduced and allow bulk capacitor size reduced.
  - The external pin (e.g. VCOMP) for adjusting the control bandwidth is not needed.

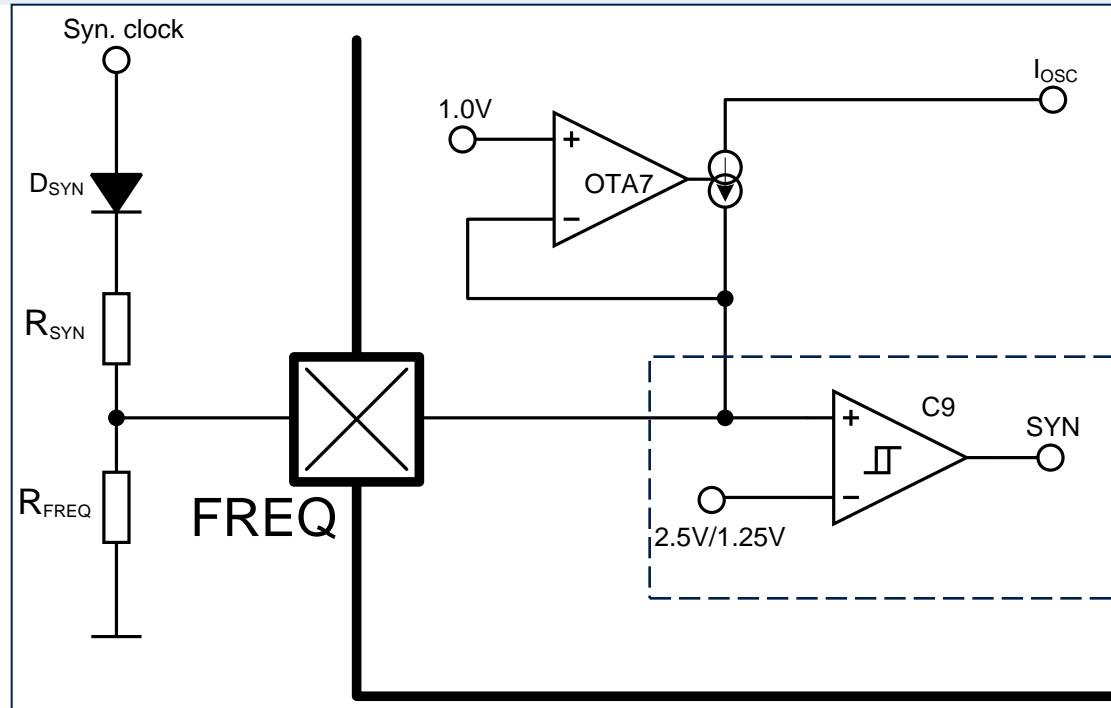
# Current Loop



# Adjustable Switching Frequency

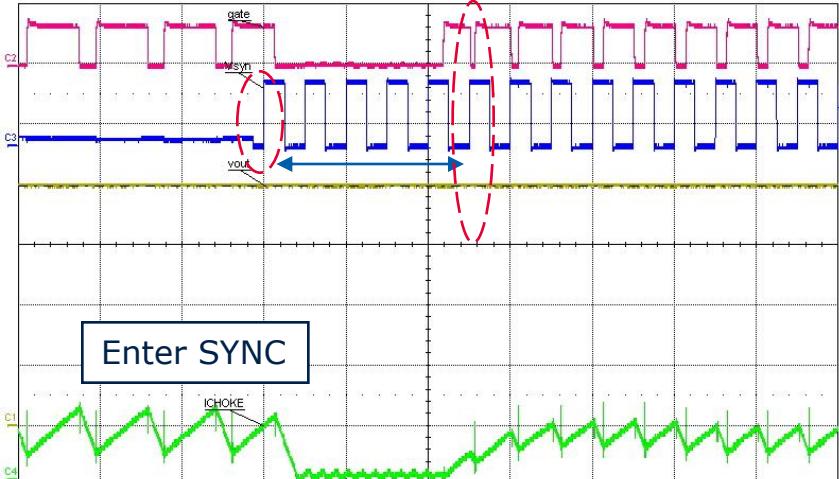


# Gate Synchronisation



- Switching frequency can be synchronized to external pulse signal after 6 external pulses delay once the voltage at FREQ pin is higher than 2.5V.
- The IC will only synchronize with external signal frequency between 50kHz to 150kHz and the duty on should be within 10% to 70%.
- During synchronization, the IC is able to track with external changing frequency.

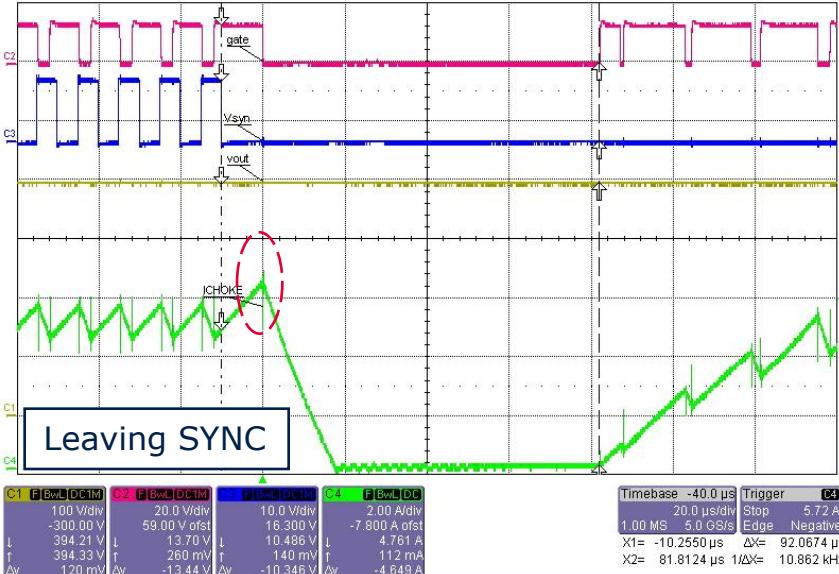
# Gate Synchronisation



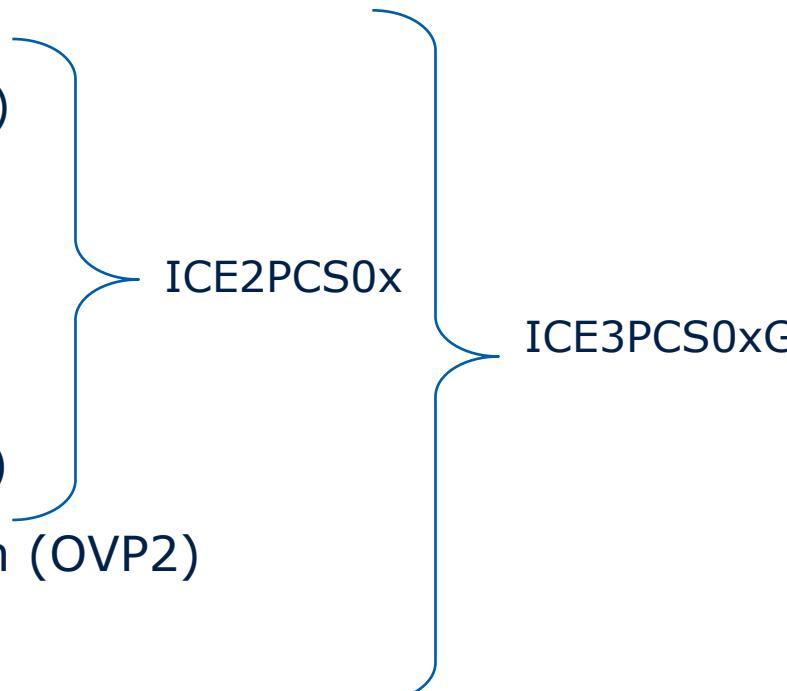
## Legend:

RED	=Gate
Blue	=External Synchronous Signal
Yellow	=Bulk Voltage
Green	=Choke Current

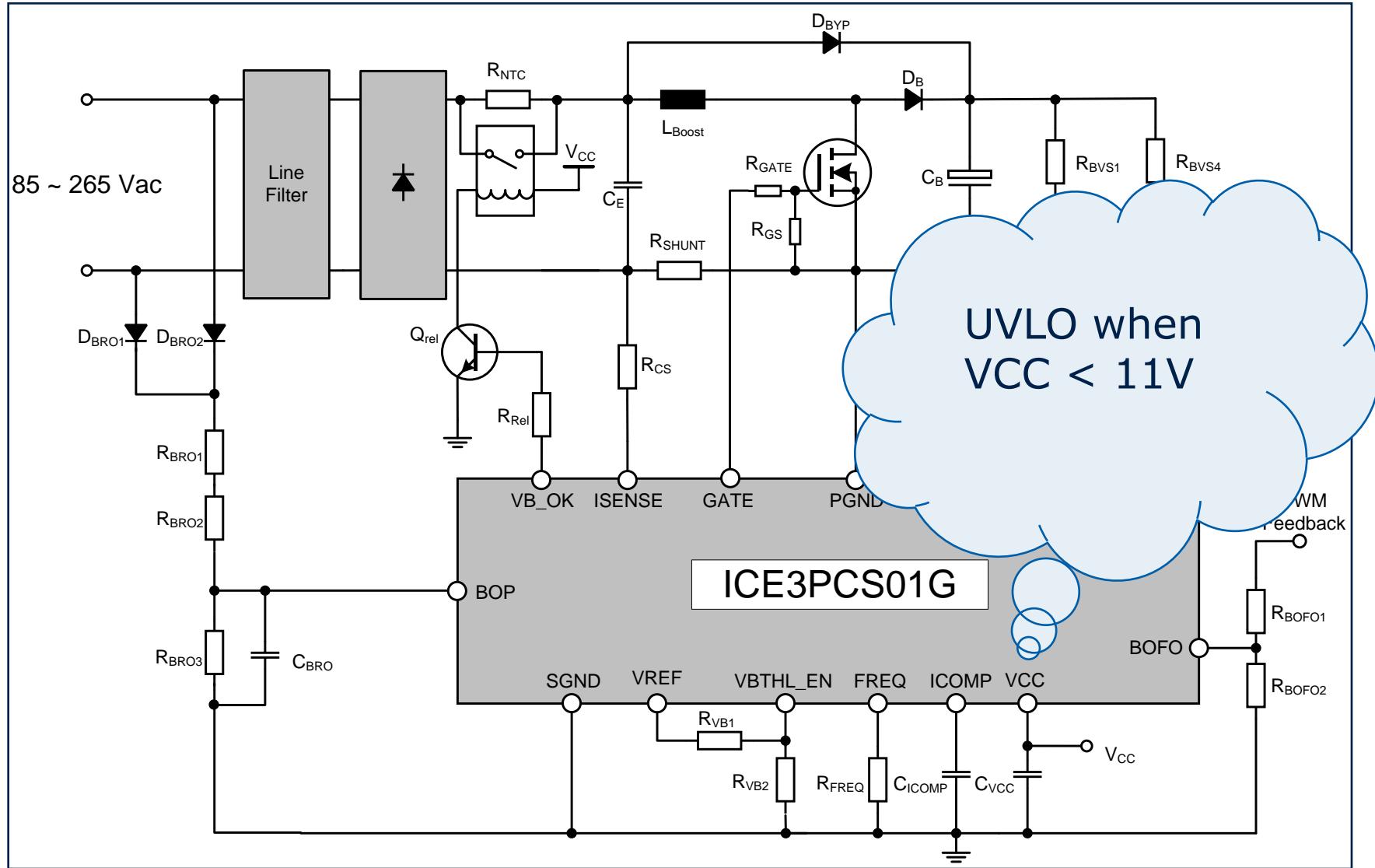
- External signal detect when voltage at FREQ pin higher than 2.5V
- Gate will sync with external signal within 6 pulses.
- Falling edge of IC's gate signal is in phase with external signal's rising edge.
- When external signal at pin FREQ (pin5) is lost, IC will trigger 'Peak Current Limit' because gate will only shut down when it detect a rising edge of the external signal hence the IC gate switching will return to its original switching frequency which is defined by  $R_{FREQ}$ .



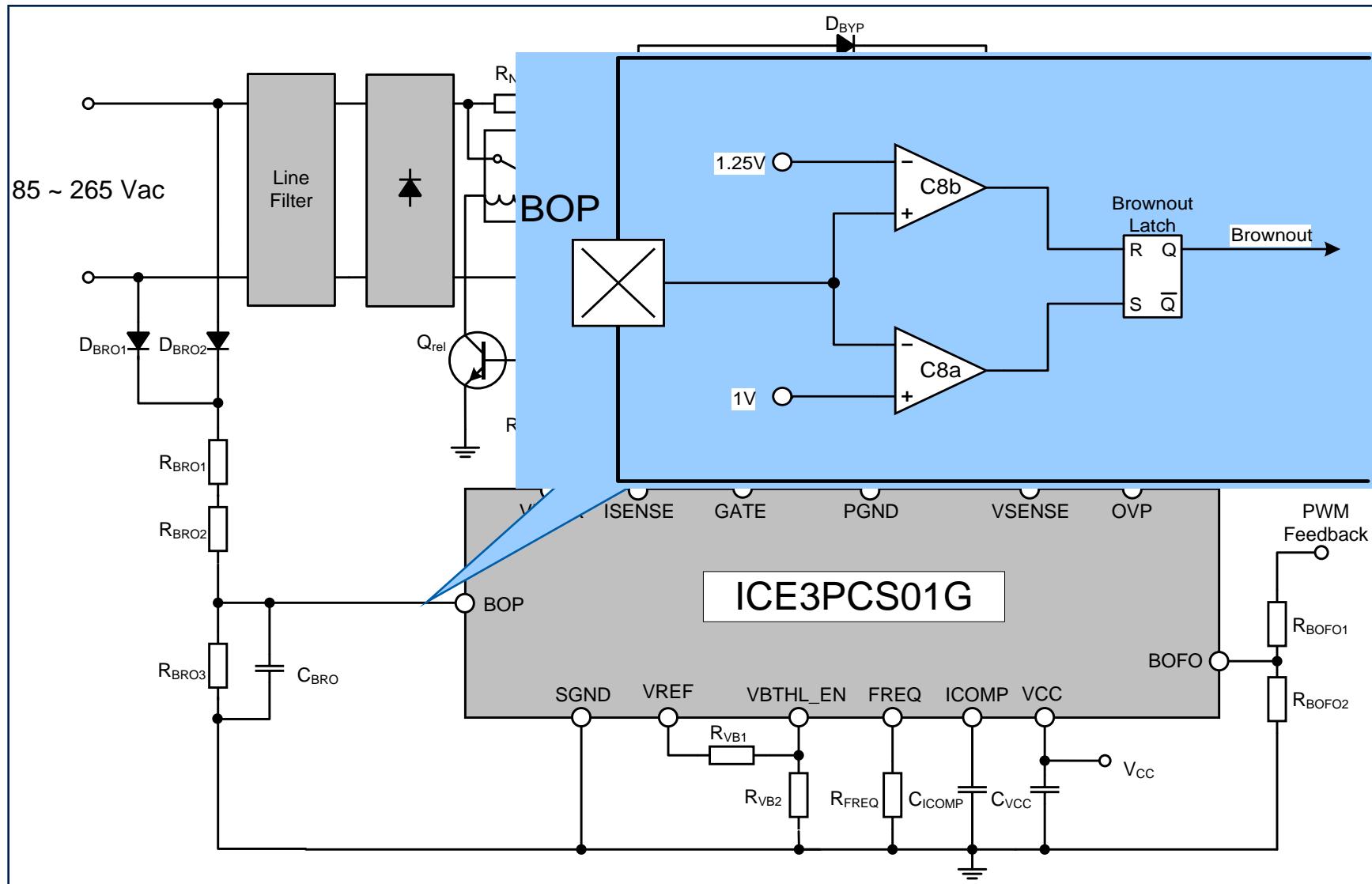
# Protections

- Under Voltage Lock Out (UVLO)
  - Brown Out Protection (BOP)
  - Open Loop Protection (OLP)
  - Peak Current Limit (PCL)
  - Over Voltage Protection (OVP1)
  - Second Over Voltage Protection (OVP2)
  - PFC enable (VBTHL\_EN)
- 
- The diagram illustrates the protection features listed above, categorized into two families: ICE2PCS0x and ICE3PCS0xG. A large curly brace on the right side groups the first six items under the heading ICE2PCS0x. Another curly brace on the far right groups the last three items under the heading ICE3PCS0xG.

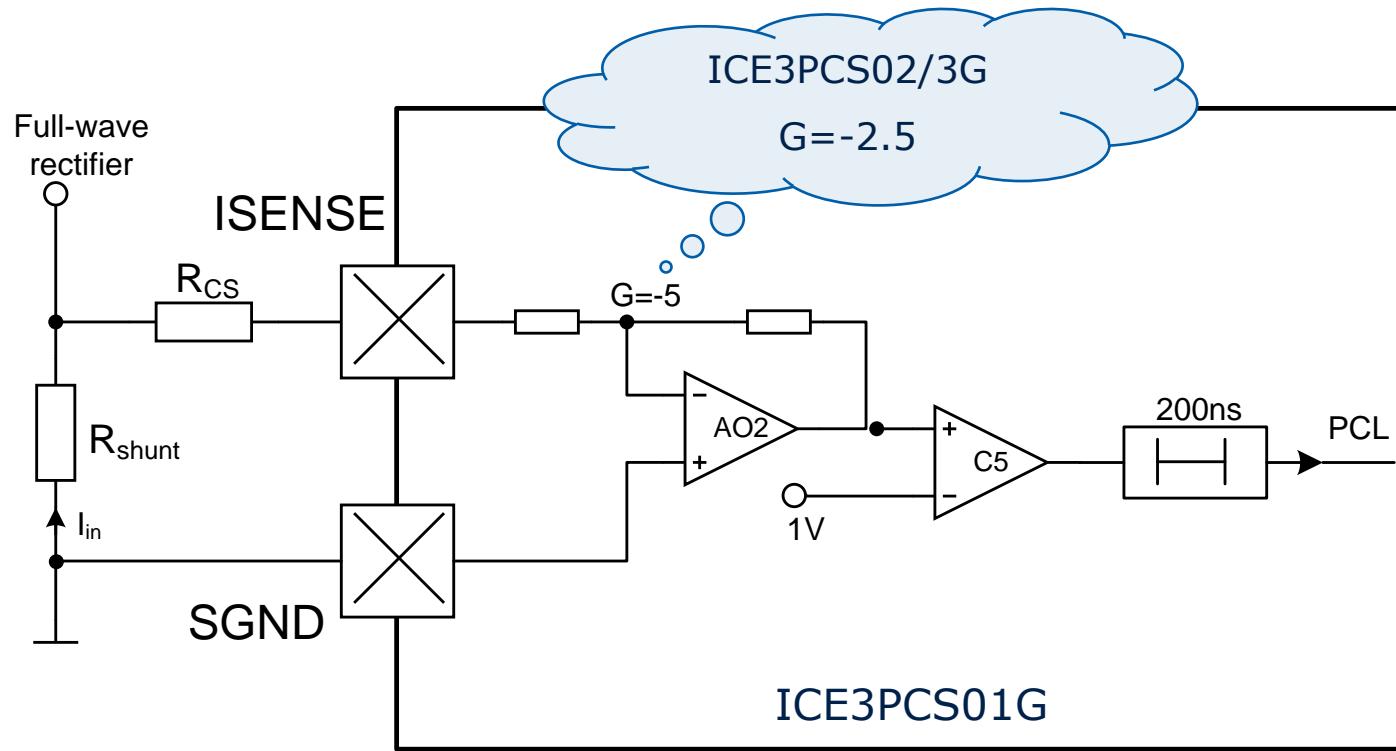
# Under Voltage Lock-Out (UVLO)



# Brown-Out Protection

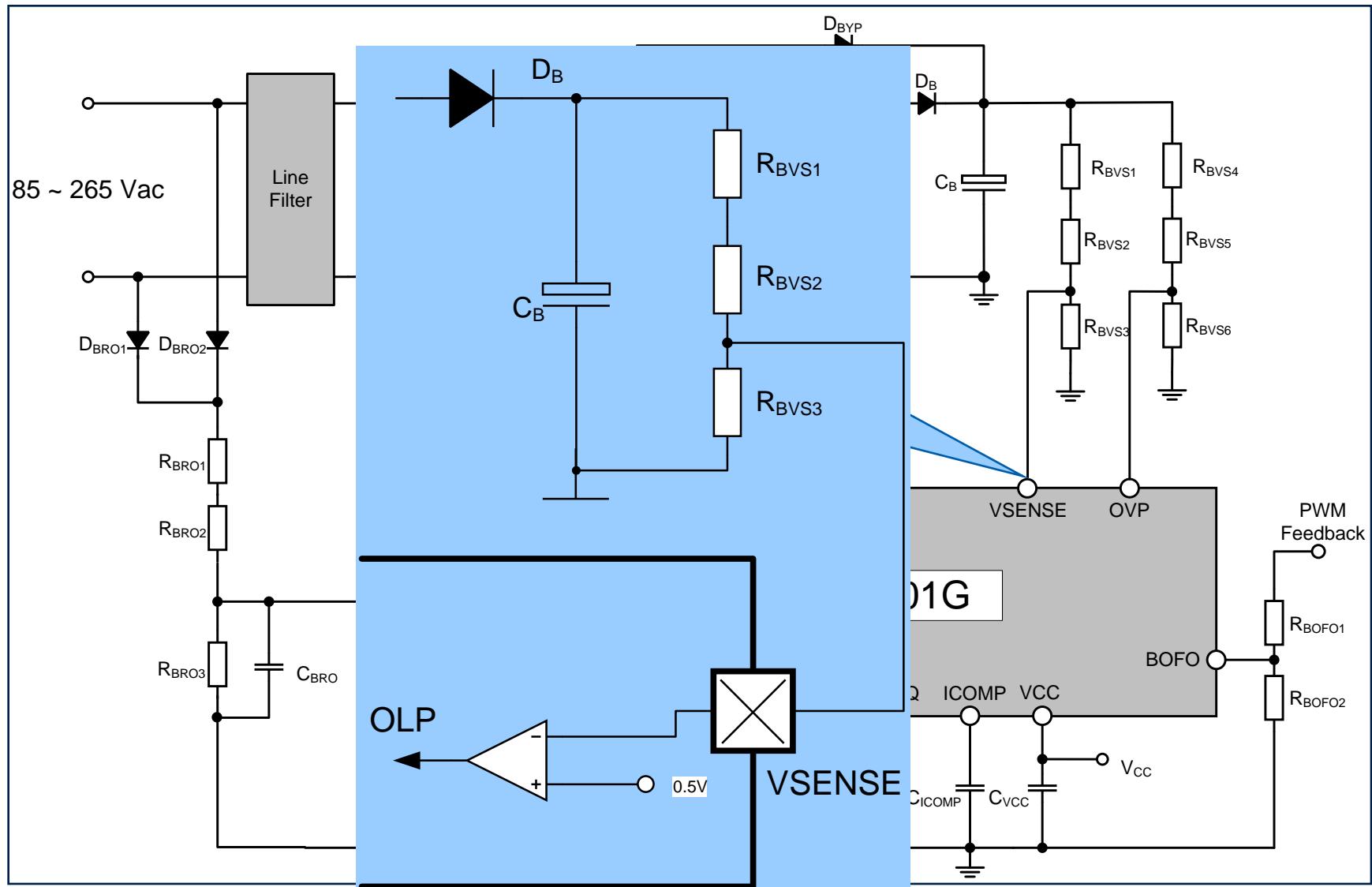


# Low Peak Current Limit Threshold

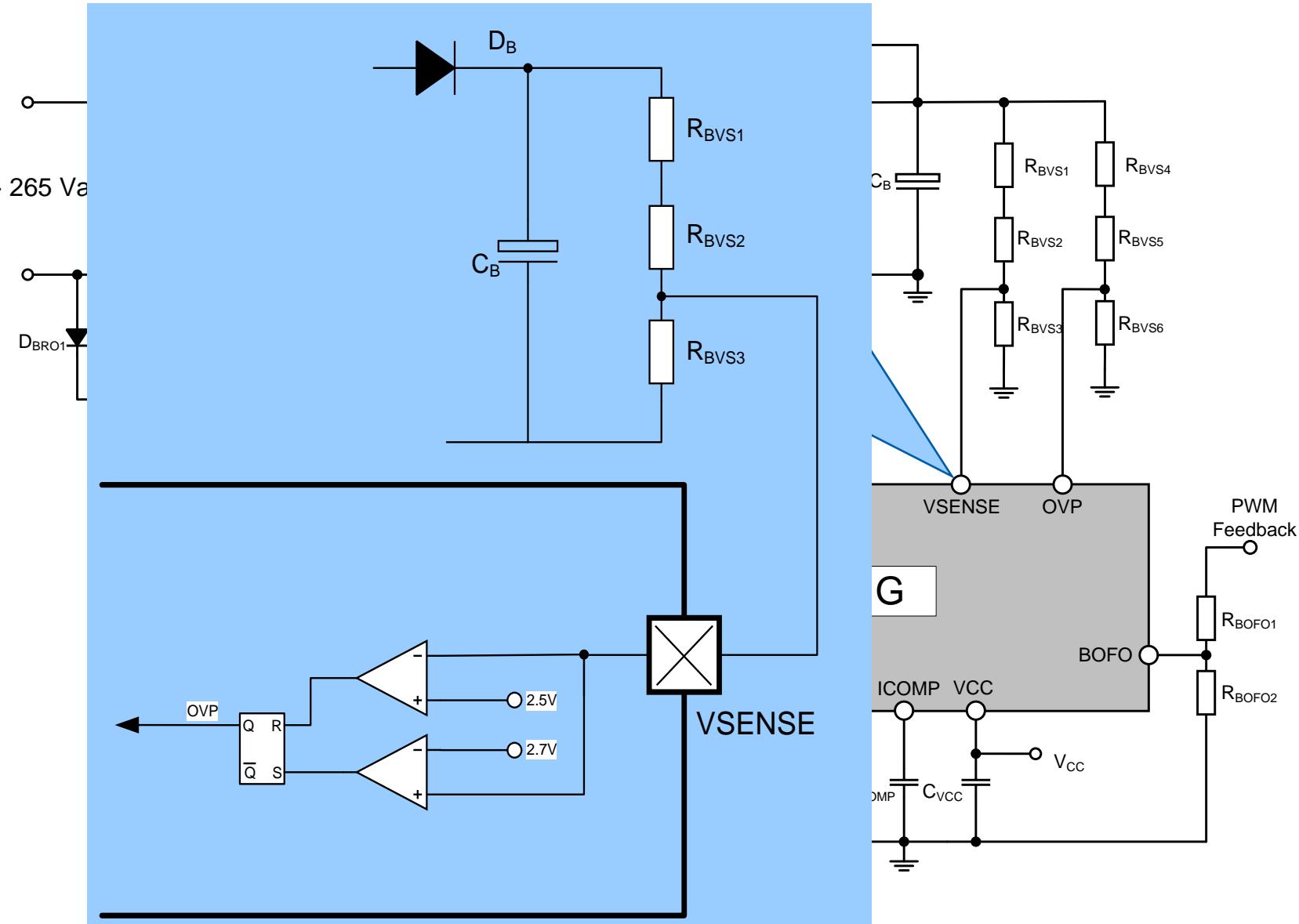


- Low Peak Current Limit:
  - ICE3PCS01G = -0.2V
  - ICE3PCS02/3G = -0.4V

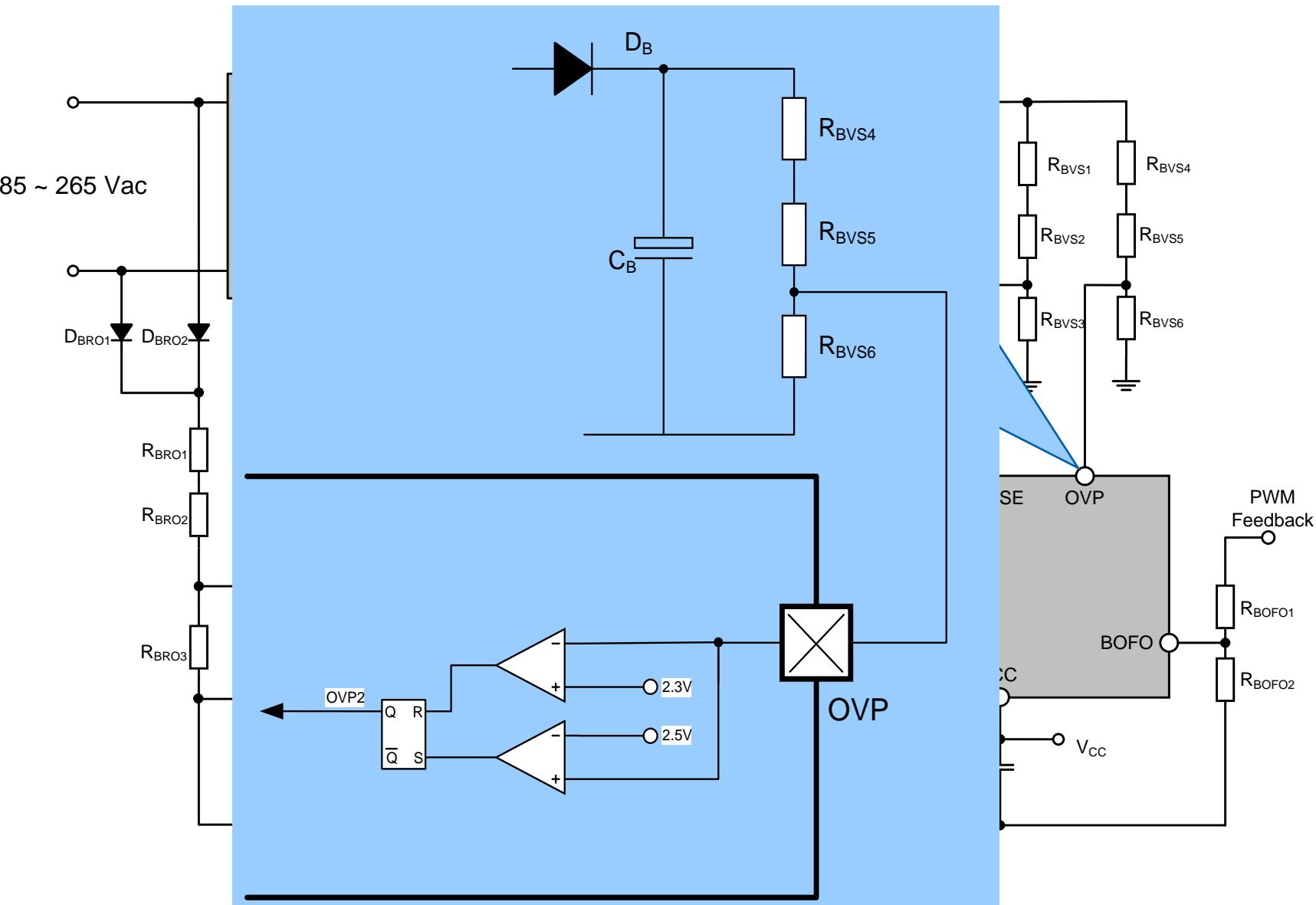
# Open Loop Protection



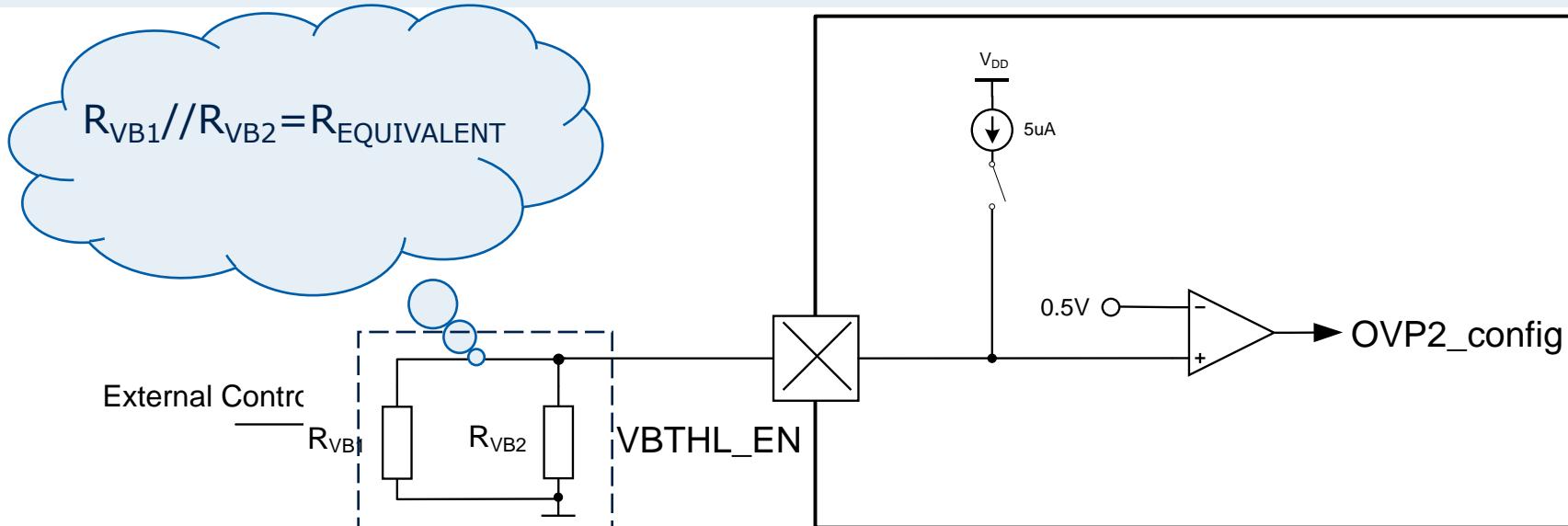
# First Over Voltage Protections (OVP1)



# Second Over Voltage Protections (OVP2)

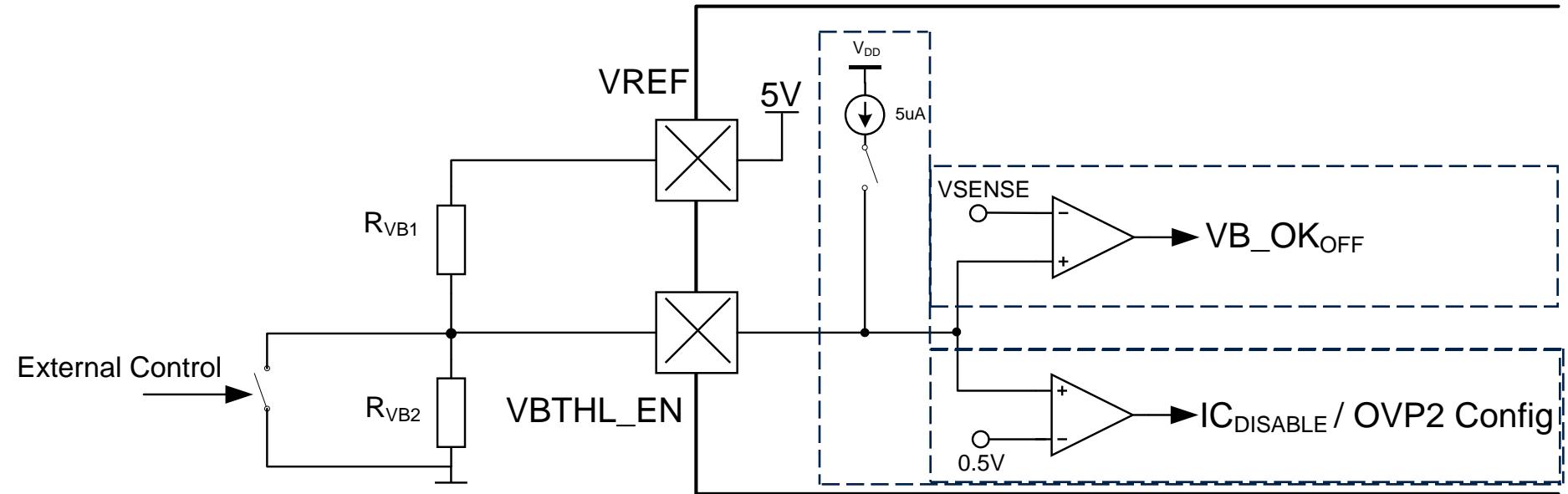


# Mode Selection for Over Voltage Protection 2 (OVP2) – During Start-Up



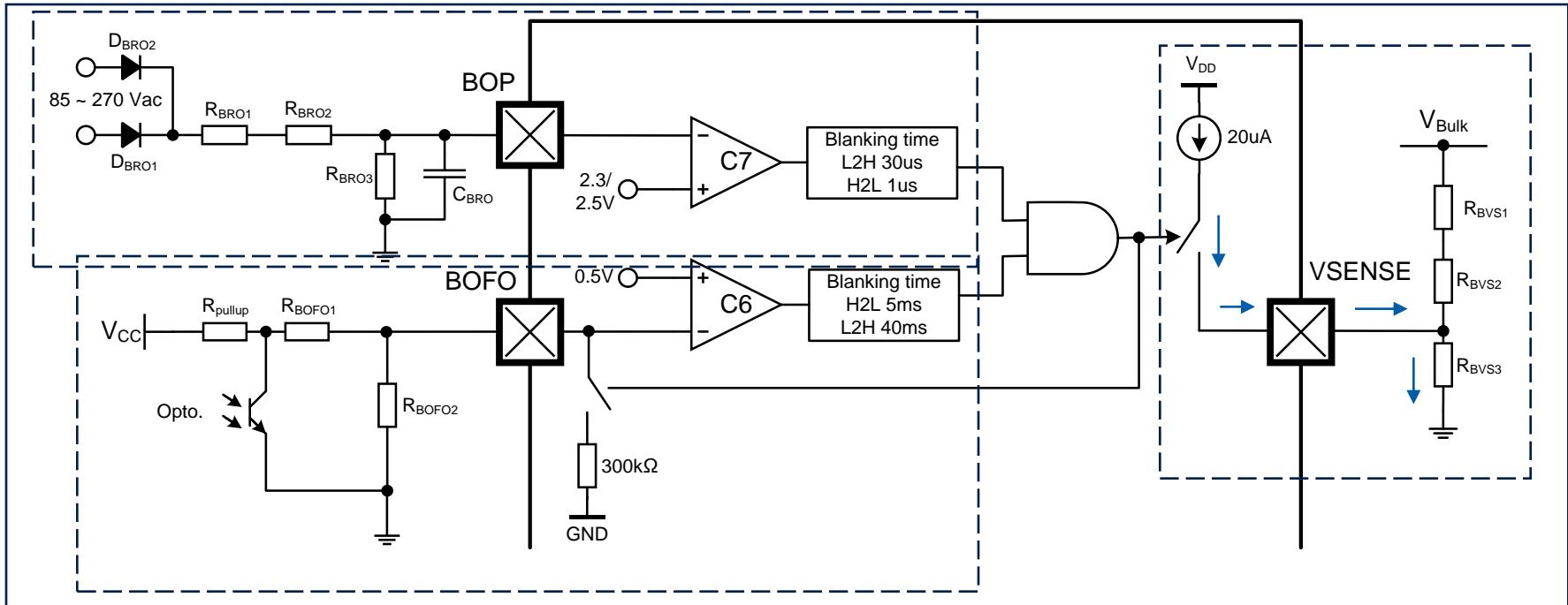
Condition	Default Mode (restart)	Alternative Mode (latch)
	$VBTHL\_EN < 0.5V$ $(R_{EQUIVALENT} < 100k\Omega)$	$VBTHL\_EN > 0.5V$ $(R_{EQUIVALENT} > 100k\Omega)$
OVP2 detected	Gate disable The IC auto softstart as soon as OVP2 is not detected anymore	Gate disable IC latched until next UVLO
OVP1 detected then OVP2 detected	Gate disable (IC resumes regulation as soon as OVP1 is not detected anymore)	

# Pin VBTHL\_EN



- Define OVP2 mode
  - Latch Mode
  - Auto restart
- Turn off threshold for  $VB\_OK$  signal
- PFC enable function

# Boost Follower Mode



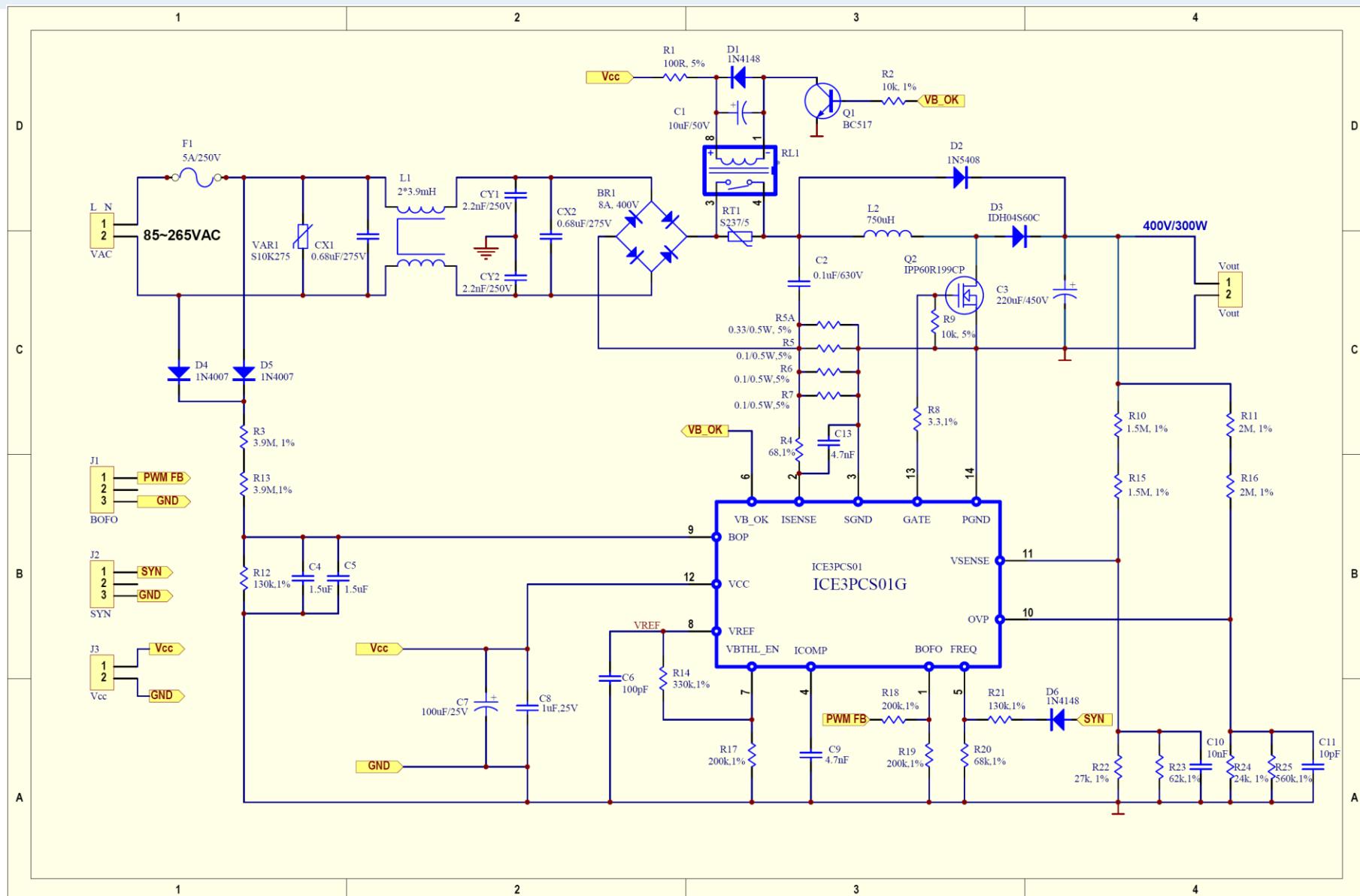
## Boost Follower mode:

- Light load detection from PWM\_feedback signal is lower than 0.5V at the pin BOFO.
- Line voltage detection which is lower than 2.3V at pin BOP.
- 20uA current will flow out of VSENSE pin during boost follower mode

# ICE3PCS01G's 300W Demoboard Description

- Board power rating = 300W
- Input Voltage = 85VAC~265Vac
- Output Voltage = 400V
- Efficiency = >95%
- Switching frequency = 67kHz

# Schematic of ICE3PCS01G Demoboard

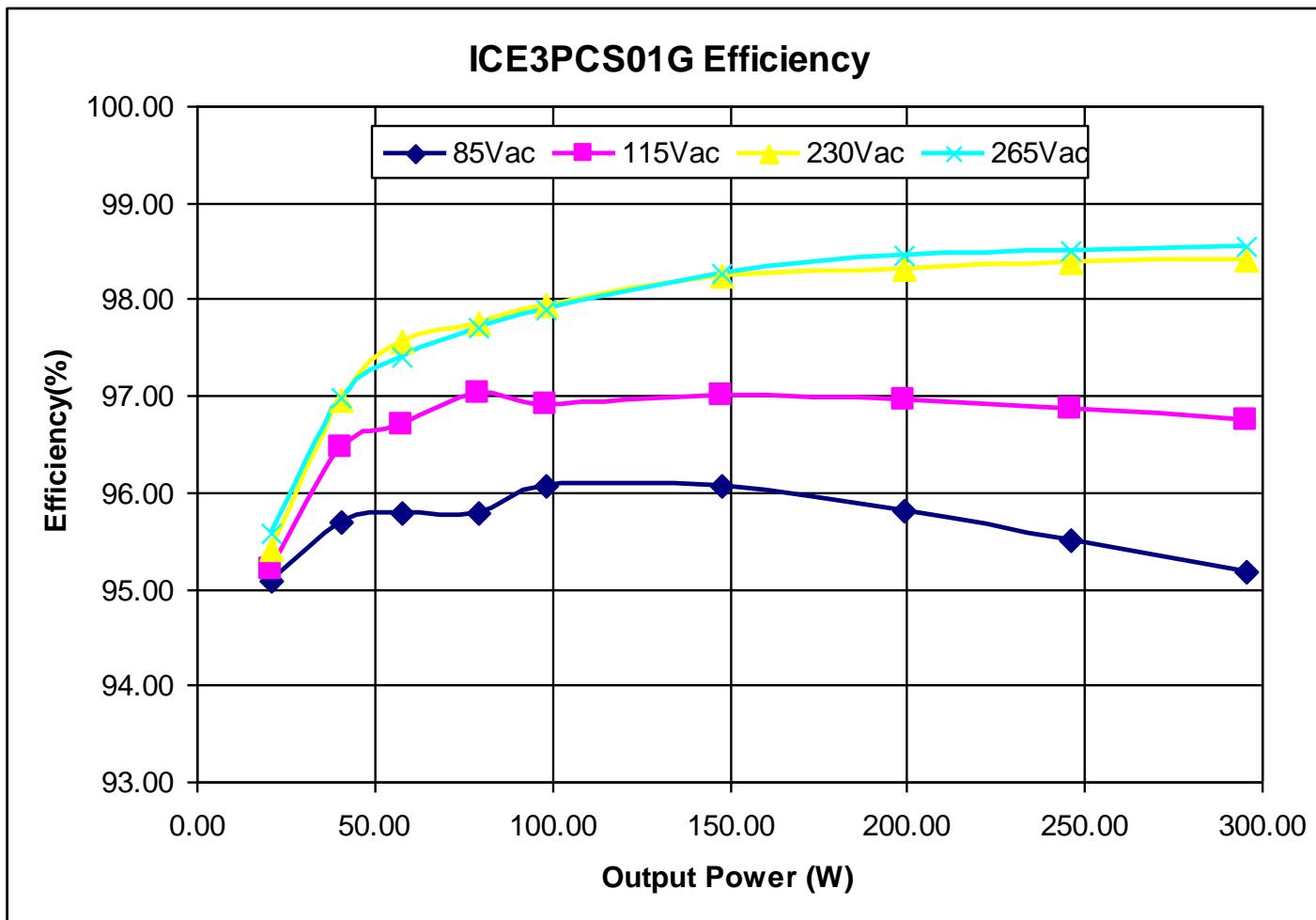


# ICE3PCS01G's 300W Demoboard

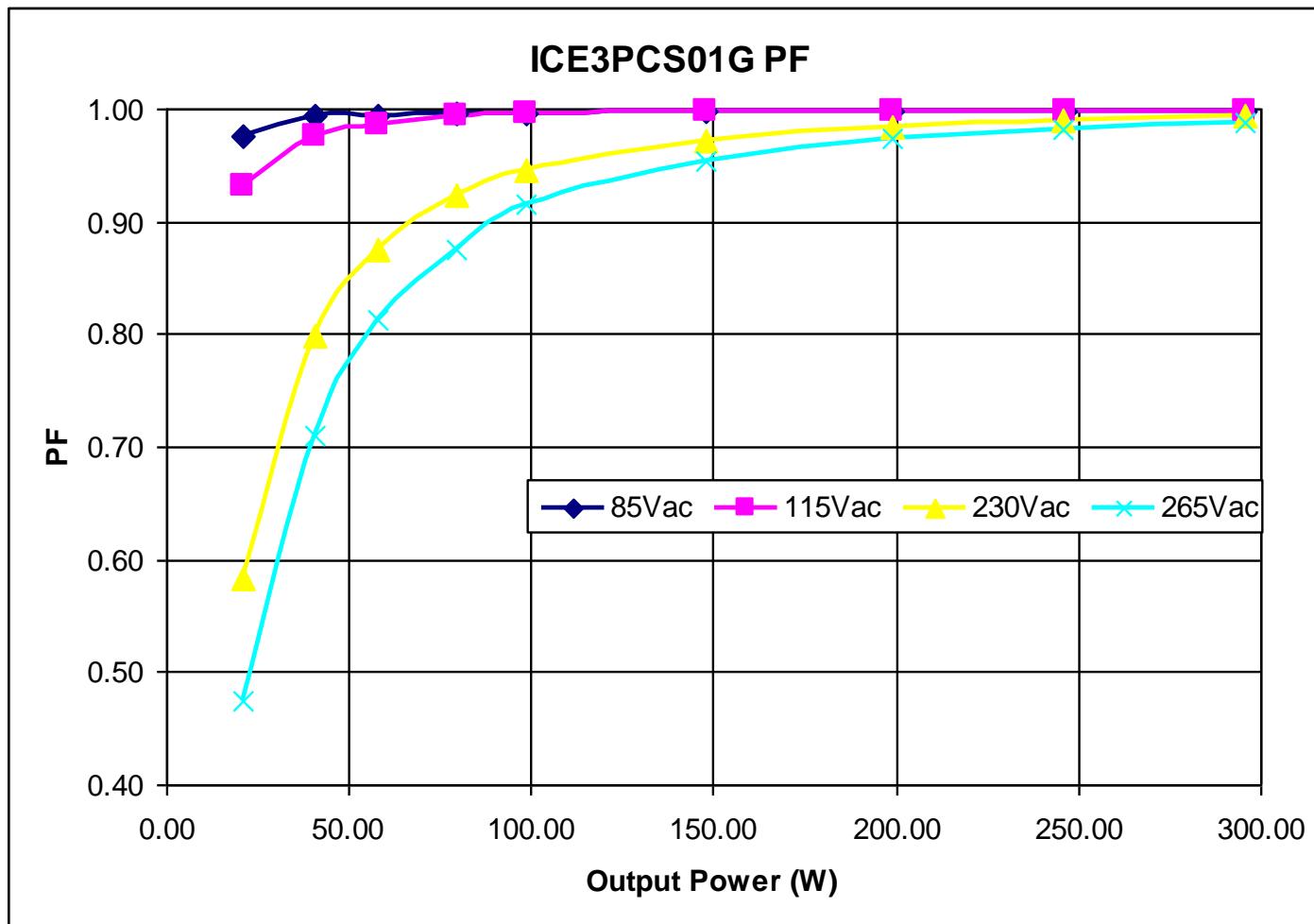


# Performance of Evaluation Board

## Efficiency Vs Output Power

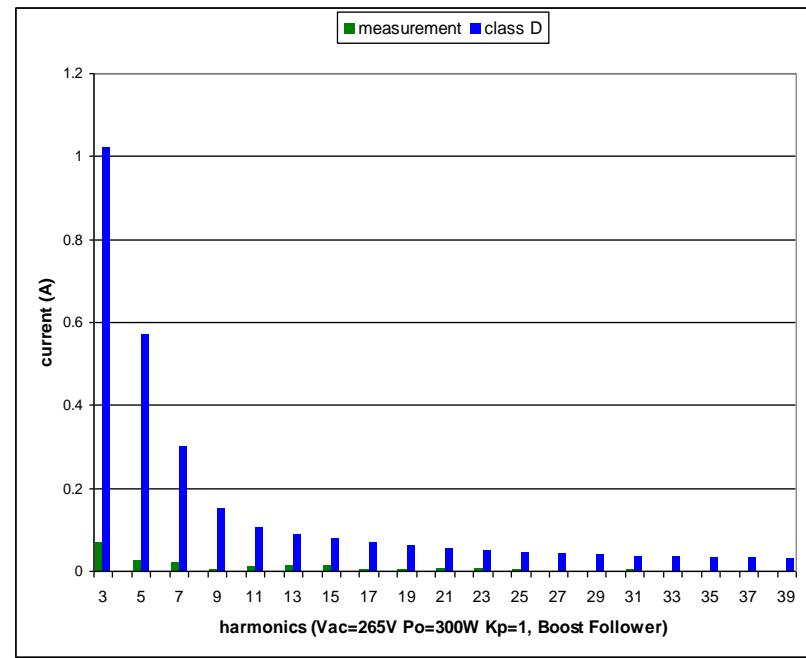
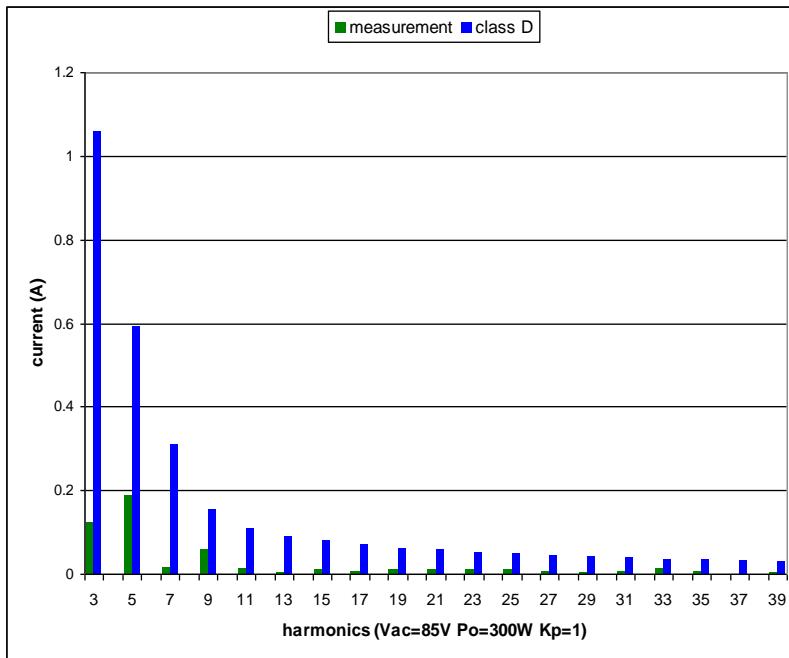


# Performance of Evaluation Board Power Factor Vs. Output Power



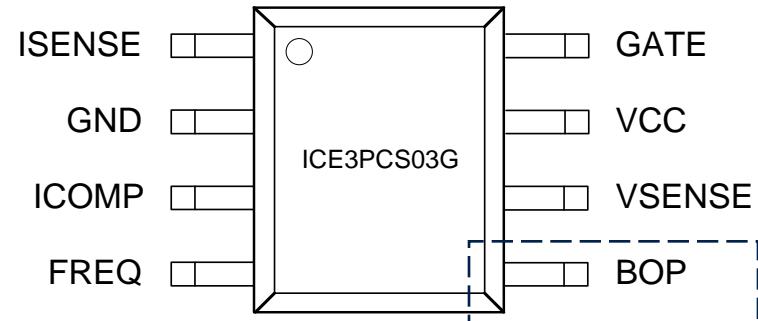
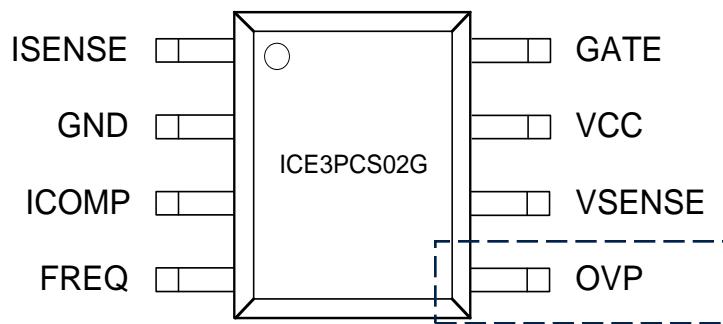
# Performance of Evaluation Board

## THD



# ICE3PCS0xG in 8-pin

## Other ICE3PCS0XG family



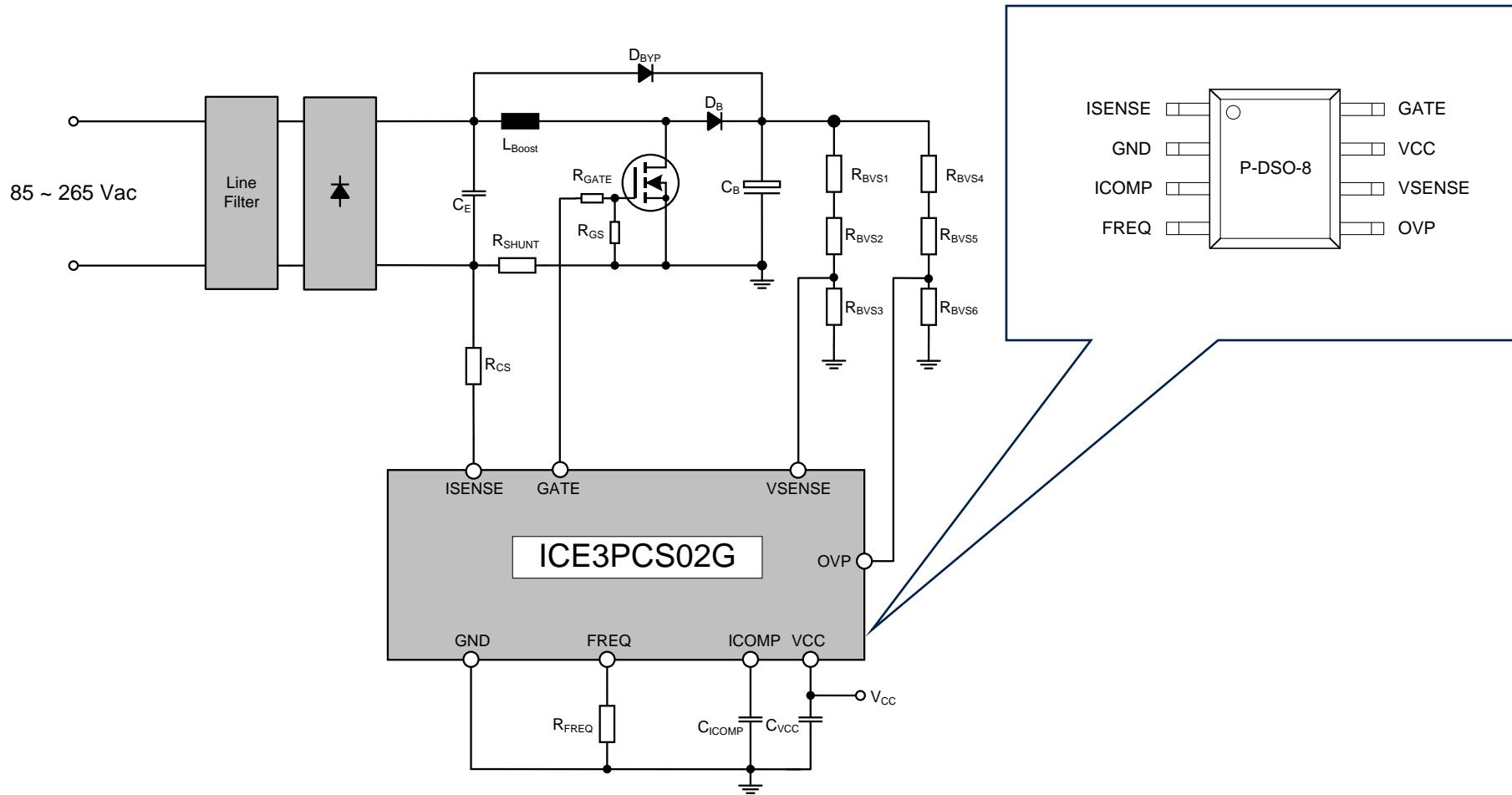
- The difference between ICE3PCS02G and ICE3PCS03G is at pin 5

# Summary of ICE3PCS0xG Family

Function \ Product	ICE3PCS03G	ICE3PCS02G	ICE3PCS01G
digital control voltage loop	YES	YES	YES
variable frequency	YES	YES	YES
synchronous frequency	YES	YES	YES
open loop protection	YES	YES	YES
low peak current limit	-0.4	-0.4	-0.2
brown out protection	YES		YES
over voltage protection	YES	YES	YES
second over voltage protection		YES	YES
PFC enable function			YES
boost follower mode			YES
5V regulator			YES

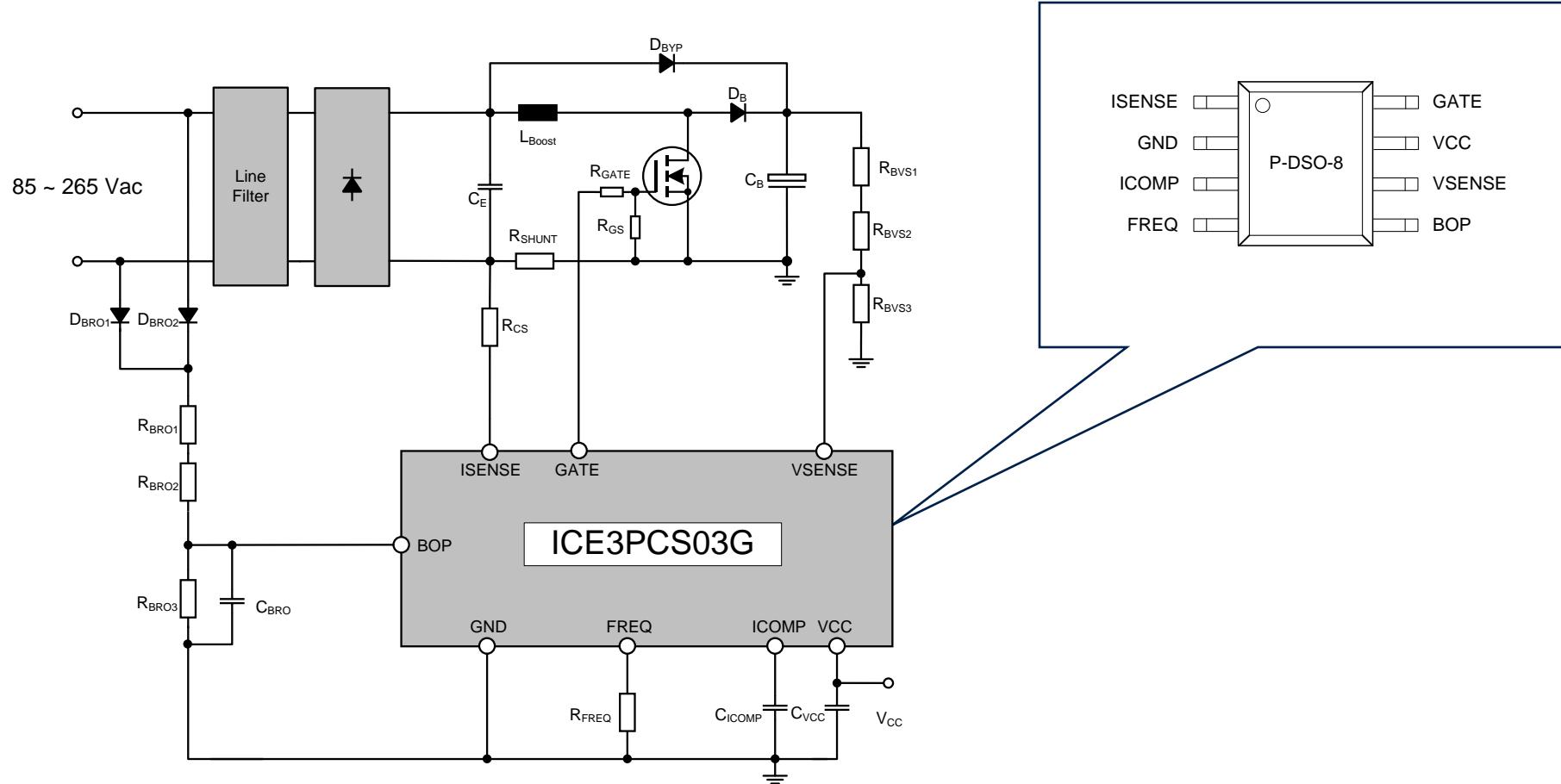
# Typical Application Circuit

## ICE3PCS02G

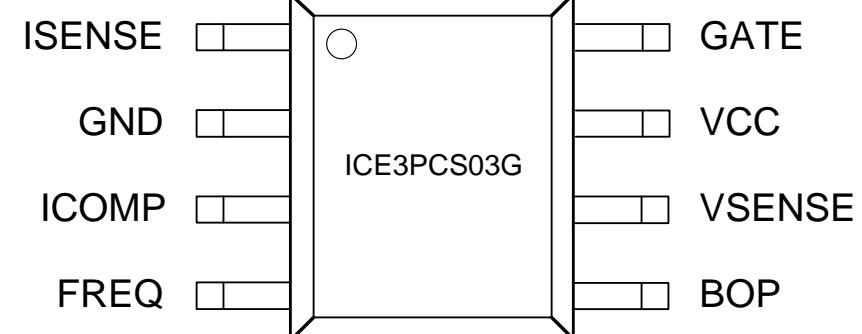
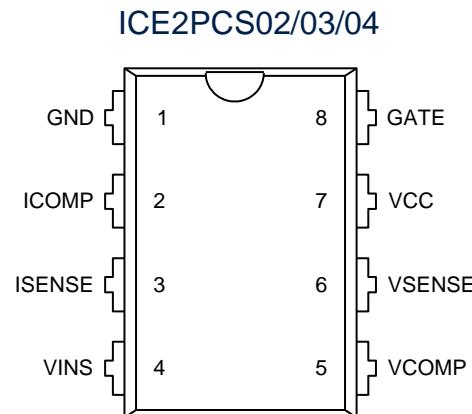
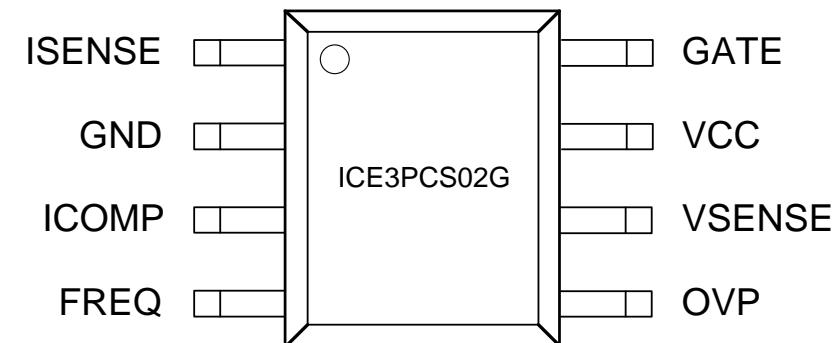
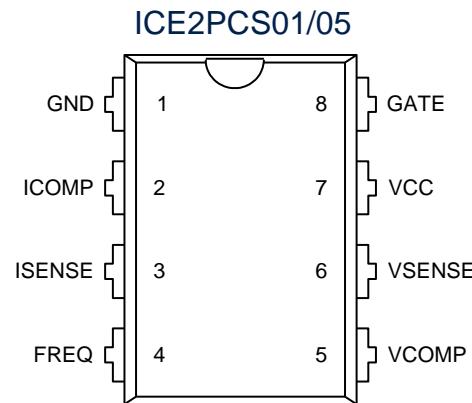


# Typical Application Circuit

## ICE3PCS03G



# Pin layout comparison between 8-pin ICE2PCS0x Vs ICE3PCS02/3G



# Features comparison

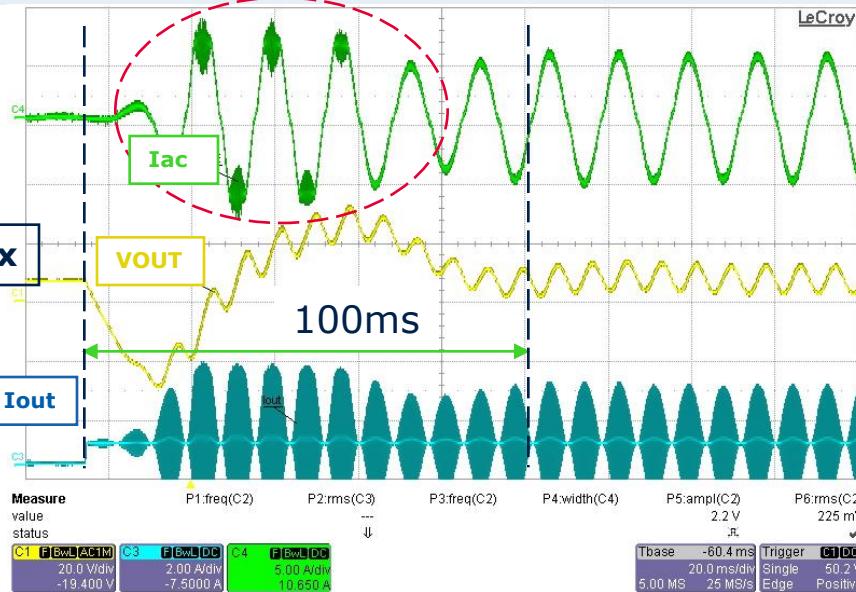
Features	ICE2PCS0x	ICE3PCS02/03G
Voltage loop compensation	External and Analogue	Integrated and Digital
Peak current limitation threshold	-1.0V	-0.4V
Dynamic response	Fair	Excellent
Operation frequency setting	ICE2PCS01/05 → adjustable	Adjustable from 21kHz to 250kHz
	ICE2PCS02/03/04 → fixed	
Brownout protection	ICE2PCS02/03/04 → integrated	ICE3PCS03→integrated
Two Over voltage protection	None	ICE3PCS02→integrated

# Features comparison

Improvement	ICE2PCS0x	ICE3PCS02/03G
Voltage Loop	The compensation of the voltage loop is installed at pin VCOMP	The compensation of the voltage loop is installed inside the IC with digital control.
SOC	Yes, induce over-high peak current design	Removed and -0.4V OCP threshold can limit maximum peak current in worst case without over-current design while save power loss on $R_{SHUNT}$
Enhance Dynamic Response (EDR)	Yes, induce input current distortion during startup and load dynamic where bulk voltage varies over $\pm 5\%$ detection window of EDR block	Removed and bulk voltage dynamic response is guaranteed by the integrated digital voltage loop

# Line Jump (0W->300W)

**ICE3PCS0x**



ICE3PCS0x

ICE2PCS0x

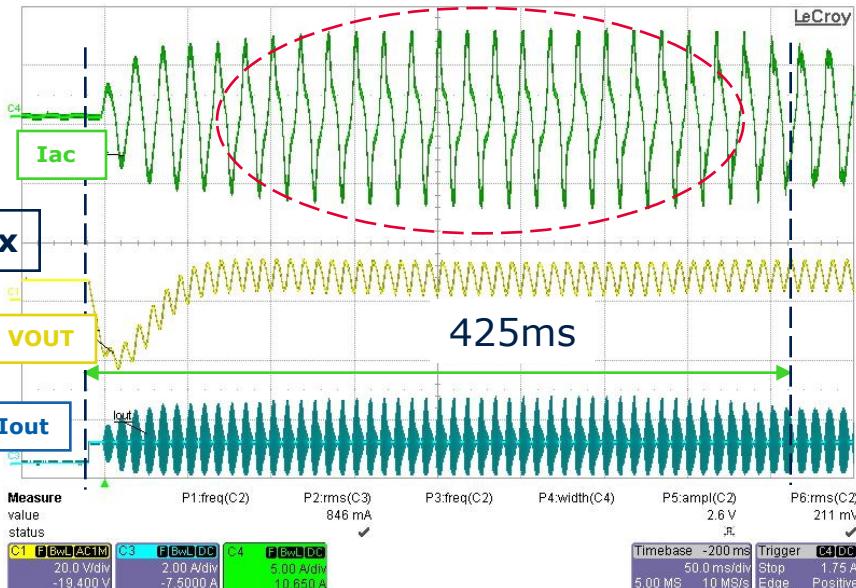
Shorter recovery time

Longer recovery time

No current distortion

Current distortion during recovery period

**ICE2PCS0x**







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