On the loss - softness trade-off: Are different chip versions needed for softness-improvement?

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Introduction

In almost any area of engineering developers are striving for technically best performing and cost effective solutions. It is a general trend that technologies are squeezed out to their limits (hopefully, without exceeding those). As a result the market asks for more and more specifically optimized solutions instead of using "one size fits all" parts. IGBT technology can not drop back from this trend and as a result the latest chip generations are offered in several versions to address specific application needs. Infineon's latest 1200V IGBT4 chip generation, for instance, has come in three versions optimized for low, medium and high power applications.
Driving force for these distinctions have been

	T4	E4 >75A	P4
Vcesat@125°C [V]	2,05	2	2
Eoff@125°C [%]	100	120	170
Rth [%]	100	100	100
typical Currentrange	up to 450A	200A - 1400A	600A - 3600A

Table 1: IGBT4 from Infineon - tradeoff Turnoff losses – saturationvoltage

varying switching softness requirements related to the applications power or rated current level, respectively. An important influencing factor is given by the implemented stray inductance of the set-up. Increased softness, however, trades off against switching losses from the technology point of view. The aim of this work is to address the effects of stray inductances on the switching performance of the available chip versions in order to derive guidelines for application designs and to investigate pros and cons for choosing one of the given chip optimizations. Besides of switching losses turn-on and turn-off speed, occurrence of snap-off and oscillation (EMI) trends are used as measurement categories. We separate our investigation into a first section addressing turn-on behavior, a second dealing with turn-off, a third addressing diode switching, followed by snap-off considerations for IGBT and diode. Finally we discuss the results with special regards to the overall system performance.

Experimental set-up

In order to investigate and to compare three different chip versions which are designed for different power levels a module has been chosen which is just close to the limits of being reasonable for use with the low power chip optimization. Hence, a 300A half-bridge configuration in the well-known 62mm package has been chosen as a platform and modules have been built with low-, medium and high power 1200V IGBT4 chips, all equipped with the same type of 1200V Emitter Controlled free wheeling diodes (medium power optimization). Table 1 shows a brief overview revealing the

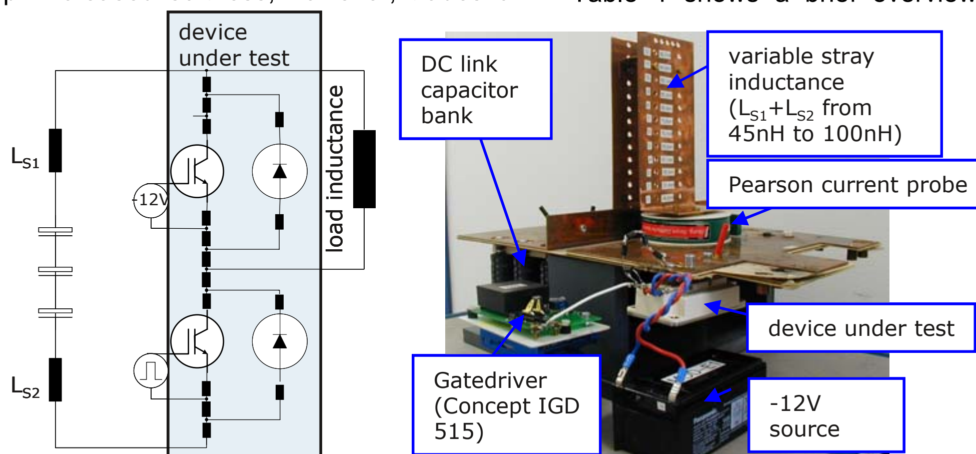

Figure1: Setup for IGBT turn on and off measurements (for turn off measurement of the free wheeling diode the highside IGBT was switched and the load inductance was in parallel to the lowside diode)

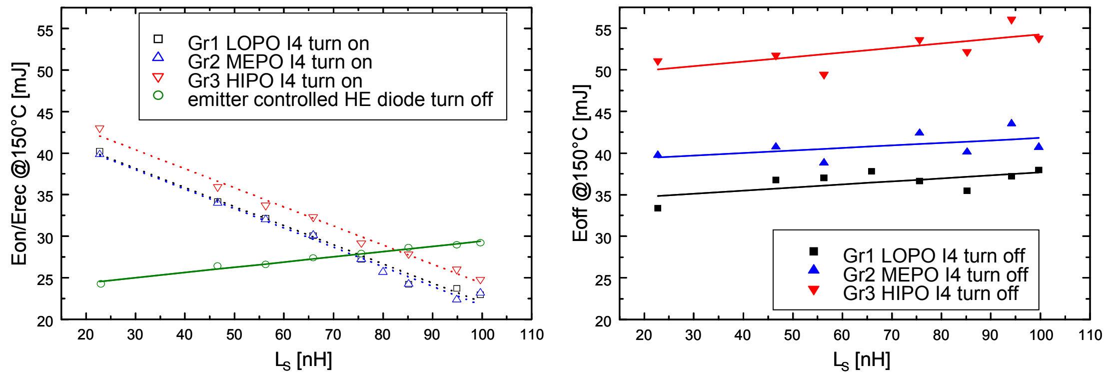

Figure 2: switching losses as function of the stray inductance L_S, the turn on losses of the IGBT (left) will be reduced by increasing the inductance and the turn off losses, both IGBT (right) and freewheeling diode , rise with the inductance.

three trade-off points of Low- Medium- and High Power IGBT and gives a short hint to the current ranges addressed. Obviously, improved softness has to be paid by increasing nominal turn-off losses. In order to obtain more general results the DC-link of the characterization set-up was designed to be adjustable in terms of its parasitic stray inductance (refer to Fig. 1). By this means, the effect of current ratings differing from the investigated 300A level can easily be evaluated, using the ratio of current rating and stray inductance as scaling factor. All switching experiments were performed using the well-known two-pulse dynamic characterization method involving fast Pearson current probes and compensated voltage probes.

Experimental Results
IGBT turn-on

Figure 3 visualizes the effect of two different stray inductances on the turn-on waveforms of a 300A halfbridge equipped with the Low Power IGBT4. In both cases, the same gate drive unit is used. As can easily be seen an increased stray inductance not only increases the inductive voltage drop (dU=-L*dI/dt) at the device terminals after onset of the current rise[1] but also affects the current rise speed dI/dt itself. Even though the turn-on speed is slowed down by the parasitic inductance, the turn-on losses are significantly reduced because roughly a 50% share of the losses results from the initial dI/dt phase during which the above mentioned voltage drop occurs. In the shown Example the losses in this initial switching phase, indicated by the time stamp "a" in Figure 2, are reduced by the increased stray inductance from 30.4 mJ to 12mJ (E = 18.4 mJ).

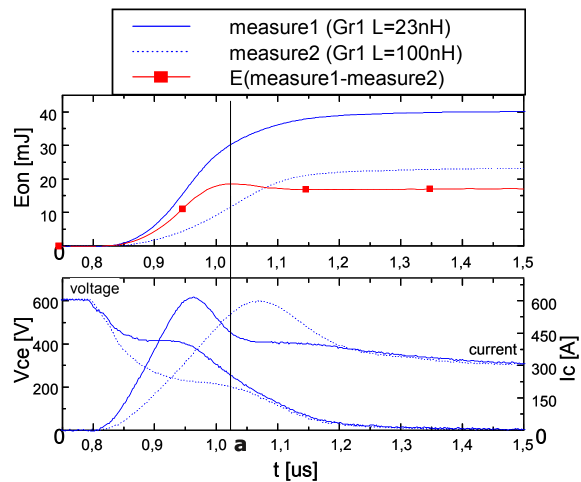

Figure 3: turn on behaviour of a low power IGBT; the diagramm on the top shows the losses as a function of the time for two inductances (solid: L=23nH, doted: L=100nH); the bottom diagramm shows the voltage and the current curves

The second phase of the switching event is characterized by the occurrence of the reverse recovery current peak of the diode and further voltage drop at the IGBT. An increased parasitic inductance leads to a delayed reverse recovery current peak and to increased switching losses during that second phase. Yet, the losses are only by 1.6 mJ higher than in case of the low-inductance set-up, because the IGBT terminal voltage has dropped to small values, already. Regarding the whole switching event, an increased parasitic inductance therefore may significantly reduce turn-on losses. In this case the reduction from 40 mJ to 23.2 mJ corresponds to a benefit of 42%.

[1] In a system without any parasitic inductance the voltage at the IGBT terminals may only drop after the current direction within the diode is inversed, i.e. the full load current is carried by the IGBT, and the diode begins to build-up a reverse voltage.

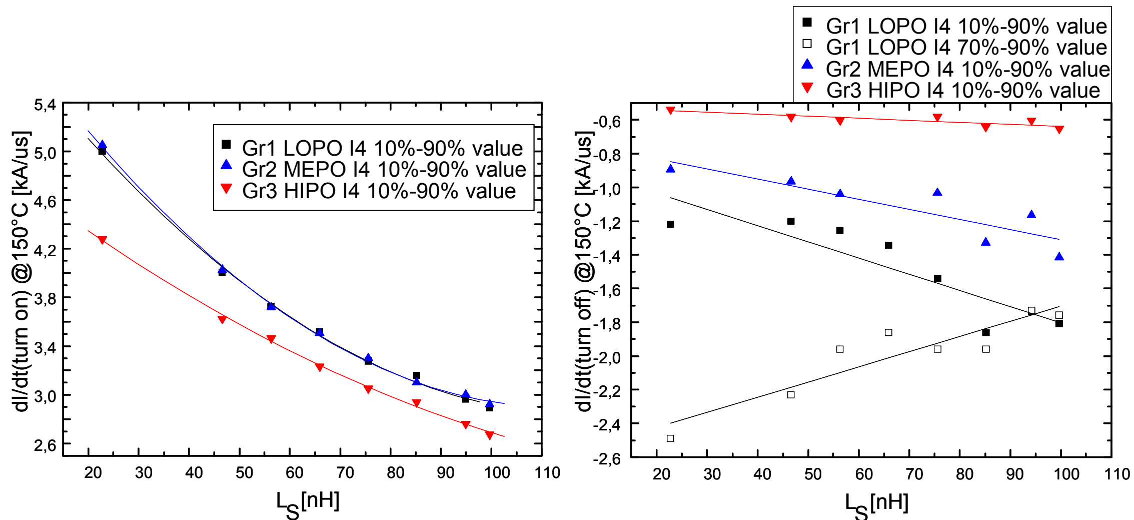

Figure 5: current slope as function of the stray inductance; left: turn on (the 10%-90% value of dI/dt during turn on is normally equal to the maximum value); right: turn off (the 10%-90% value of dI/dt is mostly lower than the maximum dI/dt, which can be described by a 70%-90% value, the difference between both dI/dt values depends by the high of the tail current, which will be reduced with a higher overvoltage peak/ a higher stray inductance)

In Figure 2 IGBT turn-on losses are plotted against the parasitic DC link stray inductance for all three IGBT versions. The dependence is almost linear in the range investigated. However a sublinear behavior is expected for even higher inductance values since the IGBT terminal voltage during turn-on dI/dt may not drop below zero, of course.

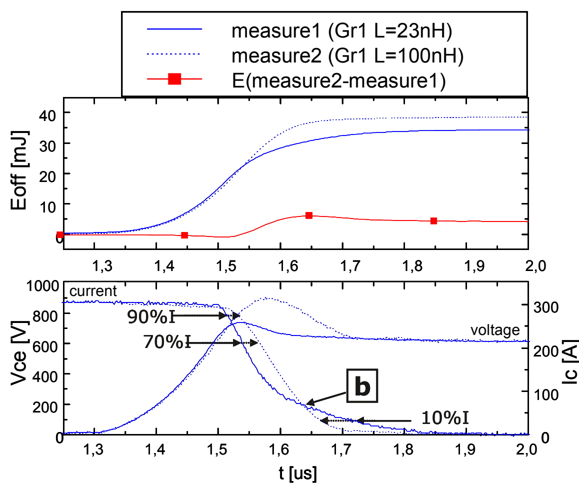

Figure 4: turn off behaviour of a low power IGBT; the diagramm on the top shows the losses as a function of the time for two inductances (solid: L=23nH, doted: L=100nH); the bottom diagramm shows the voltage and the current curves

IGBT turn-off

While dI/dt reduces the voltage at the IGBT during turn-on, it enhances the (over-)voltage at the IGBT during turn-off. This is trivially known and therefore an increase of turn-off losses with increasing DC-link inductance is expected. As can be easily derived from a left-right comparison in Figure 2, the decrease of turn-on losses with inductance is much more pronounced than the increase of turn-off losses, however.

This general trend is easily understood if one takes into account that the turn-off dI/dt of modern IGBTs is intrinsically limited by the device dynamics to a value that is at about the half of the turn-on dI/dt. Since reduction or increase of turn-on and turn-off losses, respectively are predominantly related to V = L dI/dt, a change of inductance therefore has a much more pronounced effect on turn-on than on turn-off losses.

A more detailed analysis further reveals an additional effect: Again, the switching event may be divided into two phases as sketched in Fig. 4. We use the time stamp “B” at which the current waveforms of low and high inductance set-up cross. In the first switching phase, until the crossing point “B” the increased overvoltage with the high inductance set-up results in increased losses of 36.3 mJ as compared to 30.8 mJ in the low inductance set-up (= 5.5 mJ). After Point “B” the high inductance set-up results in a shorter current tail, however, and the losses during this phase are by 1.8 mJ lower than in case of the low inductance set-up. The reason is simply, that the increased overvoltage results in a more pronounced transient plasma extraction which reduces the charge which is extracted from the device during the current tail phase.

Some further insight may be gained from a detailed study of the dI/dt during turn-off, as shown in Fig. 4. The absolute values of the so called 90%-10% dI/dt extracted from the switching times at the points of achievement of the respective shares of the switched current increase with increasing stray inductance. This effect is dominated by the reduction of the current tail, i.e. a "faster" achievement of the 10% value.

Analyzing the absolute maximum dI/dt value during turn-off yields the opposite trend (also shown in Fig. 5). This maximum dI/dt is slowed down by an increasing inductance as would simply be expected by electrical engineering basics.

In conclusion, the macroscopic 90%-10% dI/dt is enhanced by inceasing inductance while the microscopic maximum dI/dt is decreased. In total the effect on turn-off losses for the given example amounts to an increase with stray inductance by 11%. (34.2 mJ to 37.9 mJ)

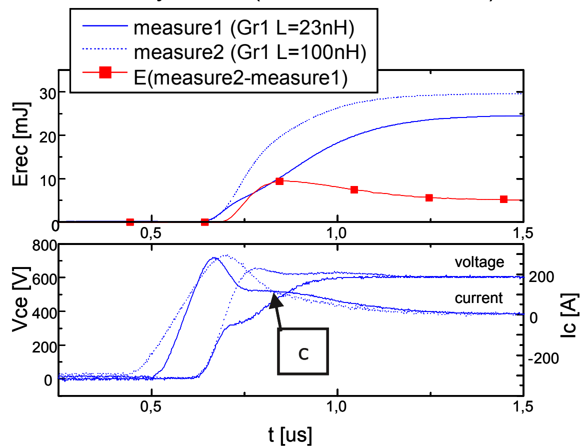

Figure 6: turn off behaviour of the diode (emitter controlled HE); the diagramm on the top shows the losses as a function of the time for two inductances (solid: L=23nH, doted: L=100nH); the bottom diagramm shows the voltage and the current curves

Diode recovery

While it has been shown that dynamic IGBT losses decrease with increased stray inductance, diode losses increase (Fig. 6). Diode turn-on is simply irrelevant for dynamic losses and therefore may not be improved. As in case of the IGBT, turn-off losses have to increase. A comparison of low- and high inductance switching is presented in Fig. 6. It becomes clear that the reduced dI/dt of the IGBT has hardly any effect on losses since the diode voltage is still about zero then. After the reverse recovery peak current the effect of the diode voltage increased by higher stray inductance dominates and induces additional losses. Again, a crossing point "C" in the diode tail currents of low and high inductance set-up can be found. Increased overvoltage results in a loss increase from 10.1 mJ to 19.6 mJ (+ 9.5 mJ) before point "C". As in case of the IGBT an increased dynamic overvoltage results in a reduction of the current tail after point "C" and the loss balance improves by 4.4 mJ in favour of the high inductance set-up then. In total the first switching phase dominates and diode losses increase with increasing inductance from 24.6 mJ to 29.7 mJ by 20%.

Softness / snap-off IGBT

The preceding paragraphs have shown that parasitic inductances may be beneficial for the overall loss balance. Unfortunately, stray inductances may also lead to oscillations, e.g. as a consequence of current snap-off, which may limit the use of a device due to EMI or robustness (overvoltage) limitations. As has been shown, tail currents which help to suppress oscillation tendencies decrease with increasing stray inductances. All measurements presented so far have been performed at a junction temperature of 150°C which is most crucial for loss considerations. Snap-off is more critical at low temperatures since the carrier injection into the device decreases with temperature and pronounces the reduction of charge available for a smooth current tail. Therefore, in Fig. 7 IGBT turn-off at rated current is compared between the three chip versions at a temperature of 25°C and a DC link voltage of 600V. As a parameter the DC link inductance is used. In the given example, the Low Power IGBT version gets snappy at a stray inductance of about 55nH and oscillations start to occur. The Medium Power version stays soft under the same conditions up to a DC link inductance of about 80 nH. In case of the High Power optimization the chip stays soft in the inductance range observed (20 nH … 100 nH). Only a slight reduction of the tail current with increased inductance is visible. This observation is not surprising at all since this IGBT is designed to be used in Power Modules with up to 3600A current rating which could be represented by switching the module considered here at a stray inductance of approximately 500 nH.

In Figure 8 a soft and not soft turn-off waveform are shown and their Fourier Transformation spectra are given in the right plot. The oscillation leads to a 20 dB enhancement of the spectrum around the oscillation frequency of roughly 10 MHz, a frequency which is quite typical for Chip-

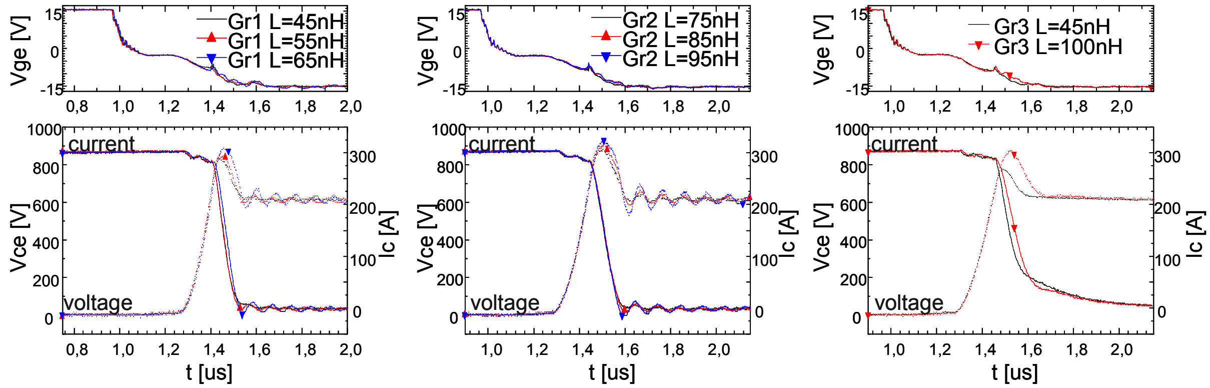

Figure 7: switching curves as function of the stray inductance L_S of three IGBTs versions (LowPower IGBT4 (left), Medium power IGBT4 (middle), High Power IGBT4 (right)); the diagrams on the top shows the gatevoltage; the diagrams on the bottom shows the current curves (dotted) and voltage curves (solid)

DC link oscillations at the given parasitic inductance. Even though such a procedure is not able to predict passing or failing of an EMI qualification it obviously demonstrates the sensitivity of EMI to snap-off phenomena.

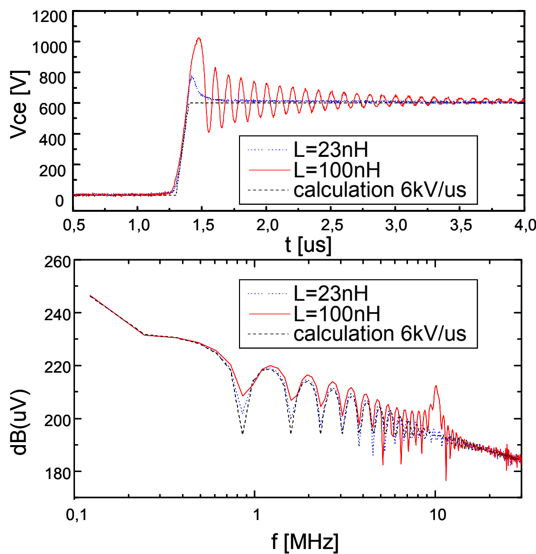

Figure 8: influence of a current snap off to the EMI; top: the voltage curves of a soft switching event with L=23nH (doted) and a snappy switching event with L=100nH (solid); bottom: FFT of the voltage curves

Softness / Snap-off Diode

While snap-off tendencies of an IGBT are usually most pronounced at low temperatures and high currents, free wheeling diode softness usually is most critical at low temperature and low current. This is due to a couple of facts: As the diode is a carrier lifetime optimized device, the plasma density is lowest at low currents and therefore the tail charge is reduced with decreasing current level. Furthermore, the switching IGBT forcing the diode to commutate usually switches faster (dV/dt) at low current levels. Finally, the diode overvoltage is not related to the switched current but results from the negative slope of the reverse recovery current peak of the diode. This also is steepest at low currents and low temperatures, usually.

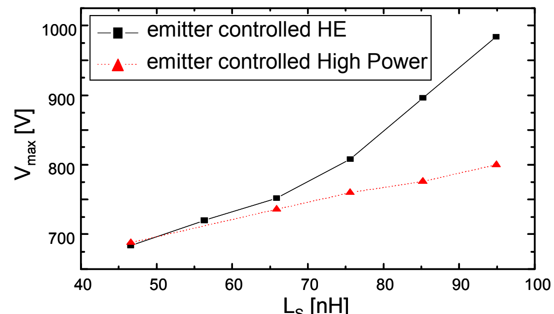

Figure 9: turn off diode – Vmax as function of Ls for two different diode versions (emitter controlled HE (solid) and emitter controlled High Power (doted)

As a consequence of fast switching transients (dV/dt and reverse recovery dI/dt) DC-link oscillations may easily be triggered at low current diode commutations even without a diode snap-off. Here, low stray inductances lead to higher resonance frequencies and may help to suppress such oscillations.

Of course, the situation gets worse if large stray inductances lead to a real snap-off of the diode. As a consequence of “intrinsic” oscillations snap-off is hard to detect. Two approaches can be used: First, a point of inflection in the voltage signal just short before reaching the maximum voltage indicates an increased dI/dt at the diode.

Secondly, when the overvoltage peak is plotted as a function of the DC link inductance as done in Figure 9 a change of the slope indicates the occurrence of snap-off. Both approaches indicate that snap-off occurs at about 70 nH. Even though this is not dangerous for the devices it may give certain limitations for the use of higher stray inductances from EMI considerations. As a consequence, Infineon has developed a second so called “high power” version Emitter Controlled Diode designated for use in larger current rating applications.

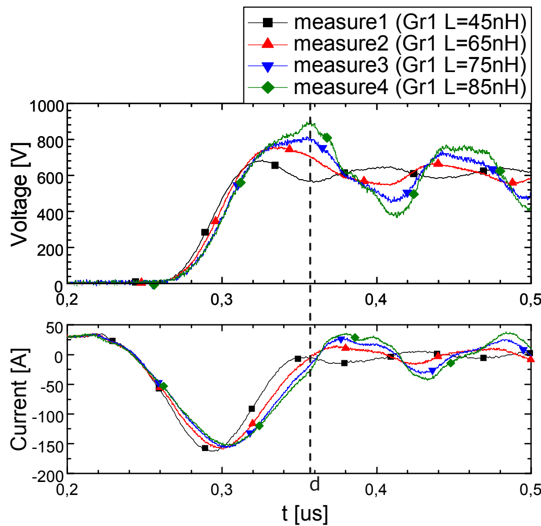

Figure 10: diode turn off at room temperature and 1/10Inominal

Summary and Discussion

IGBT optimizations designed for enhanced softness requirements pay for this feature by increased switching losses if operated under the same conditions. Increasing the DC-link stray inductance, however, results in a decrease of switching losses due to the fact that the reduction of turn-on losses is much larger than the increase of turn-off losses since turn-on dI/dt usually is much larger than turn-off dI/dt. It has been shown that under the condition of maximum stray inductance not resulting in snap-off at turn-off the switching losses of a softer optimization may be at the same level as for the chip optimization designed for lowest switching losses. Thus, generally operation of a chip close to its softness limits will yield the lowest switching losses.

Parasitic stray inductance plays an important role for DC-link resonance frequencies and diode snap-off, as well. Here, for the inductance the lower the better is a simple rule. At least diode snap-of will from EMI considerations draw a simple limit to the reduction of turn-on losses by increased stray inductance or IGBT turn-on speed.

As a simple conclusion one can state that one single IGBT optimization would do, if stray inductances could always be designed to the desired limits. Since ampere ratings in IGBT modules scale over far more than two decades, this would result in a huge challenge for high power applications which hardly can be fulfilled. Therefore, at least two chip optimizations may be expected in future as well. On the other hand, recognizing the DC link inductance as a free parameter of inverter design may create a path for further loss optimizations and also result in the conclusion that two chip versions could be sufficient. Asking for even more than three optimizations for a given IGBT generation would also be a drawback for best economic solutions.

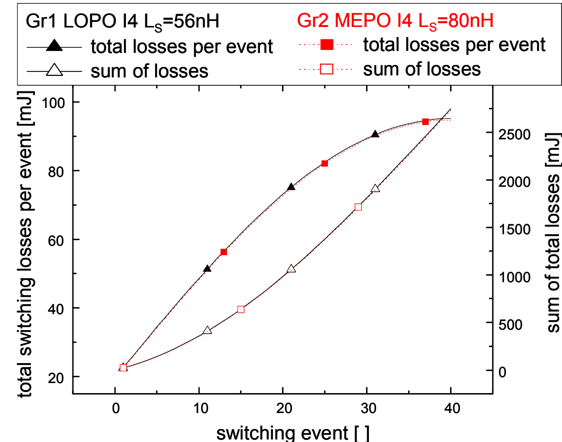

Figure 11: total switching losses (Eon + Eoff (IGBT) + Eoff(Diode)) of Low power IGBT4 and Medium power IGBT4, which works close to there snapoff boundary; assumed is a sinusoidal output current (f=50Hz, Imax=300A) and a switching frequency of 8kHz (→ 40 switching events per ¼ periode)