

16/32-Bit

Architecture

XC27x8X Derivatives

16/32-Bit Single-Chip Microcontroller
with 32-Bit Performance

XC2000 Family / Premium Line

User's Manual

V1.0 2011-01

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Table of Contents

	Table of Contents	L-1
1	Introduction	1-1
1.1	Abbreviations	1-3
1.2	Naming Conventions	1-4
2	Architectural Overview	2-1
2.1	Summary of Features	2-2
2.2	System Core Components	2-6
2.2.1	Central Processing Unit (CPU)	2-6
2.2.2	Memory Protection Unit (MPU)	2-8
2.2.3	Programmable Multiple Priority Interrupt System	2-8
2.2.4	Interfaces to System Resources	2-9
2.3	On-Chip System Resources	2-10
2.3.1	Memory Areas	2-10
2.3.2	External Bus Interface	2-11
2.4	On-Chip Peripheral Blocks	2-13
2.5	Clock Generation	2-30
2.6	Power Management	2-31
2.7	On-Chip Debug Support (OCDS)	2-32
3	Memory Organization	3-1
3.1	Address Mapping	3-3
3.2	Register Areas	3-5
3.3	Data Memory Areas	3-10
3.4	Program Memory Areas	3-12
3.4.1	Program/Data SRAM (PSRAM)	3-13
3.4.2	Non-Volatile Program Memory (Flash)	3-14
3.4.3	Using the Instruction Cache	3-14
3.5	System Stack	3-15
3.6	Protected Bits	3-16
3.7	IO Areas	3-17
3.8	External Memory Space	3-18
3.9	Reserved Memory Areas	3-18
3.10	Crossing Memory Boundaries	3-19
3.11	Embedded Flash Memory	3-20
3.11.1	Definitions	3-20
3.11.2	Operating Modes	3-22
3.11.2.1	Standard Read Mode	3-22
3.11.2.2	Command Mode	3-23
3.11.2.3	Page Mode	3-23
3.11.3	Operations	3-24

Table of Contents

3.11.3.1	Instruction Fetch from Flash Memory	3-24
3.11.3.2	Data Reads from Flash Memory	3-25
3.11.3.3	Data Writes to Flash Memory	3-25
3.11.3.4	Command Sequences	3-26
3.11.4	Details of Command Sequences	3-27
3.11.5	Sequence Errors	3-38
3.11.6	Instructions for Executing Program and Erase Jobs Concurrently ..	3-39
3.11.7	Data Integrity	3-41
3.11.7.1	Error Correcting Codes (ECC)	3-41
3.11.7.2	Aborted Program/Erase Detection	3-41
3.11.7.3	Margin Reads	3-42
3.11.7.4	Protection Overview	3-42
3.11.8	Protection Handling Details	3-45
3.11.8.1	The Lower Layer "Physical State"	3-46
3.11.8.2	The Middle Layer "Flash State"	3-47
3.11.8.3	The Upper Layer "Protection State"	3-48
3.11.8.4	Reaction on Protection Violation	3-50
3.11.8.5	Layout of the Security Pages	3-51
3.11.9	Protection Handling Examples	3-52
3.11.10	EEPROM Emulation	3-54
3.11.10.1	The Traditional EEPROM Emulation	3-54
3.11.11	Interrupt Generation	3-56
3.11.12	Recommendations for Optimized Flash Usage	3-56
3.11.12.1	Programming Code and Constant Data	3-56
3.11.12.2	EEPROM Emulation	3-57
3.12	On-Chip Program Memory Control	3-58
3.12.1	Overview	3-58
3.12.2	Register Interface	3-60
3.12.2.1	IMB Registers	3-60
3.12.2.2	System Control Registers	3-76
3.12.3	Startup, Shutdown	3-80
3.12.4	Error Reporting Summary	3-81
3.13	Data Retention Memories	3-83
3.13.1	Standby RAM Accesses	3-83
3.13.2	Standby RAM Registers	3-85
3.13.2.1	SBRAM Read Address Register	3-85
3.13.2.2	SBRAM Write Address Register	3-86
3.13.2.3	SBRAM Data Register 0	3-88
3.13.2.4	SBRAM Data Register 1	3-89
4	Memory Checker Module (MCHK)	4-1
4.1	Operational Overview	4-2
4.2	Functional Description	4-3

Table of Contents

4.2.1	Principle of the LFSR	4-5
4.2.2	Principle of the MISR	4-7
4.2.3	Commonly used Polynomials	4-8
4.2.4	Architecture of the Memory Checker Module	4-9
4.2.5	Preferable Usage of the Memory Checker Module	4-11
4.2.6	Calculation of Seed Values (Magic Word)	4-11
4.2.7	Example Application	4-13
4.3	Memory Checker Module Registers	4-15
4.3.1	General Register	4-16
4.3.2	Memory Checker Data Register	4-17
4.3.3	Memory Checker Control Register	4-19
4.4	Interfaces of the MCHK Module	4-22
5	Central Processing Unit (CPU)	5-1
5.1	Components of the CPU	5-4
5.2	Instruction Fetch and Program Flow Control	5-5
5.2.1	Branch Detection and Branch Prediction Rules	5-7
5.2.2	Zero-Cycle Jumps	5-7
5.2.3	Atomic and Extend Instructions	5-8
5.3	Instruction Processing Pipeline	5-9
5.3.1	Access to the IO Area	5-10
5.3.2	Pipeline Conflicts	5-10
5.3.2.1	Using General Purpose Registers	5-11
5.3.2.2	Using Indirect Addressing Modes	5-13
5.3.2.3	Due to Memory Bandwidth	5-14
5.3.2.4	Caused by CPU-SFR Updates	5-16
5.4	CPU Configuration Registers	5-21
5.5	Use of General Purpose Registers	5-24
5.5.1	GPR Addressing Modes	5-26
5.5.2	Context Switching	5-28
5.5.2.1	The Context Pointer (CP)	5-31
5.6	Code Addressing	5-33
5.7	Data Addressing	5-36
5.7.1	Short Addressing Modes	5-36
5.7.2	Long Addressing Modes	5-38
5.7.2.1	Data Page Pointers DPP0, DPP1, DPP2, DPP3	5-39
5.7.3	Indirect Addressing Modes	5-41
5.7.3.1	Offset Registers QR0 and QR1	5-42
5.7.4	DSP Addressing Modes	5-43
5.7.5	The System Stack	5-49
5.7.5.1	The Stack Pointer Registers SP and SPSEG	5-49
5.7.5.2	The Stack Overflow/Underflow Pointers STKOV/STKUN	5-51
5.8	Standard Data Processing	5-53

Table of Contents

5.8.1	16-bit Adder/Subtractor, Barrel Shifter, and 16-bit Logic Unit	5-57
5.8.2	Bit Manipulation Unit	5-58
5.8.3	Multiply and Divide Unit	5-60
5.9	DSP Data Processing (MAC Unit)	5-62
5.9.1	MAC Unit Control	5-63
5.9.2	Representation of Numbers and Rounding	5-63
5.9.3	The 16-bit by 16-bit Signed/Unsigned Multiplier and Scaler	5-64
5.9.4	Concatenation Unit	5-64
5.9.5	One-bit Scaler	5-64
5.9.6	The 40-bit Adder/Subtractor	5-64
5.9.7	The Data Limiter	5-65
5.9.8	The Accumulator Shifter	5-65
5.9.9	The 40-bit Signed Accumulator Register	5-66
5.9.10	The MAC Unit Status Word MSW	5-68
5.9.11	The Repeat Counter MRW	5-70
5.10	Constant Registers	5-72
6	Instruction Cache	6-1
6.1	Instruction Cache Operation	6-1
6.2	Instruction Cache Address Space	6-2
6.3	Instruction Cache Enable	6-3
6.4	Instruction Cache Invalidation	6-3
6.5	Cache Memory Data Integrity	6-4
6.5.1	Custom ICACHE ECC Setup	6-4
6.6	Cache Memory Data Access	6-5
6.7	Hit/Miss Statistics	6-6
6.8	ICACHE Registers	6-8
6.8.1	Control Register	6-8
6.8.2	Error Detection Control Register	6-9
6.8.3	Data Access Control Register	6-10
6.8.4	Read Address Register	6-12
6.8.5	Write Address Register	6-13
6.8.6	Data Registers	6-14
6.8.7	ECC Data Register	6-15
6.8.8	TAG Register	6-15
6.8.9	Hit-Miss Control Register	6-17
6.8.10	Hit Counter Register	6-18
6.8.11	Miss Counter Register	6-18
7	Interrupt and Exception Control	7-1
7.1	Interrupt System Structure	7-3
7.2	Interrupt Arbitration	7-5
7.3	Interrupt Control	7-8
7.3.1	Interrupt Control Registers	7-8

Table of Contents

7.3.2	Interrupt Priority Level and Group Level	7-9
7.3.3	General Interrupt Control Functions in Register PSW	7-9
7.3.4	Selective Interrupt Disabling	7-10
7.3.5	Interrupt Class Management	7-12
7.4	Interrupt Vector Table	7-14
7.5	Interrupt Jump Table Cache	7-16
7.6	CPU Status Saving	7-19
7.7	CPU Context Switch	7-20
7.8	Fast Bank Switching	7-21
7.9	Trap Functions	7-23
7.9.1	Software Traps	7-23
7.9.2	Hardware Traps	7-24
7.9.2.1	The Trap Flag Register TFR	7-29
7.10	Peripheral Event Controller	7-31
7.10.1	PEC Functionality	7-31
7.10.2	Source and Destination Pointers	7-32
7.10.3	Functional Control	7-35
7.10.4	End of PEC Interrupt Control	7-42
7.10.5	Channel Assignment	7-44
7.11	External Interrupts	7-46
7.11.1	External Request Unit	7-46
7.11.2	Using Peripheral Pins	7-46
7.12	OCDS Requests	7-48
7.13	Service Request Latency	7-49
7.14	Interrupt Nodes	7-51
7.14.1	Physical Interrupt Nodes	7-51
7.14.2	Interrupt Node Sharing	7-56
7.15	Interrupt Source Select Registers	7-58
7.16	Interrupt and PEC Configuration Registers	7-60
8	Memory Protection Unit (MPU)	8-1
8.1	Functional Overview	8-1
8.2	Memory Protection Registers	8-3
8.2.1	Protection Range Registers	8-3
8.2.2	Protection Mode Registers	8-5
8.2.3	Protection Range Data Register	8-8
8.2.4	Protection Range Address Register	8-8
8.3	Functional Description	8-10
8.3.1	Enabling Protection	8-10
8.3.2	Protection Levels	8-10
8.3.2.1	Protection Level 0	8-11
8.3.3	Intersecting Memory Ranges	8-11
8.3.4	Protection of the MPU registers	8-11

Table of Contents

8.3.5	Accessing SFRs and GPRs	8-12
8.3.6	Interrupts and PECs Handling	8-12
8.3.7	Special handling of RETI instruction	8-13
8.3.8	Context Switch operations	8-13
8.3.9	Debugger Access Permissions	8-14
8.3.10	Invalid Access Traps	8-14
8.3.10.1	Cancelling operations	8-15
8.4	Initializing and using the MPU	8-15
8.4.1	Installing Protection	8-15
8.4.2	Changing Protection Level	8-17
8.4.3	Executing privileged code from non-privileged one	8-17
8.4.4	Fast task switches	8-17
8.4.5	Register Bank Selection	8-17
8.4.6	Debugger Use Cases	8-17
9	System Control Unit (SCU)	9-1
9.1	Clock Generation Unit	9-3
9.1.1	Overview	9-3
9.1.2	Trimmed Current Controlled Wake-Up Clock (OSC_WU)	9-5
9.1.3	High Precision Oscillator Circuit (OSC_HP)	9-5
9.1.3.1	External Input Clock Mode	9-5
9.1.3.2	External Crystal Mode	9-5
9.1.4	Phase-Locked Loop (PLL) Module	9-7
9.1.4.1	Features	9-7
9.1.4.2	PLL Functional Description	9-7
9.1.4.3	Configuration and Operation of the PLL Modes	9-9
9.1.4.4	Power Regulator	9-14
9.1.4.5	Divider Handshake	9-15
9.1.4.6	Trimmed Current Controlled Clock	9-15
9.1.4.7	Input Clock Selection	9-15
9.1.4.8	Oscillator Watchdog	9-16
9.1.4.9	Switching PLL Parameters	9-17
9.1.5	Clock Control Unit	9-17
9.1.5.1	Clock Generation	9-17
9.1.5.2	Selecting and Changing the Operating Frequency	9-21
9.1.5.3	System Clock Emergency Handling	9-22
9.1.6	External Clock Output	9-23
9.1.6.1	Programmable Frequency Output	9-23
9.1.7	CGU Registers	9-25
9.1.7.1	Wake-up Clock Register	9-25
9.1.7.2	High Precision Oscillator Register	9-26
9.1.7.3	Trimmed Current Controlled Clock Control Register	9-29
9.1.7.4	PLL Registers	9-30

Table of Contents

9.1.7.5	System Clock Control Registers	9-40
9.1.7.6	RTC Clock Control Register	9-43
9.1.7.7	External Clock Control Register	9-43
9.2	System Timer Function (STM)	9-45
9.2.1	STM Registers	9-46
9.2.1.1	Register STMREL	9-46
9.2.1.2	Register STMCON	9-47
9.3	Wake-up Timer (WUT)	9-48
9.3.1	Wake-up Timer Operation	9-48
9.3.2	WUT Registers	9-50
9.3.2.1	Register WUTREL	9-50
9.3.2.2	Register WUCR	9-51
9.4	Reset Operation	9-54
9.4.1	Reset Architecture	9-54
9.4.1.1	Device Reset Hierarchy	9-54
9.4.1.2	Reset Types	9-54
9.4.2	General Reset Operation	9-57
9.4.2.1	Reset Counters (RSTCNTA and RSTCNTD)	9-57
9.4.2.2	De-assertion of a Reset	9-58
9.4.3	Debug Reset Assertion	9-59
9.4.4	Coupling of Reset Types	9-59
9.4.5	Reset Request Trigger Sources	9-60
9.4.5.1	Reset Sources Overview	9-61
9.4.6	Module Reset Behavior	9-62
9.4.7	Reset Controller Registers	9-64
9.4.7.1	Status Registers	9-64
9.4.7.2	Configuration Registers	9-69
9.5	External Service Request (ESR) Pins	9-74
9.5.1	General Operation	9-74
9.5.1.1	$\overline{\text{ESR}}$ as Reset Input	9-78
9.5.1.2	$\overline{\text{ESR}}$ as Reset Output	9-78
9.5.1.3	$\overline{\text{ESR}}$ as Trap Trigger	9-78
9.5.1.4	$\overline{\text{ESR}}$ as Trigger Input for the GSC	9-78
9.5.1.5	Overlay with other Product Functions	9-78
9.5.1.6	Pad Configuration for $\overline{\text{ESR}}$ Pads	9-80
9.5.2	ESR Control Registers	9-82
9.5.2.1	Configuration Registers	9-82
9.5.3	ESR Data Register	9-88
9.5.3.1	ESRDAT	9-88
9.6	Power Supply and Control	9-90
9.6.1	Supply Watchdog (SWD)	9-91
9.6.1.1	SWD Control Registers	9-94
9.6.2	Monitoring the Voltage Level of a Core Domain	9-98

Table of Contents

9.6.2.1	PVC Status and Control Registers	9-99
9.6.3	Controlling the Voltage Level of a Core Domain	9-105
9.6.3.1	Embedded Voltage Regulator	9-105
9.6.3.2	Sources for Core Supply Voltage	9-112
9.6.4	Handling the Power System	9-113
9.7	Global State Controller (GSC)	9-114
9.7.1	GSC Control Flow	9-114
9.7.1.1	Request Source Arbitration	9-114
9.7.1.2	Generation of a New Command	9-115
9.7.1.3	Usage of Commands	9-116
9.7.1.4	Terminating a Request Trigger	9-116
9.7.1.5	Suspend Control Flow	9-116
9.7.1.6	Error Feedback for a Mode Transition	9-117
9.7.2	GSC Registers	9-118
9.7.2.1	GSC Control and Status Registers	9-118
9.8	Software Boot Support	9-134
9.8.1	Start-up Registers	9-135
9.8.1.1	Start-up Status Register	9-135
9.9	External Request Unit (ERU)	9-136
9.9.1	Introduction	9-136
9.9.2	ERU Input Connections	9-138
9.9.3	External Request Select Unit (ERSx)	9-142
9.9.4	Event Trigger Logic (ETLx)	9-143
9.9.5	Connecting Matrix	9-145
9.9.6	Output Gating Unit (OGUy)	9-146
9.9.6.1	Trigger Combination	9-147
9.9.6.2	Pattern Detection	9-148
9.9.7	ERU Output Connections	9-150
9.9.8	ERU Registers	9-152
9.9.8.1	External Input Selection Register EXISEL	9-152
9.9.8.2	External Input Control Registers EXICONx	9-154
9.9.8.3	Output Control Registers EXOCONy	9-157
9.10	SCU Interrupt Generation	9-159
9.10.1	Interrupt Support	9-160
9.10.2	SCU Interrupt Sources	9-160
9.10.3	Interrupt Control Registers	9-162
9.10.3.1	Register INTSTAT	9-162
9.10.3.2	Register INTCLR	9-165
9.10.3.3	Register INTSET	9-167
9.10.3.4	Register INTDIS	9-169
9.10.3.5	Registers INTNP0 and INPNP1	9-171
9.10.3.6	Register DMPMIT	9-176
9.10.3.7	Register DMPMITCLR	9-179

Table of Contents

9.11	Temperature Compensation Unit	9-181
9.11.1	Temperature Compensation Registers	9-183
9.11.1.1	TCCR	9-183
9.12	Watchdog Timer (WDT)	9-185
9.12.1	Introduction	9-185
9.12.2	Overview	9-185
9.12.3	Functional Description	9-186
9.12.3.1	Timer Operation	9-186
9.12.3.2	Timer Modes	9-186
9.12.3.3	Suspend Mode Support	9-189
9.12.4	WDT Kernel Registers	9-191
9.12.4.1	WDT Reload Register	9-191
9.12.4.2	WDT Control and Status Register	9-192
9.12.4.3	WDT Timer Register	9-194
9.13	SCU Trap Generation	9-195
9.13.1	Trap Support	9-195
9.13.2	SCU Trap Sources	9-196
9.13.3	SCU Trap Control Registers	9-197
9.13.3.1	Register TRAPSTAT	9-197
9.13.3.2	Register TRAPCLR	9-200
9.13.3.3	Register TRAPSET	9-202
9.13.3.4	Register TRAPDIS	9-204
9.13.3.5	Register TRAPNP and TRAPNP1	9-206
9.14	Memory Content Protection for RAM Areas	9-209
9.14.1	Protection Mode Selection	9-210
9.14.2	Parity Error Handling	9-212
9.14.2.1	Parity Software Testing Support	9-213
9.14.2.2	Parity Error Registers	9-214
9.14.3	ECC Error Handling	9-221
9.14.3.1	ECC Software Testing Support	9-222
9.14.3.2	ECC Registers	9-223
9.15	Register Control	9-227
9.15.1	Register Access Control	9-227
9.15.1.1	Controlling the Security Level	9-229
9.15.2	Register Protection Registers	9-231
9.16	Miscellaneous System Registers	9-233
9.16.1	System Registers	9-233
9.16.1.1	System Control Register	9-233
9.16.2	Identification Block	9-234
9.16.2.1	Identification Registers	9-235
9.16.3	Marker Memory	9-240
9.16.3.1	Marker Memory Registers	9-240
9.17	SCU Register Addresses	9-241

Table of Contents

10	Parallel Ports	10-1
10.1	General Description	10-2
10.1.1	Basic Port Operation	10-2
10.1.2	Input Stage Control	10-6
10.1.3	Output Driver Control	10-6
10.1.3.1	Active Mode Behavior	10-6
10.1.3.2	Power Saving Mode Behavior	10-6
10.1.3.3	Reset Behavior	10-6
10.1.3.4	Power-fail Behavior	10-7
10.2	Port Register Description	10-7
10.2.1	Pad Driver Control	10-7
10.2.2	Port Output Register	10-10
10.2.3	Port Output Modification Register	10-11
10.2.4	Port Input Register	10-13
10.2.5	Port Input/Output Control Registers	10-14
10.2.6	Port Digital Input and Output Disable Register	10-17
10.3	Port Description	10-18
10.3.1	Port 0	10-19
10.3.2	Port 1	10-20
10.3.3	Port 2	10-21
10.3.4	Port 3	10-23
10.3.5	Port 4	10-24
10.3.6	Port 5	10-25
10.3.7	Port 6	10-26
10.3.8	Port 7	10-28
10.3.9	Port 8	10-29
10.3.10	Port 9	10-30
10.3.11	Port 10	10-31
10.3.12	Port 11	10-33
10.3.13	Port 15	10-34
10.4	Pin Description	10-35
11	Dedicated Pins	11-1
12	External Bus Controller (EBC)	12-1
12.1	Summary of Features	12-1
12.2	Overview	12-1
12.3	Naming Conventions	12-2
12.4	Timing Description	12-2
12.4.1	Bus Phases	12-3
12.4.2	Demultiplexed Bus	12-5
12.4.3	Multiplexed Bus	12-6
12.4.4	Fastest Access Cycles	12-7
12.5	Address Windows	12-9

Table of Contents

12.5.1	Window Allocation	12-9
12.5.2	Window Overlap	12-10
12.6	Ready Controlled Bus Access	12-11
12.6.1	Enabling the Ready Control	12-11
12.6.2	Synchronous and Asynchronous READY	12-11
12.6.3	Combining the READY function with predefined wait states	12-12
12.7	EBC Idle State	12-13
12.8	Register Description	12-14
12.8.1	EBC Mode Registers	12-14
12.8.2	Timing Control Registers	12-16
12.8.3	Function Control Registers	12-18
12.8.4	Address Window Selection Registers	12-19
12.9	EBC Implementation	12-20
12.9.1	Pin allocation for the EBC	12-20
12.9.2	Unused Registers	12-21
12.9.3	Access Control to LXBUS Modules	12-21
12.9.4	Shutdown Control	12-21
12.9.5	Dedicated Registers	12-21
12.9.5.1	Registers dedicated to LXBUS modules	12-21
13	On-Chip Debug Support (OCDS)	13-1
13.1	Debug Interface	13-2
13.1.1	Routing of Debug Signals	13-3
13.1.1.1	Register DBGPRR	13-3
13.2	OCDS Module	13-5
13.2.1	Debug Events	13-6
13.2.2	Debug Actions	13-7
13.3	Cerberus	13-8
13.3.1	Functional Overview	13-9
13.4	Emulation Device	13-10
13.5	Boundary-Scan	13-10
14	Startup Configuration and Bootstrap Loading	14-1
14.1	Startup Mode Selection	14-1
14.2	Device Status after Startup	14-2
14.2.1	Registers modified by the Startup Procedure	14-2
14.2.2	System Frequency after Startup	14-4
14.2.3	Watchdog Timer handling	14-4
14.2.3.1	Triggering Power-on Reset by WDT	14-5
14.2.4	Startup Error state	14-5
14.3	Supported Startup Modes and Options	14-5
14.3.1	Basic Startup Modes	14-6
14.3.2	Startup Modes with Debug Support	14-7
14.3.3	Special Startup Features	14-10

Table of Contents

14.3.3.1	Supplementary Startup Information from/to the User	14-10
14.3.3.2	Support for running at system frequency above 80MHz	14-12
14.3.3.3	Preparing to activate Memory Content Protection	14-12
14.4	Internal Start	14-15
14.5	External Start	14-15
14.5.1	Specific Settings	14-17
14.6	Bootstrap Loading	14-18
14.6.1	General Functionality	14-18
14.6.2	Bootstrap Loaders using UART Protocol	14-20
14.6.2.1	Standard UART Bootstrap Loader	14-20
14.6.2.2	Enhanced UART Bootstrap Loader	14-23
14.6.2.3	Choosing the Baudrate for the BSL	14-25
14.6.3	Synchronous Serial Channel Bootstrap Loader	14-27
14.6.3.1	Supported EEPROM Types	14-28
14.6.3.2	Specific Settings	14-29
14.6.4	CAN Bootstrap Loader	14-30
14.6.4.1	Specific Settings	14-32
14.6.5	Summary of Bootstrap Loader Modes	14-33
15	Instruction Set Summary	15-1
16	General Purpose Timer Units (GPT12)	16-1
16.1	Timer Block GPT1	16-3
16.1.1	GPT1 Core Timer T3 Control	16-5
16.1.2	GPT1 Core Timer T3 Operating Modes	16-7
16.1.3	GPT1 Auxiliary Timers T2/T4 Control	16-14
16.1.4	GPT1 Auxiliary Timers T2/T4 Operating Modes	16-15
16.1.5	GPT1 Clock Signal Control	16-24
16.1.6	Interrupt Control for GPT1 Timers	16-27
16.1.7	GPT1 Registers	16-28
16.1.7.1	GPT1 Timer Registers	16-28
16.1.7.2	GPT1 Timer Control Registers	16-30
16.1.7.3	GPT1 Timer Interrupt Control Registers	16-40
16.2	Timer Block GPT2	16-41
16.2.1	GPT2 Core Timer T6 Control	16-43
16.2.2	GPT2 Core Timer T6 Operating Modes	16-45
16.2.3	GPT2 Auxiliary Timer T5 Control	16-48
16.2.4	GPT2 Auxiliary Timer T5 Operating Modes	16-49
16.2.5	GPT2 Register CAPREL Operating Modes	16-53
16.2.6	GPT2 Clock Signal Control	16-59
16.2.7	Interrupt Control for GPT2 Timers and CAPREL	16-62
16.2.8	GPT2 Registers	16-63
16.2.8.1	GPT2 Timer Registers	16-63
16.2.8.2	GPT2 Timer Control Registers	16-65

Table of Contents

16.2.8.3	GPT2 Timer and CAPREL Interrupt Control Registers	16-71
16.3	Miscellaneous GPT12 Registers	16-72
16.4	Register Table	16-78
16.5	Implementation of the GPT12 Module	16-79
16.5.1	Module Connections	16-80
17	Analog to Digital Converter	17-1
17.1	Introduction and Basic Structure	17-4
17.2	Electrical Models	17-8
17.3	Transfer Characteristics and Error Definitions	17-11
17.4	Configuration of General Functions	17-12
17.4.1	Mode Control	17-12
17.4.2	Module Identification	17-15
17.4.3	General Clocking Scheme and Control	17-16
17.4.4	Module Activation and Power Saving Modes	17-22
17.5	Conversion Request Generation	17-24
17.5.1	Channel Scan Request Source Handling	17-26
17.5.2	Queued Request Source Handling	17-33
17.5.3	Hardware Trigger Selection	17-45
17.6	Request Source Arbitration	17-47
17.6.1	Arbiter Timing	17-48
17.6.2	Request Source Priority and Conversion Start Mode	17-50
17.7	Analog Input Channel Configuration	17-53
17.7.1	Channel Parameters	17-54
17.7.2	Limit Checking	17-57
17.7.3	Alias Feature	17-60
17.7.4	Conversion Timing	17-62
17.7.5	Channel Events and Interrupts	17-63
17.8	Conversion Result Handling	17-64
17.8.1	Storage of Conversion Results	17-64
17.8.2	Wait-for-Read Mode	17-72
17.8.3	Result FIFO Buffer	17-73
17.8.4	Result Events and Interrupts	17-75
17.8.5	Data Reduction and Filtering	17-76
17.9	Synchronization of Conversions	17-90
17.9.1	Synchronized Conversions for Parallel Sampling	17-90
17.9.2	Equidistant Sampling	17-94
17.10	Safety Features	17-96
17.10.1	Broken Wire Detection	17-96
17.10.2	Multiplexer Test Mode	17-100
17.11	External Multiplexer Control	17-101
17.12	Interrupt Request Handling	17-106
17.13	Implementation	17-117

Table of Contents

17.13.1	Address Map	17-117
17.13.2	Interrupt Control Registers	17-120
17.13.3	Analog Connections	17-121
17.13.4	Digital Connections	17-124
18	Real Time Clock	18-1
18.1	Defining the RTC Time Base	18-2
18.2	RTC Run Control	18-4
18.3	RTC Operating Modes	18-7
18.4	48-bit Timer Operation	18-11
18.5	System Clock Operation	18-11
18.6	Cyclic Interrupt Generation	18-12
18.7	RTC Interrupt Generation	18-13
18.8	Miscellaneous Registers	18-16
19	Capture/Compare Unit	19-1
19.1	Functional Overview	19-2
19.1.1	The CAPCOM Timers	19-3
19.1.2	Timer Interrupt	19-7
19.1.3	Capture/Compare Channels	19-8
19.1.4	Capture Mode	19-9
19.1.5	Compare Modes	19-10
19.1.5.1	Compare Mode 0	19-11
19.1.5.2	Compare Mode 1	19-11
19.1.5.3	Compare Mode 2	19-14
19.1.5.4	Compare Mode 3	19-14
19.1.6	Double-Register Compare Mode	19-18
19.1.7	CAPCOM Interrupts	19-21
19.1.8	Compare Output Signal Generation	19-21
19.1.9	Single Event Mode	19-22
19.1.10	Staggered and Non-Staggered Operation	19-22
19.1.11	External Input Signal Requirements	19-27
19.2	CAPCOM2 Registers	19-28
19.2.1	Identification Register	19-31
19.2.2	Timer 7/8 Registers	19-32
19.2.3	Timer 7/8 Control Register	19-34
19.2.4	Capture/Compare Registers	19-36
19.2.5	Capture/Compare Mode Registers	19-37
19.2.6	Compare Output Register	19-39
19.2.7	Double-Register Compare Mode Register	19-40
19.2.8	IOC Register	19-41
19.2.9	Single Event Mode Register	19-42
19.2.10	KSCCFG Register	19-43
19.3	Module Implementation	19-46

Table of Contents

19.3.1	Interfaces of the CAPCOM2 Unit	19-47
20	Capture/Compare Unit 6 (CCU6)	20-1
20.1	Introduction	20-1
20.1.1	Feature Set Overview	20-2
20.1.2	Block Diagram	20-3
20.1.3	Register Overview	20-4
20.2	Operating Timer T12	20-7
20.2.1	T12 Overview	20-8
20.2.2	T12 Counting Scheme	20-10
20.2.2.1	Clock Selection	20-10
20.2.2.2	Edge-Aligned / Center-Aligned Mode	20-11
20.2.2.3	Single-Shot Mode	20-13
20.2.3	T12 Compare Mode	20-14
20.2.3.1	Compare Channels	20-14
20.2.3.2	Channel State Bits	20-15
20.2.3.3	Hysteresis-Like Control Mode	20-20
20.2.4	Compare Mode Output Path	20-21
20.2.4.1	Dead-Time Generation	20-21
20.2.4.2	State Selection	20-23
20.2.4.3	Output Modulation and Level Selection	20-24
20.2.5	T12 Capture Modes	20-26
20.2.6	T12 Shadow Register Transfer	20-30
20.2.7	Timer T12 Operating Mode Selection	20-31
20.2.8	T12 related Registers	20-32
20.2.8.1	T12 Counter Register	20-32
20.2.8.2	Period Register	20-32
20.2.8.3	Capture/Compare Registers	20-33
20.2.8.4	Capture/Compare Shadow Registers	20-34
20.2.8.5	Dead-time Control Register	20-35
20.2.9	Capture/Compare Control Registers	20-37
20.2.9.1	Channel State Bits	20-37
20.2.9.2	T12 Mode Control Register	20-40
20.2.9.3	Timer Control Registers	20-41
20.3	Operating Timer T13	20-49
20.3.1	T13 Overview	20-49
20.3.2	T13 Counting Scheme	20-52
20.3.2.1	Clock Selection	20-52
20.3.2.2	T13 Counting	20-53
20.3.2.3	Single-Shot Mode	20-54
20.3.2.4	Synchronization to T12	20-55
20.3.3	T13 Compare Mode	20-57
20.3.4	Compare Mode Output Path	20-59

Table of Contents

20.3.5	T13 Shadow Register Transfer	20-60
20.3.6	T13 related Registers	20-62
20.3.6.1	T13 Counter Register	20-62
20.3.6.2	Period Register	20-63
20.3.6.3	Compare Register	20-64
20.3.6.4	Compare Shadow Register	20-64
20.4	Trap Handling	20-65
20.5	Multi-Channel Mode	20-67
20.6	Hall Sensor Mode	20-70
20.6.1	Hall Pattern Evaluation	20-71
20.6.2	Hall Pattern Compare Logic	20-73
20.6.3	Hall Mode Flags	20-74
20.6.4	Hall Mode for Brushless DC-Motor Control	20-76
20.7	Modulation Control Registers	20-78
20.7.1	Modulation Control	20-78
20.7.2	Trap Control Register	20-80
20.7.3	Passive State Level Register	20-83
20.7.4	Multi-Channel Mode Registers	20-84
20.8	Interrupt Handling	20-89
20.8.1	Interrupt Structure	20-89
20.8.2	Interrupt Registers	20-91
20.8.2.1	Interrupt Status Register	20-91
20.8.2.2	Interrupt Status Set Register	20-94
20.8.2.3	Status Reset Register	20-96
20.8.2.4	Interrupt Enable Register	20-98
20.8.2.5	Interrupt Node Pointer Register	20-101
20.9	General Module Operation	20-103
20.9.1	Mode Control	20-103
20.9.2	Input Selection	20-106
20.9.3	General Registers	20-107
20.9.3.1	ID Register	20-107
20.9.3.2	Port Input Select Registers	20-107
20.9.3.3	Kernel State Configuration Register	20-112
20.9.3.4	Kernel State Sensitivity Control Register	20-114
20.10	Implementation	20-115
20.10.1	Address Map	20-115
20.10.2	Interrupt Control Registers	20-116
20.10.3	Synchronous Start Feature	20-117
20.10.4	Digital Connections	20-118
20.10.4.1	Connections of CCU60	20-118
20.10.4.2	Connections of CCU61	20-122
20.10.4.3	Connections of CCU62	20-125
20.10.4.4	Connections of CCU63	20-128

Table of Contents

21	Universal Serial Interface Channel	21-1
21.1	Introduction	21-1
21.1.1	Feature Set Overview	21-2
21.1.2	Channel Structure	21-5
21.1.3	Input Stages	21-6
21.1.4	Output Signals	21-7
21.1.5	Baud Rate Generator	21-8
21.1.6	Channel Events and Interrupts	21-9
21.1.7	Data Shifting and Handling	21-9
21.1.7.1	Basic Data Buffer Structure	21-10
21.1.7.2	FIFO Buffer Structure	21-11
21.2	Operating the USIC	21-13
21.2.1	Register Overview	21-13
21.2.2	Operating the USIC Communication Channel	21-18
21.2.2.1	Protocol Control and Status	21-18
21.2.2.2	Mode Control	21-19
21.2.2.3	General Channel Events and Interrupts	21-20
21.2.2.4	Data Transfer Events and Interrupts	21-21
21.2.2.5	Protocol-specific Events and Interrupts	21-24
21.2.3	Channel Control and Configuration Registers	21-25
21.2.3.1	Channel Control Register	21-25
21.2.3.2	Channel Configuration Register	21-28
21.2.3.3	Kernel State Configuration Register	21-29
21.2.3.4	Interrupt Node Pointer Registers	21-31
21.2.4	Protocol Related Registers	21-33
21.2.4.1	Protocol Control Registers	21-33
21.2.4.2	Protocol Status Register	21-34
21.2.4.3	Protocol Status Clear Register	21-35
21.2.5	Operating the Input Stages	21-36
21.2.5.1	General Input Structure	21-36
21.2.5.2	Digital Filter	21-37
21.2.5.3	Edge Detection	21-37
21.2.5.4	Selected Input Monitoring	21-37
21.2.5.5	Loop Back Mode	21-37
21.2.6	Input Stage Register	21-38
21.2.6.1	Input Control Registers	21-38
21.2.7	Operating the Baud Rate Generator	21-41
21.2.7.1	Fractional Divider	21-41
21.2.7.2	External Frequency Input	21-41
21.2.7.3	Protocol-Related Counter in Divider Mode	21-42
21.2.7.4	Protocol-Related Counter in Capture Mode	21-43
21.2.7.5	Time Quanta Counter	21-44
21.2.7.6	Shift Clock Output Configuration	21-44

Table of Contents

21.2.8	Baud Rate Generator Registers	21-46
21.2.8.1	Fractional Divider Registers	21-46
21.2.8.2	Baud Rate Generator Registers	21-48
21.2.9	Operating the Transmit Data Path	21-51
21.2.9.1	Transmit Buffering	21-51
21.2.9.2	Transmit Control Information	21-52
21.2.9.3	Transmit Data Validation	21-53
21.2.10	Operating the Receive Data Path	21-55
21.2.10.1	Receive Buffering	21-55
21.2.10.2	Baud Rate Constraints	21-56
21.2.11	Transfer Control and Status Registers	21-57
21.2.11.1	Shift Control Registers	21-57
21.2.11.2	Transmission Control and Status Registers	21-60
21.2.11.3	Flag Modification Registers	21-67
21.2.12	Data Buffer Registers	21-69
21.2.12.1	Transmit Buffer Locations	21-69
21.2.12.2	Receive Buffer Registers RBUF0, RBUF1	21-70
21.2.12.3	Receive Buffer Registers RBUF, RBUFD, RBUFSR	21-76
21.2.13	Operating the FIFO Data Buffer	21-79
21.2.13.1	FIFO Buffer Partitioning	21-80
21.2.13.2	Data Buffer Events and Interrupts	21-81
21.2.13.3	FIFO Buffer Bypass	21-86
21.2.13.4	FIFO Access Constraints	21-87
21.2.13.5	Handling of FIFO Transmit Control Information	21-88
21.2.14	FIFO Buffer and Bypass Registers	21-89
21.2.14.1	Bypass Registers	21-89
21.2.14.2	General FIFO Buffer Control Registers	21-92
21.2.14.3	Transmit FIFO Buffer Control Registers	21-98
21.2.14.4	Receive FIFO Buffer Control Registers	21-101
21.2.14.5	FIFO Buffer Data Registers	21-105
21.2.14.6	FIFO Buffer Pointer Registers	21-108
21.3	Asynchronous Serial Channel (ASC = UART)	21-110
21.3.1	Signal Description	21-110
21.3.2	Frame Format	21-111
21.3.2.1	Idle Time	21-112
21.3.2.2	Start Bit Detection	21-113
21.3.2.3	Data Field	21-113
21.3.2.4	Parity Bit	21-113
21.3.2.5	Stop Bit(s)	21-113
21.3.3	Operating the ASC	21-114
21.3.3.1	Bit Timing	21-115
21.3.3.2	Baud Rate Generation	21-116
21.3.3.3	Noise Detection	21-116

Table of Contents

21.3.3.4	Collision Detection	21-116
21.3.3.5	Pulse Shaping	21-117
21.3.3.6	Automatic Shadow Mechanism	21-118
21.3.3.7	End of Frame Control	21-118
21.3.3.8	Mode Control Behavior	21-119
21.3.3.9	Disabling ASC Mode	21-119
21.3.3.10	Protocol Interrupt Events	21-119
21.3.3.11	Data Transfer Interrupt Handling	21-120
21.3.3.12	Protocol-Related Argument and Error	21-121
21.3.3.13	Receive Buffer Handling	21-121
21.3.3.14	Sync-Break Detection	21-121
21.3.3.15	Transfer Status Indication	21-121
21.3.4	ASC Protocol Registers	21-123
21.3.4.1	ASC Protocol Control Registers	21-123
21.3.4.2	ASC Protocol Status Register	21-127
21.3.5	Hardware LIN Support	21-129
21.4	Synchronous Serial Channel (SSC)	21-131
21.4.1	Signal Description	21-131
21.4.1.1	Transmit and Receive Data Signals	21-133
21.4.1.2	Shift Clock Signals	21-134
21.4.1.3	Slave Select Signals	21-137
21.4.2	Operating the SSC	21-139
21.4.2.1	Automatic Shadow Mechanism	21-139
21.4.2.2	Mode Control Behavior	21-139
21.4.2.3	Disabling SSC Mode	21-140
21.4.2.4	Data Frame Control	21-140
21.4.2.5	Parity Mode	21-140
21.4.2.6	Transfer Mode	21-140
21.4.2.7	Data Transfer Interrupt Handling	21-141
21.4.2.8	Protocol-Related Argument and Error	21-141
21.4.2.9	Receive Buffer Handling	21-141
21.4.3	Operating the SSC in Master Mode	21-143
21.4.3.1	Baud Rate Generation	21-143
21.4.3.2	MSLS Generation	21-144
21.4.3.3	Automatic Slave Select Update	21-145
21.4.3.4	Slave Select Delay Generation	21-146
21.4.3.5	Protocol Interrupt Events	21-147
21.4.3.6	End-of-Frame Control	21-148
21.4.4	Operating the SSC in Slave Mode	21-150
21.4.4.1	Protocol Interrupts	21-150
21.4.4.2	End-of-Frame Control	21-151
21.4.5	SSC Protocol Registers	21-152
21.4.5.1	SSC Protocol Control Registers	21-152

Table of Contents

21.4.5.2	SSC Protocol Status Register	21-156
21.4.6	SSC Timing Considerations	21-158
21.4.6.1	Closed-loop Delay	21-158
21.4.6.2	Delay Compensation in Master Mode	21-159
21.5	Inter-IC Bus Protocol (IIC)	21-161
21.5.1	Introduction	21-161
21.5.1.1	Signal Description	21-162
21.5.1.2	Symbols	21-163
21.5.1.3	Frame Format	21-164
21.5.2	Operating the IIC	21-165
21.5.2.1	Transmission Chain	21-166
21.5.2.2	Byte Stretching	21-166
21.5.2.3	Baud Rate Update	21-166
21.5.2.4	Master Arbitration	21-166
21.5.2.5	Release of TBUF	21-167
21.5.2.6	Mode Control Behavior	21-167
21.5.2.7	IIC Protocol Interrupt Events	21-168
21.5.2.8	Receiver Address Acknowledge	21-169
21.5.2.9	Receiver Handling	21-169
21.5.2.10	Receiver Status Information	21-170
21.5.3	Symbol Timing	21-171
21.5.3.1	Start Symbol	21-172
21.5.3.2	Repeated Start Symbol	21-172
21.5.3.3	Stop Symbol	21-173
21.5.3.4	Data Bit Symbol	21-173
21.5.4	Data Flow Handling	21-174
21.5.4.1	Transmit Data Formats	21-174
21.5.4.2	Valid Master Transmit Data Formats	21-176
21.5.5	IIC Protocol Registers	21-179
21.5.5.1	IIC Protocol Control Registers	21-179
21.5.5.2	IIC Protocol Status Register	21-182
21.6	IIS Protocol	21-185
21.6.1	Introduction	21-185
21.6.1.1	Signal Description	21-185
21.6.1.2	Protocol Overview	21-187
21.6.1.3	Transfer Delay	21-187
21.6.1.4	Connection of External Audio Components	21-188
21.6.2	Operating the IIS	21-189
21.6.2.1	Frame Length and Word Length Configuration	21-189
21.6.2.2	Automatic Shadow Mechanism	21-189
21.6.2.3	Mode Control Behavior	21-189
21.6.2.4	Transfer Delay	21-190
21.6.2.5	Parity Mode	21-191

Table of Contents

21.6.2.6	Transfer Mode	21-191
21.6.2.7	Data Transfer Interrupt Handling	21-192
21.6.2.8	Protocol-Related Argument and Error	21-192
21.6.2.9	Transmit Data Handling	21-192
21.6.2.10	Receive Buffer Handling	21-193
21.6.2.11	Loop-Delay Compensation	21-193
21.6.3	Operating the IIS in Master Mode	21-194
21.6.3.1	Baud Rate Generation	21-194
21.6.3.2	WA Generation	21-195
21.6.3.3	Master Clock Output	21-196
21.6.3.4	Protocol Interrupt Events	21-197
21.6.4	Operating the IIS in Slave Mode	21-198
21.6.4.1	Protocol Events and Interrupts	21-198
21.6.5	IIS Protocol Registers	21-199
21.6.5.1	IIS Protocol Control Registers	21-199
21.6.5.2	IIS Protocol Status Register	21-202
21.7	USIC Implementation in XC27x8X	21-205
21.7.1	Implementation Overview	21-205
21.7.2	Channel Features	21-206
21.7.3	Address Map	21-207
21.7.4	Module Identification Registers	21-208
21.7.5	Interrupt Control Registers	21-210
21.7.6	Input/Output Connections	21-212
21.7.6.1	USIC Module 0 I/O Lines	21-213
21.7.6.2	USIC Module 1 I/O Lines	21-216
21.7.6.3	USIC Module 2 I/O Lines	21-219
21.7.6.4	USIC Module 3 I/O Lines	21-222
21.7.6.5	USIC Module 4 I/O Lines	21-224
22	Controller Area Network (MultiCAN) Controller	22-1
22.1	MultiCAN Short Description	22-1
22.1.1	Overview	22-1
22.1.2	MultiCAN Features	22-2
22.2	CAN Functional Description	22-4
22.2.1	Conventions and Definitions	22-4
22.2.2	Introduction	22-4
22.2.2.1	Feature Overview	22-4
22.2.2.2	Module Structure	22-7
22.2.3	CAN Node Control	22-10
22.2.3.1	Bit Timing	22-10
22.2.3.2	CAN Error Handling	22-12
22.2.3.3	CAN Frame Counter	22-12
22.2.3.4	CAN Node Interrupts	22-13

Table of Contents

22.2.4	Message Object List Structure	22-14
22.2.4.1	Basics	22-14
22.2.4.2	List of Unallocated Elements	22-15
22.2.4.3	Connection to the CAN Nodes	22-15
22.2.4.4	List Command Panel	22-17
22.2.5	CAN Node Analysis Features	22-19
22.2.5.1	Analyze Mode	22-19
22.2.5.2	Loop-back Mode	22-19
22.2.5.3	Bit Timing Analysis	22-21
22.2.6	Message Acceptance Filtering	22-22
22.2.6.1	Receive Acceptance Filtering	22-22
22.2.6.2	Transmit Acceptance Filtering	22-23
22.2.7	Message Postprocessing Interface	22-25
22.2.7.1	Message Interrupts	22-25
22.2.7.2	Message Pendings	22-26
22.2.8	Message Object Data Handling	22-29
22.2.8.1	Frame Reception	22-29
22.2.8.2	Frame Transmission	22-31
22.2.9	Message Object Functionality	22-36
22.2.9.1	Standard Message Object Mode	22-36
22.2.9.2	Single Data Transfer Mode	22-36
22.2.9.3	Single Transmit Trial	22-36
22.2.9.4	Message Object FIFO Structure	22-37
22.2.9.5	Receive FIFO	22-40
22.2.9.6	Transmit FIFO	22-41
22.2.9.7	Gateway Mode	22-42
22.2.9.8	Foreign Remote Requests	22-44
22.2.10	MultiCAN Kernel Registers	22-45
22.2.10.1	Register Address Map	22-45
22.2.10.2	Module Identification Register	22-50
22.2.10.3	Command Panel	22-51
22.2.10.4	Module Setup	22-56
22.2.10.5	Interrupt Trigger Register ITR	22-57
22.2.10.6	List Pointer	22-58
22.2.10.7	Message Notifications	22-60
22.2.11	CAN Node Specific Registers	22-62
22.2.12	Message Object Registers	22-78
22.3	General Control and Status	22-100
22.3.1	Clock Control	22-100
22.3.2	Port Input Control	22-101
22.3.3	Suspend Mode	22-102
22.3.4	Interrupt Structure	22-103
22.4	MultiCAN Module Implementation	22-104

Table of Contents

22.4.1	Interfaces of the CAN Module	22-104
22.4.2	Module Clock Generation	22-105
22.4.2.1	Fractional Divider Overview	22-106
22.4.3	Mode Control	22-114
22.4.4	Connection of External Signals	22-117
22.4.5	MultiCAN Module Register Address Map	22-121
22.4.6	Module Base Address Table	22-123
Keyword Index		L-1
Register Index		L-8

1 Introduction

The rapidly growing area of embedded control applications is representing one of the most time-critical operating environments for today's microcontrollers. Complex control algorithms have to be processed based on a large number of digital as well as analog input signals, and the appropriate output signals must be generated within a defined maximum response time. Embedded control applications also are often sensitive to board space, power consumption, and overall system cost.

Embedded control applications therefore require microcontrollers, which:

- offer a high level of system integration
- eliminate the need for additional peripheral devices and the associated software overhead
- provide system security and fail-safe mechanisms
- provide effective means to control (and reduce) the device's power consumption

Addressing these goals Infineon developed the XC2000 Family of 16/32-bit CMOS microcontrollers.

Information about specific versions and derivatives will be made available with the devices themselves. Contact your Infineon representative for up-to-date material or refer to <http://www.infineon.com/microcontrollers>.

About this Manual

This manual describes the functionality of a number of microcontroller types of the Infineon XC27x8X Derivatives - the **XC27x8X** derivatives. These microcontrollers provide identical functionality to a large extent, but each device type has specific unique features. The descriptions in this manual cover a superset of the provided features.

For simplicity, the various device types are referred to by the collective term **XC27x8X** throughout this manual. The complete Pro Electron conforming designations are listed in the respective Data Sheets.

For the features of a particular derivative please refer to the device datasheet.

Complete Development Support

For the development tool support of its microcontrollers, Infineon follows a clear third party concept. Currently around 120 tool suppliers world-wide, ranging from local niche manufacturers to multinational companies with broad product portfolios, offer powerful development tools for the Infineon C500, C800, XC800, C166, XC166, XC2000, XE166, and TriCore microcontroller families, providing a remarkable variety of price-performance classes as well as early availability of high quality key tools such as compilers, assemblers, simulators, debuggers or in-circuit emulators.

Infineon incorporates its strategic tool partners very early into the product development process, making sure embedded system developers get reliable, well-tuned tool

Introduction

solutions, which help them unleash the power of Infineon microcontrollers in the most effective way and with the shortest possible learning curve.

The tool environment for the Infineon 16/32-bit microcontrollers includes the following tools:

- Compilers (C/C++)
- Macro-assemblers, linkers, locators, library managers, format-converters
- Architectural simulators
- HLL debuggers
- Real-time operating systems
- VHDL chip models
- In-circuit emulators (based on bondout or standard chips)
- Plug-in emulators
- Emulation and clip-over adapters, production sockets
- Logic analyzer disassemblers
- Starter kits
- Evaluation boards with monitor programs
- Industrial boards
- Low level driver software
- Chip code generation tool (DAVE™)

1.1 Abbreviations

The following acronyms and terms are used within this document:

ADC	Analog Digital Converter
ALE	Address Latch Enable
ALU	Arithmetic and Logic Unit
ASC	Asynchronous/synchronous Serial Channel
CAN	Controller Area Network (License Bosch)
CAPCOM	CAPture and COMpare unit
CISC	Complex Instruction Set Computing
CMOS	Complementary Metal Oxide Silicon
CPU	Central Processing Unit
DAP	Device Access Port
DMU	Data Management Unit
EBC	External Bus Controller
ESFR	Extended Special Function Register
EVVR	Embedded Validated Voltage Regulator
Flash	Non-volatile memory that may be electrically erased
GPR	General Purpose Register
GPT	General Purpose Timer unit
HLL	High Level Language
IIC	Inter Integrated Circuit (Bus)
IIS	Inter Integrated Circuit Sound (Bus)
IO	Input/Output
JTAG	Joint Test Access Group
LIN	Local Interconnect Network
LPR	Low Power Reference
LQFP	Low Profile Quad Flat Pack
LXBus	Internal representation of the external bus
MAC	Multiply/Accumulate (unit)
MCDS	Multi Core Debug System
MPU	Memory Protection Unit

OCDS	On-Chip Debug Support
OTP	One-Time Programmable memory
PEC	Peripheral Event Controller
PLA	Programmable Logic Array
PLL	Phase Locked Loop
PMU	Program Management Unit
PVC	Power Validation Circuit
PWM	Pulse Width Modulation
RAM	Random Access Memory
RISC	Reduced Instruction Set Computing
ROM	Read Only Memory
RTC	Real Time Clock
SFR	Special Function Register
SoC	System on Chip
SSC	Synchronous Serial Channel
SWD	Supply Watchdog
UART	Universal Asynchronous Receiver/Transmitter
USIC	Universal Serial Interface Channel

1.2 Naming Conventions

The diverse bitfields used for control functions and status indication and the registers housing them are equipped with unique names wherever applicable. Thereby these control structures can be referred to by their names rather than by their location. This makes the descriptions by far more comprehensible.

To describe regular structures (such as ports) indices are used instead of a plethora of similar bit names, so bit 3 of port 5 is referred to as P5.3.

Where it helps to clarify the relation between several named structures, the next higher level is added to the respective name to make it unambiguous.

The term ADC0_GLOBCTR clearly identifies register GLOBCTR as part of module ADC0, the term SYSCON0.CLKSEL clearly identifies bitfield CLKSEL as part of register SYSCON0.

2 Architectural Overview

The diagram below shows the functional blocks and their basic connectivity within an XC27x8X System.

The system components are built around a C166SV2 CPU which is an enhanced member of Infineons C166 family of CPU cores. This evolutionary step of the CPU provides a mixed 16/32 bit instruction set compatible to the C166 instruction set. Additionally 32-bit DSP/MAC instructions are available. This ensures easy upgrade for existing C166 software and provides 32-bit performance assets.

Functional abstracts of the components contained in a XC27x8X are provided in the following subchapters.

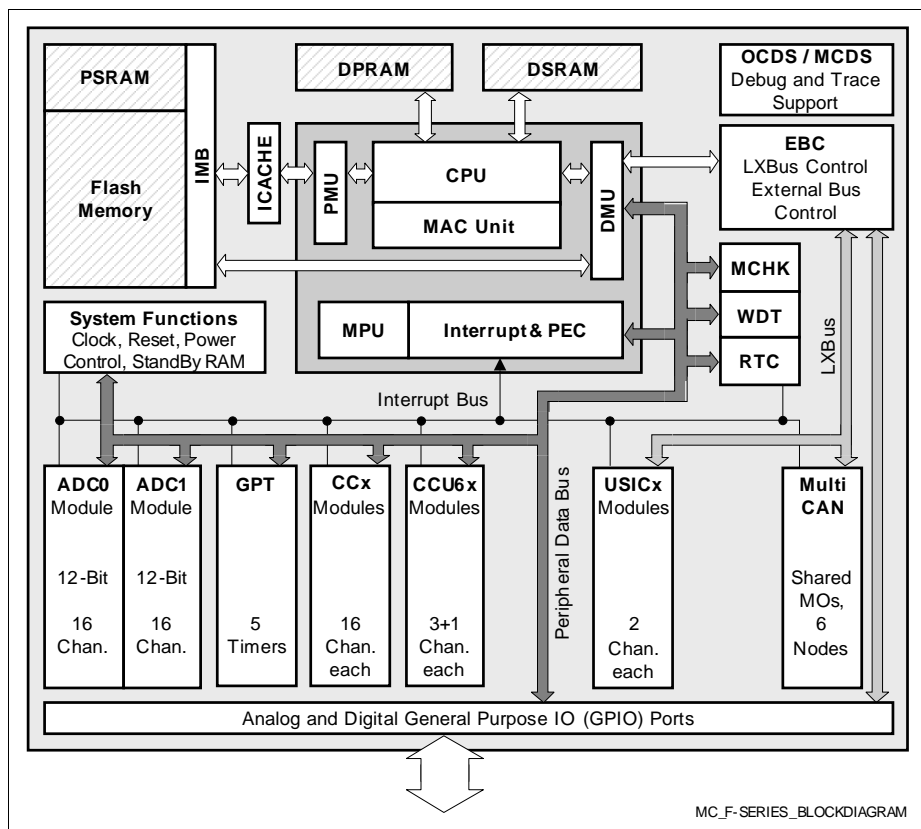


Figure 2-1 XC27x8X Block Diagram

2.1 Summary of Features

The XC27x8X combines the extended functionality and performance of the C166SV2 Core with powerful on-chip peripheral subsystems and on-chip memory units. The following key features are available within the range of XC27x8X devices:

Intelligent On-Chip Peripheral Subsystems

- Two synchronizable A/D Converters (ADC) with programmable resolution of 12-bit, 10-bit or 8-bit and conversion time of less than 1 μ s, up to 16 analog input channels, auto scan modes, channel injection, data reduction features
- One Capture/Compare Unit (CC) with 2 independent time bases, very flexible PWM unit/event recording unit with different operating modes, includes two 16-bit timers/counters, maximum resolution f_{SYS}
- Four Capture/Compare Units (CCU6) for flexible PWM Signal Generation (3 Capture/Compare Channels and 1 Compare Channel)
- Two Multifunctional General Purpose Timer Units:
 - GPT1: three 16-bit timers/counters, maximum resolution $f_{\text{SYS}}/4$
 - GPT2: two 16-bit timers/counters, maximum resolution $f_{\text{SYS}}/2$
- Five Universal Serial Interface Channel Units (USIC) providing 2 interface channels per unit, baud rate generator, receive/transmit FIFOs, programmable data length and shift direction, usable as UART, SPI-like, IIC, IIS, and LIN interface
- Controller Area Network (MultiCAN) Module, Rev. 2.0B active, up to 6 nodes operating independently or exchanging data via a gateway function, Full-CAN/Basic-CAN
- Real Time Clock (RTC) with alarm interrupt
- Watchdog Timer (WDT) with programmable time intervals
- Bootstrap Loaders for flexible system initialization
- Protection management for system configuration and control registers

Integrated On-Chip Memories

- 8 Kbytes on-chip Stand-By RAM (SBRAM) to preserve data during power-saving
- 2 Kbytes Dual-Port RAM (DPRAM) for variables, register banks, and stacks
- 24 Kbytes on-chip high-speed Data SRAM (DSRAM) for variables and stacks
- 64 Kbytes on-chip high-speed Program SRAM (PSRAM) for code and data
- 1088 Kbytes on-chip Flash Program Memory for instruction code or constant data

Instruction cache

- 16 Kbytes of 2-way set associative instruction cache (ICACHE)
- Hit and miss counters
- Simple porting of existing software

High Performance 16-bit CPU with Five-Stage Pipeline and MAC Unit

- Single clock cycle instruction execution for most instructions
- Single clock cycle multiplication (16-bit × 16-bit)
- 4 + 17 clock cycles division (32-bit/16-bit), 4 cycles pipeline delay + 17 cycles background execution
- Single cycle multiply and accumulate instruction (MAC) execution
- 32-bit addition and 32-bit subtraction (MAC unit)
- 40-bit barrel shifter and 40-bit accumulator
- Automatic saturation or rounding included
- Multiple high bandwidth internal data buses
- Register-based design with multiple, memory mapped register banks
- Two additional local register banks
- Fast context switching support
- 16 Mbytes of linear address space for code and data (von Neumann architecture)
- System stack cache support with automatic stack overflow/underflow detection
- High performance branch, call, and loop processing
- Zero-cycle jump execution

Control Oriented Instruction Set with High Efficiency

- Bit, byte, and word data types
- Flexible and efficient addressing modes for high code density
- Enhanced boolean bit manipulation with direct addressability of 6 Kbits for peripheral control and user-defined flags
- Hardware traps to identify exception conditions during runtime
- HLL support for semaphore operations and efficient data access

Safety Support Features

- Memory Protection Unit (MPU)
- Memory Checker Module (MCHK) for CRC generation

Embedded Computing Features

- System Timer (STM) for real time clock support

Power Management Features

- Two IO power domains fulfill system requirements from 3 V to 5 V
- Embedded voltage regulator (core supply voltage 1.5V)
- Supply Watchdog (SWD)
- Core Power Validation (PVC)
- Separately controllable core power domains support wake-up via external triggers or on-chip timer while drastically reducing the power consumption
- Gated clock concept for improved power consumption and EMC

- Programmable system slowdown via clock generation unit
- Flexible management of peripherals, can be individually disabled
- Programmable frequency output

16-Priority-Level Interrupt System

- 112 interrupt nodes with separate interrupt vectors on 16 priority levels
- 7 cycles minimum interrupt latency in case of internal program execution
- Fast external interrupts
- Programmable external interrupt source selection
- Programmable vector table (start location and step-width)

16-Channel Peripheral Event Controller (PEC)

- Interrupt driven single cycle data transfer
- Programmable PEC interrupt request level, (15 down to 8)
- Transfer count option
(standard CPU interrupt after programmable number of PEC transfers)
- Transfer counters programmable supporting up to 65535 transfers
- Automatic PEC pointer increase separately programmable for source and destination pointers to support memory block transfers
- Separate interrupt level for PEC termination interrupts selectable
- Overhead from saving and restoring system state for interrupt requests eliminated
- Full 24-bit addresses for source and destination pointers, supporting transfers within the total address space

On-Chip Debug Support

- Communication through DAP interface (2-wire) or JTAG interface (5-wire)
- On-chip debug controller with optional break interface
- Hardware, software and external pin breakpoints
- Up to 4 instruction pointer breakpoints
- Debug event control, e.g. with monitor call or CPU halt or trigger of data transfer
- Dedicated DEBUG instructions with control via DAP/JTAG interface
- Access to any internal register or memory location via DAP/JTAG interface
- Single step support and watchpoints with MOV-injection

Input/Output Lines With Individual Bit Addressability

- Tri-stated in input mode
- Push/pull or open drain output mode
- Programmable port driver control
- Two I/O power domains with a supply voltage range from 3.0 V to 5.5 V
(core-logic and oscillator input voltage is 1.5 V)

Various Temperature Ranges

- -40 to +85 °C
- -40 to +110 °C
- -40 to +125 °C

Note: Not all derivatives are offered in all temperature ranges.

Infineon CMOS Process

- Low power CMOS technology enables power saving modes with flexible power management.

Green Plastic Low-Profile Quad Flat Pack (LQFP) Packages

Device packages are lead-free RoHS compliant surface mount device (SMD) types with 0.5 mm (19.7 mil) lead spacing. For details about package availability for a particular derivative please check the datasheet. For informations on available delivery options for assembly support and general package see <http://www.infineon.com/packages>

- PG-LQFP-144, 20 × 20mm body
- PG-LQFP-100, 14 × 14mm body

2.2 System Core Components

The XC27x8X system core consists of the CPU with memory protection unit (MPU) and the memory interface blocks for program and data memories - PMU and DMU.

2.2.1 Central Processing Unit (CPU)

The CPU consists of a 5-stage execution pipeline with a 2-stage instruction-fetch pipeline, a 16/32-bit arithmetic and logic unit (ALU), a 40-bit multiply and accumulate unit (MAC), a register-file providing three register banks, and dedicated core (C)SFRs. The ALU features a multiply-and-divide unit, a bit-mask generator, and a barrel shifter.

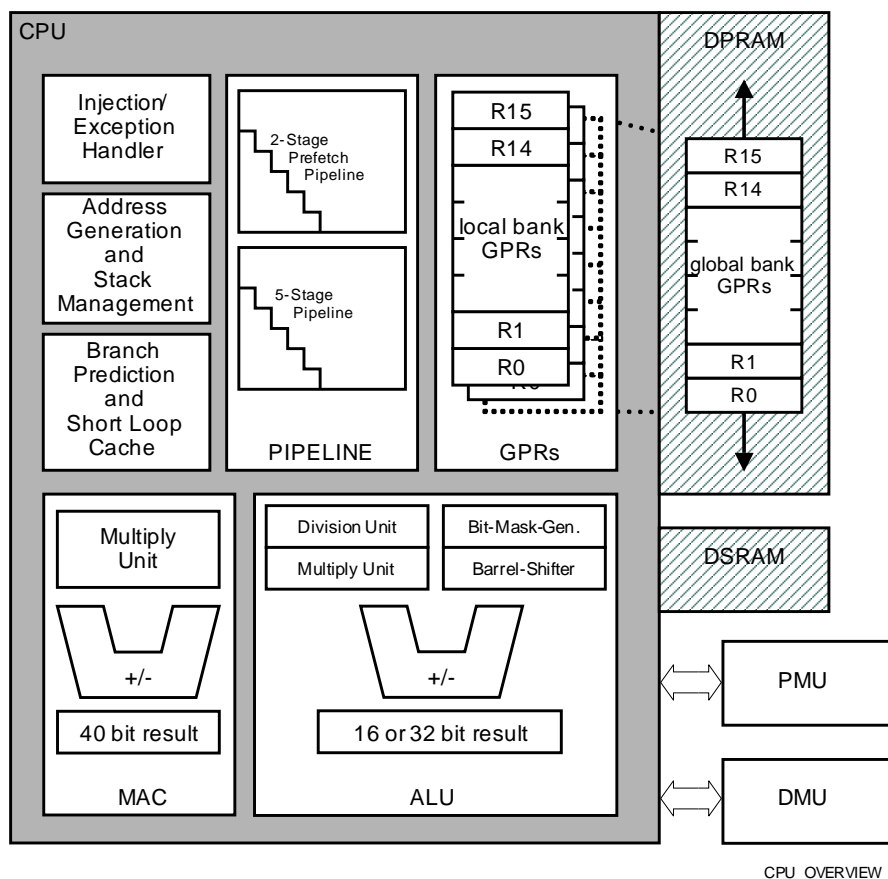


Figure 2-2

Architectural Overview

With this hardware most XC27x8X instructions can be executed in a single machine cycle of 12.5 ns with an 80-MHz CPU clock. For example, shift and rotate instructions are always processed during one machine cycle, no matter how many bits are shifted. Also, multiplication and most MAC instructions execute in one cycle. All multiple-cycle instructions have been optimized so that they can be executed very fast; for example, a 32-/16-bit division is started within 4 cycles while the remaining cycles are executed in the background. Another pipeline optimization, the branch target prediction, eliminates the execution time of branch instructions if the prediction was correct.

The CPU has a register context consisting of up to three register banks with 16 word-wide GPRs each at its disposal. One of these register banks is physically allocated within the on-chip DPRAM area. A Context Pointer (CP) register determines the base address of the active register bank accessed by the CPU at any time. The number of these register bank copies is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 32 Kwords is provided for storage of temporary data. The system stack can be allocated to any location within the address space (preferably in the on-chip RAM area); it is accessed by the CPU with the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared with the stack pointer value during each stack access to detect stack overflow or underflow.

The high performance of the CPU hardware implementation can be best utilized by the programmer with the highly efficient XC27x8X instruction set. This includes the following instruction classes:

- Standard Arithmetic Instructions
- DSP-Oriented Arithmetic Instructions
- Logical Instructions
- Boolean Bit Manipulation Instructions
- Compare and Loop Control Instructions
- Shift and Rotate Instructions
- Prioritize Instruction
- Data Movement Instructions
- System Stack Instructions
- Jump and Call Instructions
- Return Instructions
- System Control Instructions
- Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

2.2.2 Memory Protection Unit (MPU)

The XC27x8X's Memory Protection Unit (MPU) protects user-specified memory areas from unauthorized read, write, or instruction fetch accesses. The MPU can protect the whole address space including the peripheral area. This completes established mechanisms such as the register security mechanism or stack overrun/underrun detection.

Four Protection Levels support flexible system programming where operating system, low level drivers, and applications run on separate levels. Each protection level permits different access restrictions for instructions and/or data.

Every access is checked (if the MPU is enabled) and an access violating the permission rules will be marked as invalid and leads to a protection trap.

A set of protection registers for each protection level specifies the address ranges and the access permissions. Applications requiring more than 4 protection levels can dynamically re-program the protection registers.

2.2.3 Programmable Multiple Priority Interrupt System

The XC27x8X provides 112 separate interrupt nodes that may be assigned to 16 priority levels with 8 group priorities on each level. Most interrupt sources are connected to a dedicated interrupt node. In some cases, multi-source interrupt nodes are incorporated for efficient use of system resources. These nodes can be activated by several source requests and are controlled via interrupt subnode control registers.

The following enhancements within the XC27x8X allow processing of a large number of interrupt sources:

- **Peripheral Event Controller (PEC):** This processor is used to off-load many interrupt requests from the CPU. It avoids the overhead of entering and exiting interrupt or trap routines by performing single-cycle interrupt-driven byte or word data transfers between any two locations with an optional increment of the PEC source pointer, the destination pointer, or both. Only one cycle is 'stolen' from the current CPU activity to perform a PEC service.
- **Multiple Priority Interrupt Controller:** This controller allows all interrupts to be assigned any specified priority. Interrupts may also be grouped, which enables the user to prevent similar priority tasks from interrupting each other. For each of the interrupt nodes, there is a separate control register which contains an interrupt request flag, an interrupt enable flag, and an interrupt priority bitfield. After being accepted by the CPU, an interrupt service can be interrupted only by a higher prioritized service request. For standard interrupt processing, each of the interrupt nodes has a dedicated vector location.
- **Multiple Register Banks:** Two local register banks for immediate context switching add to a locatable global register bank. The user can specify several register banks located anywhere in the internal DPRAM and made of up to sixteen general purpose

registers. A single instruction switches from one register bank to another (switching banks flushes the pipeline, changing the global bank requires a validation sequence).

The XC27x8X is capable of reacting very quickly to non-deterministic events because its interrupt response time is within a very narrow range of typically 7 clock cycles (in the case of internal program execution). Its fast external interrupt inputs are sampled every clock cycle and allow even very short external signals to be recognized.

The XC27x8X also provides an excellent mechanism to identify and process exceptions or error conditions that arise during run-time, so called 'Hardware Traps'. A hardware trap causes an immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location). The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Unless another, higher prioritized, trap service is in progress, a hardware trap will interrupt any current program execution. In turn, a hardware trap service can normally not be interrupted by a standard or PEC interrupt.

Software interrupts are supported by means of the 'TRAP' instruction in combination with an individual trap (interrupt) number.

2.2.4 Interfaces to System Resources

The CPU of the XC27x8X interfaces to the system resources via several bus systems which contribute to the overall performance by transferring data concurrently.

The Dual Port RAM (DPRAM) and Data SRAM (DSRAM) are directly connected to the CPU and provide the best performance for data storage. Neither of these memories can be used for program execution.

The Program Management Unit (PMU) controls accesses to the on-chip program memory blocks such as the Flash module and the Program SRAM (PSRAM) and also fetches instructions from external memory. The program memories can also be used for data storage.

The Data Management Unit (DMU) controls accesses to the on-chip peripherals connected to the peripheral data bus, and to resources on the external bus. External program or data accesses (including data accesses to peripherals connected to the on-chip LxBus) are executed by the External Bus Controller (EBC).

2.3 On-Chip System Resources

The XC27x8X controllers provide a number of powerful system resources designed around the CPU. The combination of CPU and these resources results in the high performance of the members of this controller family.

2.3.1 Memory Areas

The memory space of the XC27x8X is configured in a Von Neumann architecture. This means that code memory, data memory, registers, and IO ports are organized within the same linear address space which covers up to 16 Mbytes. The entire memory space can be accessed byte-wise or word-wise. Particular portions of the on-chip memory have been made directly bit addressable as well.

Note: The actual memory sizes depend on the selected device type. This overview describes the maximum block sizes.

Up to 1088 Kbytes of on-chip Flash memory store code or constant data. The on-chip Flash memory consists of up to 4 Flash modules, each built up from 4-Kbyte sectors. Each sector can be separately write protected¹⁾, erased and programmed (in blocks of 128 bytes). The complete Flash area can be read-protected. A user-defined password sequence temporarily unlocks protected areas. The Flash modules combine 128-bit read accesses with protected and efficient writing algorithms for programming and erasing. Dynamic error correction provides extremely high read data security for all read accesses. Accesses to different Flash modules can be executed in parallel.

Note: Program execution from on-chip program memory is the fastest of all possible alternatives and results in maximum performance. The size of the on-chip program memory depends on the chosen derivative. On-chip program memory also includes the PSRAM.

Up to 64 Kbytes of on-chip Program SRAM (PSRAM) are provided to store user code or data. The PSRAM is accessed via the PMU and is, therefore, optimized for code fetches. A section of the PSRAM with programmable size can be write-protected.

24 Kbytes of on-chip Data SRAM (DSRAM) are provided as a storage for general user data. The DSRAM is accessed via a separate interface and is, therefore, optimized for data accesses.

2 Kbytes of on-chip Dual-Port RAM (DPRAM) are provided as a storage for user defined variables, for the system stack, and in particular for general purpose register banks. A register bank can consist of up to 16 word-wide (R0 to R15) and/or byte-wide (RL0, RH0, ..., RL7, RH7) so-called General Purpose Registers (GPRs).

¹⁾ To save control bits, sectors are clustered for protection purposes, they remain separate for programming/erasing.

The upper 256 bytes of the DPRAM are directly bitaddressable. When used by a GPR, any location in the DPRAM is bitaddressable.

8 Kbytes of on-chip Stand-By SRAM (SBRAM) are provided as a storage for system-relevant user data that must be preserved while the major part of the device is powered down. The SBRAM is accessed via a specific interface and is powered via domain M.

The CPU has an actual register context of up to 16 wordwide and/or byte-wide global GPRs at its disposal, which are physically located within the on-chip RAM area. A Context Pointer (CP) register determines the base address of the active global register bank to be accessed by the CPU at a time. The number of register banks is restricted only by the available internal RAM space. For easy parameter passing, a register bank may overlap other register banks.

A system stack of up to 32 Kwords is provided as storage for temporary data. The system stack can be located anywhere within the complete addressing range and it is accessed by the CPU via the Stack Pointer (SP) register and the Stack Pointer Segment (SPSEG) register. Two separate SFRs, STKOV and STKUN, are implicitly compared against the stack pointer value upon each stack access for the detection of a stack overflow or underflow. This mechanism also supports the control of a bigger virtual stack. Maximum performance for stack operations is achieved by allocating the system stack to internal data RAM areas (DPRAM, DSRAM).

Hardware detection of the selected memory space is placed at the internal memory decoders and allows the user to specify any address directly or indirectly and obtain the desired data without using temporary registers or special instructions.

For Special Function Registers three areas of the address space are reserved: The standard Special Function Register area (SFR) uses 512 bytes, while the Extended Special Function Register area (ESFR) uses the other 512 bytes. A range of 4 Kbytes is provided for the internal IO area (XSFR). SFRs are wordwide registers which are used for controlling and monitoring functions of the different on-chip units. Unused SFR addresses are reserved for future members of the XC27x8X Derivatives with enhanced functionality. Therefore, they should either not be accessed, or written with zeros, to ensure upward compatibility.

In order to meet the needs of designs where more memory is required than is provided on chip, up to 12 Mbytes (approximately, see memory chapter) of external RAM and/or ROM can be connected to the microcontroller. The External Bus Interface also provides access to external peripherals.

2.3.2 External Bus Interface

To meet the needs of designs where more memory is required than is provided on chip, up to 12 Mbytes of external RAM/ROM/Flash or peripherals can be connected to the XC27x8X microcontroller via its external bus interface.

Architectural Overview

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed either to Single Chip Mode when no external memory is required, or to an external bus mode with the following possible selections¹⁾:

- Address Bus Width with a range of 0 ... 24-bit
- Data Bus Width 8-bit or 16-bit
- Bus Operation Multiplexed or Demultiplexed

In the demultiplexed bus modes, addresses are output on Port 0 and Port 1 and data is input/output on Port 10 and Port 2. In the multiplexed bus modes both addresses and data use Port 10 and Port 2 for input/output. The high order address (segment) lines use Port 2. The number of active address lines is selectable, so the external address space can be restricted. This is required when interface lines are assigned to Port 2.

For up to five address areas the bus mode (multiplexed/demultiplexed), the data bus width (8-bit/16-bit) and even the length of a bus cycle (waitstates, signal delays) can be selected independently. This allows access to a variety of memory and peripheral components directly and with maximum efficiency.

Access to very slow memories or modules with varying access times is supported via a particular 'Ready' function. The active level of the control input signal is selectable.

The external bus timing is related to the rising edge of the reference clock output CLKOUT. The external bus protocol is compatible with that of the standard C166 Family.

For applications which require less than 64 Kbytes of address space, a non-segmented memory model can be selected, where all locations can be addressed by 16 bits. Thus, the upper Port 2 is not needed as an output for the upper address bits (Axx ... A16), as is the case when using the segmented memory model.

The EBC also controls accesses to resources connected to the **on-chip LXBus**. The LXBus is an internal representation of the external bus and allows accessing integrated peripherals and modules in the same way as external components.

The MultiCAN module and the USIC modules are connected to and accessed via the LXBus.

1) Bus modes are switched dynamically if several address windows with different mode settings are used.

2.4 On-Chip Peripheral Blocks

The XC27x8X Derivatives clearly separates peripherals from the core. This structure permits the maximum number of operations to be performed in parallel and allows peripherals to be added or deleted from family members without modifications to the core. Each functional block processes data independently and communicates information over common buses. Peripherals are controlled by data written to the respective Special Function Registers (SFRs). These SFRs are located within either the standard SFR area (00'FE00_H ... 00'FFFF_H), the extended ESFR area (00'F000_H ... 00'F1FF_H), or within the internal IO area (00'E000_H ... 00'EFFF_H).

These built-in peripherals either allow the CPU to interface with the external world or provide functions on-chip that otherwise would need to be added externally in the respective system.

The XC27x8X generic peripherals are:

- **Memory Checker Unit (MCHK)**
- **General Purpose Timers (GPT)**
- **Watchdog Timer (WDT)**
- **Capture/Compare Unit CAPCOM (CC2)**
- **Capture/Compare Unit CCU6 (CCU6)**
- **Analog/Digital Converter (ADC)**
- **Real Time Clock (RTC)**
- **Parallel Ports**

Because the LXBus is the internal representation of the external bus, it does not support bit-addressing. Accesses are executed by the EBC as if it were external accesses. The LXBus connects on-chip peripherals to the CPU:

- **Universal Serial Interface Channel Modules (USIC)**
- **MultiCAN Module (MultiCAN)**

Each peripheral also contains a set of Special Function Registers (SFRs) which control the functionality of the peripheral and temporarily store intermediate data results. Each peripheral has an associated set of status flags. Individually selected clock signals are generated for each peripheral from binary multiples of the master clock.

Note: The available peripherals for the different derivatives are listed in the respective datasheet.

Peripheral Interfaces

The on-chip peripherals generally have two different types of interfaces: a bus interface to the CPU and interface signals to other on-chip peripherals or to external hardware. Communication between the CPU and peripherals is performed through Special Function Registers (SFRs) and interrupts. The SFRs serve as control/status and data registers for the peripherals. Interrupt requests are generated by the peripherals based on specific events which occur during their operation, such as operation complete, error, etc.

To interface with external hardware, specific pins of the parallel ports are used, when an input or output function has been selected for a peripheral. During this time, the port pins are controlled either by the peripheral (when used as outputs) or by the external hardware which controls the peripheral (when used as inputs). This is called the 'alternate (input or output) function' of a port pin, in contrast to its function as a general purpose I/O pin.

Peripheral Timing

Internal operation of the CPU and peripherals is based on the system clock (f_{SYS}). The clock generation unit uses external (e.g. a crystal) or internal clock sources to generate the system clock signal. Peripherals can be disconnected from the clock signal either temporarily to save energy or permanently if they are not used in a specific application. Peripheral SFRs may be accessed by the CPU once per state. When an SFR is written to by software in the same state where it is also to be modified by the peripheral, the software write operation has priority. Further details on peripheral timing are included in the specific sections describing each peripheral.

Programming Hints

- **Access to SFRs:** The SFRs reside in various data pages of the memory space. The following addressing mechanisms allow access to the SFRs:
 - Indirect or direct addressing with **16-bit (mem) addresses** must guarantee that the used data page pointer (DPP0 ... DPP3) selects the corresponding data page.
 - Accesses via the Peripheral Event Controller (**PEC**) use the SRCPx and DSTPx pointers instead of the data page pointers.
 - **Short 8-bit (reg) addresses** to the standard SFR area do not use the data page pointers but directly access the registers within this 512-byte area.
 - **Short 8-bit (reg) addresses** to the extended **ESFR** area require switching to the 512-byte Extended SFR area. This is done via the EXTension instructions EXTR, EXTP(R), EXTS(R).
- **Byte Write Operations** to wordwide SFRs via indirect or direct 16-bit (mem) addressing or byte transfers via the PEC force zeros in the non-addressed byte. Byte write operations via short 8-bit (reg) addressing can access only the low byte of an SFR and force zeros in the high byte. It is therefore recommended, to use the bitfield

Architectural Overview

instructions (BFLDL and BFLDH) to write to any number of bits in either byte of an SFR without disturbing the non-addressed byte and the unselected bits.

- **Write Operations to Write-Only Bits/Registers** usually modify bits within other registers. In some cases this modification is controlled by state machines. Therefore, the effect of the write operation may not be visible, when the modified register is read immediately after the write access that triggers the modification.
- **Reserved Bits:** Some of the bits which are contained in the XC27x8X's SFRs are marked as 'Reserved'. User software should never write '1's to reserved bits. These bits are currently not implemented and may be used in future products to invoke new functions. In that case, the active state for those new functions will be '1', and the inactive state will be '0'. Therefore writing only '0's to reserved locations allows portability of the current software to future devices. After read accesses, reserved bits should be ignored or masked out.

Capture/Compare Unit CAPCOM (CC2)

CAPCOM unit supports generation and control of timing sequences on up to 16 channels with a maximum resolution of 1 system clock cycle (8 cycles in staggered mode). The CAPCOM unit is typically used to handle high speed I/O tasks such as pulse and waveform generation, pulse width modulation (PMW), Digital to Analog (D/A) conversion, software timing, or time recording relative to external events.

Two 16-bit timers with reload registers provide two independent time bases for each capture/compare register.

The input clock for the timers is programmable to several prescaled values of the internal system clock, or may be derived from an overflow/underflow of timer T6 in module GPT2. This provides a wide range of variation for the timer period and resolution and allows precise adjustments to the application specific requirements. In addition, external count inputs allow event scheduling for the capture/compare registers relative to external events.

The capture/compare register array contains 16 dual purpose capture/compare registers, each of which may be individually allocated to either CAPCOM timer and programmed for capture or compare function.

All registers have each one port pin associated with it which serves as an input pin for triggering the capture function, or as an output pin to indicate the occurrence of a compare event.

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched ('captured') into the capture/compare register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

Architectural Overview

The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the selected compare mode.

Table 2-1 Compare Modes

Compare Mode	Function
Mode 0	Interrupt-only compare mode; several compare interrupts per timer period are possible
Mode 1	Pin toggles on each compare match; several compare events per timer period are possible
Mode 2	Interrupt-only compare mode; only one compare interrupt per timer period is generated
Mode 3	Pin set '1' on match; pin reset '0' on compare timer overflow; only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; pin toggles on each compare match; several compare events per timer period are possible
Single Event Mode	Generates single edges or pulses; can be used with any compare mode

Capture/Compare Unit CCU6 (CCU6)

The CCU6 units support generation and control of timing sequences on up to three 16-bit capture/compare channels plus one independent 16-bit compare channel.

In compare mode, the CCU6 units provide two output signals per channel which have inverted polarity and non-overlapping pulse transitions (deadtime control). The compare channel can generate a single PWM output signal and is further used to modulate the capture/compare output signals.

In capture mode the contents of compare timer T12 is stored in the capture registers upon a signal transition at pins CCx.

The output signals can be generated in edge-aligned or center-aligned PWM mode. They are generated continuously or in single-shot mode.

Compare timers T12 and T13 are free running timers which are clocked by the prescaled system clock.

For motor control applications (brushless DC-drives) both subunits may generate versatile multichannel PWM signals which are basically either controlled by compare timer T12 or by a typical hall sensor pattern at the interrupt inputs (block commutation). The latter mode provides noise filtering for the hall inputs and supports automatic rotational speed measurement.

The trap function offers a fast emergency stop without CPU activity. Triggered by an external signal (CTR_{AP}) the outputs are switched to selectable logic levels which can be adapted to the connected power stages.

Note: The number of available CCU6 units and channels depends on the selected device type.

General Purpose Timers (GPT)

The GPT12E unit represents a very flexible multifunctional timer/counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT12E unit incorporates five 16-bit timers which are organized in two separate blocks, GPT1 and GPT2. Each timer in each block may operate independently in a number of different modes, or may be concatenated with another timer of the same block.

Each of the three timers T2, T3, T4 of **block GPT1** can be configured individually for one of four basic modes of operation, which are Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the system clock, divided by a programmable prescaler, while Counter Mode allows a timer to be clocked in reference to external events.

Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the 'gate' level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which serves as gate or clock input. The maximum resolution of the timers in block GPT1 is 4 system clock cycles.

The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD) to facilitate e.g. position tracking.

In Incremental Interface Mode the GPT1 timers (T2, T3, T4) can be directly connected to the incremental position sensor signals A and B via their respective inputs TxIN and TxEUD. Direction and count signals are internally derived from these two input signals, so the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer overflow/underflow. The state of this latch may be output on pin T3OUT e.g. for time out monitoring of external hardware components. It may also be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

With its maximum resolution of 2 system clock cycles, the **GPT2 block** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which

Architectural Overview

is derived from the CPU clock via a programmable prescaler or with external signals. The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD). Concatenation of the timers is supported via the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can additionally be used to clock the CAPCOM2 timers, and to cause a reload from the CAPREL register.

The CAPREL register may capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared after the capture procedure. This allows the XC27x8X to measure absolute time differences or to perform pulse multiplication without software overhead.

The capture trigger (timer T5 to CAPREL) may also be generated upon transitions of GPT1 timer T3's inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.

Real Time Clock (RTC)

The Real Time Clock (RTC) module of the XC27x8X is directly clocked with a separate clock signal. Several internal and external clock sources can be selected via register RTCCLKCON. It is, therefore, independent from the selected clock generation mode of the XC27x8X.

The RTC basically consists of a chain of divider blocks:

- Selectable 32:1 and 8:1 dividers (on - off)
- The reloadable 16-bit timer T14
- The 32-bit RTC timer block (accessible via registers RTCH and RTCL), made of:
 - a reloadable 10-bit timer
 - a reloadable 6-bit timer
 - a reloadable 6-bit timer
 - a reloadable 10-bit timer

All timers count up. Each timer can generate an interrupt request. All requests are combined to a common node request.

Note: The registers associated with the RTC are not affected by an application reset in order to maintain the contents even when intermediate resets are executed.

The RTC module can be used for different purposes:

- System clock to determine the current time and date
- Cyclic time based interrupt, to provide a system time tick independent of CPU frequency and other resources
- 48-bit timer for long term measurements
- Alarm interrupt for wake-up on a defined time

Analog/Digital Converter (ADC)

For analog signal measurement, two 12-bit A/D converters (ADC0, ADC1) with 16 multiplexed input channels including a sample and hold circuit have been integrated on-chip. They use the method of successive approximation. The sample time (for loading the capacitors) and the conversion time are programmable and can thus be adjusted to the external circuitry. The A/D converters can also operate in 8-bit or 10-bit conversion mode, where the conversion time is further reduced.

Several independent conversion result registers, selectable interrupt requests, and highly flexible conversion sequences provide a high degree of programmability to fulfill the requirements of the respective application. Both modules can be synchronized to allow parallel sampling of two input channels.

For applications that require more analog input channels, external analog multiplexers can be controlled automatically.

For applications that require less analog input channels, the remaining channel inputs can be used as digital input port pins.

The A/D converters of the XC27x8X support two types of request sources which can be triggered by several internal and external events.

- Scan requests are activated at the same time and then executed in a predefined sequence.
- Queued requests are executed in a user-defined sequence.

In addition, the conversion of a specific channel can be inserted into a running sequence without disturbing this sequence. All requests are arbitrated according to the priority level that has been assigned to them.

Data reduction features, such as limit checking or result accumulation, reduce the number of required CPU accesses and so allow the precise evaluation of analog inputs (high conversion rate) even at low CPU speed.

The Peripheral Event Controller (PEC) may be used to control the A/D converters or to automatically store conversion results into a table in memory for later evaluation, without requiring the overhead of entering and exiting interrupt routines for each data transfer. Therefore, each A/D converter contains 8 result registers which can be concatenated to build a result FIFO. Wait-for-read mode can be enabled for each result register to prevent loss of conversion data.

In order to decouple analog inputs from digital noise and to avoid input trigger noise those pins used for analog input can be disconnected from the digital input stages under software control. This can be selected for each pin separately via registers P5_DIDIS and P15_DIDIS (Port x Digital Input Disable).

The Auto-Power-Down feature of the A/D converters minimizes the power consumption when no conversion is in progress.

Note: The number of available analog channels depends on the selected device type.

Universal Serial Interface Channel Modules (USIC)

Each USIC module provides two communication channels which can be individually configured to match the application needs, e.g. the protocol can be selected or changed during run time without the need for a reset. The following protocols are supported:

- **UART** (ASC, asynchronous serial channel)
 - Module capability: receiver/transmitter with max. baud rate $f_{\text{SYS}} / 4$
 - Wide baud rate range down to single-digit baud rates
 - Number of data bits per data frame: 1 to 63
 - MSB or LSB first
- **LIN** Support by hardware (Local Interconnect Network)
 - Data transfers based on ASC protocol
 - Baud rate detection possible by built-in capture event of baud rate generator
 - Checksum generation under software control for higher flexibility
- **SSC/SPI** (synchronous serial channel with or without slave select lines)
 - Module capability: maximum baud rate $f_{\text{SYS}} / 2$, limited by loop delay
 - Number of data bits per data frame 1 to 63, more with explicit stop condition
 - MSB or LSB first
- **IIC** (Inter-IC Bus)
 - Application baud rate 100 kbit/s to 400 kbit/s
 - 7-bit and 10-bit addressing supported
 - Full master and slave device capability
- **IIS** (infotainment audio bus)
 - Module capability: maximum baud rate $f_{\text{SYS}} / 2$

Note: The real baud rates that can be achieved in a real application depend on the operating frequency of the device, timing parameters as described in the Data Sheet, signal delays on the PCB and timings of the peer device.

In addition to the flexible choice of the communication protocol, the USIC structure has been designed to reduce the system load (CPU load) allowing efficient data handling. The following aspects have been considered:

- **Data buffer capability**
 The standard buffer capability includes a double word buffer for receive data and a single word buffer for transmit data. This allows longer CPU reaction times (e.g. interrupt latency).
- **Additional FIFO buffer capability**
 In addition to the standard buffer capability, the received data and the data to be transmitted can be buffered in a FIFO buffer structure. The size of the receive and the transmit FIFO buffer can be programmed independently. Depending on the application needs, a total buffer capability of 64 data words can be assigned to the receive and transmit FIFO buffers of a USIC module (the two channels of the USIC module share the 64 data word buffer).

In addition to the FIFO buffer, a bypass mechanism allows the introduction of high-priority data without flushing the FIFO buffer.

- **Transmit control information**

For each data word to be transmitted, a 5-bit transmit control information has been added to automatically control some transmission parameters, such as word length, frame length, or the slave select control for the SPI protocol. The transmit control information is generated automatically by analyzing the address where the user SW has written the data word to be transmitted (32 input locations = $2^5 = 5$ bit transmit control information).

This feature allows individual handling of each data word, e.g. the transmit control information associated to the data words stored in a transmit FIFO can automatically modify the slave select outputs to select different communication targets (slave devices) without CPU load. Alternatively, it can be used to control the frame length.

- **Flexible frame length control**

The number of bits to be transferred within a data frame is independent of the data word length and can be handled in two different ways. The first option allows automatic generation of frames up to 63 bits with a known length. The second option supports longer frames (even unlimited length) or frames with a dynamically controlled length.

- **Interrupt capability**

The events of each USIC channel can be individually routed to one of 4 service request outputs, depending on the application needs. Furthermore, specific start and end of frame indications are supported in addition to protocol-specific events.

- **Flexible interface routing**

Each USIC channel offers the choice between several possible input and output pins connections for the communications signals. This allows a flexible assignment of USIC signals to pins that can be changed without resetting the device.

- **Input conditioning**

Each input signal is handled by a programmable input conditioning stage with programmable filtering and synchronization capability.

- **Baud rate generation**

Each USIC channel contains an own baud rate generator. The baud rate generation can be based either on the internal module clock or on an external frequency input. This structure allows data transfers with a frequency that can not be generated internally, e.g. to synchronize several communication partners.

- **Transfer trigger capability**

In master mode, data transfers can be triggered events generated outside the USIC module, e.g. at an input pin or a timer unit (transmit data validation). This feature allows time base related data transmission.

- **Debugger support**

The USIC offers specific addresses to read out received data without interaction with the FIFO buffer mechanism. This feature allows debugger accesses without the risk of a corrupted receive data sequence.

Architectural Overview

To reach a desired baud rate, two criteria have to be respected, the module capability and the application environment. The module capability is defined with respect to the module's input clock frequency f_{sys} , being the base for the module operation. Although the module's capability being much higher (depending on the module clock and the number of module clock cycles needed to represent a data bit), the reachable baud rate is generally limited by the application environment. In most cases, the application environment limits the maximum reachable baud rate due to driver delays, signal propagation times, or due to EMI reasons.

Note: Depending on the selected additional functions (such as digital filters, input synchronization stages, sample point adjustment, data structure, etc.), the maximum reachable baud rate can be limited. Please also take care about additional delays, such as (internal or external) propagation delays and driver delays (e.g. for collision detection in ASC mode, for IIC, etc.).

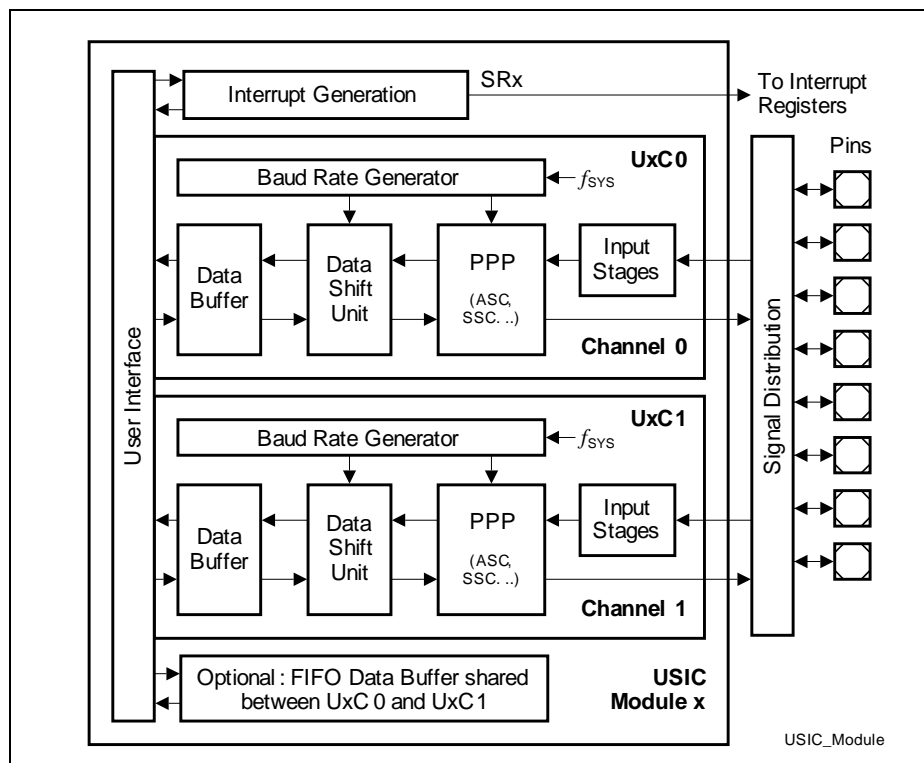


Figure 2-3 USIC Channel Structure

Architectural Overview

The USIC module contains two independent communication channels, with structure shown in **Figure 2-3**.

The data shift unit and the data buffering of each channel support full-duplex data transfers. The protocol-specific actions are handled by protocol pre-processors (PPP). In order to simplify data handling, an additional FIFO data buffer is optionally available for each USIC module to store transmit and receive data for each channel. This FIFO data buffer is not necessarily available in all devices (please refer to USIC implementation chapter for details).

Due to the independent channel control and baud rate generation, the communication protocol, baud rate and the data format can be independently programmed for each communication channel.

MultiCAN Module (MultiCAN)

The MultiCAN module contains up to 6 independently operating CAN nodes with Full-CAN functionality which are able to exchange Data and Remote Frames via a gateway function. Transmission and reception of CAN frames is handled in accordance with CAN specification V2.0 B (active). Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

Note: The number of available CAN nodes depends on the selected device type.

All CAN nodes share a common set of up to 256 message objects. Each message object can be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects can be combined to build gateways between the CAN nodes or to setup a FIFO buffer.

The message objects are organized in double-chained linked lists, where each CAN node has its own list of message objects. A CAN node stores frames only into message objects that are allocated to its own message object list, and it transmits only messages belonging to this message object list. A powerful, command-driven list controller performs all message object list operations.

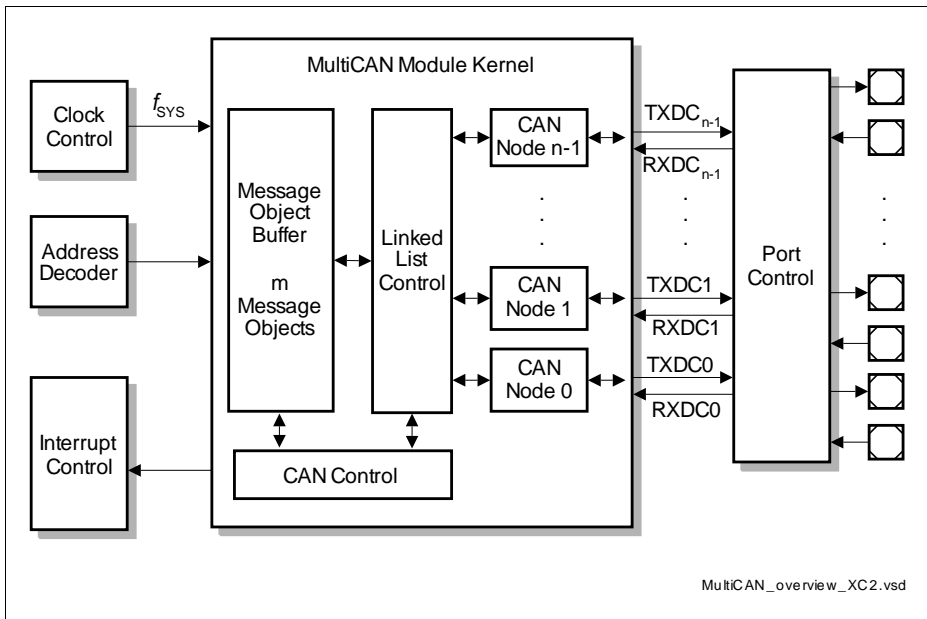


Figure 2-4 Block Diagram of the MultiCAN Module

MultiCAN Features

- CAN functionality conforms to CAN specification V2.0 B active (compliant to ISO 11898)
- 6 independent CAN nodes available
- 256 independent message objects
- Data transfer rate up to 1 Mbit/s, individually programmable for each node
- Flexible and powerful message transfer control and error handling capabilities
- Full-CAN functionality of message objects:
 - Configurable as transmit or receive object
 - Assignable to a message buffer with FIFO algorithm
 - Can handle frames with 11-bit or 29-bit identifiers
 - Provided with programmable acceptance mask register for filtering
 - Can be monitored via a frame counter
 - Configurable to Remote Monitoring Mode
- 16 individually programmable interrupt outputs
- CAN Analyzer Mode for bus monitoring
- Hardware CAN Gateway functionality supported by
 - Advanced Acceptance Filtering
 - Advanced Data Management
 - Advanced Message Object Functionality

Watchdog Timer (WDT)

The Watchdog Timer represents one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer is always enabled after a reset of the chip, and can be disabled and enabled at any time by executing instructions DISWDT and ENWDT. Thus, the chip's start-up procedure is always monitored. The software has to be designed to restart the Watchdog Timer before it overflows. If, due to hardware or software related failures, the software fails to do so, the Watchdog Timer overflows and generates a reset request.

The Watchdog Timer is a 16-bit timer, clocked with the system clock divided by 16,384 or 256. The high byte of the Watchdog Timer register can be set to a prespecified reload value (stored in WDTREL) to allow further variation of the monitored time interval. Each time it is serviced by the application software, the high byte of the Watchdog Timer is reloaded and the low byte is cleared.

Thus, time intervals between 3.2 μ s and 13.4 s can be monitored (@ 80 MHz).

The default Watchdog Timer interval after reset is 6.5 ms (@ 10 MHz).

Memory Checker Unit (MCHK)

The memory checker module (MCHK) of the XC27x8X supports checking the data consistency of memories, registers (e.g. configuration registers), or communication channels. It calculates a checksum on a block of data, often called cyclic redundancy code (CRC). It is implemented as a parallel signature generation based on a multi input linear feedback shift register (MISR). Being based on a linear feedback shift register (LFSR), it also can generate pseudo-random numbers and cyclic codes.

From the programmer's point of view, the MCHK is a set of registers associated with this peripheral. To communicate respective error or operation events a port pin may be used for the signal "MATCH" to generate an external event and an interrupt line may be used for the signal "MISMATCH" to generate an internal event.

Parallel Ports

The port lines have programmable alternate input or output functions associated with them. These alternate functions can be assigned to various port pins to support the optimal utilization for a given application. Port lines that are not used for these alternate functions may be used as general purpose IO (GPIO) port lines.

All port lines are bit-addressable, and all input/output lines can be individually (bit-wise) configured via port control registers. This configuration selects the direction (input/output), push/pull or open-drain operation, and activation of pull devices for each pin. Edge characteristics (shape) and driver characteristics (output current) of the port drivers can be selected for groups of 4 pins. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. During the internal reset, all port pins are configured as inputs without pull devices active.

The following table lists how many lines of each port are connected to package pins.

Table 2-2 Quantitative Summary

Port	LQFP-144	LQFP-100
P0	8	8
P1	8	8
P2	14	14
P3	8	-
P4	8	4
P5	16	11
P6	4	3
P7	5	4
P8	6	-
P9	8	-
P10	16	16
P11	6	-
P15	8	5
Σ GPIO ports	115	73

Note: Additionally to the listed port pins the ESRx pins can be used for GPIO.

2.5 Clock Generation

The Clock Generation Unit uses one programmable on-chip PLL with multiple prescalers to generate the clock signals for the XC27x8X with high flexibility. The system clock f_{SYS} is the reference clock signal, which can be output to the external system. The system clock f_{SYS} can be derived from several internal and external clock sources.

The on-chip high-precision oscillator (OSC_HP) can drive an external crystal or accepts an external clock signal. The oscillator clock frequency can be multiplied by the on-chip PLL (by a programmable factor) or can be divided by a programmable prescaler factor.

An internal clock source can provide a clock signal without requiring an external crystal.

The Oscillator Watchdog (OWD) supervises the input clock and enables an emergency clock if the input clock appears as not reliable.

2.6 Power Management

The XC27x8X can operate within a wide supply voltage range from 3 V to 5 V. The internal core supply voltage is generated via on-chip Embedded Voltage Regulators and is supervised by on-chip Power Validation Circuits.

Two IO power domains help to reduce heat dissipation by supplying the major part of the device with a low voltage (3 V), while still connecting analog 5 V sensor signals to the ADCs (5 V).

The XC27x8X provides several means to control the power it consumes either at a given time or averaged over a certain timespan. Three mechanisms can be used (partly in parallel):

- **Supply Voltage Management** allows the temporary reduction of the supply voltage of major parts of the logic, or even the complete disconnection. This drastically reduces the power consumed because of leakage current, in particular at high temperature. The core logic is split into 2 core power domains, for this purpose. Several power reduction modes provide the optimal balance of power reduction and wake-up time.
- **Clock Generation Management** controls the distribution and the frequency of internal and external clock signals. While the clock signals for currently inactive parts of logic are disabled automatically, the user can reduce the XC27x8X's CPU clock frequency which drastically reduces the consumed power. External circuitry can be controlled via the programmable frequency output EXTCLK.
- **Peripheral Management** permits temporary disabling of peripheral modules. Each peripheral can separately be disabled/enabled.

Wake-up from power reduction modes can be triggered either externally by signals generated by the external system, or internally by the on-chip wake-up timer, which supports intermittent operation of the XC27x8X by generating cyclic wake-up signals. This offers full performance to quickly react on action requests while the intermittent sleep phases greatly reduce the average power consumption of the system.

Note: When selecting the supply voltage and the clock source and generation method, the required parameters must be carefully written to the respective bitfields, to avoid unintended intermediate states. Recommended sequences are provided which ensure the intended operation of power supply system and clock system.

2.7 On-Chip Debug Support (OCDS)

The On-Chip Debug Support system provides a broad range of debug and emulation features built into the XC27x8X. The user software running on the XC27x8X can thus be debugged within the target system environment.

The OCDS is controlled by an external debugging device via the debug interface and an optional break interface. The debugger controls the OCDS via a set of dedicated registers accessible via the debug interface. Additionally, the OCDS system can be controlled by the CPU, e.g. by a monitor program. An injection interface allows the execution of OCDS-generated instructions by the CPU.

Multiple breakpoints can be triggered by on-chip hardware, by software, or by an external trigger input. Single stepping is supported as well as the injection of arbitrary instructions and read/write access to the complete internal address space. A breakpoint trigger can be answered with a CPU-halt, a monitor call, a data transfer, or/and the activation of an external signal.

The data transferred at a watchpoint (see above) can be obtained via the debug interface or via the external bus interface for increased performance.

For the debug interface two variants can be used:

- Debug interface through the DAP port. This interface uses 2 DAP lines.
- Debug interface through the IEEE-1149-conforming JTAG port. This interface uses 4 JTAG lines.

The optional break interface uses another 2 lines.

3 Memory Organization

The memory space of the XC27x8X is configured in a “Von Neumann” architecture. This means that code and data are accessed within the same linear address space. All of the physically separated memory areas, including internal ROM and Flash, internal RAM, the internal Special Function Register Areas (SFRs and ESFRs), the internal IO area, and external memory are mapped into one common address space.

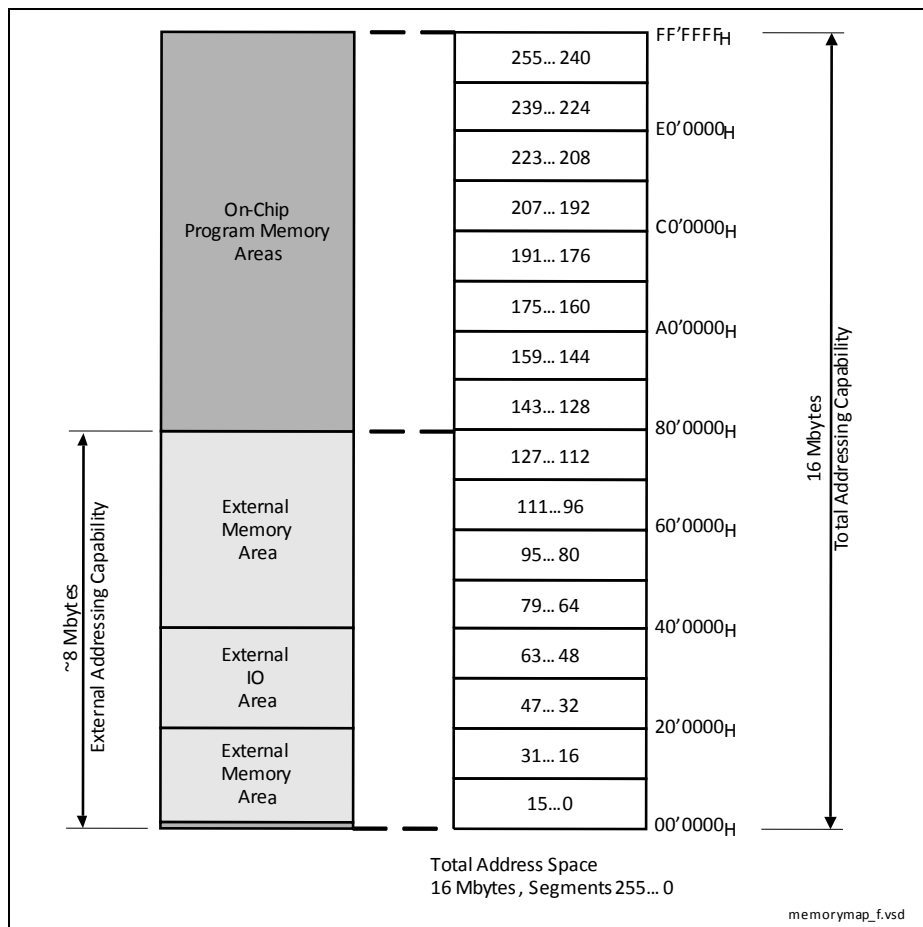


Figure 3-1 Address Space Overview

Memory Organization

The XC27x8X provides a total addressable memory space of 16 Mbytes. This address space is arranged as 256 segments of 64 Kbytes each, and each segment is again subdivided into four data pages of 16 Kbytes each (see [Figure 3-1](#)).

Bytes are stored at even or odd byte addresses. Words are stored in ascending memory locations with the low byte at an even byte address being followed by the high byte at the next odd byte address ("little endian"). Double words (code only) are stored in ascending memory locations as two subsequent words. Single bits are always stored in the specified bit position at a word address. Bit position 0 is the least significant bit of the byte at an even byte address, and bit position 15 is the most significant bit of the byte at the next odd byte address. Bit addressing is supported for a part of the Special Function Registers, a part of the internal RAM and for the General Purpose Registers.

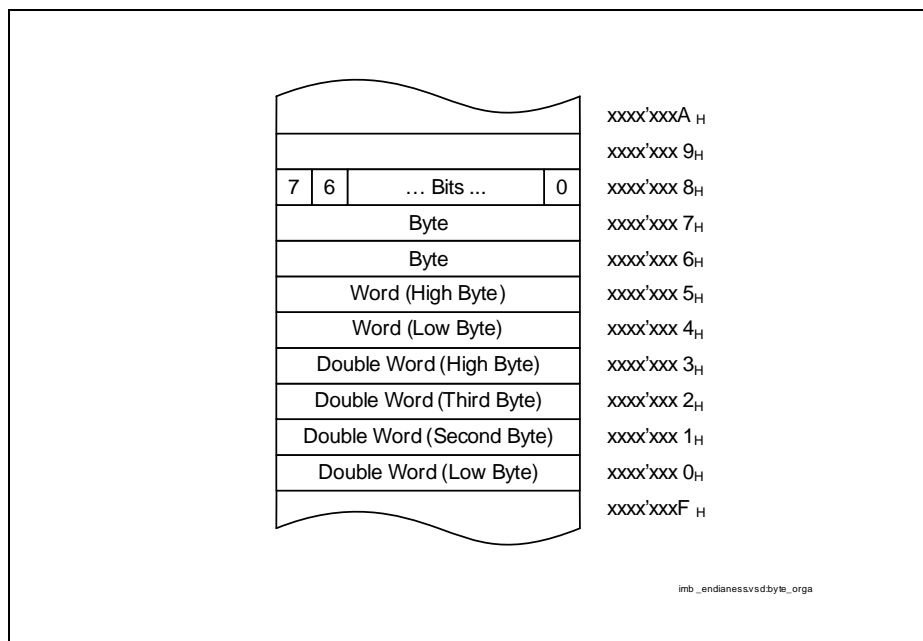


Figure 3-2 Storage of Words, Bytes and Bits in a Byte Organized Memory

Note: Byte units forming a single word or a double word must always be stored within the same physical (internal, external, ROM, RAM) and organizational (page, segment) memory area.

3.1 Address Mapping

All the various memory areas and peripheral registers (see [Table 3-1](#)) are mapped into one contiguous address space. All sections can be accessed in the same way. The memory map of the XC27x8X contains some reserved areas, so future derivatives can be enhanced in an upward-compatible fashion.

Table 3-1 XC27x8X Memory Map¹⁾

Address Area	Start Loc.	End Loc.	Area Size ²⁾	Notes
IMB register space	FF'FF00 _H	FF'FFFF _H	256 Bytes	
Reserved	F0'0000 _H	FF'FEFF _H	< 1 Mbyte	Minus IMB registers
Reserved for EPSRAM	E9'0000 _H	EF'FFFF _H	448 Kbytes	Mirrors EPSRAM
Emulated PSRAM	E8'0000 _H	E8'FFFF _H	64 Kbytes	With Flash timing
Reserved for PSRAM	E1'0000 _H	E7'FFFF _H	448 Kbytes	Mirrors PSRAM
PSRAM	E0'0000 _H	E0'FFFF _H	64 Kbytes	Program SRAM
Reserved for Flash	D1'0000 _H	DF'FFFF _H	960 Kbytes	
Flash 4	D0'0000 _H	D0'FFFF _H	64 Kbytes	
Flash 3	CC'0000 _H	CF'FFFF _H	256 Kbytes	
Flash 2	C8'0000 _H	CB'FFFF _H	256 Kbytes	
Flash 1	C4'0000 _H	C7'FFFF _H	256 Kbytes	
Flash 0	C0'0000 _H	C3'FFFF _H	256 Kbytes ³⁾	Minus res. seg.
Reserved	B0'0000 _H	BF'FFFF _H	1 Mbyte	
Reserved for PSRAM	A1'0000 _H	AF'FFFF _H	960 Kbytes	
PSRAM mirror	A0'0000 _H	A0'FFFF _H	64 Kbytes	Mapped to seg. E0 _H Only Program access supported ⁵⁾
Reserved for Flash	91'0000 _H	9F'FFFF _H	960 Kbytes	
Flash 4 cached	90'0000 _H	90'FFFF _H	64 Kbytes	Mapped to segments C0 _H - D0 _H ⁴⁾ Only Program access supported ⁵⁾
Flash 3 cached	8C'0000 _H	8F'FFFF _H	256 Kbytes	
Flash 2 cached	88'0000 _H	8B'FFFF _H	256 Kbytes	
Flash 1 cached	84'0000 _H	87'FFFF _H	256 Kbytes	
Flash 0 cached	80'0000 _H	83'FFFF _H	256 Kbytes ⁶⁾	
External memory area	40'0000 _H	7F'FFFF _H	4 Mbytes	
External IO area ⁷⁾	21'0000 _H	3F'FFFF _H	1,984 Kbytes	

Memory Organization

Table 3-1 XC27x8X Memory Map¹⁾ (cont'd)

Address Area	Start Loc.	End Loc.	Area Size ²⁾	Notes
Reserved	20'C000 _H	20'FFFF _H	16 Kbytes	
USIC0–3 alternate regs.	20'B000 _H	20'BFFF _H	4 Kbytes	Accessed via EBC
MultiCAN alternate regs.	20'8000 _H	20'AFFF _H	12 Kbytes	Accessed via EBC
Reserved	20'6800 _H	20'7FFF _H	6 Kbytes	
USIC0–4 registers	20'4000 _H	20'67FF _H	10 Kbytes	Accessed via EBC
MultiCAN registers	20'0000 _H	20'3FFF _H	16 Kbytes	Accessed via EBC
External memory area	01'0000 _H	1F'FFFF _H	1984 Kbytes	
SFR area	00'FE00 _H	00'FFFF _H	0.5 Kbytes	
Dualport RAM (DPRAM)	00'F600 _H	00'FDFE _H	2 Kbytes	
Reserved for DPRAM	00'F200 _H	00'F5FF _H	1 Kbytes	
ESFR area	00'F000 _H	00'F1FF _H	0.5 Kbytes	
XSFR area	00'E000 _H	00'EFFE _H	4 Kbytes	
Data SRAM (DSRAM)	00'8000 _H	00'DFFF _H	24 Kbytes	
External memory area	00'0000 _H	00'7FFF _H	32 Kbytes	

- 1) Accesses to the shaded areas are reserved. In devices with external bus interface these accesses generate external bus accesses.
- 2) The areas marked with "<" are slightly smaller than indicated, see column "Notes".
- 3) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use (C0'F000_H to C0'FFFF_H).
- 4) Data changes in the corresponding section (C0_H - D0_H) are not detected by the cache controller. User software should invalidate the cache to ensure data coherency.
- 5) Data read instructions are allowed and read random values. Data write instructions are allowed but have no effect to cache or memory.
- 6) The 4 KB sector from 80'F000_H to 80'FFFF_H is not accessible to the software.
- 7) Several pipeline optimizations are not active within the external IO area. This is necessary to control external peripherals properly.

*Note: **Table 3-1** shows the maximum available memory areas. The actual available memory areas depend on the selected device type.*

*Note: The double framed memory section in **Table 3-1** is provided to enable program execution from cached flash memory. The section has the same layout as the non-cached flash section (starting at C0'0000_H). This mapping shall simplify program relocation.*

3.2 Register Areas

The registers controlling the system and peripheral functions of the XC27x8X can be accessed through five address areas. The address areas differ in their access properties. Please refer to [Chapter 3.7](#) and the CPU chapter for further details.

The first three areas provide Special Function Registers (SFRs) access capabilities for controlling the system and peripheral functions of the XC27x8X:

- 512-byte SFR area (located above the DPRAM: 00'FFFF_H ... 00'FE00_H).
- 512-byte ESFR area (located below the DPRAM: 00'F1FF_H ... 00'F000_H).
- 4-Kbyte XSFR area (located below the ESFR area: 00'EFFF_H ... 00'E000_H).

The USIC and MultiCAN registers are located within the external IO area:

- 64-Kbyte external IO area (located in: 20'0000_H ... 20'FFFF_H).

The IMB registers are located within a regular memory area. CPU pipeline effects must be regarded for access in this area:

- 256-byte IMB registers area (located in: FF'FF00_H ... FF'FFFF_H).

This arrangement provides upward compatibility with the derivatives of the C166 and XC166 families.

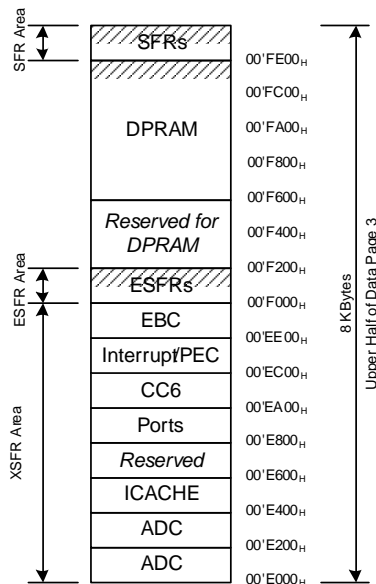
IMB Registers not in IO Area

Important to note is that IMB registers are not located within the IO area. Only in IO areas the CPU takes care that data accesses are executed exactly in the sequence of their appearance in the instruction stream. Outside of the IO areas the CPU ensures only that accesses to single addresses maintain their sequence. So special care must be taken when accessing the IMB register range. Two examples will help to understand this important issue:

1. Sequence: write to address A; read from address B.
2. Sequence: write to address C; read from address C.

If addresses A, B and C are located in IO areas then the sequence of memory accesses would resemble their sequence in the code.

If addresses A, B and C are located outside of IO areas, then pipeline effects could cause the read from address B in sequence 1 to be performed before the write to address A happens. The CPU will itself ensure that sequence 2 is executed in order. To work around this issue and to enforce sequence order, a read from address A or a write to address B should be performed after the write to address A — both ensure that the read from address B occurs after the write from address A.



regareas.vsd

Figure 3-3 Special Function Register Mapping

Note: The upper 256 bytes of SFR area, ESFR area, and internal RAM are bit-addressable (see hatched blocks in [Figure 3-3](#)).

Special Function Registers

The functions of the CPU, the bus interface, the IO ports, and the on-chip peripherals of the XC27x8X are controlled via a number of Special Function Registers (SFRs).

All Special Function Registers can be addressed via indirect and long 16-bit addressing modes. The (word) SFRs and their respective low bytes in the SFR/ESFR areas can be addressed using an 8-bit offset together with an implicit base address. However, this **does not work** for the respective high bytes!

Note: Writing to any byte of an SFR causes the not addressed complementary byte to be cleared.

The upper half of the SFR-area (00'FFFF_H ... 00'FF00_H) and the ESFR-area (00'F1FF_H ... 00'F100_H) is bit-addressable, so the respective control/status bits can be modified directly or checked using bit addressing.

Memory Organization

When accessing registers in the ESFR area using 8-bit addresses or direct bit addressing, an Extend Register (EXTR) instruction is required beforehand to switch the short addressing mechanism from the standard SFR area to the Extended SFR area. This is not required for 16-bit and indirect addresses. The GPRs R15 ... R0 are duplicated, i.e. they are accessible within both register blocks via short 2-, 4-, or 8-bit addresses without switching.

ESFR_SWITCH_EXAMPLE:

```
EXTR  #4                      ;Switch to ESFR area for next 4 instr.
MOV   STMREL, #data16         ;STMREL uses 8-bit reg addressing
BFLDL STMCON, #mask, #data8 ;Bit addressing for bitfields
BSET  WUCR.CLRTG              ;Bit addressing for single bits
MOV   T8REL, R1               ;T8REL uses 16-bit mem address,
                               ;R1 is duplicated into the ESFR space
                               ;(EXTR is not required for this access)
;---- ;-----               ;The scope of the EXTR #4 instruction ...
                               ;... ends here!
MOV   T8REL, R1               ;T8REL uses 16-bit mem address,
                               ;R1 is accessed via the SFR space
```

In order to minimize the use of the EXTR instructions the ESFR area mostly holds registers which are mainly required for initialization and mode selection. Registers that need to be accessed frequently are allocated to the standard SFR area, wherever possible.

Note: The tools are equipped to monitor accesses to the ESFR area and will automatically insert EXTR instructions, or issue a warning in case of missing or excessive EXTR instructions.

Accesses to registers in the XSFR area use 16-bit addresses and require no specific addressing modes or precautions.

General Purpose Registers

The General Purpose Registers (GPRs) use a block of 16 consecutive words either within the global register bank or within one of the two local register banks. The bit-field BANK in register PSW selects the currently active register bank. The global register bank is mirrored to a section in the DPRAM, the Context Pointer (CP) register determines the base address of the currently active global register bank section. This register bank may consist of up to 16 Word-GPRs (R0, R1, ... R15) and/or of up to 16 byte-GPRs (RL0, RH0, ... RL7, RH7). The sixteen byte-GPRs are mapped onto the first eight Word GPRs (see [Table 3-2](#)).

In contrast to the system stack, a register bank grows from lower towards higher address locations and occupies a maximum space of 32 bytes. The GPRs are accessed via short 2-, 4-, or 8-bit addressing modes using the Context Pointer (CP) register as base

Memory Organization

address for the global bank (independent of the current DPP register contents). Additionally, each bit in the currently active register bank can be accessed individually.

Table 3-2 Mapping of General Purpose Registers to DPRAM Addresses

DPRAM Address	High Byte Registers	Low Byte Registers	Word Registers
<CP> + 1E _H	–	–	R15
<CP> + 1C _H	–	–	R14
<CP> + 1A _H	–	–	R13
<CP> + 18 _H	–	–	R12
<CP> + 16 _H	–	–	R11
<CP> + 14 _H	–	–	R10
<CP> + 12 _H	–	–	R9
<CP> + 10 _H	–	–	R8
<CP> + 0E _H	RH7	RL7	R7
<CP> + 0C _H	RH6	RL6	R6
<CP> + 0A _H	RH5	RL5	R5
<CP> + 08 _H	RH4	RL4	R4
<CP> + 06 _H	RH3	RL3	R3
<CP> + 04 _H	RH2	RL2	R2
<CP> + 02 _H	RH1	RL1	R1
<CP> + 00 _H	RH0	RL0	R0

The XC27x8X supports fast register bank (context) switching. Multiple global register banks can physically exist within the DPRAM at the same time. Only the global register bank selected by the Context Pointer register (CP) is active at a given time, however. Selecting a new active global register bank is simply done by updating the CP register. A particular Switch Context (SCXT) instruction performs register bank switching by automatically saving the previous context and loading the new context. The number of implemented register banks (arbitrary sizes) is limited only by the size of the available DPRAM.

Note: The local GPR banks are not memory mapped and the GPRs cannot be accessed using a long or indirect memory address.

PEC Source and Destination Pointers

The source and destination address pointers for data transfers on the PEC channels are located in the XSFR area.

Memory Organization

Each channel uses a pair of pointers stored in two subsequent word locations with the source pointer (SRCPx) on the lower and the destination pointer (DSTPx) on the higher word address ($x = 15 \dots 0$). An additional segment register stores the associated source and destination segments, so PEC transfers can move data from/to any location within the complete addressing range.

Whenever a PEC data transfer is performed, the pair of source and destination pointers (selected by the specified PEC channel number) accesses the locations referred to by these pointers independently of the current DPP register contents.

If a PEC channel is not used, the corresponding pointer locations can be used for other purposes.

Note: Writing to any byte of the PEC pointers causes the not addressed complementary byte to be cleared.

3.3 Data Memory Areas

The XC27x8X provides two on-chip RAM areas exclusively for data storage:

- The **Dual Port RAM (DPRAM)** can be used for global register banks (GPRs), system stack, storage of variables and other data, in particular for MAC operands.
- The **Data SRAM (DSRAM)** can be used for system stack (recommended), storage of variables and other data.

Note: Data can also be stored in the PSRAM (see [Section 3.12](#)). However, both data memory areas provide the fastest access.

Depending on the device additional on-chip memory areas may exist with the special purpose to retain data while the system power domain is switched off. The XC27x8X contains:

- The **Standby RAM (SBRAM)**.
- The **Marker Memory (MKMEM)**.

Dual-Port RAM (DPRAM)

The XC27x8X provides 2 Kbytes of DPRAM (00'F600_H ... 00'FDFF_H). Any word or byte data in the DPRAM can be accessed via indirect or long 16-bit addressing modes, if the selected DPP register points to data page 3. Any word data access is made on an even byte address.

For PEC data transfers, the DPRAM can be accessed independent of the contents of the DPP registers via the PEC source and destination pointers.

The upper 256 bytes of the DPRAM (00'FD00_H through 00'FDFF_H) are provided for single bit storage, and thus they are bit addressable.

Note: Code cannot be executed out of the DPRAM.

Note: The locations 00'FBFE_H ... 00'FC01_H of the DPRAM may be altered during the initialization phase after a reset. This area, therefore, should not store data to be preserved beyond a reset.

An area of 3 Kbytes is dedicated to DPRAM (00'F200_H ... 00'FDFF_H). The locations without implemented DPRAM are reserved.

Data SRAM (DSRAM)

The XC27x8X provides 24 Kbytes of DSRAM (00'8000_H ... 00'DFFF_H). Any word or byte data in the DSRAM can be accessed via indirect or long 16-bit addressing modes, if the selected DPP register points to data page 3 (for the range 00'C000_H ... 00'DFFF_H) or to data page 2 (for the range 00'8000_H ... 00'BFFF_H). Any word data access is made on an even byte address.

For PEC data transfers, the DSRAM can be accessed independent of the contents of the DPP registers via the PEC source and destination pointers.

Note: Code cannot be executed out of the DSRAM.

An area of 24 Kbytes is dedicated to DSRAM (00'8000_H ... 00'DFFF_H). The locations without implemented DSRAM are reserved.

Standby RAM (SBRAM)

The SBRAM provides 8 Kbyte of memory supplied by the wake-up power domain (DMP_M). Its main purpose is to retain state while the system power domain (DMP_1) is switched off.

Unlike the other memories the SBRAM is not mapped into the address range of the processor. Reading and writing is done via two address and two data SFRs. Details of the access mechanism are described in [Section 3.13](#).

Note: Code cannot be executed out of the SBRAM.

Note: The upper 32 Bytes of the SBRAM may be altered during the initialization phase after a power reset. This area, therefore, should not store data to be preserved beyond a power reset. If Fast Startup Mode is used, this area must not be altered by the application software.

Marker Memory (MKMEM)

The MKMEM provides 4 bytes of memory. It can be used to store system state information during power down.

The MKMEM consists of 2 16-bit SFRs that are accessible as all other SFRs. Details are described in the SCU chapter.

Note: Code cannot be executed out of the MKMEM.

3.4 Program Memory Areas

The XC27x8X provides two on-chip program memory areas for code/data storage:

- The **Program Flash/ROM** stores code and constant data. Flash memory is (re-) programmed by the application software or flash loaders, ROM is mask-programmed in the factory.
- The **Program SRAM (PSRAM)** stores temporary code sequences and other data. For example higher level boot loader software can be written to the PSRAM and then be executed to program the on-chip Flash memory.

Both areas are mirrored to a “cached” memory area thus enabling easy migration of existing programs.

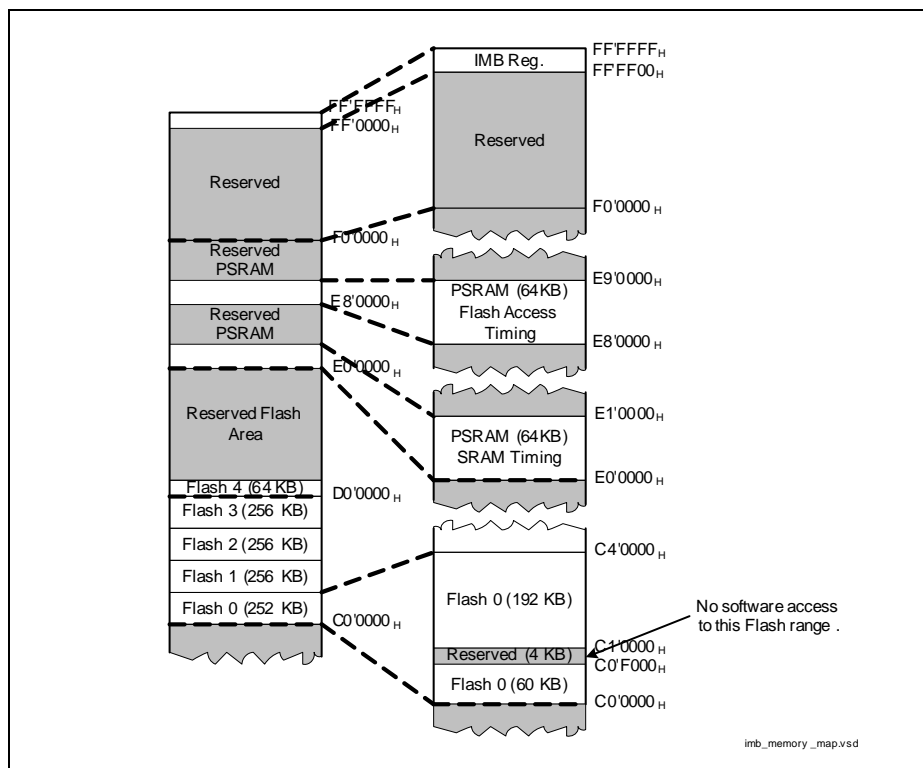


Figure 3-4 On-Chip Program Memory Mapping

3.4.1 Program/Data SRAM (PSRAM)

The XC27x8X provides up to 64 Kbytes of PSRAM (E0'0000_H ... E0'FFFF_H). The PSRAM provides fast code execution without initial delays. Therefore, it supports non-sequential code execution, for example via the interrupt vector table.

Any word or byte data in the PSRAM can be accessed via indirect or long 16-bit addressing modes, if the selected DPP register points to one of its data pages. Any word data access is made on an even byte address.

For PEC data transfers, the PSRAM can be accessed independent of the contents of the DPP registers via the PEC source and destination pointers.

Any data can be stored in the PSRAM. Because the PSRAM is optimized for code fetches, however, data accesses to the data memories provide higher performance.

Note: The PSRAM is not bit-addressable.

Note: The upper 256 Bytes of the PSRAM may be altered during the initialization phase after a reset. This area, therefore, should not store data to be preserved beyond a reset.

Also, during bootstrap loader operation, the serially received data is stored in the PSRAM starting at location E0'0000_H.

An area of 512 Kbytes is dedicated to PSRAM (E0'0000_H ... F7'FFFF_H). The locations without implemented PSRAM are reserved.

Flash Emulation

During code development the PSRAM will often be used for storing code or data that the production chip will later contain in the flash memory. In order to ensure similar execution time the PSRAM supports a second access path in the range E8'0000_H ... EF'FFFF_H with timing parameters that correspond to Flash timing. The number of wait-cycles is determined by the flash access timing configuration (see [IMB_IMBCTRL.WSFLASH](#) and [IMB_IMBCTRL.WSFLE](#)). Writes are always performed without wait-cycles.

This flash access timing imitation is nearly cycle accurate because the same read logic as for reading the flash memory is used¹⁾. Discrepancies might occur if the software uses the PSRAM for flash emulation and directly as PSRAM. During emulation access conflicts can cause a slightly different timing as in the product chip where these conflicts do not occur.

Another source of timing differences can be access conflicts at the flash modules in the product chip. Data reads and instruction fetches that target different flash modules can be executed concurrently whereas if they target the same flash module they are

1) The dual use of the flash read logic might cause unexpected behavior: while the IMB Core is busy with updating the protection configuration (after startup or after changing the security pages) read accesses to the flash emulation range of the PSRAM are blocked because Flash data reads would be blocked also.

executed sequentially with the data access as first. In the flash emulation this type of conflict can not occur. The data and the instruction access will both incur the defined number of wait-cycles (as if they would target different flash modules) and if they collide at the PSRAM interface the instruction fetch will see an additional wait-cycle.

Data Integrity

The PSRAM contains its own error control which can be switched between ECC and parity. Details are described in the SCU chapter.

Write Protection

As the PSRAM is often used to store timing critical code or constant data it is supplied with a write protection. After storing critical data in the PSRAM the register field **IMB_IMBCTRH.PSPROT** can be used to split the PSRAM into a read-only and a writable part. Write accesses to the read-only part are blocked and a trap can be activated.

3.4.2 Non-Volatile Program Memory (Flash)

The XC27x8X provides up to up to 1,088 Kbytes of program Flash starting at address C0'0000_H. Code and data fetches are always 64-bit aligned, using byte select lines for word and byte data.

Any word or byte data in the program memory can be accessed via indirect or long 16-bit addressing modes, if the selected DPP register points to one of the respective data pages. Any word data access is made on an even byte address.

For PEC data transfers, the program memory can be accessed independent of the contents of the DPP registers via the PEC source and destination pointers.

Note: The program memory is not bit-addressable.

An area of 2 Mbytes is dedicated to program memory (C0'0000_H ... DF'FFFF_H). The locations without implemented program memory are reserved.

A more detailed description can be found in **“Embedded Flash Memory” on Page 3-20**.

3.4.3 Using the Instruction Cache

The native PSRAM and Flash memory areas located between C0'0000_H and DF'FFFF_H. In the XC27x8X the area has been mirrored to the “cached” memory area starting at 80'0000_H. Due to the identical memory layout within the area, existing programs can be easily remapped to the cached memory area.

Please refer to chapter **“Instruction Cache” on Page 6-1** for details.

3.5 System Stack

The system stack may be defined anywhere within the XC27x8X's memory areas (including external memory).

For all system stack operations the respective stack memory is accessed via a 24-bit stack pointer. The Stack Pointer (SP) register provides the lower 16 bits of the stack pointer (stack pointer offset), the Stack Pointer Segment (SPSEG) register adds the upper 8 bits of the stack pointer (stack segment). The system stack grows downward from higher towards lower locations as it is filled. Only word accesses are supported to the system stack.

Register SP is decremented before data is pushed on the system stack, and incremented after data has been pulled from the system stack. Only word accesses are supported to the system stack.

By using register SP for stack operations, the size of the system stack is limited to 64 KBytes. The stack must be located in the segment defined by register SPSEG.

The stack pointer points to the latest system stack entry, rather than to the next available system stack address.

A stack overflow (STKOV) register and a stack underflow (STKUN) register are provided to control the lower and upper limits of the selected stack area. These two stack boundary registers can be used both for protection against data corruption.

For best performance it is recommended to locate the stack to the DPRAM or to the DSRAM. Using the DPRAM may conflict with register banks or MAC operands.

3.6 Protected Bits

The XC27x8X provides a special mechanism to protect bits which can be modified by the on-chip hardware from being changed unintentionally by software accesses to related bits (refer also to section “Bit Manipulation Unit” in the CPU chapter). The “rwh” and “wh” bits and bifields of the following registers support bit protection:

Table 3-3 XC27x8X Protected Bits

Register	Component(s)	Notes
TFR	CPU	Trap Flag Register
PSW	CPU	Processor Status Word
PECISNC	CPU	PEC channel interrupt request flags
MPU_PRA	MPU	Protection Range Address
SCU_GSCSWREQ	SCU	Global State Control Software Request
RTC_ISNC	RTC	Interrupt node sharing request flags
CC2_OUT	CC2	Compare output bits
GPT12E_T2CON	GPT	GPT1 timer T2 flags
GPT12E_T3CON	GPT	GPT1 timer T3 flags and output toggle latch
GPT12E_T4CON	GPT	GPT1 timer T4 flags
GPT12E_T6CON	GPT	GPT2 timer T6 output toggle latch
xC	CPU, SCU and Peripheral units	All interrupt control registers. A complete list is given in the interrupt and exception control chapter
Px_OUT	Ports	All port output registers

3.7 IO Areas

The following areas of the XC27x8X's address space are marked as IO area:

- The **external IO area** is provided for external peripherals (or memories) and also comprises the on-chip LxBus-peripherals, such as the MultiCAN or USIC modules. It is located from 20'0000_H to 3F'FFFF_H (2 Mbytes).
- The **internal IO area** provides access to the internal peripherals and is split into three blocks:
 - The SFR area, located from 00'FE00_H to 00'FFFF_H (512 bytes).
 - The ESFR area, located from 00'F000_H to 00'F1FF_H (512 bytes).
 - The XSFR area, located from 00'E000_H to 00'EFFF_H (4 Kbytes).

Note: The external IO area supports real byte accesses. The internal IO area does not support real byte transfers, the complementary byte is cleared when writing to a byte location.

The IO areas have special properties, because peripheral modules must be controlled in a different way than memories:

- Accesses are not buffered and cached, the write back buffers and caches are not used to store IO read and write accesses.
- Speculative reads are not executed, but delayed until all speculations are solved (e.g. pre-fetching after conditional branches).
- Data forwarding is disabled, an IO read access is delayed until all IO writes pending in the pipeline are executed, because peripherals can change their internal state after a write access.

3.8 External Memory Space

The XC27x8X is capable of using an address space of up to 16 Mbytes. Only parts of this address space are occupied by internal memory areas or are reserved. A total area of approximately 8 Mbytes references external memory locations. This external memory is accessed via the XC27x8X's external bus interface.

Selectable memory bank sizes are supported: The maximum size of a bank in the external memory space depends on the number of activated address bits. It can vary from 64 Kbytes (with A15 ... A0 activated) to 8 Mbytes (with A22 ... A0 activated). The logical size of a memory bank and its location in the address space is defined by programming the respective address window. It can vary from 4 Kbytes to 8 Mbytes.

Each bank can be directly addressed via the address bus, while the programmable chip select signals can be used to select various memory banks.

The XC27x8X also supports **four different bus types**:

- Multiplexed 16-bit Bus (default after Reset).
- Multiplexed 8-bit Bus.
- Demultiplexed 16-bit Bus.
- Demultiplexed 8-bit Bus.

For further details about the external bus configuration and control refer to the External Bus Controller chapter.

External word and byte data can only be accessed via indirect or long 16-bit addressing modes using one of the four DPP registers. There is no short addressing mode for external operands. Any word data access is made to an even byte address.

For PEC data transfers the external memory can be accessed independent of the contents of the DPP registers via the PEC source and destination pointers.

Note: The external memory is not bit addressable.

3.9 Reserved Memory Areas

The memory map contains reserved memory areas where no memories nor registers are currently mapped to. Generally, such memory areas must never be accessed by the user program. Otherwise, the following behavior occurs when accessing unprotected reserved memory areas:

- In case of a read access, random data is returned;
- In case of a write access, the behavior is undefined. The reserved memory areas may be mirrored to existing memories. Therefore, one consequence may be that the other data is overwritten.

Reserved memory areas may be protected against access by using the MPU. Access protection mechanisms are also implemented for reserved Flash or PSRAM sections. If an access protection is detected, a trap is executed.

3.10 Crossing Memory Boundaries

The address space of the XC27x8X is implicitly divided into equally sized blocks of different granularity and into logical memory areas. Crossing the boundaries between these blocks (code or data) or areas requires special attention to ensure that the controller executes the desired operations.

Memory Areas are partitions of the address space assigned to different kinds of memory (if provided at all). These memory areas are the SFR areas, the on-chip program or data RAM areas, the on-chip ROM/Flash (if available), the on-chip LxBus-peripherals (if integrated), and the external memory.

Accessing subsequent data locations which belong to different memory areas is no problem. However, when executing code, the different memory areas must be switched explicitly via branch instructions. Sequential boundary crossing is not supported and leads to erroneous results.

Note: Changing from the external memory area to the on-chip RAM area takes place within segment 0.

Segments are contiguous blocks of 64 Kbytes each. They are referenced via the Code Segment Pointer CSP for code fetches and via an explicit segment number for data accesses overriding the standard DPP scheme.

During code fetching, segments are not changed automatically, but rather must be switched explicitly. The instructions JMPS, CALLS and RETS will do this.

Data Pages are contiguous blocks of 16 Kbytes each. They are referenced via the data page pointers DPP3 ... DPP0 and via an explicit data page number for data accesses overriding the standard DPP scheme. Each DPP register can select one of the possible 1024 data pages. The DPP register which is used for the current access is selected via the two upper bits of the 16-bit data address. Therefore, subsequent 16-bit data addresses which cross the 16-Kbytes data page boundaries will use different data page pointers, while the physical locations need not be subsequent within memory.

3.11 Embedded Flash Memory

This chapter describes the embedded flash memory of the XC27x8X:

- **Section 3.11.1** defines the flash specific nomenclature and the structure of the flash memory.
- **Section 3.11.2** describes the operating modes.
- **Section 3.11.3** contains all operations.
- **Section 3.11.4** gives the details of operating sequences.
- The three sections **Section 3.11.7**, **Section 3.11.8** and **Section 3.11.9** look more into depth of maintaining data integrity and protection issues.
- **Section 3.11.10** discusses Flash EEPROM emulation.
- **Section 3.11.11** describes interrupt generation by the flash memory.

The **Chapter 3.12** describes how the flash memory is embedded into the memory architecture of the XC27x8X and lists all SFRs that affect its behavior.

3.11.1 Definitions

This section defines the nomenclature and some abbreviations as a base for the rest of the document. The used flash memory is a non-volatile memory ("**NVM**") based on a floating gate one-transistor cell. It is called "non-volatile" because the memory content is kept when the memory power supply is shut off.

Logical and Physical States

Flash memory content can not be changed directly as in SRAMs. Changing data is a complicated process with a typically much longer duration than reading.

- **Erasing:** The erased state of a cell is logical 0. Forcing an flash cell to this state is called "erasing". Erasing is possible with a minimum granularity of one page (see below). A device is delivered with completely erased flash memory.
- **Programming:** The programmed state of a cell is logical 1. Changing an erased cell to this state is called "programming". A page must only be programmed once and has to be erased before it can be programmed again.

The above listed processes have certain limitations:

- **Retention:** This is the time during which the data of a flash cell can be read reliably. The retention time is a statistical figure that depends on the operating conditions of the flash array (temperature profile) and the accesses to the flash array. With an increasing number of program/erase cycles (see endurance) the retention is lowered. Drain and gate disturbs decrease data retention as well.
- **Endurance:** As described above the data retention is reduced with an increasing number of program/erase cycles. A flash cell incurs one cycle whenever its page or sector is erased. This number is called "endurance". As said for the retention it is a statistical figure that depends on operating conditions and the use of the flash cells and not to forget on the required quality level.

Memory Organization

- **Drain Disturb:** Because of using a so called “one-transistor” flash cell each program access disturbs all pages of the same sector slightly. Over long these “drain disturbs” make 0 and 1 values indistinguishable and thus provoke read errors. This effect is again interrelated with the retention. A cell that incurred a high number of drain disturbs will have a lower retention. The physical sectors of the flash array are isolated from each other. So pages of a different sector do not incur a drain disturb. This effect must be therefor considered when the page erase feature is used.

The durations of programming and erasing as well as the limits for endurance, retention and drain disturbs are documented in the data sheet.

Attention: *No means exist in the device that prevent the application from violating these limitation.*

Array Structure

The flash memory is hierarchically structured:

- **Block:** A block consists of 128 user data bits (i.e. 16 bytes) and 9 ECC bits. One read access delivers one block.
- **Page:** A page consists of 8 blocks (i.e. 128 bytes). Programming changes always complete pages.
- **Sector:** A sector consists of 32 pages (i.e. 4096 bytes). The pages of one sector are affected by drain disturb as described above. The pages of different sectors are isolated from each other.
- **Array:** Each 256 KB array has 64 sectors¹⁾, a 128 KB array has 32, a 64 KB array has 16 and a 32 KB array has 8 sectors. Usually when referring to an “array” this contains as well all accompanying logic as assembly buffer, high voltage logic and the digital logic that allows to operate them in parallel.
- **Memory:** The complete flash memory of the XC27x8X consists of 5 flash array(s).

This structure of the 256 KB array is visualized in [Figure 3-5](#). The structure of the 64 KB array is analog.

1) If the Flash0 is a 256 KB array one sector is reserved for device internal purposes. It is not accessible by software, thus only 63 are usable.

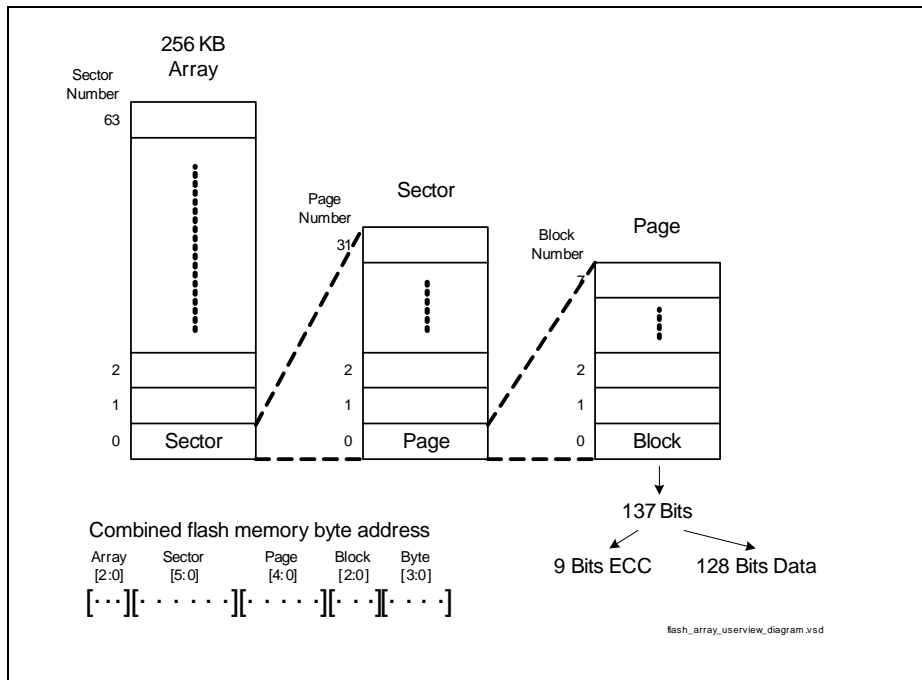


Figure 3-5 Flash Structure

3.11.2 Operating Modes

The IMB and the flash memory and each flash module have certain modes of operation. Some modes define clocking and power supply and the operating state of the analog logic as oscillators and voltage pumps. Overall system modes (e.g. startup mode) influence the behavior of the flash memory as well.

Other modes define the functional behavior. These will be discussed here.

3.11.2.1 Standard Read Mode

After reset and after performing a clean startup the flash memory with all its modules is in "standard read mode". In this mode it behaves as an on-chip ROM. This mode is entered:

- After reset when the complete start-up has been performed.
- After completion of a longer lasting command like "erase" or "program" which is acknowledged by clearing the "busy" flag.
- Immediately after each other command execution.

Memory Organization

- In case of detecting an execution error like attempting to write to a write protected range, sending a wrong password, after all sequence errors.

For the long lasting commands the read mode stays active until the last command of the sequence is received and the operation is started.

3.11.2.2 Command Mode

After receiving the last command of a command sequence the addressed flash module (not the whole flash memory!) is placed into command mode. For most commands this will not be noticed by the user as the command executes immediately and afterwards the flash module is placed again into read mode. For the long lasting commands the flash module stays in command mode for several milliseconds. This is reported by setting the corresponding “busy” flag. The data of a busy flash module cannot be read but other not busy flash modules stay readable. New command sequences are generally not accepted and cause a sequence error until the running operation has finished. In certain cases however new command sequences are accepted in order to enable concurrent programming and erase of independent flash modules.

Read accesses to busy flash modules stall the CPU until the read mode is entered again. A stalled CPU responds only to the reset. As no interrupts can be handled this state must be avoided. Nevertheless this feature can be used to execute code from a flash module that erases or programs data in the same flash module.

Note: Because command sequences to busy flash memory are not always rejected by the hardware with a sequence error it is necessary to handle all commands more careful than in previous device generations that didn't support concurrent processes. A new command sequence shall be only be issued to a flash module after checking that it is not busy anymore. This is especially vital when using the “stall CPU when reading busy flash” feature. Further advice can be found in [Section 3.11.5](#) (sequence errors) and [Section 3.11.6](#) (concurrent processes).

3.11.2.3 Page Mode

The page mode is entered with the “[Enter Page Mode](#)” command. Please find its description below. A flash module that is in page mode can still be read (so it is concurrently in “read mode”). At a time only one flash module can be in page mode.

When the flash memory is in page mode — i.e. one of the flash modules is in page mode — some command sequences are not allowed. These are all erase sequences and the “change read margin” sequence. These are ignored and a sequence error is reported.

3.11.3 Operations

The flash memory supports the following operations:

- Instruction fetch.
- Data read.
- Command sequences to change data and control the protection.

3.11.3.1 Instruction Fetch from Flash Memory

Instructions are fetched by the PMU in groups of aligned 64 bits. These code requests are forwarded to the flash memory. It needs a varying number of cycles (depending on the system clock frequency) to perform the read access. The number of cycles must be known to the IMB Core because the flash does not signal data availability. The number of wait states is therefore stored in the **IMB_IMBCTRL** register. Additionally the selected flash read timing (see **IMB_IMBCTRLH.WSFLE**) is taken into account.

The complete duration of a flash read access is: $\text{IMB_IMBCTRL.WSFLASH} + 2 * \text{IMB_IMBCTRLH.WSFLE} + 1$ cycles.

Consult the data sheet for correct values of WSFLASH and WSFLE dependent on the system clock frequency and device.

One read access to the flash memory delivers 128 data bits and a 9-bit ECC value. The ECC value is used to detect and possibly correct errors. The addressed 64-bit part of the 128-bit chunk is sent to the PMU. The complete 128 data bits and the 9 ECC bits are stored in the IMB Core with their address. If a succeeding fetch request matches this address the data is delivered from the buffer without performing a read access in the flash memory. The delivery from the buffer happens after one cycle. The flash read wait-cycles are not waited.

The stored data are a kind of instruction cache. In order to support self-modifying code (e.g. boot loaders) this cache is invalidated when the corresponding address is written (i.e. erased or programmed).

In addition to this fetch buffer the IMB Core has an additional performance increasing feature — the Linear Code Pre-Fetch. When this feature is enabled with **IMB_IMBCTRL.DLCPF** = 0 the IMB Core fetches autonomously the following instructions while the CPU executes from its own buffers or the fetch buffer. As this feature is fetching only the linear successors (it does not analyze the code stream) it is most effective for code with longer linear sequences. For code with a high density of jumps and calls it can even cause a reduction of performance and should be switched off.

3.11.3.2 Data Reads from Flash Memory

Data reads are issued by the DMU. Data is always requested in 16-bit words. The flash memory delivers for every read request 128 bits plus ECC as described in **[“Instruction Fetch from Flash Memory” on Page 3-24](#)**.

The IMB Core has to get all 128 bits to evaluate the ECC data. The requested 16 bits will be delivered to the DMU. All data and ECC bits are kept in the data register and their address is kept in the address register. For all following data reads the address is compared with the address register and in case of a match the data is delivered after one cycle from the data register. Every data read that is not delivered from this cache invalidates the cache content. When the requested data arrives the cache contains again valid data.

This small data cache is invalidated when a write (i.e. erase or program) access to this address happens.

For data reads the IMB Core does not perform any autonomous pre-fetching.

3.11.3.3 Data Writes to Flash Memory

Flash memory content can not be changed by directly writing data to this memory. Command sequences are used to execute all other operations in the flash except reading. Command sequences consist of data writes with certain data to the flash memory address range. All data moves targeting this range are interpreted as command sequences. If they do not match a defined one or if the IMB Core cannot accept a new one because it is busy a sequence error is reported.

3.11.3.4 Command Sequences

As described before changing data in the flash memory is performed with command sequences.

Table 3-4 Command Sequence Overview

Command Sequence	Description	Details on Page
Reset to Read	Reset Flash into read mode and clear error flags.	Page 3-28
Clear Status	Clear error and status flags.	Page 3-28
Change Read Margin	Change read margins.	Page 3-29
Change Read Timing	Change read timing.	Page 3-29
Enter Page Mode	Prepare page for programming.	Page 3-30
Enter Security Page Mode	Prepare security page for programming.	Page 3-31
Load Page Word	Load page with data.	Page 3-31
Program Page	Start page programming process.	Page 3-32
Erase Sector	Start sector erase process.	Page 3-33
Erase Page	Start page erase process.	Page 3-34
Erase Security Page	Start security page erase process.	Page 3-35
Disable Read Protection	Disable temporarily read protection with password.	Page 3-36
Disable Write Protection	Disable temporarily write protection with password.	Page 3-37
Re-Enable Read/Write Protection	Re-enable protection.	Page 3-37

3.11.4 Details of Command Sequences

The description defines the command sequence with pseudo assembler code. It is “pseudo” because all addresses are direct addresses which is generally not possible in real assembler code.

The commands are called by a sequence of one to six data moves into the flash memory range. The data moves must be of the “word” type, i.e. not byte move instructions. The following sections describe each command. The following abbreviations for addresses and data will be used:

- PA: “Page Address”. This is the base address of the destination page. For example the very first page has the address $C0'0000_H$. The page 13 of the second array has the $PA = C0'0000_H + 1 \cdot 256 \cdot 1024$ (for the array) $+ 0 \cdot 4 \cdot 1024$ (for the sector) $+ 13 \cdot 128$ (for the page) $= C4'0680_H$.
- SECPA: “Security Page Address”. This is the virtual address of a security page. It is “virtual” because SECPA is just used as argument of the command sequence to identify the security page but the physical storage of the security page is hidden. Two security pages are defined:
 SecP0: address $C0'0000_H$.
 SecP1: address $C0'0080_H$.
- WD: “Write Data”. This is a 16-bit data word that is written into the assembly buffer.
- SA: “Sector Address”. This is the physical sector number as defined in [Figure 3-6](#) based on the address of the flash module. Two examples as clarification:
 1. Physical sector number 16 of the first array that is based on $C0'0000_H$ is addressed with $SA = C0'0000_H + 16 \cdot 4 \cdot 1024 = C1'0000_H$.
 2. The second 256 KB array has the base address $C4'0000_H$ (as shown in [Table 3-1](#)). So its physical sector number 3 has the $SA = C4'0000_H + 3 \cdot 4 \cdot 1024 = C4'3000_H$.
- PWD: “Password”. This is a 64-bit password. It is transferred in 4 16-bit data words $PWD0 = PWD[15:0]$, $PWD1 = PWD[31:16]$, $PWD2 = PWD[47:32]$ and $PWD3 = PWD[63:48]$.
- Address XX followed by two hexadecimal digits, for example “XXAA_H”. If the command targets a certain flash module the XX must be translated to its base address. So “XXAA_H” means $C0'00AA_H$ for all commands addressing flash 0, $C4'00AA_H$ for flash 1 and $C8'00AA_H$ for flash 2. If a command (e.g. “Clear Status”) addresses the complete flash memory the base address of flash module 0 must be used.
- Data XX followed by two hexadecimal digits, e.g. XXA5_H. This is a “don’t care” data word where only the low byte must match a certain pattern. So in this example all data words like 12A5_H or 79A5_H can be used.
- MR: “Margin”. This 8-bit number defines the read margin. MR can take the values 00_H (normal read), 01_H (hard read 0), 02_H (alternate hard read 0), 05_H (hard read 1), 06_H (alternate hard read 1). All other values of MR are reserved.

Memory Organization

- RT: "Read Timing". This 2-bit number selects the Flash read timing as described in **IMB_IMBCTRH.WSFLE**. The data sheet defines which setting is necessary depending on device and system clock frequency. RT can take the values 00_H corresponding to WSFLE = 0 (5 cycle timing), 01_H corresponding to WSFLE = 1 (7 cycle timing) and 02_H corresponding to WSFLE = 2 (9 cycle timing). All other values of RT are reserved.

Reset to Read

Arguments: –

Definition:

MOV XXAA_H, XXF0_H

Timing: One cycle command that does not set any "BUSY" flags. But note that an immediately following write access to the IMB Core is stalled for a few clock cycles during which the IMB Core is busy with aborting a previous command.

Description: The internal command state machine is reset to initial state and returns to read mode. An already started programming or erase operation is not affected and will be continued (the "Reset to Read" command — i.e. all commands — will anyhow not be accepted while the IMB Core is busy).

The "Reset to Read" command is a single cycle command. It can be used during a command sequence to reset the command interpreter and return the IMB Core into its initial state. It clears also all error flags in the Flash Status Register IMB_FSR and an active page mode is aborted. "Reset to Read" can not be used to abort an active command mode. When at least one flash module is busy this command is rejected with SQER¹⁾.

This command clears: PROER, PAGE, SQER, OPER, ISBER, IDBER, DSBER, DDBER.

Clear Status

Arguments: –

Definition:

MOV XXAA_H, XXF5_H

Timing: 1-cycle command that does not set any busy flags.

¹⁾ In the XC27x8X there is one exception to this rule: when one flash module is busy with program or erase and the FAPI has received some but not all command cycles of a concurrently executable command sequence ("Erase Sector", "Erase Page", "Enter Page Mode", "Load Page Word", "Program Page") then a Reset to Read is performed without issuing a sequence error.

Memory Organization

Description: The flags OPER, SQER, PROER, ISBER, IDBER, DSBER, DDBER in Flash status register are cleared. Additionally, the process status bits (PROG, ERASE, POWER, MAR) are cleared.

This command must not be issued when any of the flash modules is in command mode. In this case it is ignored and a sequence error is reported.

Change Read Margin

Arguments: MR

Definition:

```
MOV XXAAH, XXB0H
MOV XX54H, XXMRH
```

Timing: 2-cycle command that sets “BUSY” of the addressed flash module for around 30 micro seconds.

Description: This command sequence changes the read margin of one flash module. The address XX of the second move identifies the targeted flash module. The flash module needs some time to change its read voltage. During this time BUSY is set and this flash module cannot be accessed. The other flash modules stay readable.

The argument “MR” defines the read margin:

- 00_H: normal read margin.
- 01_H: hard read 0 margin.
- 02_H: alternate hard read 0 margin.
- 05_H: hard read 1 margin.
- 06_H: alternate hard read 1 margin.
- Other values: reserved.

For understanding the read margins please refer to **“Margin Reads” on Page 3-42**.

This command must not be issued when the flash memory is in page mode or any of the flash modules is in command mode. In this case it is ignored and a sequence error is reported.

Note: As noted in **“Margin Control” on Page 3-70** the command sequences **“Program Page”**, **“Erase Sector”**, **“Erase Page”** and **“Erase Security Page”** reset the read margin back to 00_H, i.e. to the normal read margin. The same happens in case of a flash wake-up.

Change Read Timing

Arguments: RT

Definition:

```
MOV XXAAH, XXB0H
MOV XXAAH, XXRTH
```


Memory Organization

Timing: 2-cycle command that sets busy until the new read timing is effective, which can take up to 20 cycles.

Description: This command sequence changes the flash read timing and sets IMB_IMBCTRH.WSFLE accordingly.

After receiving this command sequence all BUSY bits are set so that no further new read requests are accepted (the CPU is stalled). No new internal read requests (e.g. for pre-fetching) are started and all already started reads are performed. When all flash modules are idle the read timing is switched and WSFLE is changed. After that the BUSY bits are cleared and reads can be performed again.

This command must not be issued when the flash memory is in page mode or any of the flash modules is in command mode. In this case it is ignored and a sequence error is reported.

Enter Page Mode

Arguments: PA

Definition:

```
MOV XXAAH, XX50H
MOV PA, XXAAH
```

Timing: 2-cycle command that sets “BUSY” of the addressed flash module for around 20 clock cycles¹⁾.

Description: The page mode is entered to prepare a page programming operation on page address PA. (Write data are accepted only with the “**Load Page Word**” command.)

With this command, the IMB Core initializes the write pointer of its block assembly register to zero so that it points to the first word. The page mode is indicated in the status register IMB_FSR_BUSY with the PAGE bit, separately for each flash module. The page mode and the read mode are allowed in parallel at the same time and in the same flash module so the flash module stays readable. When the addressed page PA is read the content of the flash memory is delivered. The page mode can be aborted and the related PAGE bit in IMB_FSR_BUSY be cleared with the “**Reset to Read**” command. A new “**Enter Page Mode**” command during page mode aborts the actual page mode, which is indicated with the error flag SQER, and restarts a new page operation. So as mentioned above only one of the flash modules can be in page mode at a time. If one of the erase commands or the “**Change Read Margin**” command are received while in page mode it is ignored and a sequence error is reported.

The page mode can be entered in one flash module while others are busy with executing a user data erase or program command, i.e. not while programming or erasing security pages or other blocking sequences.

1) When this command is used to abort a page mode of an other flash module the duration increases to around 30 clock cycles.

Memory Organization

If write protection is installed for the sector to be programmed, the **“Enter Page Mode”** command is only accepted when write protection has before been disabled using the unlock command sequence **“Disable Write Protection”** with four passwords. If global write protection is installed with read protection, also the command **“Disable Read Protection”** can be used if no sector specific protection is installed. If write protection is not disabled when the **“Enter Page Mode”** command is received, the command is not executed, and the protection error flag PROER is set in the IMB_FSR_PROT.

Note: In previous device families (e.g. XC16x) the “Enter Page Mode” did not set “BUSY”. In these devices the “Load Page Word” could be sent directly after issuing “Enter Page Mode”. In XC27x8X it must be waited until “BUSY” clears before sending the “Load Page Word” command sequence.

Enter Security Page Mode

Arguments: SECPA

Definition:

```
MOV XXAAH, XX55H
MOV SECPA, XXAAH
```

Timing: 2-cycle command that sets “BUSY” of flash module 0 for around 100 clock cycles.

Description: This command is identical to the **“Enter Page Mode”** command (see above), with the following exceptions: The addressed page (SECPA) belongs to the security pages of the flash memory and not to the user flash range. This command can only be executed when neither flash write protection nor read protection are active (RPA = 0 and WPA = 0), otherwise it fails with PROER.

This command is refused with SQER when any of the flash modules is in command mode.

The use of this command to install passwords and to disable them again is described in **“Protection Handling Details” on Page 3-45**.

Load Page Word

Arguments: WD

Definition:

```
MOV XXF2H, WD
```

Timing: 1-cycle command that does not set any “BUSY” flags. But note that an immediately following write access to the IMB Core or read from the flash memory is stalled for a few clock cycles if it arrives while the IMB Core is busy with copying its block assembly register content into the flash module assembly buffer. During this stall time the CPU can not perform any action! So either the user software can accept this stall time

Memory Organization

(which must be taken into account for the worst-case interrupt latency) or the software must avoid the blocking accesses.

Description: Load the IMB Core block assembly register with a 16-bit word and increment the write pointer. The 128 byte assembly buffer (i.e. a complete page) is filled by a sequence of 64 “Load Page Word” commands. The word address is not determined by the command but the “Enter Page Mode” command sets a write word pointer to zero which is incremented after each “Load Page Word” command.

This (sequential) data write access to the block assembly register belongs to and is only accepted in Page Mode. The command address of this single cycle command is always the same (F2_H). These low order address bits also identify the “Load Page Word” command and the sequential write data to be loaded into the block assembly register. The high order bits XX should address the target page. The IMB Core takes always the page address that was used by the last “Enter Page Mode” command.

When the 128-bit block assembly register of the IMB Core is filled completely after 8 “Load Page Word” commands the IMB Core calculates the 9 ECC bits and transfers the block into the assembly buffer of the flash module. After that it sets the write pointer of the block assembly register back to zero. The following 8 “Load Page Word” commands fill again the block. After all 8 blocks are filled the “Program Page” command can be used to trigger the program process that transfers the assembly buffer content into the flash array.

While the IMB Core transfers the completed block assembly register to the flash module it can not accept new data for a few cycles. A “Load Page Word” command arriving during this time is stalled by the IMB Core.

If “Program Page” is called before all blocks of the assembly buffer have received new data then the remaining bits are cleared.

If more than 8 times 8 commands are used the additional data is lost. The overflow condition is indicated by the sequence error flag, but the execution of a following “Program Page” command is not suppressed (the page mode is not aborted).

When a “Load Page Word” command is received and the flash is not in page mode, a sequence error is reported in IMB_FSR_OP with SQER flag. In case of a new “Enter Page Mode” command or a “Reset to Read” command during page mode, or in case of an Application Reset, the write data in the assembly buffer is lost. The current page mode is aborted and in case of a new “Enter Page Mode” command entered again for the new address.

Program Page

Arguments: –

Definition:

```
MOV XXAAH, XXA0H
MOV XX5AH, XXAAH
```

Memory Organization

Timing: 2-cycle command that sets “BUSY” of the selected flash module for the whole programming duration. The IMB Core is blocked a few clock cycles after receiving this command and again a few clock cycles before finishing the programming. Write accesses to the flash memory range to execute another command sequence during these times stall the CPU.

Description: The assembly buffer of the flash module is programmed into the flash array. If the last block of data was not filled completely this command finalizes its ECC calculation and copies its data into the assembly buffer before it starts the program process. The selection of the flash module and the page to be programmed depends on the page address used by the last “**Enter Page Mode**” command. The user software should always address the targeted page.

The programming process is autonomously performed by the selected flash module. The CPU is not occupied and can continue with its application.

The “**Program Page**” command is only accepted if the addressed flash module is in Page Mode (otherwise, a sequence error is reported instead of execution). With the “**Program Page**” command, the page mode is terminated, indicated by resetting the related PAGE flag and the command mode is entered and the PROG flag in the status register IMB_FSR_OP is activated and the related BUSY flag is set in IMB_FSR_BUSY.

When the program process has finished BUSY is cleared but PROG stays set. It indicates which operation has finished and will be cleared by a Power-On Reset or by “**Clear Status**”.

Read accesses to the busy flash module are not possible. Reading a busy flash module stalls until the flash module becomes ready again.

If write protection is active for the sector to be programmed, the “**Program Page**” command is not accepted because the Flash is not in Page Mode (see description of the “**Enter Page Mode**” command).

If the page to be programmed is a security page (accepted only in security page mode), the new protection configuration (including keywords or protection confirmation code) is valid directly after execution of this command. During its execution all commands are rejected with a sequence error.

While the IMB Core reads the new protection configuration all DMU accesses to any flash module are stalled.

Erase Sector

Arguments: SA

Definition:

```
MOV XXAAH, XX80H
MOV XX54H, XXAAH
MOV SA, XX33H
```

Memory Organization

Timing: 3-cycle command that sets BUSY of the addressed flash module for the whole erasing duration. The IMB Core is blocked a few clock cycles after receiving this command and again a few clock cycles before finishing the erasing. Write accesses to the flash memory range during these times stall the CPU.

Description: The addressed physical sector in the flash array is erased. Following data reads deliver all-zero data with correct ECC.

The erasing process is autonomously performed by the selected flash module. The CPU is not occupied and can continue with its application.

The sector to be erased is addressed by SA (sector address) in the last command cycle.

With the last cycle of the “**Erase Sector**” command, the command mode is entered, indicated by activation of the ERASE flag in IMB_FSR_OP and after start of erase operation also by the related busy flag in the status register IMB_FSR_BUSY. The BUSY flag is cleared after finishing the operation but ERASE stays set. It can be cleared by a Power-On Reset or the “**Clear Status**” command.

Read accesses to the busy flash module are not possible. Read accesses to the not busy flash module are especially supported. Reading a busy flash module stalls until the flash module becomes ready again.

If write protection is installed for the sector to be erased, the Erase Sector command is only accepted when write protection has before been disabled using the unlock command sequence “**Disable Write Protection**”. If global write protection is installed with read protection, also the command “**Disable Read Protection**” can be used if no sector specific protection is installed. If write protection is not disabled when the “**Erase Sector**” command is received, the command is not executed, and the protection error flag PROER is set in the IMB_FSR_PROT.

This command must not be issued when the flash memory is in page mode. In this case it is ignored and a sequence error is reported.

Erase Page

Arguments: PA

Definition:

```
MOV XXAAH, XX80H
MOV XX54H, XXAAH
MOV PA, XX03H
```

Timing: 3-cycle command that sets BUSY of the addressed flash module for the whole erasing duration. The IMB Core is blocked a few clock cycles after receiving this command and again a few clock cycles before finishing the erasing. Write accesses to the flash memory range during these times stall the CPU.

Description: The addressed page is erased. Following data reads deliver all-zero data with correct ECC.

Memory Organization

With the last cycle of the **“Erase Page”** command, the command mode is entered, indicated by activation of the ERASE flag in IMB_FSR_OP and after start of erase operation also by the related BUSY flag in the status register IMB_FSR_BUSY. BUSY is cleared automatically after finishing the operation but ERASE stays set. It is cleared by a Power-On Reset or the **“Clear Status”** command.

Read accesses to the busy flash array are not possible. Read accesses to the not busy flash modules are especially supported. Reading a busy flash module stalls until the flash module becomes ready again.

If the page to be erased belongs to a sector which is write protected, the command is only executed when write protection has before been disabled (see **“Erase Sector”** command).

In case of using the page erase care must be taken not to exceed the drain disturb limit of the other pages of the same sector.

This command must not be issued when the flash memory is in page mode. In this case it is ignored and a sequence error is reported.

Erase Security Page

Arguments: SECPA

Definition:

```
MOV XXAAH, XX80H
MOV XX54H, XXA5H
MOV SECPA, XX53H
```

Timing: 3-cycle command that sets BUSY of flash module 0 for the whole erasing duration.

Description: The addressed security page is erased.

This command is identical to the **“Erase Page”** command with the following exceptions: The addressed page (SecP0 or SecP1) belongs not to the user visible flash memory range. This command can only be executed after disabling of read protection and of sector write protection.

See **“Protection Handling Examples” on Page 3-52** for a detailed description of re-programming security pages.

The structure of the two security pages (SecP0 and SecP1) is described in **“Layout of the Security Pages” on Page 3-51**.

After erasing a security page the new protection configuration (including keywords or protection confirmation code) is valid directly after execution of this command.

While the IMB Core reads the protection configuration all DMU accesses to any flash module are stalled.

This command must not be issued when the flash memory is in page mode or any of the flash modules is in command mode. In this case it is ignored and a sequence error is reported.

Disable Read Protection

Arguments: PWD

Definition:

```
MOV XX3CH, XXXXH
MOV XX54H, PWD0
MOV XXAAH, PWD1
MOV XX54H, PWD2
MOV XXAAH, PWD3
MOV XX5AH, XX55H
```

Timing: 6-cycle command that does not set any busy flag.

Description: Disable temporarily Flash read protection and — if activated — global write protection of the whole flash memory. The RPA bit in IMB_IMBCTR_H is reset.

This is a protected command sequence, using four user defined passwords to release this command or to check the programmed keywords. For every password one command cycle is required. If the second or fourth password represents the code of the **“Reset to Read”** command, it is interpreted as password and the reset is not executed. The 16-bit passwords are internally compared with the keywords out of the “Security Page 0”. If one or more passwords are not identical to their related keywords, the protected sectors remain in the locked state and a protection error (PROER) is indicated in the Flash status register. In this case, a new **“Disable Read Protection”** command or a **“Disable Write Protection”** command is only accepted after the next Application Reset.

Note: During execution of the “Disable Read” (or Write) Protection command a password compare error is only indicated after all four passwords have been compared with the related keywords.

Note: This command sequence is also used to check the correctness of keywords before the protection is confirmed in the Security Page 1. A wrong keyword is indicated by the IMB_FSR_PROT flag PROER.

After correct execution of this command, the whole flash memory is unlocked and the read protection disable bit RPRODIS is set in the Flash Status Register (IMB_FSR_PROT). Erase and program operations on all sectors are then possible, if the flash memory was also globally write protected (WPA=1), and if they are not separately write protected. The read protection (including global write protection, if so selected) remains disabled until the command **“Re-Enable Read/Write Protection”** is executed, or until the next Application Reset (including HW and SW reset).

This command must not be issued when any of the flash modules is in command mode. In this case it is ignored and a sequence error is reported.

Disable Write Protection

Arguments: PWD

Definition:

```
MOV XX3CH, XXXXH
MOV XX54H, PWD0
MOV XXAAH, PWD1
MOV XX54H, PWD2
MOV XXAAH, PWD3
MOV XX5AH, XX05H
```

Timing: 6-cycle command that does not set any busy flag.

Description: Disable temporarily the global flash write protection or/and the sector write protection of all protected sectors. The WPA bit in IMB_IMBCTRH is reset.

This is a protected command sequence, using four user defined passwords to release this command (as described above for the **“Disable Read Protection”** command).

After correct execution of this command, all write-protected sectors are unlocked, which is indicated in the Flash Status Register (IMB_FSR_PROT) with the WPRODIS bit. Erase and program operations on all sectors are now possible, until

- The command **“Re-Enable Read/Write Protection”** is executed, or
- The next Application Reset (including HW and SW reset) is received.

This command must not be issued when any of the flash modules is in command mode. In this case it is ignored and a sequence error is reported.

Re-Enable Read/Write Protection

Arguments: –

Definition:

```
MOV XX5EH, XXXXH
```

Timing: 1-cycle command that does not set any busy flags.

Description: Flash read and write protection is resumed.

This single-cycle command clears RPRODIS and WPRODIS. The IMB Core is triggered to restore the protection states RPA and WPA from the content of the security page 0 as defined in **Table 3-6 “Flash State” Determining RPA and WPA on Page 3-48**. So in effect this command resumes all kinds of temporarily disabled protection installations.

This command is released immediately after execution.

This command must not be issued when any of the flash modules is in command mode. In this case it is ignored and a sequence error is reported.

3.11.5 Sequence Errors

A word (i.e. 16-bit) data move into the flash address range is interpreted by the command interpreter as command sequence. All byte moves are ignored and cause a sequence error which is reported by setting the bit SQER.

As soon the command interpreter detects that the data moves can't be executed as legal sequence it reports the sequence error.

Note: Data moves addressing not implemented flash areas or powered-down flash modules don't enter the command interpreter and consequently can't cause a sequence error. Usually the next correct command sequence will cause the sequence error because it is interpreted as continuation of the previous one. So instead of checking only for the absence of SQER the other flags (e.g. PAGE, PROG, ERASE) can be further evaluated. For an example see [Section 3.11.6](#).

Generally each data move received while at least one flash module is BUSY causes a sequence error. But in order to support concurrent execution of command sequences this is under certain conditions not done. A SQER is reported under the following conditions:

- If one of the flash modules is in command mode and the running command does not allow concurrent execution a SQER is reported immediately.
- If at least one of the flash modules is in command mode and the running command allows concurrent execution SQER is only reported when the new command targets a busy flash module.
- If at least one of the flash modules is in command mode SQER is reported as soon as a command cycle is detected that can not belong to a command sequence that allows concurrent execution (i.e. when the received data does not belong to "Enter Page Mode", "Load Page Word", "Program Page" or "Erase Page").

The concurrency issues are summarized in [Table 3-5](#).

Table 3-5 Concurrency Issues

New sequence while any module is in mode:	Page Mode	Busy with normal erase or program	Busy with blocking sequence ¹⁾
Reset to Read	Resets page mode	SQER ²⁾	SQER ²⁾
Enter Page Mode	SQER and Re-enters page mode	OK ³⁾	SQER
Enter Sec. Page Mode	SQER and Re-enters page mode	SQER	SQER
Load Page Word	OK	OK in page mode	SQER/ ⁴⁾

Table 3-5 Concurrency Issues (cont'd)

New sequence while any module is in mode:	Page Mode	Busy with normal erase or program	Busy with blocking sequence¹⁾
Program Page	OK	OK in page mode	SQER/— ⁴⁾
Erase Page/Sector	SQER	OK ³⁾	SQER
Erase Sec. Page	SQER	SQER	SQER
*Protection	OK	SQER	SQER
Clear Status	OK	SQER	SQER
Change Read Margin, Change Read Timing	SQER	SQER	SQER

- 1) "Blocking sequences" are: "Erase Security Page", "Program Page" for a security page, "Change Read Margin", "Enter Page Mode", "Enter Security Page Mode", "Change Read Timing" only while these set busy.
- 2) As described in **"Reset to Read"** on **Page 3-28** there is one exception to this rule.
- 3) If the new command sequence targets a different flash module that is in read mode else SQER.
- 4) Situation can not occur because "Program Page" is only allowed in page mode and page mode could not be entered.

Other conditions that cause a sequence error were mentioned above in the command descriptions.

3.11.6 Instructions for Executing Program and Erase Jobs Concurrently

All flash modules¹⁾ can be programmed and erased concurrently. This is however an exceptional case for high-speed flash programming. In the normal case at most one flash module shall be busy while the others can be read.

The limitations reported above in the command sequence descriptions enforce certain behavior for concurrent processes:

- A programming task shall be started in one not interrupted sequence: "Enter Page Mode", then 64 "Load Page Word" and finally the "Program Page". No other command sequence on any other flash module shall interrupt this sequence.
- All security page handling shall be done while all flash modules are in read mode.

1) Additional constraints may apply due to power supply and other device specific reasons. The allowed concurrent processes (including read) are described in the data sheet. This section describes only the logic hardware capabilities.

Memory Organization

- Clearing of error and status flags is as well only possible when all flash modules are in read mode. An exception is the flash module specific handling via **IMB_ECC_STAT**.
- The IMB Core can only finish an ongoing program or erase task successfully when it is not busy with interpreting a command sequence (i.e. the busy of the ongoing tasks is only cleared when the IMB Core is ready to accept a new command sequence and no new command sequence has been started but not completed).

So the required sequence for programming flash modules concurrently is as follows:

1. Send the "Erase Sector" command sequence to each flash module.
2. Wait until all "BUSY" flags are cleared. During this time the data for programming can be read from external.
3. Send "Enter Page Mode", 64 "Load Page Word" and the "Program Page" to the first flash module. Continue this sequence with the other flash modules.
4. Wait until all "BUSY" flags are cleared. This time can be used to read the data for programming the next pages from external.
5. Verify the programmed data of all flash modules.
6. Continue the steps 3 to 5 until all pages of the erased sectors are programmed.
7. Continue the steps 1 to 6 until all sectors are programmed.

The recommend sequence which detects incorrect sequences as early as possible is as follows:

1. "Clear Status" and check that SQER is 0.
2. Send the "Erase Sector" command sequence to each flash module. Check for SQER after issuing each sequence.
3. Wait until all "BUSY" flags are cleared. During this time the data for programming can be read from external.
4. Check for SQER which would indicate an incorrectly issued command sequence.
5. "Clear Status" and check again for SQER. If SQER would be set after "Clear Status" a previous "Erase Sector" hasn't been completed.
6. Send "Enter Page Mode", check if the PAGE flag was set and check if SQER stays 0, send the 64 "Load Page Word" and the "Program Page" to the first flash module. Check if the PAGE flag is cleared and SQER stays cleared after "Program Page" is accepted. Continue this sequence with the other flash modules.
7. Wait until all "BUSY" flags are cleared. This time can be used to read the data for programming the next pages from external.
8. Verify the programmed data of all flash modules.
9. Continue the steps 6 to 8 until all pages of the erased sectors are programmed.
10. Continue the steps 1 to 9 until all sectors are programmed.

3.11.7 Data Integrity

This section describes means for detecting and preventing the inadvertent modification of data in the flash memory.

3.11.7.1 Error Correcting Codes (ECC)

With very low probability a flash cell can become disturbed or lose its data value faster than specified. In order to reach the defined overall device reliability each 128-bit block of flash data is accompanied with a 9-bit ECC value. This redundancy supplies SEC-DED capability, meaning “single error correction and double error detection”. All single bit errors are corrected (and the incident is detected), all double bit errors are detected and even most triple bit errors are detected but some of these escape as valid data or corrected data.

A detected error is reported in the register **IMB_FSR_PROT** and **IMB_ECC_STAT**. Software can select which type of error should trigger a trap by the means of register **IMB_INTCTR**. In the system control further means exist to modify the handling of errors (see “**SCU Trap Control Registers**” on Page 9-197). The enabled trap requests by the flash module are handled there as “Flash Access Trap”. In case of a double-bit error the read data is always replaced with a dummy data word.

3.11.7.2 Aborted Program/Erase Detection

Where the ECC should protect from intrinsic failures of the flash memory that affect usually only single bits; an interruption of a running program or erase process might cause massive data corruption:

- The erase process programs first all cells to 1 before it erases them. So depending on the time when it is interrupted the data might be in a different state. This can be the old data, all-one, a random value, a weak all-zero or finally all-zero.
- The program process programs all bits concurrently from 0 to 1. If it is interrupted not all set bits might read as 1 or contain a weak 1.

The register **IMB_FSR_OP** contains the bits ERASE and PROG. These bits stay set until the next “**Clear Status**” command or Power-On Reset. So if an erase or program process is interrupted by an Application Reset one of these bits is still set which allows to detect the interruption. It lies in the responsibility of the software to send the “**Clear Status**” command after a finalized program/erase process to enable this evaluation.

Another possible measure against aborted program/erase processes is to prevent resets by configuring the SCU appropriately.

If a program or erase process was aborted by a Power-On Reset (e.g. due to a power failure) there do not exist reliable means to detect this by reading the affected flash range. Even with margin reads an early or late aborted process might go unnoticed although it might in the long-term affect reliability.

Therefore the application must ensure that flash processes can perform uninterrupted and under the defined operating conditions, e.g. by early brown-out warning that prevents the software from starting flash processes.

After a flash process aborted the affected address range must be erased and re-programmed.

3.11.7.3 Margin Reads

Margin reads can be used to verify that flash data is readable with a certain margin. This is typically used as additional check directly after end-of-line programming. As explained above this is not a reliable method for detecting interrupted program or erase processes but the probability of detecting such cases can be increased.

Reading with “hard read 0 margin” returns weak 0s as 1s and reading with “hard read 1 margin” returns weak 1s as 0s. Changing the read margin is done with the command sequence “**Change Read Margin**” and is reported by the status register “**IMB_MAR0**”.

3.11.7.4 Protection Overview

The flash memory supports read and write protection for the whole memory and separate write protection for each logical sector. The logical sector structure is depicted in **Figure 3-6** for a 256 KB array. The logical sector structure of the smaller arrays is equivalent but if they are used as flash module 0 the missing physical sector 15 is added on top. Thus flash module 0 offers depending on its size the following sectors:

- 256 KB: physical sectors 0 – 14, 16 – 63. Logical sector numbers: 0 – 12, logical sector 6 is shortened to 12 KB.
- 128 KB: physical sectors 0 – 14, 16 – 32. Logical sector numbers: 0 – 10, logical sector 6 is shortened to 12 KB.
- 64 KB: physical sectors 0 – 14, 16. Logical sector numbers: 0 – 7, logical sector 6 is shortened to 12 KB.

Usable physical sector numbers in the other flash modules:

- 256 KB: physical sectors 0 – 63. Logical sector numbers: 0 – 12.
- 64 KB: physical sectors 0 – 15. Logical sector numbers: 0 – 6.
- 32 KB: physical sectors 0 – 7. Logical sector numbers: 0 – 4.

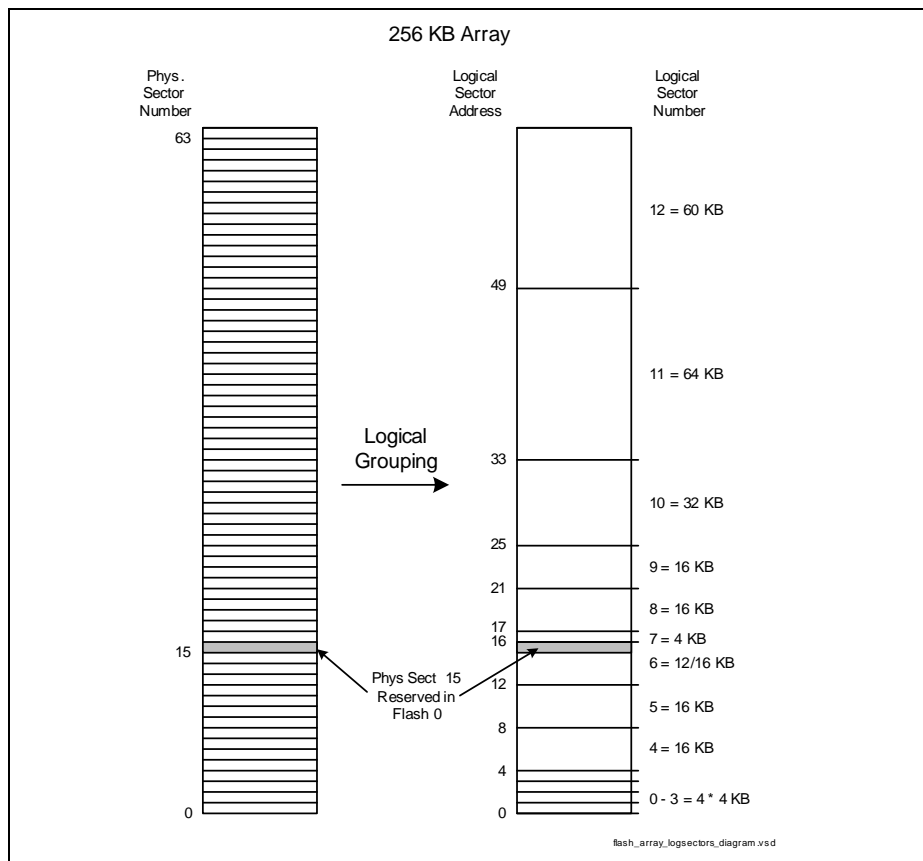


Figure 3-6 Logical Sectors

If read protection is installed and active, any flash read access is disabled in case of start after reset from external memory or from internal RAM. Debug access is as well disabled and thus the execution of injected OCDS instructions. In case of start after reset in internal flash, all flash access operations are controlled by the flash-internal user code and are therefore allowed, as long as not especially disabled by the user, e.g. before enabling the debug interface.

Per default, the read protection includes a full (global) flash memory write protection covering all flash modules. This is necessary to eliminate the possibility to program a dump routine into the Flash, which reads the whole Flash and writes it out via the external bus or a serial interface. Program and erase accesses to the flash during active read protection are only possible, if write protection is separately disabled. Flash write

Memory Organization

and read protection can be temporarily disabled, if the user authorizes himself with correct passwords.

The device also features a sector specific write protection. Software locking of flash memory sectors is provided to protect code and data. This feature disables both program and erase operations for all protected sectors. With write protection it is supported to protect the flash memory or parts of it from unauthorized programming or erase accesses and to provide virus-proof protection for all sectors.

Read and write protection is installed by specific security configuration words which are programmed by the user directly into two "Security Pages" (SecP0/1). After any reset, the security configuration is checked by the command state machine (IMB Core) and installations are stored (and indicated) in related registers. If any protection is enabled also the security pages are especially protected.

For authorization of short-term disabling of read protection or/and of write protection a password checking feature is provided. Only with correct 64-bit password a temporary unprotected state is taken and the protected command sequences are enabled. If not finished by the command **"Re-Enable Read/Write Protection"**, the unprotected state is terminated with the next reset. Password checking is based on four 16-bit keywords (together 64 bits) which are programmed by the user directly into the "Security Page 0" (SecP0).

Special support is provided to protect also the protection installation itself against any stressing or beaming aggressors. The codes of configuration bits are selected, so that in case of any violation in the flash array, on the read path or in registers the protected state is taken per default. In registers and security pages, protection control bits are coded always with two bits, having both codes, "00_B" and "11_B" as indication of illegal and therefore protected state.

3.11.8 Protection Handling Details

As shortly described in **“Protection Overview” on Page 3-42** the flash memory can be in different protection states. The protection handling can be separated into different layers that interact with each other (see **Figure 3-7**).

- The lowest layer consists of the physical content of the security pages SecP0 and SecP1. This information is used to initialize the protection system during startup.
- The next layer consists of registers that report the state of the physical layer (IMB_PROCONx) and the protection state (IMB_FSR_PROT). The protection state can be temporarily changed with command sequences which is reflected in the IMB_FSR_PROT.
- The highest layer is represented by 4 fields of the IMB_IMBCTR register. These fields define the protection rights of the customer software (are read or write accesses currently allowed or not).

The IMB Core controls the protection state of all connected flash modules centrally. In this position it can supervise all accesses that are issued by the CPU.

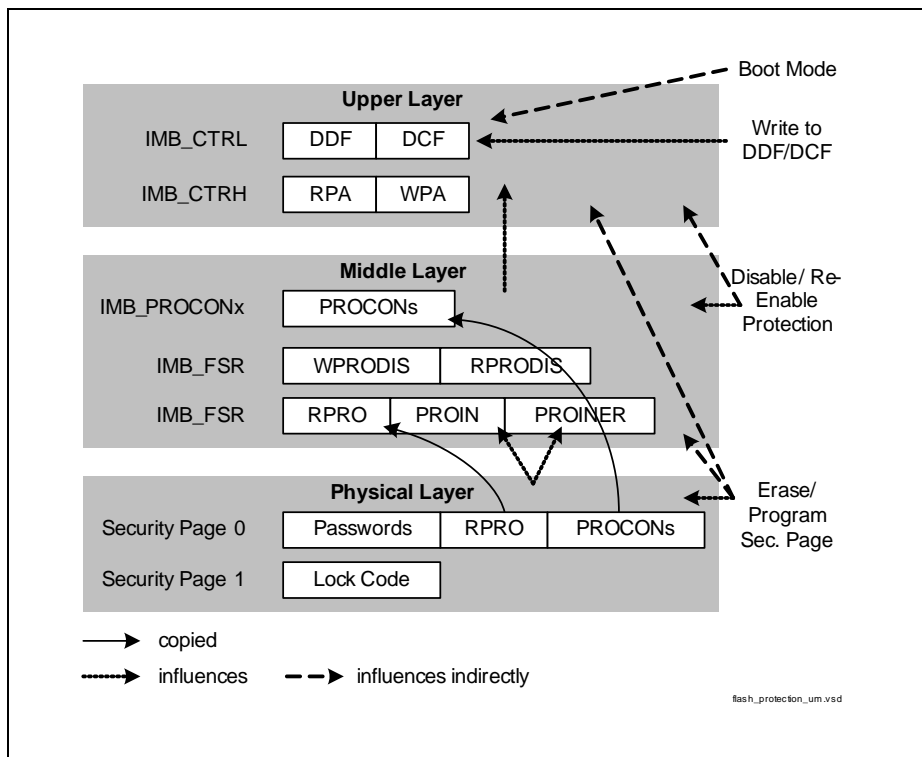


Figure 3-7 Protection Layers

3.11.8.1 The Lower Layer “Physical State”

After reset the protection state of the device is restored from the following information:

- The security page 1 contains a “lock code”. This consists of two words of data (32 bits). If it has the value AA55AA55_H then security page 0 determines the protection state. Otherwise (i.e. the lock code was not found) the device is in the “non-protected state”. The content of the security page 0 is still copied into the registers as described in **“The Middle Layer “Flash State”” on Page 3-47** but their values are ignored in the non-protected state.
- The security page 0 contains the RPRO double bit, the write protection bits SnU and 4 passwords. If the field RPRO contains a valid 01_B or 10_B entry the page is valid and the device is in the “protection installed state”. The page content determines the security settings after startup. If SecP0 contains an invalid RPRO entry the device is in the “errored protection” state.

To summarize: the content of the security pages determines if the device is in the “non-protected state”, “protection installed state” or “errored protection state”. These states are reflected in the register settings of the next layer.

The device is usually delivered in the “non-protected state”.

The exact layout of the security pages is described in [“Layout of the Security Pages” on Page 3-51](#).

3.11.8.2 The Middle Layer “Flash State”

The middle layer consists of the registers IMB_PROCONx and IMB_FSR_PROT and commands that manipulate them and the content of the security pages.

During startup the physical state is examined by the IMB Core and it is reflected in the following bit settings of IMB_FSR_PROT:

- “non-protected state”: PROIN = 0, PROINER = 0.
- “protection installed state”: PROIN = 1, PROINER = 0.
- “errored protection state”: PROIN = 0, ROINER = 1.

The fourth possible setting PROIN=1 and PROINER=1 is invalid and can not occur.

The IMB_PROCONx registers are initialized during startup with the content of the security page 0. The bits DSBER and DDBER indicate if an ECC error occurred. The customer software has thus the possibility to detect disturbed security pages and it can refresh their content.

Commands

Other bits of the IMB_FSR_PROT: RPRODIS, WPRODIS, PROER can be manipulated with command sequences and define together with the other bits the protection effective for the next layer. All three bits are 0 after system startup.

The command **“Disable Read Protection”** sets RPRODIS to 1 if the correct passwords that are stored in SecP0 are supplied. If incorrect passwords are entered the bit PROER is set and RPRODIS stays unchanged. As protection against “brute force attacks” that search the correct password the password detection is locked. So after supplying the first incorrect password all following passwords even the correct ones are rejected with PROER. This state is only left by an Application Reset or by erasing SecP0.

The disabled protection can be enabled again by the Application Reset or by the command **“Re-Enable Read/Write Protection”** which clears RPRODIS again.

The bit PROER can be reset by an Application Reset or by the commands **“Reset to Read”** and **“Clear Status”**.

The command **“Disable Write Protection”** sets WPRODIS to 1 if the correct passwords are supplied. It behaves analog to RPRODIS as described above.

The command **“Re-Enable Read/Write Protection”** clears RPRODIS and WPRODIS.

Memory Organization

The commands “**Enter Page Mode**”, “**Enter Security Page Mode**”, “**Erase Page**”, “**Erase Security Page**” and “**Erase Sector**” set PROER if the write access to the addressed range is not allowed. If a write access is allowed or not is determined by the next level.

Table 3-6 summarizes how the “Flash State” of protection determines the RPA and WPA fields of IMB_IMBCTRH. For the double bits a short notation is used here and in the following sections: 1 means active, 0 means inactive, ‘#’ means invalid and ‘—’ means do not care including invalid states. The symbol ‘|’ means logic or.

Table 3-6 “Flash State” Determining RPA and WPA

IMB_FSR. PROI N	IMB_FSR. PROI NER	IMB_FSR. RPR O	IMB_FSR. RPR ODIS	IMB_FSR. WPR ODIS	Resulting Security Level in RPA and WPA
0	0	—	—	—	Non-protected state: RPA = 0, WPA = 0.
1	0				Protection installed state (possibly disabled, see below):
		0	—	0	RPA = 0, WPA = 1.
		0	0	1	RPA = 0, WPA = 0.
		1 #	0	0	RPA = 1, WPA = 1.
		—	1	1	RPA = 0, WPA = 0 (all disabled).
		1 #	0	1	RPA = 1, WPA = 0.
		1 #	1	0	RPA = 0, WPA = 1.
0	1				Errored protection state (see below):
		—	0	0	RPA = 1, WPA = 1.
		—	0	1	RPA = 1, WPA = 0.
		—	1	0	RPA = 0, WPA = 1.
		—	1	1	RPA = 0, WPA = 0.

3.11.8.3 The Upper Layer “Protection State”

This layer consists mainly of the 4 fields DCF, DDF, WPA and RPA of the IMB_IMBCTRH register. These determine the effective protection state together with registers of the lower layers. Some of the above mentioned command sequences directly influence these fields as well. In order to increase the resistance against beaming or power supply manipulation all 4 fields are coded with 2 bits. Generally “01”

Memory Organization

means active, “10” inactive and the two other states “00” and “11” are invalid and are recognized as “attacked” state.

Effective Security Level

The effective security level based on these 4 double-bits is summarized in [Table 3-7](#) and [Table 3-8](#). For the double bits the same short notation is used as before: 1 means active, 0 means inactive, ‘#’ means invalid and ‘–’ means do not care including invalid states.

Table 3-7 Effective Read Security

RPA	DCF	DDF	Security Level
0	–	–	No read protection.
1 #	0	0	No read protection.
	–	1 #	Data reads prohibited.
	1 #	–	Code fetches prohibited.

Table 3-8 Effective Write Security

WPA	RPA	Security Level
0	–	No write protection
1 #	1 #	Global write protection.
1 #	0	Sector specific write protection depending on IMB_PROCONx.

To summarize:

- Read protection is always globally affecting the whole flash memory range. Code fetches and data reads can be separately controlled.
- Write protection can be global when the read protection is effective or it can be specific for each logical sector.

The lower and the middle security layers determine how the 4 effective IMB_IMBCTR fields are preset, changed and how software can access them. This is discussed in the following paragraphs.

Initialization of the Effective Security Level

After Application Reset protection is activated so that RPA, WPA, DDF and DCF are set. During startup the IMB Core determines the stored security level as described in [“The Lower Layer “Physical State”” on Page 3-46](#) and sets IMB_FSR_PROT.PROIN and IMB_FSR_PROT.PROINER and IMB_PROCONx as described in [“The Middle Layer](#)

“Flash State” on Page 3-47. The IMB Core further initializes the IMB_IMBCTRLH fields RPA and WPA according to the rules of **Table 3-6**.

The bits DDF and DCF of the IMB_IMBCTRL are not initialized by the IMB Core. During system startup they are initialized depending on the startup condition. If code fetching starts in the flash memory then they are set to the inactive state. In all other cases they are activated to prevent read access to the flash memory without proving password knowledge.

Changing the Effective Security Level

During run-time the effective security level can be changed. This can be done by directly writing to the IMB_IMBCTRL register or indirectly by changing the bits of the middle layer by commands as **“Disable Write Protection”** or even double indirectly by changing the content of the security pages which changes bits in the middle layer and influences the effective security level.

Writing directly to IMB_IMBCTRL:

- DCF and DDF can be deactivated only if RPA is inactive. They can always be activated.

Indirectly by using a command sequence:

- A successful **“Disable Read Protection”** sets RPRODIS and clears RPA.
- A successful **“Disable Write Protection”** sets WPRODIS and clears WPA.
- **“Re-Enable Read/Write Protection”** clears RPRODIS and WPRODIS and sets RPA and WPA according to **Table 3-6** depending on PROIN, PROINER and RPRO.

Double indirect by changing security pages. After executing a command sequence that changed the content of a security page the IMB Core immediately reads back the pages and determines all resulting security data as described for system startup in **“Initialization of the Effective Security Level” on Page 3-49**. The examples in **“Protection Handling Examples” on Page 3-52** will show how this can be used for installing and removing protection or changing passwords.

3.11.8.4 Reaction on Protection Violation

If software tries to violate the protection rules the following happens:

- Reading data when read protection is effective: The bit IMB_FSR_PROT.PROER is set and the Flash access trap can be triggered via the SCU if IMB_INTCTR.DPROTRP is 0. Default data is delivered.
- Fetching code when read protection is effective: the trap code “TRAP 15₀” is delivered instead.
- Programming or erasing memory ranges when they are write protected: PROER is set.

3.11.8.5 Layout of the Security Pages

The previous sections just mentioned the content of the security pages. This section depicts their exact layout. **Figure 3-8** depicts symbolically the layout of the security pages 0 and 1.

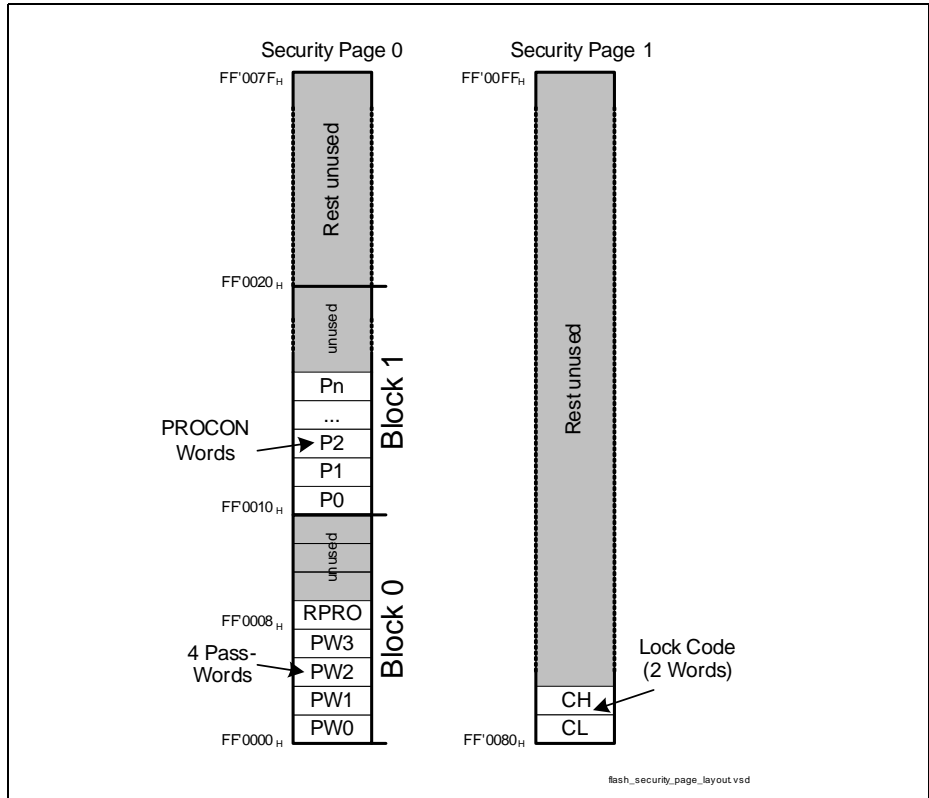


Figure 3-8 Layout of Security Pages

Generally the 16-bit words are stored as always in the XC27x8X in little endian format.

- The PW_x words contain the passwords.
- The double bit RPRO is stored as in the related ISFR **IMB_FSR_PROT** in the bits 15 and 14. The other bits of this word are unused and should be kept all-zero.
- The PROCON data is stored as defined in the **IMB_PROCON_x (x=0-4)** ISFR.
- The lock code consists of the two words CL and CH. Both contain "AA55_H" to form the correct lock code.

All bytes of the used blocks of the security pages (block 0 and 1 of SecP0 and block 0 of SecP1) are to be considered as “reserved” and must be kept erased, i.e. with all-zero content. The unused blocks of the security pages (blocks 2 to 7 of SecP0 and blocks 1 to 7 of SecP1) shall be programmed with all-one data.

3.11.9 Protection Handling Examples

Some examples on how to work with the protection system.

Delivery State

The device is delivered in the “non-protected state”.

Security page 1 is erased (so it does not contain the “lock code” AA55AA55_H).

Security page 0 is erased and so “invalid” but because SecP1 is erased this data is anyhow not evaluated. Only its content is copied into corresponding the registers.

During startup the bits DDF and DCF are set depending on the start mode but as RPA and WPA are inactive all accesses to the flash memory are allowed.

The data sectors of the flash memory are delivered in the erased state as well. All sectors can be programmed. After uploading the software the customer can install write and read protection.

First Time Password Installation

In order to install a password generally the lock code in SecP1 has to be erased. In this case the code is not present.

After that SecP0 must be erased with “**Erase Security Page**” in order to be able to change RPRO. Erasing SecP0 clears RPRO to “00_B” which is an invalid state. After finishing the erase command the IMB Core restores the IMB_FSR_PROT and IMB_IMBCTR_H fields from the flash data.

Because no lock code is present in SecP1 the invalid state of RPRO has no effect on the user visible protection. Still all parts of the flash memory can be written.

The second step is to program the information of SecP0 with the required security information. Again the IMB Core reads immediately back the stored data and initializes the security system. As SecP1 still does not contain the lock code the device stays in the “non-protected” mode.

The security pages cannot be read directly by customer software. The data programmed into SecP0 can therefore only be verified indirectly. The data of the RPRO and SnU fields can be checked by reading the IMB_PROCON and IMB_FSR_PROT registers. The passwords can be verified with the command “**Disable Read Protection**”. If the password does not match the bit PROER is set. But because of the erased SecP1 the flash memory stays writable. So after erasing SecP0 the correct password can be programmed again.

Memory Organization

After the SecP0 was verified successfully SecP1 gets programmed with the lock code AA55AA55_H which enables the security settings of SecP0.

Because the password validation left RPRODIS set the command “**Re-Enable Read/Write Protection**” must be used to finally activate the new protection.

Changing Passwords or Security Settings

Changing the passwords is a delicate operation. The interrelation of the two security pages must be kept in mind.

Usually in the protected state the SecP1 contains the lock code. First write protection must be disabled with the correct passwords. Then the lock code in SecP1 is erased. If this operation was successful PROIN will be cleared by the IMB Core. Now SecP0 can be safely erased.

From this point on the security pages are in the factory delivery state and the new passwords and security settings can be installed as described above.

Attention: *The number of times a security page may be changed is noted in the data sheet.*

3.11.10 EEPROM Emulation

The flash memory of the XC27x8X is used for three purposes:

1. Storage of program code. Updates happen usually very seldom. The main criteria to be fulfilled is a retention of the life-time of the product.
2. Storage of constant data: this data is stored together with program code. So this data is very seldom updated. Endurance is of no issue here but retention identical to the code memory is required.
3. Data updated during run-time: this might be data with a very high frequency of updates like a mileage counter or access keys for key-less entry. Other data might be changed only in case of failures and other data might only be transferred from RAM to non-volatile memory before the system is powered down.

Especially for the third type of data the non-volatile memory needs EEPROM like characteristics:

- Fine program/erase granularity which is in EEPROMs typically 1 byte.
- Higher endurance than the intrinsic endurance of flash cells.
- Short program and erase duration per byte. Especially for storing data in an emergency (e.g. power failure) short latencies might be required.

A basic requirement for changing data during run-time is that code execution can still resume, especially interrupt requests must still be serviced. This requirement is fulfilled in all devices with more than one flash module because these work independently. If one is busy with program or erase then code can still be executed from the other.

In devices with only one flash module code would have to be executed from PSRAM while the flash module is busy.

The other requirements are more difficult to fulfill because the XC27x8X does not have an EEPROM available but only the flash memory with the already frequently mentioned limitations: big program/erase granularity, moderately long program/erase duration, limited cell endurance with reduced retention at high number of program/erase cycles, pages not isolated but affected by drain disturbs.

In order to alleviate these effects on run-time storage of data software is used to emulate EEPROM. There is quite a number of algorithms for efficiently using flash memory as EEPROM. The following section describes one (the most simple) of these algorithms.

It should be noted that the XC27x8X does not offer the customer any hardware means for EEPROM emulation. All of the following must be realized by software.

3.11.10.1 The Traditional EEPROM Emulation

The key point is to solve the limited endurance by storing data in N different physical places. In XC27x8X the algorithm could use N sequential pages or groups of pages. If data is currently stored in the page group "x" then the next program happens to the page group $(x+1) \bmod N$.

Memory Organization

After boot up the last correct page group must be found. This could be done by either evaluating a counter (from 0 to $2*N-1$) or the old entries are invalidated by erasing the page after programming the new one. Additionally a CRC check could be performed over the group.

As all involved pages are re-used cyclically the endurance from customer perspective is increased by the factor N. N must be chosen high enough to fulfill endurance and retention requirements. Disturbs in the group of N pages are no issue because they incur at most N-1 disturbs before they get written with new data. Care must be taken however if one sector accommodates different groups of pages with different update behavior. In this case the updates of one group of pages could exceed the disturb limits of the other group. So generally one sector should be used only by one such EEPROM cyclic buffer.

The algorithm keeps the old data until the new data is verified so power failure during programming can only destroy the last update but the older data is still available. There are still some issues with power failure that need special treatment:

- Power is cut during programming: the following boot-up might find an apparently correctly programmed page. However the cells might be not fully programmed and thus have a much lower retention or the read data is unstable (e.g. changing operating conditions cause read errors).
If the power is cut early the page can appear as erased although some cells are partly programmed. When programming different data to this apparently erased page read errors might occur.
- Power is cut during erase: the same as above can happen. Data may appear as erased but the retention is lowered. A power failure during a page-erase can inhibit readability of all data in its physical sector. Therefore an algorithm is advantageous that performs erases only in sectors that don't contain anymore current data.

The algorithm can be improved to be more robust against such cases, e.g. program always two pages, mark the end of an erase process by programming a page. But generally aborting flash processes is a forbidden "operating condition".

The main deficiency of the described algorithm is that the software designer is required to plan the use of the flash memory thoroughly. The user has to choose the correct value of N. Then all data has to be allocated to pages. Data sharing one page should have a similar or better identical update pattern (otherwise unchanged data is unnecessarily written). If one set of data does not fill a complete sector the available pages must be possibly left unused because they might incur too many drain disturbs.

There are other algorithms that try to alleviate these efforts by monitoring the flash usage and adapt automatically the assignment of data to flash cells.

3.11.11 Interrupt Generation

Long lasting processes (these are mainly: program page, erase page, erase sector and margin changes, but also enter page mode) set the `IMB_FSR_BUSY.BUSY` flag of one flash module when accepting the request and reset this flag after finishing the process. Software is required to poll the busy flag in order to determine the end of the operation. In order to release the software from this burden an interrupt can be generated. If the interrupt is enabled by `IMB_INTCTRL.IEN` then all transitions from 1 to 0 of one of the `IMB_FSR_BUSY.BUSY` flags send an interrupt request to the SCU. In the SCU (see **“SCU Interrupt Generation” on Page 9-159** in the SCU chapter) the interrupt request (noted as “PFI” Program Flash Interrupt) is multiplexed with other interrupt sources and is forwarded to one of four interrupt nodes. The selection of the interrupt node is done with the register field `INTNP1.PF`. The SCU contains its own set of interrupt status flags (`INTSTAT`), interrupt disable control (`INTDIS`) and registers for setting this interrupt (`INTSET`) and clearing it (`INTCLR`).

The **“Enter Page Mode”** command sets `BUSY` only for a few clock cycles. It is usually not advisable to enable the interrupt for this command.

The register `IMB_INTCTR` contains fields for the interrupt status “ISR”, an enable for the interrupt request “IEN” and fields for clearing the status flag “ICLR” or setting if “ISSET”. It should be noted that the interrupt request is only sent when `ISR` becomes 1 and `IEN` was already 1. No interrupt is sent when `IEN` becomes 1 when `ISR` was already 1 or both are set to 1 at the same time.

3.11.12 Recommendations for Optimized Flash Usage

This section describes best practices for using the flash in certain application scenarios, e.g. how to use effectively ECC and margin reads. For a description of the hardware features consult **“Data Integrity” on Page 3-41**.

3.11.12.1 Programming Code and Constant Data

Code and constant data are programmed only few times during life-time of a device, e.g. end-of-line in ECU production or when service updates are performed. As the readability of this data is decisive for the product quality customers might want to implement the elaborate “best practice” advice.

Basic Advice

Always ensure correct operating conditions and prevent power failures during flash operation.

As basic protection against handling errors all data should be verified after programming. Single-bit ECC errors should be ignored. The appearance of small numbers of single-bit errors is a consequence of known physical effects.

Best Practice

This approach offers best possible quality but risks that programming steps need to be repeated even unnecessarily (“false negatives”):

- Use “Erase Sector” to erase complete sectors.
- Program the sector with data. A common protection against software crashes is to fill the unused part of the sector with trap codes.
- Change the read level to hard margin 0.
- Verify the programmed data, note comparison errors and double-bit ECC errors and count single-bit ECC errors. Take care to evaluate the ECC error flags only once per 128-bit data block and clear them afterwards.
- Repeat this check with hard margin 1.
- After programming all sectors:
 - Erase and re-program all sectors with comparison or double-bit ECC errors.
 - If a flash module contained more than a certain number (e.g. 10) of single-bit ECC errors it is recommended to erase and re-program the affected sectors (i.e. those containing at least one single-bit error).
 - Attention: a high number of single-bit errors indicates usually a violation of operating conditions.

The threshold of allowed single-bit errors could be increased for in-service updates in order to reduce the risk of false negatives.

3.11.12.2 EEPROM Emulation

For EEPROM emulation the goal is usually not readability over device life-time but highest possible robustness (against violated operating conditions, power failures, even failing flash pages e.g. due to over-cycling). The risk of false negatives should be minimized.

A good robustness is achieved with the following approach:

- Verify data after programming with the normal read level. Single-bit ECC errors should be ignored.
- In case of comparison error or double-bit ECC error the data should be programmed again to the next flash range (e.g. next page or sector).
- The number of re-programming trials should be limited (e.g. to 3) to protect against violated operating conditions.

Obviously this jumping over failed pages can be only used optimally when the algorithm does not expect data on fixed addresses.

Failing pages can prevent “Erase Sector” from erasing any data in the affected sector. The “Erase Page” command however could still erase all other pages. These other pages stay readable and programmable.

3.12 On-Chip Program Memory Control

The internal memory block “IMB” contains all memories of the so called “on-chip program memory area” in the address range from C0'0000_H to FF'FFFF_H. Included are the program SRAM, the embedded flash memories and central control logic called “IMB Core”.

In the XC27x8X device the IMB contains the following memories:

- up to 1,088 KB flash memory in five independent modules.
- up to 64 KB program SRAM (see [Section 3.4.1](#)).

The IMB connects these memories to the CPU data bus and the instruction fetch bus. Each memory can contain instruction code, data or a mixture of both. The IMB manages accesses to the memories and supports flash programming and erase.

3.12.1 Overview

The [Figure 3-9](#) shows how the IMB and its memories are integrated into the device architecture. Only the main data streams are included. The data buses are usually accompanied by address and control signals and check-sum data like parity or ECC.

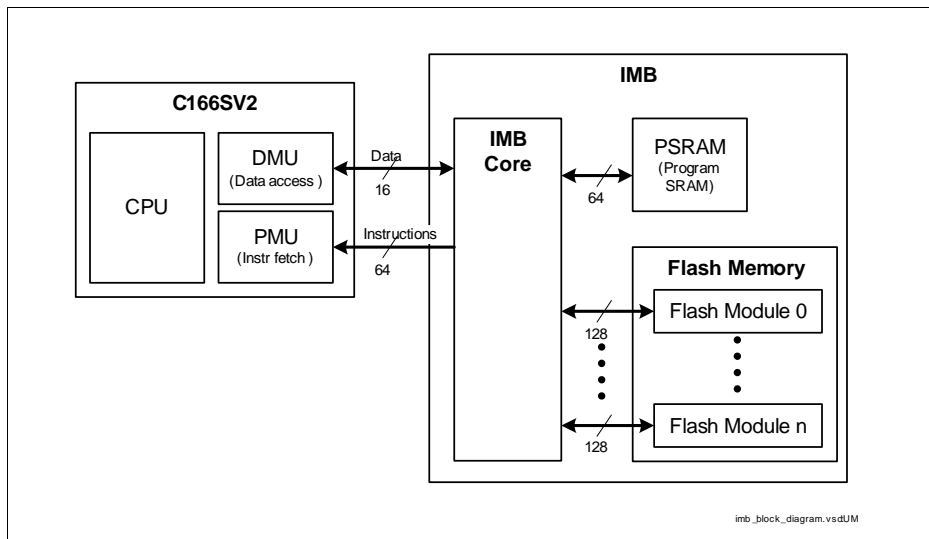


Figure 3-9 IMB Block Diagram

The CPU has two independent busses. The instruction fetch bus is controlled by the program management unit “PMU” of the CPU. It fetches instructions in aligned groups of 64 bits. The instruction fetch unit of the CPU predicts the outcome of jumps and fetches instructions on the predicted branch in advance. In case of a misprediction this interface

Memory Organization

can abort outstanding requests and continues fetching on the correct branch. As the CPU can consume up to one 32-bit instruction per clock cycle the performance of this interface determines the CPU performance.

The data bus is controlled by the data management unit "DMU" of the CPU. It reads data in words of 16 bits. Write accesses address as well 16-bit words but additional byte enables allow changing single bytes.

Because of the CPU's "von Neumann" architecture data and instructions (and "special function registers" to complete the list) share a common address range. When instructions are used as data (e.g. when copying code from an IO interface to the PSRAM) they are accessed via the data bus. The pipelined behavior of the CPU can cause that code fetches and data accesses are requested simultaneously. The IMB takes care that accesses can perform concurrently if they address different memories or flash modules.

Additional connections of the IMB to central system control units exist. These are not shown in the block diagram.

3.12.2 Register Interface

The **“IMB Registers” on Page 3-60** describes the special function registers of the IMB. In **“System Control Registers” on Page 3-76** the special function registers that influence the IMB but are not allocated to the IMB address range are described.

Note: Some registers contain bit fields named ‘reserved’. They should be written with ‘0’. Read data is unpredictable and should be ignored.

3.12.2.1 IMB Registers

The section describes all IMB special function registers.

Table 3-9 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
IMB_IMBCTRL	IMB Control Low	FF FF00 _H	Page 3-61
IMB_IMBCTRH	IMB Control High	FF FF02 _H	Page 3-63
IMB_INTCTR	Interrupt Control	FF FF04 _H	Page 3-64
IMB_FSR_BUSY	Flash State Busy	FF FF06 _H	Page 3-66
IMB_FSR_OP	Flash State Operations	FF FF08 _H	Page 3-67
IMB_FSR_PROT	Flash State Protection	FF FF0A _H	Page 3-68
IMB_MAR0	Margin 0	FF FF0C _H	Page 3-70
IMB_PROCON0	Protection Configuration 0	FF FF10 _H	Page 3-72
IMB_PROCON1	Protection Configuration 1	FF FF12 _H	Page 3-72
IMB_PROCON2	Protection Configuration 2	FF FF14 _H	Page 3-72
IMB_PROCON3	Protection Configuration 3	FF FF16 _H	Page 3-72
IMB_PROCON4	Protection Configuration 4	FF FF18 _H	Page 3-72
IMB_ECC_TRAP	ECC Trap Control	FF FF20 _H	Page 3-72
IMB_ECC_STAT	ECC Status	FF FF22 _H	Page 3-74

IMB Control

Global IMB control.

Both IMB_IMBCTRL and IMB_IMBCTRH are reset by an Application Reset.

The write access to both registers is controlled by the register security mechanism as defined in the SCU chapter **“Register Control” on Page 9-227**. Please note that the

Memory Organization

register write-protection is not activated automatically again after an access to IMB_IMBCTRL because this happens only for SCU internal registers.

IMB_IMBCTRL

IMB Control Low

ISFR (FF FF00_H)

Reset value: 55AC_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DDF		DCF		0								DLC PF		WSFLASH	
rw		rw										rw		rw	

Field	Bits	Typ	Description
WSFLASH	[2:0]	rw	Wait States for Flash Access Number of wait cycles after which the IMB expects read data from the flash memory is: $N_{WS} = WSFLASH + 2 \cdot WSFLE$. This field determines as well the read timing of the PSRAM in the flash emulation address range. See “Flash Emulation” on Page 3-13 . The correct setting of this field depends on the system clock frequency. The data sheet of the device describes this relation.
DLCPF	3	rw	Disable Linear Code Pre-Fetch 0_B “High Speed Mode”: When the next read request will be delivered from the buffer and so the flash memory would be idle, the IMB Core autonomously increments the last address and reads the next 128-bit block from the flash memory. 1_B “Low Power Mode”: This feature is disabled. Usually for code with power minimization requirements or for code with short linear code sections this feature should be disabled (DLCPF = 1). Enabling this feature is only advantageous for code section with longer linear sequences. With lower values of WSFLASH the performance gain of DLCPF=0 is reduced. In case of low WSFLASH settings DLCPF=1 might even lead to better performance than with linear code pre-fetch.

Memory Organization

Field	Bits	Typ	Description
DCF	[13:12]	rw	Disable Code Fetch from Flash Memory 01 _B Short notation DCF = 1. If RPA = 1 instructions cannot be fetched from flash memory. If RPA = 0 this field has no effect. 10 _B Short notation DCF = 0. Instructions can be fetched independent of RPA. 00 _B Illegal state. 11 _B Illegal state. Both illegal states have the same effect as "01". This state can only be left by an Application Reset. When RPA = 0 software can change this field to any value. Otherwise code fetch can only be disabled but not enabled anymore until the next Application Reset.
DDF	[15:14]	rw	Disable Data Read from Flash Memory 01 _B Short notation DDF = 1. If RPA = 1 data cannot be read from flash memory. If RPA = 0 this field has no effect. 10 _B Short notation DDF = 0. Data can be read independent of RPA. 00 _B Illegal state. 11 _B Illegal state. Both illegal states have the same effect as "01". This state can only be left by an Application Reset. When RPA = 0 software can change this field to any value. Otherwise data reads can only be disabled but not enabled anymore until the next Application Reset.
0	[11:4]	rw	Reserved Read as 0, should be written 0

IMB control high word. The WPA and RPA fields are described in **"Protection Handling Details" on Page 3-45**.

IMB_IMBCTRH

IMB Control High

ISFR (FF FF02_H)

Reset value: 0025_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSPROT								0	0	WSFLE		RPA		WPA	
rw								r	r	rh		rh		rh	

Field	Bits	Typ	Description
WPA	[1:0]	rh	Write Protection Activated 01 _B Short notation WPA = 1. The write protection of the flash memory is activated. 10 _B Short notation WPA = 0. The write protection is not activated. 00 _B Illegal state. 11 _B Illegal state. Both illegal states have the same effect as "01". This state can only be left by an Application Reset. This field is only changed by the IMB Core. Software writes are ignored.
RPA	[3:2]	rh	Read Protection Activated 01 _B Short notation RPA = 1. The read protection of the flash memory is activated. 10 _B Short notation RPA = 0. The read protection is not activated. 00 _B Illegal state. 11 _B Illegal state. Both illegal states have the same effect as "01". This state can only be left by an Application Reset. This field is only changed by the IMB Core. Software writes are ignored.
WSFLE	[5:4]	rh	Wait State Flash Extension Shows active flash read timing, which can be changed by Change Read Timing . The resulting wait cycles are: $N_{WS} = WSFLASH + 2 \cdot WSFLE$. <i>Note: Attention: the startup value can be influenced with STMEM0 (see startup chapter). Its default value after startup is 0.</i>

Memory Organization

Field	Bits	Typ	Description
PSPROT	[15:8]	rw	PSRAM Write Protection This 8-bit field determines the address up to which the PSRAM is write protected. The start address of the writable range is $E0'0000_H + 1000_H * PSPROT$. The end address is determined by the implemented memory. The equivalent range in the PSRAM area with flash access timing is protected as well. Here the writable range starts at $E8'0000_H + 1000_H * PSPROT$. So with $PSPROT=00_H$ the complete PSRAM is writable.
0	[7:6]	r	Reserved Read as 0, should be written 0

Interrupt Control

Interrupt control and status.

Reset by Application Reset.

IMB_INTCTR

Interrupt Control

ISFR (FF FF04_H)

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ISR	PSE R		0		PSE RCL R	ISET	ICLR		0			DPR OTR P	DDD TRP	DIDT RP	IEN
rh	rh		rw		w	w	w		rw			rw	rw	rw	rw

Field	Bits	Typ	Description
IEN	0	rw	Interrupt Enable If set, the interrupt signal of the IMB gets activated when ISR is set.
DIDTRP	1	rw	Disable Instruction Fetch Double Bit Error Trap If set, a double bit ECC error does not cause the replacement of the fetched data by a trap instruction. See also IMB_ECC_TRAP .DITRPx.

Memory Organization

Field	Bits	Type	Description
DDTRP	2	rw	Disable Data Read Double Bit Error Trap If set, a double bit ECC error during data read does not send a "Flash Access Error" request to the SCU, i.e. no HW trap is generated and the read data is not replaced with default data. The error flags are still set in <code>IMB_FSR_PROT</code> and <code>IMB_ECC_STAT</code> . See also IMB_ECC_TRAP .DDTRPx.
DPROTRP	3	rw	Disable Protection Trap If set, a read request from read protected flash memory does not generate a "Flash Access Error" request to the SCU, i.e. no HW trap is generated.
ICLR	8	w	Interrupt Clear When written with 1 the ISR is cleared. Reading this bit delivers always 0. Writing a 0 is ignored.
ISSET	9	w	Interrupt Set When written with 1 the ISR is set and if IEN is set the interrupt signal is activated. Reading this bit delivers always 0. Writing a 0 is ignored.
PSERCLR	10	w	Clear PSRAM Error Flag When written with 1 the PSER is cleared. Reading this bit delivers always 0. Writing a 0 is ignored.
PSER	14	rh	PSRAM Error Flag This flag is set when write requests to the write protected or not implemented PSRAM range are detected. This flag can be cleared by writing 1 to PSERCLR.
ISR	15	rh	Interrupt Service Request If set, it indicates that at least one <code>IMB_FSR_BUSY.BUSY</code> bit changed from 1 to 0. If IEN was set an interrupt request is sent to the interrupt controller. After servicing the interrupt the software handler clears this flag by writing a 1 to ICLR.
0	[13:11] ,[7:4]	r	Reserved Read as 0, should be written 0

Flash State

Flash state. Split into 3 registers IMB_FSR_BUSY, IMB_FSR_OP, and IMB_FSR_PROT. The protection relevant fields of IMB_FSR_PROT are described in [“Protection Handling Details” on Page 3-45](#).

The registers are reset by the Application Reset with the exception of “ERASE”, “PROG”, and “OPER”. These three fields are only reset by a Power-On Reset.

IMB_FSR_BUSY

Flash State Busy

ISFR (FF FF06_H)

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	PAG E4	PAG E3	PAG E2	PAG E1	PAG E0	0	0	0	BUS Y4	BUS Y3	BUS Y2	BUS Y1	BUS Y0
r	r	r	rh	rh	rh	rh	rh	r	r	r	rh	rh	rh	rh	rh

Field	Bits	Typ	Description
BUSY0	0	rh	Busy Flash 0 Flash module 0 is busy with a task. The task is indicated by the bits MAR, POWER, ERASE or PROG of IMB_FSR_OP. BUSY0 is automatically cleared when the task has finished. The corresponding task indication is not cleared in order to allow an interrupt handler to determine the finished task.
BUSY1	1	rh	Busy Flash 1 Same as BUSY0 for flash module 1.
BUSY2	2	rh	Busy Flash 2 Same as BUSY0 for flash module 2.
BUSY3	3	rh	Busy Flash 3 Same as BUSY0 for flash module 3.
BUSY4	4	rh	Busy Flash 4 Same as BUSY0 for flash module 4.
PAGE0	8	rh	Page Mode Indication Flash 0 Set as long the flash module 0 is in page mode. Page mode is entered by the “Enter Page Mode” commands and finished by a “Program Page” command. The page mode can be also left by a “Reset to Read” command. Also an Application Reset clears this bit.

Memory Organization

Field	Bits	Typ	Description
PAGE1	9	rh	Page Mode Indication Flash 1 Same as PAGE0 for flash module 1.
PAGE2	10	rh	Page Mode Indication Flash 2 Same as PAGE0 for flash module 2.
PAGE3	11	rh	Page Mode Indication Flash 3 Same as PAGE0 for flash module 3.
PAGE4	12	rh	Page Mode Indication Flash 4 Same as PAGE0 for flash module 4.
0	15,7	r	Reserved Read as 0, should be written 0

IMB_FSR_OP

Flash State Operations

ISFR (FF FF08_H)

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0										OP	SQ	MAR	POW	ERA	PRO
										R	R		ER	SE	G
										rh	rh	rh	rh	rh	rh

Field	Bits	Typ	Description
PROG	0	rh	Program Task Indication This bit is set when a program task is started. The affected flash module is indicated by a BUSY bit. The PROG bit is not automatically reset but must be cleared by a “ Clear Status ” command. This bit is not cleared by an Application Reset but only by a Power-On Reset.
ERASE	1	rh	Erase Task Indication This bit is set when an erase task is started. The affected flash module is indicated by a BUSY bit. The ERASE bit is not automatically reset but must be cleared by a “ Clear Status ” command. This bit is not cleared by an Application Reset but only by a Power-On Reset.

Memory Organization

Field	Bits	Typ	Description
POWER	2	rh	Power Change Indication This bit indicates that a flash module is in its startup phase or in a shutdown phase. The BUSY bits indicate which flash module is busy. This bit is not automatically reset but must be cleared by a “ Clear Status ” command.
MAR	3	rh	Margin Change Indication If a read margin modification is requested this bit is set together with the corresponding BUSY bit. The BUSY bit is cleared when the margin change is effective and the flash module can be read again. The MAR bit must be cleared by a “ Clear Status ” command.
SQER	4	rh	Sequence Error This bit is set by a errored command sequence or a command that is not accepted. It is cleared by “ Clear Status ” and “ Reset to Read ”.
OPER	5	rh	Operation Error The IMB Core maintains internal bits that are set when starting a program or erase process. They are cleared when this process finishes. These bits are not reset by an Application Reset but only by a Power-On Reset. If one of these bits is set after Application Reset the IMB Core sets OPER. So this signals that a running erase or program process was interrupted by an Application Reset. The OPER is cleared by “ Reset to Read ”, “ Clear Status ” or a Power-On Reset.
0	[15:6]	r	Reserved Read as 0, should be written 0

IMB_FSR_PROT

Flash State Protection

ISFR (FF FF0A_H)

Reset value: x000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RPRO	0	DDB ER	DSB ER	IDBE R	ISBE R	0	0	0	0	0	PRO ER	WPR ODIS	RPR ODIS	PROI NER	PROI N
rh	r	rh	rh	rh	rh	r	r	r	r	r	rh	rh	rh	rh	rh

Field	Bits	Typ	Description
PROIN	0	rh	Flash Protection Installed Modified by the IMB Core. Cleared by Application Reset.
PROINER	1	rh	Flash Protection Installation Error Modified by the IMB Core. Cleared by Application Reset.
RPRODIS	2	rh	Read Protection Disabled The read protection was temporarily disabled with the “ Disable Read Protection ” command. Modified by the IMB Core. Cleared by Application Reset.
WPRODIS	3	rh	Write Protection Disabled The write protection was temporarily disabled with the “ Disable Write Protection ” command. Modified by the IMB Core. Cleared by Application Reset.
PROER	4	rh	Protection Error Set by a violation of the installed protection. Reset by the “ Clear Status ” and “ Reset to Read ” commands or an Application Reset.
ISBER	8	rh	Instruction Fetch Single Bit Error Set if during instruction fetch a single-bit ECC error was detected (and corrected). Reset by “ Clear Status ” or “ Reset to Read ” commands or an Application Reset.
IDBER	9	rh	Instruction Fetch Double Bit Error Set if during instruction fetch a double-bit ECC error was detected (and not corrected). Reset by “ Clear Status ” or “ Reset to Read ” commands or an Application Reset.
DSBER	10	rh	Data Read Single Bit Error Same as ISBER for data reads.
DDBER	11	rh	Data Read Double Bit Error Same as IDBER for data reads.

Memory Organization

Field	Bits	Typ	Description
RPRO	[15:14]	rh	Read Protection Configuration This field is copied by the IMB Core from the corresponding field in the security page 0. After Application Reset read protection is activated. See Table 3-6 and ff for interpreting this and other protection bit fields. 00 _B Invalid. 01 _B Active. 10 _B Inactive. 11 _B Invalid.
0	[13:12] ,[7:5]	r	Reserved Read as 0, should be written 0

Margin Control

Read margin control. Each field corresponds to one flash module. A hard read 0 detects not completely erased cells. These are read as “1”. A hard read 1 detects not completely programmed cells. These are read as “0”. Read margin changes are caused by the command sequence “[Change Read Margin](#)”. The resulting read margin is reflected in this status register.

The command sequences “[Program Page](#)”, “[Erase Sector](#)”, “[Erase Page](#)” and “[Erase Security Page](#)” resets the read margin back to “normal”. The same happens in case of a flash wake-up.

Reset by Application Reset.

IMB_MAR0

Margin Control 0

ISFR (FF FF0C_H)

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	HREAD4			HREAD3			HREAD2			HREAD1			HREAD0		
r	rh			rh			rh			rh			rh		

Field	Bits	Typ	Description
HREAD0	[2:0]	rh	Hard Read 0 Active read margin of flash module 0. 000 _B Normal read. 001 _B Hard read 0. 010 _B Alternate hard read 0 (usually harder than 001 _B). 101 _B Hard read 1. 110 _B Alternate hard read 1 (usually harder than 101 _B). <i>Note: Other settings of the bit field are reserved.</i>
HREAD1	[5:3]	rh	Hard Read 1 Same as HREAD0 for flash module 1.
HREAD2	[8:6]	rh	Hard Read 2 Same as HREAD0 for flash module 2.
HREAD3	[11:9]	rh	Hard Read 3 Same as HREAD0 for flash module 3.
HREAD4	[14:12]	rh	Hard Read 4 Same as HREAD0 for flash module 4.

Protection Configuration

Protection configuration register of each implemented flash module. The logical sector numbering is depicted in [Figure 3-6](#).

Each bit of the PROCONs is related to a logical sector. If it is cleared the write access to the corresponding logical sector (this means to the range of physical sectors) is locked under the conditions that are documented in [“Protection Handling Details” on Page 3-45](#). The PROCON registers are exclusively modified by the IMB Core which copies them from the security page 0.

For flash modules smaller than 256 KB the SsU bits corresponding to the not implemented flash range are reserved and shall be programmed to 0 in the security page.

Reset by Application Reset.

IMB_PROCONx (x=0-4)

Protection Configuration.

ISFR (FF FF10_H+2*x)

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0			S12 U	S11 U	S10 U	S9U	S8U	S7U	S6U	S5U	S4U	S3U	S2U	S1U	S0U
r			rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Typ	Description
SsU (s=0-12)	s	rh	Sector s Unlock 0 _B Logical sector s of flash module x is write-protected. 1 _B Logical sector s of flash module x is not write-protected. <i>Note: In previous device families and the TriCore™ based products these are “lock” bits and not “unlock” bits!</i>
0	[15:13]	r	Reserved Read as 0, should be written 0

ECC Trap Control

ECC trap control register.

Reset by Application Reset.

The register IMB_ECC_TRAP allows to disable the double bit ECC error trap generation for selected flash modules in contrast to IMB_INTCTR which allows to switch this only globally. This selective control enables to operate part of the flash memory as quasi ROM with enabled error traps. But while a flash module is programmed or erased its trap generation can be switched off without affecting the “ROM” modules. Without this facility the traps would have to be globally disabled and the flash driver had to work from SRAM and all interrupts would have to be blocked.

IMB_ECC_TRAP

ECC Trap Control

ISFR (FF FF20_H)

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	DDT RP4	DDT RP3	DDT RP2	DDT RP1	DDT RP0	0	0	0	DITR P4	DITR P3	DITR P2	DITR P1	DITR P0
r	r	r	rw	rw	rw	rw	rw	r	r	r	rw	rw	rw	rw	rw

Field	Bits	Typ	Description
DITRP0	0	rw	Disable Instruction Fetch Double Bit ECC Trap 0 0_B Replacing instructions by a trap code for double bit ECC errors when fetching from flash module 0 is handled globally via IMB_INTCTR.DITRP. 1_B If set, a double bit ECC error does not cause the replacement of the fetched data by a trap instruction for fetches from flash module 0 independent of IMB_INTCTR.DITRP. Additionally IMB_FSR_PROT.ISBER/IDBER are not set for ECC errors from flash module 0.
DITRP1	1	rw	Disable Instruction Fetch Double Bit ECC Trap 1 Same as DITRP0 for flash module 1.
DITRP2	2	rw	Disable Instruction Fetch Double Bit ECC Trap 2 Same as DITRP0 for flash module 2.
DITRP3	3	rw	Disable Instruction Fetch Double Bit ECC Trap 3 Same as DITRP0 for flash module 3.
DITRP4	4	rw	Disable Instruction Fetch Double Bit ECC Trap 4 Same as DITRP0 for flash module 4.
DDTRP0	8	rw	Disable Data Read Double Bit ECC Trap 0 0_B Double bit ECC error trap for data reads from flash module 0 are handled globally via IMB_INTCTR.DDTRP. 1_B Double bit ECC error for data reads from flash module 0 does not trigger the "Flash Access Error" trap independent of IMB_INTCTR.DDTRP. Additionally IMB_FSR_PROT.DSBER/IDBER are not set for ECC errors from flash module 0 and the data from flash memory is delivered not default data. But the bits IMB_ECC_STAT.xBERx are still set for ECC errors.
DDTRP1	9	rw	Disable Data Read Double Bit ECC Trap 1 Same as DDTRP0 for flash module 1.
DDTRP2	10	rw	Disable Data Read Double Bit ECC Trap 2 Same as DDTRP0 for flash module 2.

Memory Organization

Field	Bits	Typ	Description
DDTRP3	11	rw	Disable Data Read Double Bit ECC Trap 3 Same as DDTRP0 for flash module 3.
DDTRP4	12	rw	Disable Data Read Double Bit ECC Trap 4 Same as DDTRP0 for flash module 4.
0	15,7	r	Reserved Read as 0, should be written 0

ECC Status

ECC status register.

Reset by Application Reset.

This register reports ECC data read single and double bit errors selectively per flash module. Each bit can be cleared independently. This enables to use part of the flash memory quasi as "ROM". In this part all errors trigger traps that are handled by a trap handler and trigger typically a reset of the application. However while flash modules are programmed or erased all ECC errors can be handled by a low-level driver without necessarily affecting the complete system.

IMB_ECC_STAT

ECC Status

ISFR (FF FF22_H)

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	DBE R4	DBE R3	DBE R2	DBE R1	DBE R0	0	0	0	SBE R4	SBE R3	SBE R2	SBE R1	SBE R0
r	r	r	rwh	rwh	rwh	rwh	rwh	r	r	r	rwh	rwh	rwh	rwh	rwh

Field	Bits	Typ	Description
SBER0	0	rwh	Data Read Single Bit Error 0 Set when a single bit ECC errors occurs when reading data from flash module 0. Cleared by Application Reset or by writing 1 to this bit.
SBER1	1	rwh	Data Read Single Bit Error 1 Same as SBER0 for flash module 1.
SBER2	2	rwh	Data Read Single Bit Error 2 Same as SBER0 for flash module 2.
SBER3	3	rwh	Data Read Single Bit Error 3 Same as SBER0 for flash module 3.

Memory Organization

Field	Bits	Typ	Description
SBER4	4	rwh	Data Read Single Bit Error 4 Same as SBER0 for flash module 4.
DBER0	8	rwh	Data Read Double Bit Error 0 Set when a double bit ECC errors occurs when reading data from flash module 0. Cleared by Application Reset or by writing 1 to this bit.
DBER1	9	rwh	Data Read Double Bit Error 1 Same as DBER0 for flash module 1.
DBER2	10	rwh	Data Read Double Bit Error 2 Same as DBER0 for flash module 2.
DBER3	11	rwh	Data Read Double Bit Error 3 Same as DBER0 for flash module 3.
DBER4	12	rwh	Data Read Double Bit Error 4 Same as DBER0 for flash module 4.
0	15,7	r	Reserved Read as 0, should be written 0

3.12.2.2 System Control Registers

These registers are used to wakeup and shutdown parts of the memory sub-system.

Note: The register fields named ‘—’ are reserved. They should be written with ‘0’. Read data is unpredictable and should be ignored.

Table 3-10 Registers Address Space

Module	Base Address	End Address	Note
SCU	0000 _H	0FFF _H	SCU Module

Table 3-11 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
MEM_KSCCFG	Memory Kernel Control	F012 _H	Page 3-76
FL_KSCCFG	Flash Kernel Control	FE22 _H	Page 3-77

Memory Kernel Configuration

This register controls the shutdown request of the processor sub-system units DMU, PMU, IMB and EBC. The layout of this register is identical to the other KSCCFGs but only the field COMCFG may be used. Two values of this field might be used: 00_B means that the “Clock-off Mode” does not trigger a shutdown of the processor sub-system. This may be used only if the system clock of DMP_1 is not disabled in the “Clock-off Mode”.

The second useful value is 10_B. This value must be used in all cases when the “Clock-off Mode” is accompanied by disabling the system clock of the DMP_1.

This register is reset by an Application Reset. **Attention:** the reset value of COMCFG is 00_B.

The access to this register is controlled by the register security mechanism (“Sec” type).

MEM_KSCCFG

Memory Kernel State Con **ESFR (F012_H/06_H)** **Reset Value: 0001_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BPC OM	0	COMCFG							0						1
w	r	rw							r						rw

Field	Bits	Type	Description
COMCFG	[13:12]	rw	Clock Off Mode Configuration This bit field defines if the shutdown request is activated in clock-off mode. If COMCFG[13] is 1 the shutdown request is activated in clock-off mode (i.e. CR = 10). COMCFG[12] has no functionality.
BPCOM	15	w	Bit Protection for COMCFG This bit enables the write access to the bit field COMCFG. It always reads 0. It is only active during the write access cycle. 0 _B The bit field COMCFG is not changed. 1 _B The bit field COMCFG is updated with the written value.
0	14, [11:1]	r	Reserved Read as 0, should be written 0
1	0	rw	Has to be written to 1.

Flash Kernel Configuration

This register controls the power-down request of the flash module. When configuring this register care must be taken not to enable a powered-down flash module when the operating voltage is not sufficient. In this case all CFG fields should contain 10_B.

This register is reset by an Application Reset.

The access to this register is controlled by the register security mechanism ("Sec" type).

FL_KSCCFG

Flash Kernel State Con.

SFR (FE22_H/11_H)

Reset Value: 0001_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BPCOM	0	COMCFG	BPSUM	0	SUMCFG	BPNOM	0	NOMCFG	0	BPMODEN	MODEN				
w	r	rw	w	r	rw	w	r	rw		r	w	rw			

Field	Bits	Type	Description
MODEN	0	rw	Module Enable This bit can directly set the power-down request. 0 _B The power-down request is activated. 1 _B This field has no effect.
BPMODEN	1	w	Bit Protection for MODEN This bit enables the write access to the bit MODEN. It always reads 0. It is only active during the write access cycle. 0 _B The bit MODEN is not changed. 1 _B The bit MODEN is updated with the written value.
NOMCFG	[5:4]	rw	Normal Operation Mode Configuration This bit field defines if the power-down request is activated in normal operation mode. If NOMCFG[5] is 1 the power-down request is activated in normal mode (i.e. CR = 00 or 11). NOMCFG[4] has no functionality.
BPNO	7	w	Bit Protection for NOMCFG This bit enables the write access to the bit field NOMCFG. It always reads 0. It is only active during the write access cycle. 0 _B The bit field NOMCFG is not changed. 1 _B The bit field NOMCFG is updated with the written value.
SUMCFG	[9:8]	rw	Suspend Mode Configuration This bit field defines if the power-down request is activated in suspend mode (which makes only sense if it is activated in normal mode as well). If SUMCFG[9] is 1 the power-down request is activated in shutdown mode (i.e. CR = 01). SUMCFG[8] has no functionality.
BPSUM	11	w	Bit Protection for SUMCFG This bit enables the write access to the bit field SUMCFG. It always reads 0. It is only active during the write access cycle. 0 _B The bit field SUMCFG is not changed. 1 _B The bit field SUMCFG is updated with the written value.

Memory Organization

Field	Bits	Type	Description
COMCFG	[13:12]	rw	Clock Off Mode Configuration This bit field defines if the power-down request is activated in clock-off mode. If COMCFG[13] is 1 the power-down request is activated in clock-off mode (i.e. CR = 10). COMCFG[12] has no functionality.
BPCOM	15	w	Bit Protection for COMCFG This bit enables the write access to the bit field COMCFG. It always reads 0. It is only active during the write access cycle. 0 _B The bit field COMCFG is not changed. 1 _B The bit field COMCFG is updated with the written value.
0	14,10, 6,[3:2]	r	Reserved Read as 0, should be written 0

3.12.3 Startup, Shutdown

The startup and shutdown of memories and the processor sub-system is described in the Programmer's Guide. Also the use of the Kernel Control registers is described there.

3.12.4 Error Reporting Summary

The **Table 3-12** summarizes the types of detected errors and the possible reactions.

Table 3-12 IMB Error Reporting

Error	Reaction
Data read from PSRAM with parity error.	If PECON.PEENPS: HW trap (see Section 9.14.2).
Instruction fetch from PSRAM with parity error.	If PECON.PEENPS: HW trap (see Section 9.14.2).
Data read from flash memory with single bit error.	Silently corrected. Bit IMB_FSR_PROT.DSBER set.
Data read from flash memory with double bit error.	Bit IMB_FSR_PROT.DDBER set. If IMB_INTCTR.DDDTRP = 0: Flash access trap ¹⁾ and default data is delivered.
Instruction fetch from flash memory with single bit error.	Silently corrected. Bit IMB_FSR_PROT.ISBER set.
Instruction fetch from flash memory with double bit error.	Bit IMB_FSR_PROT.IDBER set. If IMB_INTCTR.DIDTRP = 0: "TRAP 15 _D " delivered instead of corrupted data.
Data read from protected flash memory.	IMB_FSR_PROT.PROER set. If IMB_INTCTR.DPROTRP = 0: Flash access trap ¹⁾ and default data is delivered.
Instruction fetch from protected flash memory.	"TRAP 15 _D " delivered.
Program/erase request of write protected flash range.	Only bit PROER in IMB_FSR_PROT set.
Data read or instruction fetch from busy flash memory.	Read access stalled until end of busy state.
Instruction fetch from ISFR addresses.	Default data ("TRAP 15 _D ") delivered.
Data read from not implemented ISFRs.	Default data delivered.
Data writes to not implemented ISFRs.	Silently ignored.
Data read from not implemented address range.	Unpredictable. Mirrored data from other memories might be returned or default values.

Table 3-12 IMB Error Reporting (cont'd)

Error	Reaction
Instruction fetch from not implemented address range.	Unpredictable. Mirrored data from other memories might be returned or default values.
Data written to not implemented PSRAM or write protected PSRAM address range (both determined by IMB_IMBCTRH.PSPROT).	Bit IMB_INTCTR.PSER set. Flash access trap ¹⁾ and no data is changed in the PSRAM.
Program or erase command targeting not implemented flash memory.	Unpredictable. Access is ignored ²⁾ or mirrored into implemented flash memory ³⁾ .
Data read from powered-down flash modules.	Considered as access to not-implemented memory range. Default data or data from implemented flash modules will be returned.
Instruction fetch from powered-down flash modules.	Considered as access to not-implemented memory range. Default data ("TRAP 15 _D ") will be returned or data from implemented flash modules.
Program or erase command targeting powered-down flash modules.	Silently ignored ²⁾ .
Shutdown or power-down request received while the command sequence interpreter is waiting for the last words of a command sequence.	The command interpreter is reset and a "Reset to Read" command sequence is executed.

1) More information about the Flash Access Trap can be found in chapter "SCU".

2) Attention: when an access (i.e. MOV) is ignored, the command sequence interpreter will still wait for this outstanding MOV. So the next command sequence might cause a SQER because it delivers an unexpected MOV.

3) The flash protection can not be by-passed by accessing the reserved memory ranges.

3.13 Data Retention Memories

This section describes the usage of the special purpose data memories Standby RAM (SBRAM) and Marker Memory (MKMEM). Depending on the device not all of them are available. The XC27x8X contains:

- SBRAM.
- MKMEM.

Both are supplied by the wake-up power domain (DMP_M) and retain their data while the system power domain (DMP_1) is switched off.

3.13.1 Standby RAM Accesses

The SBRAM is not mapped into the address range of the processor. All accesses are done via the 4 SFRs SBRAM_WADD, SBRAM_RADD, SBRAM_DATA0 and SBRAM_DATA1. The following access options exist:

- Write without automatic increment of the write address pointer:
The software has to write the target address first to WADD and then the data to DATA0. The data written to DATA0 is transferred to the indicated address in the SBRAM if (at least) the lower byte of DATA0 is written. If DATA0 is written again the same address in SBRAM is used for data storage. Bit WADD.MOD is cleared by a write access to DATA0.
- Write with automatic increment of the write address pointer:
The software has to write the first target address to WADD and thereafter the data block can be written word by word to DATA1. The data written to DATA1 is transferred to the indicated address in the SBRAM if (at least) the lower byte of SRDR1 is written. In parallel to the data storage in the SBRAM, the write address pointer WADD.WPTR is automatically incremented by 1 (one word) for the next data to be stored. The address pointer automatically does a wrap-around after reaching its maximum value and in this case, bit WADD.WA is set. Bit WADD.MOD is set by a write access to DATA1.
- Read without automatic increment of the read address pointer:
The software has to write the target address first to RADD and then can read the data from DATA0. If DATA0 is read again the same address in SBRAM is read out. Bit RADD.MOD is cleared by a read access to DATA0.
- Read with automatic increment of the read address pointer:
The SW has to write the first target address to RADD and can then read the data block word by word from DATA1. In parallel to the read action from SBRAM, the read address pointer RADD.RPTR is automatically incremented by 1 (one word) for the next data to be read. The address pointer automatically does a wrap-around after reaching its maximum value and in this case, bit RADD.WA is set. Bit RADD.MOD is set by a read access to DATA1.

The automatic increment accesses allow performing back-to-back data writes and reads.

Memory Organization

Note: Because read accesses to SBRAM_DATA0 and SBRAM_DATA1 return the value that has been pre-read upon the most recent update of register SBRAM_RADD, any data written to location @SBRAM_RADD can only be read back after SBRAM_RADD has been updated with the very same address (either explicitly by writing to it or implicitly via the auto-increment function). Generally when switching from write to read accesses SBRAM_RADD should be written again before reading SBRAM_DATAx.

Note: Because of this pre-reading feature and the auto-increment behavior it is important to initialize always the address following the last data in order to prevent parity/ECC errors due to this pre-reading.

3.13.2 Standby RAM Registers

This section describes the SBRAM register interface in detail.

Table 3-13 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
SBRAM_RADD	SBRAM Read Address	FEDC _H	Page 3-85
SBRAM_WADD	SBRAM Write Address	FEDE _H	Page 3-86
SBRAM_DATA0	SBRAM Data Register 0	FEE0 _H	Page 3-88
SBRAM_DATA1	SBRAM Data Register 1	FEE2 _H	Page 3-89

3.13.2.1 SBRAM Read Address Register

This register defines the word location to be read.

Reset by Power-On Reset.

SBRAM_RADD

SBRAM Read Address Register SFR (FEDC_H/6E_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOD	WA	0	RPTR												0
rwh	rwh	r	rwh												r

Field	Bits	Type	Description
RPTR	[12:1]	rwh	Read Pointer Selects the word address to be read from the SBRAM. It is automatically incremented by 1 (i.e. to the next word) when register DATA1 is read.
WA	14	rwh	Wrap Around This bit indicates if a wrap-around of the read pointer RPTR occurred due to the automatic address increment. 0 _B An address wrap-around has not occurred. 1 _B An address wrap-around has been detected. It has to be cleared by software.

Memory Organization

Field	Bits	Type	Description
MOD	15	rwh	Modification This bit indicates whether the last read access to SBRAM data lead to an automatic increment of RPTR. 0_B The last data read access was done to DATA0 and RPTR was not modified automatically. 1_B The last data read access was done to DATA1 and RPTR was automatically incremented by 1.
0	0, 13	r	Reserved Read as 0; should be written with 0.

3.13.2.2 SBRAM Write Address Register

This register defines the word location to be written.

Reset by Power-On Reset.

SBRAM_WADD

SBRAM Write Address Register SFR (FEDE_H/6F_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOD	WA	0													0
rwh	rwh	r													r

Field	Bits	Type	Description
WPTR	[12:1]	rwh	Write Pointer Selects the write word address within the SBRAM. It is automatically incremented by 1 when register DATA1 is written.
WA	14	rwh	Wrap-Around This bit indicates if a wrap-around of the write pointer WPTR occurred due to the automatic address increment. 0_B An address wrap-around has not occurred. 1_B An address wrap-around has been detected. It has to be cleared by software.

Memory Organization

Field	Bits	Type	Description
MOD	15	rwh	Modification This bit indicates whether the last write access to SBRAM data lead to an automatic increment of WPTR. 0_B The last data write access was done to DATA0 and WPTR was not modified automatically. 1_B The last data write access was done to DATA1 and WPTR was automatically incremented by 1.
0	0, 13	r	Reserved Read as 0; should be written with 0.

3.13.2.3 SBRAM Data Register 0

This register delivers the read data and is the target for the write data without modification of the respective address pointer.

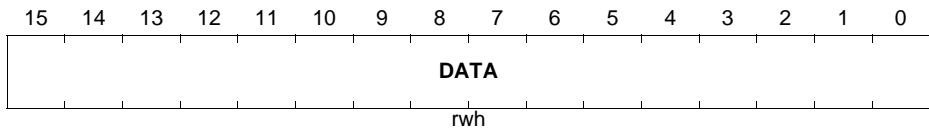
Reset by Power-On Reset.

SBRAM_DATA0

SBRAM Data Register 0

SFR (FEE0_H/70_H)

Reset Value: 0000_H



Field	Bits	Type	Description
DATA	[15:0]	rwh	SBRAM Data This bit field contains the data read during the latest SBRAM read access and is the target for the data to be written to SBRAM. A read access always delivers the data stored in the SBRAM at the address indicated by the read pointer RADD.RPTR. A write access of (at least) the low byte leads to the storage of the written data at the address indicated by the write pointer WADD.WPTR.

3.13.2.4 SBRAM Data Register 1

This register delivers the read data and is the target for the write data with modification of the respective pointer.

Reset by Power-On Reset.

SBRAM_DATA1

SBRAM Data Register 1

SFR (FEE2_H/71_H)

Reset Value: 0000_H



Field	Bits	Type	Description
DATA	[15:0]	rwh	SBRAM Data This bit field contains the data read during the latest SBRAM read access and is the target for the data to be written to SBRAM. A read access always delivers the data stored in the SBRAM at the address indicated by the read pointer RADD.RPTR. A write access of (at least) the low byte leads to the storage of the written data at the address indicated by the write pointer WADD.WPTR.

4 Memory Checker Module (MCHK)

The memory checker module (MCHK) of the XC27x8X supports checking the data consistency of memories, registers (e.g. configuration registers), or communication channels. It calculates a checksum on a block of data, often called cyclic redundancy code (CRC). It is implemented as a parallel signature generation based on a multi input linear feedback shift register (MISR). Being based on a linear feedback shift register (LFSR), it also can generate pseudo-random numbers and cyclic codes.

This chapter is structured as follows:

- An operational overview of the Memory Checker Module (see [Section 4.1](#))
- Functional description of the Memory Checker Module (see [Section 4.2](#))
- Description of the Memory Checker Module registers (see [Section 4.3](#))
- Interfaces of the Memory Checker Module (see [Section 4.4](#))

4.1 Operational Overview

From the programmer's point of view, the MCHK is a set of registers associated with this peripheral. To communicate respective error or operation events a port pin may be used for the signal "MATCH" to generate an external event and an interrupt line may be used for the signal "MISMATCH" to generate an internal event. The MCHK is reset together with the CPU so it can be used as a CPU coprocessor. This ensures a deterministic state of the MCHK after the CPU exits the reset state.

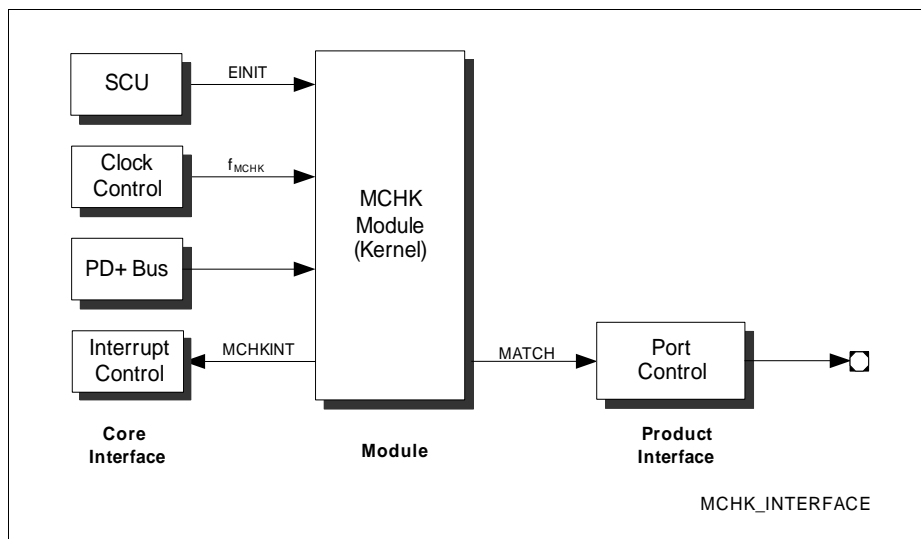


Figure 4-1 Interface Diagram

Note: The MATCH output is connected to an external port in packaged devices with 144 or more pins only.

4.2 Functional Description

Conventional digital processing systems generally are configured around volatile and non-volatile memory elements. These memories provide (store) the data and instructions to the CPU doing the main computing of an embedded system. This includes the administration of the system by coordinating the operation of various system units to perform system tasks.

Faults within these memories are in general critical for the safety and reliability of an embedded system. Therefore these memories have mechanisms to check for data consistency, e.g. parity or ECC (error correction code). These mechanisms can detect faults up to a certain amount (e.g. double bit faults) per word (bit line faults). Concatenated codes (block codes, word codes) can also detect multibit faults per word (word line faults), which increases the fault coverage.

The MCHK is a parallel signature compression circuitry that calculates a concatenated CRC block code to increase test coverage by code concatenation. This enables error detection within a block of data stored in memory, registers, or communicated e.g. via serial communication lines. The MCHK reduces the probability of error masking due to repeated error patterns by compressing parallel test inputs from a block of data to be tested. Furthermore, it can generate pseudo random numbers.

The MCHK uses a multiple input linear feedback shift register to generate a checksum (signature) of a block of data. A multiple input linear feedback shift register (MISR) is a shift register whose internal feedback input bit is driven by the exclusive-or (XOR) of some bits of the overall shift register value (LFSR: linear feedback shift register).

This generator includes an arithmetic circuitry to calculate the block code. This circuitry is implemented as an independent piece of hardware and, therefore, does not rely on the memories to be tested. Only for the configuration it requires initialization data out of the memories. To avoid the need of a multi master system (CPU, DMA, etc.), the CPU (e.g. PEC, subroutine) is used to handle the data read and write transactions. These transactions rely on the memories to be tested because they may contain the respective CPU instruction code. Therefore the MCHK implements additional measures to enable detection of erroneous data move operations by the CPU.

The following error scenarios are detected:

- The CPU configures the MCHK erroneously
- The CPU does not provide the data from the respective address range
- The CPU does not provide the correct amount of data
- The CPU is not able to check correctly the match of the online generated CRC block code and the expected offline (during development) generated CRC block code

The principle of this circuitry is to generate an external coded life signal of the CRC block code check. Furthermore the configuration of the circuitry cannot be changed without an external notification. The life signal is not a static signal, but changes polarity in a predefined manner to avoid static faults, e.g. open and short circuit in the output stages.

Memory Checker Module (MCHK)

The circuitry consists of the following components:

- An arithmetic circuitry calculating the CRC block code out of the data transferred into an input register of this circuitry.
- A compare unit to check if the value of the calculated CRC block code is correct. The MCHK compares the content of the CRC block code result registers to a fixed value (FADE'EDDA_H). Before calculating a CRC value, the result register is initialized with a specific value (magic word, seed), which results in a specific value after the CRC calculation. This so called magic word must be selected in a way that the block code ends up with the fixed value (FADE'EDDA_H). This works fine for linear code, e.g. the CRC block code.
- A method granting the CRC block code calculation over a given amount of data. Therefore functional redundancy is used to grant this. A local count register within the MCHK initiates the compare of the calculated CRC block code after a given amount of input data. Secondly the CPU reloads the magic word (seed) of the CRC block code when initiating a new CRC block code generation (loop variable within data move subroutine or count register within PEC).
- An internal service request generation to enable software recovery in case of a fault. This could be a software routine running out of a different flash block than the one that produced the error, e.g. to support a limb home function. There is a residual risk: The CPU could write dummy data into the memory checker within this error interrupt routine and then rewrite the COUNT register.
- All configuration registers are protected by a time redundant mechanism. So modifications of configuration registers are only possible following a specific sequence of write operations (EINIT protected). Additionally, the COUNT register is protected by a content dependent access scheme.
- An external MATCH signal is generated on every successful CRC block code generation and may be used to trigger an external window watchdog. This window watchdog may generate a reset in case too many or too few MATCH signal toggles fall into a specific time window. To grant a correctly working block code unit, the application must also perform from time to time a block code generation outside the watchdog time window by having an incorrect compare (no MATCH signal toggle). This will check the correct function of the compare circuitry, because in case of an erroneous compare circuitry a MATCH signal toggle is generated outside the watchdog time window.

4.2.1 Principle of the LFSR

The list of the bit positions that affect the internal feedback bit is called the tap sequence. **Figure 4-2** shows the principle of an LFSR. It assumes a tap sequence of [32, 26, 23, 22, 16, 12, 11, 10, 8, 7, 5, 4, 2, 1]. On activation, all bits in the LFSR are shifted left one bit position (in direction of the most significant bit). All bits on the tap position are exclusive-ORed and the result is fed into bit 0 as a feedback. On the next activation the same procedure is repeated.

The LFSR outputs that influence the internal feedback input are called taps (marked gray in **Figure 4-2**).

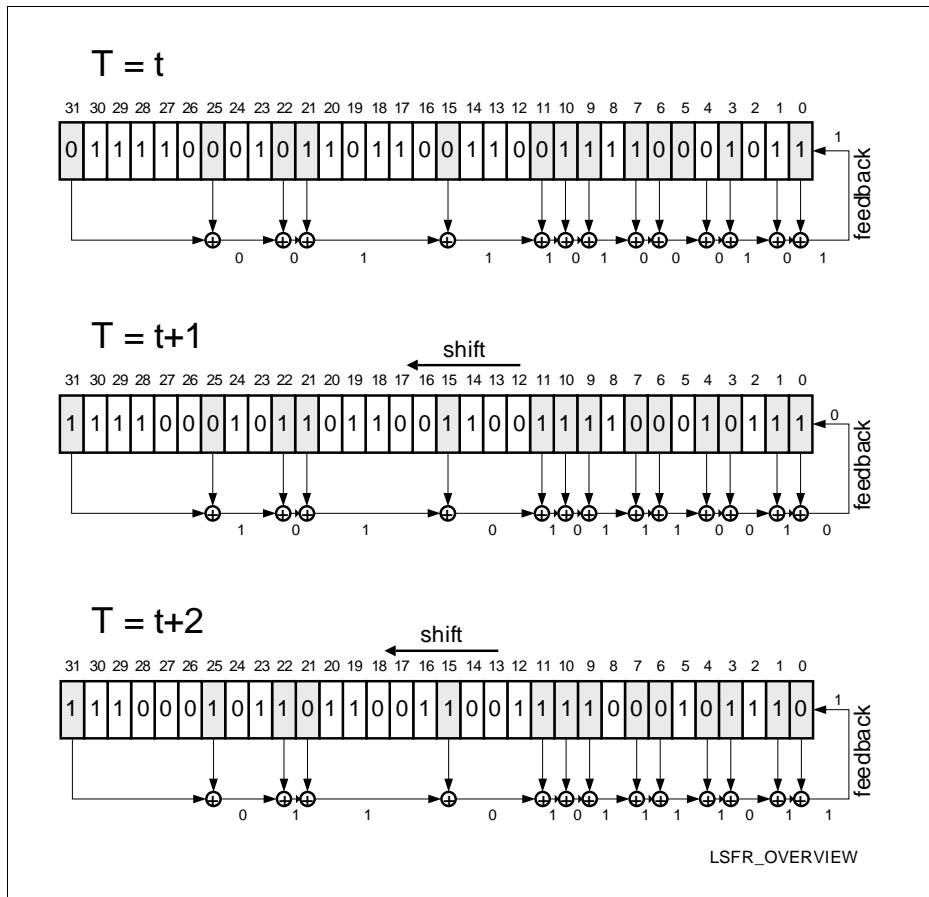


Figure 4-2 Principle of an LFSR

Memory Checker Module (MCHK)

The tap sequence of an LFSR can be represented as a polynomial mod 2. This means that the coefficients of the polynomial must be 0 in case a respective feedback is not implemented or 1 in case a feedback tap is implemented. This is called the feedback polynomial or characteristic polynomial. For example, if the taps are at the 32nd, 26th, 23rd, 22nd, 16th, 12th, 11th, 10th, 8th, 7th, 5th, 4th, and the 2nd bits (as below), the resulting LFSR polynomial is

$$G^{32} = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1 \quad (4.1)$$

The '+1' in the polynomial does not correspond to a tap. The powers of the terms represent the tapped bits, counting from the least significant bit. The polynomial may be represented by a binary number (binary representation). Every power of the terms represent a 1 in the binary format counting from the most significant bit. So for the polynomial listed above, the number would be:

$$G^{32} = 1000\ 0010\ 0110\ 0000\ 1000\ 1110\ 1101\ 1011_B = 8260'8EDB_H$$

The polynomial used by the MCHK is defined in the tap polynomial registers **TPRH** and **TPRL**.

4.2.2 Principle of the MISR

In parallel to the internal feedback input bit of the LFSR, 16 external bits may be loaded into the LFSR (multiple input).

These 16 input bits are exclusive-ORed with the bits shifted or fed back in the LFSR.

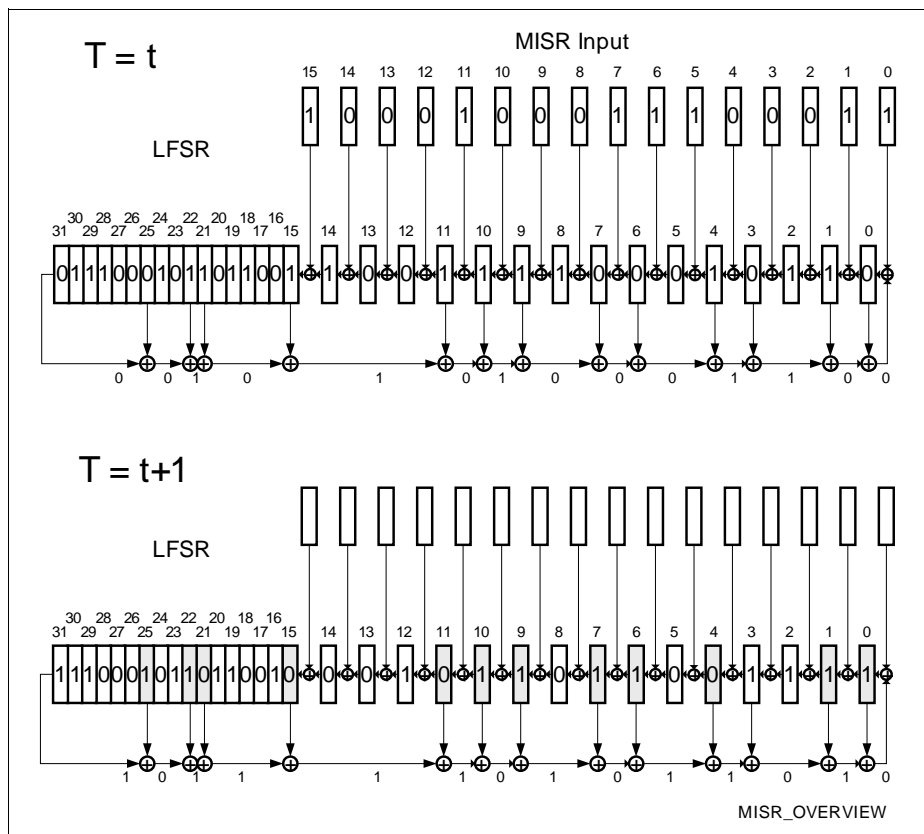


Figure 4-3 Principle of a MISR

The initial value of the LFSR/MISR is called the seed and may be defined by an initial write to the result registers **RRL** and **RRH**. Because the operation of the MISR is deterministic, the sequence of values produced by the MISR is completely determined by its current (or previous) states and inputs.

4.2.3 Commonly used Polynomials

Polynomials for cyclic codes as used in globally standardized systems have not been fully standardized themselves. Most cyclic codes in current use have some weakness with respect to strength or construction. Standardization of cyclic codes would allow for better designed cyclic codes to come into common use. The following table provides a list of common polynomials used for sequential CRC signature generation.

Table 4-1 Some Commonly used Polynomials

Name	Polynomial	Maximum Data Width	Normal (Reverse) of Reciprocal
CRC-8-ATM	x^8+x^2+x+1	8-bit	0000'0083 _H (0000'00C1 _H)
CRC-8-CCITT	$x^8+x^7+x^3+x^2+1$	8-bit	0000'00C6 _H
CRC-8-Dallas	$x^8+x^5+x^4+1$	8-bit	0000'0098 _H
CRC-8	$x^8+x^7+x^6+x^4+x^2+1$	8-bit	0000'00EA _H
CRC-8 SAE J1850	$x^8+x^4+x^3+x^2+1$	8-bit	0000'008E _H
CRC-1 (parity)	$x^8+x^7+x^6+x^5+x^4+x^3+x^2+x+1$	8-bit	0000'00FF _H
CRC-10	$x^{10}+x^9+x^5+x^4+x+1$	10-bit	0000'0319 _H (0000'0263 _H)
CRC-12	$x^{12}+x^{11}+x^3+x^2+x+1$	12-bit	0000'0C07 _H (0000'0E03 _H)
CRC-15-CAN	$x^{15}+x^{14}+x^{10}+x^8+x^7+x^4+x^3+1$	15-bit (13-bit)	0000'62CC _H (0000'19A3 _H)
CRC-1 (parity)	$x^{16}+x^{15}+x^{14}+x^{13}+x^{12}+x^{11}+x^{10}+x^9+x^8+x^7+x^6+x^5+x^4+x^3+x^2+x+1$	16-bit	0000'FFFF _H
CRC-16-CCITT	$x^{16}+x^{12}+x^5+1$	16-bit	0000'8810 _H
CRC-16-IBM	$x^{16}+x^{15}+x^2+1$	16-bit	0000'C002 _H
CRC-24- Radix-64	$x^{24}+x^{23}+x^{18}+x^{17}+x^{14}+x^{11}+x^{10}+x^7+x^6+x^5+x^4+x^3+x+1$	16-bit (24-bit polynomial)	00C3'267D _H (BE64'C300 _H)

Table 4-1 Some Commonly used Polynomials (cont'd)

Name	Polynomial	Maximum Data Width	Normal (Reverse) of Reciprocal
CRC-32-IEEE802.3/MPEG2	$x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^8+x^7+x^5+x^4+x^2+x+1$	16-bit (32-bit polynomial)	8260'8ED6 _H (DB71'0641 _H)
CRC-32C	$x^{32}+x^{28}+x^{27}+x^{26}+x^{25}+x^{23}+x^{22}+x^{20}+x^{19}+x^{18}+x^{14}+x^{13}+x^{11}+x^{10}+x^9+x^8+x^6+1$	16-bit (32/27-bit polynomial)	8F6E'37A0 _H (05EC'76F1 _H)

Note: The polynomials above are in general used for sequential signature generation (in general named as CRC), resulting in different signatures than the parallel signature generation algorithm used by the MCHK.

4.2.4 Architecture of the Memory Checker Module

The LFSR is represented by the Result Register High (**RRH**) and the Result Register Low (**RRL**). These may be used to initialize the MCHK with a seed value. When writing to register RRL, the MISR count register **COUNT** is reloaded with the last value written to register **COUNT**. The result registers **RRH** and **RRL** may be used to read the final or intermediate signature of a block of data loaded into the MCHK.

Data may be loaded into the MCHK by writing either 8-bit or 16-bit data into the MISR input register **IR**. Each write access to register IR decrements the content of the MISR count register **COUNT**.

The polynomial is defined by writing the binary normal reciprocal value into the TAP Polynomial Register High (**TPRH**) and TAP Polynomial Register Low (**TPRL**). The TAP polynomial registers and the result registers are combined by a binary AND. If the amount of ones in the result of this AND operation is odd, a 1_B is fed back, else a 0_B. The effectiveness of the Memory Checker Module is significantly reduced if a polynomial is used with a the most significant 1_B bit position in the TAP Polynomial register being smaller than the most significant 1_B in the data fed into the Memory Checker Module. So in general the content of the TAP polynomial register must be larger than 80_H for 8-bit data and larger than 8000_H for 16-bit data.

If the content of the MISR count register **COUNT** is decremented from 0001_H to 0000_H, a service request signal is generated in case the content of the LFSR result register high (**RRH**) is not equal FADE_H or the content of the LFSR result register low (**RRL**) is not equal EDDA_H. If the content of the LFSR result registers equals FADE'EDDA_H, the external MATCH signal is toggled. **Figure 4-4** summarizes the architecture of the checksum circuit.

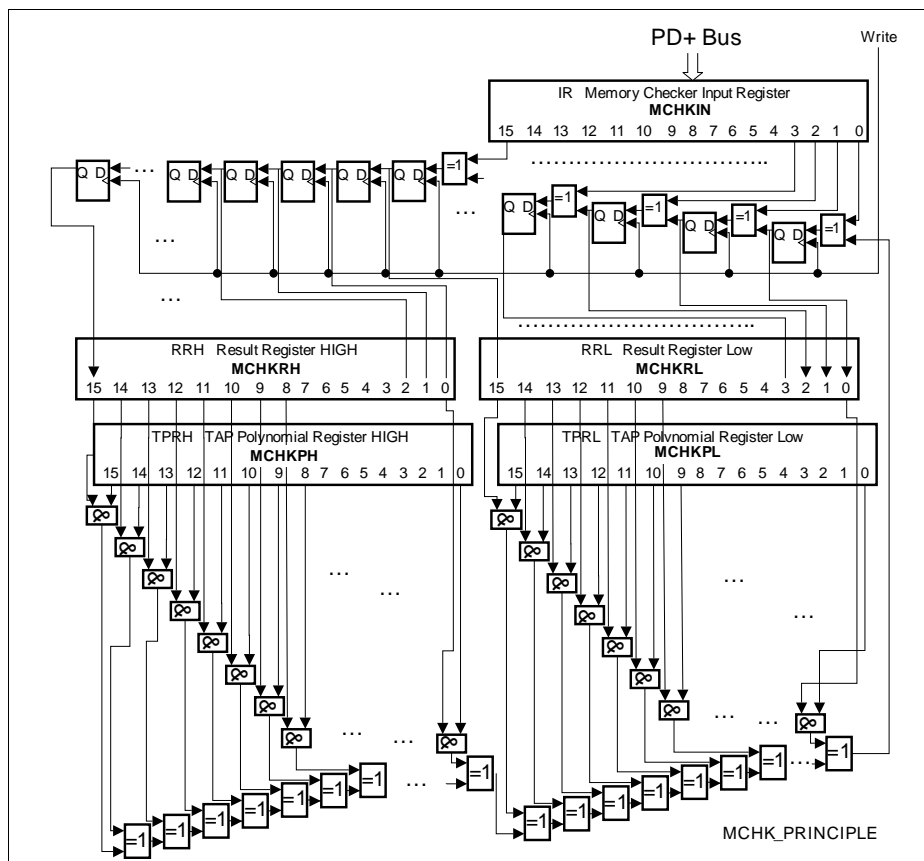


Figure 4-4 Implementation of the MCHK Checksum Circuit

4.2.5 Preferable Usage of the Memory Checker Module

Preferably the MCHK is used together with the CPU. The CPU reads the data block from the selected address area and writes it to the input register **IR**. Alternatively the PEC may be configured to move the data block to input register **IR** using 8-bit or 16-bit moves (PECCx.BWT = 0: 16-bit; PECCx.BWT = 1: 8-bit). Each write operation to register **IR** triggers a intermediate polynomial checksum calculation and the result of the calculation is stored in the result registers **RRL** and **RRH**. Furthermore, every write operation to register **IR** decrements the content of count register **COUNT**.

In order to start a memory check sequence, the result register must be initialized with a seed (e.g. written with the desired start value) and a CPU or PEC transaction must be set up (start address, length, etc.).

When the defined data block is completely written to register **IR**, an interrupt may be generated if the contents of the LFSR result registers **RRH** and **RRL** does not equal FADE'EDDA_H.

The MCHK may use e.g. the standard Ethernet (IEEE802.3/MPEG2) polynomial, which is given by:

$$G^{32} = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1 \quad (4.2)$$

Note: Although the polynomial above is used for generation, the result of the parallel signature generation (MISR) differs from the sequential signature generation (LFSR) used by the Ethernet protocol.

4.2.6 Calculation of Seed Values (Magic Word)

To achieve a successful CRC calculation and MATCH or MISMATCH signal on a block of non volatile data, a data specific seed value, the so called magic word, has to be loaded into the LFSR result registers **RRH** and **RRL** prior to the CRC calculation. This magic word should be calculated during development of the respective data. Such a magic word can only be generated, if the order of the TAP polynomial is equal order 32 (most significant bit of TAP polynomial **TPRH** must be equal 1). Otherwise the higher order bits are non equal to the required end result FADE EDDA_H. The following program sketches the principle of the program. It uses VBA (Microsoft Visual Basic) syntax. The Data_Array contains all the 16-bit data the CRC is to be calculated. COUNT passes the number of data the CRC is to be calculated, to the subroutine, as defined in the Memory Checker count register **COUNT**. The magical word is passed back to the calling routine through **RRH** and **RRL**, as it has to be written into the Result Register High (**RRH**) and the LFSR Result Register Low (**RRL**) as seed value. Because VBA has no unsigned integer format, a long integer format has been used within this demonstration code.

```
Sub MagicWord(ByRef Data_Array() As Long, _
              ByVal COUNT, TPRH, TPRL As Long, _
              ByRef RRH, RRL As Long)
```

Memory Checker Module (MCHK)

```

Dim i, j, order, feedback_bit As Integer
Dim temp As Long
    RRH = &HFADE
    RRL = &HEDDA
For j = COUNT To 1 Step -1
    If TPRH <> 0 Then                ' order of polynomial > 16
        order = 31
        Do While TPRH< 2 ^ (order - 16) ' calculate order of polynomial,
            order = order - 1           ' determines bit position
        Loop                           ' "rolled" out of LFSR
    Else                             ' order of polynomial < 17
        order = 15
        Do While TPRL< 2 ^ order       ' calculate order of polynomial,
            order = order - 1           ' determines bit position
        Loop                           ' "rolled" out of LFSR
    End If
    RRL = RRL Xor Data_Array(j)        ' MISR XOR Input
    feedback_bit = RRL And 1           ' Extract CRC feedback bit
    RRL = RRL \ 2                      ' 32 bit shift right (LFSR)
    RRL = RRL + (RRH And 1) * 2 ^ 15
    RRH = RRH \ 2
    temp = (RRH And TPRH) _
           Xor (RRL And TPRL)         ' generate 32 TAP Bits
For i = 0 To 15
    feedback_bit = feedback_bit _
                 Xor ((temp \ (2 ^ i)) And 1)
Next i                                ' XOR TAP bits to bit
If feedback_bit <> 0 Then              ' TAP feedback bit is equal 1
    If order > 16 Then
        RRH = RRH Or (2 ^ (order - 16))
    Else
        RRL = RRL Xor (2 ^ order)
    End If
End If
Next j                                ' calculate CRC of all data
End Sub

```


4.2.7 Example Application

Assuming MCHK is to be used to detect faults within a set of twenty one 16 bit Data. The Memory Checker Module uses the standard Ethernet (IEEE802.3/MPEG2) polynomial, which is given by:

$$G^{32} = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1 \quad (4.3)$$

The Polynomial is therefore 8260 8EDB_H and is written to **TPRH** and **TPRL**. Next the magical word of this set of data has to be calculated offline using a respective program as described in [Section 4.2.6: "Calculation of Seed Values \(Magic Word\)" on Page 4-11](#). For the given data in [Table 4-2](#), a magical word = AA1F ED4E_H is calculated and written to **RRH** and **RRL**.

Table 4-2 Example for a CRC Check

User Action	Data Value	Content of Register				
		COUNT	RRH	RRL	TPRH	TPRL
TAP Polynomial written to TPRH	8260 _H	xxxx	xxxx	xxxx	8260 _H	xxxx
TAP Polynomial written to TPRL	8EDB _H	xxxx	xxxx	xxxx	8260 _H	8EDB _H
Magical Word written into RRH	AA1F _H	0015 _H	AA1F _H	xxxx	8260 _H	8EDB _H
Magical Word written into RRL	ED4E _H	0015 _H	AA1F _H	ED4E _H	8260 _H	8EDB _H
Data Amount written to COUNT	0015 _H	0015 _H	xxxx	xxxx	8260 _H	8EDB _H
Data 1 written into IR	8BED _H	0014 _H	543F _H	5171 _H	8260 _H	8EDB _H
Data 2 written into IR	AA61 _H	0013 _H	A87E _H	0883 _H	8260 _H	8EDB _H
Data 3 written into IR	C64E _H	0012 _H	50FC _H	D749 _H	8260 _H	8EDB _H
Data 4 written into IR	17E4 _H	0011 _H	A1F9 _H	B976 _H	8260 _H	8EDB _H
Data 5 written into IR	A329 _H	0010 _H	43F3 _H	D1C5 _H	8260 _H	8EDB _H
Data 6 written into IR	66B5 _H	000F _H	87E7 _H	C53E _H	8260 _H	8EDB _H
Data 7 written into IR	422A _H	000E _H	0FCF _H	C857 _H	8260 _H	8EDB _H
Data 8 written into IR	4FF6 _H	000D _H	1F9F _H	DF58 _H	8260 _H	8EDB _H
Data 9 written into IR	4046 _H	000C _H	3F3F _H	FEF6 _H	8260 _H	8EDB _H
Data 10 written into IR	911C _H	000B _H	7E7F _H	6CF0 _H	8260 _H	8EDB _H
Data 11 written into IR	1FA0 _H	000A _H	FCFE _H	C640 _H	8260 _H	8EDB _H

Memory Checker Module (MCHK)

Table 4-2 Example for a CRC Check (cont'd)

User Action	Data Value	Content of Register				
		COUNT	RRH	RRL	TPRH	TPRL
Data 12 written into IR	BF38 _H	0009 _H	F9FD _H	33B9 _H	8260 _H	8EDB _H
Data 13 written into IR	9FE3 _H	0008 _H	F3FA _H	F891 _H	8260 _H	8EDB _H
Data 14 written into IR	44DD _H	0007 _H	E7F5 _H	B5FE _H	8260 _H	8EDB _H
Data 15 written into IR	749A _H	0006 _H	CFEB _H	1F67 _H	8260 _H	8EDB _H
Data 16 written into IR	8C09 _H	0005 _H	9FD6 _H	B2C7 _H	8260 _H	8EDB _H
Data 17 written into IR	D0F5 _H	0004 _H	3FAD _H	B57A _H	8260 _H	8EDB _H
Data 18 written into IR	DC5F _H	0003 _H	7F5B _H	B6AB _H	8260 _H	8EDB _H
Data 19 written into IR	DB06 _H	0002 _H	FEB7 _H	B651 _H	8260 _H	8EDB _H
Data 20 written into IR	4604 _H	0001 _H	FD6F _H	2AA7 _H	8260 _H	8EDB _H
Data 21 written into IR	B894 _H	0000 _H	FADE _H	EDDA _H	8260 _H	8EDB _H

Memory Checker Module (MCHK)

4.3 Memory Checker Module Registers

From the programmer's point of view, the MCHK is composed of a set of SFRs as summarized below.

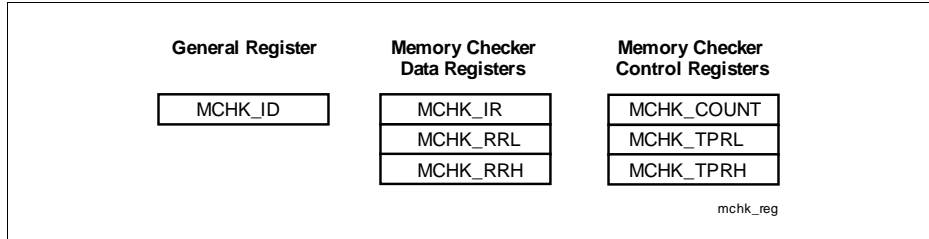


Figure 4-5 Memory Checker Module Kernel Registers

The following tables show the MCHK registers and their addresses.

Table 4-3 Registers Address Space

Module	Base Address	End Address	Note
MCHK	0000 _H	0FFF _H	

Table 4-4 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
ID	Module Identification Register	FFE0 _H	Page 4-16
IR	Input Register	FE58 _H	Page 4-17
RRL	Result Register Low	F058 _H	Page 4-17
RRH	Result Register High	F05A _H	Page 4-18
COUNT	Count Register	FE5A _H	Page 4-20
TPRL	Polynomial Register Low	F05C _H	Page 4-21
TPRH	Polynomial Register High	F05E _H	Page 4-21

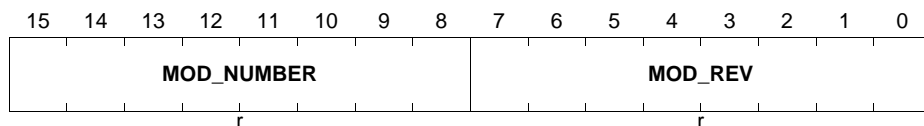
Note: All registers are reset by the same reset class as the CPU is reset.

4.3.1 General Register

The ID register is a read-only register used for MCHK module identification purposes. It provides 8 bits for module identification and 8 bits for revision numbering.

ID

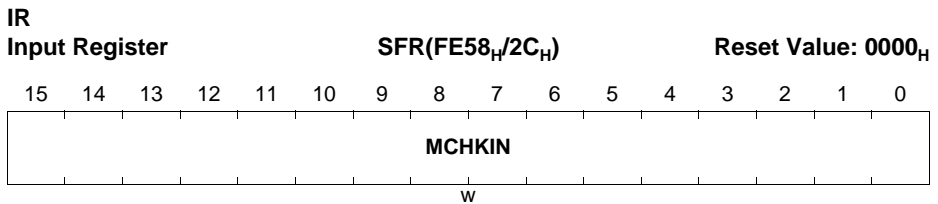
Module Identification Register (FFE0_H) **Reset Value: 3BXX_H**



Field	Bits	Type	Description
MOD_REV	[7:0]	r	Module Revision Number Value Bits 7-0 bits are used for module revision numbering. The value of the module revision number starts with 01 _H (first revision).
MOD_NUMBER	[15:8]	r	Module Identification Number Value Bits 15-8 are used for module identification. The MCHK has the module number 3B _H .

4.3.2 Memory Checker Data Register

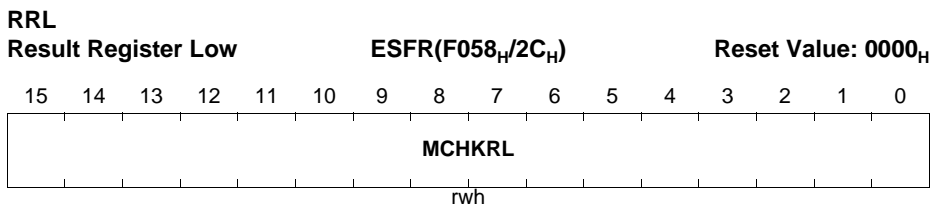
The input register receives the data written to the MCHK for checksum calculation. If the CPU moves to register MCHK_IR are 8-bit wide, the unused register bits of the 16-bit MCHKIN value are taken as 0s for the current result calculation.



Field	Bits	Type	Description
MCHKIN	[15:0]	w	Memory Checker Module Input The value written to MCHKIN is used for the next checksum calculation. Any read action will deliver 0000 _H .

Note: MCHK_IR is a write-only register. Any read action will deliver 0000_H.

The result registers contain the signature (result) of the memory check operation. Before starting a checksum calculation operation, they should be written with the initial checksum calculation value (seed).



Field	Bits	Type	Description
MCHKRL	[15:0]	rwh	Memory Checker Result Low This bit field contains the least significant 16 bits of the current result of the 32-bit checksum calculation operation.

Memory Checker Module (MCHK)

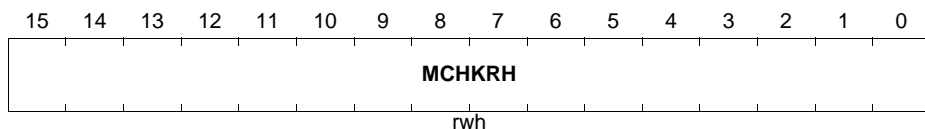
Note: Writing to the RRL.MCHKRL will reset (reload) the MCHKCNT.COUNT register to the last data written to this register MCHKCNT.COUNT value. Therefore writing to RRL will immediately initialize a new CRC calculation cycle.

RRH

Result Register High

ESFR(F05A_H/2D_H)

Reset Value: 0000_H



Field	Bits	Type	Description
MCHKRH	[15:0]	rwh	Memory Checker Result High This bit field contains the most significant 16 bits of the current result of the 32-bit checksum calculation operation.

4.3.3 Memory Checker Control Register

The count register COUNT is decremented on each write access to the input register. If the count register is decremented to 0000_H, a service request (interrupt) is generated if the content of the result registers is non equal FADE'EDDA_H, or instead the output signal MATCH is toggled if the result registers are equal FADE'EDDA_H. The count register is reloaded with the last value written to it, when the CPU transfers a new seed value (magic word) to the LFSR result register low ([RRL](#)).

When the CPU or PEC writes to register COUNT and its content is not equal to the last value written to it, the service request (interrupt) is generated and the output signal MATCH is toggled. This enables detection of software not correctly handling the MCHK, e.g. due to an erroneous program memory. The timely correct toggling of the MATCH signal may be used as a life signal e.g. by an external window watchdog. The reset value of the MATCH signal = 0_B.

Because register COUNT controls a safety critical system function, it is protected by a special register security mechanism so this vital system function cannot be changed inadvertently after executing the EINIT instruction.

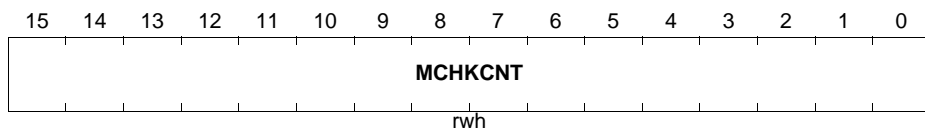
Memory Checker Module (MCHK)

COUNT

Count Register

SFR(FE5A_H/2D_H)

Reset Value: 0000_H



Field	Bits	Type	Description
MCHKCNT	[15:0]	rwh	Memory Checker Count MCHKCNT indicates the number of remaining data in the current data block to be entered into MCHK. 0001 _H One remaining data to be written to register IR to trigger the compare for the MATCH signal, interrupt signal NOMATCH. 0002 _H Two remaining data to be written to register IR FFFE _H 65534 remaining data to be written to register IR . FFFF _H 65535 remaining data to be written to register IR . 0000 _H 65536 remaining data to be written to register IR to trigger the compare for the MATCH signal, interrupt signal NOMATCH.

Note: Register COUNT should only be written if MCHKCNT is equal to the last value written to this register. Otherwise, a service request (interrupt) will be triggered and the MATCH signal will be toggled.

*Modify register COUNT only after writing to register **RRL**, which reloads COUNT to the previously written value (see also **Table 4-2**).*

Note: COUNT is write protected after the execution of EINIT by the register security mechanism.

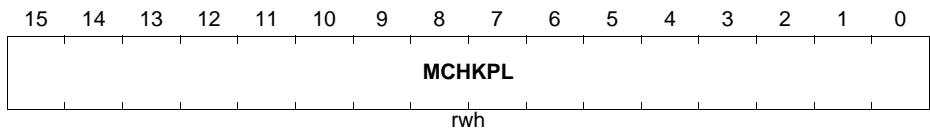
Memory Checker Module (MCHK)

The polynomial registers contain the LFSR polynomial of the checksum calculation operation.

Because the polynomial registers control a safety critical system function, they are protected by a special register security mechanism so this vital system function cannot be changed inadvertently after executing the EINIT instruction.

TPRL

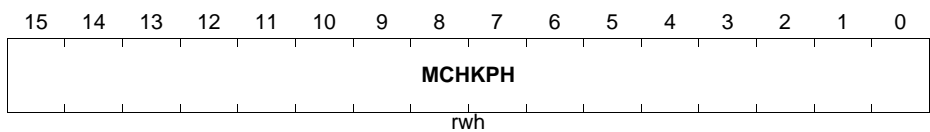
Tap Polynomial Register Low **ESFR(F05C_H/2E_H)** **Reset Value: FFFF_H**



Field	Bits	Type	Description
MCHKPL	[15:0]	rwh	Memory Checker Polynomial Low This bit field contains the least significant 16 bits of the binary tap polynomial format.

TPRH

Tap Polynomial Register High **ESFR(F05E_H/2F_H)** **Reset Value: FFFF_H**



Field	Bits	Type	Description
MCHKPH	[15:0]	rwh	Memory Checker Polynomial High This bit field contains the most significant 16 bits of the binary tap polynomial format.

Note: TPRH and TPRL is write protected after the execution of EINIT by the register security mechanism.

4.4 Interfaces of the MCHK Module

The MCHK module can generate an interrupt request and an external life signal.

The interrupt request signal is connected to the SCU and can be routed to one of the SCU's interrupt nodes.

The MATCH output is connected to an external pin in packaged devices with 144 or more pins only.

Table 4-5 MCHK Digital Connections in XC27x8X

Signal	from/to Module	I/O to MCHK
MATCH	P8.6	O
INT (MISMATCH)	SCU	O
MCHKIN_Write_Access	Write trigger from MCHKIN	I ¹⁾
MCHKCNT_Write_Access	Write trigger from MCHKCNT	I ¹⁾
EINIT	SCU	I

1) This signal is generated within the module itself and is not present at the module boundary.

5 Central Processing Unit (CPU)

Basic tasks of the Central Processing Unit (CPU) are to fetch and decode instructions, to supply operands for the Arithmetic and Logic unit (ALU) and the Multiply and Accumulate unit (MAC), to perform operations on these operands in the ALU and MAC, and to store the previously calculated results. As the CPU is the main engine of the XC27x8X microcontroller, it is also affected by certain actions of the peripheral subsystem.

Because a five-stage processing pipeline (plus 2-stage fetch pipeline) is implemented in the XC27x8X, up to five instructions can be processed in parallel. Most instructions of the XC27x8X are executed in one single clock cycle due to this parallelism.

This chapter describes how the pipeline works for sequential and branch instructions in general, and the hardware provisions which have been made to speed up execution of jump instructions in particular. General instruction timing is described, including standard timing, as well as exceptions.

While internal memory accesses are normally performed by the CPU itself, external peripheral or memory accesses are performed by a particular on-chip External Bus Controller (EBC) which is invoked automatically by the CPU whenever a code or data address refers to the external address space.

Whenever possible, the CPU continues operating while an external memory access is in progress. If external data are required but are not yet available, or if a new external memory access is requested by the CPU before a previous access has been completed, the CPU will be held by the EBC until the request can be satisfied. The EBC is described in a separate chapter.

The on-chip peripheral units of the XC27x8X operate independently of the CPU. Data and control information are interchanged between the CPU and these peripherals via Special Function Registers (SFRs) or shared memory areas.

Whenever peripherals need a non-deterministic CPU action, an on-chip Interrupt Controller compares all pending peripheral service requests against each other and prioritizes one of them. If the priority of the current CPU operation is lower than the priority of the selected peripheral request, an interrupt will occur.

There are two basic types of interrupt processing:

- **Standard interrupt processing** forces the CPU to save the current program status and return address on the stack before branching to the interrupt vector jump table.
- **PEC interrupt processing** steals only one machine cycle from the current CPU activity to perform a single data transfer via the on-chip Peripheral Event Controller (PEC).

System errors detected during program execution (hardware traps) and external non-maskable interrupts are also processed as standard interrupts with a very high priority.

Central Processing Unit (CPU)

In contrast to other on-chip peripherals, there is a closer conjunction between the watchdog timer and the CPU. If enabled, the watchdog timer expects to be serviced by the CPU within a programmable period of time, otherwise it will reset the chip. Thus, the watchdog timer is able to prevent the CPU from going astray when executing erroneous code. The CPU provides a set of instructions for enabling (ENWDT), disabling (DISWDT) and servicing (SRVWDT) the watchdog timer.

In addition to its active operation state, the CPU can enter idle mode by executing the IDLE instruction. In idle mode the CPU stops program execution but still reacts to interrupt or PEC requests. Transition to the active state can be forced by an interrupt request or a hardware reset.

The PWRDN instruction is not enabled in the XC27x8X. If executed a NOP will be performed instead. System power state transitions are controlled by the System Control Unit (SCU).

A set of Special Function Registers is dedicated to the CPU core (CSFRs):

- CPU Status Indication and Control: **PSW, CPUCON1, CPUCON2**
- Code Access Control: **IP, CSP**
- Data Paging Control: **DPP0, DPP1, DPP2, DPP3**
- Global GPRs Access Control: **CP**
- System Stack Access Control: **SP, SPSEG, STKUN, STKOV**
- Multiply and Divide Support: **MDL, MDH, MDC**
- Indirect Addressing Offset: **QR0, QR1, QX0, QX1**
- MAC Address Pointers: **IDX0, IDX1**
- MAC Status Indication and Control: **MCW, MSW, MAH, MAL, MRW**
- ALU Constants Support: **ZEROS, ONES**
- CPU identification: **CPUID**

The CPU also uses CSFRs to access the General Purpose Registers (GPRs). Since all CSFRs can be controlled by any instruction capable of addressing the SFR/CSFR memory space, there is no need for special system control instructions.

However, to ensure proper processor operation, certain restrictions on the user access to some CSFRs must be imposed. For example, the instruction pointer (CSP, IP) cannot be accessed directly at all. These registers can only be changed indirectly via branch instructions. Registers PSW, SP, and MDC can be modified not only explicitly by the programmer, but also implicitly by the CPU during normal instruction processing.

Note: Note that any explicit write request (via software) to an CSFR supersedes a simultaneous modification by hardware of the same register.

Central Processing Unit (CPU)

All CSFRs may be accessed wordwise, or bytewise (some of them even bitwise). Reading bytes from word CSFRs is a non-critical operation. Any write operation to a single byte of a CSFR clears the non-addressed complementary byte within the specified CSFR.

Attention: Reserved CSFR bits must not be modified explicitly, and will always supply a read value of 0. If a byte/word access is preferred by the programmer or is the only possible access the reserved CSFR bits must be written with 0 to provide compatibility with future versions.

Central Processing Unit (CPU)

5.1 Components of the CPU

The high performance of the CPU results from the cooperation of several units which are optimized for their respective tasks (see [Figure 5-1](#)). **Prefetch Unit** and **Branch Unit** feed the pipeline minimizing CPU stalls due to instruction reads. The **Address Unit (ADU)** supports sophisticated addressing modes avoiding additional instructions needed otherwise. **Arithmetic and Logic Unit (ALU)** and **Multiply and Accumulate Unit (MAC)** handle differently sized data and execute complex operations. **Three memory interfaces** and **Write Buffer (WB)** minimize CPU stalls due to data transfers.

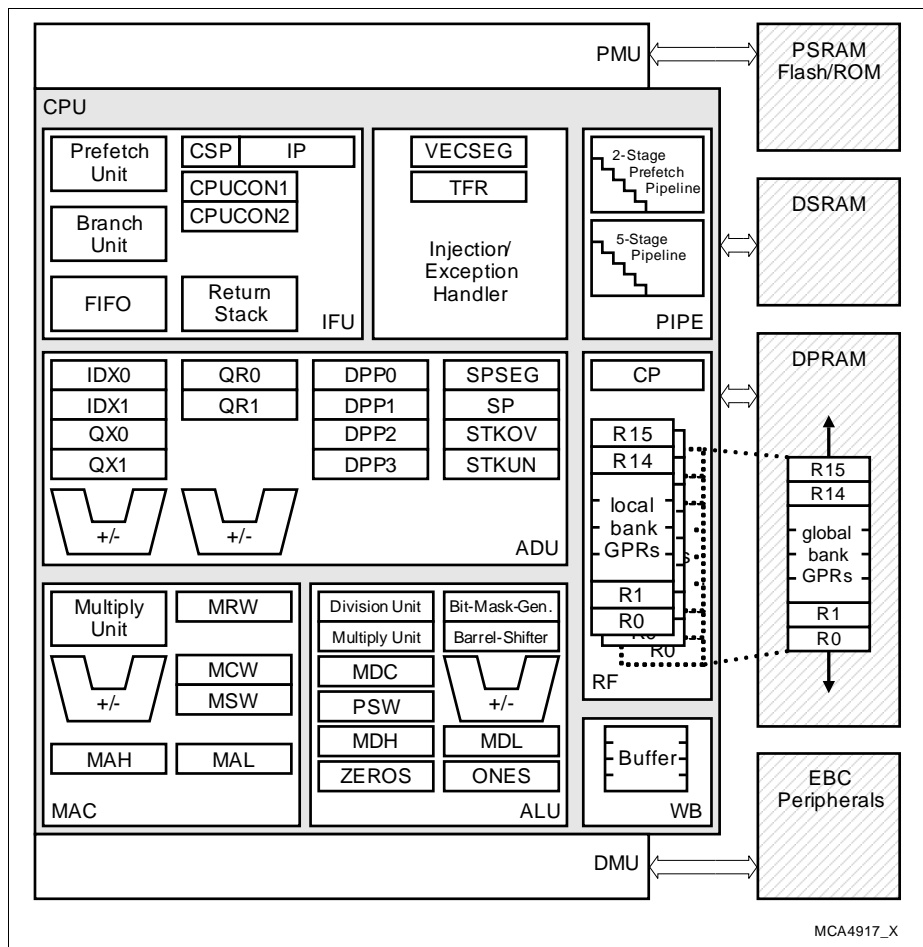


Figure 5-1 CPU Block Diagram

Central Processing Unit (CPU)

In general the instructions move through 7 pipeline stages ([Section 5.3](#)). The stages can be grouped as follows:

- **2 stages fetch pipeline** - receives instructions from program memory and stores them into an instruction FIFO. Fetch pipeline stages can be bypassed.
- **5 stages processing pipeline** - executes each instruction received from fetch stages.

Because passing through one pipeline stage takes at least one clock cycle and because the fetch pipeline stages can be bypassed, any isolated instruction takes at least five clock cycles to be completed. Pipelining, however, allows parallel (i.e. simultaneous) processing of up to five instructions (with branches up to six instructions). Therefore, most of the instructions appear to be processed during one clock cycle as soon as the pipeline has been filled once after reset.

The pipelining increases the average instruction throughput considered over a certain period of time.

5.2 Instruction Fetch and Program Flow Control

The Instruction Fetch Unit (IFU) prefetches and preprocesses instructions to provide a continuous instruction flow. The IFU can fetch simultaneously at least two instructions via a 64-bit wide bus from the Program Management Unit (PMU). The prefetched instructions are stored in an instruction FIFO.

Preprocessing of branch instructions enables the instruction flow to be predicted. While the CPU is in the process of executing an instruction fetched from the FIFO, the prefetcher of the IFU starts to fetch a new instruction at a predicted target address from the PMU. The latency time of this access is hidden by the execution of the instructions which have already been buffered in the FIFO. Even for a non-sequential instruction execution, the IFU can generally provide a continuous instruction flow. The IFU contains two pipeline stages: the Prefetch Stage and the Fetch Stage.

During the prefetch stage, the Branch Detection and Prediction Logic analyzes up to three prefetched instructions stored in the first Instruction Buffer (can hold up to six instructions). If a branch is detected, then the IFU starts to fetch the next instructions from the PMU according to the prediction rules. After having been analyzed, up to three instructions are stored in the second Instruction Buffer (can hold up to three instructions) which is the input register of the Fetch Stage.

In the case of an incorrectly predicted instruction flow, the instruction fetch pipeline is bypassed to reduce the number of dead cycles.

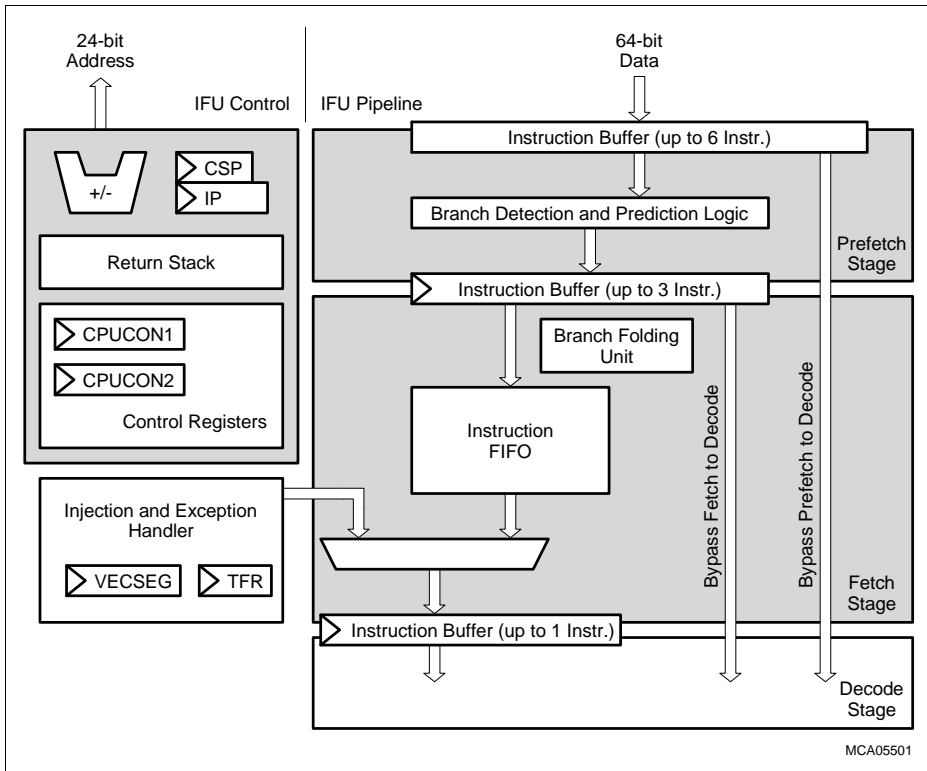


Figure 5-2 IFU Block Diagram

On the Fetch Stage, the prefetched instructions are stored in the instruction FIFO. The Branch Folding Unit (BFU) allows processing of branch instructions in parallel with preceding instructions. To achieve this the BFU preprocesses and reformats the branch instruction. First, the BFU defines (calculates) the absolute target address. This address — after being combined with branch condition and branch attribute bits — is stored in the same FIFO step as the preceding instruction. The target address is also used to prefetch the next instructions.

For the Processing Pipeline, both instructions are fetched from the FIFO again and are executed in parallel. If the instruction flow was predicted incorrectly (or FIFO is empty), the two stages of the IFU can be bypassed.

Note: Pipeline behavior in case of a incorrectly predicted instruction flow is described in the following sections.

5.2.1 Branch Detection and Branch Prediction Rules

The Branch Detection Unit preprocesses instructions and classifies detected branches. Depending on the branch class, the Branch Prediction Unit predicts the program flow using the following rules:

Table 5-1 Branch Classes and Prediction Rules

Branch Instruction Classes	Instructions	Prediction Rule (Assumption)
Inter-segment branch instructions	JMPS seg, caddr CALLS seg, caddr	The branch is always taken
Branch instructions with user programmable branch prediction	JMPA- xcc, caddr JMPA+ xcc, caddr CALLA- xcc, caddr CALLA+ xcc, caddr	User-specified ¹⁾ via bit 8 ('a') of the instruction long word: ...+: branch 'taken' (a = 0) ...-: branch 'not taken' (a = 1)
Indirect branch instructions	JMPI cc, [Rw] CALLI cc, [Rw]	Unconditional: branch 'taken' Conditional: 'not taken'
Relative branch instructions with condition code	JMPR cc, rel	Unconditional or backward: branch 'taken' Conditional forward: 'not taken'
Relative branch instructions without condition code	CALLR rel	The branch is always taken
Branch instructions with bit-condition	JB(C) bitaddr, rel JNB(S) bitaddr, rel	Backward: branch 'taken' Forward: 'not taken'
Return instructions	RET, RETP RETS, RETI	The branch is always taken

1) This bit can be also set/cleared automatically by the Assembler for generic JMPA and CALLA instructions depending on the jump condition

5.2.2 Zero-Cycle Jumps

The **"Zero-Cycle Jumps"** are one of the advanced XC27x8X specifics, which becomes possible due to the complex pipelined structure for processing instruction-flow.

This feature allows, under some circumstances, jumps to be executed in "null time". In fact, a jump is "hooked" to the previous instruction and the two instructions pass through the pipeline as one instruction. This can be only possible, if the jump instruction does not need any of the pipeline resources needed by the predecessor. Hence, the following rules are essential:

- a jump can not be hooked onto another jump instruction, as the pipeline resource "target IP" can not be shared between the two;

Central Processing Unit (CPU)

- a jump can not be executed in zero-cycle if it requires any memory access, as basically any predecessor instruction might access a memory.

The above are only preliminary conditions, needed to make a jump zero-cycle. But would this really happen, it's not reliable enough to predict: it also depends on the exact instruction sequence, speed of the program memory etc.

What can be summarized is:

- only **JMPA**, **JMPR** and **JMPS** Instructions **can be** converted to zero-cycle; if the immediately preceding instruction **is not** a branch (any **JMP**, **CALL** or **RET**).
- If a Jump is executed as zero-cycle, in fact the address of this Jump will not be assigned to the Instruction Pointer.

*Note: No IP-Breakpoint must be set over an instruction, which satisfies the two prepositions above for a zero-cycle Jump. Otherwise, if set, it is **very possible** this Breakpoint will be missed by the debug module.*

5.2.3 Atomic and Extend Instructions

The atomic and extend instructions (**ATOMIC**, **EXTR**, **EXTP**, **EXTS**, **EXTPR**, **EXTSR**) disable standard and PEC interrupts and class A traps until completion of the immediately following sequence of instructions. The number of instructions in the sequence may vary from 1 to 4. It is coded in the 2-bit constant field #rang2 and takes values from 0 to 3. The **EXTENDED** instructions additionally change the addressing mechanism during this sequence (see instruction description).

ATOMIC and **EXTENDED** instructions become active immediately, so no additional **NOPs** are required. All instructions requiring multi cycles or hold states for execution are considered to be one instruction. The **ATOMIC** and **EXTENDED** instructions can be used with any instruction type.

If a branch instruction following immediately after an atomic sequence is executed as zero-cycle jump, then this branch is part of the atomic sequence as well. If the branch instruction is not a part of the **ATOMIC** sequence, it should not be hooked on to the atomic sequence, a **NOP** could be inserted in between.

*Note: If a class B trap interrupt occurs during an **ATOMIC** or **EXTENDED** sequence, then the sequence is terminated, an interrupt lock is removed, and the standard condition is restored before the trap routine is executed. The remaining instructions of the terminated sequence executed after returning from the trap routine will run under standard conditions.*

*Note: When using nested **ATOMIC** and **EXTENDED** instructions. There is only one counter to control the length of the sequence, i.e. issuing an **ATOMIC** or **EXTENDED** instruction within a sequence will reload the counter with the value of the new instruction.*

5.3 Instruction Processing Pipeline

The XC27x8X uses five pipeline stages to execute an instruction. All instructions pass through each of the five stages of the instruction processing pipeline. The pipeline stages are listed here together with the 2 stages of the fetch pipeline:

1st -> PREFETCH: This stage prefetches instructions from the PMU in the predicted order. The instructions are preprocessed in the branch detection unit to detect branches. The prediction logic decides if the branches are assumed to be taken or not.

2nd -> FETCH: The instruction pointer of the next instruction to be fetched is calculated according to the branch prediction rules. For zero-cycle branch execution, the Branch Folding Unit preprocesses and combines detected branches with the preceding instructions. Prefetched instructions are stored in the instruction FIFO. At the same time, instructions are transported out of the instruction FIFO to be executed in the instruction processing pipeline.

3rd -> DECODE: The instructions are decoded and, if required, the register file is accessed to read the GPR used in indirect addressing modes.

4th -> ADDRESS: All the operand addresses are calculated. Register SP is decremented or incremented for all instructions which implicitly access the system stack.

5th -> MEMORY: All the required operands are fetched.

6th -> EXECUTE: An ALU or MAC-Unit operation is performed on the previously fetched operands. The condition flags are updated. All explicit write operations to CPU-SFRs and all auto-increment/auto-decrement operations of GPRs used as indirect address pointers are performed.

7th -> WRITE BACK: All external operands and the remaining operands within the internal DPRAM space are written back. Operands located in the internal SRAM are buffered in the Write Back Buffer.

Specific so-called injected instructions are generated internally to provide the time needed to process instructions requiring more than one CPU cycle for processing. They are automatically injected into the decode stage of the pipeline, then they pass through the remaining stages like every standard instruction. Program interrupt, PEC transfer, and debug operations are also performed by means of injected instructions. Although these internally injected instructions will not be noticed in reality, they help to explain the operation of the pipeline.

The performance of the CPU (pipeline) is decreased by bandwidth limitations (same resource is accessed by different stages) and data dependencies between instructions. The XC27x8X's CPU has dedicated hardware to detect and to resolve different kinds of dependencies. Some of those dependencies are described in the following section.

Because up to five different instructions are processed simultaneously, additional hardware has been dedicated to deal with dependencies which may exist between instructions in different pipeline stages. This extra hardware supports 'forwarding' of the operand read and write values and resolves most of the possible conflicts — such as

multiple usage of buses — in a time optimized way without performance loss. This makes the pipeline unnoticeable for the user in most cases. However, there are some cases in which the pipeline requires attention by the programmer.

5.3.1 Access to the IO Area

Read or write accesses to the IO Areas of the XC27x8X memory space enforce particular pipeline behavior. Thus the requirements of peripheral devices with registers located in these areas are handled appropriately.

The following typical properties of peripheral device registers are considered:

- Upon a write to a peripheral register the contents of any (also multiple) peripheral register(s) may change as a consequence of the write.
- Upon a read from a peripheral register the contents of the same register may change as a consequence of the read (e.g. read buffer of a serial channel)

These cases are handled by following pipeline measures:

Write before read execution enforced

If the instructions in the pipeline contain a write action followed by a read action both to the IO areas then the read action is delayed (held in memory stage) until the write action has passed through the writeback stage. Thus the write action will always be scheduled before a read action.

Attention: *Due to additional system delay this does not guarantee that a write will become effective before a read at the target registers.*

Additional system delay is accumulated by the bus system or caused by the peripheral itself. In case the additional read delay differs from the write delay the read may overtake the write. However since the on-chip delays are similar the programmer must take care about this in particular when using off-chip peripherals allocating IO area through the EXTBUS.

Prevention of buffered writes

Write access to the IO area is not buffered in the writeback buffer.

5.3.2 Pipeline Conflicts

The following examples describe the pipeline behavior in special cases and give provide rules to optimize performance by instruction re-ordering.

Note: The XC27x8X has a fully interlocked pipeline, which means that pipeline conflicts do not cause any malfunction. Instruction re-ordering is only required for performance reasons.

5.3.2.1 Using General Purpose Registers

The GPRs are the working registers of the CPU and there are a lot of possible dependencies between instructions using GPRs. A high-speed five-port register file prevents bandwidth conflicts. Dedicated hardware is implemented to detect and resolve the data dependencies. Special forwarding buses are used to forward GPR values from one pipeline stage to another. In most cases, this allows the execution of instructions without any delay despite of data dependencies.

Conflict_GPRs_Resolved:

```

In      ADD R0,R1      ;Compute new value for R0
In+1    ADD R3,R0      ;Use R0 again
In+2    ADD R6,R0      ;Use R0 again
In+3    ADD R6,R1      ;Use R6 again

```

Table 5-2 Resolved Pipeline Dependencies Using GPRs

Stage	T _n	T _{n+1}	T _{n+2}	T _{n+3}	T _{n+4} ¹⁾	T _{n+5} ²⁾
DECODE	I _n = ADD R0, R1	I _{n+1} = ADD R3, R0	I _{n+2} = ADD R6, R0	I _{n+3} = ADD R6, R1	I _{n+4}	I _{n+5}
ADDRESS	I _{n-1}	I _n = ADD R0, R1	I _{n+1} = ADD R3, R0	I _{n+2} = ADD R6, R0	I _{n+3} = ADD R6, R1	I _{n+4}
MEMORY	I _{n-2}	I _{n-1}	I _n = ADD R0, R1	I _{n+1} = ADD R3, R0	I _{n+2} = ADD R6, R0	I _{n+3} = ADD R6 , R1
EXECUTE	I _{n-3}	I _{n-2}	I _{n-1}	I _n = ADD R0 , R1	I _{n+1} = ADD R3, R0	I _{n+2} = ADD R6 , R0
WR.BACK	I _{n-4}	I _{n-3}	I _{n-2}	I _{n-1}	I _n = ADD R0 , R1	I _{n+1} = ADD R3, R0

1) R0 forwarded from WRITE BACK to MEMORY.

2) R6 forwarded from EXECUTE to MEMORY.

However, if a GPR is used for indirect addressing the address pointer (i.e. the GPR) will be required already in the DECODE stage. In this case the instruction is stalled in the address stage until the operation in the ALU is executed and the result is forwarded to the address stage.

Conflict_GPRs_Pointer_Stall:

```

In      ADD R0,R1      ;Compute new value for R0
In+1    MOV R3,[R0]    ;Use R0 as address pointer
In+2    ADD R6,R0
In+3    ADD R6,R1

```

Table 5-3 Pipeline Dependencies Using GPRs as Pointers (Stall)

Stage	T _n	T _{n+1}	T _{n+2} ¹⁾	T _{n+3} ²⁾	T _{n+4}	T _{n+5}
DECODE	I _n = ADD R0, R1	I _{n+1} = MOV R3, [R0]	I _{n+2}	I _{n+2}	I _{n+2}	I _{n+3}
ADDRESS	I _{n-1}	I _n = ADD R0, R1	I _{n+1} = MOV R3, [R0]	I _{n+1} = MOV R3, [R0]	I _{n+1} = MOV R3, [R0]	I _{n+2}
MEMORY	I _{n-2}	I _{n-1}	I _n = ADD R0, R1	–	–	I _{n+1} = MOV R3, [R0]
EXECUTE	I _{n-3}	I _{n-2}	I _{n-1}	I _n = ADD R0 , R1	–	–
WR.BACK	I _{n-4}	I _{n-3}	I _{n-2}	I _{n-1}	I _n = ADD R0, R1	–

1) New value of R0 not yet available.

2) R0 forwarded from EXECUTE to ADDRESS (next cycle).

To avoid these stalls, one multicycle instruction or two single cycle instructions may be inserted. These instructions must not update the GPR used for indirect addressing.

Conflict_GPRs_Pointer_NoStall:

```

In    ADD R0,R1      ;Compute new value for R0
In+1  ADD R6,R0      ;R0 is not updated, just read
In+2  ADD R6,R1
In+3  MOV R3,[R0]    ;Use R0 as address pointer

```

Table 5-4 Pipeline Dependencies Using GPRs as Pointers (No Stall)

Stage	T _n	T _{n+1}	T _{n+2}	T _{n+3} ¹⁾	T _{n+4}	T _{n+5}
DECODE	I _n = ADD R0, R1	I _{n+1} = ADD R6, R0	I _{n+2} = ADD R6, R1	I _{n+3} = MOV R3, [R0]	I _{n+4}	I _{n+5}
ADDRESS	I _{n-1}	I _n = ADD R0, R1	I _{n+1} = ADD R6, R0	I _{n+2} = ADD R6, R1	I _{n+3} = MOV R3, [R0]	I _{n+4}
MEMORY	I _{n-2}	I _{n-1}	I _n = ADD R0, R1	I _{n+1} = ADD R6, R0	I _{n+2} = ADD R6, R1	I _{n+3} = MOV R3, [R0]
EXECUTE	I _{n-3}	I _{n-2}	I _{n-1}	I _n = ADD R0 , R1	I _{n+1} = ADD R6, R0	I _{n+2} = ADD R6, R1
WR.BACK	I _{n-4}	I _{n-3}	I _{n-2}	I _{n-1}	I _n = ADD R0, R1	I _{n+1} = ADD R6, R0

1) R0 forwarded from EXECUTE to ADDRESS (next cycle).

5.3.2.2 Using Indirect Addressing Modes

In the case of read accesses using indirect addressing modes, the Address Generation Unit uses a speculative addressing mechanism. The read data path to one of the different memory areas (DPRAM, DSRAM, etc.) is selected according to a history table before the address is decoded. This history table has one entry for each of the GPRs. The entries store the information of the last accessed memory area using the corresponding GPR. In the case of an incorrect prediction of the memory area, the read access must be restarted.

It is recommended that the GPRs used for indirect addressing always point to the same memory area. If an updated GPR points to a different memory area, the next read operation will access the wrong memory area. The read access must be repeated, which leads to pipeline stalls.

Conflict_GPRs_Pointer_WrongHistory:

```

In    ADD R3,[R0]      ;R0 points to DPRAM (e.g.)
In+1  MOV R0,R4
...
Ii    MOV DPPX, ...    ;change DPPx
...
Im    ADD R6,[R0]      ;R0 now points to SRAM (e.g.)
Im+1  MOV R6,R1

```

Table 5-5 Pipeline Dependencies with Pointers (Valid Speculation)

Stage	T _n	T _{n+1}	T _{n+2}	T _{n+3}	T _{n+4}	T _{n+5}
DECODE	I _n = ADD R3, [R0]	I _{n+1} = MOV R0, R4	I _{n+2}	I _{n+3}	I _{n+4}	I _{n+5}
ADDRESS	I _{n-1}	I _n = ADD R3, [R0]	I _{n+1} = MOV R0, R4	I _{n+2}	I _{n+3}	I _{n+4}
MEMORY	I _{n-2}	I _{n-1}	I _n = ADD R3, [R0]	I _{n+1} = MOV R0, R4	I _{n+2}	I _{n+3}
EXECUTE	I _{n-3}	I _{n-2}	I _{n-1}	I _n = ADD R3, [R0]	I _{n+1} = MOV R0, R4	I _{n+2}
WR.BACK	I _{n-4}	I _{n-3}	I _{n-2}	I _{n-1}	I _n = ADD R3, [R0]	I _{n+1} = MOV R0, R4

Table 5-6 Pipeline Dependencies with Pointers (Invalid Speculation)

Stage	T_m	T_{m+1}	$T_{m+2}^{1)}$	T_{m+3}	T_{m+4}	T_{m+5}
DECODE	$I_m = \text{ADD R6, [R0]}$	$I_{m+1} = \text{MOV R6, R1}$	$I_{m+1} = \text{MOV R6, R1}$	I_{m+2}	I_{m+3}	I_{m+4}
ADDRESS	I_{m-1}	$I_m = \text{ADD R6, [R0]}$	$I_m = \text{ADD R6, [R0]}$	$I_{m+1} = \text{MOV R6, R1}$	I_{m+2}	I_{m+3}
MEMORY	I_{m-2}	I_{m-1}	–	$I_m = \text{ADD R6, [R0]}$	$I_{m+1} = \text{MOV R6, R1}$	I_{m+2}
EXECUTE	I_{m-3}	I_{m-2}	I_{m-1}	–	$I_m = \text{ADD R6, [R0]}$	$I_{m+1} = \text{MOV R6, R1}$
WR.BACK	I_{m-4}	I_{m-3}	I_{m-2}	I_{m-1}	–	$I_m = \text{ADD R6, [R0]}$

1) Access to location [R0] must be repeated due to wrong history (target area was changed).

5.3.2.3 Due to Memory Bandwidth

Memory bandwidth conflicts can occur if instructions in the pipeline access the same memory area at the same time. Special access mechanisms are implemented to minimize conflicts. The DPRAM of the CPU has two independent read/write ports; this allows parallel read and write operation without delays. Write accesses to the DSRAM can be buffered in a Write Back Buffer until read accesses are finished.

All instructions except the CoXXX instructions can read only one memory operand per cycle. A conflict between the read and one write access cannot occur because the DPRAM has two independent read/write ports. Only other pipeline stall conditions can generate a DPRAM bandwidth conflict. The DPRAM is a synchronous pipelined memory. The read access starts with the valid addresses on the address stage. The data are delivered in the Memory stage. If a memory read access is stalled in the Memory stage and the following instruction on the Address stage tries to start a memory read, the new read access must be delayed as well. But, this conflict is hidden by an already existing stall of the pipeline.

The CoXXX instructions are the only instructions able to read two memory operands per cycle. A conflict between the two read and one pending write access can occur if all three operands are located in the DPRAM area. This is especially important for performance in the case of executing a filter routine. One of the operands should be located in the DSRAM to guarantee a single-cycle execution of the CoXXX instructions.

Conflict_DPRAM_Bandwidth:

```

In    ADD op1,R1
In+1  ADD R6,R0
In+2  CoMAC [IDX0],[R0]
```


I_{n+3} `MOV R3, [R0]`

Table 5-7 Pipeline Dependencies in Case of Memory Conflicts (DPRAM)

Stage	T_n	T_{n+1}	T_{n+2}	T_{n+3}	T_{n+4} ¹⁾	T_{n+5}
DECODE	$I_n = \text{ADD op1, R1}$	$I_{n+1} = \text{ADD R6, R0}$	$I_{n+2} = \text{CoMAC ...}$	$I_{n+3} = \text{MOV R3, [R0]}$	I_{n+4}	I_{n+4}
ADDRESS	I_{n-1}	$I_n = \text{ADD op1, R1}$	$I_{n+1} = \text{ADD R6, R0}$	$I_{n+2} = \text{CoMAC ...}$	$I_{n+3} = \text{MOV R3, [R0]}$	$I_{n+3} = \text{MOV R3, [R0]}$
MEMORY	I_{n-2}	I_{n-1}	$I_n = \text{ADD op1, R1}$	$I_{n+1} = \text{ADD R6, R0}$	$I_{n+2} = \text{CoMAC ...}$	$I_{n+2} = \text{CoMAC ...}$
EXECUTE	I_{n-3}	I_{n-2}	I_{n-1}	$I_n = \text{ADD op1, R1}$	$I_{n+1} = \text{ADD R6, R0}$	—
WR.BACK	I_{n-4}	I_{n-3}	I_{n-2}	I_{n-1}	$I_n = \text{ADD op1, R1}$	$I_{n+1} = \text{ADD R6, R0}$

1) CoMAC instruction stalls due to memory bandwidth conflict.

The DSRAM is a single-port memory with one read/write port. To reduce the number of bandwidth conflict cases, a Write Back Buffer is implemented. It has three data entries. Only if the buffer is filled and a read access and a write access occur at the same time, must the read access be stalled while one of the buffer entries is written back.

Conflict_DSRAM_Bandwidth:

```

 $I_n$     ADD op1, R1
 $I_{n+1}$  ADD R6, R0
 $I_{n+2}$  ADD R6, op2
 $I_{n+3}$  MOV R3, R2

```

Table 5-8 Pipeline Dependencies in Case of Memory Conflicts (DSRAM)

Stage	T_n	T_{n+1}	T_{n+2}	T_{n+3}	T_{n+4} ¹⁾	T_{n+5}
DECODE	$I_n = \text{ADD op1, R1}$	$I_{n+1} = \text{ADD R6, R0}$	$I_{n+2} = \text{ADD R6, op2}$	$I_{n+3} = \text{MOV R3, R2}$	I_{n+4}	I_{n+4}
ADDRESS	I_{n-1}	$I_n = \text{ADD op1, R1}$	$I_{n+1} = \text{ADD R6, R0}$	$I_{n+2} = \text{ADD R6, op2}$	$I_{n+3} = \text{MOV R3, R2}$	$I_{n+3} = \text{MOV R3, R2}$
MEMORY	I_{n-2}	I_{n-1}	$I_n = \text{ADD op1, R1}$	$I_{n+1} = \text{ADD R6, R0}$	$I_{n+2} = \text{ADD R6, op2}$	$I_{n+2} = \text{ADD R6, op2}$
EXECUTE	I_{n-3}	I_{n-2}	I_{n-1}	$I_n = \text{ADD op1, R1}$	$I_{n+1} = \text{ADD R6, R0}$	—

Table 5-8 Pipeline Dependencies in Case of Memory Conflicts (DSRAM)

Stage	T_n	T_{n+1}	T_{n+2}	T_{n+3}	T_{n+4} ¹⁾	T_{n+5}
WR.BACK	I_{n-4}	I_{n-3}	I_{n-2}	I_{n-1}	$I_n = \text{ADD op1, R1}$	$I_{n+1} = \text{ADD R6, R0}$
WB.Buffer	full	full	full	full	full	full

1) ADD R6, op2 instruction stalls due to memory bandwidth conflict.

5.3.2.4 Caused by CPU-SFR Updates

CPU-SFRs control the CPU functionality and behavior. Changes and updates of CSFRs influence the instruction flow in the pipeline. Therefore, special care is required to ensure that instructions in the pipeline always work with the correct CSFR values. CSFRs are updated late on the EXECUTE stage of the pipeline. Meanwhile, without conflict detection, the instructions in the DECODE, ADDRESS, and MEMORY stages would still work without updated register values. The CPU detects conflict cases and stalls the pipeline to guarantee a correct execution. For performance reasons, the CPU differentiates between different classes of CPU-SFRs. The flow of instructions through the pipeline can be improved by following the given rules used for instruction re-ordering.

There are three classes of CPU-SFRs:

- CSFRs not generating pipeline conflicts (ONES, ZEROS, MCW)
- CSFR result registers updated late in the EXECUTE stage, causing one stall cycle
- CSFRs affecting the whole CPU or the pipeline, causing a pipeline cancellation

CSFR Result Registers

The CSFR result registers MDH, MDL, MSW, MAH, MAL, and MRW of the ALU and MAC-Unit are updated late in the EXECUTE stage of the pipeline. If an instruction (except CoSTORE) accesses these registers in the MEMORY stage, the value cannot be forwarded. The instruction must be stalled for one cycle on the MEMORY stage.

Conflict_CSFR_Update_Stall:

```

 $I_n$       MUL  R0,R1
 $I_{n+1}$     MOV  R6,MDL
 $I_{n+2}$     ADD  R6,R1
 $I_{n+3}$     MOV  R3,[R0]
```

Table 5-9 Pipeline Dependencies with Result CSFRs (Stall)

Stage	T _n	T _{n+1}	T _{n+2}	T _{n+3} ¹⁾	T _{n+4}	T _{n+5}
DECODE	I _n = MUL R0, R1	I _{n+1} = MOV R6, MDL	I _{n+2} = ADD R6, R1	I _{n+3} = MOV R3, [R0]	I _{n+3} = MOV R3, [R0]	I _{n+4}
ADDRESS	I _{n-1}	I _n = MUL R0, R1	I _{n+1} = MOV R6, MDL	I _{n+2} = ADD R6, R1	I _{n+2} = ADD R6, R1	I _{n+3} = MOV R3, [R0]
MEMORY	I _{n-2}	I _{n-1}	I _n = MUL R0, R1	I _{n+1} = MOV R6, MDL	I _{n+1} = MOV R6, MDL	I _{n+2} = ADD R6, R1
EXECUTE	I _{n-3}	I _{n-2}	I _{n-1}	I _n = MUL R0, R1	—	I _{n+1} = MOV R6, MDL
WR.BACK	I _{n-4}	I _{n-3}	I _{n-2}	I _{n-1}	I _n = MUL R0, R1	—

1) Cannot read MDL here.

By reordering instructions, the bubble in the pipeline can be filled with an instruction not using this resource.

Conflict_CSFR_Update_Resolved:

```

In      MUL  R0, R1
In+1    MOV  R3, [R0]
In+2    MOV  R6, MDL
In+3    ADD  R6, R1

```

Table 5-10 Pipeline Dependencies with Result CSFRs (No Stall)

Stage	T _n	T _{n+1}	T _{n+2}	T _{n+3}	T _{n+4} ¹⁾	T _{n+5}
DECODE	I _n = MUL R0, R1	I _{n+1} = MOV R3, [R0]	I _{n+2} = MOV R6, MDL	I _{n+3} = ADD R6, R1	I _{n+4}	I _{n+5}
ADDRESS	I _{n-1}	I _n = MUL R0, R1	I _{n+1} = MOV R3, [R0]	I _{n+2} = MOV R6, MDL	I _{n+3} = ADD R6, R1	I _{n+4}
MEMORY	I _{n-2}	I _{n-1}	I _n = MUL R0, R1	I _{n+1} = MOV R3, [R0]	I _{n+2} = MOV R6, MDL	I _{n+3} = ADD R6, R1
EXECUTE	I _{n-3}	I _{n-2}	I _{n-1}	I _n = MUL R0, R1	I _{n+1} = MOV R3, [R0]	I _{n+2} = MOV R6, MDL
WR.BACK	I _{n-4}	I _{n-3}	I _{n-2}	I _{n-1}	I _n = MUL R0, R1	I _{n+1} = MOV R3, [R0]

1) MDL can be read now, no stall cycle necessary.

CSFRs Affecting the Whole CPU

Some CSFRs affect the whole CPU or the pipeline before the Memory stage. The CPU-SFRs CPUCON1/2, CP, SP, STKUN, STKOV, VECSEG, TFR, and PSW affect the overall CPU function, while the CPU-SFRs IDX0, IDX1, QX1, QX0, DPP0, DPP1, DPP2, and DPP3 only affect the DECODE, ADDRESS, and MEMORY stage when they are modified **explicitly**. In this case the pipeline behavior depends on the instruction and addressing mode used to modify the CSFR.

In the case of modification of these CSFRs by "POP CSFR" or by instructions using the reg,#data16 addressing mode, a special mechanism is implemented to improve performance during the initialization.

For further explanation, the instruction which modifies the CSFR can be called "instruction_modify_CSFR". This special case is detected in the DECODE stage when the instruction_modify_CSFR enters the processing pipeline. Further on, instructions described in the following list are held in the DECODE stage (all other instructions are not held):

- Instructions using long addressing mode (mem)
- Instructions using indirect addressing modes ($[R_w]$, $[R_w+]$...), except JMPL and CALLI
- ENWDT, DISWDT, EINIT
- All CoXXX instructions

If the CPUCON1/2, CP, SP, STKUN, STKOV, VECSEG, TFR, or the PSW are modified and the instruction_modify_CSFR reaches the EXECUTE stage, the pipeline is canceled. The modification affects the entire pipeline and the instruction prefetch. A clean cancel and restart mechanism is required to guarantee a correct instruction flow. In case of modification of IDX0, IDX1, QX1, QX0, DPP0, DPP1, DPP2, or DPP3 only the DECODE, ADDRESS, and MEMORY stages are affected and the pipeline needs not to be canceled. The modification does not affect the instructions in the ADDRESS, MEMORY stage because they are not using this resource. Other kinds of instructions are held in the DECODE stage until the CSFR is modified.

The following example shows a case in which the pipeline is stalled. The instruction "MOV R6, R1" after the "MOV IDX1, #12" instruction which modifies the CSFR will be held in DECODE Stage until the IDX1 register is updated. The next example shows an optimized initialization routine.

Conflict_Canceling:

```
In      MOV  IDX1, #12
In+1    MOV  R6, mem
In+2    ADD  R6, R1
In+3    MOV  R3, [R0]
```

Table 5-11 Pipeline Dependencies with Control CSFRs (Canceling)

Stage	T _n	T _{n+1}	T _{n+2}	T _{n+3}	T _{n+4}	T _{n+5}
DECODE	I _n = MOV IDX1, #12	I _{n+1} = MOV R6, mem	I _{n+1} = MOV R6, mem	I _{n+1} = MOV R6, mem	I _{n+1} = MOV R6, mem	I _{n+2} = ADD R6, R1
ADDRESS	I _{n-1}	I _n = MOV IDX1, #12	–	–	–	I _{n+1} = MOV R6, mem
MEMORY	I _{n-2}	I _{n-1}	I _n = MOV IDX1, #12	–	–	–
EXECUTE	I _{n-3}	I _{n-2}	I _{n-1}	I _n = MOV IDX1, #12	–	–
WR.BACK	I _{n-4}	I _{n-3}	I _{n-2}	I _{n-1}	I _n = MOV IDX1, #12	–

Conflict_Canceling_Optimized:

```

In      MOV  IDX1, #12
In+1    MOV  MAH, #23
In+2    MOV  MAL, #25
In+3    MOV  R3, #08

```

Table 5-12 Pipeline Dependencies with Control CSFRs (Optimized)

Stage	T _n	T _{n+1}	T _{n+2}	T _{n+3}	T _{n+4}	T _{n+5}
DECODE	I _n = MOV IDX1, #12	I _{n+1} = MOV MAH, #23	I _{n+2} = MOV MAL, #25	I _{n+3} = MOV R3, #08	I _{n+4}	I _{n+5}
ADDRESS	I _{n-1}	I _n = MOV IDX1, #12	I _{n+1} = MOV MAH, #23	I _{n+2} = MOV MAL, #25	I _{n+3} = MOV R3, #08	I _{n+4}
MEMORY	I _{n-2}	I _{n-1}	I _n = MOV IDX1, #12	I _{n+1} = MOV MAH, #23	I _{n+2} = MOV MAL, #25	I _{n+3} = MOV R3, #08
EXECUTE	I _{n-3}	I _{n-2}	I _{n-1}	I _n = MOV IDX1, #12	I _{n+1} = MOV MAH, #23	I _{n+2} = MOV MAL, #25
WR.BACK	I _{n-4}	I _{n-3}	I _{n-2}	I _{n-1}	I _n = MOV IDX1, #12	I _{n+1} = MOV MAH, #23

For all the other instructions that modify this kind of CSFR, a simple stall and cancel mechanism guarantees the correct instruction flow.

A possible explicit write-operation to this kind of CSFRs is detected on the MEMORY stage of the pipeline. The following instructions on the ADDRESS and DECODE Stage are stalled. If the instruction reaches the EXECUTE stage, the entire pipeline and the Instruction FIFO of the IFU are canceled. The instruction flow is completely re-started.

Conflict_Canceling_Completely:

```

In      MOV PSW, R4
In+1    MOV R6, R1
In+2    ADD R6, R1
In+3    MOV R3, [R0]

```

Table 5-13 Pipeline Dependencies with Control CSFRs (Cancel All)

Stage	T _{n+1}	T _{n+2}	T _{n+3}	T _{n+4}	T _{n+5}	T _{n+6}
DECODE	I _{n+1} = MOV R6, R1	I _{n+2} = ADD R6, R1	I _{n+2} = ADD R6, R1	–	–	I _{n+1} = MOV R6, R1
ADDRESS	I _n = MOV PSW, R4	I _{n+1} = MOV R6, R1	I _{n+1} = MOV R6, R1	–	–	–
MEMORY	I _{n-1}	I _n = MOV PSW, R4	–	–	–	–
EXECUTE	I _{n-2}	I _{n-1}	I _n = MOV PSW, R4	–	–	–
WR.BACK	I _{n-3}	I _{n-2}	I _{n-1}	I _n = MOV PSW, R4	–	–

5.4 CPU Configuration Registers

The CPU configuration registers select a number of general features and behaviors of the XC27x8X's CPU core. In general these registers are only written by the startup software and not altered during application software run time.

Note: The CPU configuration registers are protected by the register security mechanism after the EINIT instruction has been executed.

CPUCON1

CPU Control Register 1

SFR (FE18_H/0C_H)

Reset Value: 0007_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0									VECSC	WDT CTL	SGT DIS	INTS CXT	BP	ZCJ	
r	r	r	r	r	r	r	r	r	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
0	[15:7]	r	Reserved Read as 0, should be written 0
VECSC	[6:5]	rw	Scaling Factor of Vector Table 00 _B Space between two vectors is 2 words ¹⁾ 01 _B Space between two vectors is 4 words 10 _B Space between two vectors is 8 words 11 _B Space between two vectors is 16 words
WDTCTL	4	rw	Configuration of Watchdog Timer 0 _B DISWDT executable only until End Of Init ²⁾ 1 _B DISWDT/ENWDT always executable (enhanced WDT mode)
SGTDIS	3	rw	Segmentation Disable/Enable Control 0 _B Segmentation enabled 1 _B Segmentation disabled
INTSCXT	2	rw	Enable Interruptibility of Switch Context 0 _B Switch context is not interruptible 1 _B Switch context is interruptible
BP	1	rw	Enable Branch Prediction Unit 0 _B Branch prediction disabled 1 _B Branch prediction enabled
ZCJ	0	rw	Enable Zero-Cycle Jump Function 0 _B Zero-cycle jump function disabled 1 _B Zero-cycle jump function enabled

Central Processing Unit (CPU)

- 1) The default value (2 words) is compatible with the vector distance defined in the C166 Family architecture.
- 2) The DISWDT (executed after EINIT) and ENWDT instructions are internally converted in a NOP instruction.

CPUCON2

CPU Control Register 2

SFR (FE1A_H/0D_H)

Reset Value: 8FBB_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFODEPTH			FIFOFED			BYP PF	BYP F	1	STE N	LFIC	OV RUN	RET ST	FAS TBL	1	SL
rw			rw			rw	rw	r	rw	rw	rw	rw	rw	r	rw

Field	Bits	Type	Description
FIFODEPTH	[15:12]	rw	FIFO Depth Configuration 0 _H No FIFO (entries) 1 _H One FIFO entry ... 8 _H Eight FIFO entries 9 _H reserved ... F _H reserved
FIFOFED	[11:10]	rw	FIFO Fed Configuration 00 _B FIFO disabled 01 _B FIFO filled with up to one instruction per cycle 10 _B FIFO filled with up to two instructions per cycle 11 _B FIFO filled with up to three instruction per cycle
BYP PF	9	rw	Prefetch Bypass Control 0 _B Bypass path from prefetch to decode disabled 1 _B Bypass path from prefetch to decode available
BYP F	8	rw	Fetch Bypass Control 0 _B Bypass path from fetch to decode disabled 1 _B Bypass path from fetch to decode available
1	7	r	Reserved Read as 1, should be written 1
STEN	6	rw	Stall Instruction Enable (for debug purposes) 0 _B Stall Instruction disabled 1 _B Stall Instruction enabled (see example below)
LFIC	5	rw	Linear Follower Instruction Cache 0 _B Linear Follower Instruction Cache disabled 1 _B Linear Follower Instruction Cache enabled

Central Processing Unit (CPU)

Field	Bits	Type	Description
OVRUN	4	rw	Pipeline Control 0_B Overrun of pipeline bubbles not allowed 1_B Overrun of pipeline bubbles allowed
RETST	3	rw	Enable Return Stack 0_B Return Stack is disabled 1_B Return Stack is enabled
FASTBL	2	rw	Enables the fast injection of block transfers 0_B Direct injection disabled 1_B Direct injection enabled
1	1	r	Reserved Read as 1, should be written 1
SL	0	rw	Enables Short Loop Mode 0_B Short loop mode disabled 1_B Short loop mode enabled

Note: This register must only be modified when explicitly documented - e.g. in an errata sheet.

5.5 Use of General Purpose Registers

The CPU provides three banks of sixteen dedicated registers R0, R1, R2, ... R15, called General Purpose Registers (GPRs), which can be accessed in one CPU cycle. The GPRs are the working registers of the arithmetic and logic units and many also serve as address pointers for indirect addressing modes.

The register banks are accessed via the 5-port register file providing the high access speed required for the CPU's performance. The register file is split into three independent physical register banks. There are **two types of register banks**:

- **Two local register banks** which are a part of the register file
- **One global register bank** which is memory-mapped and cached in the register file

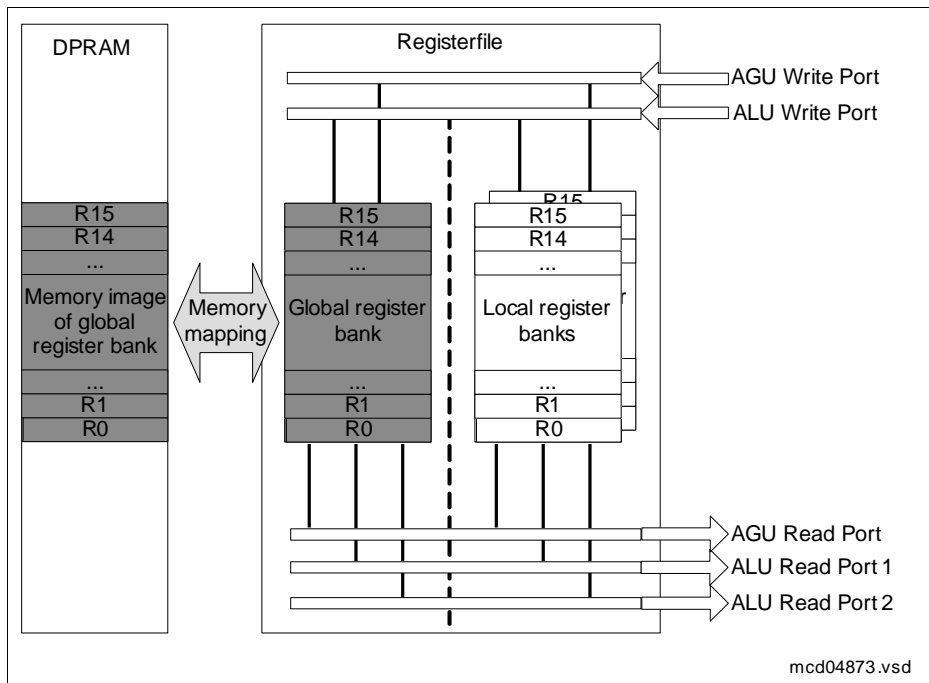


Figure 5-3 Register File

Bitfield **BANK** in register **PSW** selects which of the three physical register banks is activated. The selected bank can be changed explicitly by any instruction which writes to the **PSW**, or implicitly by a **RET1** instruction, an interrupt or hardware trap. In case of an interrupt, the selection of the register bank is configured via registers **BNKSELx** in the Interrupt Controller **ITC**. Hardware traps always use the global register bank.

Central Processing Unit (CPU)

The local register banks are built of dedicated physical registers, while the global register bank represents a cache. Multiple global banks can be mapped to the internal DPRAM. Each of these banks uses a block of 16 consecutive words. A Context Pointer (CP) register determines the base address of the current selected bank. To provide the required access speed, the GPRs located in the DPRAM are cached in the 5-port register file (only one memory-mapped GPR bank can be cached at the time). If the global register bank is activated, the cache will be validated before further instructions are executed. After validation, all further accesses to the GPRs are redirected to the global register bank.

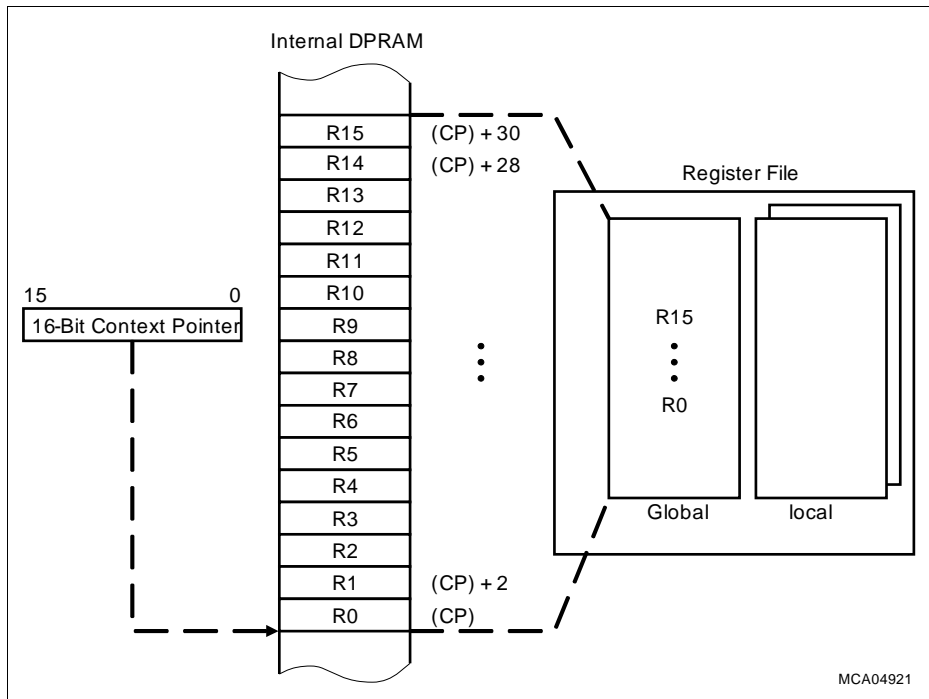


Figure 5-4 Register Bank Selection via Register CP

5.5.1 GPR Addressing Modes

Because the GPRs are the working registers and are accessed frequently, there are three possible ways to access a register bank:

- **Short GPR Address** (mnemonic: Rw or Rb)
- **Short Register Address** (mnemonic: reg or bitoff)
- **Long Memory Address** (mnemonic: mem), for the global bank only

Short GPR Addresses specify the register offset within the current register bank (selected via bitfield BANK). Short 4-bit GPR addresses can access all sixteen registers, short 2-bit addresses (used by some instructions) can access the lower four registers.

Depending on whether a register word (Rw) or byte (Rb) address is specified, the short GPR address is either multiplied by two (Rw) or not (Rb) before it is used to physically access the register bank. Thus, both byte and word GPR accesses are possible in this way.

Note: GPRs used as indirect address pointers are always accessed wordwise.

For the local register banks the resulting offset is used directly, for the global register bank the resulting offset is logically added to the contents of register CP which points to the memory location of the base of the current global register bank (see [Figure 5-5](#)).

Short 8-Bit Register Addresses within a range from $F0_H$ to FF_H interpret the four least significant bits as short 4-bit GPR addresses, while the four most significant bits are ignored. The respective physical GPR address is calculated in the same way as for short 4-bit GPR addresses. For single bit GPR accesses, the GPR's word address is calculated in the same way. The accessed bit position within the word is specified by a separate additional 4-bit value.

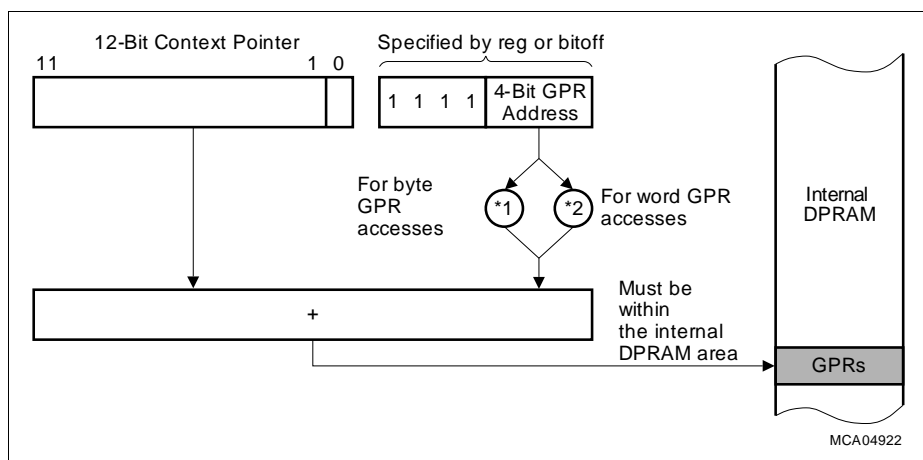


Figure 5-5 Implicit CP Use by Logical Short GPR Addressing Modes

Central Processing Unit (CPU)

24-Bit Memory Addresses can be directly used to access GPRs located in the DPRAM (not applicable for local register banks). In case of a memory read access, a hit detection logic checks if the accessed memory location is cached in the global register bank. In case of a cache hit the read is redirected to the global register bank. The data that is read from cache will be used and the read from memory will be discarded. This leads to a delay of one CPU cycle (MOV R4, **mem** [CP ≤ mem ≤ CP + 31]). In case of a memory write access, the hit detection logic determines a cache hit in advance. Nevertheless, the address conversion needs one additional CPU cycle. The value is directly written into the global register bank without further delay (MOV **mem**, R4).

Note: The 24-bit GPR addressing mode requires an extra cycle for the read and write access.

Table 5-14 Addressing Modes to Access GPRs

Word Registers ¹⁾		Byte Registers		Short Address ²⁾		
Name	Mem. Addr. ³⁾	Name	Mem. Addr. ³⁾	8-Bit	4-Bit	2-Bit
R0	(CP) + 0	RL0	(CP) + 0	F0 _H	0 _H	0 _H
R1	(CP) + 2	RH0	(CP) + 1	F1 _H	1 _H	1 _H
R2	(CP) + 4	RL1	(CP) + 2	F2 _H	2 _H	2 _H
R3	(CP) + 6	RH1	(CP) + 3	F3 _H	3 _H	3 _H
R4	(CP) + 8	RL2	(CP) + 4	F4 _H	4 _H	---
R5	(CP) + 10	RH2	(CP) + 5	F5 _H	5 _H	---
R6	(CP) + 12	RL3	(CP) + 6	F6 _H	6 _H	---
R7	(CP) + 14	RH3	(CP) + 7	F7 _H	7 _H	---
R8	(CP) + 16	RL4	(CP) + 8	F8 _H	8 _H	---
R9	(CP) + 18	RH4	(CP) + 9	F9 _H	9 _H	---
R10	(CP) + 20	RL5	(CP) + 10	FA _H	A _H	---
R11	(CP) + 22	RH5	(CP) + 11	FB _H	B _H	---
R12	(CP) + 24	RL6	(CP) + 12	FC _H	C _H	---
R13	(CP) + 26	RH6	(CP) + 13	FD _H	D _H	---
R14	(CP) + 28	RL7	(CP) + 14	FE _H	E _H	---
R15	(CP) + 30	RH7	(CP) + 15	FF _H	F _H	---

1) The first 8 GPRs (R7 ... R0) may also be accessed byte-wise. Writing to a GPR byte does not affect the other byte of the respective GPR.

2) Short addressing modes are usable for all register banks.

3) Long addressing mode only usable for the memory mapped global bank.

5.5.2 Context Switching

When a task scheduler of an operating system activates a new task or an interrupt service routine is called or terminated, the working context (i.e. the registers) of the left task must be saved and the working context of the new task must be restored. The CPU context can be changed in two ways:

- Switching the selected register bank
- Switching the context of the global register bank

Switching the Selected Physical Register Bank

By updating bitfield BANK in register PSW the active register bank is switched immediately. It is possible to switch between the current memory-mapped GPR bank cached in the global register bank (BANK = 00_B), local register bank 1 (BANK = 10_B), and local register bank 2 (BANK = 11_B).

In case of an interrupt service, the bank switch can be automatically executed by updating bitfield BANK from registers BNKSELx in the interrupt controller. By executing a RETI instruction, bitfield BANK will automatically be restored and the context will be switched to the original register bank.

The switch between the three physical register banks of the register file can also be executed by writing to bitfield BANK. Because of pipeline dependencies an explicit change of register PSW must cancel the pipeline.

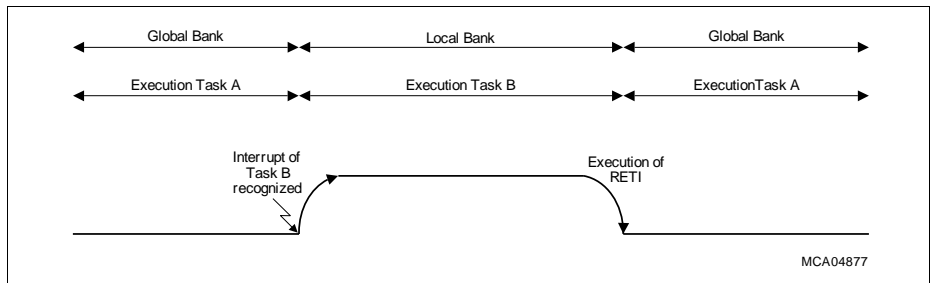


Figure 5-6 Context Switch by Changing the Physical Register Bank

After a switch to a local register bank, the new bank is immediately available. After switching to the global register bank, the cached memory-mapped GPRs must be valid before any further instructions can be executed. If the global register bank is not valid at this time (in case if the context switch process has been interrupted), the cache validation process is started automatically.

Switching the Context of the Global Register Bank

The contents of the global register bank are switched by changing the base address of the memory-mapped GPR bank. The base address is given by the contents of the Context Pointer (CP).

After the CP has been updated, a state machine starts to store the old contents of the global register bank and to load the new one. The store and load algorithm is executed in nineteen CPU cycles: the execution of the cache validation process takes sixteen cycles plus three cycles to stall an instruction execution to avoid pipeline conflicts upon the completion of the validation process. The context switch process has two phases:

- **Store phase:** The contents of the global register bank¹⁾ is stored back into the DPRAM by executing eight injected STORE instructions. After the last STORE instruction the contents of the global register bank are invalidated.
- **Load phase:** The global register bank is loaded with the new context by executing eight injected LOAD instructions. After the last LOAD instruction the contents of the global register bank are validated.

The code execution is stopped until the global register bank is valid again. A hardware interrupt can occur during the validation process. The way the validation process is completed depends on the type of register bank selected for this interrupt:

- If the interrupt also uses a global register bank the validation process is finished before executing the service routine (see [Figure 5-7](#)).
- If the interrupt uses a local register bank the validation process is interrupted and the service routine is executed immediately (see [Figure 5-8](#)). After switching back to the global register bank, the validation process is finished:
 - If the interrupt occurred during the store phase, the entire validation process is restarted from the very beginning.
 - If the interrupt occurred during the load phase, only the load phase is repeated.

If a local-bank interrupt routine (Task B in [Figure 5-9](#)) is again interrupted by a global-bank interrupt (Task C), the suspended validation process must be finished before code of Task C can be executed. This means that the validation process of Task A does not affect the interrupt latency of Task B but the latency of Task C.

Note: If Task C would immediately interrupt Task A, the register bank validation process of Task A would be finished first. The worst case interrupt latency is identical in both cases (see [Figure 5-7](#) and [Figure 5-9](#)).

¹⁾ During the store phase of the context switch the complete register bank is written to the DPRAM even if the application only uses a part of this register bank. A register bank must not be located above FDE0_H, otherwise the store phase will overwrite SFRs (beginning at FE00_H).

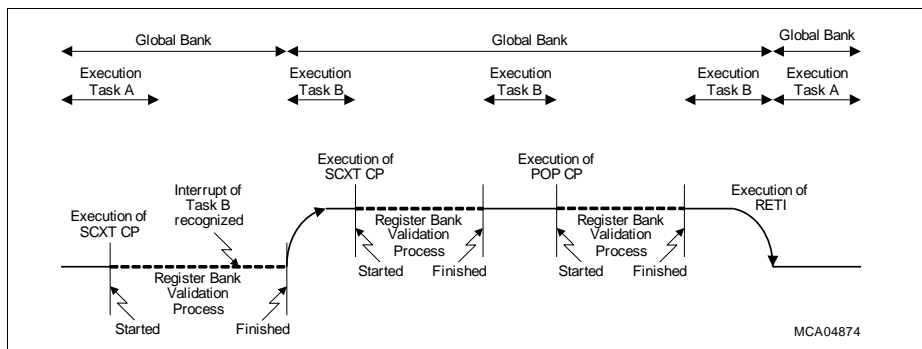


Figure 5-7 Validation Process Interrupted by Global-Bank Interrupt

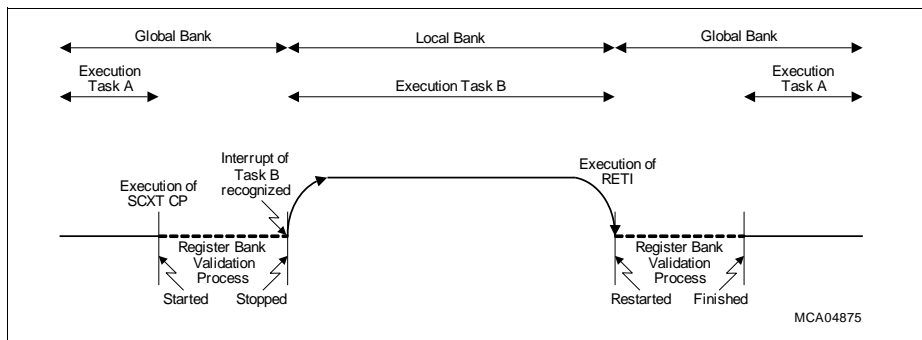


Figure 5-8 Validation Process Interrupted by Local-Bank Interrupt

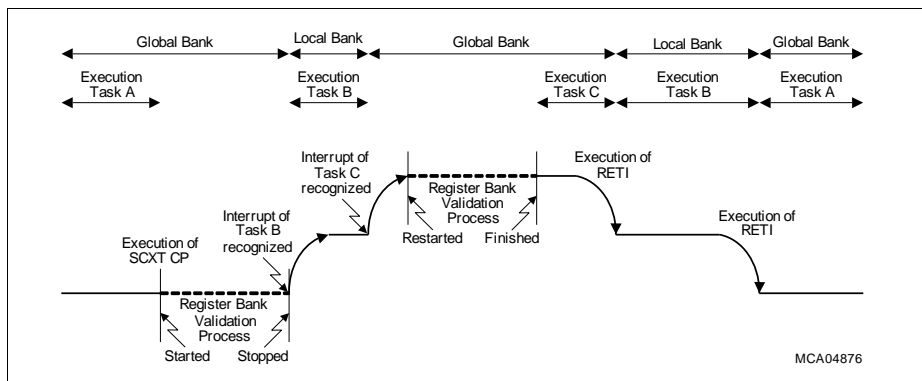


Figure 5-9 Validation Process Interrupted by Local- and Global-Bank Intr.

5.5.2.1 The Context Pointer (CP)

This non-bit-addressable register selects the current global register bank context. It can be updated via any instruction capable of modifying SFRs.

CP

Context Pointer

SFR (FE10_H/08_H)

Reset Value: FC00_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1												0
r	r	r	r						rw						r

Field	Bits	Type	Description
1	15, 14, 13, 12	r	Fixed part of CP Read as 1
CP	[11:1]	rw	Modifiable part of CP Specifies bits [11:1] of the 16-bit base address of the current global (memory-mapped) register bank. When writing a value to register CP with bits CP[11:9] = 000 _B , bits CP[11:10] are set to 11 _B by hardware.
0	0	r	Fixed part of CP Read as 0

Note: It is the user's responsibility to ensure that the physical GPR address specified via CP register plus short GPR address is always an internal DPRAM location. If this condition is not met, unexpected results may occur. Do not set CP below the internal DPRAM start address. Do not set CP above FDE0_H, otherwise the store phase will overwrite SFRs (beginning at FE00_H).

The XC27x8X switches the complete memory-mapped GPR bank with a single instruction. After switching, the service routine executes within its own separate context. The instruction "SCXT CP, #New_Bank" pushes the value of the current context pointer (CP) into the system stack and loads CP with the immediate value "New_Bank", which selects a new register bank. The service routine may now use its "own registers". This memory register bank is preserved when the service routine terminates, i.e. its contents are available on the next call.

Before returning from the service routine (RETI), the previous CP is simply popped from the system stack which returns the registers to the original bank.

Note: Due to the internal instruction pipeline, a write operation to the CP register stalls the instruction flow until the register file context switch is really executed. The

Central Processing Unit (CPU)

instruction immediately following the instruction that updates CP register can use the new value of the changed CP.

5.6 Code Addressing

The XC27x8X provides a total addressable memory space of 16 Mbytes. This address space is arranged as 256 segments of 64 Kbytes each. A dedicated 24-bit code address pointer is used to access the memories for instruction fetches. This pointer has two parts: an 8-bit code segment pointer CSP and a 16-bit offset pointer called Instruction Pointer (IP). The concatenation of the CSP and IP results directly in a correct 24-bit physical memory address.

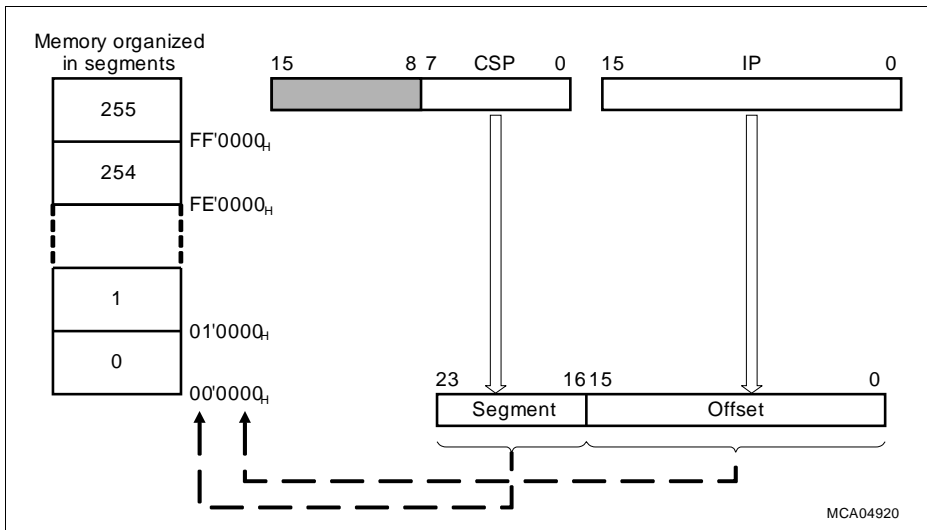


Figure 5-10 Addressing via the Code Segment and Instruction Pointer

The Code Segment Pointer CSP selects the code segment being used at run-time to access instructions. The lower 8 bits of register CSP select one of up to 256 segments of 64 Kbytes each, while the higher 8 bits are reserved for future use. The hardware reset value is 0000_H, but immediately after reset it is loaded with the contents of the VECSEG register due to an injected MOVCSIP instruction.

Note: Register CSP can only be read but cannot be written by data operations.

In segmented memory mode (default after reset), register CSP is modified either directly by Jumps and Calls instructions, or indirectly via the stack by RETs and RETI instructions.

In non-segmented memory mode (selected by setting bit SGTDIS in register CPUCON1), CSP is fixed to the segment of the instruction that disabled segmentation. Modification by inter-segment CALLs or RETurns is no longer possible.

Central Processing Unit (CPU)

For processing an accepted interrupt or a TRAP, register CSP is automatically loaded with the segment of the vector table (defined in register VECSEG).

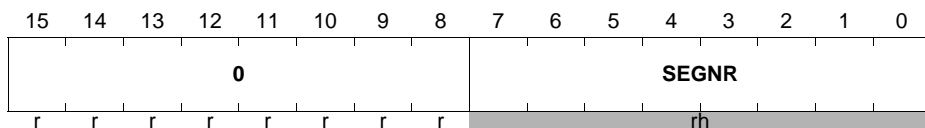
Note: For the correct execution of interrupt tasks in non-segmented memory mode, the contents of VECSEG must select the same segment as the current value of CSP, i.e. the vector table must be located in the segment pointed to by the CSP.

CSP

Code Segment Pointer

SFR (FE08_H/04_H)

Reset Value: 0000_H



Field	Bits	Type	Description
0	[15:8]	r	Reserved Read as 0, should be written 0
SEGNR	[7:0]	rh	Segment Number Specifies the code segment from which the current instruction is to be fetched.

Note: After a reset, register CSP is automatically loaded from register VECSEG.

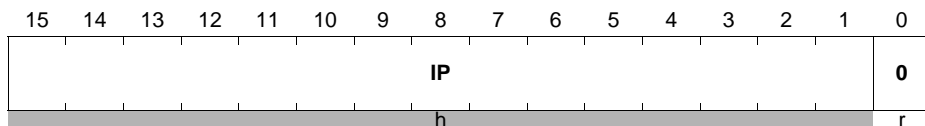
The Instruction Pointer IP determines the 16-bit intra-segment address of the currently fetched instruction within the code segment selected by the CSP register. Register IP is not mapped into the XC27x8X's address space; thus, it is not directly accessible by the programmer. However, the IP can be modified indirectly via the stack by means of a return instruction. IP is implicitly updated by the CPU for branch instructions and after instruction fetch operations.

IP

Instruction Pointer

(not addressable)

Reset Value: 0000_H



Central Processing Unit (CPU)

Field	Bits	Type	Description
IP	[15:1]	h	Instruction Pointer Specifies bits [15:1] of the intra segment offset from which the current instruction is to be fetched. IP refers to the current segment <SEGNR>.
0	0	r	Fixed part of IP Read as 0

5.7 Data Addressing

The Address Data Unit (ADU) contains two independent arithmetic units to generate, calculate, and update addresses for data accesses, the Standard Address Generation Unit (SAGU) and the DSP Address Generation Unit (DAGU). The ADU performs the following major tasks:

- Standard Address Generation (SAGU)
- DSP Address Generation (DAGU)
- Data Paging (SAGU)
- Stack Handling (SAGU)

The SAGU supports linear arithmetic for the indirect addressing modes and also generates the address in case of all other short and long addressing modes.

The DAGU contains an additional set of address pointers and offset registers which are used in conjunction with the CoXXX instructions only.

The CPU provides a lot of powerful addressing modes (short, long, indirect) for word, byte, and bit data accesses. The different addressing modes use different formats and have different scopes.

5.7.1 Short Addressing Modes

Short addressing modes allow access to the GPR, SFR or bit-addressable memory space. All of these addressing modes use an offset (8/4/2 bits) together with an implicit base address to specify a 24-bit physical address:

Table 5-15 Short Addressing Modes

Mnemonic	Base Address ¹⁾	Offset	Short Address Range	Scope of Access
Rw	(CP)	$2 \times \text{Rw}$	0 ... 15	GPRs (word)
Rb	(CP)	$1 \times \text{Rb}$	0 ... 15	GPRs (byte)
reg	00'FE00 _H 00'F000 _H (CP) (CP)	$2 \times \text{reg}$ $2 \times \text{reg}$ $2 \times (\text{reg} \wedge 0\text{F}_{\text{H}})$ $1 \times (\text{reg} \wedge 0\text{F}_{\text{H}})$	00 _H ... EF _H 00 _H ... EF _H F0 _H ... FF _H F0 _H ... FF _H	SFRs (word, low byte) ESFRs (word, low byte) GPRs (word) GPRs (bytes)
bitoff	00'FD00 _H 00'FF00 _H 00'F100 _H (CP)	$2 \times \text{bitoff}$ $2 \times (\text{bitoff} \wedge 7\text{F}_{\text{H}})$ $2 \times (\text{bitoff} \wedge 7\text{F}_{\text{H}})$ $2 \times (\text{bitoff} \wedge 0\text{F}_{\text{H}})$	00 _H ... 7F _H 80 _H ... EF _H 80 _H ... EF _H F0 _H ... FF _H	RAM Bit word offset SFR Bit word offset ESFR Bit word offset GPR Bit word offset
bitaddr	Bit word see bitoff	Immediate bit position	0 ... 15	Any single bit

1) Accesses to general purpose registers (GPRs) may also access local register banks, instead of using CP.

Physical Address = Base Address + $\Delta \times$ Short Address

Note: Δ is 1 for byte GPRs, Δ is 2 for word GPRs.

Rw, Rb: Specifies direct access to any GPR in the currently active context (global register bank or local register bank). Both 'Rw' and 'Rb' require four bits in the instruction format. The base address of the global register bank is determined by the contents of register CP. 'Rw' specifies a 4-bit word GPR address, 'Rb' specifies a 4-bit byte GPR address within a local register bank or relative to (CP).

reg: Specifies direct access to any (E)SFR or GPR in the currently active context (global or local register bank). The 'reg' value requires eight bits in the instruction format. Short 'reg' addresses in the range from 00_H to EF_H always specify (E)SFRs. In that case, the factor ' Δ ' equates 2 and the base address is 00'FE00_H for the standard SFR area or 00'F000_H for the extended ESFR area. The 'reg' accesses to the ESFR area require a preceding EXT*R instruction to switch the base address. Depending on the opcode, either the total word (for word operations) or the low byte (for byte operations) of an SFR can be addressed via 'reg'. Note that the high byte of an SFR cannot be accessed via the 'reg' addressing mode. Short 'reg' addresses in the range from F0_H to FF_H always specify GPRs. In that case, only the lower four bits of 'reg' are significant for physical address generation and, therefore, it is identical to the address generation described for the 'Rb' and 'Rw' addressing modes.

bitoff: Specifies direct access to any word in the bit addressable memory space. The 'bitoff' value requires eight bits in the instruction format. The specified 'bitoff' range selects different base addresses to generate physical addresses (see [Table 5-15](#)). The 'bitoff' accesses to the ESFR area require a preceding EXT*R instruction to switch the base address.

bitaddr: Any bit address is specified by a word address within the bit addressable memory space (see 'bitoff') and a bit position ('bitpos') within that word. Therefore, 'bitaddr' requires twelve bits in the instruction format.

5.7.2 Long Addressing Modes

Long addressing modes specify 24-bit addresses and, therefore, can access any word or byte data within the entire address space. Long addresses can be specified in different ways to generate the full 24-bit address:

- **Use one of the four Data Page Pointers (DPP registers):** The used 16-bit pointer selects a DPP with bits 15 ... 14, bits 13 ... 0 specify the 14-bit data page offset (see [Figure 5-11](#)).
- **Select the used data page directly:** The data page is selected by a preceding EXTP(R) instruction, bits 13 ... 0 of the used 16-bit pointer specify the 14-bit data page offset.
- **Select the used segment directly:** The segment is selected by a preceding EXT(S) instruction, the used 16-bit pointer specifies the 16-bit segment offset.

Note: Word accesses on odd byte addresses are not executed. A hardware trap will be triggered.

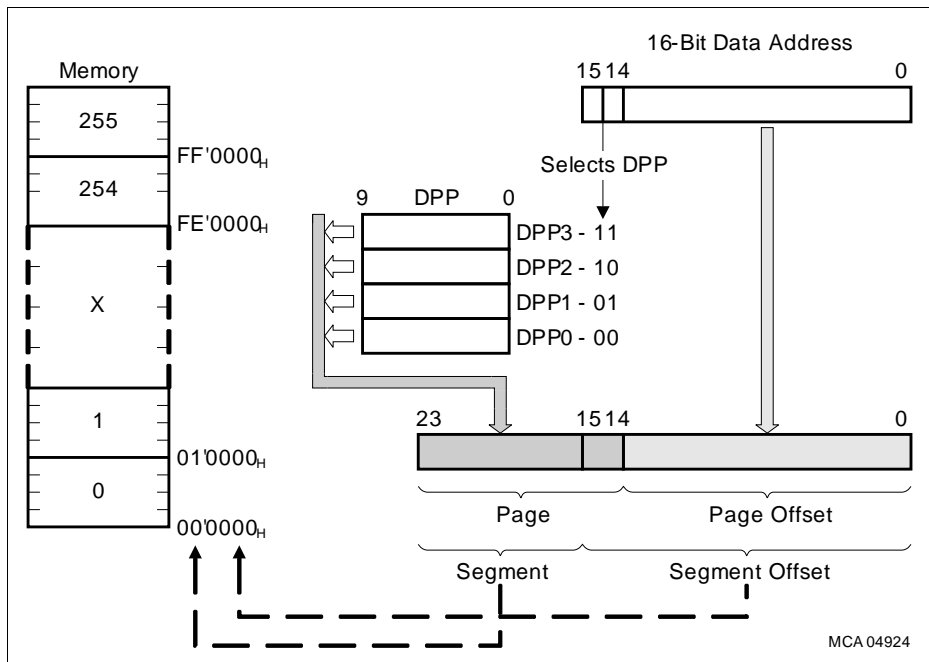


Figure 5-11 Data Page Pointer Addressing

5.7.2.1 Data Page Pointers DPP0, DPP1, DPP2, DPP3

These four non-bit-addressable registers select up to four different data pages to be active simultaneously at run-time. The lower 10 bits of each DPP register select one of the 1024 possible 16-Kbyte data pages; the upper 6 bits are reserved for future use.

DPP0

Data Page Pointer 0 **SFR (FE00_H/00_H)** **Reset Value: 0000_H**

DPP1

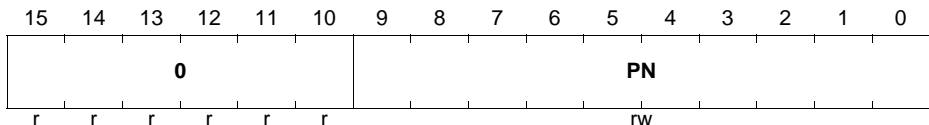
Data Page Pointer 1 **SFR (FE02_H/01_H)** **Reset Value: 0001_H**

DPP2

Data Page Pointer 2 **SFR (FE04_H/02_H)** **Reset Value: 0002_H**

DPP3

Data Page Pointer 3 **SFR (FE06_H/03_H)** **Reset Value: 0003_H**



Field	Bits	Type	Description
0	[15:8]	r	Reserved Read as 0, should be written 0
PN	[9:0]	rw	Data Page Number of DPPx Specifies the data page selected via DPPx.

The DPP registers allow access to the entire memory space in pages of 16 Kbytes each. The DPP registers are implicitly used whenever data accesses to any memory location are made via indirect or direct long 16-bit addressing modes (except for override accesses via EXTended instructions and PEC data transfers). After reset, the Data Page Pointers are initialized in such a way that all indirect or direct long 16-bit addresses result in identical 18-bit addresses. This allows access to data pages 3 ... 0 within segment 0 as shown in [Figure 5-11](#). If the user does not want to use data paging, no further action is required.

Data paging is performed by concatenating the lower 14 bits of an indirect or direct long 16-bit address with the contents of the DPP register selected by the upper two bits of the 16-bit address. The contents of the selected DPP register specify one of the 1024 possible data pages. This data page base address together with the 14-bit page offset forms the physical 24-bit address (even if segmentation is disabled).

A DPP register can be updated via any instruction capable of modifying an SFR.

Central Processing Unit (CPU)

Note: Due to the internal instruction pipeline, a write operation to the DPPx registers could stall the instruction flow until the DPP is actually updated. The instruction that immediately follows the instruction which updates the DPP register can use the new value of the changed DPPx.

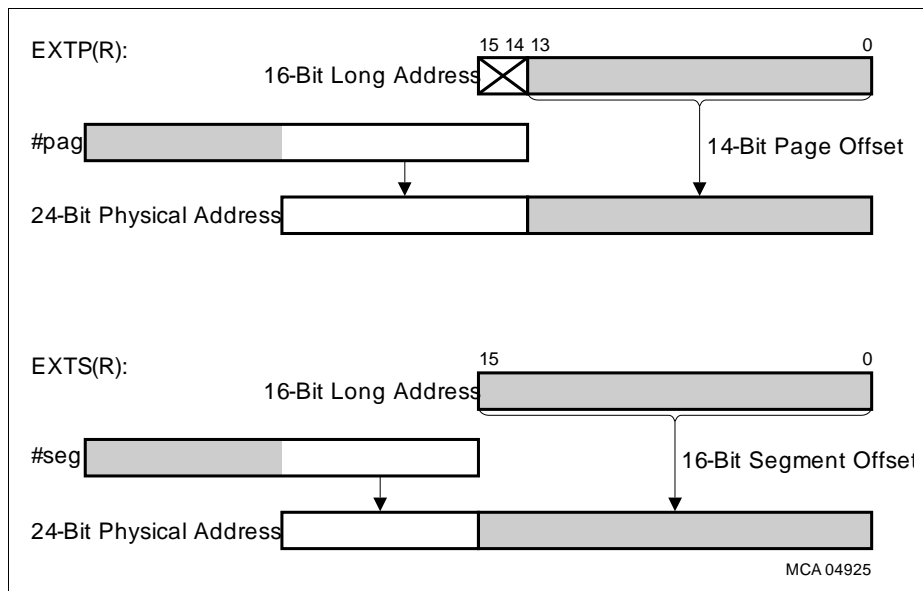


Figure 5-12 Overriding the DPP Mechanism

Note: The overriding page or segment may be specified as a constant (#pag, #seg) or via a word GPR (Rw).

Table 5-16 Long Addressing Modes

Mnemonic	Base Address ¹⁾	Offset	Scope of Access
mem	(DPPx)	mem \wedge 3FFF _H	Any Word or Byte
mem	pag	mem \wedge 3FFF _H	Any Word or Byte
mem	seg	mem	Any Word or Byte

1) Represents either a 10-bit data page number to be concatenated with a 14-bit offset, or an 8-bit segment number to be concatenated with a 16-bit offset.

5.7.3 Indirect Addressing Modes

Indirect addressing modes can be considered as a combination of short and long addressing modes. This means that the “long” 16-bit pointer is provided indirectly by the contents of a word GPR which itself is specified directly by a short 4-bit address ($Rw' = 0 \dots 15$).

There are indirect addressing modes, which add a constant value to the GPR contents before the long 16-bit address is calculated. Other indirect addressing modes can decrement or increment the indirect address pointers (GPR contents) by 2 or 1 (referring to words or bytes) or by the contents of the offset registers QR0 or QR1.

Table 5-17 Generating Physical Addresses from Indirect Pointers

Step	Executed Action	Calculation	Notes
1	Calculate the address of the indirect pointer (word GPR) from its short address	GPR Address = $2 \times \text{Short Addr.} [+ (CP)]$	see Table 5-15
2	Pre-decrement indirect pointer ($'Rw'$) depending on datatype ($\Delta = 1$ or 2 for byte or word operations)	(GPR Address) = (GPR Address) - Δ	Optional step, executed only if required by addressing mode
3	Adjust the pointer by a constant value ($'Rw + \text{const16}'$)	Pointer = (GPR Address) + Constant	Optional step, executed only if required by addressing mode
4	Calculate the physical 24-bit address using the resulting pointer	Physical Addr. = Page/Segment + Pointer offset	Uses DPPs or page/segment override mechanisms, see Table 5-16
5	Post-in/decrement indirect pointer ($'Rw \pm'$) depending on datatype ($\Delta = 1$ or 2 for byte or word operations), or depending on offset registers ($\Delta = \text{QRx}$) ¹⁾	(GPR Address) = (GPR Address) $\pm \Delta$	Optional step, executed only if required by addressing mode

1) Post-decrement and QRx-based modification is provided only for CoXXX instructions.

Note: Some instructions only use the lowest four word GPRs ($R3 \dots R0$) as indirect address pointers, which are specified via short 2-bit addresses in that case.

The following indirect addressing modes are provided:

Table 5-18 Indirect Addressing Modes

Mnemonic	Particularities
[Rw]	Most instructions accept any GPR (R15 ... R0) as indirect address pointer. Some instructions accept only the lower four GPRs (R3 ... R0).
[Rw+]	The specified indirect address pointer is automatically post-incremented by 2 or 1 (for word or byte data operations) after the access.
[-Rw]	The specified indirect address pointer is automatically pre-decremented by 2 or 1 (for word or byte data operations) before the access.
[Rw + #data16]	The specified 16-bit constant is added to the indirect address pointer, before the long address is calculated.
[Rw-]	The specified indirect address pointer is automatically post-decremented by 2 (word data operations) after the access.
[Rw + QRx]	The specified indirect address pointer is automatically post-incremented by QRx (word data operations) after the access.
[Rw - QRx]	The specified indirect address pointer is automatically post-decremented by QRx (word data operations) after the access.

5.7.3.1 Offset Registers QR0 and QR1

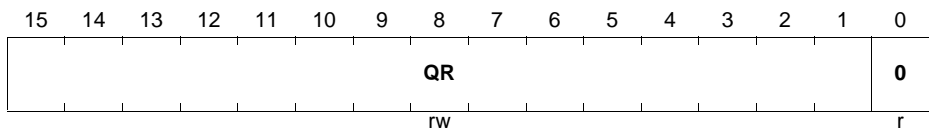
The non-bit-addressable offset registers QR0 and QR1 are used with CoXXX instructions. For possible instruction flow stalls refer to [Section 5.3.2.4](#).

QR0

Offset Register **ESFR (F004_H/02_H)** **Reset Value: 0000_H**

QR1

Offset Register **ESFR (F006_H/03_H)** **Reset Value: 0000_H**



Field	Bits	Type	Description
QR	[15:1]	rw	Modifiable part of QRx Specifies the 16-bit offset address for indirect addressing modes (LSB always zero).
0	0	r	Fixed part of QRx Read as 0

Central Processing Unit (CPU)

There are indirect addressing modes which allow parallel data move operations before the long 16-bit address is calculated (see [Figure 5-14](#) for an example). Other indirect addressing modes allow decrementing or incrementing the indirect address pointers (IDXx contents) by 2 or by the contents of the offset registers QX0 and QX1 (used in conjunction with the IDX pointers).

QX0

Offset Register

ESFR (F000_H/00_H)

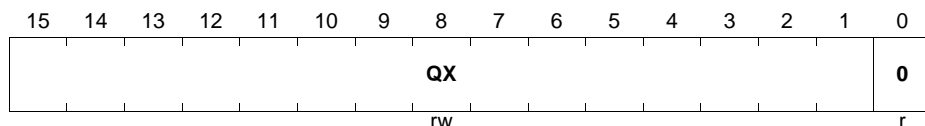
Reset Value: 0000_H

QX1

Offset Register

ESFR (F002_H/01_H)

Reset Value: 0000_H



Field	Bits	Type	Description
QX	[15:1]	rw	Modifiable part of QXx Specifies the 16-bit word offset for indirect addressing modes
0	0	r	Fixed part of QXx Read as 0

Note: During the initialization of the QX registers, instruction flow stalls are possible. For the proper operation, refer to [Section 5.3.2.4](#).

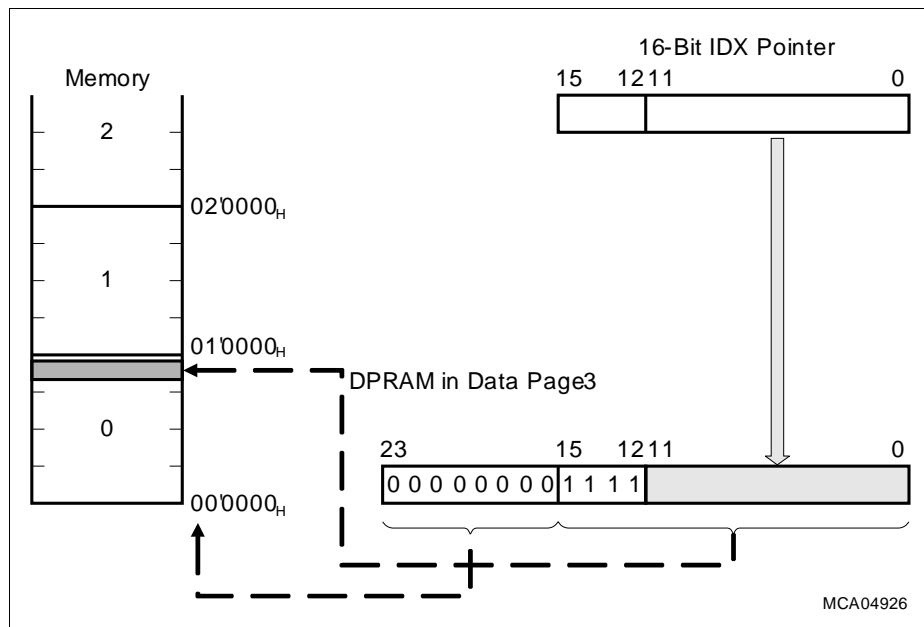


Figure 5-13 Arithmetic MAC Operations and Addressing via the IDX Pointers

Table 5-19 Generating Physical Addresses from Indirect Pointers (IDXx)

Step	Executed Action	Calculation	Notes
1	Determine the used IDXx pointer	---	—
2	Calculate an intermediate long address for the parallel data move operation and in/decrement indirect pointer ('IDXx±') by 2 ($\Delta = 2$), or depending on offset registers ($\Delta = QXx$)	Interm. Addr. = (IDXx Address) $\pm \Delta$	Optional step, executed only if required by instruction CoXXXM and addressing mode
3	Calculate long 16-bit address	Long Address = (IDXx Pointer)	—

Central Processing Unit (CPU)

Table 5-19 Generating Physical Addresses from Indirect Pointers (IDXx) (cont'd)

Step	Executed Action	Calculation	Notes
4	Calculate the physical 24-bit address using the resulting pointer	Physical Addr. = Page/Segment + Pointer offset	Uses DPPs or page/segment override mechanisms, see Table 5-16 and Figure 5-13
5	Post-in/decrement indirect pointer ('IDXx±') by 2 ($\Delta = 2$), or depending on offset registers ($\Delta = QXx$)	(IDXx Pointer) = (IDXx Pointer) $\pm \Delta$	Optional step, executed only if required by addressing mode

The following indirect addressing modes are provided:

Table 5-20 DSP Addressing Modes

Mnemonic	Particularities
[IDXx]	Most CoXXX instructions accept IDXx (IDX0, IDX1) as an indirect address pointer.
[IDXx+]	The specified indirect address pointer is automatically post-incremented by 2 after the access.
with parallel data move	In case of a CoXXXM instruction, the address stored in the specified indirect address pointer is automatically pre-decremented by 2 for the parallel move operation. The pointer itself is not pre-decremented. Then, the specified indirect address pointer is automatically post-incremented by 2 after the access.
[IDXx-]	The specified indirect address pointer is automatically post-decremented by 2 after the access.
with parallel data move	In case of a CoXXXM instruction, the address stored in the specified indirect address pointer is automatically pre-incremented by 2 for the parallel move operation. The pointer itself is not pre-incremented. Then, the specified indirect address pointer is automatically post-decremented by 2 after the access.
[IDXx + QXx]	The specified indirect address pointer is automatically post-incremented by QXx after the access.
with parallel data move	In case of a CoXXXM instruction, the address stored in the specified indirect address pointer is automatically pre-decremented by QXx for the parallel move operation. The pointer itself is not pre-decremented. Then, the specified indirect address pointer is automatically post-incremented by QXx after the access.

Table 5-20 DSP Addressing Modes (cont'd)

Mnemonic	Particularities
[IDXx - QXx]	The specified indirect address pointer is automatically post-decremented by QXx after the access.
with parallel data move	In case of a CoXXXM instruction, the address stored in the specified indirect address pointer is automatically pre-incremented by QXx for the parallel move operation. The pointer itself is not pre-incremented. Then, the specified indirect address pointer is automatically post-decremented by QXx after the access.

Note: An example for parallel data move operations can be found in [Figure 5-14](#).

The CoREG Addressing Mode

The CoSTORE instruction utilizes the special CoREG addressing mode for immediate storage of the MAC-Unit register after a MAC operation. The address of the MAC-Unit register is coded in the CoSTORE instruction format as described in [Table 5-21](#):

Table 5-21 Coding of the CoREG Addressing Mode

Mnemonic	Register	Coding of www:w bits [31:27]
MSW	MAC-Unit Status Word	00000 _B
MAH	MAC-Unit Accumulator High Word	00001 _B
MAS	Limited MAC-Unit Accumulator High Word	00010 _B
MAL	MAC-Unit Accumulator Low Word	00100 _B
MCW	MAC-Unit Control Word	00101 _B
MRW	MAC-Unit Repeat Word	00110 _B

The example in [Figure 5-14](#) shows the complex operation of CoXXXM instructions with a parallel move operation based on the descriptions about addressing modes given in [Section 5.7.3 \(Indirect Addressing Modes\)](#) and [Section 5.7.4 \(DSP Addressing Modes\)](#).

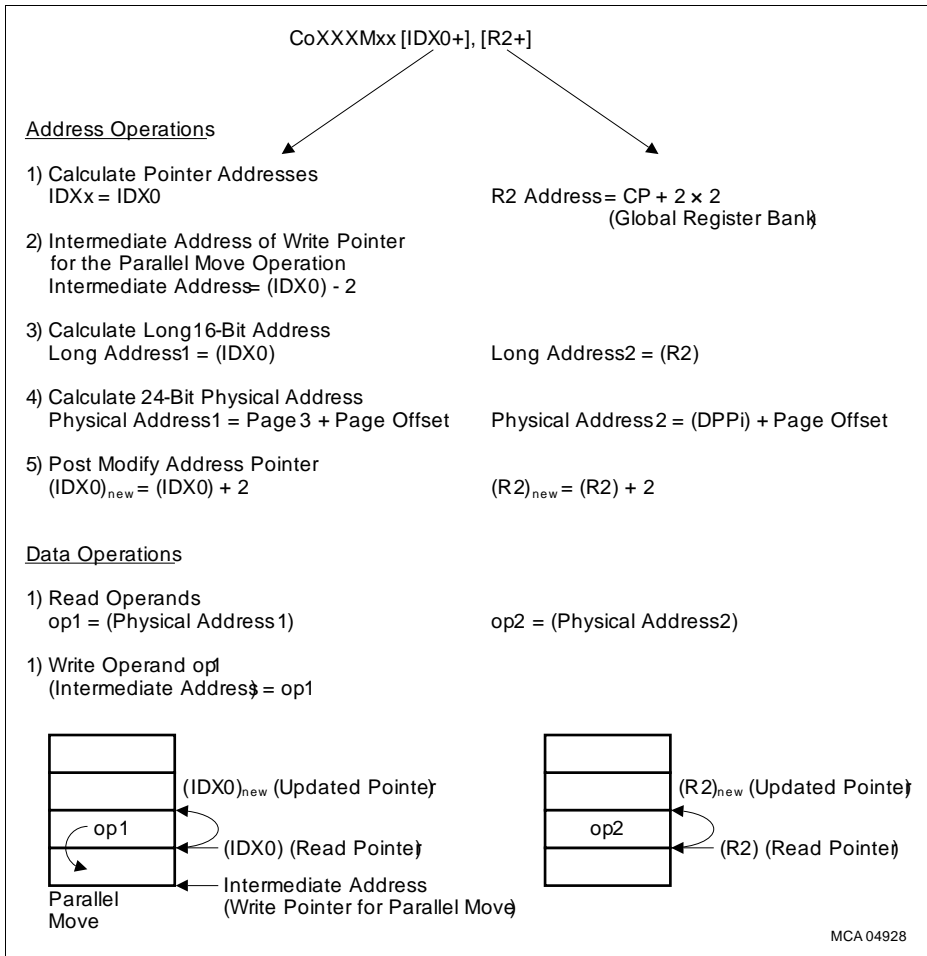


Figure 5-14 Arithmetic MAC Operations with Parallel Move

5.7.5 The System Stack

The XC27x8X supports a system stack of up to 64 Kbytes. The stack can be located internally in one of the on-chip memories or externally. The 16-bit Stack Pointer register (SP) addresses the stack within a 64-Kbyte segment selected by the Stack Pointer Segment register (SPSG). A virtual stack (usually bigger than 64 Kbytes) can be implemented by software. This mechanism is supported by the Stack Overflow register STKOV and the Stack Underflow register STKUN (see descriptions below).

5.7.5.1 The Stack Pointer Registers SP and SPSEG

Register SPSEG (not bit addressable) selects the segment being used at run-time to access the system stack. The lower eight bits of register SPSEG select one of up to 256 segments of 64 Kbytes each, while the higher 8 bits are reserved for future use.

The Stack Pointer SP (not bit addressable) points to the top of the system stack (TOS). SP is pre-decremented whenever data is pushed onto the stack, and it is post-incremented whenever data is popped from the stack. Therefore, the system stack grows from higher towards lower memory locations.

System stack addresses are generated by directly extending the 16-bit contents of register SP by the contents of register SPSEG, as shown in [Figure 5-15](#).

The system stack cannot cross a 64-Kbyte segment boundary.

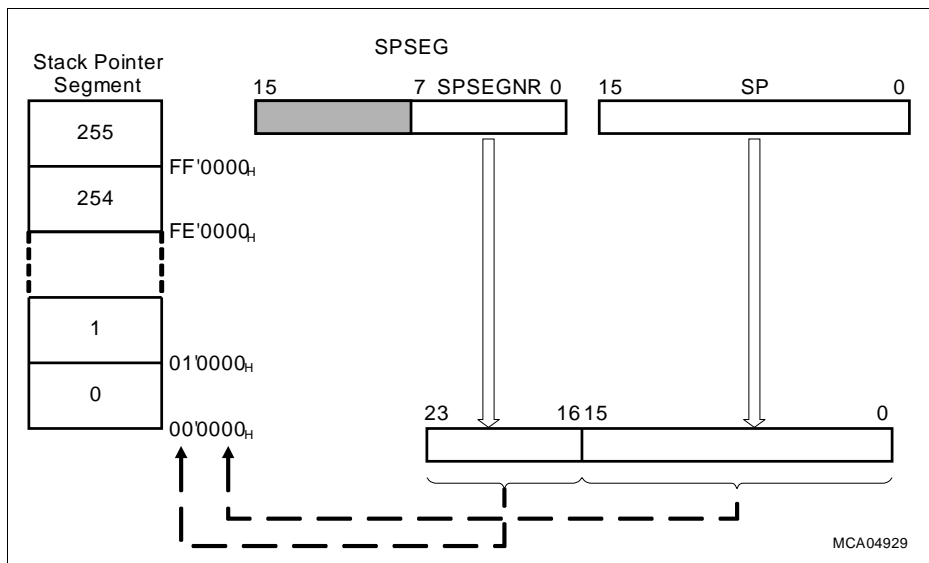


Figure 5-15 Addressing via the Stack Pointer

SP

Stack Pointer

SFR (FE12_H/09_H)

Reset Value: FC00_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SP															0
rw															r

Field	Bits	Type	Description
SP	[15:1]	rw	Modifiable part of SP Specifies bits [15:1] of the 16-bit system stack pointer intra segment address
0	0	r	Fixed part of SP Read as 0

SPSEG

Stack Pointer Segment

SFR (FF0C_H/86_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								SPSEGNR							
r	r	r	r	r	r	r	r	rw							

Field	Bits	Type	Description
0	[15:8]	r	Reserved Read as 0, should be written 0
SPSEGNR	[7:0]	rw	Stack Pointer Segment Number Specifies the segment where the stack is located.

Note: SPSEG and SP can be updated via any instruction capable of modifying a 16-bit SFR. Due to the internal instruction pipeline, a write operation to SPSEG or SP stalls the instruction flow until the register is really updated. The instruction immediately following the instruction updating SPSEG or SP can use the new value.

5.7.5.2 The Stack Overflow/Underflow Pointers STKOV/STKUN

These limit registers (not bit-addressable) supervise the stack pointer. A trap is generated when the stack pointer reaches its upper or lower limit. The Stack Pointer Segment Register SPSG is not taken into account for the stack pointer comparison. The system stack cannot cross a 64-Kbyte segment.

STKOV is compared with SP before each implicit write operation which decrements the contents of SP (instructions CALLA, CALLI, CALLR, CALLS, PCALL, TRAP, SCXT, or PUSH). If the contents of SP are equal to the contents of STKOV a stack overflow trap is triggered.

STKUN is compared with SP before each implicit read operation which increments the contents of SP (instructions RET, RETS, RETP, RETI, or POP). If the contents of SP are equal to the contents of STKUN a stack underflow trap is triggered.

The Stack Overflow/Underflow Traps may be used in two different ways:

- **Fatal error indication** treats the stack overflow as a system error and executes the associated trap service routine.
In case of a stack overflow trap, data in the bottom of the stack may have been overwritten by the status information stacked upon servicing the trap itself.
- **Virtual stack control** allows the system stack to be used as a 'Stack Cache' for a bigger external user stack: flush cache in case of an overflow, refill cache in case of an underflow.

Scope of Stack Limit Control

The stack limit control implemented by the register pair STKOV and STKUN detects cases in which the Stack Pointer (SP) crosses the defined stack area as a result of an implicit change.

If the stack pointer was explicitly changed as a result of move or arithmetic instruction, SP is not compared to the contents of STKOV and STKUN. In this case, a stack violation will not be detected if the modified stack pointer is on or outside the defined limits, i.e. below (STKOV) or above (STKUN). Stack overflow/underflow is detected only in case of implicit SP modification.

SP may be operated outside the permitted SP range without triggering a trap. However, if SP reaches the limit of the permitted SP range from outside the range as a result of an implicit change (PUSH or POP, for example), the respective trap will be triggered.

Note: STKOV and STKUN can be updated via any instruction capable of modifying an SFR. If a stack overflow or underflow event occurs in an ATOMIC/EXT sequence, the stack operations that are part of the sequence are completed. The trap is issued after the completion of the entire ATOMIC/EXT sequence.

STKOV

Stack Overflow Pointer

SFR (FE14_H/0A_H)

Reset Value: FA00_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STKOV															0
rw															r

Field	Bits	Type	Description
STKOV	[15:1]	rw	Modifiable part of STKOV Specifies the segment offset address of the lower limit of the system stack.
0	0	r	Fixed part of STKOV Read as 0

STKUN

Stack Underflow Pointer

SFR (FE16_H/0B_H)

Reset Value: FC00_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STKUN															0
rw															r

Field	Bits	Type	Description
STKUN	[15:1]	rw	Modifiable part of STKUN Specifies the segment offset address of the upper limit of the system stack.
0	0	r	Fixed part of STKUN Read as 0

5.8 Standard Data Processing

All standard arithmetic, shift-, and logical operations are performed in the 16-bit ALU. In addition to the standard functions, the ALU of the XC27x8X includes a bit-manipulation unit and a multiply and divide unit. Most internal execution blocks have been optimized to perform operations on either 8-bit or 16-bit numbers. After the pipeline has been filled, most instructions are completed in one CPU cycle. The status flags are automatically updated in register PSW after each ALU operation and reflect the current state of the microcontroller. These flags allow branching upon specific conditions. Support of both signed and unsigned arithmetic is provided by the user selectable branch test. The status flags are also preserved automatically by the CPU upon entry into an interrupt or trap routine. Another group of bits represents the current CPU interrupt status. Two separate bits (USR0 and USR1) are provided as general purpose flags.

PSW

Processor Status Word						SFR (FF10 _H /88 _H)						Reset Value: 0000 _H			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ILVL				IEN	HLD EN_ PL1	BANK		USR 1	USR 0	PL0	E	Z	V	C	N
rwh				rw	rwh	rwh		rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
ILVL	[15:12]	rwh	CPU Priority Level 0 _H Lowest Priority ... F _H Highest Priority
IEN	11	rw	Global Interrupt/PEC Enable Bit 0 _B Interrupt/PEC requests are disabled 1 _B Interrupt/PEC requests are enabled
HLDEN_PL1	10	rwh	Hold Enable/Protection Level selection 1 0 _B external bus arbitration disabled or protection level 0/1 (refer to Table 5-23) 1 _B external bus arbitration enabled or protection level 2/3 (refer to Table 5-23)
BANK	[9:8]	rwh	Reserved for Register File Bank Selection 00 _B Global register bank 01 _B Reserved 10 _B Local register bank 1 11 _B Local register bank 2

Central Processing Unit (CPU)

Field	Bits	Type	Description
USR1	7	rwh	General Purpose Flag Can be used by application software. Also set when using repeated MAC instructions (Section 5.9.11)
USR0	6	rwh	General Purpose Flag Can be used by application software. Also set when using repeated MAC instructions (Section 5.9.11)
PL0	5	rwh	Protection Level selection 0 0 _B Protection level 0/2 (refer to Table 5-23) 1 _B Protection level 1/3 (refer to Table 5-23)
E	4	rwh	End of Table Flag 0 _B Source operand is neither 8000 _H nor 80 _H 1 _B Source operand is 8000 _H or 80 _H
Z	3	rwh	Zero Flag 0 _B ALU result is not zero 1 _B ALU result is zero
V	2	rwh	Overflow Flag 0 _B No Overflow produced 1 _B Overflow produced
C	1	rwh	Carry Flag 0 _B No carry/borrow bit produced 1 _B Carry/borrow bit produced
N	0	rwh	Negative Result 0 _B ALU result is not negative 1 _B ALU result is negative

ALU/MAC Status (N, C, V, Z, E)

The condition flags (N, C, V, Z, E) within the PSW indicate the ALU status after the most recently performed ALU operation. They are set by most of the instructions according to specific rules which depend on the ALU or data movement operation performed by an instruction.

After execution of an instruction which explicitly updates the PSW register, the condition flags cannot be interpreted as described below because any explicit write to the PSW register supersedes the condition flag values which are implicitly generated by the CPU. Explicitly reading the PSW register supplies a read value which represents the state of the PSW register after execution of the immediately preceding instruction.

Note: After reset, all of the ALU status bits are cleared.

Central Processing Unit (CPU)

N-Flag: For most of the ALU operations, the N-flag is set to 1, if the most significant bit of the result contains a 1; otherwise, it is cleared. In the case of integer operations, the N-flag can be interpreted as the sign bit of the result (negative: $N = 1$, positive: $N = 0$). Negative numbers are always represented as the 2's complement of the corresponding positive number. The range of signed numbers extends from -8000_H to $+7FFF_H$ for the word data type, or from -80_H to $+7F_H$ for the byte data type. For Boolean bit operations with only one operand, the N-flag represents the previous state of the specified bit. For Boolean bit operations with two operands, the N-flag represents the logical XORing of the two specified bits.

C-Flag: After an addition, the C-flag indicates that a carry from the most significant bit of the specified word or byte data type has been generated. After a subtraction or a comparison, the C-flag indicates a borrow which represents the logical negation of a carry for the addition.

This means that the C-flag is set to 1, if **no** carry from the most significant bit of the specified word or byte data type has been generated during a subtraction, which is performed internally by the ALU as a 2's complement addition, and, the C-flag is cleared when this complement addition caused a carry.

The C-flag is always cleared for logical, multiply and divide ALU operations, because these operations cannot cause a carry.

For shift and rotate operations, the C-flag represents the value of the bit shifted out last. If a shift count of zero is specified, the C-flag will be cleared. The C-flag is also cleared for a prioritize ALU operation, because a 1 is never shifted out of the MSB during the normalization of an operand.

For Boolean bit operations with only one operand, the C-flag is always cleared. For Boolean bit operations with two operands, the C-flag represents the logical ANDing of the two specified bits.

V-Flag: For addition, subtraction, and 2's complementation, the V-flag is always set to 1 if the result exceeds the range of 16-bit signed numbers for word operations (-8000_H to $+7FFF_H$), or 8-bit signed numbers for byte operations (-80_H to $+7F_H$). Otherwise, the V-flag is cleared. Note that the result of an integer addition, integer subtraction, or 2's complement is not valid if the V-flag indicates an arithmetic overflow.

For multiplication and division, the V-flag is set to 1 if the result cannot be represented in a word data type; otherwise, it is cleared. Note that a division by zero will always cause an overflow. In contrast to the result of a division, the result of a multiplication is valid whether or not the V-flag is set to 1.

Because logical ALU operations cannot produce an invalid result, the V-flag is cleared by these operations.

The V-flag is also used as a 'Sticky Bit' for rotate right and shift right operations. With only using the C-flag, a rounding error caused by a shift right operation can be estimated up to a quantity of one half of the LSB of the result. In conjunction with the V-flag, the C-flag allows evaluation of the rounding error with a finer resolution (see [Table 5-22](#)).

Central Processing Unit (CPU)

For Boolean bit operations with only one operand, the V-flag is always cleared. For Boolean bit operations with two operands, the V-flag represents the logical ORing of the two specified bits.

Table 5-22 Shift Right Rounding Error Evaluation

C-Flag	V-Flag	Rounding Error Quantity
0	0	No rounding error
0	1	$0 < \text{Rounding error} < \frac{1}{2} \text{ LSB}$
1	0	$\text{Rounding error} = \frac{1}{2} \text{ LSB}$
1	1	$\text{Rounding error} > \frac{1}{2} \text{ LSB}$

Z-Flag: The Z-flag is normally set to 1 if the result of an ALU operation equals zero, otherwise it is cleared.

For the addition and subtraction with carry, the Z-flag is only set to 1, if the Z-flag already contains a 1 and the result of the current ALU operation also equals zero. This mechanism is provided to support multiple precision calculations.

For Boolean bit operations with only one operand, the Z-flag represents the logical negation of the previous state of the specified bit. For Boolean bit operations with two operands, the Z-flag represents the logical NORing of the two specified bits. For the prioritize ALU operation, the Z-flag indicates whether the second operand was zero.

E-Flag: End of table flag. The E-flag can be altered by instructions which perform ALU or data movement operations. The E-flag is cleared by those instructions which cannot be reasonably used for table search operations. In all other cases, the E-flag value depends on the value of the source operand to signify whether the end of a search table is reached or not. If the value of the source operand of an instruction equals the lowest negative number which is representable by the data format of the corresponding instruction (8000_H for the word data type, or 80_H for the byte data type), the E-flag is set to 1; otherwise, it is cleared.

General Control Functions (USR0, USR1, BANK, HLDEN)

A few bits in register PSW are dedicated to general control functions. Thus, they are saved and restored automatically upon task switches and interrupts.

USR0/USR1-Flags: These bits can be set automatically during the execution of repeated MAC instructions. These bits can also be used as general flags by an application.

BANK: Bitfield BANK selects the currently active register bank (local or global). Bitfield BANK is updated implicitly by hardware upon entering an interrupt service routine, and by a RETI instruction. It can be also modified explicitly via software by any instruction which can write to PSW.

Central Processing Unit (CPU)

HLDEN: Setting this bit for the first time activates the selected bus arbitration mode. Bus arbitration can be disabled by temporarily clearing bit HLDEN. In this case the bus is locked, while the bus arbitration mode remains selected. Please refer to the External Bus Controller (EBC) chapter for functional details. Note that the HLDEN bit can be accessed only when memory protection (MPU) is disabled.

Protection Level (PL0, PL1)

These flags specify the current protection level of the system. This information is needed for systems implementing memory protection (i.e. MPU). Four different protection levels are defined according to the table below. Refer to the Memory Protection (MPU) chapter for more information on how the protection system works.

Table 5-23 Decoding of Protection Level

PL1	PL0	Protection Level
0	0	Protection Level 0
0	1	Protection Level 1
1	0	Protection Level 2
1	1	Protection Level 3

A write into bit PSW.10 will be interpreted as a write into PL1 when the MPU is enabled or as a write into HLDEN when the MPU is disabled. Considering this fact it is possible to use both the EBC arbitration and MPU functionalities. Note that software made to support the external master functionality, i.e. trying to write into this HLDEN bit, may not have write permission when the MPU is enabled unless it runs in privileged mode.

CPU Interrupt Status (IEN, ILVL)

IEN: The Interrupt Enable bit allows interrupts to be globally enabled (IEN = 1) or disabled (IEN = 0).

ILVL: The four-bit Interrupt Level field (ILVL) specifies the priority of the current CPU activity. The interrupt level is updated by hardware on entry into an interrupt service routine, but it can also be modified via software to prevent other interrupts from being acknowledged. If an interrupt level 15 has been assigned to the CPU, it has the highest possible priority; thus, the current CPU operation cannot be interrupted except by hardware traps or external non-maskable interrupts.

After reset, all interrupts are globally disabled, and the lowest priority (ILVL = 0) is assigned to the initial CPU activity.

5.8.1 16-bit Adder/Subtractor, Barrel Shifter, and 16-bit Logic Unit

All standard arithmetic and logical operations are performed by the 16-bit ALU. In case of byte operations, signals from bits 6 and 7 of the ALU result are used to control the

Central Processing Unit (CPU)

condition flags. Multiple precision arithmetic is supported by a "CARRY-IN" signal to the ALU from previously calculated portions of the desired operation.

A 16-bit barrel shifter provides multiple bit shifts in a single cycle. Rotations and arithmetic shifts are also supported.

5.8.2 Bit Manipulation Unit

The XC27x8X offers a large number of instructions for bit processing. These instructions are typically used to -

- manipulate software bit flags within CPU registers, GPRs or DPRAM
- control on-chip +Bus peripherals and port logic via control bits of their respective bit addressable (E)SFRs.

The bit manipulation instructions allow short addressing mode with bitoff operands only (see [Chapter 5.7.1](#)).

Note: All GPRs are bit-addressable independently from the allocation of the register bank via the Context Pointer (CP). Even GPRs which are allocated to non-bit-addressable RAM locations provide this feature.

Instructions BSET, BCLR, BAND, BOR, BXOR, BMOV, BMOVN explicitly set or clear specific bits. The bitfield instructions BFLDL and BFLDH allow masked manipulation of up to 8 bits of a specific byte at one time. The instructions JBC and JNBS implicitly clear or set the specified bit when the jump is taken. The instructions JB and JNB evaluate the specified bit to determine if the jump is to be taken.

Note: Bit operations on undefined bit locations will always read a bit value of '0', while the write access will not affect the respective bit location.

Bit protection using mask protected write

Instructions that manipulate single bits or bit groups either use a read-modify-write sequence or mask protected write to execute the operation.

The read-modify-write sequence accesses the whole word containing the specified bit(s). The read-modify-write approach may be critical with hardware affected bits of type 'rwh' or 'wh'. In these cases, the hardware may change other bits of the register while the read-modify-write operation is in progress. Thus the writeback could overwrite the new bit value generated by the hardware.

To handle this side effect operations on **bit addressable (E)SFR registers** support the bit protection mechanism using a mask protected write.

Example:

```
BCLR      EOPIC.EOPIE      ; disable 'end of PEC' interrupts
```

Central Processing Unit (CPU)

The instruction will clear the interrupt enable bit EOPIE while the 'rwh' bit EOPIR will be mask protected. This ensures that an EOP interrupt occurring exactly at the same time will be correctly flagged.

Note: For the BFLD(LH) instructions the protection mask must be supplied by the programmer.

*Note: If a direct conflict occurs between a bit manipulation generated by hardware and an intended software access on the **same** bit, the software access has priority and determines the final value of the respective bit.*

5.8.3 Multiply and Divide Unit

The XC27x8X's multiply and divide unit has two separated parts. One is the fast 16×16 -bit multiplier that executes a multiplication in one CPU cycle. The other one is a division sub-unit which performs the division algorithm in 18 ... 21 CPU cycles (depending on the data and division types). The divide instruction requires four CPU cycles to be executed. For performance reasons, the rest of the division algorithm runs in the background during the following seventeen CPU cycles, while further instructions are executed in parallel. Interrupt tasks can also be started and executed immediately without any delay. If an instruction (from the original instruction stream or from the interrupt task) tries to use the unit while a division is still running, the execution of this new instruction is stalled until the previous division is finished.

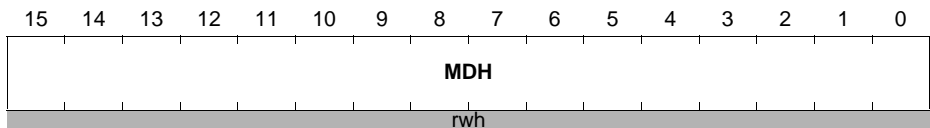
To avoid these stalls, the multiply and division unit should not be used during the first fourteen CPU cycles of the interrupt tasks. For example, this requires up to fourteen one-cycle instructions to be executed between the interrupt entry and the first instruction which uses the multiply and divide unit again (worst case).

Multiplications and divisions implicitly use the 32-bit multiply/divide register MD (represented by the concatenation of the two non-bit-addressable data registers MDH and MDL) and the associated control register MDC. This bit-addressable 16-bit register is implicitly used by the CPU when it performs a division or multiplication in the ALU.

After a multiplication, MD represents the 32-bit result. For long divisions, MD must be loaded with the 32-bit dividend before the division is started. After any division, register MDH represents the 16-bit remainder, register MDL represents the 16-bit quotient.

MDH

Multiply Divide High Word **SFR (FE0C_H/06_H)** **Reset Value: 0000_H**



Field	Bits	Type	Description
MDH	[15:0]	rwh	High Part of MD The high order sixteen bits of the 32-bit multiply and divide register MD.

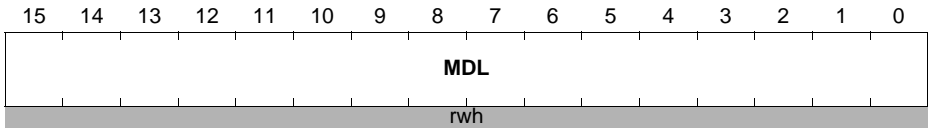
Central Processing Unit (CPU)

MDL

Multiply Divide Low Word

SFR (FE0E_H/07_H)

Reset Value: 0000_H



Field	Bits	Type	Description
MDL	[15:0]	rwh	Low Part of MD The low order sixteen bits of the 32-bit multiply and divide register MD.

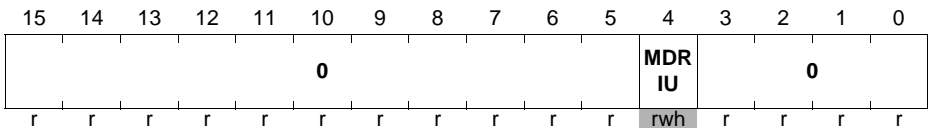
Whenever MDH or MDL is updated via software, the Multiply/Divide Register In Use flag (MDRIU) in the Multiply/Divide Control register (MDC) is set to '1'. The MDRIU flag is cleared, whenever register MDL is read via software.

MDC

Multiply Divide Control

SFR (FF0E_H/87_H)

Reset Value: 0000_H



Field	Bits	Type	Description
MDRIU	4	rwh	Multiply/Divide Register In Use 0 _B Cleared when MDL is read via software. 1 _B Set when MDL or MDH is written via software, or when a multiply or divide instruction is executed.
0	[15:5], [3:0]	r	Reserved Read as 0, should be written 0

Note: The MDRIU flag indicates the usage of register MD (MDL and MDH). In this case MD must be saved prior to a new multiplication or division operation.

5.9 DSP Data Processing (MAC Unit)

The CoXXX arithmetic instructions are executed by the MAC unit. It provides single-instruction-cycle, non-pipelined, 32-bit additions; 32-bit subtraction; right and left shifts; 16-bit by 16-bit multiplication; and multiplication with cumulative subtraction/addition. The MAC unit includes the following major components also shown in [Figure 5-16](#):

- 16-bit by 16-bit signed/unsigned multiplier with signed result¹⁾
- Concatenation Unit
- Scaler (one-bit left shifter) for fractional computing
- 40-bit Adder/Subtractor
- 40-bit Signed Accumulator
- Data Limiter
- Accumulator Shifter
- Repeat Counter

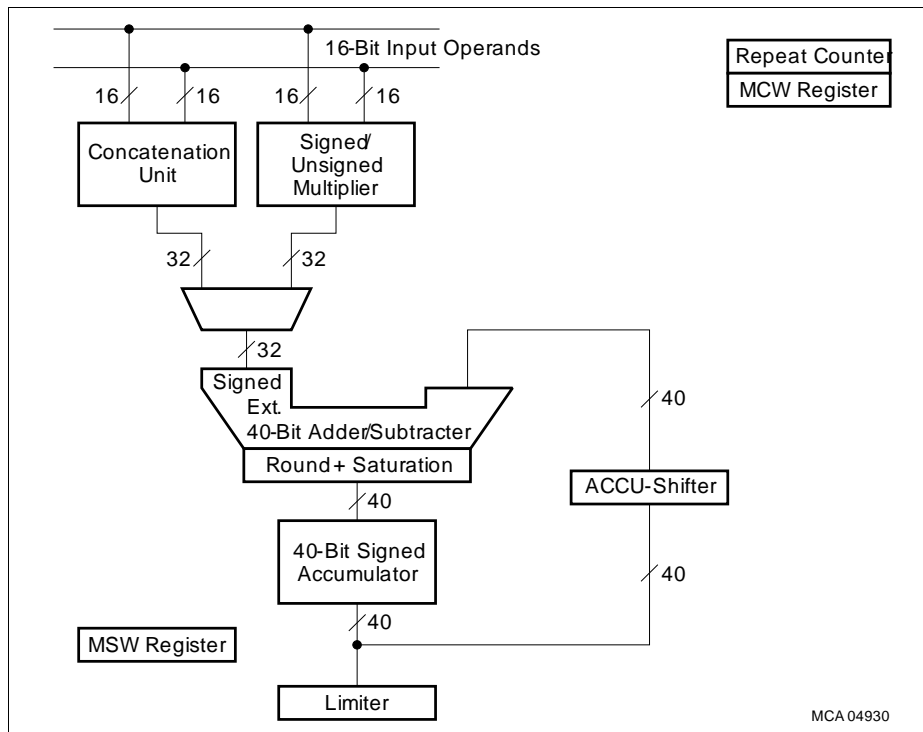


Figure 5-16 Functional MAC Unit Block Diagram

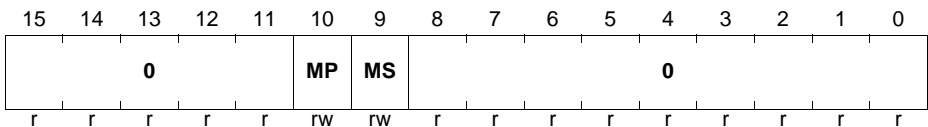
1) The same hardware-multiplier is used in the ALU.

5.9.1 MAC Unit Control

The working register of the MAC unit is a dedicated 40-bit accumulator register. A set of consistent flags is automatically updated in status register MSW after each MAC operation. These flags allow branching on specific conditions. Unlike the PSW flags, these flags are not preserved automatically by the CPU upon entry into an interrupt or trap routine. All dedicated MAC registers must be saved on the stack if the MAC unit is shared between different tasks and interrupts. General properties of the MAC unit are selected via the MAC control word MCW.

MCW

MAC Control Word **SFR (FFDC_H/EE_H)** **Reset Value: 0000_H**



Field	Bits	Type	Description
MP	10	r _w	One-Bit Scaler Control 0 _B Multiplier product shift disabled 1 _B Multiplier product shift enabled for signed multiplications
MS	9	r _w	Saturation Control 0 _B Saturation disabled 1 _B Saturation to 32-bit value enabled
0	[15:11] , [8:0]	r	Reserved Read as 0, should be written 0

5.9.2 Representation of Numbers and Rounding

The XC27x8X supports the 2's complement representation of binary numbers. In this format, the sign bit is the MSB of the binary word. This is set to zero for positive numbers and set to one for negative numbers. Unsigned numbers are supported only by multiply/multiply-accumulate instructions which specify whether each operand is signed or unsigned.

In 2's complement fractional format, the N-bit operand is represented using the 1.[N-1] format (1 signed bit, N-1 fractional bits). Such a format can represent numbers between -1 and +1 - 2^[-N-1]. This format is supported when bit MP of register MCW is set.

Central Processing Unit (CPU)

The XC27x8X implements 2's complement rounding. With this rounding type, one is added to the bit to the right of the rounding point (bit 15 of MAL), before truncation (MAL is cleared).

5.9.3 The 16-bit by 16-bit Signed/Unsigned Multiplier and Scaler

The multiplier executes 16-bit by 16-bit parallel signed/unsigned fractional and integer multiplication in one CPU-cycle. The multiplier allows the multiplication of unsigned and signed operands. The result is always presented in a signed fractional or integer format. The result of the multiplication feeds a one-bit scaler to allow compensation for the extra sign bit gained in multiplying two 16-bit 2's complement numbers.

5.9.4 Concatenation Unit

The concatenation unit enables the MAC unit to perform 32-bit arithmetic operations in one CPU cycle. The concatenation unit concatenates two 16-bit operands to a 32-bit operand before the 32-bit arithmetic operation is executed in the 40-bit adder/subtractor. The second required operand is always the current accumulator contents. The concatenation unit is also used to pre-load the accumulator with a 32-bit value.

5.9.5 One-bit Scaler

The one-bit scaler can shift the result of the concatenation unit or the output of the multiplier one bit to the left. The scaler is controlled by the executed instruction for the concatenation or by control bit MP in register MCW.

If bit MP is set the product is shifted one bit to the left to compensate for the extra sign bit gained in multiplying two 16-bit 2's-complement numbers. The enabled automatic shift is performed only if both input operands are signed.

5.9.6 The 40-bit Adder/Subtractor

The 40-bit Adder/Subtractor allows intermediate overflows in a series of multiply/accumulate operations. The Adder/Subtractor has two input ports. The 40-bit port is the feedback of the accumulator output through the ACCU-Shifter to the Adder/Subtractor. The 32-bit port is the input port for the operand coming from the one-bit Scaler. The 32-bit operands are signed and extended to 40 bits before the addition/subtraction is performed.

The output of the Adder/Subtractor goes to the accumulator. It is also possible to round the result and to saturate it on a 32-bit value automatically after every accumulation. The round operation is performed by adding $00'0000'8000_H$ to the result. Automatic saturation is enabled by setting the saturation control bit MS in register MCW.

When the accumulator is in the overflow saturation mode and an overflow occurs, the accumulator is loaded with either the most positive or the most negative value

Central Processing Unit (CPU)

representable in a 32-bit value, depending on the direction of the overflow as well as on the arithmetic used. The value of the accumulator upon saturation is either 00'7FFF'FFFF_H (positive) or FF'8000'0000_H (negative).

5.9.7 The Data Limiter

Saturation arithmetic is also provided to selectively limit overflow when reading the accumulator by means of a **CoSTORE <destination>**, **MAS** instruction. Limiting is performed on the MAC-Unit accumulator. If the contents of the accumulator can be represented in the destination operand size without overflow, then the data limiter is disabled and the operand is not modified. If the contents of the accumulator cannot be represented without overflow in the destination operand size, the limiter will substitute a "limited" data as explained in [Table 5-24](#):

Table 5-24 Limiter Output

ME-flag	MN-flag	Output of Limiter
0	x	unchanged
1	0	7FFF _H
1	1	8000 _H

Note: In this particular case, both the accumulator and the status register are not affected. MAS is readable by means of a CoSTORE instruction only.

5.9.8 The Accumulator Shifter

The accumulator shifter is a parallel shifter with a 40-bit input and a 40-bit output. The source accumulator shifting operations are:

- No shift (Unmodified)
- Up to 16-bit Arithmetic Left Shift
- Up to 16-bit Arithmetic Right Shift

Notice that bits ME, MSV, and MSL in register MSW are affected by left shifts; therefore, if the saturation mechanism is enabled (MS) the behavior is similar to the one of the Adder/Subtractor.

Note: Certain precautions are required in case of left shift with saturation enabled. Generally, if MAE contains significant bits, then the 32-bit value in the accumulator is to be saturated. However, it is possible that left shift may move some significant bits out of the accumulator. The 40-bit result will be misinterpreted and will be either not saturated or saturated incorrectly. There is a chance that the result of left shift may produce a result which can saturate an original positive number to the minimum negative value, or vice versa.

5.9.9 The 40-bit Signed Accumulator Register

The 40-bit accumulator consists of three concatenated registers MAE, MAH, and MAL. MAE is 8 bits wide, MAH and MAL are 16 bits wide. MAE is the Most Significant Byte of the 40-bit accumulator. This byte performs a guarding function. MAE is accessed as the lower byte of register MSW.

When MAH is written, the value in the accumulator is automatically adjusted to signed extended 40-bit format. That means MAL is cleared and MAE will be automatically loaded with zeros for a positive number (the most significant bit of MAH is 0), and with ones for a negative number (the most significant bit of MAH is 1), representing the extended 40-bit negative number in 2's complement notation. One may see that the extended 40-bit value is equal to the 32-bit value without extension. In other words, after this extension, MAE does not contain significant bits. Generally, this condition is present when the highest 9 bits of the 40-bit signed result are the same.

During the accumulator operations, an overflow may happen and the result may not fit into 32 bits and MAE will change. The extension flag "E" in register MSW is set when the signed result in the accumulator has exceeded the 32-bit boundary. This condition is present when the highest 9 bits of the 40-bit signed result are not the same, i.e. MAE contains significant bits.

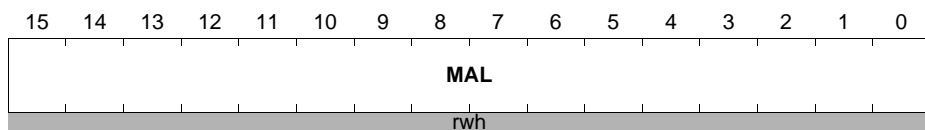
Most CoXXX operations specify the 40-bit accumulator register as a source and/or a destination operand.

MAL

Accumulator Low Word

SFR (FE5C_H/2E_H)

Reset Value: 0000_H



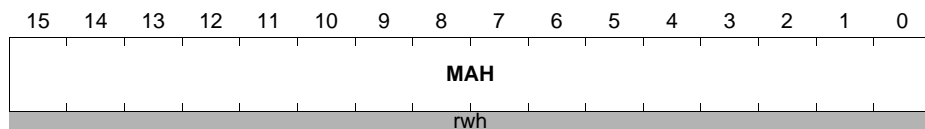
Field	Bits	Type	Description
MAL	[15:0]	rwh	Low Part of Accumulator The 40-bit accumulator is completed by the accumulator high word (MAH) and bitfield MAE

MAH

Accumulator High Word

SFR (FE5E_H/2F_H)

Reset Value: 0000_H



Field	Bits	Type	Description
MAH	[15:0]	rwh	High Part of Accumulator The 40-bit accumulator is completed by the accumulator low word (MAL) and bitfield MAE

5.9.10 The MAC Unit Status Word MSW

The upper byte of register MSW (bit-addressable) shows the current status of the MAC Unit. The lower byte of register MSW represents the 8-bit MAC accumulator extension, building the 40-bit accumulator together with registers MAH and MAL.

MSW

MAC Status Word

SFR (FFDE_H/EF_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	MV	MSL	ME	MSV	MC	MZ	MN								
r	rwh	rwh	rwh	rwh	rwh	rwh	rwh					rwh			

Field	Bits	Type	Description
0	15	r	Reserved Read as 0, should be written 0
MV	14	rwh	Overflow Flag 0 _B No Overflow produced 1 _B Overflow produced
MSL	13	rwh	Sticky Limit Flag 0 _B Result was not saturated 1 _B Result was saturated
ME	12	rwh	MAC Extension Flag 0 _B MAE does not contain significant bits 1 _B MAE contains significant bits
MSV	11	rwh	Sticky Overflow Flag 0 _B No Overflow occurred 1 _B Overflow occurred
MC	10	rwh	Carry Flag 0 _B No carry/borrow produced 1 _B Carry/borrow produced
MZ	9	rwh	Zero Flag 0 _B MAC result is not zero 1 _B MAC result is zero
MN	8	rwh	Negative Result 0 _B MAC result is positive 1 _B MAC result is negative

Field	Bits	Type	Description
MAE	[7:0]	rwh	MAC Accumulator Extension The most significant bits of the 40-bit accumulator, completing registers MAH and MAL

MAC Unit Status (MV, MN, MZ, MC, MSV, ME, MSL)

These condition flags indicate the MAC status resulting from the most recently performed MAC operation. These flags are controlled by the majority of MAC instructions according to specific rules. Those rules depend on the instruction managing the MAC or data movement operation.

After execution of an instruction which explicitly updates register MSW, the condition flags may no longer represent an actual MAC status. An explicit write operation to register MSW supersedes the condition flag values implicitly generated by the MAC unit. An explicit read access returns the value of register MSW after execution of the immediately preceding instruction. Register MSW can be accessed via any instruction capable of accessing an SFR.

Note: After reset, all MAC status bits are cleared.

MN-Flag: For the majority of the MAC operations, the MN-flag is set to 1 if the most significant bit of the result contains a 1; otherwise, it is cleared. In the case of integer operations, the MN-flag can be interpreted as the sign bit of the result (negative: MN = 1, positive: MN = 0). Negative numbers are always represented as the 2's complement of the corresponding positive number. The range of signed numbers extends from 80'0000'0000_H to 7F'FFFF'FFFF_H.

MZ-Flag: The MZ-flag is normally set to 1 if the result of a MAC operation equals zero; otherwise, it is cleared.

MC-Flag: After a MAC addition, the MC-flag indicates that a "Carry" from the most significant bit of the accumulator extension MAE has been generated. After a MAC subtraction or a MAC comparison, the MC-flag indicates a "Borrow" representing the logical negation of a "Carry" for the addition. This means that the MC-flag is set to 1 if **no** "Carry" from the most significant bit of the accumulator has been generated during a subtraction. Subtraction is performed by the MAC Unit as a 2's complement addition and the MC-flag is cleared when this complement addition caused a "Carry". For left-shift MAC operations, the MC-flag represents the value of the bit shifted out last. Right-shift MAC operations always clear the MC-flag. The arithmetic right-shift MAC operation can set the MC-flag if the enabled round operation generates a "Carry" from the most significant bit of the accumulator extension MAE.

MSV-Flag: The addition, subtraction, 2's complement, and round operations always set the MSV-flag to 1 if the MAC result exceeds the maximum range of 40-bit signed numbers. If the MSV-flag indicates an arithmetic overflow, the MAC result of an operation is not valid.

Central Processing Unit (CPU)

The MSV-flag is a 'Sticky Bit'. Once set, other MAC operations cannot affect the status of the MSV-flag. Only a direct write operation can clear the MSV-flag.

ME-Flag: The ME-flag is set if the accumulator extension MAE contains significant bits, that means if the nine highest accumulator bits are not all equal.

MSL-Flag: The MSL-flag is set if an automatic saturation of the accumulator has happened. The automatic saturation is enabled if bit MS in register MCW is set. The MSL-Flag can be also set by instructions which limit the contents of the accumulator. If the accumulator has been limited, the MSL-Flag is set.

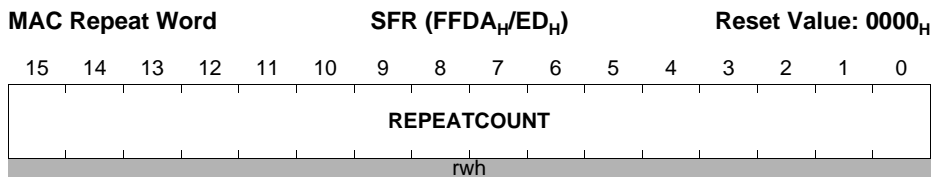
The MSL-Flag is a 'Sticky Bit'. Once set, it cannot be affected by the other MAC operations. Only a direct write operation can clear the MSL-flag.

MV-Flag: The addition, subtraction, and accumulation operations set the MV-flag to 1 if the result exceeds the maximum range of signed numbers (80'0000'0000_H to 7F'FFFF'FFFF_H); otherwise, the MV-flag is cleared. Note that if the MV-flag indicates an arithmetic overflow, the result of the integer addition, integer subtraction, or accumulation is not valid.

5.9.11 The Repeat Counter MRW

The Repeat Counter MRW controls the number of repetitions a loop must be executed. The register must be pre-loaded before it can be used with -USRx CoXXX operations. MAC operations are able to decrement this counter. When a -USRx CoXXX instruction is executed, MRW is checked for zero **before** being decremented. If MRW equals zero, bit USRx is set and MRW is not further decremented. Register **MRW** can be accessed via any instruction capable of accessing a SFR.

MRW



Field	Bits	Type	Description
REPEATCOUNT	[15:0]	rwh	MAC repeat counter

All CoXXX instructions have a 3-bit wide repeat control field 'rrr' (bit positions [31:29]) in the operand field to control the MRW repeat counter. [Table 5-25](#) lists the possible encodings.

Table 5-25 Encoding of MAC Repeat Word Control

Code in 'rrr'	Effect on Repeat Counter
000 _B	regular CoXXX instruction
001 _B	RESERVED
010 _B	'-USR0 CoXXX' instruction, decrements repeat counter and sets bit USR0 if MRW is zero
011 _B	'-USR1 CoXXX' instruction, decrements repeat counter and sets bit USR1 if MRW is zero
1XX _B	RESERVED

Note: Bit USR0 has been a general purpose flag also in previous architectures. To prevent collisions due to using this flag by programmer or compiler, use '-USR0 CoXXX' instructions very carefully.

The following example shows a loop which is executed 20 times. Every time the CoMACM instruction is executed, the MRW counter is decremented.

```

MOV      MRW, #19           ;Pre-load loop counter
loop01:
-USR1    CoMACM [IDX0+], [R0+] ;Calculate and decrement MSW
ADD      R2, #0002H
JMPA     cc_nusr1, loop01 ;Repeat loop until USR1 is set

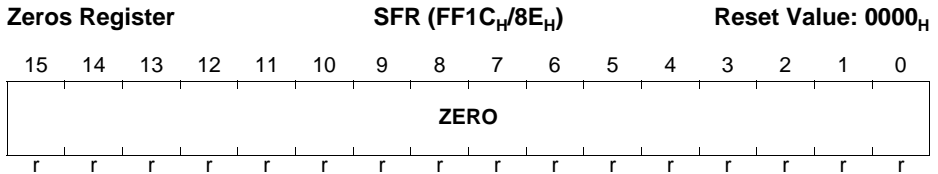
```

Note: Because correctly predicted JMPA is executed in 0-cycle, it offers the functionality of a repeat instruction.

5.10 Constant Registers

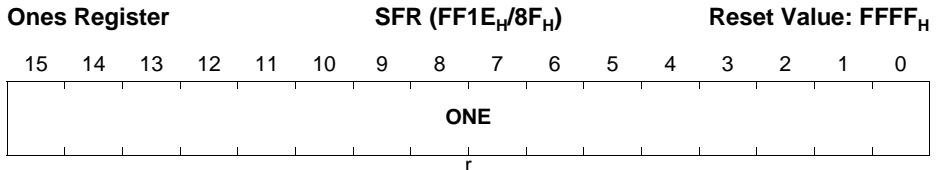
All bits of these bit-addressable registers are fixed to 0 or 1 by hardware. These registers can be read only. Register ZEROS/ONES can be used as a register-addressable constant of all zeros or all ones, for example for bit manipulation or mask generation. The constant registers can be accessed via any instruction capable of addressing an SFR.

ZEROS



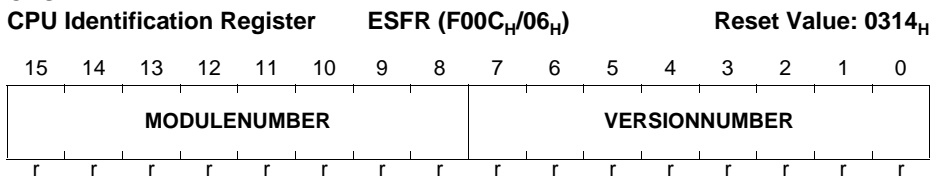
Field	Bits	Type	Description
ZERO	[15:0]	r	Constant Zero Bits

ONES



Field	Bits	Type	Description
ONE	[15:0]	r	Constant One Bits

CPUID



Field	Bits	Type	Description
MODULENUMBER	[15:8]	r	C166 Family CPU Module Number (C166S-V2)

Central Processing Unit (CPU)

Field	Bits	Type	Description
VERSIONNUMBER	[7:0]	r	C166S-V2 CPU Version Number

6 Instruction Cache

The XC27x8X contains 16 Kbytes of Instruction Cache (ICACHE). The ICACHE is a two-way set-associative cache and is organized as 512 cache lines, with 128 bits per line. Each ICACHE line has a single associated valid bit. A dedicated address space is reserved in which the program execution can be accelerated with enabled ICACHE.

6.1 Instruction Cache Operation

CPU program fetch accesses which target a cacheable memory segment also target the ICACHE. If the requested address and its associated instruction are found in the cache (Cache Hit), the instruction is passed to the CPU Prefetch Unit. If the address is not found in the cache (Cache Miss), the cache controller issues a cache refill sequence and wait states are incurred while the cache line is refilled from the Flash.

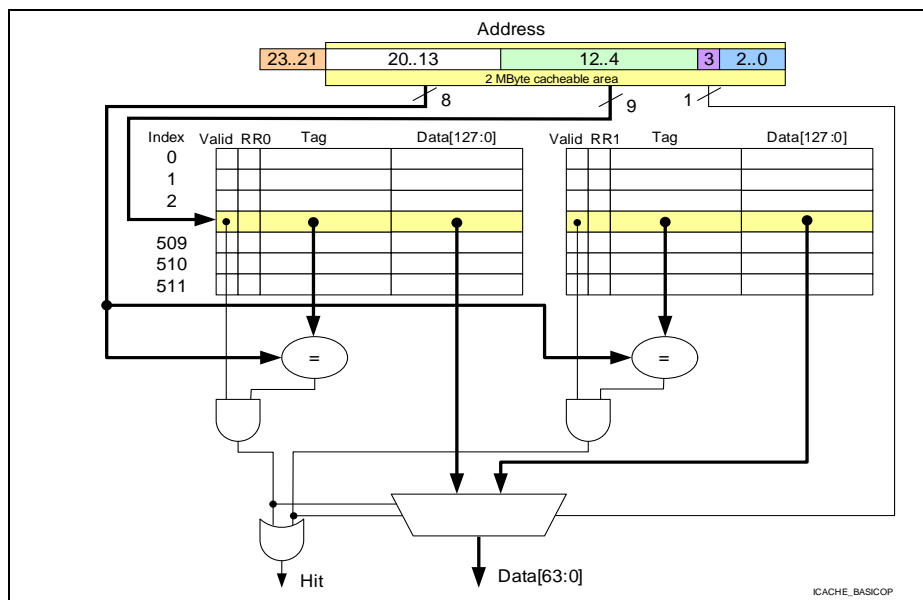


Figure 6-1 Instruction Cache Operation

To avoid starting a Flash access (that can not be aborted!) for an instruction that is already stored in the cache, accesses in the cacheable address space are delayed by one cycle for the hit/miss detection. This also avoids unnecessary collisions with data accesses to the same Flash module.

6.2 Instruction Cache Address Space

The ICACHE distinguishes between cacheable and non-cacheable address spaces. Instruction fetch accesses to the non-cacheable space are generally ignored by the cache controller. Instruction fetches from the cacheable address space are checked against the current cache content.

For instruction fetches, the cacheable address space is a mirror of the physical memory in the non-cacheable space. Cache misses are refilled from the equivalent addresses in the non-cacheable space, see [Table 6-1](#).

Data sections in the Flash must be allocated in the non-cacheable address space. Data accesses to the cacheable address space as listed in [Table 6-1](#) are not handled by the instruction cache. There is also no remapping of the alternative address spaces for data accesses.

Attention: *Data sections must not be allocated in the cacheable address space as they can't be accessed via cacheable addresses.*

Table 6-1 Instruction Cache Address Map

Start Address	End Address	Description
0x80'0000	0x9F'FFFF	Cacheable Flash address space. (misses remapped to 0xC0'0000-0xDF'FFFF)
0xC0'0000	0xDF'FFFF	Non-cacheable Flash address space.

Note: [Table 6-1](#) lists the full address ranges. The actual memory configuration is documented in the Memory Organisation chapter and in the Data Sheet of the respective device.

Instruction Cache refills are performed using a single 128-bit access. A refill always affects one complete cache line.

Prefetches by the CPU may be aborted, e.g. due to a branch misprediction. Pending refills of such aborted accesses will not be stored in the ICACHE.

To which set the refill data is written is decided based on a Round-Robin (RR) replacement algorithm. All cache lines of each set have a RR-flag. Their operation is defined by [Table 6-2](#). Writing a cache line also toggles the respective RR-flag, thus selecting the next set for the next refill.

Table 6-2 Round Robin Replacement

RR Set 0	RR Set 1	Updated Set	New RR Set 0	New RR Set 1
0	0	0	1	0
0	1	1	0	0
1	0	1	1	1
1	1	0	0	1

The CPU fetch interface generates 64-bit aligned accesses, which result in 64 bits of instruction being returned to the CPU. If the fetch request is made within a ICACHE line and a cache hit occurs, then the 64-bit instruction packet is returned to the CPU.

6.3 Instruction Cache Enable

The Instruction Cache can be enabled under control of **ICACHE_CTRL.ICEN**. The default value of **ICACHE_CTRL.ICEN** is such that the ICACHE is disabled after reset. For maximum performance of the XC27x8X the ICACHE should be enabled upon initialization of the system.

Instruction fetch requests to cacheable addresses while the ICACHE is disabled behave identically to instruction fetch requests to non-cacheable addresses. The fetch request results in a forced cache miss, but without additional wait cycle. The access is executed with the remapped address. The fetched instructions are passed to the CPU, without updating the cache contents. Cache lines remain unchanged while the ICACHE is disabled.

6.4 Instruction Cache Invalidation

The cache controller does not have automatic cache coherency support. Changes to the contents of memory areas that may have already been cached in the ICACHE are not detected. Software must provide the cache coherency in such a case. The ICACHE supports this via the cache invalidation function. The ICACHE content is globally invalidated by writing a '1' to **ICACHE_CTRL.CLRV**.

The ICACHE invalidation is performed over multiple cycles, one cycle per cache line, both sets in parallel. The status of the invalidation may be determined by reading **ICACHE_CTRL.CLRV**. While the invalidation is running, the cache is not available and behaves as if disabled, disregarding **ICACHE_CTRL.ICEN** (see [Chapter 6.3](#)).

With an application reset the ICACHE invalidation is started automatically. Along with the invalidation, the ICACHE memories are also initialized. The valid flags and the Round-Robin bits are cleared. The TAG bit fields point to a reserved address space. They are initialized with "FF_H", pointing to the upper part of segment "9F_H". The data bit fields are initialized with a trap code (Trap 15_D, "9B1E_H").

6.5 Cache Memory Data Integrity

ECC logic is used to ensure the integrity of the ICACHE memory content. Per default, single bit error correction (SEC) and double bit error detection (DED) is selected in its memories. It is possible to change this setup for special applications, see [Chapter 6.5.1](#).

With enabled ICACHE, data is always stored with its full ECC information.

Because of that and along with the initialization phase after a system reset (see [Chapter 6.4](#)), in normal cache operation the ICACHE memory content is always supposed to be ECC correct.

Note: In order to use error detection and correction for the ICACHE, it must be enabled with the ECCCON register in the SCU.

Once enabled and with the default setup single bit errors are 'silently' corrected.

A cache hit with a double bit error in the respective cache line will return a Trap Code (Trap 15_D, "9B1E_H") instead of the erroneous data. This allows for a synchronous trap that only occurs if the erroneous instruction would have been executed. Instead of the faulty instruction the trap code is passed to the CPU and if the trap code reaches the execute stage of the CPU pipeline it starts the execution of the trap handler.

In cases where an ECC error does not affect the program execution a detected error is just flagged via the respective sticky flag (see below).

ECC errors of cache misses do not interrupt the application. Instead, the instruction is fetched and executed from the Flash, also refilling the cache with the fetched data.

ECC errors of cache hits that are canceled before execution do not trigger an error either.

All ECC errors are flagged via the sticky bits [ICACHE_EDCON.SED](#) and [ICACHE_EDCON.DED](#), independent of access type and [ICACHE_EDCON.SELED](#) configuration. If set, these flags can only be cleared by software via [ICACHE_CTRL.CLREDF](#).

Table 6-3 ECC Error Handling (Default)

Error	ICACHE_EDCON			Instruction Fetch Data
	SELED	SED	DED	
No error	don't care	0	0	Raw data
Single bit error	SECD	1	0	Corrected data
Double bit error	SECD	0	1	Trap code 9B1E _H

6.5.1 Custom ICACHE ECC Setup

For special use cases it is possible to change the error detection setup. The selection of the error detection is handled via [ICACHE_EDCON.SELED](#). Depending on the type of access, the selection defines which data is returned and how an error is flagged. The detailed behavior is summarized in [Table 6-4](#).

Instruction Cache

In data access mode (see [Chapter 6.6](#)), depending on **ICACHE_EDCON.SELED** the respective error information for data accesses is passed on to the **ECCSTAT** register in the SCU and can be used to trigger a trap via the SCU (see chapter “ECC Error Handling” of the SCU).

The option **ICACHE_EDCON.SELED=SEC** allows for a single bit error correction without error indication of single or double bit errors.

Table 6-4 Custom ECC Error Handling

Error	ICACHE_EDCON			Read data		SCU_ECCSTAT (for data accesses)
	SELED	SED	DED	Instruction Fetch	Data access	
No error	don't care	0	0	Raw data	Raw data	No error
Single bit error	SEC	1	0	Corrected	Corrected	No error
	SECSSED	1	0	Corrected	Corrected	Error
	SECDDED	1	0	Corrected	Corrected	No error
	SED and DED	1	0	Corrected	Corrected	Error
Double bit error	SEC	0	1	Raw data	Raw data	No error
	SECSSED	0	1	Raw data	Raw data	No error
	SECDDED	0	1	Trap code 9B1E _H	Raw data	Error
	SED and DED	0	1	Trap code 9B1E _H	Raw data	Error

6.6 Cache Memory Data Access

For test purposes a data access interface is defined for the cache memory. A set of registers allows the access to a complete cache line. Data read and write accesses to the cache memories are only possible while the instruction cache is disabled.

Table 6-5 shows the mapping of the registers to the actual cache line, addressing is handled by the read and write address pointer registers, **ICACHE_RADD** and **ICACHE_WADD**.

While the data access is enabled, **ICACHE_DACON.WRECC** allows to either write custom values, stored in **ICACHE_ECCLH** and **ICACHE_TAG.ECCT**, to the ECC bits of the ICACHE memories or to ignore these registers and write the actual hardware generated ECC values.

Note: Data reads are also subject to the ECC error detection and correction (see [Chapter 6.5.1](#)). The Valid flag does not mask ECC errors for data accesses.

When enabling the data access to the cache memories the cache controller might still be busy with a refill access. To avoid collisions all data accesses to the memory are

Instruction Cache

blocked until the cache controller has finished its pending accesses. The flag **ICACHE_DACON.DAGTD** indicates that the cache controller has finished its last access and that data accesses to the cache memories are possible. Memory data access triggers, e.g. the 'pre-read', are ignored while this bit is not set. The access to the ICACHE SFRs is not affected. Read accesses will return the current content of the addressed SFR, writes will update the SFR content. With an access to the **ICACHE_TAG** register no accesses to the cache memories are triggered and no pointers will be auto-incremented while **ICACHE_DACON.DAGTD** is not set.

ICACHE_DACON.DAGTD is cleared while a cache memory invalidation is running.

Note: After data writes to the ICACHE memories the cache should be invalidated before enabling the ICACHE as the data coherency between the (supposed to be cached) program in the Flash and the actual cache content is no longer given.

Table 6-5 Cache Line Mapping

Register/Bit field	Cache Line Bit field
ICACHE_DATA0	Data bit field [15:0]
ICACHE_DATA1	Data bit field [31:16]
ICACHE_DATA2	Data bit field [47:32]
ICACHE_DATA3	Data bit field [63:48]
ICACHE_DATA4	Data bit field [79:64]
ICACHE_DATA5	Data bit field [95:80]
ICACHE_DATA6	Data bit field [111:96]
ICACHE_DATA7	Data bit field [127:112]
ICACHE_ECCLH .ECCL	ECC value for data bit field [63:0]
ICACHE_ECCLH .ECCH	ECC value for data bit field [127:64]
ICACHE_TAG .TAG	TAG RAM [7:0]
ICACHE_TAG .RR	Round Robin bit
ICACHE_TAG .VALID	Valid flag
ICACHE_TAG .ECCT	ECC value for the combined TAG RAM bit field, Round Robin bit and Valid flag

6.7 Hit/Miss Statistics

For trace purposes in software development counters are implemented to count cache hits and cache misses. These counters trace all fetch accesses from the CPU to the cacheable address space.

All instruction fetch/prefetch accesses are counted once the fetch data has been delivered to the CPU. Not counted are accesses that have been subsequently aborted

Instruction Cache

before completion. Aborts can be triggered by different effects, e.g. due to a branch misprediction.

The length of the counters is asymmetric, a 24 bit Hit Counter and a 21 bit Miss Counter, as for a reasonably long program sample many more hits than misses are expected. If one of the counters reaches its maximum value, both counters are stopped (and **ICACHE_HMCON**.HMEN is automatically cleared) to be able to deduce the last cache hit rate at the time the maximum was reached.

The counters should only be evaluated when stopped, either by software or after one has counted to the maximum. Afterwards they can be reset by **ICACHE_HMCON**.HMCLR and restarted again by **ICACHE_HMCON**.HMEN.

Note: Re-enabling the counters restarts counting with both counters. Counting continues with the current values. If not cleared, this results in a wrap-around if a counter had reached its maximum before.

Note: The cache hit rate in percent is calculated as $100 \times (\text{Hit} / (\text{Hit} + \text{Miss}))$.

Results may vary and heavily depend on the structure of the application and the measured sample. Aspects like the interrupt load, task scheduling, memory allocation and others can severely influence measurement results.

With the bit **ICACHE_HMCON**.BRKGT it is possible to gate the counters by an internal connection to the BRKOUT function of the OCDS. By this it is possible to profile specific software routines, e.g. by their IPs or TASKIDs. This allows hit/miss measurements for the respective routines without the instrumentation (and recompilation) of the source code just by the configuration via OCDS/debugger and without the need for an external pin for the BRKOUT signal.

Note: There is a delay between fetch accesses and instruction execution indicated by the BRKOUT signal due to the pipelined architecture of the CPU. This causes a skew for the gated profiling, as the fetch(es) of the first instructions will be missed and at the end some fetches might be counted that are not part of the monitored routine.

This delay introduces an error in the Hit/Miss Statistic that becomes more and more relevant the smaller the code section is that is monitored with the BRKOUT gating function.

There are several CPU pipeline effects that cause some imprecisions in the counter results, most notably compulsory misses at the start of the measurement, the difference between instruction size and cache/fetch interface width, speculative fetches due to branch prediction, and others more.

Because of such effects and depending on the structure of the application, results might be skewed to one or the other direction, e.g. for a short sample more cache misses might be traced due to the compulsory misses.

6.8 ICACHE Registers

6.8.1 Control Register

The ICACHE control register provides bits to enable the Instruction Cache, flush the Cache by invalidating its current content and to clear the error detection flags in [ICACHE_EDCON](#).

Normal cache operation with [ICACHE_CTRL](#).ICEN set and data access to the ICACHE memories via [ICACHE_DACON](#).DAEN are mutually exclusive operating modes. To ensure that both are not enabled at the same time, enabling the cache via [ICACHE_CTRL](#).ICEN automatically clears [ICACHE_DACON](#).DAEN and vice versa.

ICACHE_CTRL

ICACHE Control Register

XSFR(E400_H)

Reset Value: 0004_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0												CLR EDF	CLR V	BP ICEN	ICEN
r												w	rwh	w	rwh

Field	Bits	Type	Description
ICEN	0	rw	ICACHE Enable With this bit it is possible to disable/enable the Instruction Cache. 0 _B The ICACHE is disabled. 1 _B The ICACHE is enabled.
BPICEN	1	w	Bit Protection for ICACHE Enable This bit enables the write access to ICEN. It always reads 0. 0 _B ICEN is not changed. 1 _B ICEN is updated with the written value.

Instruction Cache

Field	Bits	Type	Description
CLRV	2	rwh	Clear Valid Flag With this bit it is possible to clear the Valid Flags of all cache lines. It is cleared by hardware once the invalidation is finished. Write: 0 _B No change. 1 _B Invalidate the entire instruction cache. Read: 0 _B Instruction cache available. 1 _B Invalidation running. Instruction cache not available.
CLREDF	3	w	Clear Error Detection Flags A write of 1 to this bit clears the Single- and Double-Bit Error Detection flags. It always reads 0. 0 _B The ICACHE_EDCON .SED/DED flags are not changed. 1 _B The ICACHE_EDCON .SED/DED flags are cleared.
0	[15:4]	r	Reserved returns 0 if read; should be written with 0;

6.8.2 Error Detection Control Register

The ICACHE Error Detection control register allows the selection of the ECC error detection and contains status flags that indicate the occurrence of an error independent of the configuration. For details see [Table 6-4](#).

Write accesses to this register are restricted by the EINIT protection.

ICACHE_EDCON

ICACHE Error Detection Control RegisterXSFR(E406_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DED	SED	0										BP SEL ED	SELED		
rh	rh	r										w	rw		

Field	Bits	Type	Description
SELED	[1:0]	rw	Select Error Detection This bit field selects which error detection information is passed on to the ECCSTAT. 00 _B Double Bit Error Detection (SECDDED) selected. 01 _B Single Bit Error Detection (SECSDED) selected. 10 _B SED and DED (logical OR of SED and DED) selected. 11 _B Single Bit Error Correction (SEC) only.
BPSELED	2	w	Bit Protection for Select Error Detection This bit enables the write access to SELED. It always reads 0. 0 _B SELED is not changed. 1 _B SELED is updated with the written value.
SED	14	rh	Single-Bit Error Detection Flag This flag indicates that a Single-Bit Error occurred since it was last cleared/reset. Can be cleared by ICACHE_CTRL.CLREDF . 0 _B No Single-Bit Error occurred. 1 _B A Single-Bit Error occurred.
DED	15	rh	Double-Bit Error Detection Flag This flag indicates that a Double-Bit Error occurred since it was last cleared/reset. Can be cleared by ICACHE_CTRL.CLREDF . 0 _B No Double-Bit Error occurred. 1 _B A Double-Bit Error occurred.
0	[13:3]	r	Reserved returns 0 if read; should be written with 0;

6.8.3 Data Access Control Register

The ICACHE data access control register allows data accesses to the ICACHE memories.

Normal cache operation with [ICACHE_CTRL.ICEN](#) set and data access to the ICACHE memories via [ICACHE_DACON.DAEN](#) are mutually exclusive operating modes. To ensure that both are not enabled at the same time, enabling data access via [ICACHE_DACON.DAEN](#) automatically clears [ICACHE_CTRL.ICEN](#) and vice versa.

Write accesses to this register are restricted by the EINIT protection.

ICACHE_DACON

ICACHE Data Access Control RegisterXSFR(E402_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0						BP WR ECC	WR ECC	DA GTD	0						BP DA EN	DA EN
r						w	rw	rh	r						w	rwh

Field	Bits	Type	Description
DAEN	0	rw	Data Access Enable With this bit it is possible to enable data accesses to the Instruction Cache for test and debug purposes. 0 _B The data access is disabled. 1 _B The data access is enabled.
BPDAEN	1	w	Bit Protection for Data Access Enable This bit enables the write access to DAEN. It always reads 0. 0 _B DAEN is not changed. 1 _B DAEN is updated with the written value.
DAGTD	7	rh	Data Access Granted Flag This flag indicates whether data accesses to the ICACHE memories are possible. 0 _B Data accesses are blocked. 1 _B Data accesses are possible.
WRECC	8	rw	Write ECC Data Enable This bit controls whether the hardware generated ECC value or the content of the ECC register bit fields are written to the ECC bits of the memory. <i>Note: This bit is only considered while data access is enabled.</i> 0 _B The hardware generated ECC values are written to the ECC bits. 1 _B The register values are written to the ECC bits.

Field	Bits	Type	Description
BPWRECC	9	w	Bit Protection for Write ECC Data Enable This bit enables the write access to WRECC. It always reads 0. 0 _B WRECC is not changed. 1 _B WRECC is updated with the written value.
0	[6:2], [15:10]	r	Reserved returns 0 if read; should be written with 0;

6.8.4 Read Address Register

While in data access mode, the ICACHE data read address register selects the cache line and set that is currently read and stored in the **ICACHE_DATAx (x=0-7)**, **ICACHE_ECCLH** and **ICACHE_TAG** registers.

An update of the ICACHE_RADD register, by a software write or an auto-increment of the cache line pointer, 'pre-reads' from the addressed ICACHE memory and the software can then read the data from the **ICACHE_DATAx (x=0-7)**, **ICACHE_ECCLH** and **ICACHE_TAG** registers.

With the RMOD bit it is also possible to enable an auto-increment of the cache line pointer with each read of the **ICACHE_TAG** register. The RWA indicates whether the auto-increment led to a wrap-around of the cache line pointer.

ICACHE_RADD

ICACHE Read Address Register XSFR(E410_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R MOD		RWA		0			R SET		RCL						
rw		rwh		r			rw		rwh						

Field	Bits	Type	Description
RCL	[8:0]	rwh	Read Cache Line Selection Defines the cache line that is read by a write or autoincrement of ICACHE_RADD.RCL .
RSET	9	rw	Read Set Selection Selects to which cache set the next read access is redirected to. 0 _B Cache set 0 is selected. 1 _B Cache set 1 is selected.

Field	Bits	Type	Description
RWA	14	rwh	Read Wrap Around This bit indicates that a wrap around of the RCL bit field has occurred. This bit is sticky, can only be set by hardware and has to be cleared by software. 0 _B No wrap around of RCL has occurred. 1 _B A wrap around of RCL has been detected.
RMOD	15	rw	Auto-Increment Mode for read accesses This bit controls the auto-increment mode of the RCL bit field. 0 _B The auto-increment is disabled. 1 _B The auto-increment is enabled.
0	[13:10]	r	Reserved returns 0 if read; should be written with 0;

6.8.5 Write Address Register

While in data access mode, the ICACHE data write address register selects the cache line and set that is written with the data stored in the [ICACHE_DATAx \(x=0-7\)](#), [ICACHE_ECCLH](#) and [ICACHE_TAG](#) registers. The actual write is triggered when [ICACHE_TAG.WR](#) is written with 1_B.

With the WMOD bit it is also possible to enable an auto-increment of the cache line pointer with each triggered write. The WWA indicates whether the auto-increment led to a wrap-around of the cache line pointer.

ICACHE_WADD

ICACHE Write Address Register XSFR(E412_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W MOD	WW A	0				W SET	WCL								
rw	rwh	r				rw	rwh								

Field	Bits	Type	Description
WCL	[8:0]	rwh	Write Cache Line Pointer Defines the cache line that is written by writing 1 _B to ICACHE_TAG.WR .

Instruction Cache

Field	Bits	Type	Description
WSET	9	rw	Write Set Selection Selects to which cache set the next write access is redirected to. 0 _B Cache set 0 is selected. 1 _B Cache set 1 is selected.
WWA	14	rwh	Write Wrap Around This bit indicates that a wrap around of the WCL bit field has occurred. This bit is sticky, can only be set by hardware and has to be cleared by software. 0 _B No wrap around of WCL has occurred. 1 _B A wrap around of WCL has been detected.
WMOD	15	rw	Auto-Increment Mode for Write accesses This bit controls the auto-increment mode of the WCL bit field. 0 _B The auto-increment is disabled. 1 _B The auto-increment is enabled.
0	[13:10]	r	Reserved returns 0 if read; should be written with 0;

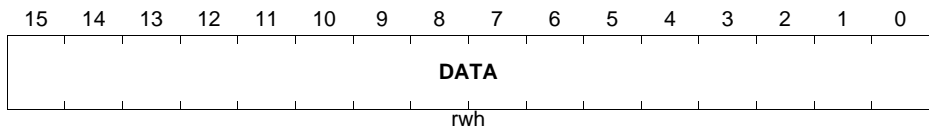
6.8.6 Data Registers

While in data access mode, the ICACHE data registers contain the read or write data of the cache line. See [Table 6-5](#) for the exact mapping.

With enabled ECC a read returns the ECC-corrected values, otherwise the raw data.

ICACHE_DATAx (x=0-7)

ICACHE Data Field Register **XSFR(E420_H+2*x)** **Reset Value: 0000_H**



Field	Bits	Type	Description
DATA	[15:0]	rwh	ICACHE Data Data value read/written.

6.8.7 ECC Data Register

While in data access mode, the ICACHE ECC data register contains the ECC values for the cache line according to [Table 6-5](#).

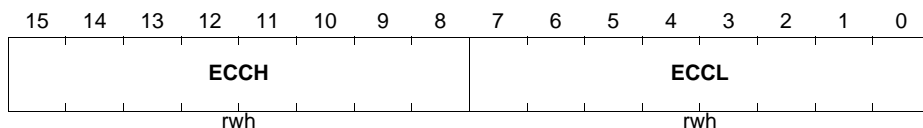
With enabled ECC a read returns the ECC-corrected values, otherwise the raw ECC bits. The register content is ignored for writes with enabled ECC.

ICACHE_ECCLH

ICACHE ECC Data Register

XSFR(E430_H)

Reset Value: 0000_H



Field	Bits	Type	Description
ECCL	[7:0]	rwh	ICACHE ECCL Bit field ECC bit field of the lower half of the cache line. With enabled ECC this bit field is ignored for write accesses.
ECCH	[15:8]	rwh	ICACHE ECCH Bit field ECC bit field of the upper half of the cache line. With enabled ECC this bit field is ignored for write accesses.

6.8.8 TAG Register

While in data access mode, the ICACHE TAG register accesses the TAG RAM of the selected cache line, including the Round Robin flag and the ECC value of them. Additionally it provides a write bit to trigger the actual write of the data stored in the [ICACHE_DATAx](#) (x=0-7), [ICACHE_ECCLH](#) and [ICACHE_TAG](#) registers to the selected cache memory.

With active write address auto-increment, upon a write access with [ICACHE_TAG.WR](#)=1, the bit field [ICACHE_WADD.WCL](#) is incremented to address the next cache line. A write to the last cache line triggers a wrap-around in [ICACHE_WADD.WCL](#) and is indicated in [ICACHE_WADD.WWA](#).

With active read address auto-increment, upon a read access to [ICACHE_TAG](#) the bit field [ICACHE_RADD.RCL](#) is incremented. A read of the [ICACHE_TAG](#) of the last cache line triggers a wrap-around in [ICACHE_RADD.RCL](#) and is indicated in [ICACHE_RADD.RWA](#).

Instruction Cache

With enabled ECC a read returns the ECC-corrected values, otherwise the raw data. The ECCT bit field is ignored for writes with enabled ECC.

ICACHE_TAG

ICACHE TAG Register

XSFR(E432_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WR	VA LID	ECCT					RR	TAG							
w	rwh	rwh					rwh	rwh							

Field	Bits	Type	Description
TAG	[7:0]	rwh	ICACHE TAG Bit field
RR	8	rwh	ICACHE Round Robin Flag
ECCT	[13:9]	rwh	ICACHE TAG RAM ECC Bit field ECC value of the combined TAG bit field, the Round Robin flag and the Valid flag. With enabled ECC this bit field is ignored for write accesses.
VALID	14	rwh	ICACHE Valid Bit Valid bit of the selected cache line. 0 _B Invalid cache line. 1 _B Valid cache line.
WR	15	w	Write Trigger Triggers the write of the Data, TAG and ECC registers to the ICACHE memories. It is read 0. 0 _B No change. 1 _B Write to the ICACHE is triggered.

6.8.9 Hit-Miss Control Register

The ICACHE hit and miss control register provides basic controls to enable, gate and clear the ICACHE hit and miss counters. Additionally it contains the upper bits of the counters.

ICACHE_HMCON

ICACHE Hit-Miss Control Register XSFR(E404_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HITH								MISSH				BRK GT	HM CLR	HM EN	
rh								rh				rw	w	rwh	

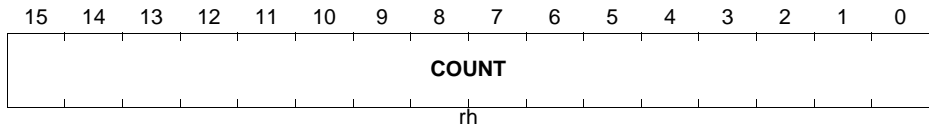
Field	Bits	Type	Description
HMEN	0	rwh	Hit-Miss Counter Enable With this bit it is possible to enable the Hit-Miss counter. If one of the counters reaches its maximum value this bit is cleared automatically and thus stops both counters. 0 _B The counters are disabled. 1 _B The counters are enabled.
HMCLR	1	w	Hit/Miss Counter Clear With this bit it is possible to clear the Hit-Miss counter. It always reads 0. 0 _B Hit/Miss Counters not changed. 1 _B Hit/Miss Counters are cleared.
BRKGT	1	rw	BRKOUT Gating Enable With this bit it is possible to gate the counters by the BRKOUT signal of the OCDS. 0 _B Counting is not gated. 1 _B Counting is gated by OCDS BRKOUT.
MISSH	[7:2]	rh	Miss Counter [20:16] Upper bits of the miss counter.
HITH	[15:8]	rh	Hit Counter [23:16] Upper bits of the hit counter.

6.8.10 Hit Counter Register

The ICACHE hit counter register stores the lower 16 bit of the Hit Counter, with the upper part stored in [ICACHE_HMCON.HITH](#). If either the Hit or Miss counter reaches its maximum value both counters get stopped and the bit [ICACHE_HMCON.HMEN](#) is automatically cleared.

ICACHE_HIT

ICACHE Hit Counter Register **XSFR(E414_H)** **Reset Value: 0000_H**



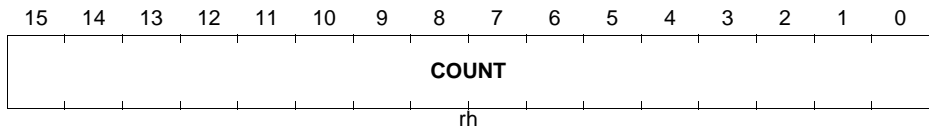
Field	Bits	Type	Description
COUNT	[15:0]	rh	ICACHE Hit Counter [15:0] Lower 16 bit of the ICACHE hit counter.

6.8.11 Miss Counter Register

The ICACHE miss counter register stores the lower 16 bit of the Miss Counter, with the upper part stored in [ICACHE_HMCON.HITH](#). If either the Hit or Miss counter reaches its maximum value both counters get stopped and the bit [ICACHE_HMCON.HMEN](#) is automatically cleared.

ICACHE_MISS

ICACHE Miss Counter Register **XSFR(E416_H)** **Reset Value: 0000_H**



Field	Bits	Type	Description
COUNT	[15:0]	rh	ICACHE Miss Counter [15:0] Lower 16 bit of the ICACHE miss counter.

7 Interrupt and Exception Control

The architecture of the XC27x8X supports several mechanisms for fast and flexible response to service requests from various sources internal or external to the micro controller. Different kinds of exceptions are handled in a similar way:

- Interrupts generated by the Interrupt Controller (ITC)
- DMA transfers issued by the Peripheral Event Controller (PEC)
- Traps caused by the TRAP instruction or issued by faults or specific system states

Normal Interrupt Processing

The CPU temporarily suspends the current program execution and branches to an interrupt service routine in order to service an interrupt requesting device. As a result, the current program status (IP, PSW, and, in segmentation mode, also CSP) is saved on the system stack. A prioritization scheme with sixteen priority levels specifies the execution order of multiple interrupt requests.

PEC Interrupt Processing

A faster alternative to normal interrupt processing is the use of the XC27x8X's integrated **Peripheral Event Controller** (PEC) to service an interrupt requesting device. Triggered by an interrupt request, the PEC performs a single word or byte data transfer between any two memory locations. During a PEC transfer, the normal program execution of the CPU is interrupted only for the data transfer. No internal program status information needs to be saved. The same prioritization scheme is used for PEC service as for normal interrupt processing.

Trap Functions

Trap Functions are activated in response to special conditions that occur during the execution of instructions. A trap can also be caused externally by the External Service Request pins ESRx (e.g. used to implement NMI like behavior). Several hardware trap functions are provided for handling erroneous conditions and exceptions that arise during the program execution. Hardware traps always have highest priority and cause immediate system reaction. The software trap function is invoked by the TRAP instruction that generates a software interrupt for a specified interrupt vector. For all types of traps, the current program status is saved on the system stack.

External Interrupt Processing

The XC27x8X does not provide dedicated external interrupt input pins but rather allows to configure a subset of its input pins as interrupt inputs. Interrupt (trap) input pins can be chosen from standard inputs or External Service Request pins ESRx. The available options are detailed in the **External Interrupts** section.

Interrupt Sources and Routing

To activate and correctly route an interrupt source programming of the following on-chip components must be considered:

- Interrupt control of each peripheral
- IMB memory controller **Interrupt Generation**
- SCU **External Request Unit (ERU)**
- **SCU Interrupt Generation**

Additionally the port programming must be considered if external interrupt sources are to be used.

7.1 Interrupt System Structure

The XC27x8X provides 112 separate interrupt nodes assignable to 16 priority levels, with 8 sub-levels (group priority) on each level. In order to support modular and consistent software design techniques, most sources of an interrupt or PEC request are supplied with a separate interrupt control register and an interrupt vector. The control register contains the interrupt request flag, the interrupt enable bit, and the interrupt priority of the associated source. Each source request is then activated by one specific event, determined by the selected operating mode of the respective device. For efficient resource usage, multi-source interrupt nodes are also incorporated. These nodes can be activated by several source requests, such as by different kinds of errors in the serial interfaces. However, specific status flags which identify the type of error are implemented in the respective peripheral control registers. Additional sharing of interrupt nodes is supported via [Interrupt Node Sharing](#).

The XC27x8X provides a vectored interrupt system. In this system specific vector locations in the memory space are reserved for the reset, trap, and interrupt service functions. Whenever a request occurs, the CPU branches to the location that is associated with the respective interrupt source. The Class B hardware traps all share the same interrupt vector. The status flags in the Trap Flag Register (TFR) can then be used to determine which exception caused the trap. For the special software TRAP instruction, the vector address is specified by the operand field of the instruction, which is a seven bit trap number.

The reserved vector locations build a jump table in the low end of a segment (selected by register VECSEG) in the XC27x8X's address space. The jump table consists of the appropriate jump instructions which transfer control to the interrupt or trap service routines and which may be located anywhere within the address space. The entries of the jump table are located at the lowest addresses in the selected code segment. Each entry occupies 2, 4, 8, or 16 words (selected by bitfield VECSC in register CPUCON1), providing room for at least one double word instruction. The respective vector location results from multiplying the trap number by the selected step width ($2^{(VECSC+2)}$).

All pending interrupt requests are arbitrated. The arbitration winner is indicated to the CPU together with its priority level and action request. The CPU triggers the corresponding action based on the required functionality (normal interrupt, PEC, jump table cache, etc.) of the arbitration winner.

An action request will be accepted by the CPU if the requesting source has a higher priority than the current CPU priority level and interrupts are globally enabled. If the requesting source has a lower (or equal) interrupt level priority than the current CPU task, it remains pending.

Interrupt and Exception Control

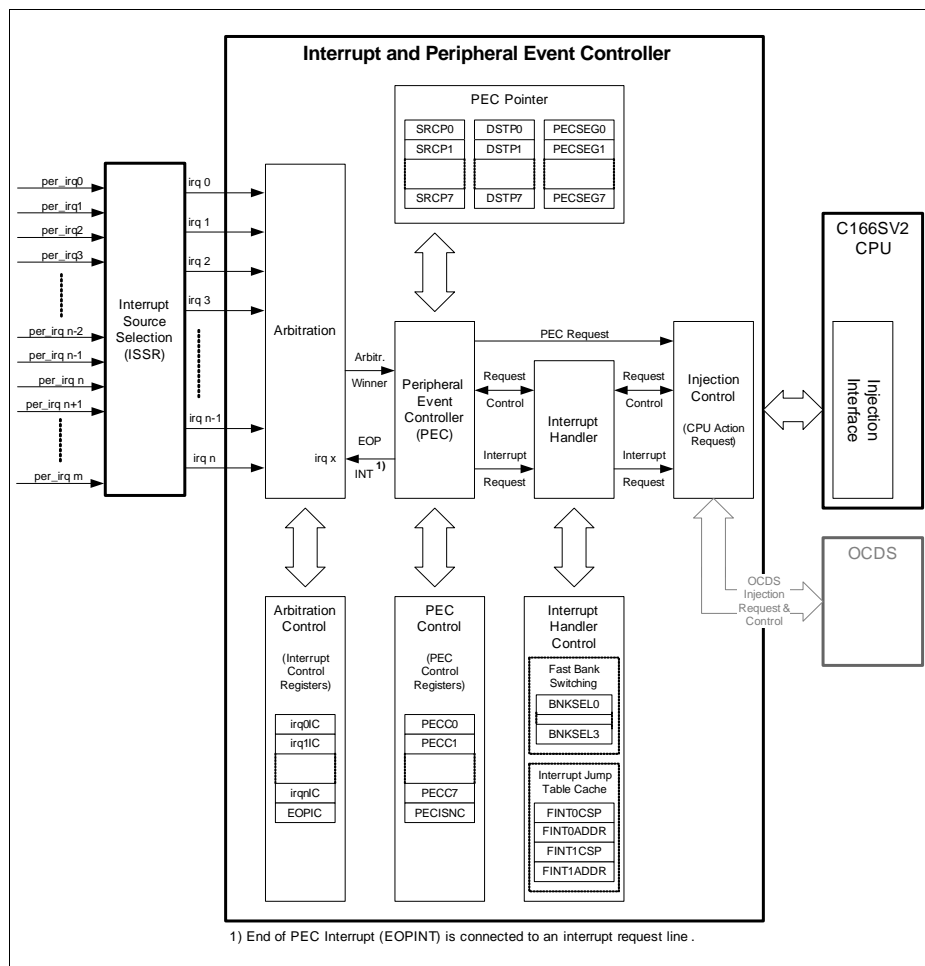


Figure 7-1 Block Diagram of the Interrupt and PEC Controller

7.2 Interrupt Arbitration

The XC27x8X interrupt arbitration system can handle interrupt requests from up to 112 sources. Interrupt requests may be triggered either by the internal peripherals or by external inputs. The “End of PEC” interrupt for supporting enhanced PEC functionality is connected internally to one of the interrupt request lines.

The arbitration process starts with an enabled interrupt request and stays active for as long as an enabled interrupt request is pending.

Each interrupt request line is controlled by its interrupt control register xxIC (here and below xx stands for the mnemonic of the respective interrupt source). An interrupt request event sets the interrupt request flag in the corresponding interrupt control register (bit xxIC.IR). The interrupt request can also be triggered by the software if the program sets the respective interrupt request bit.

If the request bit has been set and this interrupt request is enabled by the interrupt enable bit of the same control register (bit xxIC.IE), an arbitration cycle starts with the next clock cycle. However, if an arbitration cycle is currently in progress, the new interrupt request will be delayed until the next arbitration cycle. If an interrupt request (or PEC request) is accepted by the core, the respective interrupt request flag is cleared automatically.

All interrupt requests pending at the beginning of a new arbitration cycle are considered simultaneous. Within the arbitration cycle, the arbitration is independent of the actual request time.

The XC27x8X uses a three-stage interrupt prioritization scheme for interrupt arbitration as shown in [Figure 7-2](#).

Interrupt and Exception Control

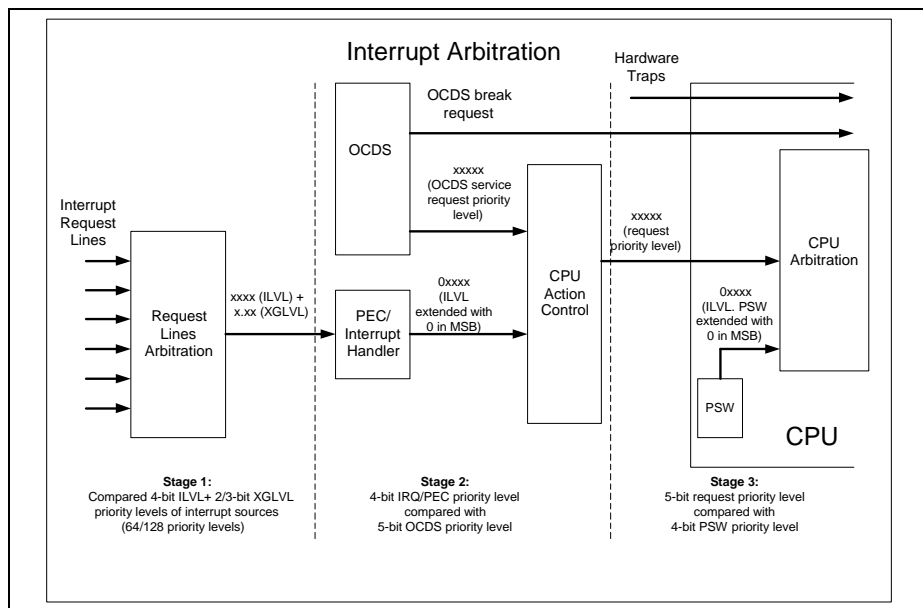


Figure 7-2 Interrupt Arbitration

The first arbitration stage compares the priority levels of interrupt request lines. The priority level of each requestor consists of interrupt priority level and group priority level. An interrupt priority level is programmed for each interrupt request line by the 4-bit bitfield ILVL of respective xxIC register. The group priority level is programmed for each interrupt request line by the 2-bit bitfield GLVL and the extension bit GPX of the register xxIC. Both together, GPX and GLVL form the 3-bit (extended) group priority level XGLVL, controlling up to eight interrupt sub-priorities within one of the 16 interrupt levels.

Note: All interrupt request sources that are enabled and programmed to the same interrupt priority level (ILVL) must have different group priority levels. Otherwise, an incorrect interrupt vector may be generated.

The second arbitration stage compares the priority of the first stage winner with the priority of OCDS service requests. OCDS service requests bypass the first stage of arbitration and go directly to the CPU Action Control Unit. The CPU Action Control Unit disregards the group priority level of interrupt/PEC requests and deals only with interrupt priority levels (ILVL). To compare with OCDS service request priority programmed by 5-bit value, the 4-bit ILVL of the interrupt/PEC request is extended to a 5-bit value with MSB equal to 0. This means that any OCDS request with MSB=1 will always win the second stage arbitration. However, if there is an OCDS request with MSB=0 conflicting with the same priority interrupt/PEC request, the latter is sent to the CPU.

Interrupt and Exception Control

On the third arbitration stage, the priority level of the second stage winner is compared with the priority of the current CPU task. An action request will be accepted by the CPU if the requesting source has a higher priority level than the current CPU priority level (bits ILVL of the PSW register) and interrupts are globally enabled by the global interrupt enable flag IEN in PSW. The CPU denies all requests in case of a cleared IEN flag. To compare with the 5-bit priority level of the second stage winner, the 4-bit ILVL.PSW is extended to a 5-bit value with MSB equal to 0. This means that any request with MSB=1 will always win the arbitration against any CPU level. If the requester has a lower or equal priority level than current CPU task, the request stays pending.

Note: Priority level 0000_B is the default level of the CPU. Therefore, a request on interrupt priority level 0000_B will be arbitrated, but the CPU will never accept an action request on this level. However, every enabled interrupt request (including a denied interrupt request and a priority level 0000_B request) triggers a CPU wake-up from idle state independent of setting the global interrupt enable bit PSW.IEN.

7.3 Interrupt Control

This section describes:

- interrupt control registers
- how to temporarily or selectively disable interrupts
- concept of interrupt class management

7.3.1 Interrupt Control Registers

All interrupt control registers are organized identically. The lower nine bits of an interrupt control register contain the complete interrupt control and status information of the associated source required during one round of prioritization (arbitration cycle). The upper seven bits of the respective register are reserved. All interrupt control registers are bit addressable and all control bits can be read or written via software. Therefore, each interrupt source can be programmed or modified with just one instruction. In the case of reading the interrupt control registers with instructions that operate with word data types, the upper 7 bits (15...9) will return zeros. It is recommended to always write zeros to these bit positions.

The IR bit of any IC register is of type “rwh” and is set by hardware upon occurrence of an interrupt. If the software requires to write to the IC register while the interrupt source is enabled the software write may conflict with a hardware access to bit IR. To address this conflict scenario all xxIC registers are located in the bit addressable memory area. The use of C166 bit modification instructions is therefore possible and recommended. These instructions provide a special “protection mask” feature which allows to protect IR bit from unintended software write. Refer to CPU Bit Manipulation Unit chapter for details.

The layout of the interrupt control registers shown below is applicable to all xxIC registers.

xxIC

Interrupt Control Register

(E)SFR (xxxx_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	GPX	IR	IE	ILVL				GLVL	
r	r	r	r	r	r	r	rw	rwh	rw			rw			rw

When accessing interrupt control registers through instructions which operate on word data types, their upper 7 bits (15 ... 9) will return zeros when read, and will discard written data. It is recommended to always write zeros to these bit positions.

The **Interrupt Request Flag** is set by hardware whenever a service request from its respective source occurs. It is cleared automatically upon entry into the interrupt service routine or upon a PEC service. In the case of PEC service, the Interrupt Request flag

Interrupt and Exception Control

remains set if the COUNT field in register PECCx of the selected PEC channel decrements to zero and bit EOPINT is cleared. This allows a normal CPU interrupt to respond to a completed PEC block transfer on the same priority level.

Note: Modifying the Interrupt Request flag via software causes the same effects as if it had been set or cleared by hardware.

The **Interrupt Enable Control Bit** determines whether the respective interrupt node takes part in the arbitration process (enabled) or not (disabled). The associated request flag will be set upon a source request in any case. The occurrence of an interrupt request can so be polled via xxIR even while the node is disabled.

Note: In this case the interrupt request flag xxIR is not cleared automatically but must be cleared via software.

7.3.2 Interrupt Priority Level and Group Level

The four bits of bitfield ILVL specify the priority level of a service request for the arbitration of simultaneous requests. The priority increases with the numerical value of ILVL: so, 0000_B is the lowest and 1111_B is the highest priority level.

When more than one interrupt request on a specific level becomes active at the same time, the values in the respective bitfields GPX and GLVL are used for second level arbitration to select one request to be serviced. Again, the group priority increases with the numerical value of the concatenation of bitfields GPX and GLVL, so 000_B is the lowest and 111_B is the highest group priority.

Note: All interrupt request sources enabled and programmed to the same priority level must always be programmed to different group priorities. Otherwise, an incorrect interrupt vector will be generated.

Upon entry into the interrupt service routine, the priority level of the source that won the arbitration and whose priority level is higher than the current CPU level, is copied into bitfield ILVL of register PSW after pushing the old PSW contents onto the stack.

The interrupt system of the XC27x8X allows nesting of up to 15 interrupt service routines of different priority levels (level 0 cannot be arbitrated).

Interrupt requests programmed to priority levels 15 ... 8 (i.e., ILVL = 1XXX_B) can be serviced by the PEC if the associated PEC channel is properly assigned and enabled (please refer to [Section 7.10.5](#)). Interrupt requests programmed to priority levels 7 through 1 will always be serviced by normal interrupt processing.

7.3.3 General Interrupt Control Functions in Register PSW

The acceptance of an interrupt request depends on the current CPU priority level (bitfield ILVL in register PSW) and the global interrupt enable control bit IEN in register PSW (see [Section 5.8](#)).

Interrupt and Exception Control

CPU Priority ILVL defines the current level for the operation of the CPU. This bitfield reflects the priority level of the routine currently executed. Upon entry into an interrupt service routine, this bitfield is updated with the priority level of the request being serviced. The PSW is saved on the system stack before the request is serviced. The CPU level determines the minimum interrupt priority level which will be serviced. Any request on the same or a lower level will not be acknowledged. The current CPU priority level may be adjusted via software to control which interrupt request sources will be acknowledged. PEC transfers do not really interrupt the CPU, but rather “steal” a single cycle, so PEC services do not influence the ILVL field in the PSW.

Hardware traps switch the CPU level to maximum priority (i.e. 15) so no interrupt or PEC requests will be acknowledged while an exception trap service routine is executed.

Note: The TRAP instruction does not change the CPU level, so software invoked trap service routines may be interrupted by higher requests.

Interrupt Enable bit IEN globally enables or disables PEC operation and the acceptance of interrupts by the CPU. When IEN is cleared, no new interrupt requests are accepted by the CPU. When IEN is set to 1, all interrupt sources, which have been individually enabled by the interrupt enable bits in their associated control registers, are globally enabled. Traps are non-maskable and are, therefore, not affected by the IEN bit.

Note: To generate requests, interrupt sources must be also enabled by the interrupt enable bits in their associated control register.

Register Bank Select bitfield BANK defines the currently used register bank for the CPU operation. When the CPU enters an interrupt service routine, this bitfield is updated to select the register bank associated with the serviced request:

- Requests on priority levels 15 ... 12 use the register bank pre-selected via the respective bitfield GPRSELx in the corresponding BNKSEL register
- Requests on priority levels 11 ... 1 always use the global register bank, i.e. BANK = 00_B
- Hardware traps always use the global register bank, i.e. BANK = 00_B
- The TRAP instruction does not change the current register bank

7.3.4 Selective Interrupt Disabling

Interrupt requests may be temporarily disabled and enabled during the execution of the software. This may be required to exclude specific interrupt sources based on the current status of the application. In particular, this is necessary to achieve a deterministic execution of time-critical code sequences.

Interrupt requests in the XC27x8X can be disabled and enabled on three different levels:

- Disable all interrupt requests for a certain code sequence
- Disable all interrupt requests globally
- Disable single interrupt requests

Interrupt and Exception Control

The **ATOMIC** and **EXTend** instructions automatically disable all interrupt requests for the duration of the following 1 ... 4 instructions. This is useful for semaphore handling, for example, and does not require to re-enable the interrupt system after the inseparable instruction sequence.

Global interrupt control is achieved with a single instruction:

```
BCLR IEN                ;Clear IEN flag (causes pipeline restart)
```

Specific interrupt control is achieved by controlling the enable bits in the associated interrupt control registers.

```
BCLR T2IE              ;Clear enable flag to disable intr.node
```

Due to pipeline effects, however, an interrupt request may be executed after the corresponding node was disabled, if the request coincides with clearing the enable flag.

If the application must avoid this, the following sequence can be used, ensuring that no interrupt requests from this source will be serviced after disabling the interrupt node:

```
BCLR IEN                ;Globally disable interrupts
BCLR T2IE              ;Disable Timer 2 interrupt node
JNB T2IE, Next          ;Any instruction reading T2IC can be used
Next:                  ;(assures that T2IC is written by BCLR
                      ;before being read by JNB or other instr.)
BSET IEN                ;Globally enable interrupts again
```

Please note that the sequence above blindly controls the global enable flag. If the global setting must not be changed, the code sequence can be enhanced, as shown below:

```
JNB IEN, GlobalIntOff
BCLR IEN                ;Globally disable interrupts
BCLR T2IE              ;Disable Timer 2 interrupt node
JNB T2IE, Next          ;Any instruction reading T2IC can be used
Next:                  ;(assures that T2IC is written by BCLR
                      ;before being read by JNB or other instr.)
BSET IEN                ;Globally enable interrupts again
JMPR cc_uc, Continue
GlobalIntOff:          ;Interrupts are globally disabled anyway
BCLR T2IE              ;Disable Timer 2 interrupt node

JNB T2IE, Continue     ;Reading T2IC can be omitted if the next
Continue:              ;few instructions do not set IEN
...
```

The same function can easily be implemented as a C macro:

```
#define Disable_One_Interrupt(IE_bit) \
{if(IEN) {IEN=0; IE_bit=0; while (IE_bit); IEN=1;} else \
{IE_bit=0; while IE_bit);}}
```

Usage Example:

Interrupt and Exception Control

```
Disable_One_Interrupt(T2IE) ; // T2 interrupt enable flag
```

ATOMIC or EXTend sequences preserve the status of the interrupt arbitration when they begin. An accepted request is processed after the ATOMIC/EXTend sequence. Therefore, the following code sequence may not produce the desired result:

```
AvoidThis:
```

```
ATOMIC #3
```

```
NOP
```

```
BCLR T2IE ;Disable Timer 2 interrupt node
```

```
NOP ;Timer 2 request may be processed
```

```
;after this instruction!!!
```

7.3.5 Interrupt Class Management

An interrupt class covers a set of interrupt sources with the same importance, i.e. the same priority from the system's viewpoint. Interrupts of the same class must not interrupt each other. The XC27x8X supports this function with two features:

- **Classes with up to eight members** can be established by using the same interrupt priority (ILVL) and assigning a dedicated group level to each member. This functionality is built-in and handled automatically by the interrupt controller.
- **Classes with more than eight members** can be established by using a number of adjacent interrupt priorities (ILVL) and the respective group levels (eight per ILVL). Each interrupt service routine within this class sets the CPU level to the highest interrupt priority within the class. All requests from the same or any lower level are blocked now, i.e. no request of this class will be accepted.

Interrupt and Exception Control

The example shown below establishes 3 interrupt classes which cover 2 or 3 interrupt priorities, depending on the number of members in a class. A level 6 interrupt disables all other sources in class 2 by changing the current CPU level to 8, which is the highest priority (ILVL) in class 2. Class 1 requests or PEC requests are still serviced, in this case. In this way, the interrupt sources (excluding PEC requests) are assigned to 3 classes of priority rather than to 7 different levels, as the hardware support would do.

Table 7-1 Software Controlled Interrupt Classes (Example)

ILVL (Priority)	Group Level								Interpretation
	7	6	5	4	3	2	1	0	
15									PEC service on up to 16 channels
14									
13									
12	X	X	X	X	X	X	X	X	Interrupt Class 1 9 sources on 2 levels
11	X								
10									
9									
8	X	X	X	X	X	X	X	X	Interrupt Class 2 17 sources on 3 levels
7	X	X	X	X	X	X	X	X	
6	X								
5	X	X	X	X	X	X	X	X	Interrupt Class 3 9 sources on 2 levels
4	X								
3									
2									
1									
0									No service!

7.4 Interrupt Vector Table

The XC27x8X provides a vectored interrupt system. This system reserves a set of specific memory locations, which are accessed automatically upon the respective trigger event. Entries for the following events are provided:

- Reset (hardware, software, watchdog)
- Traps (hardware-generated by fault conditions or via TRAP instruction)
- Interrupt service requests

Whenever a request is accepted, the CPU branches to the location associated with the respective trigger source. This vector position directly identifies the source causing the request, with the following exceptions:

- Class B hardware traps all share the same interrupt vector. The status flags in the Trap Flag Register (TFR) are used to determine which exception caused the trap. For details, see [Section 7.9](#).
- An interrupt node may be shared by several interrupt requests, e.g. within a module. Additional flags identify the requesting source, so the software can handle each request individually. For details, see [Section 7.14.2](#).
- The interrupt jump cache feature is used. For details, see [Section 7.5](#)

The reserved vector locations build a vector table located in the address space of the XC27x8X. The vector table usually contains the appropriate jump instructions that transfer control to the interrupt or trap service routines. These routines may be located anywhere within the address space. The location and organization of the vector table is programmable.

The Vector Segment register VECSEG defines the segment of the Vector Table (can be located in all segments, except for reserved areas).

Bitfield VECSC in register CPUCON1 defines the space between two adjacent vectors (can be 2, 4, 8, or 16 words). For a summary of register CPUCON1, please refer to [Section 5.4](#).

Each vector location has an offset address to the segment base address of the vector table (given by VECSEG). The offset can be easily calculated by multiplying the vector number with the vector space programmed in bitfield VECSC.

[Table 7-10](#) lists all sources capable of requesting interrupt or PEC service in the XC27x8X, the associated interrupt vector locations, the associated vector numbers, and the associated interrupt control registers.

Note: Interrupt nodes which are not used by their associated modules or are not connected to a module in the actual derivative may be used to generate software controlled interrupt requests by setting the respective IR flag.

VECSEG

Vector Segment Pointer

SFR(FF12_H)

Reset Value: 00XX_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0								
r	r	r	r	r	r	r	r								

VECSEG

rwh

Field	Bits	Type	Description
VECSEG	[7:0]	rwh	Segment number of the Vector Table
0	[15:8]	r	Reserved read as 0; should be written with 0.

The initial user value of register VECSEG is configured according to settings made for [Startup Configuration and Bootstrap Loading](#).

7.5 Interrupt Jump Table Cache

The mechanism that uses the vector table location as the entry point for the interrupt service routines can be overwritten by the Interrupt Controller (ITC). For a very fast interrupt response time, the XC27x8X offers the Interrupt Jump Table Cache (also called “fast interrupt”). The ITC can transfer to the CPU a 24-bit vector which is directly used as a start address for the service routine. This feature skips the path through the vector table which normally saves the execution of at least one branch. Therefore, avoiding the vector table may significantly improve interrupt response time. However, the number of 24-bit vectors in the ITC is limited.

Fast interrupt is available for two interrupt sources with interrupt priority levels greater than or equal to 12. The Interrupt Jump Table Cache skips the instruction fetches from the interrupt vector table and executes a direct jump to the interrupt service routines entry point. This feature is controlled by a set of two interrupt jump table cache registers (FINTxCSP, FINTxADDR) for each of the two jump table entries.

Every interrupt jump table cache entry contains an enable bit, an associated arbitration priority level (ILVL and GLVL), and the 24-bit address of the interrupt service routine. Note that only the two lower bits of the interrupt priority level are selectable in the respective control registers. The two upper bits of the interrupt priority level are fixed to 11_B, which limits the allowed interrupt priority level to be greater than or equal to 12.

FINT0CSP

Fast Interrupt Control 0 XSFR(EC00_H) Reset Value: 0000_H

FINT1CSP

Fast Interrupt Control 1 XSFR(EC04_H) Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	0	0	GPX	ILVL	GLVL	SEG									
rw	r	r	rw	rw	rw	rw									

Field	Bits	Type	Description
EN	15	rw	Fast Interrupt Enable 0 _B The interrupt jump table cache is disabled. No fast interrupt is used. 1 _B The interrupt jump table cache is enabled. A fast interrupt (direct jump to the interrupt service routine) is used instead of the normal fetch from the interrupt vector table.

Interrupt and Exception Control

Field	Bits	Type	Description
GPX	12	rw	Group Priority Extension This bit together with bitfield GLVL selects the group priority level (XGLVL) of the associated interrupt jump table cache entry.
ILVL	[11:10]	rw	Interrupt Priority Level This bitfield selects the lower two bits of the interrupt priority level associated with this interrupt jump table cache entry. <i>Note: The two upper bits of the interrupt priority level are fixed to 11_B, which ends in an interrupt priority level greater than or equal to 12.</i>
GLVL	[9:8]	rw	Group Priority Level This bitfield together with GPX-bit selects the group priority level (XGLVL) of the associated interrupt jump table cache entry.
SEG	[7:0]	rw	Segment Number of Interrupt Service Routine Address bits 23:16 of the interrupt service routine's entry point.
0	[14:13]	r	Reserved read as 0; should be written with 0.

FINT0ADDR

Fast Interrupt Address 0

XSFR (EC02_H)

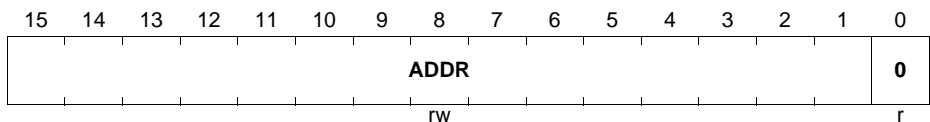
Reset Value: 0000_H

FINT1ADDR

Fast Interrupt Address 1

XSFR (EC06_H)

Reset Value: 0000_H



Field	Bits	Type	Description
ADDR	[15:1]	rw	Address of Interrupt Service Routine Address bits 15:1 of the interrupt service routine's entry point.

Interrupt and Exception Control

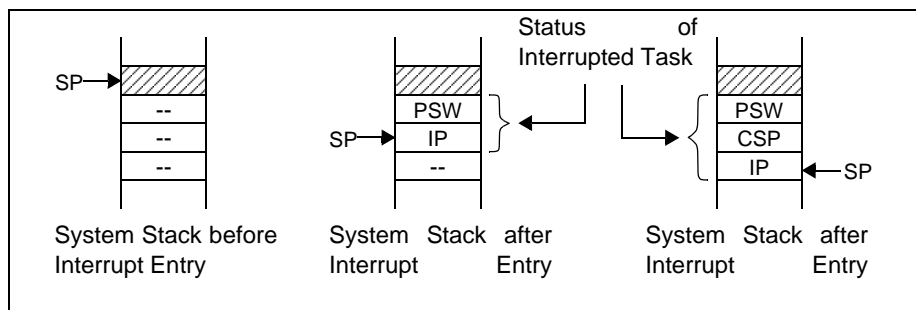
Field	Bits	Type	Description
0	0	r	Interrupt Service Routine Address Bit 0 LSB of the interrupt service routine's entry point address. This address bit is always 0 because of the program code's word alignment.

7.6 CPU Status Saving

Before an interrupt request that has been arbitrated is actually serviced, the status of the current task is automatically saved on the system stack. The CPU status (PSW) is saved together with the location at which execution of the interrupted task is to be resumed after returning from the service routine. This return location is specified through the Instruction Pointer (IP) and, in the case of a segmented memory model, the Code Segment Pointer (CSP). Bit SGTDIS in register CPUCON1 controls how the return location is stored.

- The system stack receives the PSW first, followed by the IP (unsegmented), or followed by CSP and then IP (segmented mode). This optimizes the usage of the system stack if segmentation is disabled.
- The CPU priority field (ILVL in PSW) is updated with the priority of the interrupt request to be serviced, so the CPU now executes on the new level.
- The register bank select field (BANK in PSW) is changed to select the register bank associated with the interrupt request. The association between interrupt requests and register banks are partly pre-defined and can partly be programmed.
- The interrupt request flag of the source being serviced is cleared. IP and CSP are loaded with the vector associated with the requesting source, and the first instruction of the service routine is fetched from the vector location which is expected to branch to the actual service routine (except when the interrupt jump table cache is used). All other CPU resources, such as data page pointers and the context pointer, are not affected.

When the interrupt service routine is exited (RETI is executed), the status information is popped from the system stack in the reverse order, taking into account the value of bit SGTDIS.



Task Status saved on the System Stack

7.7 CPU Context Switch

An interrupt service routine usually saves all the registers it uses on the stack and restores them before returning. To ease this process the XC27x8X allows switching the complete bank of CPU registers (GPRs) either automatically or with a single instruction, so that the service routine executes within its own separate context (see also [Section 5.5.2](#)).

There are two ways to switch context:

1. **Context switch on interrupt** automatically updates bitfield PSW.BANK to select one of the two local register banks or the current global register bank, so the service routine may now use its “own registers” directly. This local register bank is preserved when the service routine is terminated; thus, its contents are available on the next call. For interrupt priority levels 15 ... 12 the target register bank can be pre-selected. The register bank selection registers BNKSELx provide a 2-bit field for each priority level. The respective bitfield is then copied to bitfield BANK in register PSW to select the register bank, as soon as the respective interrupt request is accepted.
2. **Explicit context switch by software** is initiated by a write to CP or PSW registers.
 - a) A write to PSW.BANK bitfields allows to switch between global and local banks.
 - b) A write to CP allows to relocate the memory mapped global bank to another memory location.

For example the instruction “SCXT CP, #New_Bank” pushes the contents of the context pointer (CP) on the system stack and loads CP with the immediate value “New_Bank”. The new CP value sets a new global register bank. The service routine may now use its “own registers”. This global register bank is preserved when the service routine is terminated, i.e. its contents are available for the next call. Before returning (RETI), the previous CP simply be restored from the system stack using “POP CP”.

Note: Other resources used by an interrupting program (like DPP registers) must be saved and restored separately.

Note: There are certain timing restrictions during context switching associated with pipeline behavior. For details, see [Section 5.5.2](#).

7.8 Fast Bank Switching

The interrupt handler supports an additional enhanced feature (compared to the C166 family) for normal interrupts called Fast Bank Switching. To speed up interrupt handling, the core can use fast General Purpose Register (GPR) bank switching for interrupts with an interrupt level greater or equal than 12. For every arbitration priority level with $[ILVL = '15_D'-'12_D$ and $XGLVL = '7_D'-'0_D']$, the register bank can be selected with two bits. The select-bits are located in the four register bank selection registers BNKSELx ($x = 0...3$).

The following table identifies the arbitration priority level assignment to the respective bit fields within the four register bank selection registers:

Table 7-2 Register Bank Assignment

ILVL	XGLVL	Assigned GPRSELx Register	ILVL	XGLVL	Assigned GPRSELx Register
15	7	BNKSEL3.GPRSEL7	13	7	BNKSEL2.GPRSEL7
15	6	BNKSEL3.GPRSEL6	13	6	BNKSEL2.GPRSEL6
15	5	BNKSEL3.GPRSEL5	13	5	BNKSEL2.GPRSEL5
15	4	BNKSEL3.GPRSEL4	13	4	BNKSEL2.GPRSEL4
15	3	BNKSEL1.GPRSEL7	13	3	BNKSEL0.GPRSEL7
15	2	BNKSEL1.GPRSEL6	13	2	BNKSEL0.GPRSEL6
15	1	BNKSEL1.GPRSEL5	13	1	BNKSEL0.GPRSEL5
15	0	BNKSEL1.GPRSEL4	13	0	BNKSEL0.GPRSEL4
14	7	BNKSEL3.GPRSEL3	12	7	BNKSEL2.GPRSEL3
14	6	BNKSEL3.GPRSEL2	12	6	BNKSEL2.GPRSEL2
14	5	BNKSEL3.GPRSEL1	12	5	BNKSEL2.GPRSEL1
14	4	BNKSEL3.GPRSEL0	12	4	BNKSEL2.GPRSEL0
14	3	BNKSEL1.GPRSEL3	12	3	BNKSEL0.GPRSEL3
14	2	BNKSEL1.GPRSEL2	12	2	BNKSEL0.GPRSEL2
14	1	BNKSEL1.GPRSEL1	12	1	BNKSEL0.GPRSEL1
14	0	BNKSEL1.GPRSEL0	12	0	BNKSEL0.GPRSEL0

Interrupt and Exception Control

BNKSEL0

Register Bank Selection 0 **XSFR(EC20_H)** **Reset Value: 0000_H**

BNKSEL1

Register Bank Selection 1 **XSFR(EC22_H)** **Reset Value: 0000_H**

BNKSEL2

Register Bank Selection 2 **XSFR(EC24_H)** **Reset Value: 0000_H**

BNKSEL3

Register Bank Selection 3 **XSFR(EC26_H)** **Reset Value: 0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPRSEL7		GPRSEL6		GPRSEL5		GPRSEL4		GPRSEL3		GPRSEL2		GPRSEL1		GPRSEL0	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
GPRSEL0, GPRSEL1, GPRSEL2, GPRSEL3, GPRSEL4, GPRSEL5, GPRSEL6, GPRSEL7	[1:0], [3:2], [5:4], [7:6], [9:8], [11:10], [13:12], [15:14]	rw	Register Bank Selection 00 _B Global register bank 01 _B Reserved 10 _B Local register bank 1 11 _B Local register bank 2

Note: The GPRSELx value of the current triggered interrupt is automatically transferred into the Program Status Word (PSW).

:

7.9 Trap Functions

The C166SV2 CPU supports software and hardware trap functions.

7.9.1 Software Traps

The TRAP instruction is used to cause a software call to an interrupt service routine. The trap number specified in the operand field of the trap instruction determines which vector location of the vector table will be used.

The TRAP instruction has an effect similar to an interrupt request at the same vector. PSW, CSP (in segmentation mode), and IP are pushed into the system stack and then a jump is taken to the specified vector location. When a software trap is executed, the CSP for the trap service routine is loaded with the value of the VECSEG register. No Interrupt Request flags are affected by the TRAP instruction. The interrupt service routine called by a TRAP instruction must be terminated with a RETI (return from interrupt) instruction to ensure correct operation.

Note: The CPU priority level and the selected register bank in PSW register are not modified by the TRAP instruction; so, the service routine is executed with the same priority level as the interrupt task. Therefore, the service routine entered by the TRAP instruction can be interrupted by other traps or by higher priority interrupts, unless triggered by a real hardware event. The service routine also works with an unchanged register bank. If the hardware triggers the same service routine, register bank can be selected by the ITC and may be different.

Note: Software traps are also generated and issued, when data reads from the internal program memory space are requested which are not allowed, e.g. a user-read access to the protected Flash.

7.9.2 Hardware Traps

Hardware Traps are issued by faults or specific system states that occur during runtime (not identified at assembly time). The XC27x8X distinguishes twelve different hardware trap functions. When a hardware trap condition has been detected, the CPU branches to the trap vector location for the respective trap condition. The instruction causing the trap event is completed before the trap handling routine is entered.

Hardware traps are not-maskable and always have a priority higher than any other CPU task. If several hardware trap conditions are detected within the same instruction cycle, the highest priority trap is serviced (see [Table 7-3](#)). In case of a hardware trap, the injection unit injects a ITRAP instruction into the pipeline. The ITRAP instruction performs the following actions:

- Push PSW, CSP (in segmented mode) and IP into the System Stack
- Set CPU level in the PSW register to the highest possible priority level, which disables all interrupts and PEC transfers
- Select the global register bank for the trap service routine
- Branch to the trap vector location specified by the trap number of the trap condition

The hardware trap functions of the core are divided in two classes.

Class A traps are

- System Request 0 (SR0)
- Stack Overflow
- Stack Underflow
- Software Break

These traps share the same trap priority, but have an individual vector address.

Class B traps are

- System Request 1 (SR1)
- Memory Protection
- Undefined Opcode
- Memory Access Error
- Protection Fault
- Illegal Word Operand Access

The Class B traps share the same interrupt node and interrupt vector. The bit addressable Trap Flag Register (TFR) allows a trap service routine to identify the trap which caused the exception.

Note: The trap service routine must clear the respective trap flag; otherwise, a new trap will be requested after exiting the service routine. Setting a trap request flag by software causes the same effects as if it had been set by hardware.

Interrupt and Exception Control

The reset functions (hardware, software, watchdog) may be also regarded as a type of trap. Reset functions have the highest priority (trap priority III). Class A traps have the second highest priority (trap priority II), on the 3rd rank are class B traps (trap priority I); thus, a class A trap can interrupt a class B trap (for priority see also [Table 7-3](#)).

Class A Traps

Class A traps are generated by the high priority system request SR0 or by special CPU events such as the software break, a stack overflow, or an underflow event. Class A traps are not used to indicate hardware failures. After a class A event, a dedicated service routine is called to react to the events. Each class A trap has its own vector location in the vector table. After finishing the service routine, the instruction flow must be further correctly executed. This explains why class A traps cannot interrupt atomic/extend sequences and IO accesses in progress. For example, an interrupted extend sequence cannot be restarted.

All class A traps are generated in the pipeline during the execution of instructions, with the exception of SR0, which is an asynchronous external event. It is not possible for two different instructions in the pipeline to generate traps in the same CPU cycle. Class A trap events can be generated only during the memory stage of execution. An execution of instruction which caused a class A trap event is always completed. In the case of a class A trap, the pipeline is directly canceled and the IP of the instruction following the last executed one is pushed into the stack. In the case of an atomic/extend sequence or IO read access in progress, the execution continues till the sequence completion. Upon completion of the sequence, the IP of the instruction following the last one executed is pushed into the stack. Therefore, in the case of a class A trap, the stack always contains the IP of the first not-executed instruction in the instruction flow.

Note: The Branch Folding Unit allows an execution of branch instructions in parallel with the preceding instruction. The pre-processed branch instruction is combined with the preceding instruction. The branch is executed together with the instruction which caused the Class A trap. The IP of the first following not-executed instruction in the instruction flow is then pushed into the stack.

If more than one Class A trap occurs at a same time, they are prioritized internally. The SR0 trap has the highest priority and the software break has the lowest.

Note: In the case of two different class A trap occurring simultaneously, both trap flags are set. The IP of the instruction following the last one executed is pushed into the stack. The trap with the higher priority is executed. After return from the service routine, the IP is popped from the stack and immediately pushed again because of the other pending class A trap (unless the trap related to the second trap flag in TFR has been cleared by the first trap service routine).

Class B Traps

Class B traps are generated by unrecoverable hardware failures. In the case of a hardware failure, the CPU must immediately start a failure service routine. Class B traps can interrupt an atomic/extend sequence and an IO read access. After finishing the class B service routine, a restoration of the interrupted instruction flow is not possible.

All Class B traps have the same priority (trap priority I). When several class B traps become active at the same time, the corresponding flags in the TFR register are set and the trap service routine is entered. Because all class B traps have the same vector, the priority of service of simultaneously occurring class B traps is determined by the software in the trap service routine.

All class B traps are synchronous to instruction execution; most of them are generated in the pipeline during the execution of instructions. It is not possible for two different instructions in the pipeline to generate class A and class B traps in the same CPU cycle. Class B trap events can be generated only during memory stage execution. SR1 and ACER are exceptions, because they are generated by the SCU.

Instructions which caused a class B trap event are always executed. In the case of a class B trap, the pipeline is directly canceled and the IP of the instruction following the one which caused the trap is pushed on the stack. Therefore, the stack always contains the IP of the first following not executed instruction in the instruction flow.

Note: The Branch Folding Unit allows the execution of branch instructions in parallel with the preceding instruction. The pre-processed branch instruction is combined with the preceding instruction. The branch is executed together with the instruction causing the Class B trap. The IP of the first following not executed instruction in the instruction flow is pushed into the stack.

During execution of a class A trap service routine, any class B trap will not be serviced until the class A trap service routine is exited with a RETI instruction. In this case, the class B trap condition is stored in the TFR register, but the IP value of the instruction which caused this trap will be lost.

Note: If a class A trap occurs simultaneously with a class B trap, both trap flags are set. The IP of the instruction following the one which caused the trap is pushed into the stack, and the class A trap is executed. If this occurs during execution of an atomic/extend sequence or IO read access in progress, then the presence of the class B trap breaks the protection of atomic/extend operations and the class A trap will be executed immediately without waiting for the sequence completion. After return from the service routine, the IP is popped from the system stack and immediately pushed again because of the other pending class B trap. In this situation, the restoration of the interrupted instruction flow is not possible.

- **System Request 0 Trap (A):** The control signal is generated by the SCU. See chapter SCU Trap Generation.

Interrupt and Exception Control

- **Stack Overflow Trap (A):** Whenever the stack pointer is implicitly decremented and if the stack pointer was equal to the value in the stack overflow register STKOV, the STKOF flag in register TFR is set and the CPU will enter the stack overflow trap routine.
- **Stack Underflow Trap (A):** Whenever the stack pointer is implicitly incremented and if the stack pointer was equal to the value in the stack underflow register STKUN, the STKUF flag is set in register TFR, and the CPU will enter the stack underflow trap routine.
- **Software Break Trap (A):** When the instruction currently being executed by the CPU is a SBRK instruction, the SOFTBRK flag is set in register TFR and the CPU enters the software break debug routine. The flag generation of the software break instruction can be disabled by an On-chip Emulation Module. In this case, the instruction only breaks the instruction flow and signals this event to the debugger. The flag is not set and the trap will not be executed.
- **System Request 1 Trap (B):** The control signal is generated by the SCU. See chapter SCU Trap Generation.
- **Memory Protection Traps (B):** When an access violation outside the permitted address ranges is detected. Depending on the access type it is differentiated between Read (MPR), Write (MPW) and Execute (MPX) violations.
- **Undefined Opcode Trap (B):** When the instruction currently being decoded by the CPU does not contain a valid C166SV2 opcode, the UNDOPC flag is set in register TFR and the CPU enters the undefined opcode trap routine. The instruction which causes the undefined opcode trap is executed as a NOP.
- **Memory Access Error (B):** The control signal is generated by the SCU. See chapter SCU Trap Generation.
- **Protection Fault Trap (B):** Whenever one of the special protected instructions is executed where the opcode of that instruction is not repeated twice in the second word of the instruction and the byte following the opcode is not the complement of the opcode, the PRFTFLT flag in register TFR is set and the CPU enters the protection fault trap routine. The protected instructions include DISWDT, EINIT, IDLE, PWRDN, SRST, ENWDT and SRVWDT. The instruction which causes the protection fault trap is executed as a NOP. For products supporting MPU, RETI is also defined as a protected instruction in the sense that its execution is only allowed for privileged code, i.e. code executed with protection level 0. This flag is then used to indicate that a RETI instruction was tried to be executed from a protection level different to 0. Note that RETI will be still executed even if it causes a protection fault trap (it is not executed as a NOP).
- **Illegal Word Operand Access Trap (B):** Whenever a word operand read or write access (including Flash commands!) is attempted to an odd byte address, the ILLOPA flag in register TFR is set and the CPU enters the illegal word operand access trap routine.

Interrupt and Exception Control

Trap Vector Locations

Table 7-3 lists the vector locations for hardware traps and the corresponding status flags in register TFR. It also lists the priorities of trap service for those cases in which more than one trap condition might be detected within the same instruction. After any reset (hardware reset, software reset instruction SRST, or reset by watchdog timer overflow) program execution starts at the reset vector at location xx'0000_H. Reset conditions have priority over every other system activity and, therefore, have the highest priority (trap priority III).

Software traps may be initiated to any defined vector location. A service routine entered via a software TRAP instruction is always executed on the current CPU priority level which is indicated in bitfield ILVL in register PSW. This means that routines entered via the software TRAP instruction can be interrupted by all hardware traps or higher level interrupt requests.

Table 7-3 Hardware Trap Summary

Exception Condition	Trap Flag	Trap Vector	Vector Location ¹⁾	Vector Number	Trap Priority
Application Reset	—	RESET	xx'0000 _H	00 _H	III
Class A Hardware Traps:					
• System Request 0	SR0	SR0TRAP	xx'0008 _H	02 _H	II
• Stack Overflow	STKOF	STOTRAP	xx'0010 _H	04 _H	II
• Stack Underflow	STKUF	STUTRAP	xx'0018 _H	06 _H	II
• Software Break	SOFTBRK	SBRKTRAP	xx'0020 _H	08 _H	II
Class B Hardware Traps:					
• System Request 1	SR1	BTRAP	xx'0028 _H	0A _H	I
• Memory Protection	MPR/W/X	BTRAP	xx'0028 _H	0A _H	I
• Undefined Opcode	UNDOPC	BTRAP	xx'0028 _H	0A _H	I
• Memory Access Error	ACER	BTRAP	xx'0028 _H	0A _H	I
• Protected Instruction Fault	PRTFLT	BTRAP	xx'0028 _H	0A _H	I
• Illegal Word Operand Access	ILLOPA	BTRAP	xx'0028 _H	0A _H	I

1) Register VECSEG defines the segment where the vector table is located to.

Bitfield VECSC in register CPUCON1 defines the distance between two adjacent vectors. This table represents the default setting, with a distance of 4 (two words) between two vectors.

7.9.2.1 The Trap Flag Register TFR

The XC27x8X provides a number of trap vectors (class A and class B) which are indicated in the trap flag register TFR.

TFR

Trap Flag Register				SFR(FFAC _H /D6 _H)							Reset Value: 0000 _H				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SR0	STK OF	STK UF	SOF T BRK	SR1	MPR	MPW	MPX	UND OPC	0	0	AC ER	PRT FLT	ILL OPA	0	0
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	r	r	rwh	rwh	rwh	r	r

Field	Bits	Type	Description
SR0	15	rwh	System request flag 0 0 _B No trigger detected 1 _B The selected condition has been detected
STKOF	14	rwh	Stack overflow flag 0 _B No stack overflow event detected 1 _B The current stack pointer value falls below the contents of register STKOV
STKUF	13	rwh	Stack underflow flag 0 _B No stack underflow event detected 1 _B The current stack pointer value exceeds the contents of register STKUN
SOFTBRK	12	rwh	Software Break 0 _B No software break event detected 1 _B Software break event detected
SR1	11	rwh	System request flag 1 0 _B No trigger detected 1 _B The selected condition has been detected
MPR	10	rwh	Memory Protection Read 0 _B No read protection violation detected 1 _B Read protection violation detected
MPW	9	rwh	Memory Protection Write 0 _B No write protection violation detected 1 _B Write protection violation detected

Interrupt and Exception Control

Field	Bits	Type	Description
MPX	8	rwh	Memory Protection Execute 0 _B No execute protection violation detected 1 _B Execute protection violation detected
UNDOPC	7	rwh	Undefined Opcode 0 _B No undefined opcode event detected 1 _B The currently decoded instruction has no valid opcode
ACER	4	rwh	Memory Access Error 0 _B No access error event detected 1 _B Illegal or erroneous access detected
PRTFLT	3	rwh	Protection Fault 0 _B No protection fault event detected 1 _B A protected instruction with an illegal format has been detected
ILLOPA	2	rwh	Illegal word operand access 0 _B No illegal word operand access event detected 1 _B A word operand access (read or write) to an odd address has been attempted
0	[6:5], [1:0]	r	Reserved read as 0; should be written with 0.

Note: Flags TFR.15, TFR.11 and TFR.4 are generated via SCU. TFR.8, TFR.9 and TFR.10 are generated via MPU. Other flags are generated by the CPU.

7.10 Peripheral Event Controller

The "PEC" feature provides a DMA-like data transfer functionality.

7.10.1 PEC Functionality

The XC27x8X's Peripheral Event Controller (PEC) provides 16 PEC service channels which can be used to perform the following tasks:

- Repeatable DMA-like data transfers with
 - selectable byte or word data type
 - automatic increment of source and/or destination pointers
 - support of channel linking using two alternating channels
- Interrupt request upon data transfer completion programmable to the
 - interrupt node associated with the PEC channel
 - "End of PEC" interrupt node shared by all PEC channels

Each single PEC transfer is triggered by an interrupt service request. Because of this it is executed only if its priority level is higher than current CPU priority level.

A PEC transfer is the fastest possible interrupt response. In many cases it is sufficient to service peripheral requests (for example, serial channels, etc.). PEC transfers are fast because they are executed by the CPU "on-the-fly". The program flow is not changed by the PEC action itself. Therefore the current program status and context needs not to be saved and restored as with standard interrupts.

7.10.2 Source and Destination Pointers

The PEC channels source and destination pointers specify the locations between which the data is to be moved.

All pointers x are 24-bits wide. The 24-bit source address is stored in the register SRCP x (lower 16 bits of address) and in the high byte of register PECSEG x (highest 8 address bits). The 24-bit destination address is stored in the register DSTP x (lower 16 bits of address) and in the low byte of register PECSEG x (highest 8 address bits).

Only the lower 16 bits of the PEC address pointers (segment offset) can be modified by the PEC Increment Control hardware (programmed by PECC x .INC). The highest 8 bits, which represent the segment number, are not modified by hardware. Therefore, the PEC pointers may be incremented within the address space of one segment and may not cross the segment border. If the offset address pointer reaches FFFF $_H$ in case of byte transfers (BWT = 1) or FFFE $_H$ in case of word transfers (BWT = 0), the next increment will be disregarded. The address register will keep one of these maximum values and no overflow will happen. This behavior protects subsequent memory from unintentional overwriting. No explicit error event is generated by the system in case of address pointer(s) saturation; therefore, it is the user's responsibility to handle this condition.

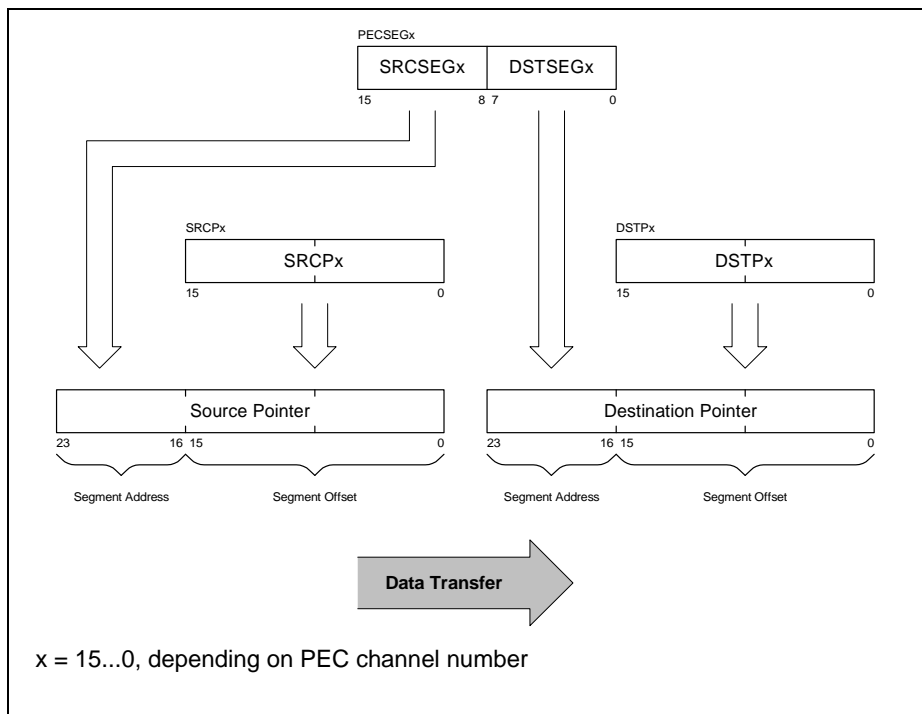


Figure 7-3 PEC Pointer Address Composition

Note: PEC data transfers do not use the data page pointers DPP3...DPP0.

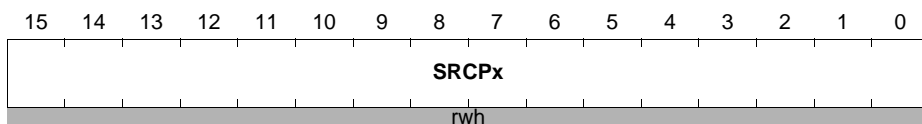
Note: If a word data transfer is selected for a specific PEC channel (i.e. BWT = 0), the respective source and destination pointers must both contain a valid word address which points to an even byte boundary. Otherwise, the Illegal Word Operand Access trap will be invoked when this channel is used.

SRCP_x (x=0-15)

PEC Source Pointer x

XSFR(EC40_H+4*x)

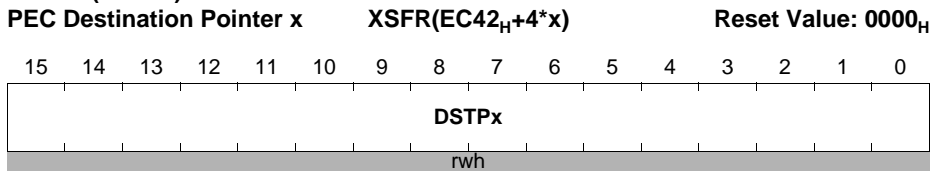
Reset Value: 0000_H



Interrupt and Exception Control

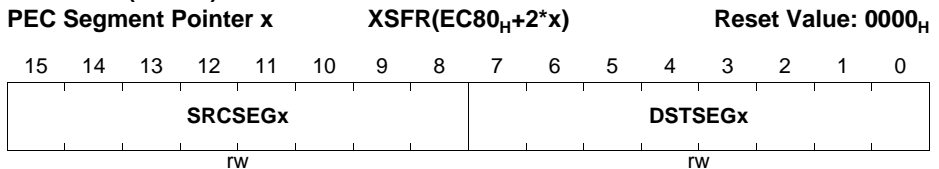
Field	Bits	Type	Description
SRCPx	[15:0]	rwh	Source Pointer Offset of Channel x Source address bits 15 ... 0

DSTPx (x=0-15)



Field	Bits	Type	Description
DSTPx	[15:0]	rwh	Destination Pointer Offset of Channel x Destination address bits 15 ... 0

PECSEGx (x=0-15)



Field	Bits	Type	Description
SRCSEGx	[15:8]	rw	Source Pointer Segment of Channel x Source address bits 23 ... 16
DSTSEGx	[7:0]	rw	Destination Pointer Segment Address of Channel x Destination address bits 23 ... 16

7.10.3 Functional Control

Each PEC channel x is controlled by its respective PEC control register PECCx. The registers are used to program the PECs functional operation mode and associated options. The following operation modes are supported:

- **Short Transfer Mode**
- **Long Transfer Mode**
- **Channel Link Mode for Data Chaining**

For control of the long transfer mode the extended control registers PECXCx are additionally provided.

PECCx (x=0-7)

PEC Channel Control x **SFR(FEC0_H+2*x)** **Reset Value: 0000_H**

PECCy (y=8-15)

PEC Channel Control y **SFR(EC90_H+2*y)** **Reset Value: 0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PT	EOP INT	PLEV	CL	INC	BWT	COUNT									
rw	rw	rw	rw	rw	rw	rwh									

Field	Bits	Type	Description
PT	15	rw	Transfer Mode 0 _B Short Transfer Mode 1 _B Long Transfer Mode
EOPINT	14	rw	End of PEC Interrupt Selection 0 _B End of PEC interrupt with the same level as the PEC transfer is triggered 1 _B End of PEC interrupt is serviced by a separate interrupt node with programmable interrupt level (EOPIC) and interrupt sharing control register (PECISNC)
PLEV	[13:12]	rw	PEC Level Selection 00 _B Interrupt Levels 15 and 14 selected 01 _B Interrupt Levels 13 and 12 selected 10 _B Interrupt Levels 11 and 10 selected 11 _B Interrupt Levels 9 and 8 selected
CL	11	rw	Channel Link Control 0 _B PEC channels work independent 1 _B Pairs of channels are linked together

Interrupt and Exception Control

Field	Bits	Type	Description
INC	[10:9]	rw	Increment Control (Modification of source and destination pointer after PEC transfer) 00 _B No modification 01 _B Increment of destination pointer DSTPx by 1 (BWT = 1) or by 2 (BWT = 0) 10 _B Increment of source pointer SRCPx by 1 (BWT = 1) or by 2 (BWT = 0) 11 _B Increment of destination pointer DSTPx and source pointer SRCPx by 1 (BWT = 1) or by 2 (BWT = 0)
BWT	8	rw	Byte/Word Transfer Selection 0 _B Transfer a word 1 _B Transfer a byte
COUNT	[7:0]	rwh	PEC Short Transfer Count Counts PEC transfers and influences the channel's action (see Table 7-4)

PECXC0

PEC Extended Count Register 0 **SFR(ECB0_H)** **Reset Value: 0000_H**

PECXC2

PEC Extended Count Register 2 **SFR(ECB2_H)** **Reset Value: 0000_H**

PECXC4

PEC Extended Count Register 4 **SFR(ECB4_H)** **Reset Value: 0000_H**

PECXC6

PEC Extended Count Register 6 **SFR(ECB6_H)** **Reset Value: 0000_H**

PECXC8

PEC Extended Count Register 8 **SFR(ECB8_H)** **Reset Value: 0000_H**

PECXC10

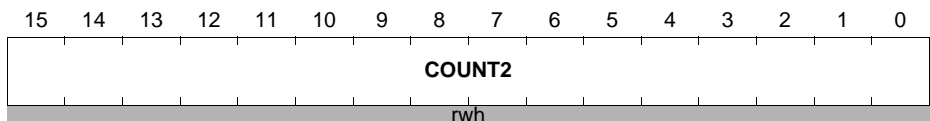
PEC Extended Count Register 10 **SFR(ECBA_H)** **Reset Value: 0000_H**

PECXC12

PEC Extended Count Register 12 **SFR(ECBC_H)** **Reset Value: 0000_H**

PECXC14

PEC Extended Count Register 14 **SFR(ECBE_H)** **Reset Value: 0000_H**



Interrupt and Exception Control

Field	Bits	Type	Description
COUNT2	[15:0]	rwh	PEC Long Transfer Count Counts PEC transfers and influences the channel's action (see Table 7-5)

Short Transfer Mode

If the short transfer mode is enabled by setting PT=0 the PEC transfer count field COUNT controls directly the action of the associated PEC channel according to [Table 7-4](#). Besides the option to have continuous transfers this mode supports up to 254 consecutive transfers.

Table 7-4 Short Transfer Mode Channel Actions

Previous COUNT field value	Modified COUNT field value	Action of PEC Channel and Comments
FF _H	FF _H	Move a Byte/Word Continuous transfer mode, i.e. COUNT is not modified
FE _H ...02 _H	FD _H ...01 _H	Move a Byte/Word and decrement COUNT
01 _H	00 _H	Move a Byte/Word Depending on bit EOPINT, one of two different actions are taken: EOPINT=0 The service request flag (xxIC.IR) of the respective interrupt remains set (it is cleared for all other COUNT values). Therefore, an additional interrupt request is triggered on the next arbitration cycle with a COUNT field value of 00 _H (see next row) EOPINT=1 The service request flag (xxIC.IR) of the respective interrupt is cleared. Additionally, the interrupt request flag of the EOP sub node control register PEC(X)ISNC.CxIR is set. Furthermore, the interrupt request flag of the end of PEC interrupt node (EOPIC.EOPIR) is automatically set if the sub node request is enabled PEC(X)ISNC.CxIE = 1'.
00 _H	00 _H	No PEC action! A normal interrupt is requested instead of a PEC data transfer.

Long Transfer Mode

If the long transfer mode is enabled by setting PT=1 the extended PEC transfer count field PECXCx.COUNT2 directly controls the action of the associated PEC channel according to [Table 7-5](#). This mode supports up to 65,535 consecutive transfers.

Table 7-5 Long Transfer Mode Channel Actions

Previous COUNT2 field value	Modified COUNT2 field value	Action of PEC Channel and Comments
FFFF _H ...0002 _H	FFFE _H ...0001 _H	Move a Byte/Word and decrement COUNT2
0001 _H	0000 _H	<p>Move a Byte/Word Depending on bit EOPINT, one of two different actions are taken:</p> <p>EOPINT=0 The service request flag (xxIC.IR) of the respective interrupt remains set (it is cleared for all other COUNT2 values). Therefore, an additional interrupt request is triggered on the next arbitration cycle with a COUNT2 field value of 0000_H (see next row)</p> <p>EOPINT=1 The service request flag (xxIC.IR) of the respective interrupt is cleared. Additionally, the interrupt request flag of the EOP sub node control register PEC(X)ISNC.CxIR is set. Furthermore, the interrupt request flag of the end of PEC interrupt node (EOPIC.EOPIR) is automatically set if the sub node request is enabled PEC(X)ISNC.CxIE = 1'.</p>
0000 _H	0000 _H	<p>No PEC action! A normal interrupt is requested instead of a PEC data transfer.</p>

Channel Link Mode for Data Chaining

Channel linking, if enabled, links two channels together to commonly serve the same data transfer task.

The whole data transfer (for example a peripheral message) is divided into separately controlled and chained block transfers. The two PEC channels which are linked together, handle chained block transfers alternately to each other. At the end of a data block transfer, controlled by one PEC channel, automatically the other (linked) PEC channel is started to continue the transfer with the next data block.

Channel linking and thus data (block) chaining is supported within pairs of PEC channels (channels 0&1, 2&3 a.s.o.). Each data block is controlled by one PEC channel of the channel pair. While one of the two channels is active, the CPU can update the pointer and counter values of the other channel to prepare it for continuation of data transfer after next channel linking.

Channel linking is enabled, if in the active PEC channel of the channel pair the Channel Link Control Bit "CL" in its PECCx register is set to 1. The data transfer of linked channels is started always with the even numbered channel of the channel pair. If in Channel Link mode (at least one CL bit of the pair is set) the channel's data block is completely transferred the PEC service request processing is automatically switched to the other PEC channel of the channel-pair.

Channel linking and thus the switching from one channel to the other channel is performed, when the CL bit of first (active) channel is set (in its PEC control register) and its transfer count is changed from one to zero with the last transfer. If the channel link flag CL of the first (terminated) PEC control register is found to be zero or if the count field of linked channel is zero, the whole data transfer is finished.

Note: The CL-flags are fully controlled by software and should be cleared by SW when the whole data transfer shall be finished and the termination of transfer shall be executed. Because termination can also be entered with a zero-value of the transfer count field of linked channel, termination of whole data transfer is automatically performed if the channels count field was not updated after the last channel link interrupt for this channel.

When a data block of a linked channel is completely transferred and PEC servicing switches to the other channel of channel pair, a channel specific channel link interrupt is generated (for the old channel) to inform the CPU that the channel is inactive now and may be configured for its next block transfer. The channel link interrupt is requested, indicated and enabled in the respective PEC Interrupt Subnode Control Register (PECISNC), which is also used for the channel's End of PEC interrupt. Thus, all channel link interrupts are also controlled with the one EOP Interrupt Control register EOPIC and therefore with the same interrupt priority level as the EOP interrupt. This service request node requests CPU interrupt service in case of one or more pending channel link interrupt requests or End of PEC interrupt requests, if the respective enable control bit(s)

Interrupt and Exception Control

is (are) set in the PEC interrupt subnode control register PECISNC and in the interrupt control register EOPIC.

Note: The generation of Channel Link/EOP interrupt is automatically enabled, if the CL-bit of the active (terminated) channel is set. If it is not set, either a standard interrupt or an EOP interrupt is initiated according to the EOPINT bit in the channel's PEC Control Register. The channel is not switched in this case, because a missing CL flag defines the last block of data transfer.

Note: If Channel Link mode is active (at least one of the pair's CL bits is set), interrupt requests connected to the odd channel (via priority levels) will trigger only a standard interrupt but no PEC transfer.

Note: The start of data transfer on linked channels is always performed with the even numbered PEC channel of the channel pair.

7.10.4 End of PEC Interrupt Control

The EOPIC register is the interrupt control register of the End Of PEC interrupt.

EOPIC

End Of PEC Interrupt Control **ESFR(F19E_H/CF_H)** **Reset Value: 0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	GPX	EOP IR	EOP IE	ILVL			GLVL		
r	r	r	r	r	r	r	rw	rwh	rw	rw			rw		

PEC Interrupt Sub Node Control Register

The Registers PECISNC and PECXISNC contain flags of the “End of PEC” interrupt node. This node is used when control bit PECCx.EOPINT=1.

PECISNC

PEC Interrupt Sub Node Control SFR(FFD8_H/EC_H) **Reset Value: 0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C7IR	C7IE	C6IR	C6IE	C5IR	C5IE	C4IR	C4IE	C3IR	C3IE	C2IR	C2IE	C1IR	C1IE	C0IR	C0IE
rwh	rw	rwh	rw	rwh	rw	rwh	rw	rwh	rw	rwh	rw	rwh	rw	rwh	rw

Field	Bits	Type	Description
CxIR (x=0-7)	2*x+1	rwh	Interrupt Sub Node Request Flag of PEC Channel x 0 _B No special end of PEC interrupt request is pending for PEC channel x 1 _B PEC channel x has raised an end of PEC interrupt request
CxIE (x=0-7)	2*x	rw	Interrupt Sub Node Enable Control Bit of PEC Channel x ¹⁾ (individually enables/disables a specific source) 0 _B End of PEC interrupt request of PEC channel x is disabled 1 _B End of PEC interrupt request of PEC channel x is enabled

1) It is recommended to clear an interrupt request flag (CxIR) before setting the respective enable flag (CxIE). Otherwise, former requests still pending will immediately trigger an interrupt request after setting the enable bit.

Interrupt and Exception Control

Note: The “End of PEC” sub-node interrupt request flags are not cleared by hardware when entering the interrupt service routine (interrupt has been accepted by the CPU), unlike the interrupt request flags of the interrupt nodes (request flags $xxIC.xxIR$). The interrupt service routine must check the request flags and clear them before executing the RETI instruction.

PECXISNC

PEC Interrupt Sub Node Control SFR(FFD6_H/EB_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C15 IR	C15 IE	C14 IR	C14 IE	C13 IR	C13 IE	C12 IR	C12 IE	C11 IR	C11 IE	C10 IR	C10 IE	C9IR	C9IE	C8IR	C8IE
rwh	rw	rwh	rw	rwh	rw	rwh	rw	rwh	rw	rwh	rw	rwh	rw	rwh	rw

Field	Bits	Type	Description
CxIR (x=8-15)	2*x+1	rwh	Interrupt Sub Node Request Flag of PEC Channel x 0 _B No special end of PEC interrupt request is pending for PEC channel x 1 _B PEC channel x has raised an end of PEC interrupt request
CxIE (x=8-15)	2*x	rw	Interrupt Sub Node Enable Control Bit of PEC Channel x ¹⁾ (individually enables/disables a specific source) 0 _B End of PEC interrupt request of PEC channel x is disabled 1 _B End of PEC interrupt request of PEC channel x is enabled

- 1) It is recommended to clear an interrupt request flag (CxIR) before setting the respective enable flag (CxIE). Otherwise, former requests still pending will immediately trigger an interrupt request after setting the enable bit.

Note: The “End of PEC” sub-node interrupt request flags are not cleared by hardware when entering the interrupt service routine (interrupt has been accepted by the CPU), unlike the interrupt request flags of the interrupt nodes (request flags $xxIC.xxIR$). The interrupt service routine must check the request flags and clear them before executing the RETI instruction.

Generation of the “End of PEC” interrupt

As shown in [Figure 7-4](#) the request flag of the “End of PEC” interrupt EOPIC.IR can be generated from any of the PEC sub nodes. Single or multiple sub node event(s) produce a single EOPIC.IR trigger. The EOPIC interrupt service routine therefore must evaluate (and reset) all sub node request flags.

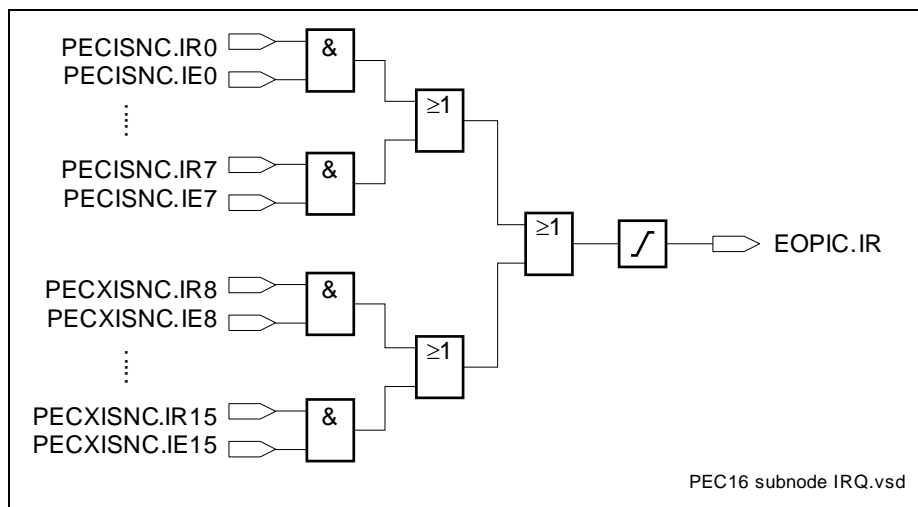


Figure 7-4 End of PEC Interrupt Sub Node

7.10.5 Channel Assignment

All interrupt requests with interrupt priority levels 8 to 15 can be associated with the PEC functionality. The PEC channel used for executing the transfer depends on the programming of the interrupt, group and PEC levels.

Note that the programming of the PEC level (PECC.PLEV - see [Section](#)) and Interrupt level ([xxIC.ILVL](#)) must match to make the assignment valid. All interrupt requests not assigned to a PEC channel go to the interrupt service routine handler.

The following table lists the possible channel assignments.

Table 7-6 PEC Channel Assignment

ICx.GPX	ICx.ILVL(0)	ICx.GLVL	Assigned PEC Channel
1 _B	1 _B	11 _B	15
1 _B	1 _B	10 _B	14
1 _B	1 _B	01 _B	13

Interrupt and Exception Control

Table 7-6 PEC Channel Assignment (cont'd)

ICx.GPX	ICx.ILVL(0)	ICx.GLVL	Assigned PEC Channel
1 _B	1 _B	00 _B	12
1 _B	0 _B	11 _B	11
1 _B	0 _B	10 _B	10
1 _B	0 _B	01 _B	9
1 _B	0 _B	00 _B	8
0 _B	1 _B	11 _B	7
0 _B	1 _B	10 _B	6
0 _B	1 _B	01 _B	5
0 _B	1 _B	00 _B	4
0 _B	0 _B	11 _B	3
0 _B	0 _B	10 _B	2
0 _B	0 _B	01 _B	1
0 _B	0 _B	00 _B	0

7.11 External Interrupts

Although the XC27x8X has no dedicated interrupt input pins, it supports many possibilities to react to external asynchronous events by providing a number of IO lines which can be selected as interrupt inputs.

7.11.1 External Request Unit

Please refer to the [External Request Unit \(ERU\)](#) chapter. The ERU provides routing capabilities and allows to define advanced trigger conditions for the interrupt input signals. The resulting ERU interrupt requests are forwarded to the interrupt controller registers ERU_0IC ... ERU_3IC.

7.11.2 Using Peripheral Pins

The interrupt function of some peripheral pins may be either combined with the pin's main function or used instead of it if the main pin function is not required.

Table 7-7 Pins Usable as External Interrupt Inputs

Port Pin	Original Function	Control Register
P4.7-0/CC31-24IO	CAPCOM Register 31-24 Capture Input	CC31-CC24 ¹⁾
P2.10-3/CC23-16IO	CAPCOM Register 23-16 Capture Input ²⁾	CC23-CC16 ¹⁾
P4.2/T2IN	Auxiliary timer T2 input pin	T2CON
P4.6/T4IN	Auxiliary timer T4 input pin	T4CON
P2.10/CAPIN	GPT2 capture input pin ²⁾	T5CON

1) Must be enabled by [Interrupt Node Sharing](#).

2) Pin P2.10 overlays two possible input functions.

For each of these pins, either a positive, a negative, or both a positive and a negative external transition can be selected to cause an interrupt or PEC service request. The edge selection is performed in the control register of the peripheral device associated with the respective port pin. The peripheral must be programmed to a specific operating mode to allow generation of an interrupt by the external signal. The priority of the interrupt request is determined by the interrupt control register of the respective peripheral interrupt source, and the interrupt vector of this source will be used to service the external interrupt request.

Note: In order to use any of the listed pins as an external interrupt input, it must be switched to input mode via its port control register.

When port pins CCxIO are to be used as external interrupt input pins, bitfield CCMODx in the control register of the corresponding capture/compare register CCx must select capture mode. When CCMODx is programmed to 001_B, the interrupt request flag CCxIR

Interrupt and Exception Control

in register CCxIC will be set on a positive external transition at pin CCxIO. When CCMODx is programmed to 010_B, a negative external transition will set the interrupt request flag. When CCMODx = 011_B, both a positive and a negative transition will set the request flag. In all three cases, the contents of the allocated CAPCOM timer will be latched into capture register CCx, independent of whether or not the timer is running. When the interrupt enable bit CCxIE is set, a PEC request or an interrupt request for vector CCxINT will be generated.

Pins T2IN or T4IN can be used as external interrupt input pins when the associated auxiliary timer T2 or T4 in block GPT1 is configured for capture mode. This mode is selected by programming the mode control fields T2M or T4M in control registers T2CON or T4CON to 101_B. The active edge of the external input signal is determined by bitfields T2I or T4I. When these fields are programmed to X01_B, interrupt request flags T2IR or T4IR in registers T2IC or T4IC will be set on a positive external transition at pins T2IN or T4IN, respectively. When T2I or T4I is programmed to X10_B, then a negative external transition will set the corresponding request flag. When T2I or T4I is programmed to X11_B, both a positive and a negative transition will set the request flag. In all three cases, the contents of the core timer T3 will be captured into the auxiliary timer registers T2 or T4 based on the transition at pins T2IN or T4IN. When the interrupt enable bits T2IE or T4IE are set, a PEC request or an interrupt request for vector T2INT or T4INT will be generated.

Pin CAPIN differs slightly from the timer input pins as it can be used as external interrupt input pin without affecting peripheral functions. When the capture mode enable bit T5SC in register T5CON is cleared to '0', signal transitions on pin CAPIN will only set the interrupt request flag CRIR in register CRIC, and the capture function of register CAPREL is not activated.

So register CAPREL can still be used as reload register for GPT2 timer T5, while pin CAPIN serves as external interrupt input. Bitfield CI in register T5CON selects the effective transition of the external interrupt input signal. When CI is programmed to 01_B, a positive external transition will set the interrupt request flag. CI = 10_B selects a negative transition to set the interrupt request flag, and with CI = 11_B, both a positive and a negative transition will set the request flag. When the interrupt enable bit CRIE is set, an interrupt request for vector CRINT or a PEC request will be generated.

7.12 OCDS Requests

The OCDS module issues high-priority break requests or standard service requests. The break requests are routed directly to the CPU (like the hardware trap requests) and are prioritized there. Therefore, break requests ignore the standard interrupt arbitration and receive highest priority.

The standard OCDS service requests are routed to the CPU Action Control Unit together with the arbitrated interrupt/PEC requests. The service request with the higher priority is sent to the CPU to be serviced. If both the interrupt/PEC request and the OCDS request have the same priority level, the interrupt/PEC request wins.

This approach ensures precise break control, while affecting the system behavior as little as possible.

The CPU Action Control Unit also routes back request acknowledges and denials from the core to the corresponding requestor.

7.13 Service Request Latency

The numerous service requests of the XC27x8X (requests for interrupt or PEC service) are generated asynchronously with respect to the execution of the instruction flow. Therefore, these requests are arbitrated and are inserted into the current instruction stream. This decouples the service request handling from the currently executed instruction stream, but also leads to a certain latency.

The request latency is the time from activating a request signal at the interrupt controller (ITC) until the corresponding instruction reaches the pipeline's execution stage.

Table 7-8 lists the consecutive steps required for this process.

Table 7-8 Steps Contributing to Service Request Latency

Description of Step	Interrupt Response	PEC Response
Request arbitration in 3 stages, leads to acceptance by the CPU (see Section 7.2)	3 cycles	3 cycles
Injection of an internal instruction into the pipeline's instruction stream	4 cycles	4 cycles
The first instruction fetched from the interrupt vector table reaches the pipeline's execution stage	4 cycles / 0 ¹⁾	- - -
Resulting minimum request latency	11/7 cycles	7 cycles

1) Can be saved by using the interrupt jump table cache (see [Section 7.5](#)).

Sources for Additional Delays

Because the service requests are inserted into the current instruction stream, the properties of this instruction stream can influence the request latency.

Table 7-9 Additional Delays Caused by System Logic

Reason for Delay	Interrupt Response	PEC Response
Interrupt controller busy, because the previous interrupt request is still in process	max. 7 cycles	max. 7 cycles
Pipeline is stalled, because instructions preceding the injected instruction in the pipeline need to write/read data to/from a peripheral or memory	$2 \times T_{ACCmax}^{1)}$	$2 \times T_{ACCmax}$
Pipeline cancelled, because instructions preceding the injected instruction in the pipeline update core SFRs	4 cycles	4 cycles
Memory access for stack writes (if not to DPRAM or DSRAM)	$2/3 \times T_{ACC}^{2)}$	- - -
Memory access for vector table read (except for intr. jump table cache)	$2 \times T_{ACC}$	- - -

1) This is the longest possible access time within the XC27x8X system.

2) Depending on segmentation off/on.

The actual response to an interrupt request may be delayed further depending on programming techniques used by the application. The following factors can contribute:

- Actual interrupt service routine is only reached via a JUMP from the interrupt vector table.
Time-critical instructions can be placed directly into the interrupt vector table, followed by a branch to the remaining part of the interrupt service routine. The space between two adjacent vectors can be selected via bitfield VECSC in register CPUCON1.
- Context switching is executed before the intended action takes place (see [Section 7.6](#))
Time-critical instructions can be programmed “non-destructive” and can be executed before switching context for the remaining part of the interrupt service routine.

7.14 Interrupt Nodes

This section describes the available physical interrupt nodes and how some of the nodes are shared among selected peripherals.

7.14.1 Physical Interrupt Nodes

The full set of enabled and used modules integrated in the XC27x8X would require more than the 112 interrupt nodes provided by the C166SV2 interrupt controller. Therefore some of the physically available interrupt nodes are shared between selected modules.

The sources selected by ISSR.ISSx are listed in [Chapter 7.14.2](#).

The following table summarizes the 112 physical interrupt nodes with their related

- trap number
- vector location
- control register name and address
- node sharing information

Table 7-10 XC27x8X Interrupt Nodes

Source of Interrupt or PEC Service Request	Trap Number	Vector ¹⁾ Location	Control Register	Register Address
selected by SCU_ISSR.ISS0	10 _H	xx'0040 _H	CC2_CC16IC	F1C0 _H
selected by SCU_ISSR.ISS1	11 _H	xx'0044 _H	CC2_CC17IC	F1C2 _H
selected by SCU_ISSR.ISS2	12 _H	xx'0048 _H	CC2_CC18IC	F1C4 _H
selected by SCU_ISSR.ISS3	13 _H	xx'004C _H	CC2_CC19IC	F1C6 _H
selected by SCU_ISSR.ISS4	14 _H	xx'0050 _H	CC2_CC20IC	F1C8 _H
selected by SCU_ISSR.ISS5	15 _H	xx'0054 _H	CC2_CC21IC	F1CA _H
selected by SCU_ISSR.ISS6	16 _H	xx'0058 _H	CC2_CC22IC	F1CC _H
selected by SCU_ISSR.ISS7	17 _H	xx'005C _H	CC2_CC23IC	F1CE _H
selected by SCU_ISSR.ISS8	18 _H	xx'0060 _H	CC2_CC24IC	F1D0 _H
selected by SCU_ISSR.ISS9	19 _H	xx'0064 _H	CC2_CC25IC	F1D2 _H
selected by SCU_ISSR.ISS10	1A _H	xx'0068 _H	CC2_CC26IC	F1D4 _H
selected by SCU_ISSR.ISS11	1B _H	xx'006C _H	CC2_CC27IC	F1D6 _H
selected by SCU_ISSR.ISS12	1C _H	xx'0070 _H	CC2_CC28IC	F1D8 _H
selected by SCU_ISSR.ISS13	1D _H	xx'0074 _H	CC2_CC29IC	F1DA _H
selected by SCU_ISSR.ISS14	1E _H	xx'0078 _H	CC2_CC30IC	F1DC _H
selected by SCU_ISSR.ISS15	1F _H	xx'007C _H	CC2_CC31IC	F1DE _H
GPT1 Timer 2	20 _H	xx'0080 _H	GPT12E_T2IC	FF60 _H

Interrupt and Exception Control

Table 7-10 XC27x8X Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Trap Number	Vector¹⁾ Location	Control Register	Register Address
GPT1 Timer 3	21 _H	xx'0084 _H	GPT12E_T3IC	FF62 _H
GPT1 Timer 4	22 _H	xx'0088 _H	GPT12E_T4IC	FF64 _H
GPT2 Timer 5	23 _H	xx'008C _H	GPT12E_T5IC	FF66 _H
GPT2 Timer 6	24 _H	xx'0090 _H	GPT12E_T6IC	FF68 _H
GPT2 CAPREL	25 _H	xx'0094 _H	GPT12E_CRIC	FF6A _H
CAPCOM2 Timer 7	26 _H	xx'0098 _H	CC2_T7IC	FF6C _H
CAPCOM2 Timer 8	27 _H	xx'009C _H	CC2_T8IC	FF6E _H
A/D Converter Request 0	28 _H	xx'00A0 _H	ADC_0IC	FF70 _H
A/D Converter Request 1	29 _H	xx'00A4 _H	ADC_1IC	FF72 _H
A/D Converter Request 2	2A _H	xx'00A8 _H	ADC_2IC	FF74 _H
A/D Converter Request 3	2B _H	xx'00AC _H	ADC_3IC	FF76 _H
A/D Converter Request 4	2C _H	xx'00B0 _H	ADC_4IC	FF78 _H
A/D Converter Request 5	2D _H	xx'00B4 _H	ADC_5IC	FF7A _H
A/D Converter Request 6	2E _H	xx'00B8 _H	ADC_6IC	FF7C _H
A/D Converter Request 7	2F _H	xx'00BC _H	ADC_7IC	FF7E _H
CCU60 Request 0	30 _H	xx'00C0 _H	CCU60_0IC	F160 _H
CCU60 Request 1	31 _H	xx'00C4 _H	CCU60_1IC	F162 _H
CCU60 Request 2	32 _H	xx'00C8 _H	CCU60_2IC	F164 _H
CCU60 Request 3	33 _H	xx'00CC _H	CCU60_3IC	F166 _H
CCU61 Request 0	34 _H	xx'00D0 _H	CCU61_0IC	F168 _H
CCU61 Request 1	35 _H	xx'00D4 _H	CCU61_1IC	F16A _H
CCU61 Request 2	36 _H	xx'00D8 _H	CCU61_2IC	F16C _H
CCU61 Request 3	37 _H	xx'00DC _H	CCU61_3IC	F16E _H
CCU62 Request 0	38 _H	xx'00E0 _H	CCU62_0IC	F170 _H
CCU62 Request 1	39 _H	xx'00E4 _H	CCU62_1IC	F172 _H
CCU62 Request 2	3A _H	xx'00E8 _H	CCU62_2IC	F174 _H
CCU62 Request 3	3B _H	xx'00EC _H	CCU62_3IC	F176 _H
CCU63 Request 0	3C _H	xx'00F0 _H	CCU63_0IC	F178 _H
CCU63 Request 1	3D _H	xx'00F4 _H	CCU63_1IC	F17A _H
CCU63 Request 2	3E _H	xx'00F8 _H	CCU63_2IC	F17C _H

Interrupt and Exception Control

Table 7-10 XC27x8X Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Trap Number	Vector ¹⁾ Location	Control Register	Register Address
CCU63 Request 3	3F _H	xx'00FC _H	CCU63_3IC	F17E _H
CAN0	40 _H	xx'0100 _H	CAN_0IC	F140 _H
CAN1	41 _H	xx'0104 _H	CAN_1IC	F142 _H
CAN2	42 _H	xx'0108 _H	CAN_2IC	F144 _H
CAN3	43 _H	xx'010C _H	CAN_3IC	F146 _H
CAN4	44 _H	xx'0110 _H	CAN_4IC	F148 _H
CAN5	45 _H	xx'0114 _H	CAN_5IC	F14A _H
CAN6	46 _H	xx'0118 _H	CAN_6IC	F14C _H
CAN7	47 _H	xx'011C _H	CAN_7IC	F14E _H
CAN8	48 _H	xx'0120 _H	CAN_8IC	F150 _H
CAN9	49 _H	xx'0124 _H	CAN_9IC	F152 _H
CAN10	4A _H	xx'0128 _H	CAN_10IC	F154 _H
CAN11	4B _H	xx'012C _H	CAN_11IC	F156 _H
CAN12	4C _H	xx'0130 _H	CAN_12IC	F158 _H
CAN13	4D _H	xx'0134 _H	CAN_13IC	F15A _H
CAN14	4E _H	xx'0138 _H	CAN_14IC	F15C _H
CAN15	4F _H	xx'013C _H	CAN_15IC	F15E _H
USIC0 CH0 SR0	50 _H	xx'0140 _H	U0C0_0IC	F120 _H
USIC0 CH0 SR1	51 _H	xx'0144 _H	U0C0_1IC	F122 _H
USIC0 CH0 SR2	52 _H	xx'0148 _H	U0C0_2IC	F124 _H
USIC0 CH1 SR0	53 _H	xx'014C _H	U0C1_0IC	F126 _H
USIC0 CH1 SR1	54 _H	xx'0150 _H	U0C1_1IC	F128 _H
USIC0 CH1 SR2	55 _H	xx'0154 _H	U0C1_2IC	F12A _H
USIC1 CH0 SR0	56 _H	xx'0158 _H	U1C0_0IC	F12C _H
USIC1 CH0 SR1	57 _H	xx'015C _H	U1C0_1IC	F12E _H
USIC1 CH0 SR2	58 _H	xx'0160 _H	U1C0_2IC	F130 _H
USIC1 CH1 SR0	59 _H	xx'0164 _H	U1C1_0IC	F132 _H
USIC1 CH1 SR1	5A _H	xx'0168 _H	U1C1_1IC	F134 _H
USIC1 CH1 SR2	5B _H	xx'016C _H	U1C1_2IC	F136 _H
USIC2 CH0 SR0	5C _H	xx'0170 _H	U2C0_0IC	F138 _H

Interrupt and Exception Control

Table 7-10 XC27x8X Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Trap Number	Vector ¹⁾ Location	Control Register	Register Address
USIC2 CH0 SR1	5D _H	xx'0174 _H	U2C0_1IC	F13A _H
USIC2 CH0 SR2	5E _H	xx'0178 _H	U2C0_2IC	F13C _H
USIC2 CH1 SR0	5F _H	xx'017C _H	U2C1_0IC	F13E _H
USIC2 CH1 SR1	60 _H	xx'0180 _H	U2C1_1IC	F180 _H
USIC2 CH1 SR2	61 _H	xx'0184 _H	U2C1_2IC	F182 _H
USIC3 CH0 SR0	62 _H	xx'0188 _H	U3C0_0IC	F184 _H
USIC3 CH0 SR1	63 _H	xx'018C _H	U3C0_1IC	F186 _H
USIC3 CH0 SR2	64 _H	xx'0190 _H	U3C0_2IC	F188 _H
USIC3 CH1 SR0	65 _H	xx'0194 _H	U3C1_0IC	F18A _H
USIC3 CH1 SR1	66 _H	xx'0198 _H	U3C1_1IC	F18C _H
USIC3 CH1 SR2	67 _H	xx'019C _H	U3C1_2IC	F18E _H
SCU External Request 0	68 _H	xx'01A0 _H	ERU_0IC	F190 _H
SCU External Request 1	69 _H	xx'01A4 _H	ERU_1IC	F192 _H
SCU External Request 2	6A _H	xx'01A8 _H	ERU_2IC	F194 _H
SCU Interrupt 1	6B _H	xx'01AC _H	SCU_1IC	F196 _H
SCU Interrupt 0	6C _H	xx'01B0 _H	SCU_0IC	F198 _H
SCU External Request 3	6D _H	xx'01B4 _H	ERU_3IC	F19A _H
RTC	6E _H	xx'01B8 _H	RTC_IC	F19C _H
End of PEC Subchannel	6F _H	xx'01BC _H	EOPIC	F19E _H
(not connected)	70 _H	xx'01C0 _H	-	F108 _H
(not connected)	71 _H	xx'01C4 _H	-	F10A _H
(not connected)	72 _H	xx'01C8 _H	-	F1A2 _H
(not connected)	73 _H	xx'01CC _H	-	F1A4 _H
(not connected)	74 _H	xx'01D0 _H	-	F1A6 _H
(not connected)	75 _H	xx'01D4 _H	-	FF3E _H
(not connected)	76 _H	xx'01D8 _H	-	FFA0 _H
(not connected)	77 _H	xx'01DC _H	-	FFBE _H
(not connected)	78 _H	xx'01E0 _H	-	FFC0 _H
(not connected)	79 _H	xx'01E4 _H	-	FFC2 _H
USIC4 CH0 SR0	7A _H	xx'01E8 _H	U4C0_0IC	F114 _H

Interrupt and Exception Control

Table 7-10 XC27x8X Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Trap Number	Vector ¹⁾ Location	Control Register	Register Address
USIC4 CH0 SR1	7B _H	xx'01EC _H	U4C0_1IC	F116 _H
USIC4 CH0 SR2	7C _H	xx'01F0 _H	U4C0_2IC	F118 _H
USIC4 CH1 SR0	7D _H	xx'01F4 _H	U4C1_0IC	F11A _H
USIC4 CH1 SR1	7E _H	xx'01F8 _H	U4C1_1IC	F11C _H
USIC4 CH1 SR2	7F _H	xx'01FC _H	U4C1_2IC	F11E _H

1) Register VECSEG defines the segment where the vector table is located to.

Bitfield VECSC in register CPUCON1 defines the distance between two adjacent vectors. This table represents the default setting, with a distance of 4 (two words) between two vectors.

7.14.2 Interrupt Node Sharing

Interrupt source selection is adjustable to the application focus. The concept described in this chapter allows to adjust the focus to be more on control (CAPCOM2) or on communication (USIC) side.

Interrupt node sharing is controlled by SCU register ISSR (see [Section](#)).

Shared Nodes controlled by ISSR

The following figure visualizes the sharing principle controlled by ISSR register. The default interrupt source is CAPCOM2. The alternate source selections are the SCU interrupts 2 and 3 and the SR3 requests of all USIC channels.

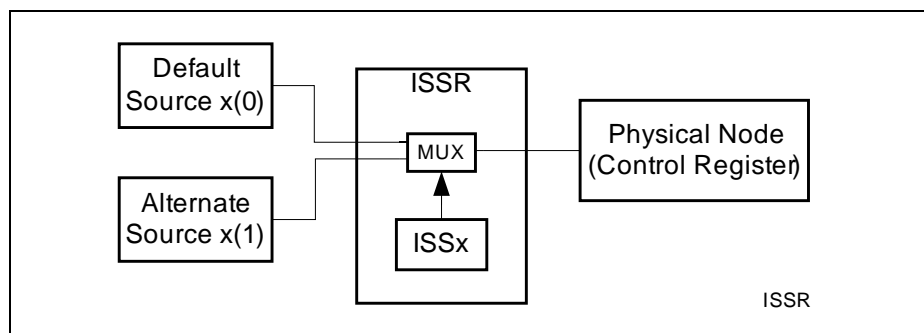


Figure 7-5 Node Sharing Principle controlled by ISSR

The table below lists the possible selections of interrupt request sources to the physical interrupt nodes (Control Register). Selection is controlled through ISSx bits of the ISSR register.

Table 7-11 Nodes Sharing controlled by ISSR

Control Register	Select Bit	Default Source (ISSx=0)	Alternate Source (ISSx=1)
CC2_CC16IC	ISS0	CAPCOM2 Request 16	USIC4 CH0 SR3
CC2_CC17IC	ISS1	CAPCOM2 Request 17	USIC4 CH1 SR3
CC2_CC18IC	ISS2	CAPCOM2 Request 18	USIC3 CH0 SR3
CC2_CC19IC	ISS3	CAPCOM2 Request 19	USIC3 CH1 SR3
CC2_CC20IC	ISS4	CAPCOM2 Request 20	USIC0 CH0 SR3
CC2_CC21IC	ISS5	CAPCOM2 Request 21	USIC0 CH1 SR3
CC2_CC22IC	ISS6	CAPCOM2 Request 22	USIC1 CH0 SR3
CC2_CC23IC	ISS7	CAPCOM2 Request 23	USIC1 CH1 SR3

Interrupt and Exception Control

Table 7-11 Nodes Sharing controlled by ISSR (cont'd)

Control Register	Select Bit	Default Source (ISSx=0)	Alternate Source (ISSx=1)
CC2_CC24IC	ISS8	CAPCOM2 Request 24	(not assigned)
CC2_CC25IC	ISS9	CAPCOM2 Request 25	(not assigned)
CC2_CC26IC	ISS10	CAPCOM2 Request 26	(not assigned)
CC2_CC27IC	ISS11	CAPCOM2 Request 27	(not assigned)
CC2_CC28IC	ISS12	CAPCOM2 Request 28	USIC2 CH0 SR3
CC2_CC29IC	ISS13	CAPCOM2 Request 29	USIC2 CH1 SR3
CC2_CC30IC	ISS14	CAPCOM2 Request 30	SCU Interrupt 2
CC2_CC31IC	ISS15	CAPCOM2 Request 31	SCU Interrupt 3

7.15 Interrupt Source Select Registers

In order to map the interrupt request sources in the complete system to the available interrupt nodes, interrupt nodes are shared between selected modules.

SCU_ISSR

Interrupt Source Select Register

SFR (FF2E_H/97_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ISS 15	ISS 14	ISS 13	ISS 12	ISS 11	ISS 10	ISS 9	ISS 8	ISS 7	ISS 6	ISS 5	ISS 4	ISS 3	ISS 2	ISS 1	ISS 0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ISS0	0	rw	Interrupt Source Select for CC2_CC16IC 0 _B CC2 channel 16 interrupt is selected 1 _B USIC4 channel 0 SR3 is selected
ISS1	1	rw	Interrupt Source Select for CC2_CC17IC 0 _B CC2 channel 17 interrupt is selected 1 _B USIC4 channel 1 SR3 is selected
ISS2	2	rw	Interrupt Source Select for CC2_CC18IC 0 _B CC2 channel 18 interrupt is selected 1 _B USIC3 channel 0 SR3 is selected
ISS3	3	rw	Interrupt Source Select for CC2_CC19IC 0 _B CC2 channel 19 interrupt is selected 1 _B USIC3 channel 1 SR3 is selected
ISS4	4	rw	Interrupt Source Select for CC2_CC20IC 0 _B CC2 channel 20 interrupt is selected 1 _B USIC0 channel 0 SR3 is selected
ISS5	5	rw	Interrupt Source Select for CC2_CC21IC 0 _B CC2 channel 21 interrupt is selected 1 _B USIC0 channel 1 SR3 is selected
ISS6	6	rw	Interrupt Source Select for CC2_CC22IC 0 _B CC2 channel 22 interrupt is selected 1 _B USIC1 channel 0 SR3 is selected
ISS7	7	rw	Interrupt Source Select for CC2_CC23IC 0 _B CC2 channel 23 interrupt is selected 1 _B USIC1 channel 1 SR3 is selected

Interrupt and Exception Control

Field	Bits	Type	Description
ISS8	8	rw	Interrupt Source Select for CC2_CC24IC 0 _B CC2 channel 24 interrupt is selected 1 _B No interrupt source assigned
ISS9	9	rw	Interrupt Source Select for CC2_CC25IC 0 _B CC2 channel 25 interrupt is selected 1 _B No interrupt source assigned
ISS10	10	rw	Interrupt Source Select for CC2_CC26IC 0 _B CC2 channel 26 interrupt is selected 1 _B No interrupt source assigned
ISS11	11	rw	Interrupt Source Select for CC2_CC27IC 0 _B CC2 channel 27 interrupt is selected 1 _B No interrupt source assigned
ISS12	12	rw	Interrupt Source Select for CC2_CC28IC 0 _B CC2 channel 28 interrupt is selected 1 _B USIC2 channel 0 SR3 is selected
ISS13	13	rw	Interrupt Source Select for CC2_CC29IC 0 _B CC2 channel 29 interrupt is selected 1 _B USIC2 channel 1 SR3 is selected
ISS14	14	rw	Interrupt Source Select for CC2_CC30IC 0 _B CC2 channel 30 interrupt is selected 1 _B SCU Interrupt 2 is selected
ISS15	15	rw	Interrupt Source Select for CC2_CC31IC 0 _B CC2 channel 31 interrupt is selected 1 _B SCU Interrupt 3 is selected

7.16 Interrupt and PEC Configuration Registers

The following table lists all registers used to configure the interrupt and PEC behavior of the XC27x8X. Registers are ordered by address. The Interrupt Control registers `xxIC`, assigned to each interrupt request, are listed separately (see [Section 7.14](#)).

Bit addressable SFRs are marked with the letter “b” in column “Name”.

Table 7-12 Register Overview Interrupt and PEC - ordered by address

Name	Physical Address	8-bit Address	Description	Reset Value
FINT0CSP	EC00 _H	--	Fast Interrupt 0 CSP Register	0000 _H
FINT0ADDR	EC02 _H	--	Fast Interrupt 0 Address Register	0000 _H
FINT1CSP	EC04 _H	--	Fast Interrupt 1 CSP Register	0000 _H
FINT1ADDR	EC06 _H	--	Fast Interrupt 1 Address Register	0000 _H
BNKSEL0	EC20 _H	--	Bank Selection Register 0	0000 _H
BNKSEL1	EC22 _H	--	Bank Selection Register 1	0000 _H
BNKSEL2	EC24 _H	--	Bank Selection Register 2	0000 _H
BNKSEL3	EC26 _H	--	Bank Selection Register 3	0000 _H
SRCP0	EC40 _H	--	PEC Channel 0 Source Pointer	0000 _H
DSTP0	EC42 _H	--	PEC Channel 0 Destination Pointer	0000 _H
SRCP1	EC44 _H	--	PEC Channel 1 Source Pointer	0000 _H
DSTP1	EC46 _H	--	PEC Channel 1 Destination Pointer	0000 _H
SRCP2	EC48 _H	--	PEC Channel 2 Source Pointer	0000 _H
DSTP2	EC4A _H	--	PEC Channel 2 Destination Pointer	0000 _H
SRCP3	EC4C _H	--	PEC Channel 3 Source Pointer	0000 _H
DSTP3	EC4E _H	--	PEC Channel 3 Destination Pointer	0000 _H
SRCP4	EC50 _H	--	PEC Channel 4 Source Pointer	0000 _H
DSTP4	EC52 _H	--	PEC Channel 4 Destination Pointer	0000 _H
SRCP5	EC54 _H	--	PEC Channel 5 Source Pointer	0000 _H
DSTP5	EC56 _H	--	PEC Channel 5 Destination Pointer	0000 _H
SRCP6	EC58 _H	--	PEC Channel 6 Source Pointer	0000 _H
DSTP6	EC5A _H	--	PEC Channel 6 Destination Pointer	0000 _H
SRCP7	EC5C _H	--	PEC Channel 7 Source Pointer	0000 _H
DSTP7	EC5E _H	--	PEC Channel 7 Destination Pointer	0000 _H

Interrupt and Exception Control

Table 7-12 Register Overview Interrupt and PEC - ordered by address (cont'd)

Name	Physical Address	8-bit Address	Description	Reset Value
SRCP8	EC60 _H	--	PEC Channel 8 Source Pointer	0000 _H
DSTP8	EC62 _H	--	PEC Channel 8 Destination Pointer	0000 _H
SRCP9	EC64 _H	--	PEC Channel 9 Source Pointer	0000 _H
DSTP9	EC66 _H	--	PEC Channel 9 Destination Pointer	0000 _H
SRCP10	EC68 _H	--	PEC Channel 10 Source Pointer	0000 _H
DSTP10	EC6A _H	--	PEC Channel 10 Destination Pointer	0000 _H
SRCP11	EC6C _H	--	PEC Channel 11 Source Pointer	0000 _H
DSTP11	EC6E _H	--	PEC Channel 11 Destination Pointer	0000 _H
SRCP12	EC70 _H	--	PEC Channel 12 Source Pointer	0000 _H
DSTP12	EC72 _H	--	PEC Channel 12 Destination Pointer	0000 _H
SRCP13	EC74 _H	--	PEC Channel 13 Source Pointer	0000 _H
DSTP13	EC76 _H	--	PEC Channel 13 Destination Pointer	0000 _H
SRCP14	EC78 _H	--	PEC Channel 14 Source Pointer	0000 _H
DSTP14	EC7A _H	--	PEC Channel 14 Destination Pointer	0000 _H
SRCP15	EC7C _H	--	PEC Channel 15 Source Pointer	0000 _H
DSTP15	EC7E _H	--	PEC Channel 15 Destination Pointer	0000 _H
PECSEG0	EC80 _H	--	PEC Pointer 0 Segment Address	0000 _H
PECSEG1	EC82 _H	--	PEC Pointer 1 Segment Address	0000 _H
PECSEG2	EC84 _H	--	PEC Pointer 2 Segment Address	0000 _H
PECSEG3	EC86 _H	--	PEC Pointer 3 Segment Address	0000 _H
PECSEG4	EC88 _H	--	PEC Pointer 4 Segment Address	0000 _H
PECSEG5	EC8A _H	--	PEC Pointer 5 Segment Address	0000 _H
PECSEG6	EC8C _H	--	PEC Pointer 6 Segment Address	0000 _H
PECSEG7	EC8E _H	--	PEC Pointer 7 Segment Address	0000 _H
PECSEG8	EC90 _H	--	PEC Pointer 8 Segment Address	0000 _H
PECSEG9	EC92 _H	--	PEC Pointer 9 Segment Address	0000 _H
PECSEG10	EC94 _H	--	PEC Pointer 10 Segment Address	0000 _H
PECSEG11	EC96 _H	--	PEC Pointer 11 Segment Address	0000 _H
PECSEG12	EC98 _H	--	PEC Pointer 12 Segment Address	0000 _H
PECSEG13	EC9A _H	--	PEC Pointer 13 Segment Address	0000 _H

Interrupt and Exception Control

Table 7-12 Register Overview Interrupt and PEC - ordered by address (cont'd)

Name	Physical Address	8-bit Address	Description	Reset Value
PECSEG14	EC9C _H	--	PEC Pointer 14 Segment Address	0000 _H
PECSEG15	EC9E _H	--	PEC Pointer 15 Segment Address	0000 _H
PECISNC b	FFD8 _H	EC _H	PEC Interrupt Subnode Control	0000 _H
PECC0	FEC0 _H	60 _H	PEC Channel 0 Control Register	0000 _H
PECC1	FEC2 _H	61 _H	PEC Channel 1 Control Register	0000 _H
PECC2	FEC4 _H	62 _H	PEC Channel 2 Control Register	0000 _H
PECC3	FEC6 _H	63 _H	PEC Channel 3 Control Register	0000 _H
PECC4	FEC8 _H	64 _H	PEC Channel 4 Control Register	0000 _H
PECC5	FECA _H	65 _H	PEC Channel 5 Control Register	0000 _H
PECC6	FECC _H	66 _H	PEC Channel 6 Control Register	0000 _H
PECC7	FECE _H	67 _H	PEC Channel 7 Control Register	0000 _H
PECC8	ECA0 _H	--	PEC Channel 8 Control Register	0000 _H
PECC9	ECA2 _H	--	PEC Channel 9 Control Register	0000 _H
PECC10	ECA4 _H	--	PEC Channel 10 Control Register	0000 _H
PECC11	ECA6 _H	--	PEC Channel 11 Control Register	0000 _H
PECC12	ECA8 _H	--	PEC Channel 12 Control Register	0000 _H
PECC13	ECAA _H	--	PEC Channel 13 Control Register	0000 _H
PECC14	ECAC _H	--	PEC Channel 14 Control Register	0000 _H
PECC15	ECAE _H	--	PEC Channel 15 Control Register	0000 _H

8 Memory Protection Unit (MPU)

The Memory Protection Unit (MPU) provides the hardware mechanisms needed for implementing memory protection. The MPU allows detection of unauthorized accesses (read, write or instruction fetch) in user-defined memory ranges. It offers protection for the complete address space, including the peripheral area.

The MPU can be used to support the encapsulation of different applications or software components running on the processor. This encapsulation provides the means to ensure integrity and fault isolation capabilities in today's complex systems relying on multiple-sources software.

8.1 Functional Overview

Different protection levels are usually needed to support a programming system where for example an operating system or software kernel runs and controls different application and low level drivers parts. One level can be associated to the operating system and for the other tasks that need protection against each other or against the operating system, other levels can be used. For every protection level different address ranges with different access permissions for instructions and/or data can be defined. When a piece of code is executed and the memory protection is enabled, the permissions associated to its protection level are selected and every time a memory access is performed it will be checked if the access is outside of the specified ranges or violates the access permissions. In this case the access may not be performed but marked as invalid and a protection trap routine can be executed.

The basic MPU functionality is shown in [Figure 8-1](#).

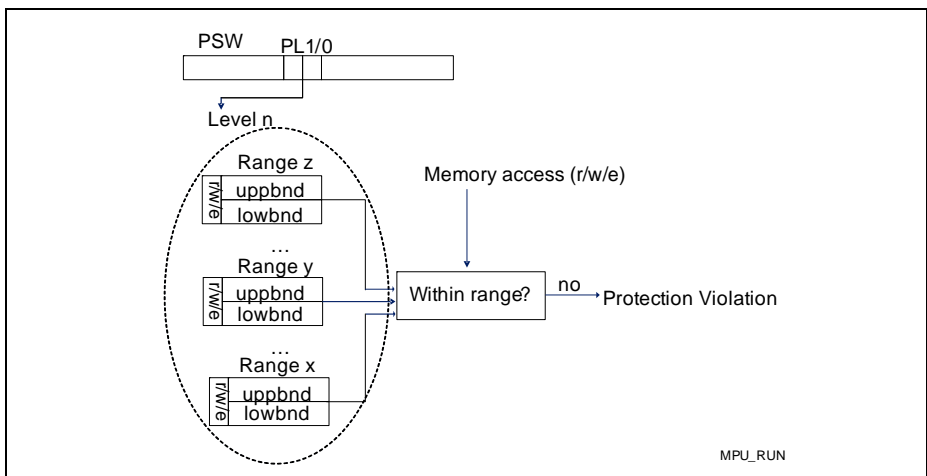


Figure 8-1 MPU Operation

Memory Protection Unit (MPU)

Four Protection Levels can coexist during run time in this architecture. Two bits in the Processor Status Word (PSW) are used to select which protection level is active at a given time. If an application requires more than 4 protection levels, a re-mapping of all the levels to the 4 possible values has to be performed and during run time re-programming of the protection register sets when switching levels is needed.

A protection register set is associated to every protection level, every set contains all the address ranges and the access permissions associated to the corresponding protection level. Every protection register set can contain a programmable number of range registers. All together, a maximum of 12 ranges is supported. Associated to every code or data range, a protection mode register defines the permissions for this range. Refer to the next chapters for a detailed explanation of the MPU registers needed for the protection system and its usage.

8.2 Memory Protection Registers

A protection register set consists of a variable number of Protection Range register pairs (PRUx/PRLx) and the corresponding number of Protection Mode registers (PMx). The PMx registers are located in the SFRs area and are accessed through the Peripheral Data Bus -PD-Bus-. The PRUx/PRLx registers are not memory mapped, their access mechanism is supported through the memory mapped registers Protection Range Address register (PRA) and Protection Range Data register (PRD).

Table 8-1 Registers Address Space

Module	Base Address	End Address	Note
MPU	0000 _H	0FFF _H	

Table 8-2 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
PRUx (x =0-11)	Protection Range Register x Upper Bound	none _H	8-4
PRLx (x =0-11)	Protection Range Register x Lower Bound	none _H	8-4
PM5	Protection Mode Register 5	FFD2 _H	8-7
PM4	Protection Mode Register 4	FFD0 _H	8-7
PM3	Protection Mode Register 3	FFCE _H	8-7
PM2	Protection Mode Register 2	FFCC _H	8-7
PM1	Protection Mode Register 1	FFCA _H	8-7
PM0	Protection Mode Register 0	FFC8 _H	8-7
PRD	Protection Range Data	FFC6 _H	8-8
PRA	Protection Range Address	FFC4 _H	8-9

8.2.1 Protection Range Registers

The PRUx/PRLx pairs are 16-bits registers and specify the upper 16 bits of the physical addresses, upper and lower bound, for data and/or code for all the allowed ranges (12 is the maximum supported). Only these upper 16 bits of the physical addresses are considered in the address comparisons, as a consequence, the minimum granularity of the ranges is 256 bytes and all the ranges are aligned to this size.

The PRUx and PRLx registers specify respectively the Upper and Lower addresses of a Range. If due to a programming error PRLx specifies a value bigger than PRUx, the corresponding range will not specify a correct address range, and as a consequence the corresponding range is useless (i.e. ignored). Note that due to the 256 byte range

Memory Protection Unit (MPU)

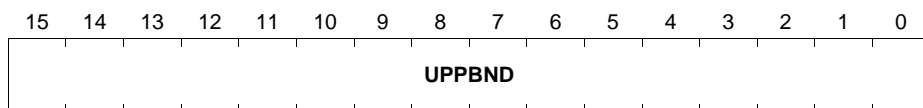
granularity, to program a range of this smallest size, both upper and lower range need to be program with the same value, i.e. the 16-bits base address of the range.

For programming a protection range in the PRUx/PRLx registers, it has to be selected first which range is going to be written by programming the address into PRA, then the data write operation can be performed by writing the data into PRD. In a similar way, a read operation has to be performed by selecting first which range in going to be read (by programming the address into PRA) and then the read operation can be performed by reading PRD. Programming a PRUx/PRLx register requires then two write operations. Similarly, reading a PRUx/PRLx register requires also two operations (one write and one read). For continuous accesses and when using the auto increment feature only one initialization into PRA is needed, afterwards only the PRD register needs to be written/read every time. Registers PRD and PRA are described in [Chapter 8.2.3](#) and [Chapter 8.2.4](#) respectively.

PRUx (x =0-11)

Protection Range Register x Upper Bound

Reset Value: 0000_H

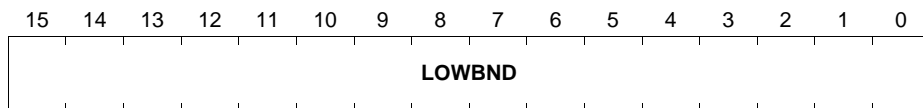


Field	Bits	Type	Description
UPPBND	[15:0]	rw	Upper Boundary Address (upper 16 bits)

PRLx (x =0-11)

Protection Range Register x Lower Bound

Reset Value: 0000_H



Field	Bits	Type	Description
LOWBND	[15:0]	rw	Lower Boundary Address (upper 16 bits)

8.2.2 Protection Mode Registers

All the control information associated to every address range is contained in the Protection Mode registers. Access permissions (execute, read and/or write) are defined here and also the range-to-level mapping. Every range can be individually enabled to be used for any protection level, even can be used for more than one level (but with the same access permissions). Also the field used to enable the protection system is implemented in one of the protection mode registers.

Note that no hardware mechanism is implemented to flush the pipeline upon a modification of these registers. This is usually not a problem because a (re-)programming of the MPU configuration registers should be anyhow performed having the protection disabled. Also the configuration affecting a particular protection level will be usually (re-)programmed from another level meaning that even at the point when protection is enabled the software currently running will not be affected by the configuration change (the configuration change is usually seen once the protection level is changed according to the procedure described in [Chapter 8.4.2](#)). For special cases where the change will and needs to be immediately seen, the software has to take care that the write is effective before executing the next affected instruction (by reading for example the latest written register).

The bit fields of the PMx registers in the description below use generic Range names (A, B), their mapping to the physical ranges is given after the PMx register name where they belong to. Given a Protection Mode register x, the range named A is addressing the physical range $2 \cdot x$ and range named B the range $2 \cdot x + 1$.

The PMx registers are EINIT protected.

PM0

Protection Mode Register 0 **SFR (FFC8_H)** **Reset Value: 0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L3E B	L2E B	L1E B	L0E B	WEB	REB	XEB	0	L3E A	L2E A	L1E A	L0E A	WEA	REA	XEA	PRO TEN
rw	rw	rw	rw	rw	rw	rw	r	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
PROTEN	0	rw	Protection Enable bit This bit enables the Protection mechanism 0 _B Protection not enabled 1 _B Protection enabled

Memory Protection Unit (MPU)

Field	Bits	Type	Description
XEA, XEB	1, 9	rw	Execute Enable 0 _B Instruction fetch accesses to associated address range (A, B) not permitted 1 _B Instruction fetch accesses to associated address range (A, B) permitted
REA, REB	2, 10	rw	Read Enable 0 _B Data read accesses to associated address range (A, B) not permitted 1 _B Data read accesses to associated address range (A, B) permitted
WEA, WEB	3, 11	rw	Write Enable 0 _B Data write accesses to associated address range (A, B) not permitted 1 _B Data write accesses to associated address range (A, B) permitted
L0EA, L0EB	4, 12	rw	Level 0 Enable 0 _B Range (A, B) not enabled for Protection Level 0 1 _B Range (A, B) enabled for Protection Level 0
L1EA, L1EB	5, 13	rw	Level 1 Enable 0 _B Range (A, B) not enabled for Protection Level 1 1 _B Range (A, B) enabled for Protection Level 1
L2EA, L2EB	6, 14	rw	Level 2 Enable 0 _B Range (A, B) not enabled for Protection Level 2 1 _B Range (A, B) enabled for Protection Level 2
L3EA, L3EB	7, 15	rw	Level 3 Enable 0 _B Range (A, B) not enabled for Protection Level 3 1 _B Range (A, B) enabled for Protection Level 3
0	8	r	Reserved field

The field PROTEN exists only in the Protection Mode Register 0.

Memory Protection Unit (MPU)

PMx (x =1-5)

Protection Mode Register x

SFR (FFC8_H+2*x)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L3E B	L2E B	L1E B	L0E B	WEB	REB	XEB	0	L3E A	L2E A	L1E A	L0E A	WEA	REA	XEA	0
rw	rw	rw	rw	rw	rw	rw	r	rw	rw	rw	rw	rw	rw	rw	r

Field	Bits	Type	Description
0	0	r	Reserved field
XEA, XEB	1, 9	rw	Execute Enable 0 _B Instruction fetch accesses to associated address range (A, B) not permitted 1 _B Instruction fetch accesses to associated address range (A, B) permitted
REA, REB	2, 10	rw	Read Enable 0 _B Data read accesses to associated address range (A, B) not permitted 1 _B Data read accesses to associated address range (A, B) permitted
WEA, WEB	3, 11	rw	Write Enable 0 _B Data write accesses to associated address range (A, B) not permitted 1 _B Data write accesses to associated address range (A, B) permitted
L0EA, L0EB	4, 12	rw	Level 0 Enable 0 _B Range (A, B) not enabled for Protection Level 0 1 _B Range (A, B) enabled for Protection Level 0
L1EA, L1EB	5, 13	rw	Level 1 Enable 0 _B Range (A, B) not enabled for Protection Level 1 1 _B Range (A, B) enabled for Protection Level 1
L2EA, L2EB	6, 14	rw	Level 2 Enable 0 _B Range (A, B) not enabled for Protection Level 2 1 _B Range (A, B) enabled for Protection Level 2

Field	Bits	Type	Description
L3EA, L3EB	7, 15	rw	Level 3 Enable 0 _B Range (A, B) not enabled for Protection Level 3 1 _B Range (A, B) enabled for Protection Level 3
0	8	r	Reserved field

8.2.3 Protection Range Data Register

The Protection Range Data register contains the 16 bits data value needed to program the content of the Protection Range Registers. It also contains the data read during the last read access on the Protection Range Registers. A write into PRD triggers immediately a write into the corresponding PRUx/PRLx register (the one that is currently selected by the write pointer -in PRA register-). Also a read into PRD delivers the corresponding PRUx/PRLx data immediately (the one that is currently selected by the read pointer -in PRA register-).

The PRD register is EINIT protected.

PRD

Protection Range Data

SFR (FFC6_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA															
rwh															

Field	Bits	Type	Description
DATA	[15:0]	rwh	Data Value for/from PRUx/PRLx

8.2.4 Protection Range Address Register

The Protection Range Address register contains two access pointers, one used for write operations and the other for read operations. With every 5-bit pointer it is possible to select a PRUx/PRLx register from a set of 24 register (the 24 PRUx/PRLx registers needed to implement 12 protection ranges).

An auto increment capability can be enabled for the access pointers (controlled by WMOD and RMOD fields), after every write or read into/from PRD the write or read pointers are incremented respectively. This feature enables a faster programming of the protection range registers. When the auto increment mode is active, the access pointers automatically do a wrap around (i.e. initialized to 0) after reaching its maximum value.

Memory Protection Unit (MPU)

The occurrence of a wrap around is shown in the status bits WWA or RWA. The software can then check if this situation has happened taking the corresponding action and resetting the corresponding flag.

Special care has to be taken when programming the PRA register in order not to modify one of the pointers unintentionally. It is recommended to use bit instructions for that (bit field instructions for example). Also when using the auto increment feature and during debugging it has to be considered that a debugger access can also modify the pointer values, the debugger software should then take care of restoring the original status of this register.

The PRA register is EINIT protected.

PRA

Protection Range Address				SFR (FFC4 _H)				Reset Value: 0000 _H							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RMO D	RWA	0	RPTR				WM OD	WW A	0	WPTR					
rw	rwh	r	rwh				rw	rwh	r	rwh					

Field	Bits	Type	Description
WPTR	[4:0]	rwh	Write Pointer Selects the Protection Range Register to be written 00000 _B Selects PRL0 00001 _B Selects PRU0 00010 _B Selects PRL1 00011 _B Selects PRU1 00100 _B Selects PRL2 00101 _B Selects PRU2 ... 11110 _B Selects PRL15 11111 _B Selects PRU15
0	5	r	Reserved field
WWA	6	rwh	Write Wrap Around Status 0 _B No WPTR Wrap Around occurred on last Write 1 _B A WPTR Wrap Around occurred on last Write Bit to be cleared by SW
WMOD	7	rw	Auto increment Write Mode 0 _B No increment WPTR on every Write 1 _B Auto increment WPTR on every Write

Field	Bits	Type	Description
RPTR	[12:8]	rwh	Read Pointer Selects the Protection Range Register to be read 00000 _B Selects PRL0 00001 _B Selects PRU0 00010 _B Selects PRL1 00011 _B Selects PRU1 00100 _B Selects PRL2 00101 _B Selects PRU2 ... 11110 _B Selects PRL15 11111 _B Selects PRU15
0	13	r	Reserved field
RWA	14	rwh	Read Wrap Around Status 0 _B No RPTR Wrap Around occurred on last Read 1 _B A RPTR Wrap Around occurred on last Read Bit to be cleared by SW
RMOD	15	rw	Auto increment Read Mode 0 _B No increment RPTR on every Read 1 _B Auto increment RPTR on every Read

8.3 Functional Description

8.3.1 Enabling Protection

Protection has to be globally enabled per software, bit PM0.PROTEN implements this functionality, refer to chapter [Chapter 8.2.2](#).

8.3.2 Protection Levels

The bits PSW.PL1/0 select the current protection level, i.e the protection register set currently active. The decoding of PL1/0 is as follows:

Table 8-3 Decoding of Protection Level

PL1	PL0	Protection Level
0	0	Protection Level 0
0	1	Protection Level 1
1	0	Protection Level 2
1	1	Protection Level 3

Memory Protection Unit (MPU)

PL1 and PL0 bits are mapped into PSW.10 and PSW.5 bits respectively. Note that due to the shared functionality implemented on the bit PSW.10, a write on this bit will be interpreted as a write on the PSW.PL1 only when the MPU is itself enabled (PM0.PROTEN is 1). When the MPU is not enabled a write on this bit will be interpreted as a write on the HLDEN flag. For consistency, the flag PSW.PL0 is handled in a similar way, a write on PSW.PL0 is only effective when the MPU is enabled.

8.3.2.1 Protection Level 0

For the protection mechanism to work properly, the MPU has to be operated under a kind of privileged mode, programming and changing the protection information should only be allowed during this mode. Even if the C166 family architecture does not support directly this operation mode (only the one associated to the initialization phase ended by the EINIT execution), the privileged mode can be defined in this context as the mode entered when the processor runs with protection Level 0. This is the level entered after reset and the level automatically entered after an interrupt/trap is taken. Level 0 should be then the level used by the operating system, software kernel or the software components needing access to the whole system resources (specially to system control registers and peripheral area).

But note that defining and programming address ranges and permissions is still needed for Level 0 (even if it is the whole space). Per default (i.e. after reset), no access in any address range is allowed, also not for this level.

Note: The need to program Level 0 allows in special occasions to give restricted access also to this level. Restriction sometimes needed to probe reliability of the software running under this level.

8.3.3 Intersecting Memory Ranges

The permission to access a memory location is the OR of the memory range permissions. When two or more ranges intersect, the intersecting region has the permission of the most permissive range.

8.3.4 Protection of the MPU registers

As mentioned in [Chapter 8.3.2.1](#), the MPU registers need to be protected. A protection mechanism comes automatically with the use of the MPU and the fact that the whole address space, including SFRs, is under control of the MPU, see also [Chapter 8.3.5](#). Once protection is enabled, changing protection information can then only be performed from a protection level which has access to the corresponding SFR area (i.e. to the protection registers).

In addition to this inherited protection mechanism, the protection control registers are also EINIT protected. The EINIT protection creates some overhead during dynamic re-programming, however it adds an additional protection level that may be needed in case

different software component need to be executed at the same protection level (the one having access to these control registers -usually level 0-).

8.3.5 Accessing SFRs and GPRs

Once the protection system is activated, a task is not free anymore to access per software any special function register (SFR) unless this is explicitly covered by the address ranges and permissions assigned to this task. This applies to the internal IO area (SFR, ESFR, XSFR) and also to the external IO area (on chip LxBus peripherals or external peripherals). Since the minimum granularity of the address ranges is 256 bytes, the IO space is partitioned into blocks. A task will have access either to one of these blocks with its full set of registers or to none. For example the SFR/ESFR area (1 Kbyte), is divided into four blocks (F000h...F0FFh, F100h...F1FFh, FE00h...FEFFh, FF00h...FFFFh). For the XSFRs area, 4 Kbyte, the space is divided in 16 blocks.

CSFRs are also handled by the protection scheme, but exceptions are required for those CSFRs that are user registers. CSFR that are kept under the protection scheme are:

- PSW (partly), CPUCON1/2, CP, CSP, SP, SPSEG, STKUN, STKOV, TFR, VECSEG.

The USR0/1 bits of PSW, that are user bits, are excluded from the protection scheme. Also the PSW condition flags are excluded. Instructions like JBC/JNBS on the PSW conditions flags can then still be used in user mode. Read accesses to all the PSW fields are allowed.

CSFR that are excluded from the protection mechanism are:

- DPP0/1/2/3, MDL, MDH, MSW, MDC, MAH, MAL, MRW, MCW, QR0/1, QX0/1, IDX0/1, ZEROS, ONES, CPUID.

The DPP registers are handled as user registers to support its re-programming during run time (practice needed for code optimization purposes). When used in this way, it will be responsibility of the software to ensure their right handling, for example saving and restoring them in task switches. CPUID is not strictly a user register, however it is not required to define it as protected since it is anyhow not writable.

GPRs are excluded from the memory protection mechanism. Protection on the DPRAM is however guaranteed since the CP itself is protected. Similarly, GPRs mapped into the Local Register Banks are excluded from the protection mechanism.

8.3.6 Interrupts and PECs Handling

Any interrupt taken by the CPU will switch automatically the protection level to 0. This is valid for peripheral interrupts, debugger interrupts, hardware and software traps. As a consequence Interrupt Service Routines (ISRs) are always started with protection level 0, having usually access to all the system resources. The ISR itself can afterwards reduce the protection level and execute user code with protection restrictions.

Interrupt requests can be also serviced through PEC transfers, that is, fast data transfers between two memory locations. PEC transfers will be executed by the CPU without protection. Protection can still be ensured through the programming of the PEC control registers that should be only performed under the right protection level, usually in privileged mode (i.e. protection level 0). At the configuration time the software should then check for the correctness of the PEC source and destination pointers (according to the permissions allowed) and the PEC control register. Special care has to be taken when using continuous mode, in this case the software can not take care at the configuration time if the PEC will not violate an area in the future. Additional run time checks may be needed to support this mode (executed by the privileged software) or this mode will have to be avoided.

8.3.7 Special handling of RETI instruction

The PSW and specially the Protection Level selection flags (PSW.PLO/1) are handled under the protection scheme: explicit writes on the PSW are detected by the hardware and checked if they are triggered under the right protection level. In case the access is not allowed, a trap will be generated and the modification of the PSW will be avoided by the protection logic.

But the PSW can also be modified implicitly by the hardware and this hardware update can hardly be managed by the protection logic. Hardware updates on the PSW.PLO/1 field are triggered by the execution of a RETI instruction. These PSW hardware updates are in principle not critical as long as the PSW (and PSW.PLO/1) value that is taken from the Stack has not been manipulated by any user code. But since there is no possibility to prohibit user code from this possible manipulations (user code may make use of local stacks with write access to it) the only work around is to prohibit un-trusted user code from using the RETI instruction. RETI will be then specially handled as a kind of protected instruction that can only be executed when the protection level 0. This handling is consistent with the fact that interrupts are handled under protection level 0, returning from interrupts should then also be performed under the same level.

8.3.8 Context Switch operations

The Context Switch mechanism is executed in the core with the help of internal instructions that are auto-injected in the pipeline. Usually auto-injected instructions should run with the same protection level as the instruction causing the auto injection. However, due to the fact that the context switch is an interruptible operation and its completion may be delayed in certain situations, these context switch auto injected instructions have to be executed without considering protection. That means, while they are executed, the protection checks are not performed and/or are ignored. As a consequence only the CP update operation, that is not performed by the auto-injected instruction but by the context switch instruction itself, is performed under the protection scheme. The saving procedure of registers into DPRAM or the read of GPRs from

Memory Protection Unit (MPU)

DPRAM is not performed under the protection scheme. DPRAM protection in this case will have to be ensured, in case it is needed, by the software, the software can check if the region addressed by the values programmed into CP are allowed.

8.3.9 Debugger Access Permissions

The debugger must be able to access all the memory space even if memory protection is active, this includes also the IO space (i.e. SFRs). The OCDS/Cerberus implements basically 2 mechanisms for accessing the system resources:

- triggering the CPU to execute a Monitor Routine that contains the code to access the resources (Call a Monitor)
- Injecting any instruction that can by itself access any resource

When using the first mechanism, that is started by the injection of an ITRAP instruction, the debugger will automatically run in privileged mode, i.e. with protection level 0. As defined in [Chapter 8.3.2.1](#), this is the level automatically entered after an interrupt (in this case after the injection of the debug TRAP instruction).

When using the second mechanism (also if the CPU is halted) the injected instruction will run without protection. The CPU keeps track of the fact that an instruction was injected by the Debugger and disables the protection check for that instruction.

With respect to accessing OCDS/Cerberus/MCDS SFRs by the debugger it just needs to be ensured that the debug monitor (used to program the debug logic) can access these registers with minimum overhead and without any impact on the user code. Since the debug monitor routine will always be executed with protection level 0, it is expected that all the memory space is then allowed. Also accessing these registers via injecting instructions can be performed without restrictions as explained above.

8.3.10 Invalid Access Traps

If an access is performed in a protected area an invalid access trap will be generated. Three traps are defined for this purpose:

MPR Memory Protection, Read

MPW Memory Protection, Write

MPX Memory Protection, Execute

They are defined as Class B traps. They are mapped to TFR.10,9,8 respectively (MPR is TFR.10, MPW is TFR.9 and MPX is TFR.8). Refer to the Hardware Traps description chapter for the complete description of the TFR register.

Note that no trap must be performed on accesses that are performed speculatively, this is why these traps can just be generated when it is known that the instruction is not cancelled anymore (this is, when the instruction goes into the Execute stage).

Memory Protection Unit (MPU)

The already existing trap PRTFLT Protection Fault Trap is also used to indicate the execution of a RETI instruction from a protection level different to 0. Even when RETI causes a protection fault trap, it is normally executed.

8.3.10.1 Cancelling operations

Instructions causing a protection violation will be detected by the MPU but its full execution can not be suppressed, only the writes operations causing a protection fault or derived from an instruction causing a protection fault will be cancelled. Read operations can not be cancelled since they are triggered very soon in the pipeline (sometimes speculatively), however, the read data will not be written by the corresponding instruction in any memory mapped address.

There are some exceptions to the above general rule of cancelling writes operations, in particular, for instructions performing 2 write operations sometimes the first write can not be cancelled. These are the concrete cases:

- SCXT instruction. The write into the Stack can not be avoided when a Read protection violation on the mem operand is detected (for SCXT reg, mem) or a Write protection violation on the reg operand.
- CALLS, PCALL instruction. The first write into the Stack (CSP, or reg in case of PCALL) can not be avoided when a Write protection violation on the second Stack address is detected (where the IP should be pushed). This situation assumes that the Stack has grown over the limit of an allowed area right while executing this instruction (first stack push in an allowed area, second stack push in a non-allowed area).

As a consequence of the fact that Read operations can not be cancelled, destructive reads on the IO space can be still performed even if the MPU detects a protection violation.

As a consequence of the fact that Execute operations can not be cancelled, system instructions and their corresponding actions may be still executed even if they trigger an Execute protection violation. For example an IDLE instruction may still put the CPU in idle mode before the corresponding hardware trap routine can be executed (once the idle mode is left).

8.4 Initializing and using the MPU**8.4.1 Installing Protection**

This chapter describes briefly the SW sequences needed for initializing and using the protection system. It also analyses the overhead created (real time performance). The implementation with 12 ranges is analyzed.

Memory Protection Unit (MPU)

The initialization sequence that can be used for installing protection is:

- Disable Protection in case it is not (after reset protection is disabled), 1 write into PM0.
- Program the Range Registers, 1 PRA write, 24 writes into PRD (absolute maximum value, assumes that all ranges are used).
- Program Protection Mode Registers, 6 PMx writes.
- Enable protection, 1 write into PM0. This last write can be performed together with the write into the PM0 above, but in this case care should be taken to write this register at the end.

When the applications or software components using different protection levels can exactly be mapped to the protection sets implemented, this code sequence would set up the system and no additional overhead when using the MPU would exist during run time. After the initialization phase, whenever a change in the protection level is needed, the corresponding protection set has to be selected (changing PSW.PL). This is the only additional operation during run time.

This initialization, and in general any change in the protection registers, should be performed always having the protection disabled and usually will be executed from protection level 0. Note that in cases where the protection configuration and its activation needs to be immediately seen, the software has to take care that the latest write activating the protection is effective before executing the next affected instruction (by reading for example the latest written register). This is because as explained in [Chapter 8.2.2](#), there is no hardware mechanism to flush the pipeline when the protection is activated.

In case the protection needs can not be mapped into the implemented protection sets, some re-programming during run time is needed. The worst case scenario is that the ranges have to be re-programmed, then a sequence similar to the one during the initialization is needed. However it may be that only some already defined Ranges needs to be activated/deactivated, in this case only the Protection Mode Registers will need to be re-programmed. This assumes that at every moment it is known which ranges are used, so the PSW.PL1/0 has to be read before deciding what to change. An additional overhead during reprogramming is coming from the EINIT protection. After EINIT execution, reprogramming of the PMU registers is only allowed by releasing temporarily this protection by going to an unprotected mode (a command sequence of 4 write instructions with the use of a password is needed for that). After the re-programming the EINIT-protection has to be of course restored (again a command sequence of 4 write instructions). Note that reprogramming of protection registers that are currently not active (i.e. selected through PSW.PL) and do not become active through the reprogramming, is still possible without having to disable protection.

8.4.2 Changing Protection Level

Special care has to be taken when changing the protection level by writing explicitly into PSW. This is because any write into PSW takes effect immediately. If the privileged code handling protection would write into the PSW before performing a code/task switch, the level of the privileged code would be itself changed and eventually the code/task switch (function call for example) couldn't be performed. For avoiding this immediate effect when writing into the PSW some tricks have to be used: stack manipulation and calling functions using the RETI/RETP instructions. The value of the new PSW with the new protection level has to be then stored in the stack, instead of writing the PSW explicitly. The RET instruction will then update the PSW associated to the new task with the correct protection level and at the right time.

8.4.3 Executing privileged code from non-privileged one

It is possible for a non-privileged (un-trusted) software to invoke a privileged software component (trusted). The non-privileged part has to give control to a privileged part, this can be performed by executing a software TRAP instruction. Automatically this instruction will change the protection level to 0. This mechanism allows for example invoking low level drivers from an application software and also returning from the user part of an ISR to the ISR itself, i.e. to the part handle by the OS or software kernel.

8.4.4 Fast task switches

Any task switch that is not controlled by the OS or software kernel will be handled as a trusted task with respect to the software that is invoking it. This is because if the switch is not performed under a software running with enough protection level (usually level 0), there is no possibility to change the protection level explicitly for this task.

8.4.5 Register Bank Selection

Since PSW.BANK field is now handled within the protection scheme, the register bank selection (global or local 1/2) will have to be settled by the software running with enough access permissions, i.e. enough protection level (usually level 0). The bank selection should then be done in the part of the ISR running on level 0 (starting level of all ISRs).

8.4.6 Debugger Use Cases

This chapter documents how to debug the system when memory protection is in use.

The following 4 use cases are identified:

- user wants to find the reason for a MPU trap
- user wants to debug the MPU trap routine
- user doesn't want to debug, he just wants to poll a variable with Cerberus
- user wants to debug without any irregular influence from the protection system

Memory Protection Unit (MPU)

For the first use case, the standard debugging resources (OCDS) can be used for setting an IP breakpoint on the ISR/s handling the trap. Once there, it will be known which access type causes the trap, either implicitly because there are different trap routines depending on the exception type or explicitly by reading the TFR flags. Also the protection level causing the violation can be obtained by reading the stacked PSW. With respect to the IP causing the trap, there is no direct access to it but to the linear following one, that is also stored in the stack.

The second use case, i.e. the debugging of the MPU trap routine, can be done similarly to the debugging of any trap routine and will be started probably also by setting an IP breakpoint on the corresponding ISR.

With respect the third use case, the variable polling action can be performed at any time independently of if the MPU is enabled or not. The debugger has always access to all the system resources even if the MPU is enabled.

The fourth use case, i.e. debugging without influence from the PMU, can be covered by disabling explicitly the MPU (PM0.PROTEN) via the debugger. Since the debugger does not know when the application will enable the MPU after the reset of the system, the debugger will have to monitor the status of the MPU (PMU0.PROTEN) and re-disable it once enabled. This use case is however rather strange because debugging is intended to be done with the real system behavior, if an application causes a MPU exception, this should also be seen during debugging.

9 System Control Unit (SCU)

The System Control Unit (SCU) of the XC27x8X handles all system control tasks besides the debug related tasks which are controlled by the OCDS/Cerberus. All functions described in this chapter are tightly coupled, thus, they are conveniently handled by one unit, the SCU.

The SCU contains the following functional sub-blocks:

- Clock Generation (see [Chapter 9.1](#))
- System Timer (see [Chapter 9.2](#))
- Wake-up Timer (see [Chapter 9.3](#))
- Reset Operation (see [Chapter 9.4](#))
- External Service Requests (see [Chapter 9.5](#))
- Power Supply and Control (see [Chapter 9.6](#))
- Global State Control (see [Chapter 9.7](#))
- Software Boot Support (see [Chapter 9.8](#))
- External Request Unit (see [Chapter 9.9](#))
- Interrupt Generation (see [Chapter 9.10](#))
- Temperature Compensation (see [Chapter 9.11](#))
- Watchdog Timer (see [Chapter 9.12](#))
- Trap Generation (see [Chapter 9.13](#))
- Memory Content Protection (see [Chapter 9.14](#))
- Register Access Control (see [Chapter 9.15](#))
- Miscellaneous System Registers (see [Chapter 9.16](#))
- SCU Registers and Address map (see [Chapter 9.17](#))

Important Information: Register Programming

Some of XC27x8X registers are initialized during the startup procedure with values different from their reset-content (defined into respective registerdescriptions). They are listed in section "Registers modified by the Startup Procedure".

The System Control Unit contains special function registers, which can not be programmed in an arbitrary order in particular due to the usage of an internal voltage regulator. In order to prevent critical system conditions because of an improper setup and to provide means for easy and quick configuration and control of sensitive features such as power supply and clock generation, recommendations and examples for the programming sequence of the registers will be given in the Programmer's Guide.

In particular the registers listed below have to be updated with care:

- Clock Generation Unit: WUOSCCON, HPOSCCON, PLLOSCCON, PLLCONx
- Power Supply: EVR1CON0, EVR1SET15VHP, EVRMCON0, EVRMSET15VHP, PVC1CON0, PVC1MCON0, SWDCON0

- System: SYSCON0

9.1 Clock Generation Unit

The Clock Generation Unit (CGU) allows a very flexible clock generation for the XC27x8X. During user program execution the frequency can be programmed for an optimal ratio between performance and power consumption in the actual application state.

9.1.1 Overview

The CGU can convert a low-frequency external clock to a high-speed system clock or can create a high-speed system clock without external input.

The CGU consists of a Clock Generator and a Clock Control Unit (CCU).

The following table shows the input connection of the CGU.

Table 9-1 CGU Input Connection

Input	Connected to
XTAL 1	XTAL 1
XTAL 2	XTAL 2
CLKIN1	Port 2.9

The following clock signals are generated:

- System clock f_{SYS}
- RTC count clock f_{RTC}
- Wake-Up Timer (WUT) clock f_{WUT}
- STM clock f_{STM}
- External clock f_{EXT}

Chapter 9.1.5 and **Chapter 9.1.6** describe which clock signals are generated out of which selectable clocks.

Register Overview

The CGU is controlled by a number of registers shown in the following figure.

System Control Unit (SCU)

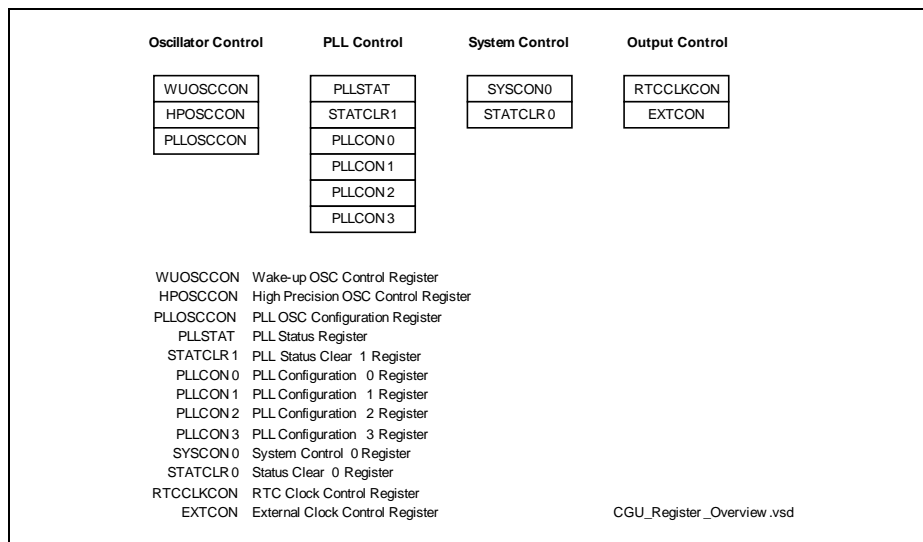


Figure 9-1 Clock Generation Unit Register Overview

The following sections describe the different parts of the CGU.

9.1.2 Trimmed Current Controlled Wake-Up Clock (OSC_WU)

The trimmed current controlled wake-up clock source provides a clock to control internal operations independent of the standard clock supplies and requires no external components. Its output frequency f_{WU} is configured via bit field **WUOSCCON.FREQSEL**.

9.1.3 High Precision Oscillator Circuit (OSC_HP)

The high precision oscillator circuit can drive an external crystal or accepts an external clock source. It consists of an inverting amplifier with XTAL1 as input, and XTAL2 as output.

Figure 9-3 and **Figure 9-2** show the recommended external circuitries for both operating modes, External Crystal Mode and External Input Clock Mode.

9.1.3.1 External Input Clock Mode

An external clock signal is supplied directly not using an external crystal and bypassing the amplifier of the oscillator. The maximum allowed input frequency depends on the characteristics of pin XTAL1.

When using an external clock signal it must be connected to XTAL1. XTAL2 is left open (unconnected).

Note: Voltages on XTAL1 must comply to the voltage defined in the data sheet.

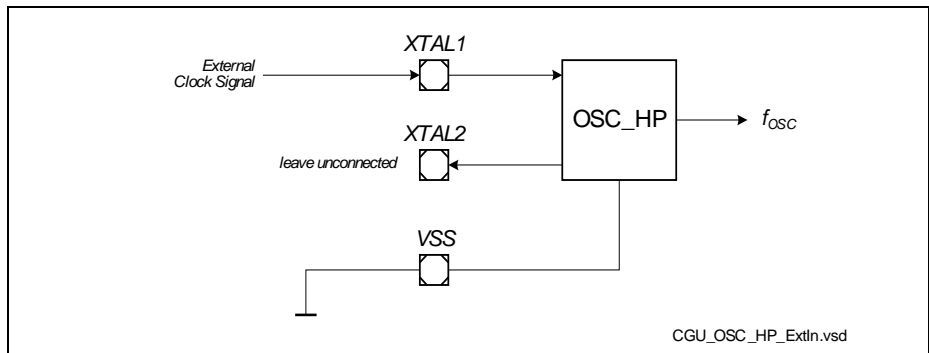


Figure 9-2 XC27x8X External Clock Input Mode for the High-Precision Oscillator

9.1.3.2 External Crystal Mode

An external oscillator load circuitry must be used, connected to both pins, XTAL1 and XTAL2. It consists normally of the two load capacitances C1 and C2. For some crystals a series damping resistor might be necessary. The exact values and related operating

range depend on the crystal and have to be determined and optimized together with the crystal vendor using the negative resistance method.

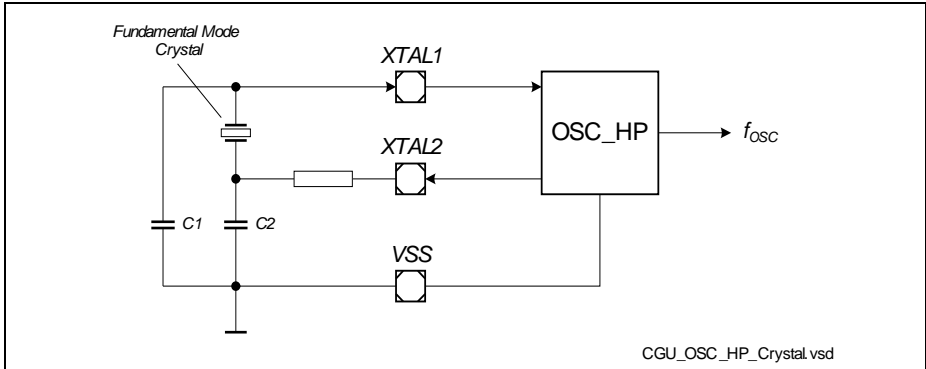


Figure 9-3 XC27x8X External Crystal Mode Circuitry for the High-Precision Oscillator

Support for Start-up Control of an External Crystal

The first time before the system clock is generated based on an external crystal 1000 cycles of the crystal clock should be waited before the clock control system is changed to External Crystal Mode. Bit **PLLSTAT.OSCLOCK** indicates if the oscillator OSC_HP operates for at least 2^{11} periods. Bit **PLLSTAT.OSCSTAB** indicates if OSC_HP operates for at least 2^{15} periods.

Oscillator Gain Control

The oscillator starts with a high drive level (gain) during and after a Power-on Reset to ensure safe start-up behavior in the beginning (force the crystal oscillation). When a stable oscillation has been reached after oscillation start-up (**PLLSTAT.OSCSTAB** = 1), the gain of the oscillator can be reduced. This reduces the power consumption of the oscillator, which is especially important in the power saving modes. This gain reduction is selected by **HPOSCCON.GAINSEL**.

Note: Choosing the gain setting is only possible with detailed consideration of parasitics, external circuitry, frequency range and quality of the applied crystal and has to be verified by testing together with the crystal manufacturer.

9.1.4 Phase-Locked Loop (PLL) Module

The PLL can convert a low-frequency external clock signal to a high-speed system clock for maximum performance. The PLL also has fail-safe logic that detects degenerate external clock behavior such as abnormal frequency deviations or a total loss of the external clock. It can execute emergency actions if it loses its lock on the external clock.

This module is a phase locked loop for integer frequency synthesis. It allows the use of input and output frequencies of a wide range by varying the different divider factors.

9.1.4.1 Features

Here is a brief overview of the functions that are offered by the PLL.

- VCO lock detection
- 4-bit input divider **P**: (divide by PDIV+1)
- 7-bit feedback divider **N**: (multiply by NDIV+1)
- 10-bit output divider **K2**: (divide K2DIV+1) with a fractional mode (2-bit)
- 10-bit VCO bypass divider **K1**: (divide by either by K1DIV+1)
- Oscillator run detection and Watchdog
- Different operating modes
 - Prescaler Mode
 - Unlocked Mode
 - Normal Mode
- Different power saving modes
 - Power Down
 - Sleep Mode (VCO Power Down)
- Glitchless programming of output divider K2 and VCO bypass divider K1
- Glitchless switching between Normal Mode and Prescaler Mode
- Trimmed current controlled clock source

9.1.4.2 PLL Functional Description

The PLL consists of a Voltage Controlled Oscillator (VCO) with a feedback path. A divider in the feedback path (N-Divider) divides the VCO frequency. The resulting frequency is then compared with the divided external frequency (P-Divider). The phase detection logic determines the difference between the two clocks and accordingly controls the frequency of the VCO (f_{VCO}). A PLL lock detection unit monitors and signals this condition. The phase detection logic continues to monitor the two clocks and adjusts the VCO clock if required. The PLL output clock f_{PLL} is derived from the VCO clock using the K2-Divider or from the oscillator clock using the K1-Divider.

The following figure shows the PLL block structure.

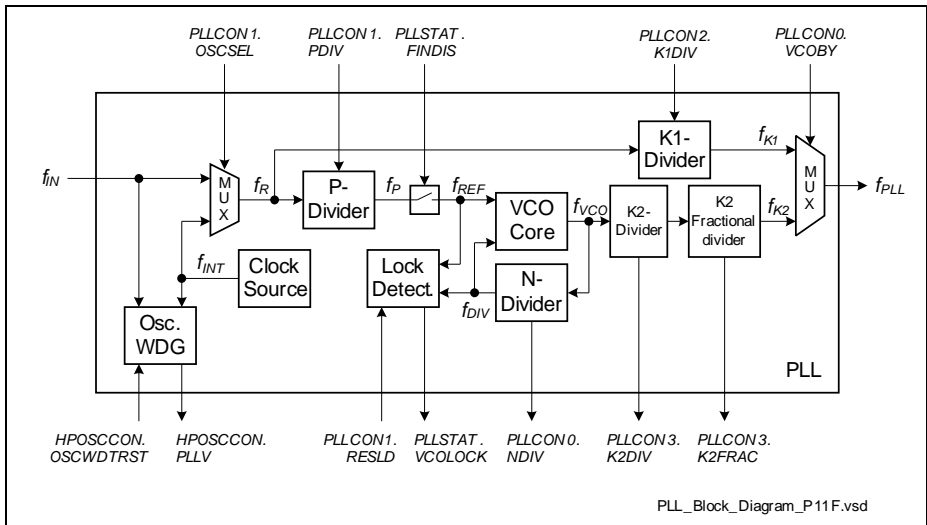


Figure 9-4 PLL Block Diagram

Clock Source Control

The reference frequency f_R can be selected to be either taken from the trimmed current controlled clock source f_{INT} or from an external clock source f_{IN} .

PLL Modes

The PLL clock f_{PLL} is generated from f_R in one of the following software selectable modes:

- Normal Mode
- Prescaler Mode
- Unlocked Mode

In Normal Mode the reference frequency f_R is divided by a factor P, multiplied by a factor N and then divided by a factor K2. The output frequency is given by

(9.1)

$$f_{PLL} = \frac{N}{P \cdot K2} \cdot f_R$$

In order to have a finer step width to ramp-up/down the system frequency K2-Divider provides a fractional mode. In this mode the clock frequency is further reduced by either an approximation of 8.3%, 16.7% or 25% depending on the bit PLLCON3.K2FRAC.

System Control Unit (SCU)

In Prescaler Mode the reference frequency f_R is divided by a factor K1. The output frequency is given by

(9.2)

$$f_{\text{PLL}} = \frac{f_R}{K1}$$

In Unlocked Mode the base output frequency of the Voltage Controlled Oscillator (VCO) f_{VCObase} is divided by a factor K2. The output frequency is given by

(9.3)

$$f_{\text{PLL}} = \frac{f_{\text{VCObase}}}{K2}$$

PLL Power Saving Modes

PLL Power Down Mode The PLL offers a Power Down Mode to save power if the PLL is not needed at all. While the PLL is in Power Down Mode no PLL output frequency is generated.

PLL Sleep Mode The PLL offers a Sleep Mode (also called VCO Power Down Mode) to save power within the PLL. While the PLL is in Sleep Mode only the Prescaler Mode can be used.

9.1.4.3 Configuration and Operation of the PLL Modes

The following section describes the configuration and the operation of the different PLL modes.

Configuration and Operation of the Unlocked Mode

In Unlocked Mode, the PLL is running at its VCO base frequency and f_{PLL} is derived from f_{VCO} by the K2-Divider.

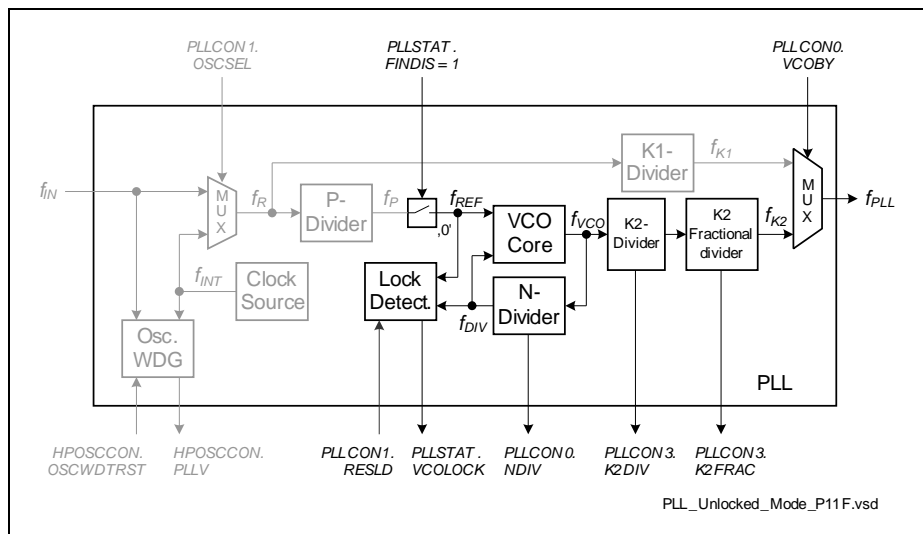


Figure 9-5 PLL Unlocked Mode Diagram

The Unlocked Mode is selected by the following settings:

- STATCLR1.SETFINDIS = 1
- PLLCON0.VCOBY = 0

The Unlocked Mode is entered when all following conditions are true:

- PLLSTAT.FINDIS = 1
- PLLSTAT.VCOBYST = 1

Operation in Unlocked Mode does not require an input clock f_{IN} . The Unlocked Mode is automatically entered on a PLL VCO Loss-of-Lock event if bit PLLCON1.EMFINDISEN is cleared. This mechanism allows a fail-safe operation of the PLL as in emergency cases still a clock is available.

The frequency of the Unlocked Mode $f_{VCObase}$ is listed in the Data Sheet as “free running” mode.

Note: Changing the system operation frequency by changing the value of the K2-Divider or the VCO range has a direct influence on the power consumption of the device. Therefore, this has to be done carefully. In order to have a finer step width to ramp-up/down the system frequency K2-Divider provides a fractional mode in which the frequency is further reduced. In this mode the clock frequency is further reduced by either an approximation of 8.3%, 16.7% or 25% depending on the bit PLLCON3.K2FRAC.

Configuration and Operation of the Normal Mode

In Normal Mode, the PLL is running at frequency f_{PLL} , where f_R is divided by a factor P, multiplied by a factor N and then divided by a factor K2.

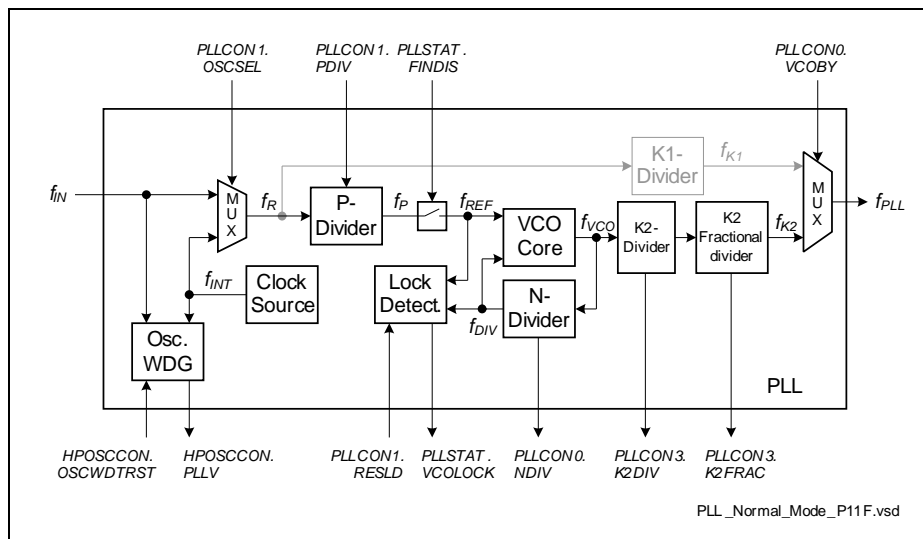


Figure 9-6 PLL Normal Mode Diagram

The Normal Mode is selected by the following settings:

- PLLCON0.VCOBY = 0
- STATCLR1.CLRFINDIS = 1

The Normal Mode is entered when all following conditions are true:

- PLLSTAT.FINDIS = 0
- PLLSTAT.VCOBYST = 1
- PLLSTAT.VCOLOCK = 1
- HPOSCCON.PLLV = 1

Operation in Normal Mode requires a clock frequency of f_R . When f_{IN} is selected as source for f_R it is recommended to check and monitor if an input frequency f_R is available at all by checking HPOSCCON.PLLV.

The system operation frequency in Normal Mode is controlled by the values of the three dividers: P, N, and K2. A modification of the two dividers P and N has a direct influence on the VCO frequency and leads to a loss of the VCO Lock status. A modification of the K2-divider has no impact on the VCO Lock status but changes the PLL output frequency.

Note: Changing the system operation frequency by changing the value of the K2-Divider has a direct influence on the power consumption of the device. Therefore, this has

System Control Unit (SCU)

to be done carefully. In order to have a finer step width to ramp-up/down the system frequency K2-Divider provides a fractional mode (K2FRAC) in which the frequency is further reduced. In this mode the clock frequency is further reduced by either an approximation of 8.3%, 16.7% or 25% depending on the bit PLLCON3.K2FRAC.

To modify or enter the Normal Mode frequency, follow the sequence described below:

Configure and enter Prescaler Mode. For more details see the Prescaler Mode.

Disable the trap generation for the VCO Lost-of-Lock.

While the Prescaler Mode is used the Normal Mode can be configured and checked for a positive VCO Lock status. The first target frequency of the Normal Mode should be selected in a way that it matches or is only slightly higher as the one used in the Prescaler Mode. This avoids big changes in the system operation frequency and, therefore, the power consumption when switching later from Prescaler Mode to Normal Mode. The P and N dividers should be selected in the following way:

- Selecting P and N in a way that f_{VCO} is in the lower area of its allowed values leads to a slightly reduced power consumption but to a slightly increased jitter
- Selecting P and N in a way that f_{VCO} is in the upper area of its allowed values leads to a slightly increased power consumption but to a slightly reduced jitter

After the P, and N dividers are updated for the first configuration, the indication of the VCO Lock status (PLLSTAT.VCOLOCK = 1) should be awaited.

Note: It is recommended to reset the VCO Lock detection (PLLCON1.RESLD = 1) after the new values of the dividers have been configured to get a defined VCO lock check time.

When this happens the switch from Prescaler Mode to Normal Mode can be done. Normal Mode is requested by clearing PLLCON0.VCOBY. The Normal Mode is entered when the status bit PLLSTAT.VCOBYST is set.

Now the Normal Mode is entered. The trap status flag for the VCO Lock trap should be cleared and then enabled again.

The intended PLL output target frequency can be configured by changing only the K2-Divider. Depending on the selected divider value of the K2-Divider, the duty cycle of the clock is selected. This can have an impact on the operation with an external communication interface. In order to avoid too big frequency changes it might be necessary to change the K2-Divider in multiple steps. When the value of the K2-Diver was changed the next update of this value should not be done before bit PLLSTAT.K2RDY is set.

Note: The Programmers's Guide describes a smooth frequency stepping to achieve an appropriate load regulation of the internal voltage regulator.

PLL VCO Lock Detection

- PLLSTAT.VCOBYST = 0
- HPOSCCON.PLLV = 1

Operation in Prescaler Mode requires an input clock frequency f_R . If f_{IN} is selected as clock source for f_R it is recommended to check and monitor if an input frequency f_{OSC} is available at all by checking HPOSCCON.PLLV. There are no requirements regarding the frequency of f_R .

The system operation frequency in Prescaler Mode is controlled by the value of the K1-Divider. When the value of PLLCON1.K1DIV was changed the next update of this value should not be done before bit PLLSTAT.K1RDY is set.

Note: Changing the system operation frequency by changing the value of the K1-Divider has a direct influence on the power consumption of the device. Therefore, this has to be done carefully.

The duty cycle of the clock signal depends on the selected value of the K1-Divider. This can have an impact for the operation with an external communication interface.

The Prescaler Mode is requested from the Unlocked or Normal Mode by setting bit PLLCON0.VCOBY. The Prescaler Mode is entered when the status bit PLLSTAT.VCOBYST is cleared.

Before the Prescaler Mode is requested the K1-Divider should be configured with a value generating a PLL output frequency f_{PLL} that matches the one generated by the Unlocked or Normal Mode as much as possible. In this way the frequency change resulting out of the mode change is reduced to a minimum.

The Prescaler Mode is requested to be left by clearing bit PLLCON0.VCOBY. The Prescaler Mode is left when the status bit PLLSTAT.VCOBYST is set.

Configuration and Operation of the PLL Power Down Mode

The Power Down Mode is entered by setting bit PLLCON0.PLLPWD. While the PLL is in Power Down Mode no PLL output frequency is generated.

Configuration and Operation of the PLL Sleep Mode

The Sleep Mode (also called VCO Power Down Mode) is entered by setting bit PLLCON0.VCOPWD. While the PLL is in Sleep Mode only the Prescaler Mode is operable. Selecting the Sleep Mode does not automatically switch to the Prescaler Mode. Therefore, before the Sleep Mode is entered the Prescaler Mode must be active.

9.1.4.4 Power Regulator

The analog parts of the PLL (VCO, trimmed current controlled clock source) are running on a dedicated supply generated by a dedicated regulator integrated within the PLL unit.

The regulator has to be enabled separately before the analog blocks of the PLL are activated, i.e. trimmed current controlled clock source and VCO must be kept off until

the supply is stable. After activation, the PLL regulator will need its ramp-up time to properly ramp-up the analog PLL supply.

When the regulator shall be disabled in conjunction with a power down of the PLL digital part, it has to be taken into account that the digital part needs an active clock at the output of the PLL to ramp down. In case this clock is generated by one of the PLL oscillators, power down of PLL must be entered before the regulator is disabled. VCO and trimmed current controlled clock source may be activated or switched off together.

9.1.4.5 Divider Handshake

The PLL provides several handshake interfaces for dividers. This section describes how a handshake is to be conducted upon a change of configuration.

The general conduction of the handshake is the same for all interfaces. However, a sample sequence is described here in conjunction with re-programming of a divider.

Note: The described handshake only works if the new setting (e.g. divider value) changes the current value upon the handshake.

The handshake should be done in the the following steps:

1. Clear acknowledge bit together with setting the new divider value
2. Poll on ready bit to be 0
3. Set acknowledge bit
4. Poll on ready bit to be 1

This approach will even work in case the handshake has not been properly served before, and ready is already at 0 from the beginning. In any case, a change of the divider value will set ready to 0.

9.1.4.6 Trimmed Current Controlled Clock

The trimmed current controlled clock source provides a clock f_{INT} for the PLL.

Note: The clock f_{INT} is also required for the operation of the oscillator watchdog.

9.1.4.7 Input Clock Selection

The reference clock f_R can be provided by the PLL input clock source f_{IN} or by the trimmed current controlled clock source f_{INT} . This is selected via bit **PLLCON1.OSCSEL**.

The PLL input clock f_{IN} can be selected to be either taken from the high-precision oscillator clock source f_{OSC} or from the direct clock input f_{CLKIN1} . This is configured by **PLLCON1.INSEL**.

9.1.4.8 Oscillator Watchdog

The oscillator watchdog continuously monitors the input clock f_{IN} . If the input frequency becomes too low or if the input clock fails, this oscillator fail condition is indicated by `HPOSCCON.PLLV = 0` and an interrupt request is generated.

By setting bit `HPOSCCON.OSCWDTRST` the detection can be restarted without a reset of the complete PLL, e.g. in case of a VCO loss-of-lock condition.

Note: The oscillator watchdog requires the trimmed current controlled clock f_{INT} as a reference. Therefore, it can only be used (`HPOSCCON.PLLV` is valid) while the clock source is active.

9.1.4.9 Switching PLL Parameters

The following restriction applies when changing PLL parameters inside the PLLCON0 to PLLCON3 registers:

- The VCO bypass switch may be used at any time, however, it has to be ensured that the maximum operating frequency of the device (see data sheet) will not be exceeded.
- Prescaler Mode should be selected.
- After switching to Prescaler Mode, NDIV and PDIV can be adjusted.
- Before deselecting the Prescaler Mode, the RESLD bit has to be set and then the VCOLOCK flag has to be checked. Only when the VCOLOCK flag is set again, the Prescaler Mode may be deselected.
- Before changing VCOSEL, the Prescaler Mode must be selected.

Note: PDIV and NDIV can also be switched in Normal Mode. When changing NDIV, it must be regarded that the VCO clock f_{VCO} may exceed the target frequency until the PLL becomes locked. After changing PDIV or NDIV, it must be waited for the PLL lock condition. This procedure is typically used for increasing the VCO clock step-by-step.

9.1.5 Clock Control Unit

The Clock Control Unit selects the current clock sources for the clock signals used in the XC27x8X. It generates the following clocks:

- System clock f_{SYS}
- RTC count clock f_{RTC}
- WUT clock f_{WUT}
- System timer clock f_{STM}
- Output clock f_{EXT}

The following clock signals can be selected:

- PLL clock f_{PLL}
- The oscillator clock (OSC_HP) f_{OSC}
- Wake-up clock f_{WU}
- Input CLKIN1 as Direct Clock Input f_{CLKIN1}

9.1.5.1 Clock Generation

Different clock sources can be selected for the generated clock signals.

Note: The selected clock sources are affected by the start-up procedure. See chapter Device Status after Start-up for the register values set by the different start-up procedures.

System Clock Generation

The system clock f_{SYS} can be selected from the following clock sources in the CCU:

- Wake-up clock f_{WU}
- The oscillator clock (OSC_HP) f_{OSC}
- PLL clock f_{PLL}
- Input CLKIN1 as Direct Clock Input f_{CLKIN1}

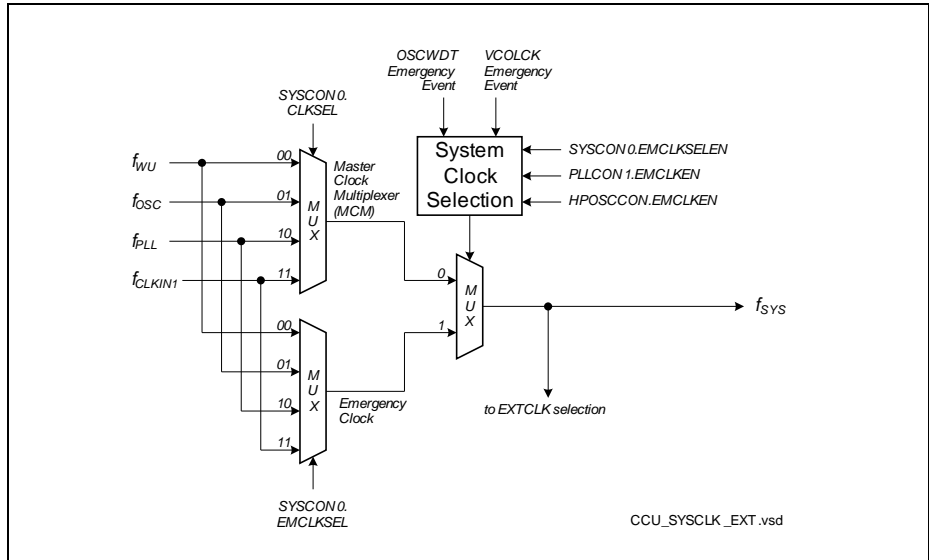


Figure 9-8 Clock Control Unit, System Clock Generation

RTC Clock Generation

For the RTC module it is possible to select the operation in synchronous or asynchronous mode in the module itself. The asynchronous clock for the RTC can be selected out of following clock sources in the CCU:

- PLL clock f_{PLL}
- The oscillator clock (OSC_HP) f_{OSC}
- Wake-up clock f_{WU}

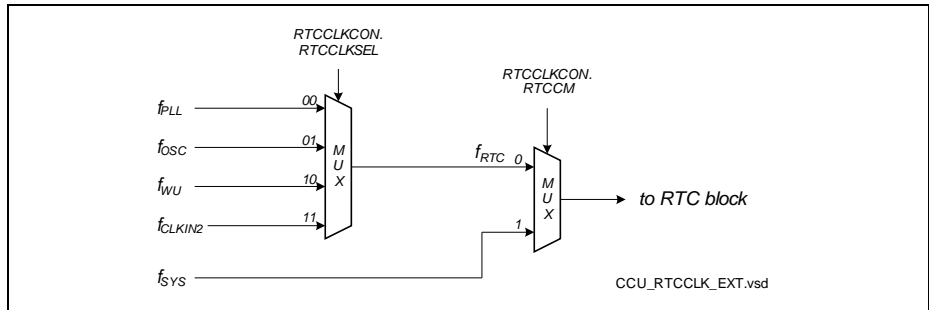


Figure 9-9 Clock Control Unit, RTC Clock Generation

System Timer (STM) Clock Generation

The system timer clock can be selected out of following clock sources:

- The Direct Clock from oscillator OSC_HP f_{OSC}
- PLL clock f_{PLL}
- Input CLKIN1 as Direct Clock Input f_{CLKIN1}
- Wake-up clock f_{WU}

Then the selected clock can be divided by the factor defined in **STMCON.CLKDIV** (see [Chapter 9.2.1.2](#)).

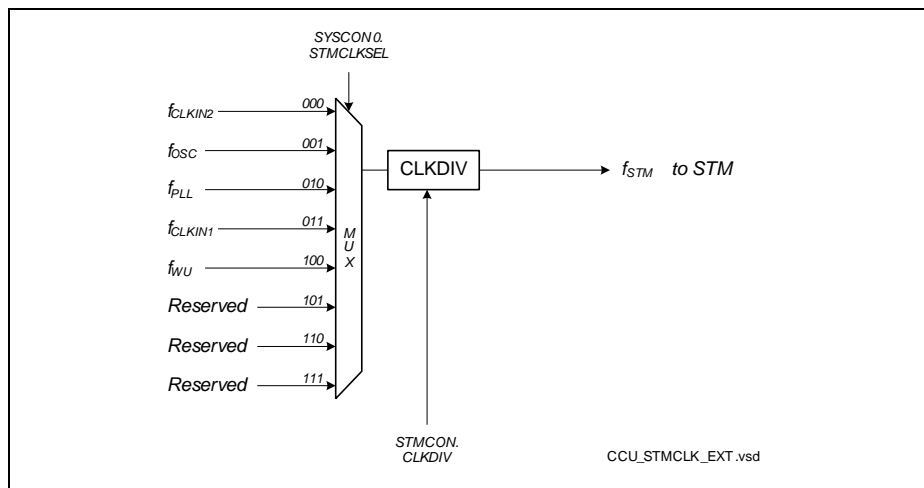


Figure 9-10 Clock Control Unit, STM Clock Generation

Wake-up Timer (WUT) Clock Generation

The wake-up timer clock can be selected out of following clock sources in the CCU:

- Wake-up clock f_{WU}
- The Direct Clock from oscillator OSC_HP f_{OSC}
- PLL clock f_{PLL}
- Input CLKIN1 as Direct Clock Input f_{CLKIN1}

Then the selected clock can be divided by the factor defined in **WUCR.CLKDIV** (see [Chapter 9.3.2.2](#)).

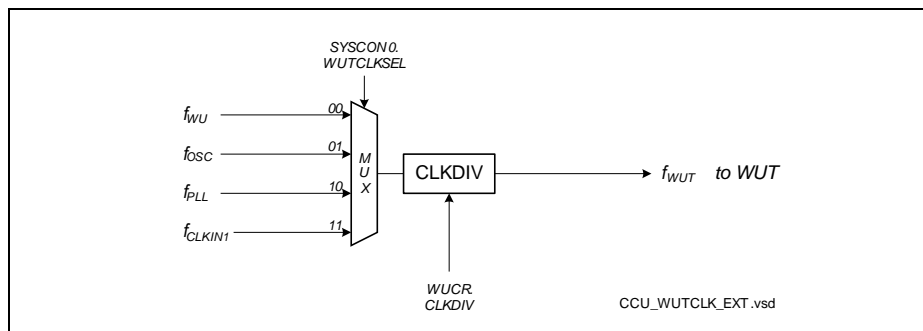


Figure 9-11 Clock Control Unit, WUT Clock Generation

9.1.5.2 Selecting and Changing the Operating Frequency

When selecting the clock source and the clock generation method, the required parameters must be carefully written to the respective bit fields, to avoid unintended intermediate states.

Many applications change the frequency of the system clock f_{SYS} during operation to optimize performance and power consumption of the system. Modifying the operating frequency changes the consumed switching current, which influences the power supply. Therefore, while the core voltage is generated by the on-chip Embedded Voltage Regulators (EVRs), the operating frequency may only be changed according to the rules given in the Data Sheet.

Note: To avoid the indicated problems, specific sequences are recommended that ensure the intended operation of the clock system interacting with the power system. Please refer to the document Programmer's Guide.

9.1.5.3 System Clock Emergency Handling

The generation of the system clock f_{SYS} can be affected, if either the PLL is no more locked to its input signal f_{IN} , or if the input clock f_{IN} is no more active. Both events can be detected and are indicated to the application software. The clock system takes appropriate actions where necessary, so the device and the application is never left without an alternate clock signal.

Oscillator Watchdog Event

If the clock frequency of the external source drops below a limit value the oscillator watchdog (OSCWDT) (see [Chapter 9.1.4.8](#)) then the clock source for the system clock f_{SYS} is switched to an alternate clock source, if enabled (HPOSCCON.EMCLKEN = 1). In this case following information is available:

- The oscillator watchdog trap flag (TRAPSTAT.OSCWDTT) is set and a trap request to the CPU is activated, if enabled (TRAPDIS.OSCWDTT = 0).
- Bit HPOSCCON.PLLV = 0, while the clock f_{IN} is missing
- Bit SYSCON0.EMSOSC is set, if SYSCON0.EMCLKSELEN is set
- The source of the system clock f_{SYS} is switched to alternate clock source selected by SYSCON0.EMCLKSEL, if enabled (SYSCON0.EMCLKSELEN = 1). This is indicated by bit SYSCON0.SELSTAT = 1.

PLL VCO Loss-of-Lock Event

If the PLL output frequency is no longer locked to its input frequency f_{IN} , the PLL switches from PLL Normal mode to the Unlocked mode, if enabled (PLLCON1.EMFINDISEN = 1). In this case following information is available:

- The PLL VCO loss of lock trap flag (TRAPSTAT.VCOLCKT) is set and a trap request to the CPU is activated, if enabled (TRAPDIS.VCOLCKT = 0).
- Bit PLLSTAT.VCOLOCK = 0, while the PLL is not locked
- Bit SYSCON0.EMSVCO is set, if SYSCON0.EMCLKSELEN is set
- The PLL VCO clock input is disconnected (PLLSTAT.FINDIS = 1) and the PLL clock slows down to its VCO base frequency.

System Behavior

Emergency routines can be executed with the alternate clock (emergency clock or VCO base frequency). The application can then enter a safe status and stop operation, or it can switch to an emergency operating mode, where a reduced performance and/or feature set is provided.

The Programmer's Guide describes both, how to enable these features, and how to react properly on each of the two events.

9.1.6 External Clock Output

An external clock output can be provided via pin EXTCLK to clock an external system or to observe one of the selectable device clocks. This external clock is enabled by setting bit EXTCON.EN and by selecting the clock signal as alternate output function at pin EXTCLK. Following clocks can be selected by EXTCON.SEL for external clock f_{EXT} :

- System clock f_{SYS}
- Programmable clock output f_{OUT}
- Direct Clock from oscillator OSC_HP f_{OSC}
- Direct Clock Input f_{CLKIN1}
- PLL clock f_{PLL}
- Wake-up clock f_{WU}
- RTC clock f_{RTC}

Note: Changing bit field EXTCON.SEL can lead to spikes at pin EXTCLK.

9.1.6.1 Programmable Frequency Output

The programmable frequency output f_{OUT} can be selected as clock output (EXTCLK). This clock can be controlled via software, and so can be adapted to the requirements of the connected external circuitry. The programmability also extends the power management to a system level, as also circuitry (peripherals, etc.) outside the XC27x8X can be run at a scalable frequency or can temporarily be left without a clock.

Clock f_{OUT} is generated via a reload counter, so the output frequency can be selected in small steps.

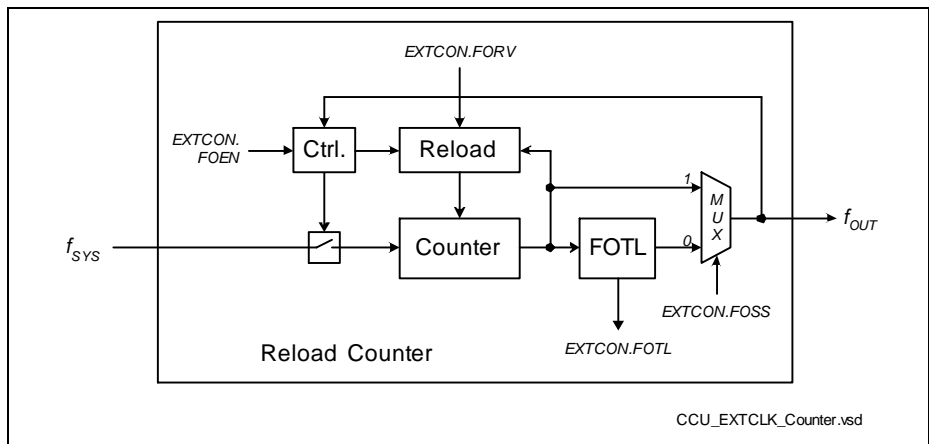


Figure 9-12 Programmable Frequency Output Generation

f_{OUT} always provides complete output periods (provided f_{SYS} is available):

System Control Unit (SCU)

- When f_{OUT} is started (EXTCON.FOEN is set) counter FOCNT is loaded from EXTCON.FORV
- When OUT is stopped (EXTCON.FOEN is cleared) counter FOCNT is stopped when f_{OUT} has reached (or is) '0'.

Register EXTCN provides control over the output generation (frequency, waveform, activation) as well as all status information (EXTCON.FOTL).

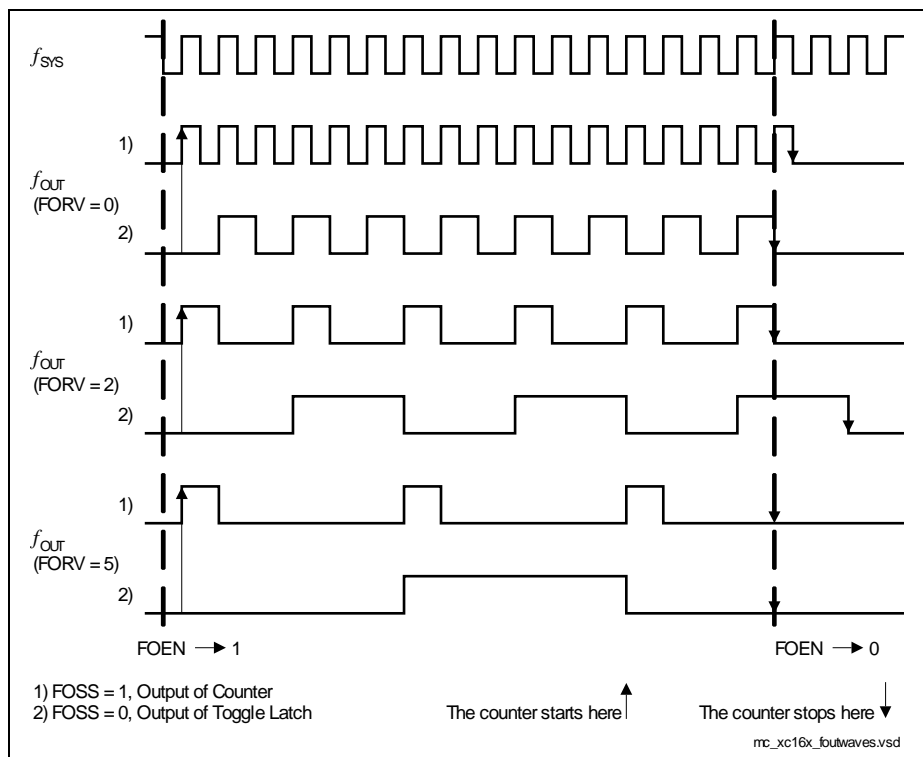


Figure 9-13 Output Waveforms Examples

*Note: The output (for EXTCN.FOSS= 1) is high for the duration of one f_{SYS} cycle for all reload values EXTCN.FORV > 0. For EXTCN.FORV = 0 the output frequency corresponds to f_{SYS} .
 When a reference clock is required (e.g. for the bus interface), f_{SYS} must be selected directly.*

9.1.7 CGU Registers

9.1.7.1 Wake-up Clock Register

This register controls the settings of OSC_WU.

WUOSCCON

Wake-up OSC Control Register ESFR (F1AE_H/D7_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0											DIS	0	FREQSEL		
r											rw	rw	rw		

Field	Bits	Type	Description
FREQSEL	[1:0]	rw	Frequency Selection The values for the different settings are listed in the data sheet. <i>Note: This value must not be changed while f_{WU} is used as clock source for any logic.</i>
0	[3:2]	rw	Reserved Do not change this value when writing to this register
DIS	4	rw	Clock Disable 0 _B The oscillator is switched on and the clock is enabled 1 _B The oscillator is switched off and the clock is disabled
0	[15:5]	r	Reserved Read as 0; should be written with 0.

9.1.7.2 High Precision Oscillator Register

This register controls the setting of OSC_HP.

HPOSCCON

High Precision OSC Control Register

ESFR (F1B4_H/DA_H)

Reset Value: 053C_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0			OSC 2 L0	OSC 2 L1	EM FIN DIS EN	EM CLK EN	SH BY	X1D EN	X1D	GAINSEL	MODE		OSC WDT RST	PLL V	
r			rh	rh	rw	rw	rw	rw	rh	rw	rw		w	rh	

Field	Bits	Type	Description
PLL V	0	rh	Oscillator for PLL Valid Status Bit This bit indicates whether the frequency output of OSC_HP is usable. This is checked by the Oscillator Watchdog of the PLL. 0 _B The OSC_HP frequency is not usable. The frequency is below the limit. 1 _B The OSC_HP frequency is usable. The frequency is not below the limit. For more information see Chapter 9.1.4.8 .
OSCWDT RST	1	w	Oscillator Watchdog Reset 0 _B No action 1 _B The Oscillator Watchdog of the PLL is reset and restarted <i>Note: This bit is always read as 0.</i>
MODE	[3:2]	rw	Oscillator Mode 00 _B The oscillator is active (External Crystal Mode) 01 _B Reserved, do not use 10 _B External Input Clock Mode; oscillator is in power-saving mode 11 _B OSC_HP is disabled and in power-saving mode

System Control Unit (SCU)

Field	Bits	Type	Description
GAINSEL	[5:4]	rw	Oscillator Gain Selection 00 _B Supply current is typically 300 µA (not tested) 01 _B Supply current is typically 530 µA (not tested) 10 _B Supply current is typically 450 µA (not tested) 11 _B Supply current is typically 610 µA (not tested)
X1D	6	rh	XTAL1 Data Value This bit reflects the inverted level of pin XTAL1. This bit is sampled with f_{SYS} while X1DEN is set. <i>Note: Voltages on XTAL 1 must comply to the voltage defined in the data sheet.</i>
X1DEN	7	rw	XTAL1 Data Enable 0 _B Bit X1D is not updated 1 _B Bit X1D can be updated
SHBY	8	rw	Shaper Bypass The shaper forms a proper signal from the input signal. This bit must be 0 for proper operation. 0 _B The shaper is not bypassed 1 _B The shaper is bypassed
EMCLKEN	9	rw	OSCWDT Emergency System Clock Source Select Enable This bit requests the master clock multiplexer (MCM) to switch to an alternate clock (selected by bit field SYSCON0.EMCLKSEL) in an OSCWDT emergency case. 0 _B MCM remains controlled by SYSCON0.CLKSEL 1 _B MCM is controlled by SYSCON0.EMCLKSEL
EMFINDISEN	10	rw	Emergency Input Clock Disconnect Enable This bit defines if bit PLLSTAT.FINDIS is set in an OSCWDT emergency case. 0 _B No action 1 _B PLLSTAT.FINDIS is set in an emergency case <i>Note: Please refer to the Programmer's Guide for a description of the proper handling.</i>

System Control Unit (SCU)

Field	Bits	Type	Description
OSC2L1	11	rh	OSC_HP Not Usable Frequency Event This sticky bit indicates if bit PLLV has been cleared since OSC2L1 has last been cleared (by writing 1 to bit STATCLR1.OSC2L1CLR). 0 _B No change of PLLV detected 1 _B Bit PLLV has been cleared at least once
OSC2L0	12	rh	OSC_HP Usable Frequency Event This sticky bit indicates if bit PLLV has been set since OSC2L0 has last been cleared (by writing 1 to bit STATCLR1.OSC2L0CLR). 0 _B No change of PLLV detected 1 _B PLLV has been set at least once
0	[15:13]	r	Reserved Read as 0; should be written with 0.

9.1.7.3 Trimmed Current Controlled Clock Control Register

This register controls the trimmed current controlled clock source.

PLLOSCCON

PLL OSC Control Register

ESFR (F1B6 _H /DB _H)										Reset Value: 0000 _H					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0						OSCTRIM									OSC PD
r						rw									rw

Field	Bits	Type	Description
OSCPD	0	rw	Clock Source Power Saving Mode 0 _B Trimmed current controlled clock source is active 1 _B Trimmed current controlled clock source is off
OSCTRIM	[9:1]	rw	Clock Source Trim Configuration This value is used to adjust the frequency range of the current controlled clock source. Do not change this value when writing to this register.
0	[15:10]	r	Reserved Read as 0; should be written with 0.

9.1.7.4 PLL Registers

PLLSTAT

PLL Status Register

ESFR (F0BC_H/5E_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OSC LOC K	OSC STA B	0	REG STA T	VCO L1	VCO L0	FIN DIS	K2 RDY	K1 RDY	N RDY	P RDY	0	VCO LOC K	OSC SEL ST	PWD STA T	VCO BY ST
rh	rh	r	rh	rh	rh	rh	rh	rh	rh	rh	r	rh	rh	rh	rh

Field	Bits	Type	Description
VCObYST	0	rh	VCO Bypass Status 0 _B The PLL clock is derived from divider K1 (Prescaler Mode) 1 _B The PLL clock is derived from divider K2 (Normal / Unlocked Mode) <i>Note: Coding of PLLCON0.VCOBY and VCObYST are different.</i>
PWDSTAT	1	rh	PLL Power-saving Mode Status 0 _B The PLL is operable 1 _B The digital part of the PLL is disabled
OSCSELST	2	rh	Oscillator Input Selection Status 0 _B External input clock source for the PLL (f_{IN}) 1 _B Internal input clock source for the PLL
VCOLOCK	3	rh	PLL VCO Lock Status 0 _B The frequency difference of f_{REF} and f_{DIV} is greater than allowed. The PLL cannot lock. 1 _B The PLL clock f_{PLL} is locked to f_{REF} and is stable. <i>Note: In case of a loss of lock, the VCO frequency f_{VCO} approaches to the upper/lower boundary of the selected VCO band if the reference frequency is higher/lower than possible for locking.</i>
PRDY	5	rh	P-Divider Ready Status 0 _B Bit field PLLCON1.PDIV has been changed, new K1 divider value not yet used. 1 _B The P-Divider operates with the value defined in bit field PLLCON1.PDIV.

System Control Unit (SCU)

Field	Bits	Type	Description
NRDY	6	rh	N-Divider Ready Status 0_B Bit field PLLCON0.NDIV has been changed, new K1 divider value not yet used. 1_B The P-Divider operates with the value defined in bit field PLLCON0.NDIV.
K1RDY	7	rh	K1-Divider Ready Status 0_B Bit field PLLCON2.K1DIV has been changed, new K1 divider value not yet used. 1_B The K1-Divider operates with the value defined in bit field PLLCON2.K1DIV.
K2RDY	8	rh	K2-Divider Ready Status 0_B Bit field PLLCON3.K2DIV has been changed, new K2 divider value not yet used. 1_B The K2-Divider operates with the value defined in bit field PLLCON3.K2DIV.
FINDIS	9	rh	Input Clock Disconnect Select Status 0_B The VCO is connected to the reference clock 1_B The VCO is disconnected from the reference clock <i>Note: Software can control this bit by writing 1 to bits SETFINDIS or CLRFINDIS in register STATCLR1.</i>
VCOL0	10	rh	VCO Lock Detection Lost Status This sticky bit indicates if bit VCOLOCK has been cleared since VCOL0 has last been cleared (by writing 1 to bit STATCLR1.VCOL0CLR). 0_B No falling edge detected 1_B PLLV has been cleared at least once (VCO lock was lost)
VCOL1	11	rh	VCO Lock Detection Reached Status This sticky bit indicates if bit VCOLOCK has been set since VCOL1 has last been cleared (by writing 1 to bit STATCLR1.VCOL1CLR). 0_B No rising edge detected 1_B VCO lock was reached

System Control Unit (SCU)

Field	Bits	Type	Description
VCOL1CLR	1	w	VCOL1 Clear Trigger 0 _B No action 1 _B Bit PLLSTAT.VCOL1 is cleared
OSC2L1CLR	2	w	OSC2L1 Clear Trigger 0 _B No action 1 _B Bits HPOSCCON.OSC2L1 is cleared
OSC2L0CLR	3	w	OSC2L0 Clear Trigger 0 _B No action 1 _B Bit HPOSCCON.OSC2L0 is cleared
SETFINDIS	4	w	Set Status Bit PLLSTAT.FINDIS 0 _B No action 1 _B Bit PLLSTAT.FINDIS is set. The VCO input clock is disconnected.
CLRFINDIS	5	w	Clear Status Bit PLLSTAT.FINDIS 0 _B No action 1 _B Bit PLLSTAT.FINDIS is cleared. The VCO input clock is connected.
0	[15:6]	r	Reserved Read as 0; should be written with 0.

Note: Bits of type w are always read as 0.

These registers control the configuration of the PLL.

PLLCON0

PLL Configuration 0 Register ESFR (F1B8_H/DC_H)

Reset Value: 1302_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
N ACK									IN SEL	REG EN SET	REG EN CLR	VCOSEL	VCO PWD	VCO BY	
rw									rw	w	w	rw	rw	rw	

Field	Bits	Type	Description
VCOBY	0	rw	VCO Bypass 0 _B Select divider K2 for PLL clock (Normal / Unlocked Mode) 1 _B Select divider K1 for PLL clock (Prescaler Mode, i.e. VCO is bypassed) Bit PLLSTAT.VCOBYST shows the actually selected divider. <i>Note: Coding of VCOBY and PLLSTAT.VCOBYST are different.</i>
VCOPWD	1	rw	VCO Power Saving Mode 0 _B Normal behavior 1 _B The VCO is put into a power saving mode and can no longer be used. Only the Prescaler Mode is active if previously selected.
VCOSEL	[3:2]	rw	VCO Range Select The values for the different settings are listed in the data sheet.
REGENCLR	4	w	Power Regulator Enable Clear 0 _B No action 1 _B Switch off the PLL's power regulator. The PLL is not powered (no operation possible). <i>Note: This bit is always read as 0.</i>
REGENSET	5	w	Power Regulator Enable Set 0 _B No action 1 _B Switch on the PLL's power regulator. The PLL is powered (operation possible). <i>Note: This bit is always read as 0.</i>

System Control Unit (SCU)

Field	Bits	Type	Description
INSEL	[7:6]	rw	Input Select 00 _B f_{OSC} is selected as input for the PLL 01 _B f_{CLKIN1} is selected as input for the PLL 10 _B Reserved, do not use this combination 11 _B Reserved, do not use this combination
NDIV	[14:8]	rw	N-Divider Value The value the N-Divider operates is NDIV+1. Only values between N = 8 and N = 28 are allowed for VCOSEL = 00 _B . Only values between N = 16 and N = 50 are allowed for VCOSEL = 01 _B . Only values between N = 24 and N = 64 are allowed for VCOSEL = 10 _B . Outside of this range, stable operation cannot be ensured.
NACK	15	rw	N-Divider Ready Acknowledge Setting this bit provides the acknowledge signal to NRDY.

PLLCON1

PLL Configuration 1 Register ESFR (F1BA_H/DD_H)

Reset Value: 000A_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P ACK		0				PDIV		0	EM FIN DIS EN	EM CLK EN	0	A OSC SEL	RES LD	OSC SEL	PLL PWD
rw		r				rw		r	rw	rw	r	rw	w	rw	rw

Field	Bits	Type	Description
PLLPWD	0	rw	PLL Power Saving Mode 0 _B Normal behavior 1 _B Complete PLL block is put into a power saving mode and no longer operates
OSCSEL	1	rw	Oscillator Input Selection 0 _B Select external clock as input for PLL 1 _B Select trimmed current controlled clock as input for PLL
RESLD	2	w	Restart VCO Lock Detection Setting this bit will reset bit PLLSTAT.VCOLOCK and restart the VCO lock detection. <i>Note: This bit is always read as 0.</i>
AOSCSEL	3	rw	Asynchronous Oscillator Input Selection This bit overrules the setting of bit OSCSEL. 0 _B Configuration is controlled via bit OSCSEL 1 _B Select asynchronously trimmed current controlled clock as input for PLL
EMCLKEN	5	rw	VCOLCK Emergency System Clock Source Select Enable This bit requests the master clock multiplexer (MCM) to switch to an alternate clock (selected by bit field SYSCON0.EMCLKSEL) in a VCOLCK emergency case. 0 _B MCM remains controlled by SYSCON0.CLKSEL 1 _B MCM is controlled by SYSCON0.EMCLKSEL

System Control Unit (SCU)

Field	Bits	Type	Description
EMFINDISEN	6	rw	Emergency Input Clock Disconnect Enable This bit defines if bit PLLSTAT.FINDIS is set in a VCOLCK emergency case. 0 _B No action 1 _B PLLSTAT.FINDIS is set in a VCOLCK emergency case <i>Note: Please refer to the Programmer's Guide for a description of the proper handling.</i>
PDIV	[11:8]	rw	P-Divider Value The value the P-Divider operates is PDIV+1.
PACK	15	rw	P-Divider Ready Acknowledge Setting this bit provides the acknowledge to PRDY.
0	4, 7, [14:12]	r	Reserved Read as 0; should be written with 0.

PLLCON3

PLL Configuration 3 Register **ESFR (F1BE_H/DF_H)** **Reset Value: 00CB_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
K2 ACK	0	K2FRAC		0							K2DIV				
rw	r	rw		r							rw				

Field	Bits	Type	Description
K2DIV	[9:0]	rw	K2-Divider Value The value the K2-Divider operates is K2DIV+1.
K2FRAC	[13:12]	rw	K2-Divider Fractional Mode This bit field defines the further reduction of the divided clock frequency. 00 _B No frequency reduction 01 _B Approx. 8.3% frequency reduction 10 _B Approx. 16.7% frequency reduction 11 _B Approx. 25% frequency reduction
K2ACK	15	rw	K2-Divider Ready Acknowledge¹⁾ Setting this bit provides the acknowledge to K2RDY.
0	[11:10], 14	r	Reserved Read as 0; should be written with 0.

1) Please refer to the Programmer's Guide for a description of the proper handling.

9.1.7.5 System Clock Control Registers

These registers control the system level clock behavior.

SYSCON0

System Control 0 Register

SFR (FF4A_H/A5_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL STA T	0	EMS VCO	EMS OSC	STM CLKSEL		WUT CLKSEL		EM CLK SEL EN	0	EM CLKSEL		0	CLKSEL		
rh	r	rh	rh	rw		rw		rw	r	rw		r	rw		

Field	Bits	Type	Description
CLKSEL	[1:0]	rw	Clock Select This bit field defines the clock source that is used as system clock for normal operation. 00 _B The Wake-up clock f_{WU} is used 01 _B The oscillator clock (OSC_HP) f_{OSC} is used 10 _B The PLL clock f_{PLL} is used 11 _B CLKIN1 as direct input clock f_{CLKIN1} is used
EMCLKSEL	[4:3]	rw	Emergency Clock Select This bit field defines the clock source that is used as system clock in case of an OSCWDT or VCOLCK emergency event. 00 _B The Wake-up clock f_{WU} is used 01 _B The oscillator clock (OSC_HP) f_{OSC} is used 10 _B The PLL clock f_{PLL} is used 11 _B CLKIN1 as direct input clock f_{CLKIN1} is used
EMCLKSELEN	6	rw	Emergency Clock Select Enable Controls switching the system clock to an alternate source in case of an OSCWDT or VCOLCK event. 0 _B The switching is disabled 1 _B The switching is enabled

Field	Bits	Type	Description
WUTCLKSEL	[8:7]	rw	WUT Clock Select This bit field defines the clock source that is used as wake-up timer clock for operation. 00 _B The Wake-up clock f_{WU} is used 01 _B The oscillator clock (OSC_HP) f_{OSC} is used 10 _B The PLL clock f_{PLL} is used 11 _B CLKIN1 as direct Input clock f_{CLKIN1} is used
STMCLKSEL	[11:9]	rw	STM Clock Select This bit field defines the clock source that is used as STM clock for operation. 001 _B The oscillator clock (OSC_HP) f_{OSC} is used 010 _B The PLL clock f_{PLL} is used 011 _B CLKIN1 as direct Input clock f_{CLKIN1} is used 100 _B The Wake-up clock f_{WU} is used 101 _B Reserved, do not use this combination 110 _B Reserved, do not use this combination 111 _B Reserved, do not use this combination
EMSOSC	12	rh	OSCWDT Emergency Event Source Status 0 _B No OSCWDT emergency event occurred since EMSOSC has been cleared last 1 _B An OSCWDT emergency event has occurred <i>Note: This bit is only set if EMCLKSELEN is set.</i>
EMSVCO	13	rh	VCOLCK Emergency Event Source Status 0 _B No VCOLCK emergency event occurred since EMSVCO has been cleared last 1 _B A VCOLCK emergency event has occurred <i>Note: This bit is only set if EMCLKSELEN is set.</i>
SELSTAT	15	rh	Clock Select Status 0 _B The standard configuration from bit field CLKSEL is used currently 1 _B The configuration from bit field EMCLKSEL is used currently
0	2, 5, 14	r	Reserved Read as 0; should be written with 0.

STATCLR0

Status Clear 0 Register

ESFR (F0E0_H/70_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		EMC VCO	EMC OSC							0					
r		w	w							r					

Field	Bits	Type	Description
EMCOSC	12	w	EMSOSC Clear Trigger 0 _B No action 1 _B Bit SYSCON0.EMSOSC is cleared <i>Note: This bit is always read as 0.</i>
EMCVCO	13	w	EMSVCO Clear Trigger 0 _B No action 1 _B Bit SYSCON0.EMSVCO is cleared <i>Note: This bit is always read as 0.</i>
0	[11:0], [15:14]	r	Reserved Read as 0; should be written with 0.

9.1.7.6 RTC Clock Control Register

Note: Only change register RTCCCLKCON while the RTC is off.

RTCCCLKCON

RTC Clock Control Register

SFR (FF4E_H/A7_H)

Reset Value: 0006_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0													RTC CM	RTC CLKSEL	
r													rw	rw	

Field	Bits	Type	Description
RTCCCLKSEL	[1:0]	rw	RTC Clock Select This bit field defines the count clock source for the RTC. 00 _B The PLL clock f_{PLL} is used 01 _B The oscillator clock (OSC_HP) f_{OSC} is used 10 _B The Wake-up clock signal f_{WU} is used
RTCCM	2	rw	RTC Clocking Mode 0 _B Asynchronous Mode: The RTC internally operates with f_{RTC} . No register access is possible. 1 _B Synchronous Mode: The RTC internally operates with f_{SYS} clock. Registers can be read and written.
0	[15:3]	r	Reserved Read as 0; should be written with 0.

9.1.7.7 External Clock Control Register

This register control the setting of external clock for pin 2.8 and 7.1.

EXTCON

External Clock Control Register SFR (FF5E_H/AF_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FO EN	FO SS	FORV						0	FO TL	0	SEL				EN
rw	rw	rw						r	rh	r	rw				rw

Field	Bits	Type	Description
EN	0	rw	External Clock Enable 0_B No external clock signal is provided. The signal is tied to zero. 1_B The configured external clock signal is provided as alternate output signal
SEL	[4:1]	rw	External Clock Select Selects the clock signal to be routed to the EXTCLK pin: 0000_B System clock f_{SYS} 0001_B Programmable clock signal f_{OUT} 0010_B PLL output clock f_{PLL} 0011_B Oscillator clock f_{OSC} 0100_B Wake-up clock f_{WU} 0101_B Direct Input clock f_{CLKIN1} 1000_B RTC count clock f_{RTC} All other combination are reserved, do not use.
FOTL	6	rh	Frequency Output Toggle Latch Toggled upon each underflow of FOCNT.
FORV	[13:8]	rw	Frequency Output Reload Value Copied to FOCNT upon each underflow of FOCNT.
FOSS	14	rw	Frequency Output Signal Select 0_B Output of the toggle latch 1_B Output of the reload counter: duty cycle depends on FORV
FOEN	15	rw	Frequency Output Enable 0_B Frequency output generation stops when f_{OUT} is/becomes low. 1_B FOCNT is running, f_{OUT} is gated to pin. First reload after 0 - 1 transition.
0	5, 7	r	Reserved Read as 0; should be written with 0.

9.2 System Timer Function (STM)

The System Timer equips the device with a real time counter function

The STM function can operate on the clock sources described in [System Timer \(STM\) Clock Generation](#).

The STM consists of a 16-bit counter that is able to generate up to two interrupts. Driven by a clock source the counter can be used to count time based events and upon an interrupt trigger based on a time generated out of a clock different than the remaining of the system. A clock function can easily be implemented based on these interrupts in software.

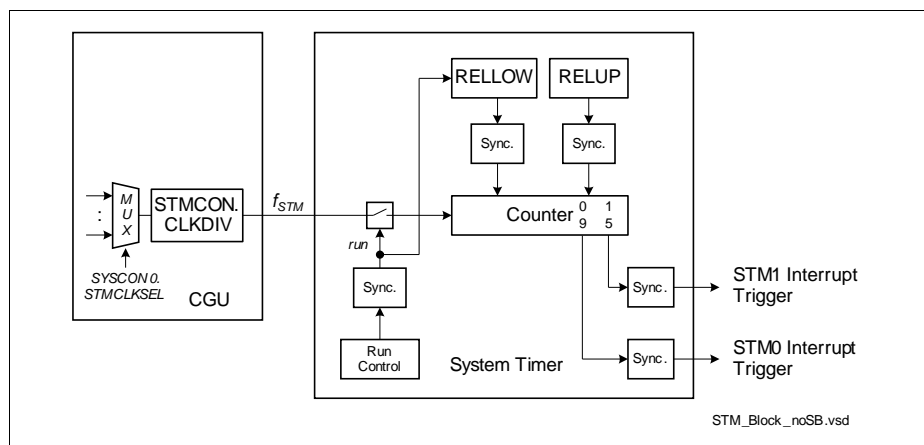


Figure 9-14 STM Block Diagram

Note: The STM0 and STM1 interrupts are enabled by default upon a reset (register INTDIS = 0000_H). It may lead to interrupt requests being triggered at an inappropriate time as described in [Chapter 9.10](#). Hence, it is advised to disable interrupt sources that will not be used via the INTDIS register. In addition, pending request flags (SCU_xIC.IR) need to be cleared before enabling interrupts in interrupt controller.

9.2.1 STM Registers

9.2.1.1 Register STMREL

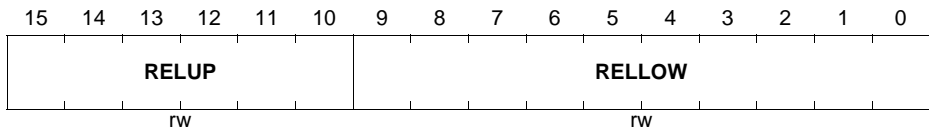
Via this register, the reload value and therefore the period of the STM is defined.

STMREL

STM Reload Register

ESFR (F1A8_H/D4_H)

Reset Value: 0000_H



Field	Bits	Type	Description
RELOW	[9:0]	rw	Reload Lower Value The counter counts up and issues an interrupt trigger when bit 9 changes from 1 _B to 0 _B . Upon this trigger the counter is loaded with the reload value defined by this bit field.
RELUP	[15:10]	rw	Reload Upper Value The counter counts up and issues an interrupt trigger when bit 15 changes from 1 _B to 0 _B . Upon this trigger the counter is loaded with the reload value defined by this bit field and by bit field RELOW.

9.2.1.2 Register STMCON

This register holds the status and control bits for the STM.

STMCON

STM Control Register

ESFR (F1AA_H/D5_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0											CLKDIV			RUN	
r											rw			rw	

Field	Bits	Type	Description
RUN	0	rw	Run Control 0 _B STM is stopped 1 _B STM is operating By setting this bit the STM is started and the reload value STMREL.REL is loaded into the counter.
CLKDIV	[4:1]	rw	Clock Divider for the STM Clock This bit field defines the divider factor of the STM clock input. The selected input clock is divided by $2^{<CLKDIV>}$.
0	[15:5]	r	Reserved Read as 0; should be written with 0.

9.3 Wake-up Timer (WUT)

The Wake-up Timer provides an additional resource to trigger system functions after a specific period of time.

The Wake-up Timer function can operate on the clock sources described in [Wake-up Timer \(WUT\) Clock Generation](#).

The wake-up timer clock f_{WUT} drives a simple counter. All functions are controlled by register WUCR.

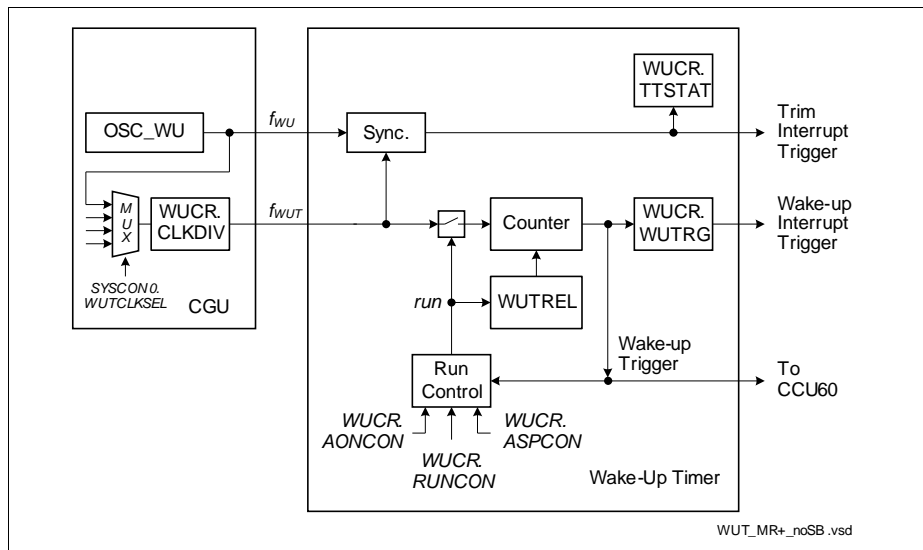


Figure 9-15 Wake-up Timer Logic

9.3.1 Wake-up Timer Operation

The Wake-up Timer start and stop is controlled by the Run Control logic. The timer can be started in the following way:

- bit $WUCR.RUN$ is set

When the timer is started the prescaler is reset and the counter starts to count down.

The wake-up interval counter is clocked with f_{WUT} and counts down until it reaches zero. It then generates a wake-up trigger and sets bit $WUCR.WUTRG$.

The timer is stopped in the following ways:

- bit $WUCR.RUN$ is cleared
- bit $WUCR.ASP$ is set AND a wake-up trigger is generated

If the counter is not stopped by its zero trigger it continues counting down from $WUTREL$.

Determination of Wake-up Period

The actual frequency of the trimmed current controlled wake-up clock (OSC_WU) can be measured prior to entering power-save mode in order to adjust the number of clock cycles to be counted (value written to the counter) and so to define the time until wake-up. The period of the the OSC_WU can be measured by evaluating the (synchronized) trigger that can generate interrupt requests or can be monitored with bit WUCR.TTSTAT.

As using an interrupt together with software contain some uncertainty there is a second way to determine the wake-up period. The wake-up triggers generated by the WUT are forwarded to the CCU60 and can there be evaluated compared to the accurate system clock.

Note: The Wake-up Timer interrupts are enabled by default upon a reset (register INTDIS = 0000_H). It may lead to interrupt requests being triggered at an inappropriate time as described in [Chapter 9.10](#). Hence, it is advised to disable interrupt sources that will not be used via the INTDIS register. In addition, pending request flags (SCU_xIC.IR) need to be cleared before enabling interrupts in interrupt controller.

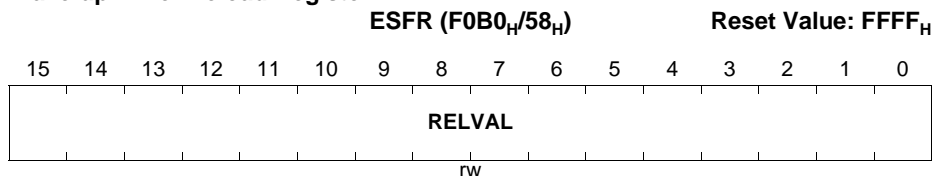
9.3.2 WUT Registers

9.3.2.1 Register WUTREL

This register configures the reload value of the counter.

WUTREL

Wake-up Timer Reload Register



Field	Bits	Type	Description
RELVAL	[15:0]	rw	Wake-up Timer Reload Value The WUT counter is reloaded with this value and starts to count down when the timer is started.

9.3.2.2 Register WUCR

This register the status and control bits for the WUT.

WUCR

Wake-up Control Register

ESFR (F1B0_H/D8_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WU TRG	TTS TAT	CLKDIV			ASP	AON	RUN	CLR TRG	0	ASP CON	AON CON		RUN CON		
rh	rh	rw			rh	rh	rh	w	r	w	w		w		

Field	Bits	Type	Description
RUNCON	[1:0]	w	Control Field for RUN 00 _B No action 01 _B Set bit RUN 10 _B Clear bit RUN 11 _B Reserved, do not use this combination <i>Note: This bit is always read as 0.</i>
AONCON	[3:2]	w	Control Field for AON 00 _B No action 01 _B Reserved, do not use this combination 10 _B Clear bit AON 11 _B Reserved, do not use this combination <i>Note: This bit is always read as 0.</i>
ASPCON	[5:4]	w	Control Field for ASP 00 _B No action 01 _B Set bit ASP 10 _B Clear bit ASP 11 _B Reserved, do not use this combination <i>Note: This bit is always read as 0.</i>
CLRTRG	7	w	Clear Bit WUTRG 0 _B No action 1 _B Clear bit WUTRG <i>Note: This bit is always read as 0.</i>

System Control Unit (SCU)

Field	Bits	Type	Description
RUN	8	rh	Run Indicator 0_B Wake-up counter is stopped 1_B Wake-up counter is counting down <i>Note: Clearing this bit via a write action to bit field RUNCON stops the WUT after four cycles of f_{WUT}.</i>
AON	9	rh	Auto-Start Indicator 0_B Wake-up counter is started by software only 1_B Reserved, do not use this combination <i>Note: This bit is cleared by writing 01_B to bit field AONCON.</i>
ASP	10	rh	Auto-Stop Indicator 0_B Wake-up counter runs continuously 1_B Wake-up counter stops after generating a trigger when reaching zero
CLKDIV	[13:11]	rw	Clock Divider for the WUT Clock This bit field defines the divider factor of the WUT clock input. The selected input clock is divided by $2^{<CLKDIV>}$.
TTSTAT	14	rh	Trim Trigger Status 0_B No trim trigger event is active. No trim interrupt trigger is generated. 1_B A trim trigger event is active. A trim interrupt trigger is generated. <i>Note: This bit is not valid if $f_{WUT} = f_{WU}$ is configured by SYSCON0.WUTCLKSEL</i>
WUTRG	15	rh	WUT Trigger Indicator 0_B No trigger event has occurred since WUTRG has been cleared last. No interrupt trigger is generated. 1_B A wake-up trigger event has occurred. A wake-up interrupt trigger is generated.
0	6	r	Reserved Read as 0; should be written with 0.

Note: The bits in the upper byte of register WUCR indicate the current status of the wake-up counter logic. They are not influenced by a write access, but are controlled by their associated control fields (lower byte) or by hardware.

System Control Unit (SCU)

The control bit(field)s in the lower byte of register WUCR determine the state of the status bits (upper byte) of the wake-up counter logic. Setting bits by software triggers the associated action, writing 0 has no effect.

9.4 Reset Operation

All resets are generated by the Reset Control Block. It handles the control of the reset triggers as well as the length of a reset and the reset timing. A reset leads the system, or a part of the system depending on the reset, to a initialization into a defined state.

9.4.1 Reset Architecture

The XC27x8X contains a very sophisticated reset architecture to offer the greatest amount of flexibility for the support of different applications. The reset architecture supports the different power domains.

Different reset types for the complete system are supported.

9.4.1.1 Device Reset Hierarchy

The device reset hierarchy is divided according to the power domains (see [Chapter 9.6](#)) into following linked levels:

Level 1: I/O domain (power domain DMP_B)

Level 2: System power domain DMP_M

Level 3: System power domain DMP_1

If a power domain (level) is deactivated all resets of the deactivated level and all resets of all lower power domains are asserted.

9.4.1.2 Reset Types

The following summary shows the different reset types.

Power Reset

- Power-on Reset
This reset leads to a defined state of the complete system. This reset should only be requested on a real power-on event and not by any non power related event.
- Power Reset for DMP_M and DMP_1 power domains
This reset regains data consistency upon a power fail in the DMP_M or DMP_1 power domains.

Functional / User Reset

- Debug Reset
This reset leads to a defined state of the complete debug system.
- Internal Application Reset
This reset leads to a defined state of the complete application system with the following parts: all peripherals (except the RTC), the CPU and partially the SCU and the flash memory.

- **Application Reset**

This reset leads to a defined state of the complete application system with the following parts: all peripherals (except the Ports and the RTC), the CPU and partially the SCU and the flash memory.

After a reset has been executed, the Reset Status registers RSTSTATx indicate the latest reset that has occurred.

To identify the type and the trigger of the latest reset registers **RSTSTAT0**, **RSTSTAT1** and **SWDCON1** may be evaluated according to **Table 9-2**. The latest reset that has occurred is always the reset of the highest type. If two reset triggers of the same type are indicated, this means that the two triggers have been active at the same time. If two or more reset triggers of a different type are reported, always the reset of the highest type is the latest one.

Table 9-2 Identification of a Reset

Type of Reset (in hierarchical order, highest on top)	Identification
Power-on Reset	SWDCON1.PON = 1 _B RSTSTAT1.STM = 11 _B RSTSTAT1.ST1 = 11 _B Further action: clear PON bit to be able to identify a Power Reset for DMP_M and DMP_1 power domains.
Power Reset for DMP_M and DMP_1 power domains	SWDCON1.PON = 0 _B (unchanged after clearing) RSTSTAT1.STM = 11 _B RSTSTAT1.ST1 = 11 _B
Internal Application Reset	RSTSTAT1.ST1 = 00 _B any bit field y in RSTSTATx.y = 10 _B
Application Reset	RSTSTAT1.ST1 = 00 _B any bit field y in RSTSTATx.y = 11 _B (except RSTSTAT1.ST1 and RSTSTAT1.STM)

The algorithm depicted in **Figure 9-16** shows a sequence to detect the type of the reset comprising the conditions in **Table 9-2**.

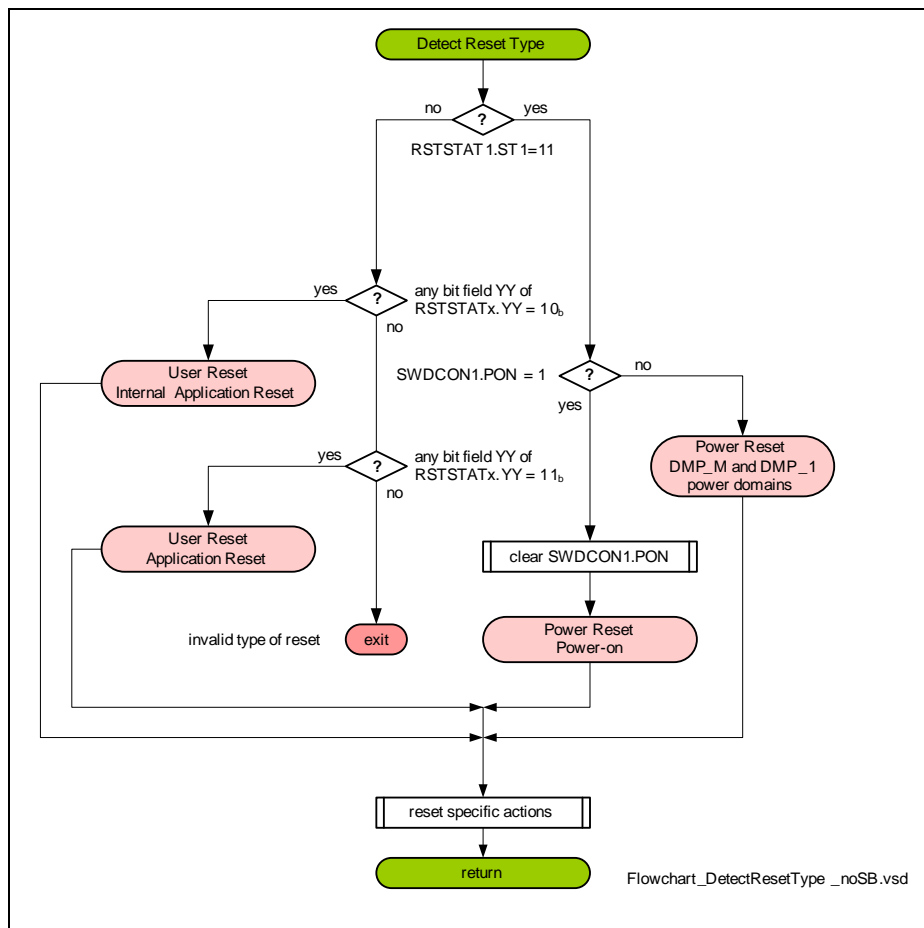


Figure 9-16 Algorithm for the Detection of the Type of a Reset

9.4.2 General Reset Operation

A reset is generated if an enabled reset request trigger is asserted. Most reset request triggers can be configured for the reset type it should initiate. No action (disabled) is one possible configuration and can be selected for a reset request trigger by setting the respective bit field in a Reset Configuration Register to 00_B. The debug reset can only be requested by dedicated reset request triggers and can not be selected via a Reset Configuration Register. For more information see also registers **RSTCON0** and **RSTCON1**.

The duration of a reset is defined by two independent counters. One counter for the System and Application Reset types and one separate counter for the debug reset. A separate counter for the debug reset was implemented to allow a non-intrusive adaptation of the reset length to the debugger needs without modification of the application setting.

9.4.2.1 Reset Counters (RSTCNTA and RSTCNTD)

RSTCNTA is the reset counter that controls the reset length for all application relevant resets (Internal Application Reset, and Application Reset). RSTCNTD is the reset counter that controls the reset length for the debug reset.

The reset counters control the length of the internal resets. This can be used to configure the duration of a reset output via the ESRx pins, so this matches with the reset input requirements of external blocks connected to these signals.

A reset counter RSTCNT is an 8-bit counter counting down from the reload value defined by **RSTCNTCON.RELx** (x = A or D). The counter is started by the reset control block as soon as a reset request trigger condition becomes active (for more information see **Table 9-3** and **Table 9-4**). Whether the counter has to be started or not depends on the reset request trigger and whether the counter is already active or not. In case of that the counter is inactive, not counting down, it is always started. While the counter is already active it depends on the reset type of the new reset request trigger that was asserted anew if the counter is restarted or not. This behavior is summarized in **Table 9-3** and **Table 9-4**.

Table 9-3 Restart of RSTCNTA

Reset Active	New Reset Trigger			
	Power-On	Debug Reset	Internal Application Reset	Application Reset
Internal Application Reset	Restart with default delay	No Change	No Change	No Change
Application Reset	Restart with default delay	No Change	Restart with defined delay	No Change

Table 9-4 Restart of RSTCNTD

Reset Active	New Reset Trigger			
	Power-On	Debug Reset	Internal Application Reset	Application Reset
Debug Reset	Restart with default delay	No Change	No Change	No Change

The reset counters RSTCNTx ensure a configurable minimum duration of a generated reset. If a reset request trigger remains asserted after the respective counter has counted down, the counter is not started again, instead the reset control block keeps the reset asserted until the reset request trigger is deasserted.

9.4.2.2 De-assertion of a Reset

The reset of a dedicated type is de-asserted when all of the following conditions are fulfilled:

- The reset counter has been expired (reached zero).
- No reset request trigger that is configured to generate a reset of the dedicated type (or higher) is currently asserted.

Example1

Reset request trigger A is asserted and leads to an Application Reset. If the reset request trigger is de-asserted before RSTCNTA reached zero the Application Reset is de-asserted when RSTCNTA reaches zero. If the reset request trigger is de-asserted after RSTCNTA reached zero the Application Reset is de-asserted when the reset request trigger is de-asserted.

Example2

Reset request trigger A is asserted and leads to an Application Reset. Reset request trigger A is de-asserted before RSTCNTA reached zero. Reset request trigger B is asserted after reset request trigger A but before RSTCNTA reaches zero. Reset request trigger B is also configured to result in a Application Reset. If the reset request trigger B is de-asserted before RSTCNTA reached zero the Application Reset is de-asserted when RSTCNTA reaches zero. If the reset request trigger B is de-asserted after RSTCNTA reached zero the Application Reset is de-asserted when the reset request trigger B is de-asserted.

9.4.3 Debug Reset Assertion

Unlike the other reset types a Debug Reset can only be asserted if the following two conditions are valid:

- A reset request trigger is asserted that request a debug reset
- An Application Reset is already active in the system

9.4.4 Coupling of Reset Types

The different reset types are coupled for a better usage:

- The assertion of a Power-on Reset automatically asserts also the following reset types:
 - Debug Reset
 - Internal Application Reset
 - Application Reset
- The assertion of an Internal Application Reset automatically asserts also the following reset type:
 - Application Reset

9.4.5 Reset Request Trigger Sources

The following overview summarizes the different reset request trigger sources within the system.

Power-On Reset Pin $\overline{\text{PORST}}$

A Power-on Reset is requests asynchronously, by driving the $\overline{\text{PORST}}$ pin low.

Supply Watchdog (SWD)

If the power supply for I/O domain is below the value required for proper functionality, a non-synchronized reset request trigger is generated if the SWD reset generation is enabled. This ensures a reproducible behavior in the case of power-fail. This can also be used to restart the system without the usage of the $\overline{\text{PORST}}$ pin. As long as the I/O power domain does not get the required voltage level the system is held in the reset.

Core Power Validation (PVC_M and PVC_1)

If the core power supply is below the value required for proper functionality of the main power domain (PVC_M), a reset request trigger can be forwarded to the system. The generation of a Power-on Reset is configured by bit $\text{PVC_MCON0.L1RSTEN} = 1_{\text{B}}$. If the bit $\text{PVC_MCON0.L1RSTEN} = 1_{\text{B}}$ a request trigger is asserted for PVC_M1 upon a level check match. If the bit $\text{PVC_MCON0.L2RSTEN} = 1_{\text{B}}$ a request trigger is asserted for PVC_M2 upon a level check match.

If the core power supply is below the value required for proper functionality of the application power domain (PVC_1), a reset request trigger can be forwarded to the system. The generation of a Power-on Reset (Application Power Domain only) is configured by bit $\text{PVC1CON0.L1RSTEN} = 1_{\text{B}}$. If bit $\text{PVC1CON0.L1RSTEN} = 1_{\text{B}}$ a request trigger is asserted for PVC_11 upon a level check match. If the bit $\text{PVC1CON0.L2RSTEN} = 1_{\text{B}}$ a request trigger is asserted for PVC_12 upon a level check match.

For more information about the Power Validation Circuit see [Chapter 9.6.2](#).

$\overline{\text{ESRx}}$

An $\overline{\text{ESRx}}$ reset request trigger leads to a configurable reset. The type of reset can be configured via [RSTCON1](#).ESRx.

The pins $\overline{\text{ESRx}}$ can serve as an external reset input as well as a reset output (open drain) for Internal Application and Application Resets. Furthermore, several GPIO pad triggers, that can be enabled additionally via register ESREXCONx ($x = 1, 2$), interfere with the ESR pin function. GPIO and $\overline{\text{ESRx}}$ pin triggers can be enabled/disabled individually and are combined for the reset trigger generation.

System Control Unit (SCU)

If pin $\overline{\text{ESRx}}$ is enabled as reset output and the input level is low while the output stage is disabled (indicating that it is still driven low externally), the reset circuitry holds the chip in reset until a high level is detected on $\overline{\text{ESRx}}$. Minimum value for `RSTCNTCON.RELA` must be the reset value.

Note: The reset output is only driven low for the duration the reset counter `RSTCNTA` is active. During a possible reset extension the reset output is no longer driven.

Software

A software reset request trigger leads to a configurable reset. The type of reset can be configured via `RSTCON0.SW`.

Watchdog Timer

A WDT reset request trigger leads to a configurable reset. The type of reset can be configured via `RSTCON1.WDT`. A WDT reset is requested on a WDT overflow event. For more information see [Chapter 9.12](#).

CPU

A CPU reset request trigger leads to a configurable reset. The type of reset can be configured via `RSTCON0.CPU`. A CPU reset is requested when instruction `SRST` is executed.

Memory Parity

A MP reset request trigger leads to a configurable reset. The type of reset can be configured via `RSTCON1.MP`. For more information see [Chapter 9.14.2](#).

OCDS Block

The OCDS block has several options to request different reset types:

1. A Debug Reset either via the OCDS reset function or via bit `CBS_OJCONF.RSTCL1` AND `CBS_OJCONF.RSTCL3`
2. An Internal Application Reset via bit `CBS_OJCONF.RSTCL2`
3. An Application Reset via bit `CBS_OJCONF.RSTCL3`

9.4.5.1 Reset Sources Overview

The connection of the reset sources and the activated reset types are shown in [Table 9-5](#).

Table 9-5 Effects of Reset Types for Reset Activation

Reset Request Trigger	Application Reset	Internal Application Reset	Debug Reset
PORST	Activated	Activated	Activated
SWD	Activated	Activated	Activated
PVC_M1	Activated	Activated	Activated
PVC_M2	Activated	Activated	Activated
PVC_11	Activated	Activated	Activated
PVC_12	Activated	Activated	Activated
ESR0	Configurable	Configurable	Not Activated
ESR1	Configurable	Configurable	Not Activated
ESR2	Configurable	Configurable	Not Activated
WDT	Configurable	Configurable	Not Activated
SW	Configurable	Configurable	Not Activated
CPU	Configurable	Configurable	Not Activated
MP	Configurable	Configurable	Not Activated
OCDS Reset	Not Activated	Not Activated	Activated ¹⁾
CBS_OJCONF.RSTCL1	Not Activated	Not Activated	Activated ¹⁾
CBS_OJCONF.RSTCL2	Activated	Activated	Not Activated
CBS_OJCONF.RSTCL3	Activated	Not Activated	Not Activated

1) Only if an Application Reset is active or is requested in parallel.

9.4.6 Module Reset Behavior

Table 9-6 lists how the various functions of the XC27x8X are affected through a reset depending on the reset type. A "X" means that this block has at least some register/bits that are affected by this reset type.

Table 9-6 Effect of Reset on Device Functions

Module / Function		Application Reset	Internal Application Reset	Debug Reset
CPU Core		X	X	X
Peripherals (except SCU and RTC)		X	X	X
SCU		X	Not affected	Not affected
RTC		Not affected	Not affected	X
On-chip Static RAMs¹⁾	DPRAM	Not affected, reliable	Not affected, reliable	Not affected, reliable
	PSRAM	Not affected, reliable	Not affected, reliable	Not affected, reliable
	DSRAM	Not affected, reliable	Not affected, reliable	Not affected, reliable
Flash Memory		X ²⁾	X ²⁾	Not affected, reliable
JTAG Interface		Not affected	Not affected	Not affected
OCDS		Not affected	Not affected	X
Oscillator, PLL		Not affected	Not affected	Not affected
Port Pins		Not affected ³⁾	X	Not affected
Pins ESRx		X ⁴⁾	X ⁴⁾	Not affected

1) Reliable here means that also the redundancy is not affected by the reset.

2) Parts of the flash memory block are only reset by a Power-on Reset. For more detail see the flash chapter.

3) The reset of the internal peripherals can change the data driven on the outputs, see also description of port behavior in section "Reset Behavior" in chapter "Parallel Ports".

4) The behavior depends on the configuration of ESRCFGx.PC (see [Table 9-9](#)).

9.4.7 Reset Controller Registers

9.4.7.1 Status Registers

After a reset has been executed, the Reset Status registers provide information on the type of the last reset. The reset status registers are updated upon each reset.

RSTSTAT0

Reset Status 0 Register

ESFR (F0B2_H/59_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SW		CPU		0											
rh		rh		r											

Field	Bits	Type	Description
CPU	[13:12]	rh	CPU Reset Type Status 00 _B The CPU reset trigger was not relevant for the last reset 01 _B Reserved 10 _B The CPU reset trigger was relevant for the last reset. Internal Application and Application Resets were generated. 11 _B The CPU reset trigger was relevant for the last reset. Application Reset was generated.
SW	[15:14]	rh	Software Reset Type Status 00 _B The Software reset trigger was not relevant for the last reset 01 _B Reserved 10 _B The Software reset trigger was relevant for the last reset. Internal Application and Application Resets were generated. 11 _B The Software reset trigger was relevant for the last reset. Application Reset was generated.
0	[11:0]	r	Reserved Read as 0; should be written with 0.

RSTSTAT1

Reset Status 1 Register

ESFR (F0B4_H/5A_H)

Reset Value: F000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ST1		STM		0		MP		WDT		ESR2		ESR1		ESR0	
rh		rh		r		rh		rh		rh		rh		rh	

Field	Bits	Type	Description
ESR0	[1:0]	rh	ESR0 Reset Status 00 _B The <u>ESR0</u> reset trigger was not relevant for the last reset 01 _B Reserved 10 _B The <u>ESR0</u> reset trigger was relevant for the last reset. Internal Application, and Application Resets were generated. 11 _B The <u>ESR0</u> reset trigger was relevant for the last reset. Application Reset was generated.
ESR1	[3:2]	rh	ESR1 Reset Status 00 _B The <u>ESR1</u> reset trigger was not relevant for the last reset 01 _B Reserved 10 _B The <u>ESR1</u> reset trigger was relevant for the last reset. Internal Application, and Application Resets were generated. 11 _B The <u>ESR1</u> reset trigger was relevant for the last reset. Application Reset was generated.
ESR2	[5:4]	rh	ESR2 Reset Status 00 _B The <u>ESR2</u> reset trigger was not relevant for the last reset 01 _B Reserved 10 _B The <u>ESR2</u> reset trigger was relevant for the last reset. Internal Application, and Application Resets were generated. 11 _B The <u>ESR2</u> reset trigger was relevant for the last reset. Application Reset was generated.

System Control Unit (SCU)

Field	Bits	Type	Description
WDT	[7:6]	rh	WDT Reset Status 00 _B The WDT reset trigger was not relevant for the last reset 01 _B Reserved 10 _B The WDT reset trigger was relevant for the last reset. Internal Application, and Application Resets were generated. 11 _B The WDT reset trigger was relevant for the last reset. Application Reset was generated.
MP	[9:8]	rh	MP Reset Status 00 _B The MP reset trigger was not relevant for the last reset 01 _B Reserved 10 _B The MP reset trigger was relevant for the last reset. Internal Application, and Application Resets were generated. 11 _B The MP reset trigger was relevant for the last reset. Application Reset was generated.
STM	[13:12]	rh	Power-on for DMP_M Reset Status 00 _B The power-on reset for DMP_M reset trigger was not relevant for the last reset 01 _B The power-on reset for DMP_M reset trigger was not relevant for the last reset 10 _B The power-on reset for DMP_M reset trigger was not relevant for the last reset 11 _B The power-on reset for DMP_M reset trigger was relevant for the last reset
ST1	[15:14]	rh	Power-on for DMP_1 Reset Status 00 _B The power-on reset for DMP_1 reset trigger was not relevant for the last reset 01 _B The power-on reset for DMP_1 reset trigger was not relevant for the last reset 10 _B The power-on reset for DMP_1 reset trigger was not relevant for the last reset 11 _B The power-on reset for DMP_1 reset trigger was relevant for the last reset
0	[11:10]	r	Reserved Read as 0; should be written with 0.

RSTSTAT2

Reset Status 2 Register

ESFR (F0B6_H/5B_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0						OJCONF3		OJCONF2		OJCONF1		OJCONF0		DB	
r						rh		rh		rh		rh		rh	

Field	Bits	Type	Description
DB	[1:0]	rh	Debug Reset Status 00 _B The DB reset trigger was not relevant for the last reset 01 _B The DB reset trigger was not relevant for the last reset 10 _B The DB reset trigger was not relevant for the last reset 11 _B The DB reset trigger was relevant for the last reset
OJCONF0	[3:2]	rh	OJCONF0 Reset Status Value undefined; should be written with 0.
OJCONF1	[5:4]	rh	OJCONF1 Reset Status 00 _B The OJCONF1 reset trigger was not relevant for the last reset 01 _B The OJCONF1 reset trigger was not relevant for the last reset 10 _B The OJCONF1 reset trigger was not relevant for the last reset 11 _B The OJCONF1 reset trigger was relevant for the last reset. Debug Reset was generated.
OJCONF2	[7:6]	rh	OJCONF2 Reset Status 00 _B The OJCONF2 reset trigger was not relevant for the last reset 01 _B The OJCONF2 reset trigger was not relevant for the last reset 10 _B The OJCONF2 reset trigger was relevant for the last reset. Internal Application, and Application Resets were generated. 11 _B The OJCONF2 reset trigger was not relevant for the last reset

System Control Unit (SCU)

Field	Bits	Type	Description
OJCONF3	[9:8]	rh	OJCONF3 Reset Status 00 _B The OJCONF3 reset trigger was not relevant for the last reset 01 _B The OJCONF3 reset trigger was not relevant for the last reset 10 _B The OJCONF3 reset trigger was not relevant for the last reset 11 _B The OJCONF3 reset trigger was relevant for the last reset. Application Reset was generated.
0	[3:2], [15:10]	r	Reserved Read as 0; should be written with 0.

9.4.7.2 Configuration Registers

These registers allow the behavioral configuration for the various reset trigger sources.

RSTCON0

Reset Configuration 0 Register ESFR (F0B8_H/5C_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SW		CPU		0											
rw		rw		rw											

Field	Bits	Type	Description
CPU	[13:12]	rw	CPU Reset Type Selection This bit field defines which reset types are generated by a CPU reset request trigger. 00 _B No reset is generated 01 _B Reserved, do not use this combination 10 _B Internal Application, and Application Resets are generated 11 _B Application Reset is generated
SW	[15:14]	rw	Software Reset Type Selection This bit field defines which reset types are generated by a software reset request trigger. 00 _B No reset is generated 01 _B Reserved, do not use this combination 10 _B Internal Application, and Application Resets are generated 11 _B Application Reset is generated
0	[11:0]	rw	Reserved Must be written with reset value 0.

RSTCON1

Reset Configuration 1 Register ESRF (F0BA_H/5D_H)

Reset Value: 0002_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0						MP		WDT		ESR2		ESR1		ESR0	
rw						rw		rw		rw		rw		rw	

Field	Bits	Type	Description
ESR0	[1:0]	rw	ESR0 Reset Type Selection This bit field defines which reset types are generated by a ESR0 reset request trigger. 00 _B No reset is generated 01 _B Reserved, do not use this combination 10 _B Internal Application, and Application Resets are generated 11 _B Application Reset is generated
ESR1	[3:2]	rw	ESR1 Reset Type Selection This bit field defines which reset types are generated by a ESR1 reset request trigger. 00 _B No reset is generated 01 _B Reserved, do not use this combination 10 _B Internal Application, and Application Resets are generated 11 _B Application Reset is generated
ESR2	[5:4]	rw	ESR2 Reset Type Selection This bit field defines which reset types are generated by a ESR2 reset request trigger. 00 _B No reset is generated 01 _B Reserved, do not use this combination 10 _B Internal Application, and Application Resets are generated 11 _B Application Reset is generated

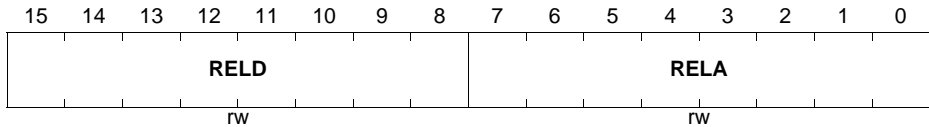
System Control Unit (SCU)

Field	Bits	Type	Description
WDT	[7:6]	rw	WDT Reset Type Selection This bit field defines which reset types are generated by a WDT reset request trigger. 00 _B No reset is generated 01 _B Reserved, do not use this combination 10 _B Internal Application, and Application Resets are generated 11 _B Application Reset is generated
MP	[9:8]	rw	MP Reset Type Selection This bit field defines which reset types are generated by a MP reset request trigger. 00 _B No reset is generated 01 _B Reserved, do not use this combination 10 _B Internal Application, and Application Resets are generated 11 _B Application Reset is generated
0	[15:10]	rw	Reserved Should be written with 0.

RSTCNTCON

Reset Counter Control RegisterESFR (F1B2_H/D9_H)

Reset Value: 0A0A_H



Field	Bits	Type	Description
RELA	[7:0]	rw	Application Reset Counter Reload Value This bit field defines the reload value of RSTCNTA. This value is always used when counter RSTCNTA is started. This counter value is used for Internal Application, and Application Resets. In case of an ESRx reset the counter value must be not less than the reset value.
RELD	[15:8]	rw	Debug Reset Counter Reload Value This bit field defines the reload value of RSTCNTD. This value is always used when counter RSTCNTD is started. This counter value is used for the Debug Reset. In case of an ESRx reset the counter value must be not less than the reset value.

Software Reset Control Register

This register controls the software reset operation.

SWRSTCON

Software Reset Control RegisterESFR (F0AE_H/57_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SWCFG								0						SW RST REQ	SW BOOT
rw								r						w	rw

Field	Bits	Type	Description
SWBOOT	0	rw	Software Boot Configuration Selection 0 _B Bit field STSTAT.HWCFCG is not updated with the content of SWCFG upon an Application Reset 1 _B Bit field STSTAT.HWCFCG is updated with the content of SWCFG upon an Application Reset
SWRSTREQ	1	w	Software Reset Request 0 _B No software reset is requested 1 _B A software reset request trigger is generated <i>Note: This bit is always read as 0.</i>
SWCFG	[15:8]	rw	Software Boot Configuration A valid software boot configuration (also different from the external applied hardware configuration) can be specified with these bits. The configuration encoding is equal to the HWCFCG encoding in register STSTAT.
0	[7:2]	r	Reserved Read as 0; should be written with 0.

9.5 External Service Request (ESR) Pins

The $\overline{\text{ESR}}$ pins serve as multi-functional pins for an amount of different options:

- Act as reset trigger input
- Act as reset output
- Act as trap input
- Act as trigger input for the GSC
- Overlay with other product functions
- Independent pad configuration

9.5.1 General Operation

Each $\overline{\text{ESR}}$ pin is equipped with an edge detection that allows the selection of the edges used as triggers. One, both, or no edge can be selected via bit field ESRCFGx.SEDCON if a clock is active. Additionally, there is a digital (3-stage median) filter (DF) to suppress spikes. The signal at $\overline{\text{ESR}}_x$ pin has to be held at the active signal level for at least 2 system clock cycles (f_{SYS}) in order to generate a trigger. The digital filter can be disabled by clearing bit ESRCFGx.DFEN .

Each $\overline{\text{ESR}}_x$ pin can be individually configured.

If an $\overline{\text{ESR}}$ trigger is generated please note that triggers for all purposes (reset, trap, GSC, and non SCU module functions) are generated. If some of the actions resulting out of such a trigger should not occur this has to be disabled by each feature for its own.

The pins that should be used as trigger input for an ESR operation have to be configured as input pin.

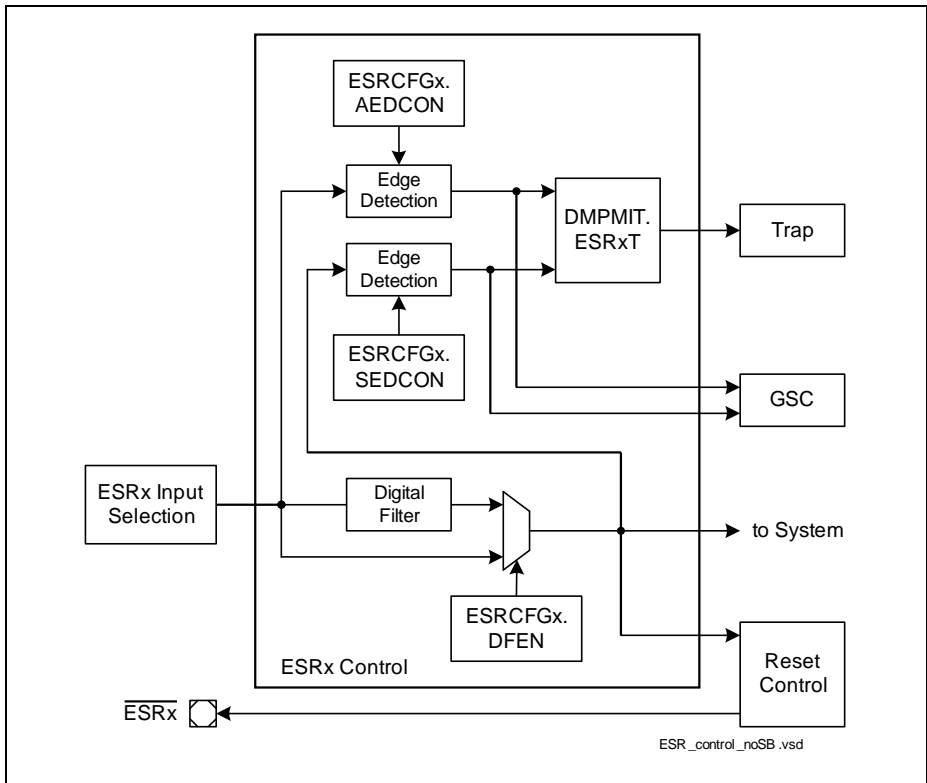


Figure 9-17 ESRx Control

Furthermore, an overlay with other product functions (i.e. inputs of serial interfaces) can be configured via register `ESREXCONx` to trigger ESR operations. The conjunction of the inputs (logically AND) are used for the trigger generation. Thus, if more than one pin shall be used for ESR trigger generation, then any signal at the respective pin must have an inactive high level. In addition, it is possible to invert some inputs to support active high levels.

To extend the overlay possibilities the conjugated inputs of the ESRx input selection structure are combined to one common event in a second AND gate level with the ESR input stage and the output of the combined inputs of the other input conjugation block, if enabled (`ESREXCONx.ESRIN12EN`). This allows all possible inputs to trigger an ESR function even if the second ESR logic is used for other purposes.

Pin `ESR0` does not offer an overlay with other product functions.

For information which other peripheral input signal is on an ESR overlay pin see [Chapter 9.5.1.5](#).

The following figure shows the the ESR Input selection function for $\overline{\text{ESR1}}$ and $\overline{\text{ESR2}}$.

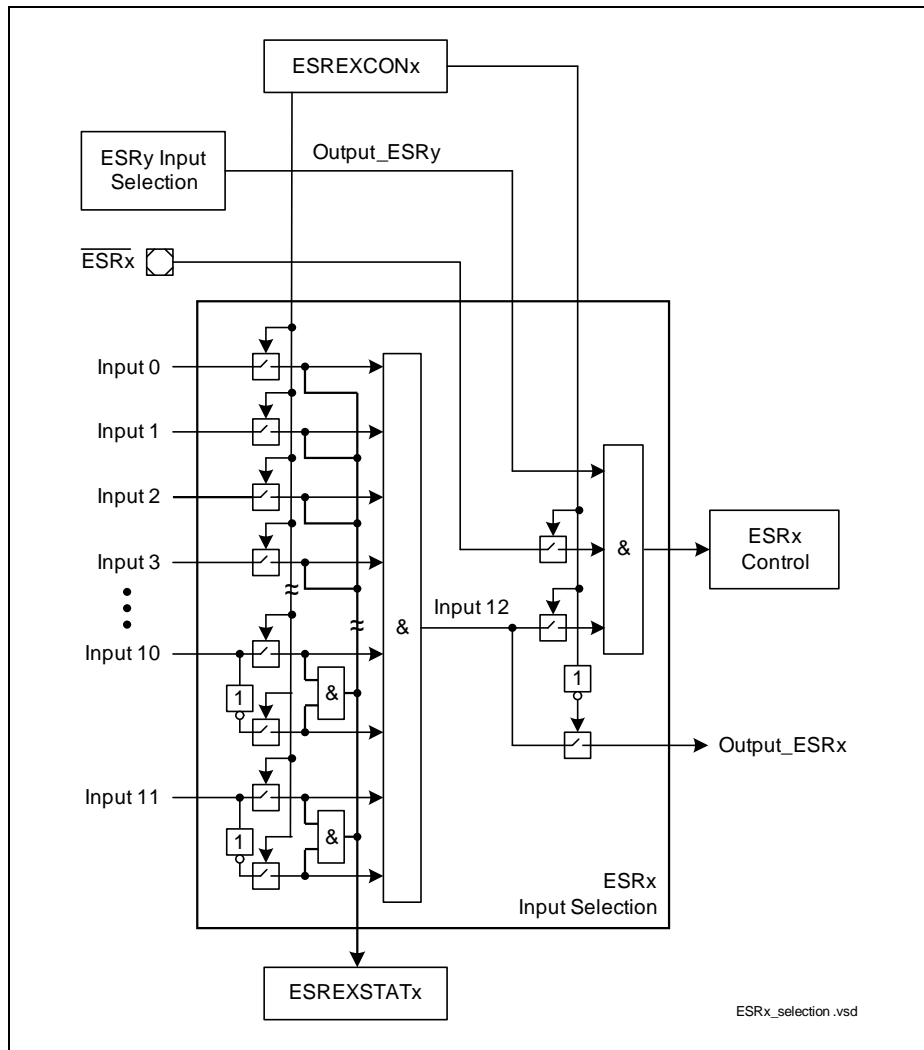


Figure 9-18 ESRx Input Selection

System Control Unit (SCU)

Up to three $\overline{\text{ESR}}$ pins ($\overline{\text{ESR0}}/\overline{\text{ESR1}}/\overline{\text{ESR2}}$) are available. The availability of pins $\overline{\text{ESR1}}$ and $\overline{\text{ESR2}}$ is device and package dependent and is described in the data sheet.

Even if pin $\overline{\text{ESR1}}$ or $\overline{\text{ESR2}}$ are not available in the device an overlay with other product functions (i.e. inputs of serial interfaces) can be configured via register **ESREXCON1** **ESREXCON2** to trigger ESR operations.

9.5.1.1 $\overline{\text{ESR}}$ as Reset Input

The pins $\overline{\text{ESR}}_x$ can serve as an external reset input as well as a reset output (open drain) for Internal Application and Application Resets. Additionally several GPIO pad triggers that can be enabled additionally via register ESREXCON_x interfere with the $\overline{\text{ESR}}$ pin function. GPIO and $\overline{\text{ESR}}$ pin triggers can be enabled/disabled individually and are combined for the reset trigger generation. For more information about the reset system see [Chapter 9.4](#).

Note: The reset output is only asserted for the duration the reset counter RSTCNTA is active. During a possible reset extension the reset output is not longer asserted.

9.5.1.2 $\overline{\text{ESR}}$ as Reset Output

If pin $\overline{\text{ESR}}_x$ is enabled as reset output and the input level is low while the output stage is disabled (indicating that it is still driven low externally), the reset circuitry holds the chip in reset until a high level is detected on $\overline{\text{ESR}}_x$. The internal output stage drives a low level during reset only while RSTCNTA is active. It deactivates the output stage when the time defined by RSTCNTCON.RELA has passed. For more information about the reset system see [Chapter 9.4](#).

9.5.1.3 $\overline{\text{ESR}}$ as Trap Trigger

The $\overline{\text{ESR}}$ can request traps. The control mechanism if and which trap is requested is located in the trap control logic. For more information see [Chapter 9.13](#).

9.5.1.4 $\overline{\text{ESR}}$ as Trigger Input for the GSC

The $\overline{\text{ESR}}$ can be used to request a change in the Control Mode. For more information see [Chapter 9.7](#).

9.5.1.5 Overlay with other Product Functions

Additionally other port inputs (e.g. serial communication input) can be used to generate $\overline{\text{ESR}}$ operations. For pins $\overline{\text{ESR}}_1$ and $\overline{\text{ESR}}_2$ an overlay with the $\overline{\text{ESR}}_x$ inputs listed in [Table 9-7](#) and [Table 9-8](#) is possible. Even if an $\overline{\text{ESR}}_x$ pin is not available an overlay with the $\overline{\text{ESR}}_x$ inputs listed in the tables is possible. The $\overline{\text{ESR}}_x$ logic part is fully functional. Pin $\overline{\text{ESR}}_0$ does not offer an overlay with other product functions.

The availability of pins $\overline{\text{ESR}}_1$ and $\overline{\text{ESR}}_2$ is device and package dependent. It is described in the data sheet.

Table 9-7 ESR1 Input Connection

Input	Connected to
Input 0	Port 2.4
Input 1	Port 3.0
Input 2	Port 10.0
Input 3	Port 1.0
Input 4	Port 1.2
Input 5	Port 2.1
Input 6	Port 6.1
Input 7	Port 11.0
Input 8	Port 4.1
Input 9	Port 10.4
Input 10	Port 2.5
Input 11	Port 0.0

Table 9-8 ESR2 Input Connection

Input	Connected to
Input 0	Port 2.3
Input 1	Port 7.0
Input 2	Port 10.14
Input 3	Port 1.1
Input 4	Port 1.3
Input 5	Port 2.2
Input 6	Port 2.6
Input 7	Port 2.7
Input 8	Port 0.4
Input 9	XTAL 1
Input 10	Port 4.5
Input 11	Port 10.8

This feature can be used for various applications:

System Control Unit (SCU)

- Wake-up from a Clock-off Mode on an external Interrupt or CCU6x trigger and on a CAN or USIC operation
- Request to enter a Clock-off Mode on an external Interrupt or CCU6x trigger and on a CAN or USIC operation
- Stop input for the CCU6x modules on an external event

For more information about the external interrupt trigger see [Chapter 9.9](#).

9.5.1.6 Pad Configuration for $\overline{\text{ESR}}$ Pads

The configuration is selected via bit field ESRCFGx.PC .

The pad functionality control can be configured independently for each pin, comprising:

- A selection of the driver type (open-drain or push-pull)
- An enable function for the output driver (input and/or output capability)
- An enable function for the pull-up/down resistance

The following table defines the coding of the bit fields PC in registers ESRCFG0 , ESRCFG1 , and ESRCFG2 .

Note: The coding is the same as for the port register bit fields Pn_IOCRx.PC .

Table 9-9 PC Coding

PCx[3:0]	Selected Pull-up/Pull-down / Selected Output Function	I/O	Output Characteristics
0000 _B	No pull device activated	Input is not inverted, the input stage is active in power-down mode	
0001 _B	Pull-down device activated		
0010 _B	Pull-up device activated		
0011 _B	No pull device activated		
0100 _B	No pull device activated	Input is inverted, the input stage is active in power-down mode	
0101 _B	Pull-down device activated		
0110 _B	Pull-up device activated		
0111 _B	No pull device activated		

Table 9-9 PC Coding

PCx[3:0]	Selected Pull-up/Pull-down / Selected Output Function	I/O	Output Characteristics
1000 _B	Output of ESRCFGx.OUT	Output, the input stage is not inverted and active in power-down mode	Push-pull
1001 _B	Output of ESRCFGx.OUT		
1010 _B	Output drives a 0 for an Internal Application Reset, a 1 otherwise.		
1011 _B	Output drives a 0 for an Application Reset, a 1 otherwise.		
1100 _B	Output of ESRCFGx.OUT		Open-drain, a pull-up device is activated while the output is not driving a 0
1101 _B	Output of ESRCFGx.OUT		
1110 _B	Output drives a 0 for an Internal Application Reset		
1111 _B	Output drives a 0 for an Application Reset		

When an internal application reset or an application reset occurs with the setting of PC[3:0] = 1x1x_B, an ESR reset will also be triggered if it is enabled in RSTCON1.ESR0.

9.5.2 $\overline{\text{ESR}}$ Control Registers

9.5.2.1 Configuration Registers

$\overline{\text{ESR}}$ External Control Register

The $\overline{\text{ESR}}$ External Control registers contain enable/disable bits for the different inputs that can lead to an $\overline{\text{ESR}}$ action. For $\overline{\text{ESR0}}$ this option is not available.

ESREXCON1

ESR1 External Control Register

SFR (FF32_H/99_H)

Reset Value: 0001_H

ESREXCON2

ESR2 External Control Register

SFR (FF34_H/9A_H)

Reset Value: 0001_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ESR N IN11 EN	ESR N IN10 EN	ESR IN12 EN	ESR IN11 EN	ESR IN10 EN	ESR IN9 EN	ESR IN8 EN	ESR IN7 EN	ESR IN6 EN	ESR IN5 EN	ESR IN4 EN	ESR IN3 EN	ESR IN2 EN	ESR IN1 EN	ESR IN0 EN	ESR EN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ESREN	0	rw	ESRy Pin Enable This bit enables/disables the $\overline{\text{ESRy}}$ pin for the activation of all $\overline{\text{ESRy}}$ related actions. 0 _B The input from pin $\overline{\text{ESRy}}$ is disabled 1 _B The input from pin $\overline{\text{ESRy}}$ is enabled
ESRINxEN (x = 0-11)	x+1	rw	ESR Input X Enable This bit enables/disables the input x for the activation of all $\overline{\text{ESRy}}$ related actions. 0 _B The input is disabled 1 _B The input is enabled

System Control Unit (SCU)

Field	Bits	Type	Description
ESRIN12EN	13	rw	ESR Input 12 Enable This bit enables/disables the input 12 for the activation of all ESRy related actions. 0 _B The input 12 is disabled for the activation of all ESRy related actions. It is used in the second conjugation stage of the other ESRz Input Selection. 1 _B The input 12 is enabled for the activation of all ESRy related actions.
ESRNIN10EN	14	rw	Negated ESR Input 10 Enable This bit enables/disables the negated input 10 for the activation of all ESRy related actions. 0 _B The input is disabled 1 _B The input is enabled
ESRNIN11EN	15	rw	Negated ESR Input 11 Enable This bit enables/disables the negated input 11 for the activation of all ESRy related actions. 0 _B The input is disabled 1 _B The input is enabled

ESREXSTAT1

ESR1 External Status Register **SFR (FF36_H/9B_H)** **Reset Value: 0000_H**

ESREXSTAT2

ESR2 External Status Register **SFR (FF38_H/9C_H)** **Reset Value: 0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0			IN11	IN10	IN9	IN8	IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0	ESR
r			rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
ESR	0	rh	Input ESRy Status This bit is set upon a trigger on input x if ESREXCONy.ESREN was set. This bit can be cleared only by software. 0 _B No trigger for input <u>ESRy</u> occurred 1 _B A trigger for <u>ESRy</u> occurred since it was cleared last time
INx (x = 0-11)	x+1	rh	Input x Status This bit is set upon a trigger on input x if ESREXCONy.ESRINxEN was set for <u>ESRy</u> . This bit can be cleared only by software. 0 _B No trigger for input x occurred 1 _B A trigger for input x occurred since it was cleared last time
0	[15:13]	r	Reserved Read as 0; should be written with 0.

CLRESREXSTAT1

Clear ESR1 External Status RegisterSFR (FF3A_H/9D_H)

Reset Value: 0000_H

CLRESREXSTAT2

Clear ESR2 External Status RegisterSFR (FF3C_H/9E_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0			IN11	IN10	IN9	IN8	IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0	ESR
r			w	w	w	w	w	w	w	w	w	w	w	w	w

Field	Bits	Type	Description
ESR	0	w	Clear Input ESRy Status Setting this bit clears the bit ESREXSTATy.ESR. This bit always read as zero. 0 _B No effect 1 _B Bit ESREXSTATy.ESR is cleared <i>Note: This bit is always read as 0.</i>
INx (x = 0-11)	x+1	w	Clear Input x Status Setting this bit clears the associated bit ESREXSTATy.INx. This bit always read as zero. 0 _B No effect 1 _B Bit ESREXSTATy.INx is cleared <i>Note: This bit is always read as 0.</i>
0	[15:13]	r	Reserved Read as 0; should be written with 0.

ESR Configuration Register

The ESR configuration registers contains bits required for the behavioral control of the ESR pins.

ESRCFG0

ESR0 Configuration Register **ESFR (F100_H/80_H)** **Reset Value: 000E_H**

ESRCFG1

ESR1 Configuration Register **ESFR (F102_H/81_H)** **Reset Value: 0002_H**

ESRCFG2

ESR2 Configuration Register **ESFR (F104_H/82_H)** **Reset Value: 0002_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0					AEDCON		SEDCON		IN	OUT	DF EN	PC			
r					rw		rw		rh	rh	rw	rw			

Field	Bits	Type	Description
PC	[3:0]	rw	Pin Control of ESRx This bit field controls the behavior of the associated <u>ESRx</u> pin. The coding is described in Table 9-9 .
DFEN	4	rw	Digital Filter Enable This bit defines if the 3-stage median filter of the <u>ESRx</u> is used or bypassed. 0 _B The filter is bypassed 1 _B The filter is used
OUT	5	rh	Data Output This bit can be used as output value for the associated <u>ESRx</u> pin. 0 _B If selected, the output level is 0 1 _B If selected, the output level is 1 This bit is controlled via bit field ESRDAT.MOUTx.
IN	6	rh	Data Input This bit monitors the input value at the associated <u>ESRx</u> pin.

System Control Unit (SCU)

Field	Bits	Type	Description
SEDCON	[8:7]	rw	Synchronous Edge Detection Control This bit field defines the edges that lead to an $\overline{\text{ESRx}}$ trigger of the synchronous path. 00 _B No trigger is generated 01 _B A trigger is generated upon a raising edge 10 _B A trigger is generated upon a falling edge 11 _B A trigger is generated upon a raising AND falling edge Other combinations than 00 _B are only allowed if bit field AEDCON is configured to 00 _B .
AEDCON	[10:9]	rw	Asynchronous Edge Detection Control This bit field defines the edges that lead to an $\overline{\text{ESRx}}$ trigger of the asynchronous path. 00 _B No trigger is generated 01 _B A trigger is generated upon a raising edge 10 _B A trigger is generated upon a falling edge 11 _B A trigger is generated upon a raising AND falling edge Other combinations than 00 _B are only allowed if bit field SEDCON is configured to 00 _B .
0	[15:11]	r	Reserved Read as 0; should be written with 0.

9.5.3 ESR Data Register

9.5.3.1 ESRDAT

The $\overline{\text{ESR}}$ data register contains bits required if $\overline{\text{ESRx}}$ are used as data ports.

ESRDAT

ESR Data Register

ESFR (F106_H/83_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0										MOUT2		MOUT1		MOUT0	
r										w		w		w	

Field	Bits	Type	Description
MOUT0	[1:0]	w	Modification of Data Output at $\overline{\text{ESR0}}$ Writing to this bit field can modify the content of bit $\overline{\text{ESRCFG0.OUT}}$ which updates the output at $\overline{\text{ESR0}}$. It always reads 0. 00 _B $\overline{\text{ESR0}}$ output (bit $\overline{\text{ESRCFG0.OUT}}$) is unchanged 01 _B $\overline{\text{ESR0}}$ output (bit $\overline{\text{ESRCFG0.OUT}}$) is set 10 _B $\overline{\text{ESR0}}$ output (bit $\overline{\text{ESRCFG0.OUT}}$) is cleared 11 _B Reserved, do not use this combination <i>Note: This bit is always read as 0.</i>
MOUT1	[3:2]	w	Modification of Data Output at $\overline{\text{ESR1}}$ Writing to this bit field can modify the content of bit $\overline{\text{ESRCFG1.OUT}}$ which updates the output at $\overline{\text{ESR1}}$. It always reads 0. 00 _B $\overline{\text{ESR1}}$ output (bit $\overline{\text{ESRCFG1.OUT}}$) is unchanged 01 _B $\overline{\text{ESR1}}$ output (bit $\overline{\text{ESRCFG1.OUT}}$) is set 10 _B $\overline{\text{ESR1}}$ output (bit $\overline{\text{ESRCFG1.OUT}}$) is cleared 11 _B Reserved, do not use this combination <i>Note: This bit is always read as 0.</i>

System Control Unit (SCU)

Field	Bits	Type	Description
MOUT2	[5:4]	w	Modification of Data Output at ESR2 Writing to this bit field can modify the content of <u>bit ESRCFG2.OUT</u> which updates the output at <u>ESR2</u> . It always reads 0. 00 _B <u>ESR2</u> output (bit ESRCFG2.OUT) is unchanged 01 _B <u>ESR2</u> output (bit ESRCFG2.OUT) is set 10 _B <u>ESR2</u> output (bit ESRCFG2.OUT) is cleared 11 _B Reserved, do not use this combination <i>Note: This bit is always read as 0.</i>
0	[15:6]	r	Reserved Read as 0; should be written with 0.

9.6 Power Supply and Control

The XC27x8X can run from a single external power supply. The core supply voltages can be generated by on-chip Embedded Voltage Regulators (EVRs).

Power Domains

The I/O part is divided in two parts DMP_A and DMP_B. DMP_A contains all ADC related I/Os and DMP_B the remaining system and communication I/Os.

The major part of the on-chip logic is located in an independent core power domain (DMP_1). A second power domain (DMP_M), marked grey in the figure below, controls important device infrastructure plus a Standby RAM (SBRAM).

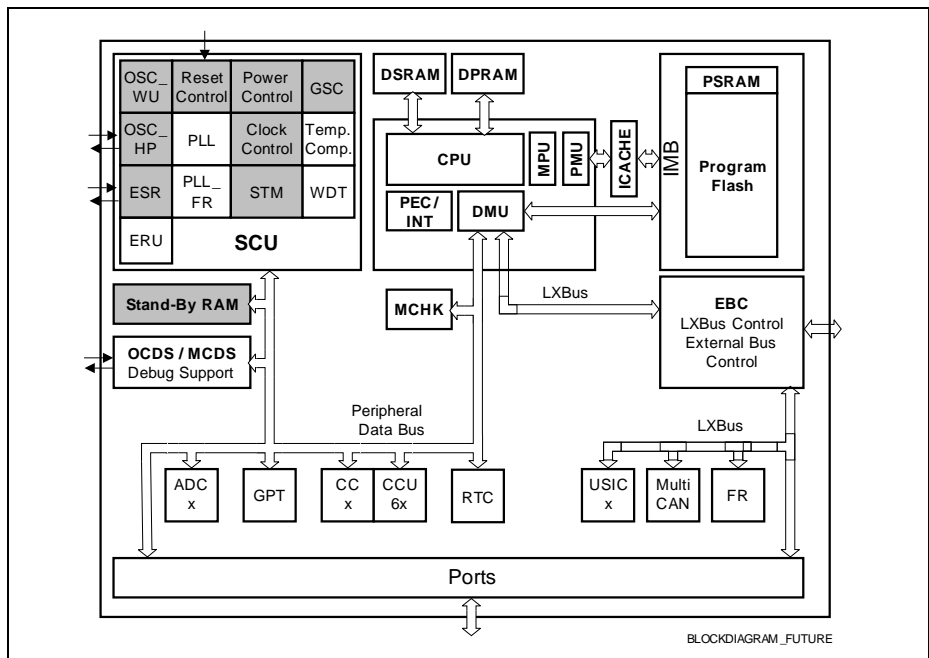


Figure 9-19 XC27x8X Power Domain Structure

Power Supply and Control Functions

The power supply and control is divided into following parts:

- monitoring of the supply voltage
- controlling and adjusting the supply voltage

System Control Unit (SCU)

The supply voltage of pad IO domain for system and communication I/Os (power domain DMP_B) is monitored by a Supply Watchdog (SWD, see [Chapter 9.6.1](#)).

The core voltage for each of the two core supply domains is supervised by a separate Power Validation Circuit (PVC) that provides two monitoring levels. Each monitoring level can request an interrupt (e.g. power-fail warning) or a reset depending on the voltage level. A PVC is used to detect under voltage due to an external short (see [Chapter 9.6.2](#)).

By controlling the regulator, the core power can be switched off to save the leakage current (see [Chapter 9.6.3](#)).

Table 9-10 XC27x8X Power Domains Supply and Control

Power Domain	Supply Source	Supply Voltage [V]	Supply Checked by
Pad IO domain (DMP_B)	External supply	V_{DDPB} : 3.0 ... 5.5 typ See data sheet	SWD
ADC IO domain (DMP_A)	External supply	V_{DDPA} : 3.0 ... 5.5 typ See data sheet	-
Core domain (DMP_M and DMP_1)	EVR_M EVR_1	V_{DDIM} , V_{DDI1} : 1.5 typ See data sheet	PVC_1, PVC_M

9.6.1 Supply Watchdog (SWD)

The supply voltage of the pad I/O domain for systems and communication I/Os (DMP_B) is monitored to validate the overall power supply. The external supply voltage is monitored for following purposes:

- **POR**
Detecting the ramp-up of the external supply voltage, so the device can be started without requiring an external power-on reset (PORST).
- **Brown-out**
Detecting the ramp-down of the external supply voltage, so the device can be brought into a save state without requiring an external power-on reset (PORST).
- Monitoring the external power supply allows the usage of a low-cost regulator without additional status signals (standard 3-pin device).
- Guarantee that the supply voltage for the EVRs is sufficient to generate a valid core voltage under every operating condition

Feature list

The following list is a summary of the SWD functions.

- Trigger a power-on reset whenever the supply falls and as long as the supply remains below V_{VAL}

- Two completely independent threshold levels and comparators
- 16 selectable threshold levels
- Power Saving Mode (only V_{VAL} detection active)

Operating the SWD

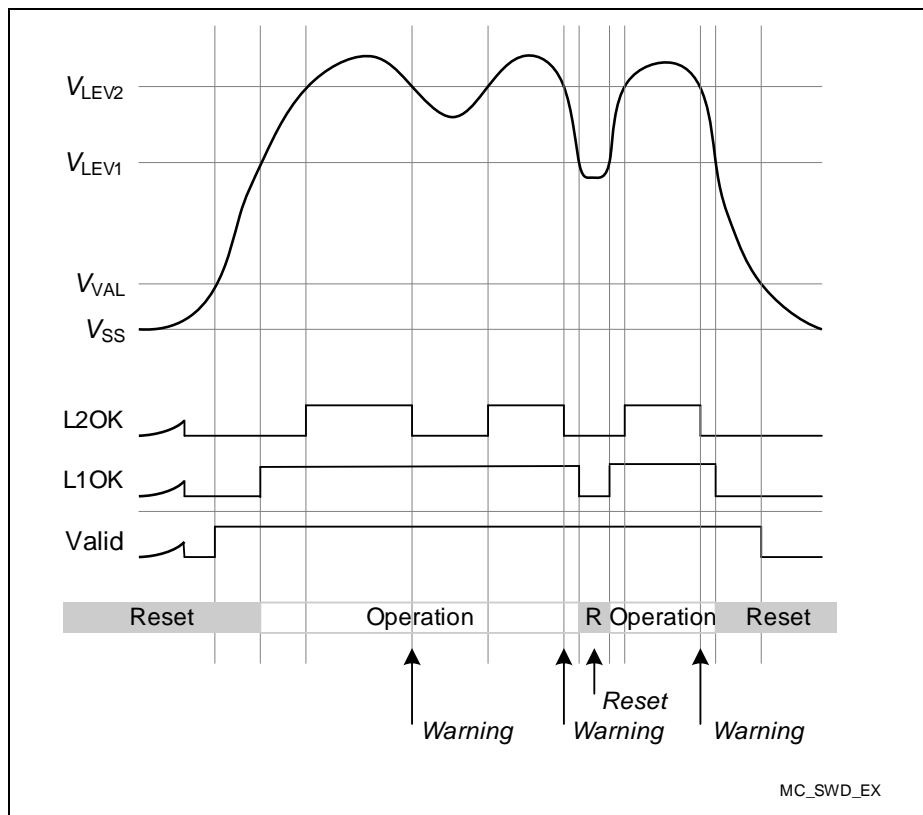


Figure 9-20 SWD Power Validation Example

V_{VAL} defines the fixed internal threshold where the device is held in reset. If V_{VAL} has not been reached the device is held in reset. When V_{DDPB} raises above V_{VAL} , bit **SWDCON1.PON** is set.

The SWD provides two adjustable threshold levels (LEV1 and LEV2) that can be individually programmed, via **SWDCON0.LEV1V** and **SWDCON0.LEV2V**, and deliver a compare value each. The two compare results can be monitored via bits **SWDCON0.L1OK** and **SWDCON0.L2OK**. A reset or interrupt request can be generated

System Control Unit (SCU)

while the voltage level is below or equal/above the configured level of a threshold. If an action and which action is triggered by each threshold can be configured via bits SWDCON0.LxRSTEN and SWDCON0.LxINTEN and bit field SWDCON0.LxALEV ($x = 1, 2$).

The SWD control (programming of the threshold levels) is done by software only.

With these features, an external supply watchdog, e.g. integrated in some external VR, can be replaced. It detects the minimum specified supply voltage level and can be configured to monitor other voltage levels.

Note: If the \overline{PORST} pin is used it has the same functionality as the min-power detection of the SWD.

Power-Saving Mode of the SWD

The two configurable thresholds can be disabled if not needed. This is called the SWD Power Saving Mode. The minimum operating voltage detection (POR/Brown-out detection) can not be disabled and it is always active. The SWD Power Saving Mode is entered by setting bit **SWDCON1.POWENSET** and exit by setting bit SWDCON1.POWENCLR. If the SWD Power Saving Mode is active is indicated by bit SWDCON1.POWEN.

Note: The reset request and interrupt request action should be switched off before entering power-save mode.

9.6.1.1 SWD Control Registers

The following registers are the software interface for the SWD.

SWDCON0

SWD Control 0 Register

ESFR (F080_H/40_H)

Reset Value: 0941_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L2 A LEV	L2 RST EN	L2 INT EN	L2 OK	LEV2V			L1 A LEV	L1 RST EN	L1 INT EN	L1 OK	LEV1V				
rw	rw	rw	rh	rw			rw	rw	rw	rh	rw				

Field	Bits	Type	Description
LEV1V	[3:0]	rw	Level Threshold 1 Voltage This bit field defines the voltage level that is used as threshold 1 check level. The values of the level thresholds are listed in the data sheet.
L1OK	4	rh	Level Threshold 1 Check Result 0 _B The supply voltage is below the Level Threshold 1 voltage LEV1V 1 _B The supply voltage is equal or above the Level Threshold 1 voltage LEV1V
L1INTEN	5	rw	Level Threshold 1 Interrupt Request Enable This bit field defines if an interrupt is requested if the supply voltage comparison matches the action level L1ALEV. 0 _B No interrupt is requested 1 _B An interrupt is requested
L1RSTEN	6	rw	Level Threshold 1 Reset Request Enable This bit field defines if a reset is requested if the supply voltage comparison matches the action level L1ALEV. 0 _B No reset is requested 1 _B An reset is requested

Field	Bits	Type	Description
L1ALEV	7	rw	Level Threshold 1 Action Level 0_B When the supply voltage is below the Level Threshold 1 voltage LEV1V the actions configured by bits L1INTEN and L1RSTEN are requested 1_B When the supply voltage is equal or above the Level Threshold 1 voltage LEV1V the actions configured by bits L1INTEN and L1RSTEN are requested
LEV2V	[11:8]	rw	Level Threshold 2 Voltage This bit field defines the voltage level that is used as check level threshold 2. The values of the level thresholds are listed in the data sheet.
L2OK	12	rh	Level Threshold 2 Check Result 0_B The supply voltage is below the Level Threshold 2 voltage LEV2V 1_B The supply voltage is equal or above the Level Threshold 2 voltage LEV2V
L2INTEN	13	rw	Level Threshold 2 Interrupt Request Enable This bit field defines if an interrupt is requested if the supply voltage comparison matches the action level L2ALEV. 0_B No interrupt is requested 1_B An interrupt is requested
L2RSTEN	14	rw	Level Threshold 2 Reset Request Enable This bit field defines if a reset is requested if the supply voltage comparison matches the action level L2ALEV. 0_B No reset is requested 1_B An reset is requested

System Control Unit (SCU)

Field	Bits	Type	Description
L2ALEV	15	rw	Level Threshold 2 Action Level 0_B When the supply voltage is below the Level Threshold 2 voltage LEV2V the actions configured by bits L2INTEN and L2RSTEN are requested 1_B When the supply voltage is equal or above the Level Threshold 2 voltage LEV2V the actions configured by bits L2INTEN and L2RSTEN are requested

SWDCON1

SWD Control 1 Register

ESFR (F082_H/41_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
											CLR PON	PON	POW EN	POW EN SET	POW EN CLR
											w	rh	rh	w	w

Field	Bits	Type	Description
POWENCLR	0	w	SWD Power Saving Mode Enable Clear 0 _B No action 1 _B Bit POWEN is cleared <i>Note: This bit is always read as 0.</i>
POWENSET	1	w	SWD Power Saving Mode Enable Set 0 _B No action 1 _B Bit POWEN is set <i>Note: This bit is always read as 0.</i>
POWEN	2	rh	SWD Power Saving Mode Enable 0 _B All SWD functions are enabled 1 _B The SWD Power Saving Mode is enabled. Comparators are disabled.
PON	3	rh	Power-On Status Flag 0 _B No power-on event occurred 1 _B A power-on event occurred (V_{DDP} became greater than V_{VAL}).
CLRPN	4	w	Clear Power-On Status Flag 0 _B No action 1 _B Bit PON is cleared <i>Note: This bit is always read as 0.</i>
0	[15:5]	r	Reserved Read as 0; should be written with 0.

9.6.2 Monitoring the Voltage Level of a Core Domain

A Power Validation Circuit (PVC) monitors the internal core supply voltage of a core domain. It can be configured to monitor two programmable independent voltage levels.

The voltage of the core domain is monitored by PVC_1 and PVC_M.

Feature list

The following list summarizes the features of a PVC.

- Two independent comparators
- Threshold levels selectable
- Shut-off, which disables the complete module
- Configurable action level

A PVC provides two adjustable threshold levels (LEV1 and LEV2) that can be individually programmed via PVCxCON0.LEV1V and PVCxCON0.LEV2V (x = M or 1). The current supply level of a domain is compared with the threshold values. The two compare results can be monitored via bits PVCxCON0.LEV1OK and PVCxCON0.LEV2OK (x = M or 1).

Note: The PVC has a build in Hysteresis in the range of 40..50mV. The threshold level given in the data-sheet represents the lower corner of the hysteresis.

A reset or interrupt request can be generated in case the core domain voltage level is below or equal / above the configured threshold level. An interrupt is requested if bit PVCxCON0.L1INTEN and / or PVCxCON0.L2INTEN (x = M or 1) is set. A reset is requested if bit PVCxCON0.L1RSTEN and / or PVCxCON0.L2RSTEN (x = M or 1) is set.

Note: For a single threshold both interrupt and reset request generation should not be enabled at the same time.

Note: Due to variations of the tolerance of the EVR and the PVC levels, the LEV2V interrupt can be triggered inadvertently, even though the core voltage is within the normal range. Hence, it is recommended not to use this warning level.

9.6.2.1 PVC Status and Control Registers

These registers are the software interface for PVC_1 and PVC_M.

PVC1CON0

PVC_1 Control Step 0 Register

ESFR (F014_H/0A_H)

Reset Value: 0504_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L2 AS EN	L2 RST EN	L2 INT EN	L2 A LEV	LEV 2 OK		LEV2V		L1 AS EN	L1 RST EN	L1 INT EN	L1 A LEV	LEV 1 OK		LEV1V	
rw	rw	rw	rw	rh		rw		rw	rw	rrw	rw	rh		rw	

Field	Bits	Type	Description
LEV1V	[2:0]	rw	Level Threshold 1 Voltage This bit field defines the Level Threshold 1 that is compared with the DMP_1 core voltage. The values for the different configurations are listed in the data sheet.
LEV1OK	3	rh	Level Threshold 1 Check Result 0 _B The core supply voltage of the DMP_1 is below Level Threshold 1 voltage LEV1V 1 _B The core supply voltage of the DMP_1 is equal or above the Level Threshold 1 voltage LEV1V
L1ALEV	4	rw	Level Threshold 1 Action Level 0 _B When the core supply voltage is below Level Threshold 1 voltage LEV1V the action configured by bits L1INTEN, L1RSTEN, and L1ASEN are requested 1 _B When the core supply voltage is equal or above Level Threshold 1 voltage LEV1V the actions configured by bits L1INTEN, L1RSTEN, and L1ASEN are requested
L1INTEN	5	rw	Level Threshold 1 Interrupt Request Enable This bit defines if an interrupt request trigger is requested if the comparison check was successful. When a check is successful is defined via bit L1ALEV. 0 _B No interrupt is requested 1 _B An interrupt is requested

Field	Bits	Type	Description
L1RSTEN	6	rw	Level Threshold 1 Reset Request Enable This bit defines if a reset request trigger is requested if the comparison check was successful. When a check is successful is defined via bit L1ALEV. 0 _B No reset is requested 1 _B An reset is requested
L1ASEN	7	rw	Level Threshold 1 Asynchronous Action Enable This bit defines if asynchronous action can be performed if the comparison check was successful. When a check is successful is defined via bit L1ALEV. 0 _B No asynchronous actions are performed 1 _B Asynchronous actions can be performed
LEV2V	[10:8]	rw	Level Threshold 2 Voltage This bit field defines the level of threshold 2 that is compared with the DMP_1 core voltage.. The values for the different configurations are listed in the data sheet.
LEV2OK	11	rh	Level Threshold 2 Check Result 0 _B The core supply voltage of the DMP_1 is below the Level Threshold 2 LEV2V 1 _B The core supply voltage of the DMP_1 is equal or above the Level Threshold 2 LEV2V
L2ALEV	12	rw	Level Threshold 2 Action Level 0 _B When the core supply voltage is below the Level Threshold 2 voltage LEV2V the action configured by bits L2INTEN, L2RSTEN, and L2ASEN are requested 1 _B When the core supply voltage is equal or above the Level Threshold 2 voltage LEV2V the action configured by bits L2INTEN, L2RSTEN, and L2ASEN are requested
L2INTEN	13	rw	Level Threshold 2 Interrupt Request Enable This bit defines if an interrupt request trigger is requested if the comparison check was successful. When a check is successful is defined via bit L2ALEV. 0 _B No interrupt is requested 1 _B An interrupt is requested

System Control Unit (SCU)

Field	Bits	Type	Description
L2RSTEN	14	rw	Level Threshold 2 Reset Request Enable This bit defines if a reset request trigger is requested if the comparison check was successful. When a check is successful is defined via bit L2ALEV. 0_B No reset is requested 1_B An reset is requested
L2ASEN	15	rw	Level Threshold 2 Asynchronous Action Enable This bit defines if asynchronous action can be performed if the comparison check was successful. When a check is successful is defined via bit L2ALEV. 0_B No asynchronous actions are performed 1_B Asynchronous actions can be performed

PVCMCON0

PVC_M Control Step 0 Register

MEM (F1E4_H/--)

Reset Value: 0544_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L2 AS EN	L2 RST EN	L2 INT EN	L2 A LEV	LEV 2 OK	LEV2V			L1 AS EN	L1 RST EN	L1 INT EN	L1 A LEV	LEV 1 OK	LEV1V		
rw	rw	rw	rw	rh	rw			rw	rw	rw	rw	rh	rw		

Field	Bits	Type	Description
LEV1V	[2:0]	rw	Level Threshold 1 Voltage This bit field defines the Level Threshold 1 that is compared with the DMP_M core supply voltage. The values for the different configurations are listed in the data sheet.
LEV1OK	3	rh	Level Threshold 1 Check Result 0 _B The core supply voltage of the DMP_M is below Level Threshold 1 voltage LEV1V 1 _B The core supply voltage of the DMP_M is equal or above the Level Threshold 1 voltage LEV1V
L1ALEV	4	rw	Level Threshold 1 Action Level 0 _B When the core supply voltage is below Level Threshold 1 voltage LEV1V the action configured by bits L1INTEN, L1RSTEN, and L1ASEN are requested 1 _B When the core supply voltage is equal or above Level Threshold 1 voltage LEV1V the actions configured by bits L1INTEN, L1RSTEN, and L1ASEN are requested
L1INTEN	5	rw	Level Threshold 1 Interrupt Request Enable This bit defines if an interrupt request trigger is requested if the comparison check was successful. When a check is successful is defined via bit L1ALEV. 0 _B No interrupt is requested 1 _B An interrupt is requested

Field	Bits	Type	Description
L1RSTEN	6	rw	Level Threshold 1 Reset Request Enable This bit defines if a reset request trigger is requested if the comparison check was successful. When a check is successful is defined via bit L1ALEV. 0 _B No reset is requested 1 _B An reset is requested
L1ASEN	7	rw	Level Threshold 1 Asynchronous Action Enable This bit defines if asynchronous action can be performed if the comparison check was successful. When a check is successful is defined via bit L1ALEV. 0 _B No asynchronous actions are performed 1 _B Asynchronous actions can be performed
LEV2V	[10:8]	rw	Level Threshold 2 Voltage This bit field defines the Level Threshold 2 that is compared with the DMP_M core supply voltage. The values for the different configurations are listed in the data sheet.
LEV2OK	11	rh	Level Threshold 2 Check Result 0 _B The core supply voltage of the DMP_M is below Level Threshold 2 voltage LEV2V 1 _B The core supply voltage of the DMP_M is equal or above the Level Threshold 2 voltage LEV2V
L2ALEV	12	rw	Level Threshold 2 Action Level 0 _B When the core supply voltage is below the Level Threshold 2 voltage LEV2V the action configured by bits L2INTEN, L2RSTEN, and L2ASEN are requested 1 _B When the core supply voltage is equal or above the Level Threshold 2 voltage LEV2V the action configured by bits L2INTEN, L2RSTEN, and L2ASEN are requested
L2INTEN	13	rw	Level Threshold 2 Interrupt Request Enable This bit defines if an interrupt request trigger is requested if the comparison check was successful. When a check is successful is defined via bit L2ALEV. 0 _B No interrupt is requested 1 _B An interrupt is requested

System Control Unit (SCU)

Field	Bits	Type	Description
L2RSTEN	14	rw	Level Threshold 2 Reset Request Enable This bit defines if a reset request trigger is requested if the comparison check was successful. When a check is successful is defined via bit L2ALEV. 0 _B No reset is requested 1 _B An reset is requested
L2ASEN	15	rw	Level Threshold 2 Asynchronous Action Enable This bit defines if asynchronous action can be performed if the comparison check was successful. When a check is successful is defined via bit L2ALEV. 0 _B No asynchronous actions are performed 1 _B Asynchronous actions can be performed

9.6.3 Controlling the Voltage Level of a Core Domain

The core power can be controlled within certain limits. The voltage level is controlled by two **Embedded Voltage Regulators** (EVR).

The power domain is controlled by both EVR_M and EVR_1.

9.6.3.1 Embedded Voltage Regulator

The main part of the device logic operates at a typical voltage level of 1.5 V. This supply voltage is generated by the Embedded Power Regulators (EVRs) out of the pad voltage. External buffer caps are required for stable regulation.

Feature list:

- Multiple core voltage levels including zero
- Core voltage generation based on a High Precision Bandgap
- Core current limit

The EVR configurations to select the desired voltage and reference pair are combined within EVR settings EVRxSETyyV (x = M or 1 and yy = 15). Each setting contains a bit field (VRSEL) to select the voltage level and reference and a bit field to fine-tune the voltage level (VLEV). One out of the possible settings is used to control each of the EVRs, but only in the allowed combinations for the two EVRs. The EVRs use a High Precision Bandgap (HP) as reference.

The BG voltage of each setting can be adjusted to compensate application and environmental influences by the bit field EVRxSETyyV.VLEV. VLEV is set by default or trimmed by each device during production test to reach the default setting targets.

High Precision Bandgap (HP)

The HP bandgap of the system is used for following purposes:

- Provide a very stable reference for the two EVRs
- Provide an accurate reference for the flash memory. For more information see the flash memory description.

Only one HP bandgap is implemented which is used by both EVRs. The HP bandgap can be enabled / disabled via the bit **EVRMCON1.HPEN**.

EVR Status and Control Registers

EVR1CON0

EVR_1 Control 0 Register

ESFR (F088_H/44_H)

Reset Value: DF20_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EVR DIS	-	0	CC DIS	CCLEV	LPR DIS	1	0	LPRLEV			0				
rh	-	rw	rh	rw	rh	rw	rw	rw			r				

Field	Bits	Type	Description
LPRLEV	[5:3]	rw	Reserved Do not change this value when writing to this register.
0	[7:6]	rw	Reserved Do not change this value when writing to this register
1	8	rw	Reserved Do not change this value when writing to this register
LPRDIS	9	rh	Reserved Value is undefined
CCLEV	[11:10]	rw	Current Control Level This bit field is required for enabling/disabling the current control (CCDIS). Valid values are described in the Programmer's Guide.
CCDIS	12	rh	Current Control Disable 0 _B The current control is enabled 1 _B The current control is disabled This bit is updated by bit EVR1SETy.CCDIS.
0	13	rw	Reserved Do not change this value when writing to this register
EVRDIS	15	rh	EVR_1 Disable 0 _B The EVR_1 is enabled 1 _B The EVR_1 is disabled This bit is updated by bit EVR1SETy.EVRDIS.
0	[2:0]	r	Reserved Read as 0; should be written with 0.

EVR1SET15VHP

EVR_1 Setting for 1.5 V HP Register

ESFR (F09E_H/4F_H)

Reset Value: 001B_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EVR DIS	0		CC DIS	0		LPR DIS	0		VRSEL	VLEV					
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
VLEV	[5:0]	rw	Voltage Level Adjust This bit field adjusts the BG voltage and is trimmed by each device during production test to reach the default setting targets. Do not change this value when writing to this register.
VRSEL	[7:6]	rw	Voltage Reference Selection 00 _B 15VHP - Full Voltage with high precision bandgap selected 01 _B Reserved, do not use this combination 10 _B Reserved, do not use this combination 11 _B Reserved, do not use this combination <i>Note: The reset value should always be written to this bit field.</i>
LPRDIS	9	rw	Reserved Do not change this value when writing to this register
CCDIS	12	rw	Current Control Disable 0 _B The current control is enabled 1 _B The current control is disabled This bit updates bit EVR1CON0.CCDIS. <i>Note: Before switching off the current control the CCLEV setting in EVR1CON0 has to be set to 00_B.</i>
EVRDIS	15	rw	EVR_1 Disable 0 _B The EVR_1 is enabled 1 _B The EVR_1 is disabled This bit updates bit EVR1CON0.EVRDIS.

System Control Unit (SCU)

Field	Bits	Type	Description
0	8, [11:10], [14:13]	rw	Reserved Should be written with 0.

EVRMCON0

EVR_M Control 0 Register

ESFR (F084_H/42_H)

Reset Value: 0D20_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EVR DIS	0	CC DIS	CCLEV	LPR DIS	1	0	ULP EVR ON	LPRLEV			0				
rh	r	rh	rw	rh	rw	rw	rw	rw			r				

Field	Bits	Type	Description
LPRLEV	[5:3]	rw	Reserved Do not change this value when writing to this register
ULPEVRON	6	rw	Reserved Do not change this value when writing to this register
0	7	rw	Reserved Do not change this value when writing to this register
1	8	rw	Reserved Do not change this value when writing to this register
LPRDIS	9	rh	Low Power Reference Disable 0 _B The LPR is enabled 1 _B The LPR is disabled This bit is updated by bit EVRMSETy.LPRDIS.
CCLEV	[11:10]	rw	Current Control Level This bit field is required for enabling/disabling the current control (CCDIS). Valid values are described in the Programmer's Guide.
CCDIS	12	rh	Current Control Disable 0 _B The current control is enabled 1 _B The current control is disabled This bit is updated by bit EVRMSETy.CCDIS.
EVRDIS	15	rh	EVR_M Disable 0 _B The EVR_M is enabled 1 _B The EVR_M is disabled This bit is updated by bit EVRMSETy.EVRDIS.
0	[2:0], [14:13]	r	Reserved Read as 0; should be written with 0.

EVRMCON1

EVR_M Control 1 Register

ESFR (F086_H/43_H)

Reset Value: 0101_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							HP EN	HPADJUST							
r							rw	rw							

Field	Bits	Type	Description
HPADJUST	[7:0]	rw	HP Bandgap Adjustment This bit field is a device specific trimmvalue for the HP bandgap. Do not change this value when writing to this register.
HPEN	8	rw	HP Bandgap Enable 0 _B The HP bandgap is disabled 1 _B The HP bandgap is enabled
0	[15:9]	r	Reserved Read as 0; should be written with 0.

EVRMSET15VHP

EVR_M Setting for 1.5 V HP Register

ESFR (F096_H/4B_H)

Reset Value: 001B_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EVR DIS	0		CC DIS	0		LPR DIS	0		VRSEL	VLEV					
rw	rw		rw	rw		rw	rw		rw	rw					

Field	Bits	Type	Description
VLEV	[5:0]	rw	Voltage Level Adjust This bit field adjusts the BG voltage and is trimmed by each device during production test to reach the default setting targets. Do not change this value when writing to this register.

System Control Unit (SCU)

Field	Bits	Type	Description
VRSEL	[7:6]	rw	Voltage Reference Selection 00 _B 15VHP - Full Voltage with high precision bandgap selected 01 _B Reserved, do not use this combination 10 _B Reserved, do not use this combination 11 _B Reserved, do not use this combination <i>Note: The reset value should always be written to this bit field.</i>
LPRDIS	9	rw	Reserved Do not change this value when writing to this register
CCDIS	12	rw	Current Control Disable 0 _B The current control is enabled 1 _B The current control is disabled This bit updates bit EVRMCON0.CCDIS. <i>Note: Before switching off the current control the CCLEV setting in EVRMCON0 has to be set to 00_B.</i>
0	14	rw	Reserved Do not change this value when writing to this register
EVRDIS	15	rw	EVR_M Disable 0 _B The EVR_M is enabled 1 _B The EVR_M is disabled This bit updates bit EVR1CON0.EVRDIS.
0	8, [11:10], 13	rw	Reserved Should be written with 0.

9.6.3.2 Sources for Core Supply Voltage

The on-chip EVRs can generate the XC27x8X's core supply voltage from the (externally supplied) IO voltage.

Core Supply via On-chip EVRs

Generating the core supply voltage via the integrated EVRs is the preferred operating mode, because it saves an additional external voltage regulator. The integrated EVRs are fed from supply voltage V_{DDPB} .

Proper operation of the EVRs requires external buffer capacitances. Please refer to the respective Data Sheet for the recommended values. The current is delivered by the integrated pass devices.

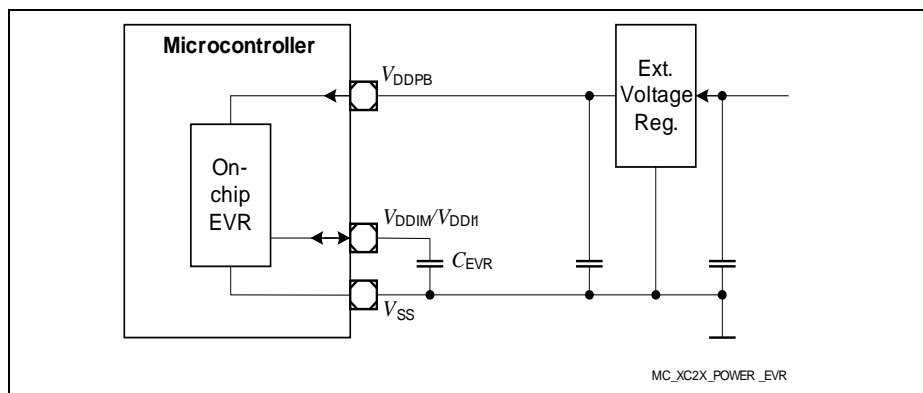


Figure 9-21 Selecting the EVR for Core Supply

Generating the core supply voltage with on-chip resources provides full control of power reduction modes, so the application can control and minimize the energy consumption of the XC27x8X using built-in mechanisms without requiring additional external circuitry.

9.6.4 Handling the Power System

Using the power system correctly is the key to power saving. Depending on the application different operating states can be defined in order to save maximal power. The XC27x8X supports following power saving mechanisms:

- Reduction of the system performance
 - the power consumption depends directly on the frequency of the system
 - the system performance is controlled with the clock operation mechanism
- Stopping single unused peripheral
 - a peripheral not needed for an application can be disabled
 - the module operation is controlled via register MOD_KSCCFG
- Stopping multiple unused peripherals
 - peripherals not needed for an application can be disabled
 - system peripheral operation is controlled via the Global State Controller (GSC)
- Stopping single unused analog parts
 - an analog part not needed for an application can be stopped
 - the operation is controlled via register either located in the SCU (PLL, clocks, PVCs, SWD, Temperature Compensation) or the ADC

9.7 Global State Controller (GSC)

Mode Control for the system peripherals provides besides power saving modes and the clock management an additional opportunity for configuring the system to the application needs.

Mode Control is described in detail in this chapter and is implemented by the Global State Controller (GSC). The GSC enables the user to configure one operating mode in a fast and easy way, reacting fast and explicit to needs of an application.

Feature Overview

The following issues are handled by the GSC:

- Control of peripheral clock operation
- Suspend control for debugging
- Arbitration between the different request sources

According to the requests coming from the OCDS, the SWD pre-warning detection or other blocks, the GSC does an internal prioritization. The result is forwarded as command request broadcast to all peripherals. The GSC internal prioritization scheme for the implemented request sources is shown in [Table 9-11](#).

9.7.1 GSC Control Flow

The sequence begins when at least one request source asserts its trigger in order to request a mode change in the SoC. If several requests are pending there is an arbitration mechanism that treats this issue. Request triggers are not stored by the GSC, therefore a trigger source has to assert its trigger until the trigger is no longer valid or needed.

A request trigger is kept asserted as long as either the request is still pending or the resulting command of the request was entered and acknowledged by the system. The communication of the GSC and the peripherals is based on commands. Three different commands are defined resulting in three modes:

- Wake-up command: requests Normal Mode
- Clock-off command: requests Stop Mode
- Debug command: requests Suspend Mode

The specific behavior in these three modes is defined for each peripheral in its module register `mod_KSCCFG`.

9.7.1.1 Request Source Arbitration

The highest priority for the arbitration is zero (see [Table 9-11](#)).

Each system clock cycle a new arbitration round is started. The winner of an arbitration round requests the next command towards the SoC. Please note that winning an arbitration does not lead automatically to a new command raised. Only if currently no command is broadcast in the SoC a new command can be generated and broadcast. If

the winner of the arbitration round is the same request trigger as in the previous round or if no winner was detected no new command request is generated.

Table 9-11 Connection of the Request Sources

Request Source	Priority
OCDS exit	4
ESR0	5
ESR1	6
ESR2	7
WUT	8
ITC	9
GPT12E	10
SW1	11
SW2	12
OCDS entry	14

9.7.1.2 Generation of a New Command

When a new request trigger was detected and arbitrated a new command request is generated if currently no command request is broadcast that is not received by all slaves.

Table 9-12 Request Source and Command Request Coupling

Request Source	Command Description
OCDS exit	Wake-up; Normal Mode
ESR0	Wake-up; Normal Mode
ESR1	Wake-up; Normal Mode
ESR2	Clock-off; Stop Mode
WUT	Wake-up; Normal Mode
ITC	Wake-up; Normal Mode
GPT12E	Wake-up; Normal Mode
SW1	Wake-up; Normal Mode
SW2	Clock-off; Stop Mode
OCDS entry	Debug; Suspend Mode

9.7.1.3 Usage of Commands

The complete control mechanism for the different operation modes of the various slaves is divided into two parts:

- A central control and configuration part; the Global State Controller (GSC)
- One local control part in each slave; the Kernel State Controller (KSC)

Via the GSC either different hardware sources (e.g. the WUT or the OCDS) or the software can request the system to enter a specific mode. The parts that are affected by the mode can be pre-defined locally for each part via the KSC. For each command a specific reaction can be pre-configured in each KSC for each individual part.

Note: Requesting a peripheral to be permanently shut off by clearing `mod_KSCCFG.MODEN` to 0 does not start a GSC run. However, a GSC run triggered in parallel to the ramp down of this peripheral will have the finite state machine of the GSC waiting for an acknowledge also of this peripheral as long as the peripheral does not deliver its acknowledge or the respective bit in `GSCPERSTATEN` is cleared.

The proposal is either to disable automatic GSC runs (by setting `GSCEN` respectively) in case the application needs the information of the shutdown acknowledge of the peripheral or to disable the respective bit in `GSCPERSTATEN`, so that the missing acknowledge is not taken into account.

Note: When a GSC mode request has been successfully entered, the GSC arbiter is open for any new request. In case a request occurs to enter the current mode, this request is pipelined and remains pending.

*It is recommended to request a command by a software trigger. In particular the clock-off command should be triggered by `SW2`. The usage of commands requested by hardware has to be done carefully. Only hardware resources requesting Normal Mode should be selected. If the software has detected a wake-up then pending mode change requests can be removed by clearing the bits of the selected sources in **GSCEN** and then enabling the bits in `GSCEN` again.*

9.7.1.4 Terminating a Request Trigger

A request trigger is no longer taken into account for the arbitration after the de-assertion of the request trigger, if it is not enabled or when its respective enable bit is cleared.

9.7.1.5 Suspend Control Flow

The suspend feature is controlled by the OCDS block. The GSC operates only as control and communication interface towards the system. The suspend feature is composed out of two requirements:

The mode that has to be entered when the Suspend Mode is requested.

The mode that has to be entered when the Suspend Mode is left.

System Control Unit (SCU)

The request to enter Suspend Mode is forwarded from the OCDS. When the Suspend Mode is requested the system is expected to be stopped as soon as possible in an idle state where no internal process is pending and in a way that this system state does not lead to any damage internally or externally and can also be left without any damage. Therefore all peripherals in the system are requested to enter a mode where the clock can be stopped. This is done by sending a debug command.

Leaving the Suspend Mode should serve the goal that debugging is a non-intrusive operation. Therefore leaving the Suspend Mode can not lead to only one dedicated system mode, instead it leads to the system mode the system left when it was requested to exit the Suspend Mode. The system mode is stored when a Suspend Mode request is detected by the GSC and is used as target system mode when a leave Suspend Mode trigger is detected by the GSC.

9.7.1.6 Error Feedback for a Mode Transition

In case at least one peripheral reports an error the error flag in register GSCSTAT is set. If no error is currently detected upon a new assertion of a system mode by the GSC the error flag is cleared. To inform the system of this erroneous state an interrupt can be generated.

9.7.2 GSC Registers

9.7.2.1 GSC Control and Status Registers

The following register control and configure the behavior of the GSC.

GSCSWREQ

GSC Software Request Register

SFR (FF14_H/8A_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							0							SW TRG 2	SW TRG 1
							r							rwh	rwh

Field	Bits	Type	Description
SWTRG1	0	rwh	Software Trigger 1 (SW1) 0 _B No SW1 request trigger is generated 1 _B A SW1 request trigger is generated This bit is automatically cleared if the SW1 request trigger wins the arbitration and was broadcast to the system.
SWTRG2	1	rwh	Software Trigger 2 (SW2) 0 _B No SW2 request trigger is generated 1 _B A SW2 request trigger is generated This bit is automatically cleared if the SW2 request trigger wins the arbitration and was broadcast to the system.
0	[15:2]	r	Reserved Read as 0; should be written with 0.

GSCEN

GSC Enable Register

SFR (FF16_H/8B_H)

Reset Value: 7FFF_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	OCD SEN EN	1	SW2 EN	SW1 EN	GPT EN	ITC EN	WUT EN	ESR 2 EN	ESR 1 EN	ESR 0 EN	OCD SEX EN	PSC AEN EN	PSC AEX EN	PSC BEN EN	PSC BEX EN
r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
PSCBEXEN	0	rw	Reserved Must be written with 0 _B .
PSCBENEN	1	rw	Reserved Must be written with 0 _B .
PSCAEXEN	2	rw	Reserved Must be written with 0 _B .
PSCAENEN	3	rw	Reserved Must be written with 0 _B .
OCDSEXEN	4	rw	OCDS Exit Request Trigger Enable 0 _B OCDS exit request trigger is not taken into account (disabled) 1 _B OCDS exit request trigger is taken into account (enabled)
ESR0EN	5	rw	ESR0 Request Trigger Enable 0 _B ESR0 request trigger is not taken into account (disabled) 1 _B ESR0 request trigger is taken into account (enabled)
ESR1EN	6	rw	ESR1 Request Trigger Enable 0 _B ESR1 request trigger is not taken into account (disabled) 1 _B ESR1 request trigger is taken into account (enabled)
ESR2EN	7	rw	ESR2 Request Trigger Enable 0 _B ESR2 request trigger is not taken into account (disabled) 1 _B ESR2 request trigger is taken into account (enabled)

System Control Unit (SCU)

Field	Bits	Type	Description
WUTEN	8	rw	WUT Request Trigger Enable 0 _B WUT request trigger is not taken into account (disabled) 1 _B WUT request trigger is taken into account (enabled)
ITCEN	9	rw	ITC Request Trigger Enable 0 _B ITC request trigger is not taken into account (disabled) 1 _B ITC request trigger is taken into account (enabled)
GPTEN	10	rw	GTP12E Request Trigger Enable 0 _B GPT12E request trigger is not taken into account (disabled) 1 _B GPT12E request trigger is taken into account (enabled)
SW1EN	11	rw	Software 1 Request Trigger Enable 0 _B SW1 request trigger is not taken into account (disabled) 1 _B SW1 request trigger is taken into account (enabled)
SW2EN	12	rw	Software 2 Request Trigger Enable 0 _B SW2 request trigger is not taken into account (disabled) 1 _B SW2 request trigger is taken into account (enabled)
1	13	rw	Reserved Read as 1; should be written with 1.
OCDSENEN	14	rw	OCDS Entry Request Trigger Enable 0 _B OCDS entry request trigger is not taken into account (disabled) 1 _B OCDS entry request trigger is taken into account (enabled) OCDS entry is the request source belonging to the according connector interface.
0	15	r	Reserved Read as 0; should be written with 0.

GSCSTAT

GSC Status Register

SFR (FF18_H/8C_H)

Reset Value: 3C00_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		SOURCE				PEN	ERR	0		NEXT		0	CURRENT		
r		rh				rh	rh	r		rh		r	rh		

Field	Bits	Type	Description
CURRENT	[1:0]	rh	Currently used Command This bit field states the currently used system mode.
NEXT	[5:4]	rh	Next to use Command This bit field states the next to be used system mode.
ERR	8	rh	Error Status Flag This bit flags if with the last command that was broadcast was acknowledge with at least one error. This bit is automatically cleared when a new command is broadcast.
PEN	9	rh	Command Pending Flag This flag states if currently a command is pending or not. A command is pending after the broadcast as long as no all blocks acknowledge that they finished the operation requested by the command.

System Control Unit (SCU)

Field	Bits	Type	Description
SOURCE	[13:10]	rh	Requesting Source Status This bit field monitors the source that triggered the last request. 0000 _B Reserved 0001 _B Reserved 0010 _B Reserved 0011 _B Reserved 0100 _B OCDS exit 0101 _B <u>ESR0</u> 0110 _B <u>ESR1</u> 0111 _B <u>ESR2</u> 1000 _B WUT 1001 _B ITC 1010 _B GPT12E 1011 _B SW1 1100 _B SW2 1101 _B Reserved, do not use this combination 1110 _B OCDS entry 1111 _B Reserved, do not use this combination
0	[3:2], [7:6], [15:14]	r	Reserved Read as 0; should be written with 0.

GSCPERSTATEN

GSC Peripheral Status Enable Register

SFR (FF04_H/82_H)

Reset Value: FFFF_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USIC 3	USIC 2	USIC 1	USIC 0	FL	MEM	RTC	CCU 63	CCU 62	CCU 61	CCU 60	M CAN	CC2	1	GPT 12E	ADC
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ADC	0	rw	<p>ADC Acknowledge Enable This bit defines if the acknowledge status of ADC modules is taken into account and displayed or ignored.</p> <p>0_B The ADC modules acknowledge is ignored, it is treated as always asserted</p> <p>1_B The ADC modules acknowledge is used</p>
GPT12E	1	rw	<p>GPT12E Acknowledge Enable This bit defines if the acknowledge status of GPT12E module is taken into account and displayed or ignored.</p> <p>0_B The GPT12E module acknowledge is ignored, it is treated as always asserted</p> <p>1_B The GPT12E module acknowledge is used</p>
CC2	3	rw	<p>CC2 Acknowledge Enable This bit defines if the acknowledge status of CC2 module is taken into account and displayed or ignored.</p> <p>0_B The CC2 module acknowledge is ignored, it is treated as always asserted</p> <p>1_B The CC2 module acknowledge is used</p>
MCAN	4	rw	<p>MultiCAN Acknowledge Enable This bit defines if the acknowledge status of MultiCAN module is taken into account and displayed or ignored.</p> <p>0_B The MultiCAN module acknowledge is ignored, it is treated as always asserted</p> <p>1_B The MultiCAN module acknowledge is used</p>

System Control Unit (SCU)

Field	Bits	Type	Description
CCU60	5	rw	CCU60 Acknowledge Enable This bit defines if the acknowledge status of CCU60 module is taken into account and displayed or ignored. 0 _B The CCU60 module acknowledge is ignored, it is treated as always asserted 1 _B The CCU60 module acknowledge is used
CCU61	6	rw	CCU61 Acknowledge Enable This bit defines if the acknowledge status of CCU61 module is taken into account and displayed or ignored. 0 _B The CCU61 module acknowledge is ignored, it is treated as always asserted 1 _B The CCU61 module acknowledge is used
CCU62	7	rw	CCU62 Acknowledge Enable This bit defines if the acknowledge status of CCU62 module is taken into account and displayed or ignored. 0 _B The CCU62 module acknowledge is ignored, it is treated as always asserted 1 _B The CCU62 module acknowledge is used
CCU63	8	rw	CCU63 Acknowledge Enable This bit defines if the acknowledge status of CCU63 module is taken into account and displayed or ignored. 0 _B The CCU63 module acknowledge is ignored, it is treated as always asserted 1 _B The CCU63 module acknowledge is used
RTC	9	rw	RTC Acknowledge Enable This bit defines if the acknowledge status of RTC module is taken into account and displayed or ignored. 0 _B The RTC module acknowledge is ignored, it is treated as always asserted 1 _B The RTC module acknowledge is used

Field	Bits	Type	Description
MEM	10	rw	C166SV2 Subsystem Acknowledge Enable This bit defines if the acknowledge status of C166SV2 Subsystem module is taken into account and displayed or ignored. 0 _B The C166SV2 Subsystem module acknowledge is ignored, it is treated as always asserted 1 _B The C166SV2 Subsystem module acknowledge is used
FL	11	rw	Flash Acknowledge Enable This bit defines if the acknowledge status of Flash module is taken into account and displayed or ignored. 0 _B The Flash module acknowledge is ignored, it is treated as always asserted 1 _B The Flash module acknowledge is used
USIC0	12	rw	USIC0 Acknowledge Enable This bit defines if the acknowledge status of USIC0 module is taken into account and displayed or ignored. 0 _B The USIC0 module acknowledge is ignored, it is treated as always asserted 1 _B The USIC0 module acknowledge is used
USIC1	13	rw	USIC1 Acknowledge Enable This bit defines if the acknowledge status of USIC1 module is taken into account and displayed or ignored. 0 _B The USIC1 module acknowledge is ignored, it is treated as always asserted 1 _B The USIC1 module acknowledge is used
USIC2	14	rw	USIC2 Acknowledge Enable This bit defines if the acknowledge status of USIC2 module is taken into account and displayed or ignored. 0 _B The USIC2 module acknowledge is ignored, it is treated as always asserted 1 _B The USIC2 module acknowledge is used

System Control Unit (SCU)

Field	Bits	Type	Description
USIC3	15	rw	USIC3 Acknowledge Enable This bit defines if the acknowledge status of USIC3 module is taken into account and displayed or ignored. 0 _B The USIC3 module acknowledge is ignored, it is treated as always asserted 1 _B The USIC3 module acknowledge is used

GSCPERSTATEN1

GSC Peripheral Status Enable 1 Register

SFR (FF06_H/83_H)

Reset Value: FFFF_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						-							FR	1	USIC 4
						-							rw	rw	rw

Field	Bits	Type	Description
USIC4	0	rw	USIC4 Acknowledge Enable This bit defines if the acknowledge status of USIC4 module is taken into account and displayed or ignored. 0 _B The USIC4 module acknowledge is ignored, it is treated as always asserted 1 _B The USIC4 module acknowledge is used
1	1	rw	Reserved Read as 1; should be written with 1 _B .
FR	2	rw	FlexRay Acknowledge Enable This bit defines if the acknowledge status of FR module is taken into account and displayed or ignored. 0 _B The FR module acknowledge is ignored, it is treated as always asserted 1 _B The FR module acknowledge is used

GSCPERSTAT
GSC Peripheral Status Register

SFR (FF1A_H/8D_H)

Reset Value: FFFF_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USIC 3	USIC 2	USIC 1	USIC 0	FL	MEM	RTC	CCU 63	CCU 62	CCU 61	CCU 60	M CAN	CC2	-	GPT 12E	ADC
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	-	rh	rh

Field	Bits	Type	Description
ADC	0	rh	ADC Acknowledge Status This bit shows the acknowledge status of the modules ADC. 0 _B The modules ADC change currently their kernel state. Their acknowledge has not been received. 1 _B Acknowledge of the modules ADC is taken into account and has been received or is not relevant.
GPT12E	1	rh	GPT12E Acknowledge Status This bit shows the acknowledge status of the modules GPT12E. 0 _B The module GPT12E changes currently its kernel state. Its acknowledge has not been received. 1 _B Acknowledge of the module GPT12E is taken into account and has been received or is not relevant.
CC2	3	rh	CC2 Acknowledge Status This bit shows the acknowledge status of the module CC2. 0 _B The module CC2 changes currently its kernel state. Its acknowledge has not been received. 1 _B Acknowledge of the module CC2 is taken into account and has been received or is not relevant.

System Control Unit (SCU)

Field	Bits	Type	Description
MCAN	4	rh	MultiCAN Acknowledge Status This bit shows the acknowledge status of the module MultiCAN. 0 _B The module MultiCAN changes currently its kernel state. Its acknowledge has not been received. 1 _B Acknowledge of the module MultiCAN is taken into account and has been received or is not relevant.
CCU60	5	rh	CCU60 Acknowledge Status This bit shows the acknowledge status of the module CCU60. 0 _B The module CCU60 changes currently its kernel state. Its acknowledge has not been received. 1 _B Acknowledge of the module CCU60 is taken into account and has been received or is not relevant.
CCU61	6	rh	CCU61 Acknowledge Status This bit shows the acknowledge status of the module CCU61. 0 _B The module CCU61 changes currently its kernel state. Its acknowledge has not been received. 1 _B Acknowledge of the module CCU61 is taken into account and has been received or is not relevant.
CCU62	7	rh	CCU62 Acknowledge Status This bit shows the acknowledge status of the module CCU62. 0 _B The module CCU62 changes currently its kernel state. Its acknowledge has not been received. 1 _B Acknowledge of the module CCU62 is taken into account and has been received or is not relevant.

Field	Bits	Type	Description
CCU63	8	rh	CCU63 Acknowledge Status This bit shows the acknowledge status of the module CCU63. 0_B The module CCU63 changes currently its kernel state. Its acknowledge has not been received. 1_B Acknowledge of the module CCU63 is taken into account and has been received or is not relevant.
RTC	9	rh	RTC Acknowledge Status This bit shows the acknowledge status of the module RTC. 0_B The module RTC changes currently its kernel state. Its acknowledge has not been received. 1_B Acknowledge of the module RTC is taken into account and has been received or is not relevant.
MEM	10	rh	C166SV2 Subsystem Acknowledge Status This bit shows the acknowledge status of the module C166SV2 Subsystem. 0_B The module C166SV2 Subsystem changes currently its kernel state. Its acknowledge has not been received. 1_B Acknowledge of the module C166SV2 Subsystem is taken into account and has been received or is not relevant.
FL	11	rh	Flash Acknowledge Status This bit shows the acknowledge status of the module Flash. 0_B The module Flash changes currently its kernel state. Its acknowledge has not been received. 1_B Acknowledge of the module Flash is taken into account and has been received or is not relevant.

System Control Unit (SCU)

Field	Bits	Type	Description
USIC0	12	rh	USIC0 Acknowledge Status This bit shows the acknowledge status of the module USIC0. 0 _B The module USIC0 changes currently its kernel state. Its acknowledge has not been received. 1 _B Acknowledge of the module USIC0 is taken into account and has been received or is not relevant.
USIC1	13	rh	USIC1 Acknowledge Status This bit shows the acknowledge status of the module USIC1. 0 _B The module USIC1 changes currently its kernel state. Its acknowledge has not been received. 1 _B Acknowledge of the module USIC1 is taken into account and has been received or is not relevant.
USIC2	14	rh	USIC2 Acknowledge Status This bit shows the acknowledge status of the module USIC2. 0 _B The module USIC2 changes currently its kernel state. Its acknowledge has not been received. 1 _B Acknowledge of the module USIC2 is taken into account and has been received or is not relevant.
USIC3	15	rh	USIC3 Acknowledge Status This bit shows the acknowledge status of the module USIC3. 0 _B The module USIC3 changes currently its kernel state. Its acknowledge has not been received. 1 _B Acknowledge of the module USIC3 is taken into account and has been received or is not relevant.

The acknowledge status bit is set, if acknowledge of the module x is taken into account and has been received or is not relevant. The acknowledge of the module x is not relevant if the acknowledge of the module x is not taken into account or the module x currently

System Control Unit (SCU)

does not undergo a change of kernel state mode. In these cases the acknowledge is assumed to be received.

GSCPERSTAT1

GSC Peripheral Status Register

SFR (FE9A_H/4D_H)

Reset Value: FFFF_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						-							FR	-	USIC 4
						-							rh	r	rh

Field	Bits	Type	Description
USIC4	0	rh	USIC4 Acknowledge Status This bit shows the acknowledge status of the module USIC4. 0 _B The module USIC4 changes currently its kernel state. Its acknowledge has not been received. 1 _B Acknowledge of the module USIC4 is taken into account and has been received or is not relevant.
FR	2	rh	FlexRay Acknowledge Status This bit shows, what is assumed for the acknowledge status of the module FR. 0 _B The module FR changes currently its kernel state. Its acknowledge has not been received. 1 _B Acknowledge of the module FR is taken into account and has been received or is not relevant.
1	[15:3]	r	Reserved Read as 1

The acknowledge status bit is set, if acknowledge of the module x is taken into account and has been received or is not relevant. The acknowledge of the module x is not relevant if the acknowledge of the module x is not taken into account or the module x currently does not undergo a change of kernel state mode. In these cases the acknowledge is assumed to be received.

9.8 Software Boot Support

In order to determine the correct starting point of operation for the software a minimum of hardware support is required. As much as possible is done via software. Some decisions have to be done in hardware because they must be known before any software is operational.

9.9 External Request Unit (ERU)

The External Request Unit (ERU) is a versatile event and pattern detection unit. Its major task is the **generation of interrupts based on selectable trigger events at different inputs**, e.g. to generate external interrupt requests if an edge occurs at an input pin.

The detected events can also be used by other modules to trigger or to gate module-specific actions, such as conversions of the ADC module.

9.9.1 Introduction

The ERU of the XC27x8X can be split in three main functional parts:

- 4 independent **Input Channels x** for input selection and conditioning of trigger or gating functions
- Event distribution: A **Connecting Matrix** defines the events of the Input Channel x that lead to a reaction of an Output Channel y.
- 4 independent **Output Channels y** for combination of events, definition of their effects and distribution to the system (interrupt generation, ADC conversion triggers)

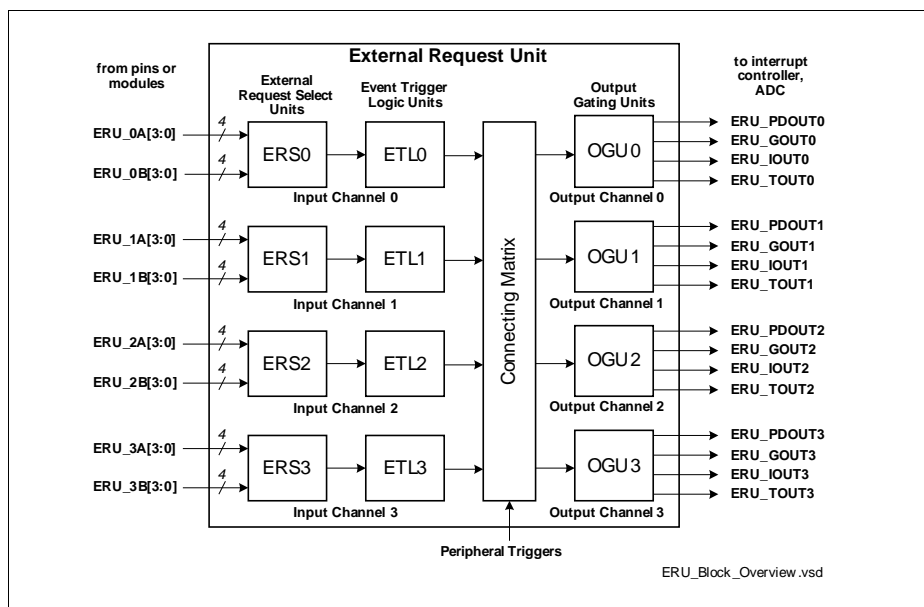


Figure 9-22 External Request Unit Overview

These tasks are handled by the following building blocks:

- An **External Request Select Unit (ERSx)** per Input Channel allows the selection of one out of two or a logical combination of two input signals (ERU_xA, ERU_xB) to a

System Control Unit (SCU)

common trigger. For each of these two signals, an input vector of 4 possible inputs is available (e.g. the actual input ERU_xA can be selected from one of the ERU inputs ERU_xA[3:0], similar for ERU_xB).

- An **Event Trigger Logic (ETLx)** per Input Channel allows the definition of the transition (edge selection, or by software) that lead to a trigger event and can also store this status. Here, the input levels of the selected signals are translated into events (event detected = event flag becomes set, independent of the polarity of the original input signals).
- The **Connecting Matrix** distributes the events and status flags generated by the Input Channels to the Output Channels. Additionally, some Peripheral Trigger signals from other modules (e.g. CC2) are made available and can be combined with the triggers generated by the Input Channels of the ERU.
- An **Output Gating Unit (OGUy)** per Output Channel that combines the available trigger events and status information from the Input Channels. An event of one Input Channel can lead to reactions of several Output Channels, or also events of several Input Channels can be combined to a reaction of one Output Channel (pattern detection).

Different types of reactions are possible, e.g. interrupt generation (based on signals ERU_IOUTy), triggering of ADC conversions (based on signals ERU_TOUTy), or gating of ADC conversions (based on signals ERU_GOUTy).

The ERU is controlled by a number of registers, shown in [Figure 9-23](#), and described in [Section 9.9.8](#).

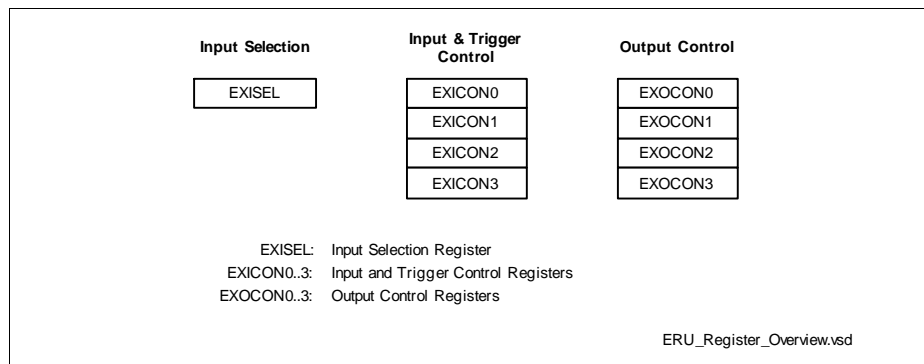


Figure 9-23 ERU Registers Overview

9.9.2 ERU Input Connections

The inputs to the ERU can be selected from a large number of input signals. While some of the inputs come directly from a pin, other inputs use signals from various peripheral modules, such as the USIC (signals named with prefix UxCy to indicate the communication channel) and the MultiCAN modules. These signals are input signals from the pin that has been selected as input for a USIC or MultiCAN function. The selection of the input is made within the respective USIC or MultiCAN module.

Usually, such signals would be selected for an ERU function when the input function to the USIC or MultiCAN module is not used otherwise, or the module is not used at all. However, it is also possible to select a input which is actually needed in a USIC or MultiCAN module, and to use it also in the ERU to provide a certain trigger functions, eventually combined with other signals (e.g. to generate an interrupt trigger in case a start of frame is detected at a selected communication).

With this structure, the number of possible input pins is significantly increased, because not only the selection capability of the ERU is used, but also the selection capability of the communication modules.

Note: All functional inputs of the ERU are synchronized to f_{SYS} before they can affect the internal logic. The resulting delay of $2/f_{SYS}$ and an uncertainty of $1/f_{SYS}$ have to be taken into account for precise timing calculation.

An edge of an input can only be correctly detected if both, the high phase and the low phase of the input are each longer than $1/f_{SYS}$.

The following figure shows the ERU input connections, either directly with pins or via communication modules, such as USIC or MultiCAN. These communication modules provide their input signals (e.g. CAN receive input, or USIC data, clock, or control inputs) that have been selected in these modules.

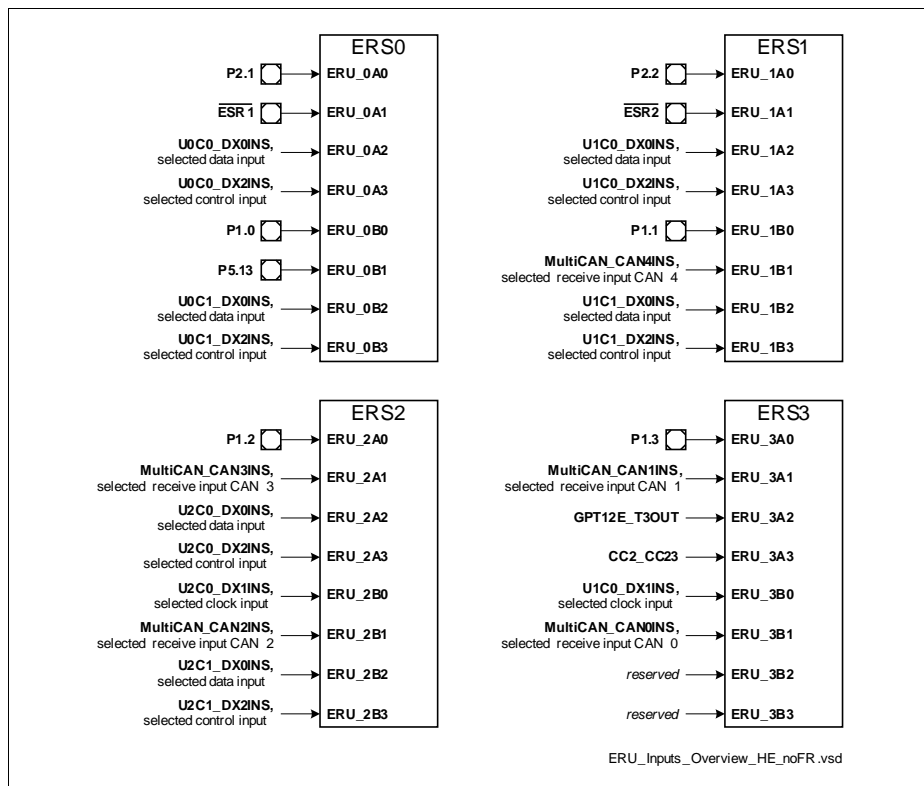


Figure 9-24 ERU Inputs Overview

System Control Unit (SCU)

The following table describes the ERU input connections for the ERSx stages. The selection is defined by the bit fields in register **EXISEL**.

Table 9-13 ERSx Connections in XC27x8X

Input	from/to Module	I/O to ERSx	Can be used to/as
-------	-------------------	----------------	-------------------

ERS0 Inputs

ERU_0A0	P2.1	I	ERS0 input A
ERU_0A1	ESR1	I	
ERU_0A2	U0C0_DX0INS	I	
ERU_0A3	U0C0_DX2INS	I	
ERU_0B0	P1.0	I	ERS0 input B
ERU_0B1	P5.13	I	
ERU_0B2	U0C1_DX0INS	I	
ERU_0B3	U0C1_DX2INS	I	

ERS1 Inputs

ERU_1A0	P2.2	I	ERS1 input A
ERU_1A1	ESR2	I	
ERU_1A2	U1C0_DX0INS	I	
ERU_1A3	U1C0_DX2INS	I	
ERU_1B0	P1.1	I	ERS1 input B
ERU_1B1	MultiCAN_CAN4INS	I	
ERU_1B2	U1C1_DX0INS	I	
ERU_1B3	U1C1_DX2INS	I	

ERS2 Inputs

ERU_2A0	P1.2	I	ERS2 input A
ERU_2A1	MultiCAN_CAN3INS	I	
ERU_2A2	U2C0_DX0INS	I	
ERU_2A3	U2C0_DX2INS	I	

Table 9-13 ERSx Connections in XC27x8X (cont'd)

Input	from/to Module	I/O to ERSx	Can be used to/as
ERU_2B0	U2C0_DX1INS	I	ERS2 input B
ERU_2B1	MultiCAN_CAN2INS	I	
ERU_2B2	U2C1_DX0INS	I	
ERU_2B3	U2C1_DX2INS	I	

ERS3 Inputs

ERU_3A0	P1.3	I	ERS3 input A
ERU_3A1	MultiCAN_CAN1INS	I	
ERU_3A2	GPT12E_T3OUT	I	
ERU_3A3	CC2_CC23	I	
ERU_3B0	U1C0_DX1INS	I	ERS3 input B
ERU_3B1	MultiCAN_CAN0INS	I	
ERU_3B2	0	I	
ERU_3B3	0	I	

9.9.3 External Request Select Unit (ERSx)

For each Input Channel x ($x = 0-3$), an ERS x unit handles the input selection for the associated ETL x unit. Each ERS x performs a logical combination of two signals (A_x , B_x) to provide one combined output ERS x O to the associated ETL x . Input A_x can be selected from 4 options of the input vector ERU_ x A[3:0] and can be optionally inverted. A similar structure exists for input B_x (selection from ERU_ x B[3:0]).

In addition to the direct choice of either input A_x or B_x or their inverted values, the possible logical combinations for two selected inputs are a logical AND or a logical OR.

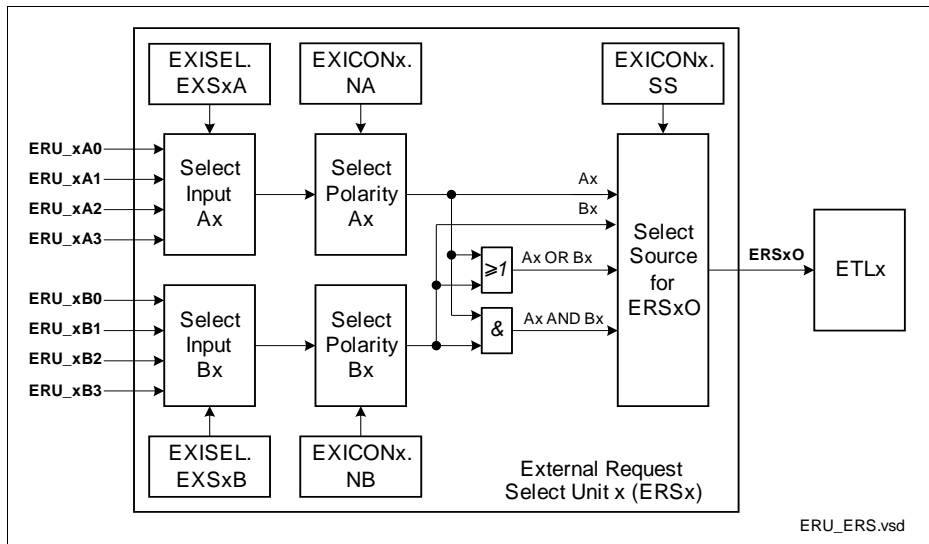


Figure 9-25 External Request Select Unit Overview

The ERS units are controlled via register **EXISEL** (one register for all four ERS x units) and registers EXICON x (one register for each ERS x and associated ETL x unit, e.g. **EXICON0** for Input Channel 0).

9.9.4 Event Trigger Logic (ETLx)

For each Input Channel x ($x = 0-3$), an event trigger logic ETLx derives a trigger event and a status from the input ERUxO delivered by the associated ERSx unit. Each ETLx is based on an edge detection block, where the detection of a rising or a falling edge can be individually enabled. Both edges lead to a trigger event if both enable bits are set (e.g. to handle a toggling input).

Each of the four ETLx units has an associated EXICONx register, that controls all options of an ETLx (the register also holds control bits for the associated ERSx unit, e.g. **EXICON0** to control ESR0 and ETLO).

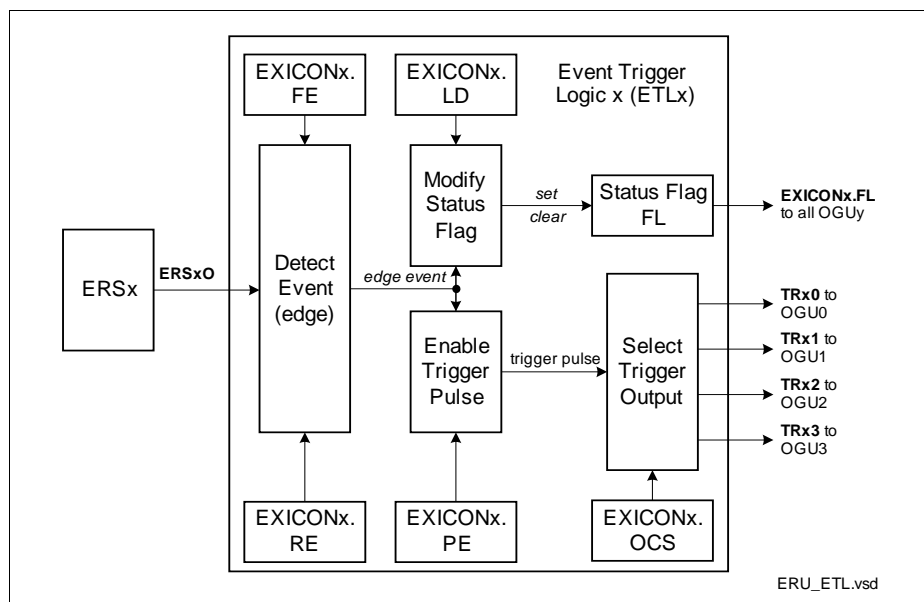


Figure 9-26 Event Trigger Logic Overview

When the selected event (edge) is detected, the status flag EXICONx.FL becomes set. This flag can also be modified by software (set or clear). Two different operating modes are supported by this status flag.

It can be used as “sticky” flag, that is set by hardware when the desired event has been detected and has to be cleared by software. In this operating mode, it indicates that the event has taken place, but without indicating the actual status of the input.

In the second operating mode, it is cleared automatically if the “opposite” event is detected. For example, if only the falling edge detection is enabled to set the status flag, it is cleared when the rising edge is detected. In this mode, it can be used for pattern

System Control Unit (SCU)

detection where the actual status of the input is important (enabling both edge detections is not useful in this mode).

The output of the status flag is connected to all following Output Gating Units (OGUy) in parallel (see [Figure 9-27](#)) to provide **pattern detection capability of all OGUy** units based on different or the same status flags.

In addition to the modification of the status flag, a trigger pulse output TRxy of ETLx can be enabled (by bit EXICONx.PE) and selected to **trigger actions in one of the OGUy** units. The target OGUy for the trigger is selected by bit field EXICON.OCS.

The trigger becomes active when the selected edge event is detected, independently from the status flag EXICONx.FL.

9.9.5 Connecting Matrix

The connecting matrix distributes the trigger signals (TRxy) and status signals (EXICONx.FL) from the different ETLx units between the OGUy units. In addition, it receives peripheral trigger signals that can be OR-combined with the ETLx trigger signals in the OGUy units. **Figure 9-27** provides a complete overview of the connections between the ETLx and the OGUy units.

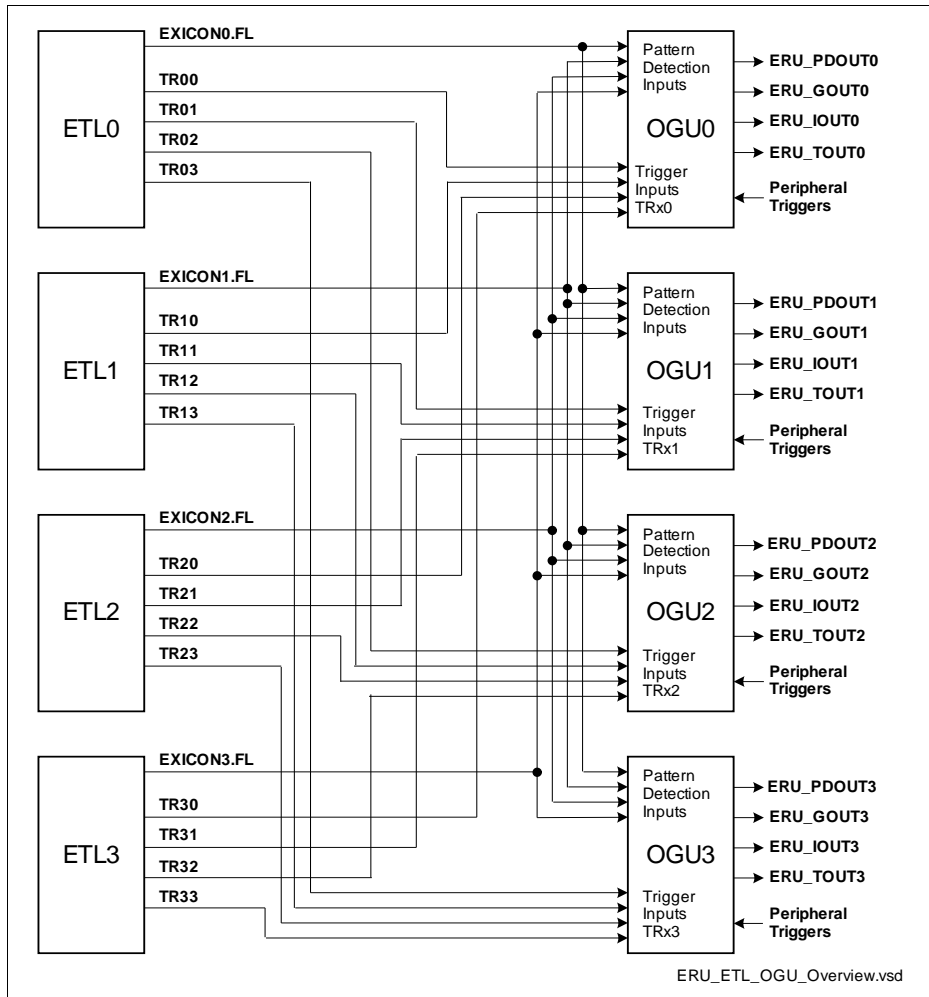


Figure 9-27 Connecting Matrix between ETLx and OGUy

9.9.6 Output Gating Unit (OGUy)

Each OGUy (y = 0-3) unit combines the available trigger events and status flags from the Input Channels and distributes the results to the system. **Figure 9-28** illustrates the logic blocks within an OGUy unit. All functions of an OGUy unit are controlled by its associated EXOCONy register, e.g. **EXOCON0** for OGU0. The function of an OGUy unit can be split into two parts:

- **Trigger combination** (see **Section 9.9.6.1**):
All trigger signals TRxy from the Input Channels that are enabled and directed to OGUy, a selected peripheral-related trigger event, and a pattern change event (if enabled) are logically OR-combined.
- **Pattern detection** (see **Section 9.9.6.2**):
The status flags EXICONx.FL of the Input Channels can be enabled to take part in the pattern detection. A pattern match is detected while all enabled status flags are set.

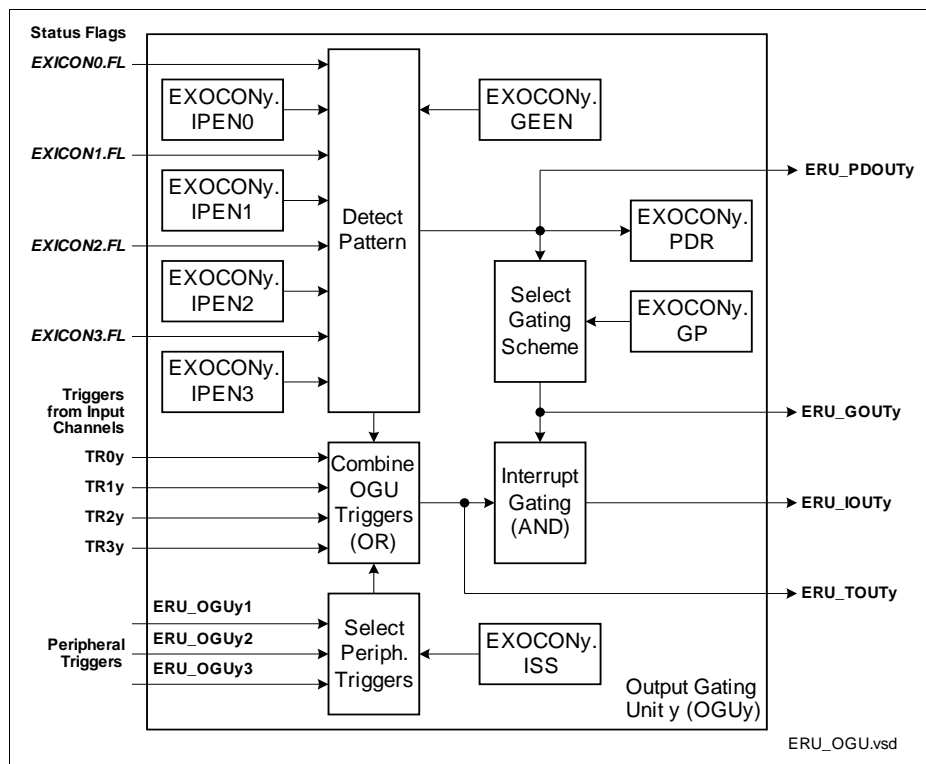


Figure 9-28 Output Gating Unit for Output Channel y

System Control Unit (SCU)

Each OGUy unit generates 4 output signals that are distributed to the system (not all of them are necessarily used, please refer to [Section 9.9.7](#)):

- **ERU_PDOUTy** to directly output the pattern match information for gating purposes in other modules (pattern match = 1).
- **ERU_GOUTy** to output the pattern match or pattern miss information (inverted pattern match), or a permanent 0 or 1 under software control for gating purposes in other modules.
- **ERU_TOUTy** as combination of a peripheral trigger, a pattern detection result change event, or the ETLx trigger outputs TRxy to trigger actions in other modules.
- **ERU_IOUTy** as gated trigger output (ERU_GOUTy logical AND-combined with ERU_TOUTy) to trigger interrupts (e.g. the interrupt generation can be gated to allow interrupt activation during a certain time window).

Note: An unexpected falling edge on ERU_PDOUTx could trigger a trap interrupt in CCU6 if using an improper initialization sequence. Therefore, initialize ERU_PDOUTx prior to the configuration of other modules (e.g. CCU6 and ADC).

9.9.6.1 Trigger Combination

The trigger combination logically OR-combines different trigger inputs to form a common trigger ERU_TOUTy. Possible trigger inputs are:

- In each ETLx unit of the **Input Channels**, the trigger output TRxy can be enabled and the trigger event can be directed to one of the OGUy units.
- One out of three **peripheral trigger** signals per OGUy can be selected as additional trigger source. These peripheral triggers are generated by on-chip peripheral modules, such as capture/compare or timer units. The selection is done by bit field EXOCONy.ISS.
- In the case that at least one **pattern detection** input is enabled (EXOCONy.IPENx) and a change of the pattern detection result from pattern match to pattern miss (or vice-versa) is detected, a trigger event is generated to indicate a pattern detection result event (if enabled by ECOCONy.GEEN).

The trigger combination offers the possibility to program different trigger criteria for several input signals (independently for each Input Channel) or peripheral signals, and to combine their effects to a single output, e.g. to generate an interrupt or to start an ADC conversion. This combination capability allows the generation of an interrupt per OGU that can be triggered by several inputs (multitude of request sources -> one reaction).

The following table describes the peripheral trigger connections for the OGUy stages.

The selection is defined by the bit fields ISS in registers **EXOCON0** (for OGU0), **EXOCON1** (for OGU1), **EXOCON2** (for OGU2), or **EXOCON3** (for OGU3).

Table 9-14 OGUy Peripheral Trigger Connections in XC27x8X

Input	from/to Module	I/O to OGUy	Can be used to/as
-------	----------------	-------------	-------------------

OGU0 Inputs

ERU_OGU01	CCU60_MCM_ST	I	Peripheral triggers for OGU0
ERU_OGU02	CCU60_T13_PM	I	
ERU_OGU03	CC2_28	I	

OGU1 Inputs

ERU_OGU11	CCU61_MCM_ST	I	Peripheral triggers for OGU1
ERU_OGU12	CCU61_T13_PM	I	
ERU_OGU13	CC2_29	I	

OGU2 Inputs

ERU_OGU21	CCU62_MCM_ST	I	Peripheral triggers for OGU2
ERU_OGU22	CCU62_T13_PM	I	
ERU_OGU23	CC2_30	I	

OGU3 Inputs

ERU_OGU31	CCU63_MCM_ST	I	Peripheral triggers for OGU3
ERU_OGU32	CCU63_T13_PM	I	
ERU_OGU33	CC2_31	I	

9.9.6.2 Pattern Detection

The pattern detection logic allows the combination of the status flags of all ETLx units. Each status flag can be individually included or excluded from the pattern detection for each OGUy, via control bits EXOCONy.IPENx. The pattern detection block outputs the following pattern detection results:

- **Pattern match** (EXOCONy.PDR = 1 and ERU_PDOUTy = 1):
A pattern match is indicated while all status flags FL that are included in the pattern detection are 1.
- **Pattern miss** (EXOCONy.PDR = 0 and ERU_PDOUTy = 0):
A pattern miss is indicated while at least one of the status flags FL that are included in the pattern detection is 0.

System Control Unit (SCU)

In addition, the pattern detection can deliver a trigger event if the pattern detection result changes from match to miss or vice-versa (if enabled by EXOCONy.GEEN = 1). The pattern result change event is logically OR-combined with the other enabled trigger events to support interrupt generation or to trigger other module functions (e.g. in the ADC). The event is indicated when the pattern detection result changes and EXOCONy.PDR becomes updated.

The interrupt generation in the OGUy is based on the trigger ERU_TOUTy that can be gated (masked) with the pattern detection result ERU_PDOUTy. This allows an automatic and reproducible generation of interrupts during a certain time window, where the request event is elaborated by the trigger combination block and the time window information (gating) is given by the pattern detection. For example, interrupts can be issued on a regular time base (peripheral trigger input from capture/compare unit is selected) while a combination of input signals occurs (pattern detection based on ETLx status bits).

A programmable gating scheme introduces flexibility to adapt to application requirements and allows the generation of interrupt requests ERU_IOUTy under different conditions:

- **Pattern match** (EXOCONy.GP = 10_B):
An interrupt request is issued when a trigger event occurs while the pattern detection shows a pattern match.
- **Pattern miss** (EXOCONy.GP = 11_B):
An interrupt request is issued when the trigger event occurs while the pattern detection shows a pattern miss.
- **Independent of pattern detection** (EXOCONy.GP = 01_B):
In this mode, each occurring trigger event leads to an interrupt request. The pattern detection output can be used independently from the trigger combination for gating purposes of other peripherals (independent use of ERU_TOUTy and ERU_PDOUTy with interrupt requests on trigger events).
- **No interrupts** (EXOCONy.GP = 00_B, default setting)
In this mode, an occurring trigger event does not lead to an interrupt request. The pattern detection output can be used independently from the trigger combination for gating purposes of other peripherals (independent use of ERU_TOUTy and ERU_PDOUTy without interrupt requests on trigger events).

9.9.7 ERU Output Connections

The following table describes the connections of the ERU output signals for gating or triggering other module functions, as well as the connections to the interrupt control registers.

Table 9-15 ERU Output Connections in XC27x8X

Output	from/to Module	I/O to OGUy	Can be used to/as
--------	-------------------	----------------	-------------------

OGU0 Outputs

ERU_PDOUT0	ADC0 (REQGT0E) ADC0 (REQGT1E) ADC0 (REQGT2E) ADC1 (REQGT0E) ADC1 (REQGT1E) ADC1 (REQGT2E) FR (STPWT0)	O	Pattern detection output
ERU_GOUT0	not connected	O	Gated pattern detection output
ERU_TOUT0	not connected	O	Trigger output
ERU_IOUT0	ITC (SCU_ERU_0IC)	O	Interrupt output

OGU1 Outputs

ERU_PDOUT1	ADC0 (REQGT0F) ADC0 (REQGT1F) ADC0 (REQGT2F) ADC1 (REQGT0F) ADC1 (REQGT1F) ADC1 (REQGT2F) FR (STPWT1)	O	Pattern detection output
ERU_GOUT1	not connected	O	Gated pattern detection output
ERU_TOUT1	ADC0 (REQTR0B) ADC0 (REQTR1B) ADC0 (REQTR2B) ADC1 (REQTR0B) ADC1 (REQTR1B) ADC1 (REQTR2B)	O	Trigger output

System Control Unit (SCU)

Table 9-15 ERU Output Connections in XC27x8X (cont'd)

Output	from/to Module	I/O to OGUy	Can be used to/as
ERU_IOUT1	ITC (SCU_ERU_1IC)	O	Interrupt output

OGU2 Outputs

ERU_PDOUT2	FR (STPWT2) CCU60 (CTRAPD)	O	Pattern detection output
ERU_GOUT2	not connected	O	Gated pattern detection output
ERU_TOUT2	not connected	O	Trigger output
ERU_IOUT2	ITC (SCU_ERU_2IC)	O	Interrupt output

OGU3 Outputs

ERU_PDOUT3	FR (STPWT3) CCU63 (CTRAPD)	O	Pattern detection output
ERU_GOUT3	not connected	O	Gated pattern detection output
ERU_TOUT3	not connected	O	Trigger output
ERU_IOUT3	ITC (SCU_ERU_3IC)	O	Interrupt output

9.9.8 ERU Registers

9.9.8.1 External Input Selection Register EXISEL

This register selects the A and B inputs for all four ERS units. The possible input signals are given in [Table 9-13](#).

EXISEL

External Input Select Register ESFR (F1A0_H/D0_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXS3B		EXS3A		EXS2B		EXS2A		EXS1B		EXS1A		EXS0B		EXS0A	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
EXS0A	[1:0]	rw	External Source Select for A0 (ERS0) This bit field defines which input is selected for A0. 00 _B Input ERU_0A0 is selected 01 _B Input ERU_0A1 is selected 10 _B Input ERU_0A2 is selected 11 _B Input ERU_0A3 is selected
EXS0B	[3:2]	rw	External Source Select for B0 (ERS0) This bit field defines which input is selected for B0. 00 _B Input ERU_0B0 is selected 01 _B Input ERU_0B1 is selected 10 _B Input ERU_0B2 is selected 11 _B Input ERU_0B3 is selected
EXS1A	[5:4]	rw	External Source Select for A1 (ERS1) This bit field defines which input is selected for A1. 00 _B Input ERU_1A0 is selected 01 _B Input ERU_1A1 is selected 10 _B Input ERU_1A2 is selected 11 _B Input ERU_1A3 is selected
EXS1B	[7:6]	rw	External Source Select for B1 (ERS1) This bit field defines which input is selected for B1. 00 _B Input ERU_1B0 is selected 01 _B Input ERU_1B1 is selected 10 _B Input ERU_1B2 is selected 11 _B Input ERU_1B3 is selected

Field	Bits	Type	Description
EXS2A	[9:8]	rw	External Source Select for A2 (ERS2) This bit field defines which input is selected for A2. 00 _B Input ERU_2A0 is selected 01 _B Input ERU_2A1 is selected 10 _B Input ERU_2A2 is selected 11 _B Input ERU_2A3 is selected
EXS2B	[11:10]	rw	External Source Select for B2 (ERS2) This bit field defines which input is selected for B2. 00 _B Input ERU_2B0 is selected 01 _B Input ERU_2B1 is selected 10 _B Input ERU_2B2 is selected 11 _B Input ERU_2B3 is selected
EXS3A	[13:12]	rw	External Source Select for A3 (ERS3) This bit field defines which input is selected for A3. 00 _B Input ERU_3A0 is selected 01 _B Input ERU_3A1 is selected 10 _B Input ERU_3A2 is selected 11 _B Input ERU_3A3 is selected
EXS3B	[15:14]	rw	External Source Select for B3 (ERS3) This bit field defines which input is selected for B3. 00 _B Input ERU_3B0 is selected 01 _B Input ERU_3B1 is selected 10 _B Input ERU_3B2 is selected 11 _B Input ERU_3B3 is selected

9.9.8.2 External Input Control Registers EXICONx

These registers control the inputs of the ERSx unit and the trigger functions of the ETLx units (x = 0..3).

EXICON0

External Input Control 0 Register

ESFR (F030_H/18_H)

Reset Value: 0000_H

EXICON1

External Input Control 1 Register

ESFR (F032_H/19_H)

Reset Value: 0000_H

EXICON2

External Input Control 2 Register

ESFR (F034_H/1A_H)

Reset Value: 0000_H

EXICON3

External Input Control 3 Register

ESFR (F036_H/1C_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				NB	NA	SS		FL	OCS			FE	RE	LD	PE
r				rw	rw	rw		rwh	rw			rw	rw	rw	rw

Field	Bits	Type	Description
PE	0	rw	Output Trigger Pulse Enable for ETLx This bit enables the generation of an output trigger pulse at TRxy when the selected edge is detected (set condition for the status flag FL). 0 _B The trigger pulse generation is disabled 1 _B The trigger pulse generation is enabled

Field	Bits	Type	Description
LD	1	rw	Rebuild Level Detection for Status Flag for ETLx This bit selects if the status flag FL is used as “sticky” bit or if it rebuilds the result of a level detection. 0 _B The status flag FL is not cleared by hardware and is used as “sticky” bit. Once set, it is not influenced by any edge until it becomes cleared by software. 1 _B The status flag FL rebuilds a level detection of the desired event. It becomes automatically set with a rising edge if RE = 1 or with a falling edge if FE = 1. It becomes automatically cleared with a rising edge if RE = 0 or with a falling edge if FE = 0.
RE	2	rw	Rising Edge Detection Enable ETLx This bit enables/disables the rising edge event as edge event as set condition for the status flag FL or as possible trigger pulse for TRxy. 0 _B A rising edge is not considered as edge event 1 _B A rising edge is considered as edge event
FE	3	rw	Falling Edge Detection Enable ETLx This bit enables/disables the falling edge event as edge event as set condition for the status flag FL or as possible trigger pulse for TRxy. 0 _B A falling edge is not considered as edge event 1 _B A falling edge is considered as edge event
OCS	[6:4]	rw	Output Channel Select for ETLx Output Trigger Pulse This bit field defines which Output Channel OGUy is targeted by an enabled trigger pulse TRxy. 000 _B Trigger pulses are sent to OGU0 001 _B Trigger pulses are sent to OGU1 010 _B Trigger pulses are sent to OGU2 011 _B Trigger pulses are sent to OGU3 1XX _B Reserved, do not use this combination
FL	7	rwh	Status Flag for ETLx This bit represents the status flag that becomes set or cleared by the edge detection. 0 _B The enabled edge event has not been detected 1 _B The enabled edge event has been detected

System Control Unit (SCU)

Field	Bits	Type	Description
SS	[9:8]	rw	Input Source Select for ERSx This bit field defines which logical combination is taken into account as ESRxO. 00 _B Input A without additional combination 01 _B Input B without additional combination 10 _B Input A OR input B 11 _B Input A AND input B
NA	10	rw	Input A Negation Select for ERSx This bit selects the polarity for the input A. 0 _B Input A is used directly 1 _B Input A is inverted
NB	11	rw	Input B Negation Select for ERSx This bit selects the polarity for the input B. 0 _B Input B is used directly 1 _B Input B is inverted
0	[15:12]	r	Reserved Read as 0; should be written with 0.

9.9.8.3 Output Control Registers EXOCONy

These registers control the outputs of the Output Gating Unit y (y = 0..3).

EXOCON0

External Output Trigger Control 0 Register

SFR (FE30_H/18_H)

Reset Value: 0008_H

EXOCON1

External Output Trigger Control 1 Register

SFR (FE32_H/19_H)

Reset Value: 0008_H

EXOCON2

External Output Trigger Control 2 Register

SFR (FE34_H/1A_H)

Reset Value: 0008_H

EXOCON3

External Output Trigger Control 3 Register

SFR (FE36_H/1B_H)

Reset Value: 0008_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IPEN 3	IPEN 2	IPEN 1	IPEN 0	0						GP		PDR	GE EN	ISS	
rw	rw	rw	rw	r						rw		rh	rw	rw	

Field	Bits	Type	Description
ISS	[1:0]	rw	Internal Trigger Source Selection This bit field defines which input is selected as peripheral trigger input for OGUy. The possible input signals are given in Table 9-14 . 00 _B The peripheral trigger function is disabled 01 _B Input ERU_OGUy1 is selected 10 _B Input ERU_OGUy2 is selected 11 _B Input ERU_OGUy3 is selected
GEEN	2	rw	Gating Event Enable Bit GEEN enables the generation of a trigger event when the result of the pattern detection changes from match to miss or vice-versa. 0 _B The event detection is disabled 1 _B The event detection is enabled
PDR	3	rh	Pattern Detection Result Flag This bit represents the pattern detection result. 0 _B A pattern miss is detected 1 _B A pattern match is detected

System Control Unit (SCU)

Field	Bits	Type	Description
GP	[5:4]	rw	Gating Selection for Pattern Detection Result This bit field defines the gating scheme for the interrupt generation (relation between the OGU output ERU_PDOUTy and ERU_GOUTy). 00 _B ERU_GOUTy is always disabled and ERU_IOUTy can not be activated 01 _B ERU_GOUTy is always enabled and ERU_IOUTy becomes activated with each activation of ERU_TOUTy 10 _B ERU_GOUTy is equal to ERU_PDOUTy and ERU_IOUTy becomes activated with an activation of ERU_TOUTy while the desired pattern is detected (pattern match PDR = 1) 11 _B ERU_GOUTy is inverted to ERU_PDOUTy and ERU_IOUTy becomes activated with an activation of ERU_TOUTy while the desired pattern is not detected (pattern miss PDR = 0)
IPENx (x = 0-3)	12+x	rw	Pattern Detection Enable for ETLx Bit IPENx defines whether the trigger event status flag EXICONx.FL of ETLx takes part in the pattern detection of OGUy. 0 _B Flag EXICONx.FL is excluded from the pattern detection 1 _B Flag EXICONx.FL is included in the pattern detection
0	[11:6]	r	Reserved Read as 0; should be written with 0.

9.10 SCU Interrupt Generation

The interrupt structure of the SCU is shown in **Figure 9-29**.

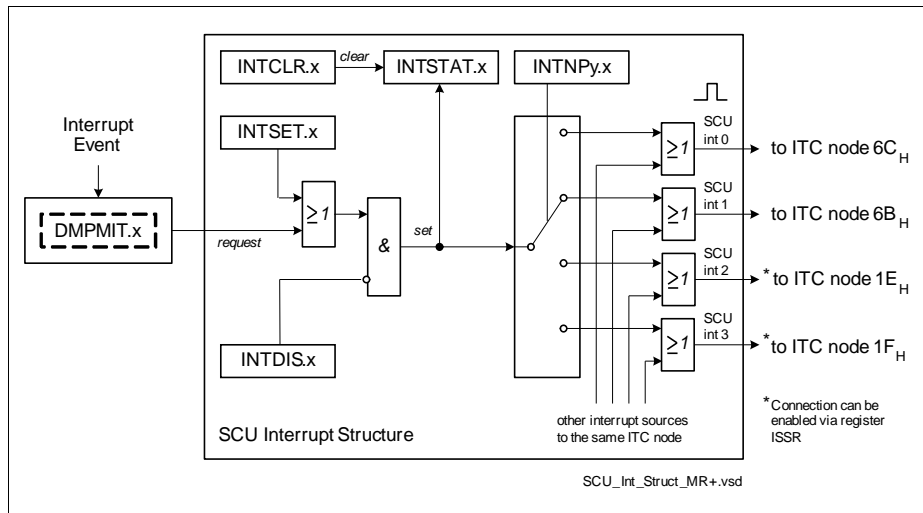


Figure 9-29 SCU Interrupt Structure

If enabled by the corresponding bit in register **INTDIS**, an interrupt is triggered either by the incoming interrupt request line, or by a software set of the respective bit in register **INTSET**. The trigger sets the respective flag in register **INTSTAT** and is gated to one of the interrupt nodes, selected by the node pointer registers **INTNP0** or **INTNP1**.

The interrupt flag can be cleared by software by writing to the corresponding bit in register **INTCLR**.

If more than one interrupt source is connected to the same interrupt node pointer (in register **INTNPx**), the requests are combined to one common line.

Attention: *Following a reset, the SCU interrupts are enabled by default (register **INTDIS** = 0000_H). This may lead to interrupt requests being triggered in the SCU immediately, even before user software has begun to execute. In the SCU, multiple interrupt sources are 'ORed' to a common interrupt node of the CPU interrupt controller. Due to the "ORing" of multiple interrupt sources, only one interrupt request to the interrupt controller will be generated if multiple sources at the input of this OR gate are active at the same time. If user software enables an interrupt in the interrupt controller (SCU_xIC) which shares the same node as the SCU interrupt request active after reset, it may lead to the effect of suppressing the intended interrupt source. So, for all SCU interrupt*

sources which will not be used, make sure to disable the interrupt source (SCU_INTDIS) and clear any pending request flags (SCU_xIC.IR) before enabling interrupts in interrupt controller.

Interrupt Node Assignment

The interrupt sources of the SCU module can be mapped to the dedicated interrupt node 6C_H or 6B_H by programming the interrupt node pointer registers INTNP0 and INTNP1.

Furthermore, If the CAPCOM2 interrupts for channels 30 or 31 are not used the SCU interrupts can be mapped via register ISSR to the interrupt nodes 1E_H or 1F_H which are assigned to the CAPCOM2 interrupts. So for the SCU interrupts can be selected the interrupt node 6C_H, 6B_H, or in addition via register ISSR the node 1E_H or 1F_H.

The default assignment of the interrupt sources to the nodes and their corresponding control registers are shown in [Table 9-16](#).

9.10.1 Interrupt Support

Some of the interrupt requests are first fed through a sticky flag register in the DMP_M domain. These flags are set with a trigger and if set trigger the interrupt generation in the DMP_1..

Which of the interrupt requests have a sticky flag in register **DMPMIT** is listed in [Table 9-16](#).

*Note: When servicing an SCU interrupt request, make sure that all related request flags are cleared after the identified request has been handled. To clear an interrupt request that is stored in register DMPMIT, first clear the request source of the source (e.g. WUTRG), clear the request within DMP_M via **DMPMITCLR**, and then clear the request within DMP_1 via INTCLR.*

9.10.2 SCU Interrupt Sources

The SCU receives the interrupt request lines listed in [Table 9-16](#).

Table 9-16 SCU Interrupt Overview

Source of Interrupt	Short Name	Sticky Flag in DMPMIT	Default Interrupt Node Assignment in INTNPx
SWD OK 1 Interrupt	SWDI1	yes	6C _H
SWD OK 2 Interrupt	SWDI2	yes	6B _H
PVC_M OK 1 Interrupt	PVCMI1	yes	6C _H
PVC_M OK 2 Interrupt	PVCMI2	yes	6B _H
PVC_1 OK 1 Interrupt	PVC111	yes	6C _H

System Control Unit (SCU)

Table 9-16 SCU Interrupt Overview (cont'd)

Source of Interrupt	Short Name	Sticky Flag in DMPMIT	Default Interrupt Node Assignment in INTNPx
PVC_1 OK 2 Interrupt	PVC1I2	yes	6B _H
Wake-up Timer Interrupt	WUI	yes	6B _H
Wake-up Timer Trim Interrupt	WUTI	yes	6C _H
Watchdog Timer Interrupt	WDTI	---	6B _H
GSC Interrupt	GSCI	yes	6C _H
STM0 Interrupt	STM0I	yes	6B _H
STM1 Interrupt	STM1I	yes	6C _H
MCHK Interrupt	MCHKI	---	6B _H
Program Flash Interrupt	PFI	---	6C _H

9.10.3 Interrupt Control Registers

9.10.3.1 Register INTSTAT

This register contains the status flags for all interrupt request trigger sources of the SCU. For setting and clearing of these status bits by software see registers INTSET and INTCLR, respectively.

INTSTAT

Interrupt Status Register

SFR (FF00_H/80_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	PF I	M CHK I	STM 1 I	STM 0 I	GSC I	WDT I	WU I	WUT I	PVC 1 I2	PVC 1 I1	PVC M I2	PVC M I1	SWD I2	SWD I1	
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
SWDI1	0	rh	SWD Interrupt Request Flag 1 This bit is set if bit DMPMIT.SWDI1 is set. 0 _B No SWDI1 interrupt trigger has occurred since this bit was cleared the last time 1 _B A SWDI1 interrupt trigger has occurred since this bit was cleared the last time
SWDI2	1	rh	SWD Interrupt Request Flag 2 This bit is set if bit DMPMIT.SWDI2 is set. 0 _B No SWDI2 interrupt trigger has occurred since this bit was cleared the last time 1 _B A SWDI2 interrupt trigger has occurred since this bit was cleared the last time
PVCMI1	2	rh	PVC_M Interrupt Request Flag 1 This bit is set if bit DMPMIT.PVCMI1 is set. 0 _B No PVCMI1 interrupt trigger has occurred since this bit was cleared the last time 1 _B A PVCMI1 interrupt trigger has occurred since this bit was cleared the last time

Field	Bits	Type	Description
PVCM12	3	rh	PVC_M Interrupt Request Flag 2 This bit is set if bit DMPMIT.PVCM12 is set. 0 _B No PVCM12 interrupt trigger has occurred since this bit was cleared the last time 1 _B A PVCM12 interrupt trigger has occurred since this bit was cleared the last time
PVC111	4	rh	PVC_1 Interrupt Request Flag 1 This bit is set if bit DMPMIT.PVC111 is set. 0 _B No PVC111 interrupt trigger has occurred since this bit was cleared the last time 1 _B A PVC11 interrupt trigger has occurred since this bit was cleared the last time
PVC112	5	rh	PVC_1 Interrupt Request Flag 2 This bit is set if bit DMPMIT.PVC112 is set. 0 _B No PVC112 interrupt trigger has occurred since this bit was cleared the last time 1 _B A PVC112 interrupt trigger has occurred since this bit was cleared the last time
WUTI	6	rh	Wake-up Timer Trim Interrupt Request Flag This bit is set if the WUT trim trigger event occur and bit is INTDIS.WUTI = 0. 0 _B No WUT interrupt trigger has occurred since this bit was cleared the last time 1 _B A WUT interrupt trigger has occurred since this bit was cleared the last time
WUI	7	rh	Wake-up Timer Interrupt Request Flag This bit is set if the WU trigger event occur and bit is INTDIS.WUI = 0. 0 _B No WU interrupt trigger has occurred since this bit was cleared the last time 1 _B A WU interrupt trigger has occurred since this bit was cleared the last time
WDTI	8	rh	Watchdog Timer Interrupt Request Flag This bit is set if the WDT Prewarning Mode is entered and bit is INTDIS.WDTI = 0. 0 _B No WDT interrupt trigger has occurred since this bit was cleared the last time 1 _B A WDT interrupt trigger has occurred since this bit was cleared the last time

Field	Bits	Type	Description
GSCI	9	rh	GSC Interrupt Request Flag This bit is set if the GSC error bit is set and bit is INTDIS.GSCI = 0. 0 _B No GSC interrupt trigger has occurred since this bit was cleared the last time 1 _B A GSC interrupt trigger has occurred since this bit was cleared the last time
STM0I	10	rh	STM Interrupt 0 Request Flag This bit is set if the STM interrupt trigger 0 is set and bit is INTDIS.STM0I = 0. 0 _B No STM0 interrupt trigger has occurred since this bit was cleared the last time 1 _B A STM0 interrupt trigger has occurred since this bit was cleared the last time
STM1I	11	rh	STM Interrupt 1 Request Flag This bit is set if the STM interrupt trigger 1 is set and bit is INTDIS.STM1I = 0. 0 _B No STM1 interrupt trigger has occurred since this bit was cleared the last time 1 _B A STM1 interrupt trigger has occurred since this bit was cleared the last time
MCHKI	12	rh	MCHK Interrupt Request Flag This bit is set if the MCHK interrupt trigger is set and bit is INTDIS.MCHKI = 0. 0 _B No MCHK interrupt trigger has occurred since this bit was cleared the last time 1 _B A MCHK interrupt trigger has occurred since this bit was cleared the last time
PFI	13	rh	Program Flash Interrupt Request Flag This bit is set if the Program Flash interrupt trigger is set and bit is INTDIS.PFI = 0. 0 _B No PF interrupt trigger has occurred since this bit was cleared the last time 1 _B A PF interrupt trigger has occurred since this bit was cleared the last time
0	[15:14]	rh	Reserved Read as 0; should be written with 0.

9.10.3.2 Register INTCLR

This register contains the software clear option for all status flags of all interrupt request trigger sources of the SCU.

INTCLR

Interrupt Clear Register

SFR (FE82_H/41_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	PF I	M CHK I	STM 1 I	STM 0 I	GSC I	WDT I	WU I	WUT I	PVC 1 I2	PVC 1 I1	PVC M I2	PVC M I1	SWD I2	SWD I1	
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Field	Bits	Type	Description
SWDI1	0	w	Clear SWD Interrupt Request Flag 1 0 _B No action 1 _B Bit INTSTAT.SWDI1 is cleared
SWDI2	1	w	Clear SWD Interrupt Request Flag 2 0 _B No action 1 _B Bit INTSTAT.SWDI2 is cleared
PVCM11	2	w	Clear PVC_M Interrupt Request Flag 1 0 _B No action 1 _B Bit INTSTAT.PVCM11 is cleared
PVCM12	3	w	Clear PVC_M Interrupt Request Flag 2 0 _B No action 1 _B Bit INTSTAT.PVCM12 is cleared
PVC111	4	w	Clear PVC_1 Interrupt Request Flag 1 0 _B No action 1 _B Bit INTSTAT.PVC111 is cleared
PVC112	5	w	Clear PVC_1 Interrupt Request Flag 2 0 _B No action 1 _B Bit INTSTAT.PVC112 is cleared
WUTI	6	w	Clear Wake-up Timer Trim Interrupt Request Flag 0 _B No action 1 _B Bit INTSTAT.WUTI is cleared
WUI	7	w	Clear Wake-up Timer Interrupt Request Flag 0 _B No action 1 _B Bit INTSTAT.WUI is cleared

System Control Unit (SCU)

Field	Bits	Type	Description
WDTI	8	w	Clear Watchdog Timer Interrupt Request Flag 0 _B No action 1 _B Bit INTSTAT.WDTI is cleared
GSCI	9	w	Clear GSC Interrupt Request Flag 0 _B No action 1 _B Bit INTSTAT.GSCI is cleared
STM0I	10	w	Clear STM0 Interrupt Request Flag 0 _B No action 1 _B Bit INTSTAT.STM0I is cleared
STM1I	11	w	Clear STM1 Interrupt Request Flag 0 _B No action 1 _B Bit INTSTAT.STM1I is cleared
MCHKI	12	w	Clear MCHK Interrupt Request Flag 0 _B No action 1 _B Bit INTSTAT.MCHKI is cleared
PFI	13	w	Clear Program Flash Interrupt Request Flag 0 _B No action 1 _B Bit INTSTAT.PFI is cleared
0	[15:14]	w	Reserved Must be written with 0.

Note: These bits are always read as 0.

9.10.3.3 Register INTSET

This register contains the software set option for all status flags of all interrupt request trigger sources of the SCU.

INTSET

Interrupt Set Register

SFR (FE80_H/40_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	PF I	M CHK I	STM 1 I	STM 0 I	GSC I	WDT I	WU I	WUT I	PVC 1 I2	PVC 1 I1	PVC M I2	PVC M I1	SWD I2	SWD I1	
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Field	Bits	Type	Description
SWDI1	0	w	Set SWD Interrupt Request Flag 1 0 _B No action 1 _B Bit INTSTAT.SWDI1 is set
SWDI2	1	w	Set SWD Interrupt Request Flag 2 0 _B No action 1 _B Bit INTSTAT.SWDI2 is set
PVCM11	2	w	Set PVC_M Interrupt Request Flag 1 0 _B No action 1 _B Bit INTSTAT.PVCM11 is set
PVCM12	3	w	Set PVC_M Interrupt Request Flag 2 0 _B No action 1 _B Bit INTSTAT.PVCM12 is set
PVC111	4	w	Set PVC_1 Interrupt Request Flag 1 0 _B No action 1 _B Bit INTSTAT.PVC111 is set
PVC112	5	w	Set PVC_1 Interrupt Request Flag 2 0 _B No action 1 _B Bit INTSTAT.PVC112 is set
WUTI	6	w	Set Wake-up Timer Trim Interrupt Request Flag 0 _B No action 1 _B Bit INTSTAT.WUTI is set
WUI	7	w	Set Wake-up Timer Interrupt Request Flag 0 _B No action 1 _B Bit INTSTAT.WUI is set

System Control Unit (SCU)

Field	Bits	Type	Description
WDTI	8	w	Set Watchdog Timer Interrupt Request Flag 0 _B No action 1 _B Bit INTSTAT.WDTI is set
GSCI	9	w	Set GSC Interrupt Request Flag 0 _B No action 1 _B Bit INTSTAT.GSCI is set
STM0I	10	w	Set STM0 Interrupt Request Flag 0 _B No action 1 _B Bit INTSTAT.STM0I is set
STM1I	11	w	Set STM1 Interrupt Request Flag 0 _B No action 1 _B Bit INTSTAT.STM1I is set
MCHKI	12	w	Set MCHK Interrupt Request Flag 0 _B No action 1 _B Bit INTSTAT.MCHKI is set
PFI	13	w	Set Program Flash Interrupt Request Flag 0 _B No action 1 _B Bit INTSTAT.PFI is set
0	[15:14]	w	Reserved Must be written with 0.

Note: These bits are always read as 0.

9.10.3.4 Register INTDIS

This register contains the software disable control for all interrupt request trigger sources of the SCU.

INTDIS

Interrupt Disable Register

SFR (FE84_H/42_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	PF I	M CHK I	STM 1 I	STM 0 I	GSC I	WDT I	WU I	WUT I	PVC 1 I2	PVC 1 I1	PVC M I2	PVC M I1	SWD I2	SWD I1	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
SWDI1	0	rw	Disable SWD Interrupt Request 1 0 _B SWDI1 interrupt request enabled 1 _B SWDI1 interrupt request disabled
SWDI2	1	rw	Disable SWD Interrupt Request 2 0 _B SWDI2 interrupt request enabled 1 _B SWDI2 interrupt request disabled
PVCM11	2	rw	Disable PVC_M Interrupt Request 1 0 _B PVCM11 interrupt request enabled 1 _B PVCM11 interrupt request disabled
PVCM12	3	rw	Disable PVC_M Interrupt Request 2 0 _B PVCM12 interrupt request enabled 1 _B PVCM12 interrupt request disabled
PVC111	4	rw	Disable PVC_1 Interrupt Request 1 0 _B PVC111 interrupt request enabled 1 _B PVC111 interrupt request disabled
PVC112	5	rw	Disable PVC_1 Interrupt Request 2 0 _B PVC112 interrupt request enabled 1 _B PVC112 interrupt request disabled
WUTI	6	rw	Disable Wake-up Timer Trim Interrupt Request 0 _B WUT interrupt request enabled 1 _B WUT interrupt request disabled
WUI	7	rw	Disable Wake-up Timer Interrupt Request 0 _B WU interrupt request enabled 1 _B WU interrupt request disabled

System Control Unit (SCU)

Field	Bits	Type	Description
WDTI	8	rw	Disable Watchdog Timer Interrupt Request 0 _B WDT interrupt request enabled 1 _B WDT interrupt request disabled
GSCI	9	rw	Disable GSC Interrupt Request 0 _B GSC interrupt request enabled 1 _B GSC interrupt request disabled
STM0I	10	rw	Disable STM0 Interrupt Request 0 _B STM0 interrupt request enabled 1 _B STM0 interrupt request disabled
STM1I	11	rw	Disable STM1 Interrupt Request 0 _B STM1 interrupt request enabled 1 _B STM1 interrupt request disabled
MCHKI	12	rw	Disable MCHK Interrupt Request 0 _B MCHK interrupt request enabled 1 _B MCHK interrupt request disabled
PFI	13	rw	Disable Program Flash Interrupt Request 0 _B PF interrupt request enabled 1 _B PF interrupt request disabled
0	[15:14]	rw	Reserved Should be written with 0.

9.10.3.5 Registers INTNP0 and INPNP1

These registers contain the control for the interrupt node pointers of all interrupt request trigger sources of the SCU.

INTNP0

Interrupt Node Pointer 0 Register

SFR (FE86_H/43_H)

Reset Value: 4444_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WU		WUT		PVC12		PVC11		PVCM2		PVCM1		SWD2		SWD1	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
SWD1	[1:0]	rw	Interrupt Node Pointer for SWD 1 Interrupts This bit field defines the interrupt node, which is requested due to the set condition for bit INTSTAT.SWDI1 (if enabled by bit INTDIS.SWDI1). 00 _B Interrupt node 6C _H is selected 01 _B Interrupt node 6B _H is selected 10 _B Interrupt node 1E _H is selected if enabled by bit ISSR.ISS14 (bit is set) 11 _B Interrupt node 1F _H is selected if enabled by bit ISSR.ISS15 (bit is set)
SWD2	[3:2]	rw	Interrupt Node Pointer for SWD 2 Interrupts This bit field defines the interrupt node, which is requested due to the set condition for bit INTSTAT.SWDI2 (if enabled by bit INTDIS.SWDI2). 00 _B Interrupt node 6C _H is selected 01 _B Interrupt node 6B _H is selected 10 _B Interrupt node 1E _H is selected if enabled by bit ISSR.ISS14 (bit is set) 11 _B Interrupt node 1F _H is selected if enabled by bit ISSR.ISS15 (bit is set)

Field	Bits	Type	Description
PVCM1	[5:4]	rw	Interrupt Node Pointer for PVC_M 1 Interrupts This bit field defines the interrupt node, which is requested due to the set condition for bit INTSTAT.PCVMI1 (if enabled by bit INTDIS.PVCMI1). 00 _B Interrupt node 6C _H is selected 01 _B Interrupt node 6B _H is selected 10 _B Interrupt node 1E _H is selected if enabled by bit ISSR.ISS14 (bit is set) 11 _B Interrupt node 1F _H is selected if enabled by bit ISSR.ISS15 (bit is set)
PVCM2	[7:6]	rw	Interrupt Node Pointer for PVC_M 2 Interrupts This bit field defines the interrupt node, which is requested due to the set condition for bit INTSTAT.PCVMI2 (if enabled by bit INTDIS.PVCMI2). 00 _B Interrupt node 6C _H is selected 01 _B Interrupt node 6B _H is selected 10 _B Interrupt node 1E _H is selected if enabled by bit ISSR.ISS14 (bit is set) 11 _B Interrupt node 1F _H is selected if enabled by bit ISSR.ISS15 (bit is set)
PVC11	[9:8]	rw	Interrupt Node Pointer for PVC_1 1 Interrupts This bit field defines the interrupt node, which is requested due to the set condition for bit INTSTAT.PCV1I1 (if enabled by bit INTDIS.PVC1I1). 00 _B Interrupt node 6C _H is selected 01 _B Interrupt node 6B _H is selected 10 _B Interrupt node 1E _H is selected if enabled by bit ISSR.ISS14 (bit is set) 11 _B Interrupt node 1F _H is selected if enabled by bit ISSR.ISS15 (bit is set)
PVC12	[11:10]	rw	Interrupt Node Pointer for PVC_1 2 Interrupts This bit field defines the interrupt node, which is requested due to the set condition for bit INTSTAT.PCV1I2 (if enabled by bit INTDIS.PVC1I2). 00 _B Interrupt node 6C _H is selected 01 _B Interrupt node 6B _H is selected 10 _B Interrupt node 1E _H is selected if enabled by bit ISSR.ISS14 (bit is set) 11 _B Interrupt node 1F _H is selected if enabled by bit ISSR.ISS15 (bit is set)

Field	Bits	Type	Description
WUT	[13:12]	rw	Interrupt Node Pointer for Wake-up Timer Trim Interrupts This bit field defines the interrupt node, which is requested due to the set condition for bit INTSTAT.WUTI (if enabled by bit INTDIS.WUTI). 00 _B Interrupt node 6C _H is selected 01 _B Interrupt node 6B _H is selected 10 _B Interrupt node 1E _H is selected if enabled by bit ISSR.ISS14 (bit is set) 11 _B Interrupt node 1F _H is selected if enabled by bit ISSR.ISS15 (bit is set)
WU	[15:14]	rw	Interrupt Node Pointer for Wake-up Timer Interrupts This bit field defines the interrupt node, which is requested due to the set condition for bit INTSTAT.WUI (if enabled by bit INTDIS.WUI). 00 _B Interrupt node 6C _H is selected 01 _B Interrupt node 6B _H is selected 10 _B Interrupt node 1E _H is selected if enabled by bit ISSR.ISS14 (bit is set) 11 _B Interrupt node 1F _H is selected if enabled by bit ISSR.ISS15 (bit is set)

INTNP1

Interrupt Node Pointer 1 Register

SFR (FE88_H/44_H)

Reset Value: 1111_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-				PF		MCHK		STM1		STM0		GSC		WDT	
-				rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
WDT	[1:0]	rw	Interrupt Node Pointer for WDT Interrupts This bit field defines the interrupt node, which is requested due to the set condition for bit INTSTAT.WDTI (if enabled by bit INTDIS.WDTI). 00 _B Interrupt node 6C _H is selected 01 _B Interrupt node 6B _H is selected 10 _B Interrupt node 1E _H is selected if enabled by bit ISSR.ISS14 (bit is set) 11 _B Interrupt node 1F _H is selected if enabled by bit ISSR.ISS15 (bit is set)
GSC	[3:2]	rw	Interrupt Node Pointer for GSC Interrupts This bit field defines the interrupt node, which is requested due to the set condition for bit INTSTAT.GSCI (if enabled by bit INTDIS.GSCI). 00 _B Interrupt node 6C _H is selected 01 _B Interrupt node 6B _H is selected 10 _B Interrupt node 1E _H is selected if enabled by bit ISSR.ISS14 (bit is set) 11 _B Interrupt node 1F _H is selected if enabled by bit ISSR.ISS15 (bit is set)
STM0	[5:4]	rw	Interrupt Node Pointer for STM0 Interrupts This bit field defines the interrupt node, which is requested due to the set condition for bit INTSTAT.STM0I (if enabled by bit INTDIS.STM0I). 00 _B Interrupt node 6C _H is selected 01 _B Interrupt node 6B _H is selected 10 _B Interrupt node 1E _H is selected if enabled by bit ISSR.ISS14 (bit is set) 11 _B Interrupt node 1F _H is selected if enabled by bit ISSR.ISS15 (bit is set)

Field	Bits	Type	Description
STM1	[7:6]	rw	Interrupt Node Pointer for STM1 Interrupts This bit field defines the interrupt node, which is requested due to the set condition for bit INTSTAT.STM1I (if enabled by bit INTDIS.STM1I). 00 _B Interrupt node 6C _H is selected 01 _B Interrupt node 6B _H is selected 10 _B Interrupt node 1E _H is selected if enabled by bit ISSR.ISS14 (bit is set) 11 _B Interrupt node 1F _H is selected if enabled by bit ISSR.ISS15 (bit is set)
MCHK	[9:8]	rw	Interrupt Node Pointer for MCHK Interrupts This bit field defines the interrupt node, which is requested due to the set condition for bit INTSTAT.MCHKI (if enabled by bit INTDIS.MCHKI). 00 _B Interrupt node 6C _H is selected 01 _B Interrupt node 6B _H is selected 10 _B Interrupt node 1E _H is selected if enabled by bit ISSR.ISS14 (bit is set) 11 _B Interrupt node 1F _H is selected if enabled by bit ISSR.ISS15 (bit is set)
PF	[11:10]	rw	Interrupt Node Pointer for Program Flash Interrupts This bit field defines the interrupt node, which is requested due to the set condition for bit INTSTAT.PFI (if enabled by bit INTDIS.PFI). 00 _B Interrupt node 6C _H is selected 01 _B Interrupt node 6B _H is selected 10 _B Interrupt node 1E _H is selected if enabled by bit ISSR.ISS14 (bit is set) 11 _B Interrupt node 1F _H is selected if enabled by bit ISSR.ISS15 (bit is set)

9.10.3.6 Register DMPMIT

This register contains additional sticky interrupt and trap flags within the DMP_M power domain.

DMPMIT

DMP_M Interrupt and Trap Trigger Register

SFR (FE96_H/4B_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RA T	0	ESR 2 T	ESR 1 T	ESR 0 T	STM 1	STM 0	GSC	WU I	WUT I	PVC 1 I2	PVC 1 I1	PVC M I2	PVC M I1	SWD I2	SWD I1
rh	r	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
SWDI1	0	rh	SWD Interrupt Request Flag 1 This bit is set if bit SWDCON0.L1OK matches the action level defined by SWDCON0.L1ALEV and SWDCON0.L1INTEN = 1 _B . 0 _B No SWDI1 interrupt was requested since this bit was cleared the last time 1 _B A SWDI1 interrupt was requested since this bit was cleared the last time
SWDI2	1	rh	SWD Interrupt Request Flag 2 This bit is set if bit SWDCON0.L2OK matches the action level defined by SWDCON0.L2ALEV and SWDCON0.L2INTEN = 1 _B . 0 _B No SWDI2 interrupt was requested since this bit was cleared the last time 1 _B A SWDI2 interrupt was requested since this bit was cleared the last time
PVCM I1	2	rh	PVC_M Interrupt Request Flag 1 This bit is set if bit PVCMCON0.LEV1OK is cleared and PVCMCON0.L1INTEN = 1 _B . 0 _B No PVCM I1 interrupt was requested since this bit was cleared the last time 1 _B A PVCM I1 interrupt was requested since this bit was cleared the last time

Field	Bits	Type	Description
PVCM12	3	rh	PVC_M Interrupt Request Flag 2 This bit is set if bit PVCMCON0.LEV2OK is cleared and PVCMCON0.L2INTEN = 1 _B . 0 _B No PVCM12 interrupt was requested since this bit was cleared the last time 1 _B A PVCM12 interrupt was requested since this bit was cleared the last time
PVC111	4	rh	PVC_1 Interrupt Request Flag 1 This bit is set if bit PVC1CON0.LEV1OK is cleared and PVC1CON0.L1INTEN = 1 _B . 0 _B No PVC111 interrupt was requested since this bit was cleared the last time 1 _B A PVC111 interrupt was requested since this bit was cleared the last time
PVC112	5	rh	PVC_1 Interrupt Request Flag 2 This bit is set if bit PVC1CON0.LEV2OK is cleared and PVC1CON0.L2INTEN = 1 _B . 0 _B No PVC112 interrupt was requested since this bit was cleared the last time 1 _B A PVC112 interrupt was requested since this bit was cleared the last time
WUTI	6	rh	Wake-up Timer Trim Interrupt Request Flag This bit is set if a wake-up timer trim trigger occurs. 0 _B No WUT interrupt was requested since this bit was cleared the last time 1 _B A WUT interrupt was requested since this bit was cleared the last time
WUI	7	rh	Wake-up Timer Interrupt Request Flag This bit is set if a wake-up timer trigger occurs. 0 _B No WU interrupt was requested since this bit was cleared the last time 1 _B A WU interrupt was requested since this bit was cleared the last time
GSC	8	rh	GSC Interrupt Request Flag This bit is set if a GSC trigger occurs. 0 _B No GSC interrupt was requested since this bit was cleared the last time 1 _B A GSC interrupt was requested since this bit was cleared the last time

Field	Bits	Type	Description
STM0	9	rh	STM0 Interrupt Request Flag This bit is set if a STM0 trigger occurs. 0 _B No STM0 interrupt was requested since this bit was cleared the last time 1 _B A STM0 interrupt was requested since this bit was cleared the last time
STM1	10	rh	STM1 Interrupt Request Flag This bit is set if a STM1 trigger occurs. 0 _B No STM1 interrupt was requested since this bit was cleared the last time 1 _B A STM1 interrupt was requested since this bit was cleared the last time
ESR0T	11	rh	ESR0 Trap Request Flag This bit is set if pin ESR0 is asserted. 0 _B No ESR0 trap was requested since this bit was cleared the last time 1 _B An ESR0 trap was requested since this bit was cleared the last time
ESR1T	12	rh	ESR1 Trap Request Flag This bit is set if pin ESR1 is asserted. 0 _B No ESR1 trap was requested since this bit was cleared the last time 1 _B An ESR1 trap was requested since this bit was cleared the last time
ESR2T	13	rh	ESR2 Trap Request Flag This bit is set if pin ESR2 is asserted. 0 _B No ESR2 trap was requested since this bit was cleared the last time 1 _B An ESR2 trap was requested since this bit was cleared the last time
RAT	15	rh	Register Access Trap Request Flag This bit is set a protected register is written by an non-authorized access. 0 _B No RA trap was requested since this bit was cleared the last time 1 _B A RA trap was requested since this bit was cleared the last time
0	14	r	Reserved Read as 0; should be written with 0.

9.10.3.7 Register DMPMITCLR

This register contains the software clear option for all sticky status flags of all interrupt and trap request trigger sources of the DMP_M power domain.

DMPMITCLR

DMP_M Interrupt and Trap Clear Register

SFR (FE98_H/4C_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RA T	0	ESR 2 T	ESR 1 T	ESR 0 T	STM 1	STM 0	GSC	W UI	WUT I	PVC 1 I2	PVC 1 I1	PVC M I2	PVC M I1	SWD I2	SWD I1
W	r	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Field	Bits	Type	Description
SWDI1	0	w	Clear SWD1 Interrupt Request Flag 1 0 _B No action 1 _B Bit DMPMIT.SWDI1 is cleared
SWDI2	1	w	Clear SWD Interrupt Request Flag 2 0 _B No action 1 _B Bit DMPMIT.SWDI2 is cleared
PVCMI1	2	w	Clear PVC_M Interrupt Request Flag 1 0 _B No action 1 _B Bit DMPMIT.PVCMI1 is cleared
PVCMI2	3	w	Clear PVC_M Interrupt Request Flag 2 0 _B No action 1 _B Bit DMPMIT.PVCMI2 is cleared
PVC1I1	4	w	Clear PVC_1 Interrupt Request Flag 1 0 _B No action 1 _B Bit DMPMIT.PVC1I1 is cleared
PVC1I2	5	w	Clear PVC_1 Interrupt Request Flag 2 0 _B No action 1 _B Bit DMPMIT.PVC1I2 is cleared
WUTI	6	w	Clear Wake-up Trim Interrupt Request Flag 0 _B No action 1 _B Bit DMPMIT.WUTI is cleared
WUI	7	w	Clear Wake-up Interrupt Request Flag 0 _B No action 1 _B Bit DMPMIT.WUI is cleared

System Control Unit (SCU)

Field	Bits	Type	Description
GSC	8	w	Clear GSC Interrupt Request Flag 0 _B No action 1 _B Bit DMPMIT.GSCI is cleared
STM0	9	w	Clear STM0 Interrupt Request Flag 0 _B No action 1 _B Bit DMPMIT.STM0I is cleared
STM1	10	w	Clear STM1 Interrupt Request Flag 0 _B No action 1 _B Bit DMPMIT.STM1I is cleared
ESR0T	11	w	Clear ESR0 Trap Request Flag 0 _B No action 1 _B Bit DMPMIT.ESR0T is cleared
ESR1T	12	w	Clear ESR1 Trap Request Flag 0 _B No action 1 _B Bit DMPMIT.ESR1T is cleared
ESR2T	13	w	Clear ESR2 Trap Request Flag 0 _B No action 1 _B Bit DMPMIT.ESR2T is cleared
RAT	15	w	Clear Register Access Trap Request Flag 0 _B No action 1 _B Bit DMPMIT.RAT is cleared
0	14	r	Reserved Read as 0; should be written with 0.

Note: The bits of type w are always read as 0.

9.11 Temperature Compensation Unit

The temperature compensation for the port drivers provides driver output characteristics which are stable (within a certain band of parameter variation) over the specified temperature range.

The temperature compensation oscillator (sensor) provides a reference clock from a free-running temperature-dependent oscillator. An enable trigger is used to define counting cycles where the reference clock pulses are accumulated to build the sensor value TCLR.THCOUNT. The enable trigger is derived from the system clock by a prescaler and a programmable divider (see [Figure 9-30](#)). The value for the programmable divider must be written by the user according to the selected system frequency.

After the count cycle, the resulting count value, i.e. the number of reference clock cycles, is copied to bit field TCLR.THCOUNT. Thus, TCLR.THCOUNT is updated after every count cycle while the temperature compensation is enabled.

Software can compare the temperature-related count value (TCLR.THCOUNT) to several thresholds (temperature levels) in order to determine the control values TCCR.TCC.

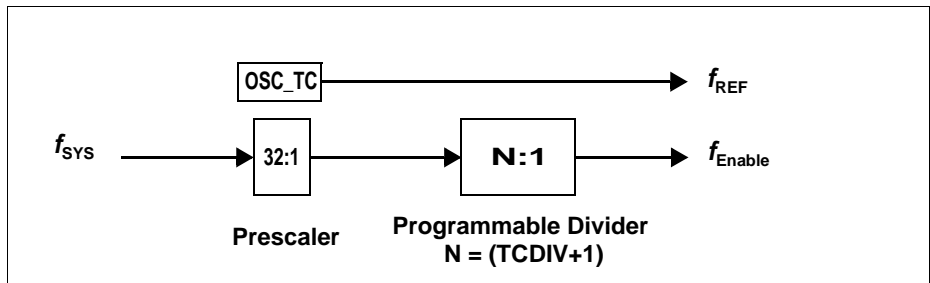


Figure 9-30 Temperature Compensation Clock Generation

The clock divider is programmed via bit field TCCR.TCDIV. The value that should be used for bit field TCCR.TCDIV can be calculated using the following formula:

$$\text{TCDIV} = \text{Integer} ((f_{\text{SYS}} \times 0.3125) - 1) \quad [f_{\text{SYS}} \text{ in MHz}]$$

Example for $f_{\text{SYS}} = 33 \text{ MHz}$:

$$\text{TCDIV} = \text{Integer} ((33 \times 0.3125) - 1) = \text{Integer} (10.3125 - 1) = 9.$$

Generally, temperature compensation is a user-controlled feature. The Temperature Compensation Control Register TCCR provides access to the actual compensation value (generated by the sensor) and allows software control of the pads. During operation the device (i.e. the pads) can be controlled by the value of the on-chip sensor, or by externally provided compensation values. Register TCCR also provides the programmable divider value.

System Control Unit (SCU)

Note: The relation between the counter value and the temperature can differ between two devices and need to be evaluated for each device individually.

Note: The temperature compensation circuit does not generate temperature compensation values continuously. The idea is, that the SW frequently updates the pad control with the value currently found in the tempcomp register (e.g. by an interrupt generated by a timer). Since temperature is a continuous function it is not relevant, whether the temperature value read is new or the value of a previous measurement.

9.11.1 Temperature Compensation Registers

9.11.1.1 TCCR

This register contains the control options.

TCCR

Temperature Compensation Control Register

ESFR (F1AC_H/D6_H)

Reset Value: 0003_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								TCE	TCDIV				TCC		
r								rw	rw				rw		

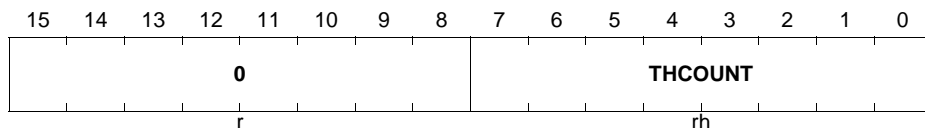
Field	Bits	Type	Description
TCC	[1:0]	rw	Temperature Compensation Control The value which controls the temperature compensation inputs of the pads. 00 _B Maximum reduction = min. driver strength, i.e. very low temperature 11 _B No reduction = max. driver strength, i.e. very high temperature
TCDIV	[6:2]	rw	Temperature Compensation Clock Divider This value adjusts the temperature compensation logic to the selected operating frequency.
TCE	7	rw	Temperature Compensation Enable 0 _B No action 1 _B Enable counting to generate new temperature values. Clearing this bit also stops the temperature compensation oscillator.
0	[15:8]	r	Reserved Read as 0; should be written with 0.

TCLR

Temperature Comp. Level Register

ESFR (F0AC_H/56_H)

Reset Value: 0000_H



Field	Bits	Type	Description
THCOUNT	[7:0]	rh	Threshold Counter Returns the result of the most recent count cycle of the temperature sensor, to be compared with the thresholds.
0	[15:8]	r	Reserved Read as 0; should be written with 0.

Note: The threshold counter will not overflow but rather stop at count 255.

9.12 Watchdog Timer (WDT)

The following part describes the Watchdog Timer (WDT) and its functionality.

9.12.1 Introduction

The Watchdog Timer (WDT) is a secure mechanism to overcome life- and dead-locks. An enabled WDT generates a reset for the system if not serviced in a configured time frame.

Features

The following list is a summary of the WDT functions:

- 16-bit Watchdog Timer
- Selectable operating frequency: $f_{IN} / 256$ or $f_{IN} / 16384$
- Timer overflow error detection
- Individual disable for timer functionality
- Double Reset Detection

Figure 9-31 provides an overview on the registers of the Watchdog Timer.

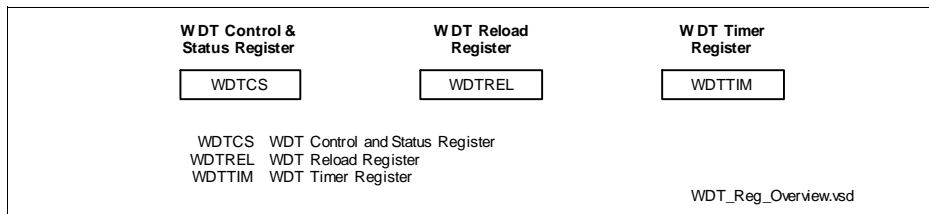


Figure 9-31 Watchdog Timer Register Overview

9.12.2 Overview

The Watchdog Timer (WDT) provides a highly reliable and secure way to detect and recover from software or hardware failure. The WDT helps to abort an accidental malfunction of the XC27x8X in a user-specified time period. When enabled, the WDT will cause the XC27x8X system to be reset if the WDT is not serviced within a user-programmable time period. The CPU must service the WDT within this time interval to prevent the WDT from causing a WDT reset request trigger. Hence, regular service of the WDT confirms that the system is functioning properly.

A further feature of the Watchdog Timer is its reset prewarning operation. Instead of immediately resetting the device on the detection of an error, a prewarning output is given to the system via an interrupt request. This makes it possible to bring the system into a defined and predictable status, before the reset is finally issued.

9.12.3 Functional Description

The following part describes all functions of the WDT.

9.12.3.1 Timer Operation

The timer is enabled when instruction ENWDT (Enable Watchdog Timer) is executed correctly.

The WDT uses the input clock f_{IN} which is equal to the system clock f_{sys} . A clock divider in front of the WDT timer provides two output frequencies, $f_{IN} / 256$ and $f_{IN} / 16384$. The selection of the counting rate is done via bit **WDTCS.IR**.

WDT Periods

The general formula to calculate a Watchdog period is:

$$\text{period} = \frac{(2^{16} - \text{startvalue}) \cdot 256 \cdot 2^{(1 - \text{IR}) \cdot 6}}{f_{IN}} \quad (9.4)$$

The parameter <startvalue> represents either the user-programmable reload value WDTREL.RELV (default value FFFF_{H}) for the calculation of the period in Normal Mode or the fixed value FFFF_{H} for the calculation of the period in Prewarning Mode.

WDT Timer Reload

The counter is reloaded and the prescaler is cleared when one of the following conditions occurs:

- A successful access to register **WDTREL**
- The WDT is serviced via instruction SRWDT
- A WDT overflow condition (Prewarning Mode is entered).
The different reload value for the counter in Prewarning Mode is FFFF_{H} .
- The Disable Mode is entered (when instruction DISWDT is executed)
- Upon any reset

9.12.3.2 Timer Modes

The Watchdog Timer provides following modes:

- Normal Mode
- Disable Mode
- Prewarning Mode

Figure 9-32 provides a state diagram of the different Timer Modes and the transition possibilities. Please refer to the description of the conditions for changing from one mode to the other.

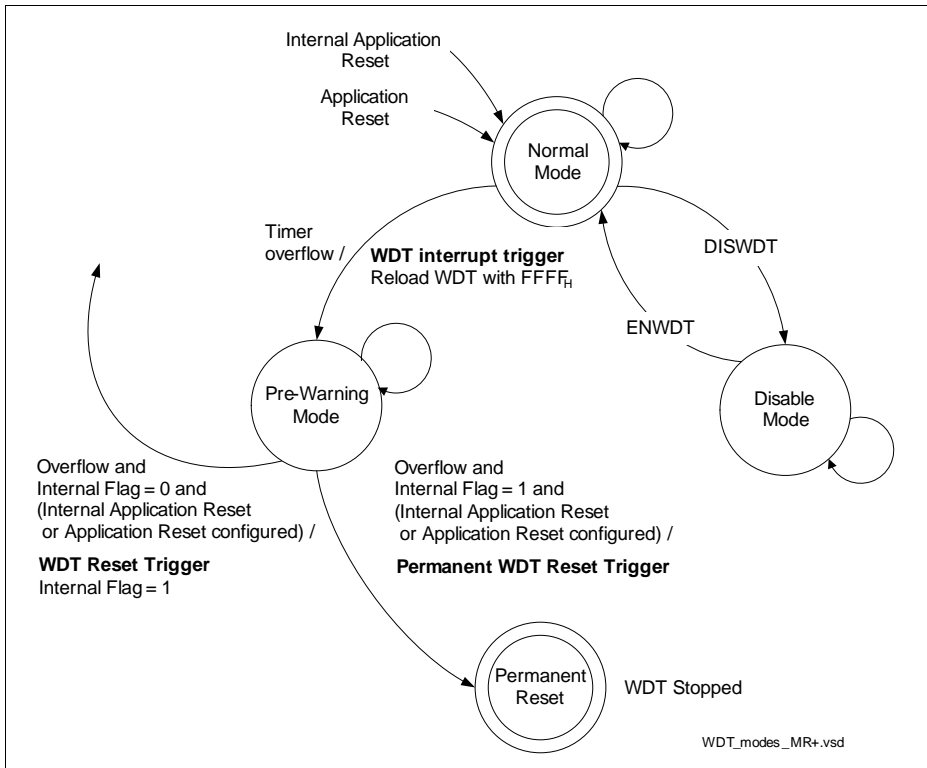


Figure 9-32 State Diagram of the Timer Modes

Normal Mode

Normal Mode is the default mode after an Application Reset or an Internal Application Reset. Normal Mode can be entered from Disable Mode only when instruction ENWDT is executed.

The timer is loaded with RELV when the Normal Mode is entered, and it starts counting upwards. After reset the timer is loaded with $FFFF_{\text{H}}$ (default value of RELV).

It has to be serviced before the counter overflows. Servicing is performed by the CPU via instructions SRVWDT and/or ENWDT.

If the WDT is not serviced before the timer overflows, a system malfunction is assumed, and following operations are done:

- An WDT interrupt trigger request is issued
- Prewarning Mode is entered

- Timer is reloaded with $FFFF_H$

Disable Mode

Disable Mode is provided for applications that do not require the Watchdog Timer function. Disable Mode is entered when instruction DISWDT is executed, either before End-of-Init, if CPUCON1.WDTCTL = 0, or at any time, if CPUCON1.WDTCTL = 1.

The timer is reloaded with the value of WDTREL.RELV when Disable Mode is entered.

A transition from Disable Mode to Normal Mode is performed when instruction ENWDT is executed while CPUCON1.WDTCTL = 1.

Prewarning Mode

Prewarning Mode is entered always when a Watchdog error is detected. This is an overflow in Normal Mode. Instead of immediately requesting a reset of the device, the WDT enables the system to enter a secure state by issuing the prewarning output before the reset occurs. Receiving the prewarning, the CPU and the system are requested to finish all pending transaction requests and to not generate new ones. The prewarning is signalled via an interrupt. The CPU can recognize the WDT prewarning interrupt via register **INTSTAT**. After finishing all pending transactions, the CPU should execute the IDLE instruction to stop all further processing before the coming reset.

In Prewarning Mode, the WDT starts counting from $FFFF_H$ upwards, and then requests a WDT reset on the overflow of the WDT from $FFFF_H$ to 0000_H . A reset request of the type as configured in **RSTCON1**.WDT can not be avoided. No reset will be requested if RSTCON1.WDT is cleared. The WDT does not react anymore to accesses to its registers and to the ENWDT or DISWDT instruction, nor will it change its state until it is reset.

A further feature of the WDT detects double errors and sets the whole system into a permanent WDT reset. This feature prevents the XC27x8X from executing random wrong code for longer than the occurrence of the overflow, and prevents the XC27x8X from being repeatedly reset by the WDT.

*Note: The WDT interrupt is enabled by default upon a reset (register INTDIS = 0000_H). It may lead to interrupt requests being triggered at an inappropriate time as described in **Chapter 9.10**. Hence, it is advised to disable interrupt source that will not be used via the INTDIS register. In addition, pending request flag (SCU_xIC.IR) need to be cleared before enabling interrupts in interrupt controller.*

Double WDT Reset

If the Watchdog induced reset (Application or Internal Application Reset) occurs twice, a severe system malfunction is assumed and the XC27x8X is held in a reset of the type as configured in **RSTCON1**.WDT (or just not) until a Power-on Reset occurs. This prevents

System Control Unit (SCU)

the device from being periodically reset if, for instance, connection to the external memory has been lost such that even system initialization could not be performed.

Note: Triggering a PORST upon a WDT reset will never result in a double WDT overflow.

If the WDT is configured by RSTCON1.WDT to request an Application Reset or an Internal Application Reset the second reset request will be permanently asserted resulting (without any change in the reset configuration) in a permanent reset of the type configured by RSTCON1.WDT.

The information about the first WDT reset request is stored in an internal flag. The internal flag is set when a WDT overflow has occurred in Prewarning Mode and the reset request is generated. If the internal flag is already set then a double WDT reset event has occurred and a permanent reset request is generated.

This internal flag is cleared by any Power-on Reset or when bit **WDTCS.CLRIRF** is set. A correct service of the WDT does not clear this internal flag nor do any access to the WDT related registers or commands. Therefore, if correct WDT-servicing has been done after the first WDT reset and a next WDT reset must not immediately lead to a double error state, application software has to clear the internal flag.

Note: Regarding the handling of the internal flag It does not matter whether a reset was generated on a WDT reset request or if the reset configuration was changed between the two reset requests.

Note: After the double WDT reset request trigger is generated the counter is stopped after the overflow.

Port Configuration during WDT Reset

The behavior of the ESRx ports can be defined with respect to the reset type by bit field ESRCFGx.PC. For the coding of PC see [Table 9-9](#). This allows to signal the occurrence of a reset.

The configuration of the GPIOs ports depends on the reset type. The port behavior is described in section "Reset Behavior" in chapter "Parallel Ports".

9.12.3.3 Suspend Mode Support

In an enabled and active debug session, the Watchdog functionality can lead to unintended resets. Therefore, to avoid these resets, the OCDS can control whether the WDT is enabled or disabled (default after reset). This is done via bit CBS_IOSR.DB.

Table 9-17 OCDS Behavior of WDT

WDTCS.DS	CBS_DBGSR.DBGEN	CBS_IOSR.DB	WDT Action
1	X	X	Stopped
0	0	X	Running

Table 9-17 OCDS Behavior of WDT

WDTCS.DS	CBS_DBGSR.DBGEN	CBS_IOSR.DB	WDT Action
0	1	0	Stopped
0	1	1	Running

9.12.4 WDT Kernel Registers

9.12.4.1 WDT Reload Register

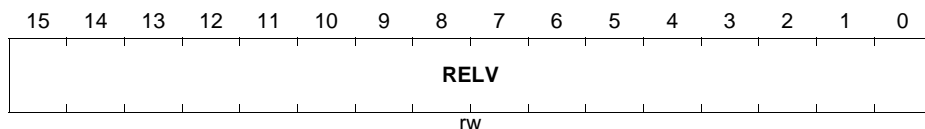
This register defines the WDT reload value.

WDTREL

WDT Reload Register

ESFR (F0C8_H/64_H)

Reset Value: FFFC_H



Field	Bits	Type	Description
RELV	[15:0]	rw	Reload Value for the Watchdog Timer This bit field defines the reload value for the WDT.

9.12.4.2 WDT Control and Status Register

The Control and Status Register can only be accessed in Secured Mode.

WDTCS

WDT Control and Status Register

ESFR (F0C6_H/63_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							IR	0				CLR IRF	PR	DS	OE
r							rw	r				w	rh	rh	rh

Field	Bits	Type	Description
OE	0	rh	Overflow Error Status Flag 0 _B No WDT overflow error 1 _B A WDT overflow error has occurred. This bit is set by hardware when the Watchdog Timer overflows in Prewarning Mode from FFFF _H to 0000 _H . This bit is only cleared through: <ul style="list-style-type: none"> any Power-on Reset an executed SRVWDT or ENWDT instruction <i>Note: The WDT is always enabled by ENWDT in the startup procedure (see section "Watchdog Timer handling"). Therefore, the bit is cleared in case of an Application Reset or an Internal Application Reset.</i> <i>Note: It is not possible to clear this bit in Prewarning Mode with the SRVWDT or ENWDT instruction.</i>
DS	1	rh	Timer Enable/Disable Status Flag 0 _B Timer is enabled (default after reset) 1 _B Timer is disabled This bit is cleared when instruction ENWDT was executed and CPUCON1.WDTCTL = 1. This bit is set when instruction DISWDT was executed before EINIT or CPUCON1.WDTCTL = 1. <i>Note: ENWDT and DISWDT instruction will be reflected in this bit but in Prewarning Mode the WDT mode is not changed.</i>

System Control Unit (SCU)

Field	Bits	Type	Description
PR	2	rh	Prewarning Mode Flag 0_B Normal Mode (default after reset) 1_B Prewarning Mode
CLRIRF	3	w	Clear Internal Reset Flag This bit is used to request a clear of the internal flag storing the information about the first WDT reset request. 0_B No action 1_B Request to clear the internal flag <i>Note: The bit is always read as 0.</i>
IR	8	rw	Input Frequency Request Bit 0_B Request to set input frequency to $f_{IN} / 16384$ 1_B Request to set input frequency to $f_{IN} / 256$ An update of this bit is taken into account after the next successful execution of instruction SRVWDT or ENWDT, on a write to register WDTREL, and always when the WDT is in Disable Mode.
0	[7:4], [15:9]	r	Reserved Read as 0; should be written with 0.

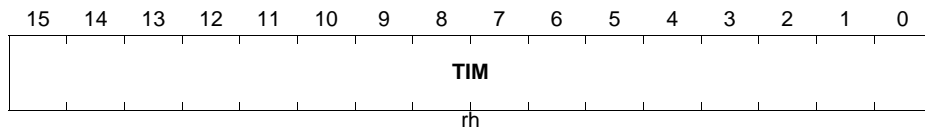
9.12.4.3 WDT Timer Register

WDTTIM

WDT Timer Register

ESFR (F0CA_H/65_H)

Reset Value: FFFC_H



Field	Bits	Type	Description
TIM	[15:0]	rh	Timer Value Reflects the current contents of the Watchdog Timer.

9.13 SCU Trap Generation

The basic trap structure of the SCU is shown in **Figure 9-33**.

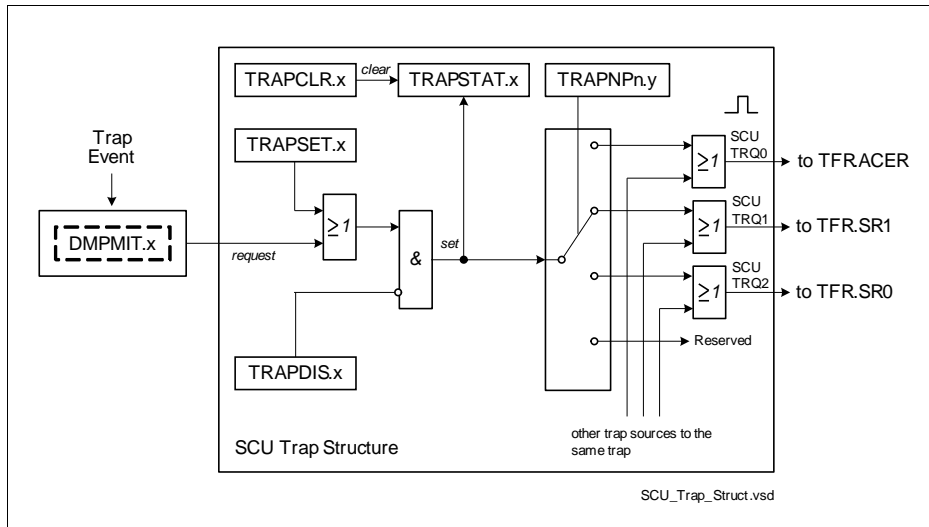


Figure 9-33 SCU Trap Structure

If enabled by the corresponding bit in register **TRAPDIS**, a trap is triggered either by a pulse on the incoming trap line, or by a software set of the respective bit in register **TRAPSET**. The trigger sets the respective flag in register **TRAPSTAT** and is gated to one of the trap nodes, selected by the node pointer registers **TRAPNP** and **TRAPNP1**.

The trap flag in register **TRAPSTAT** can be cleared by software by writing to the corresponding bit in register **TRAPCLR**.

If more than one trap source is connected to the same trap (via registers **TRAPNP** and **TRAPNP1**), the requests are combined to one common line.

Trap Node Assignment

The trap sources of the system can be mapped to three trap nodes by programming the trap node pointer registers **TRAPNP** and **TRAPNP1**. The default assignment of the trap sources to the nodes and their corresponding control register is listed in **Table 9-18**.

9.13.1 Trap Support

Some of the trap requests are first fed through a sticky flag register in the **DMP_M** domain. These flags are set with a trigger and if set trigger the trap generation in the **DMP_1**.

System Control Unit (SCU)

Which of the trap requests have a sticky flag in register DMPMIT is listed in [Table 9-18](#).

Note: When servicing an SCU trap request, make sure that all related request flags are cleared after the identified request has been handled. To clear a trap request that is stored in register DMPMIT, first clear the request source of the source, clear the request within DMP_M via DMPMITCLR, and then clear the request within DMP_1 via TRAPCLR.

9.13.2 SCU Trap Sources

The SCU receives the trap lines listed in [Table 9-18](#).

Table 9-18 SCU Trap Request Overview

Source of Trap	Short Name	Sticky Flag in DMPMIT	Default Trap Flag Assignment in Register TFR
Flash Access Trap	FAT	---	TFR.ACER (SCU_TRQ0)
ESR0 Trap	ESR0T	yes	TFR.SR1 (SCU_TRQ1)
ESR1 Trap	ESR1T	yes	TFR.SR1 (SCU_TRQ1)
ESR2 Trap	ESR2T	yes	TFR.SR1 (SCU_TRQ1)
PLL Trap	OSCWDTT	---	TFR.SR0 (SCU_TRQ2)
Register Access Trap	RAT	yes	TFR.ACER (SCU_TRQ0)
Parity Error Trap	PET	---	TFR.ACER (SCU_TRQ0)
VCO Lock Trap	VCOLCKT	---	TFR.SR0 (SCU_TRQ2)
ECC Error Trap	ECCT	---	TFR.ACER (SCU_TRQ0)

9.13.3 SCU Trap Control Registers

9.13.3.1 Register TRAPSTAT

This register contains the status flags for all trap request trigger sources of the SCU.
 For setting and clearing of these status bits by software see registers TRAPSET and TRAPCLR, respectively.

TRAPSTAT

Trap Status Register

SFR (FF02_H/81_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0						FR VCO LCK T	ECC T	VCO LCK T	PE T	RA T	OSC WDT T	ESR 2 T	ESR 1 T	ESR 0 T	FA T
r						rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
FAT	0	rh	Flash Access Trap Request Flag TRAPSTAT.FAT is set when a flash access violation occurs and TRAPDIS.FAT = 0. 0 _B No FA trap trigger has occurred since this bit was cleared the last time 1 _B A FA trap trigger has occurred since this bit was cleared the last time
ESR0T	1	rh	ESR0 Trap Request Flag TRAPSTAT.ESR0T is set when bit DMPMIT.ESR0T is set and TRAPDIS.ESR0T = 0. 0 _B No ESR0 trap trigger has occurred since this bit was cleared the last time 1 _B An ESR0 trap trigger has occurred since this bit was cleared the last time
ESR1T	2	rh	ESR1 Trap Request Flag TRAPSTAT.ESR1T is set when bit DMPMIT.ESR1T is set and TRAPDIS.ESR1T = 0. 0 _B No ESR1 trap trigger has occurred since this bit was cleared the last time 1 _B An ESR1 trap trigger has occurred since this bit was cleared the last time

Field	Bits	Type	Description
ESR2T	3	rh	ESR2 Trap Request Flag TRAPSTAT.ESR2T is set when bit DMPMIT.ESR0T is set and TRAPDIS.ESR2T = 0. 0 _B No ESR2 trap trigger has occurred since this bit was cleared the last time 1 _B An ESR2 trap trigger has occurred since this bit was cleared the last time
OSCWDTT	4	rh	OSCWDT Trap Request Flag TRAPSTAT.OSCWDTT is set when an OSCWDT emergency event occurs and TRAPDIS.OSCWDTT = 0. 0 _B No OSCWDT trap trigger has occurred since this bit was cleared the last time 1 _B An OSCWDT trap trigger has occurred since this bit was cleared the last time
RAT	5	rh	Register Access Trap Request Flag TRAPSTAT.RAT is set when bit DMPMIT.RAT is set and TRAPDIS.RAT = 0. 0 _B No RA trap trigger has occurred since this bit was cleared the last time 1 _B A RA trap trigger has occurred since this bit was cleared the last time
PET	6	rh	Parity Error Trap Request Flag TRAPSTAT.PET is set when a memory parity error occurs and TRAPDIS.PET = 0. 0 _B No PE trap trigger has occurred since this bit was cleared the last time 1 _B A PE trap trigger has occurred since this bit was cleared the last time
VCOLCKT	7	rh	VCOLCK Trap Request Flag TRAPSTAT.VCOLCKT is set when a VCOLCK emergency event occurs and TRAPDIS.VCOLCKT = 0. 0 _B No VCOLCK trap trigger has occurred since this bit was cleared the last time 1 _B A VCOLCK trap trigger has occurred since this bit was cleared the last time

System Control Unit (SCU)

Field	Bits	Type	Description
ECCT	8	rh	ECC Error Trap Request Flag TRAPSTAT.ECCT is set when a memory ECC error occurs and TRAPDIS.ECCT = 0. 0 _B No ECC trap trigger has occurred since this bit was cleared the last time 1 _B An ECC trap trigger has occurred since this bit was cleared the last time
FRVCOLCKT	9	rh	Reserved Should be written with 0.
0	[15:10]	r	Reserved Read as 0; should be written with 0.

9.13.3.2 Register TRAPCLR

This register contains the software clear control for the trap status flags in register TRAPSTAT. Clearing a bit in this register has no effect, reading a bit always returns zero.

TRAPCLR

Trap Clear Register

SFR (FE8E_H/47_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						FR VCO LCK T	ECC T	VCO LCK T	PE T	RA T	OSC WDT T	ESR 2 T	ESR 1 T	ESR 0 T	FA T
			0												
			r			w	w	w	w	w	w	w	w	w	w

Field	Bits	Type	Description
FAT	0	w	Clear Flash Access Trap Request Flag 0 _B No action 1 _B Flag TRAPSTAT.FAT is cleared
ESR0T	1	w	Clear ESR0 Trap Request Flag 0 _B No action 1 _B Flag TRAPSTAT.ESR0T is cleared
ESR1T	2	w	Clear ESR1 Trap Request Flag 0 _B No action 1 _B Flag TRAPSTAT.ESR1T is cleared
ESR2T	3	w	Clear ESR2 Trap Request Flag 0 _B No action 1 _B Flag TRAPSTAT.ESR2T is cleared
OSCWDTT	4	w	Clear OSCWDT Trap Request Flag 0 _B No action 1 _B Flag TRAPSTAT.OSCWDTT is cleared
RAT	5	w	Clear Register Access Trap Request Flag 0 _B No action 1 _B Flag TRAPSTAT.RAT is cleared
PET	6	w	Clear Parity Error Access Trap Request Flag 0 _B No action 1 _B Flag TRAPSTAT.PET is cleared
VCOLCKT	7	w	Clear VCOLCK Trap Request Flag 0 _B No action 1 _B Flag TRAPSTAT.VCOLCKT is cleared

System Control Unit (SCU)

Field	Bits	Type	Description
ECCT	8	w	Clear ECC Error Trap Request Flag 0 _B No action 1 _B Flag TRAPSTAT.ECCT is cleared
FRVCOLCKT	9	w	Reserved Should be written with 0
0	[15:10]	r	Reserved Read as 0; should be written with 0

Note: These bits are always read as 0.

System Control Unit (SCU)

Field	Bits	Type	Description
ECCT	8	w	Set ECC Error Trap Request Flag 0 _B No action 1 _B Flag TRAPSTAT.ECCT is set
FRVCOLCKT	9	w	Reserved Should be written with 0
0	[15:10]	r	Reserved Read as 0; should be written with 0.

Note: These bits are always read as 0.

System Control Unit (SCU)

Field	Bits	Type	Description
VCOLCKT	7	rw	Disable VCOLCK Trap Request 0 _B VCOLCK trap request enabled 1 _B VCOLCK trap request disabled
ECCT	8	rw	Disable ECC Error Trap Request 0 _B ECC trap request enabled 1 _B ECC trap request disabled
FRVCOLCKT	9	rw	Reserved Should be written with 0
0	[15:10]	r	Reserved Read as 0; should be written with 0.

9.13.3.5 Register TRAPNP and TRAPNP1

These register contain the control for the trap node pointers of all SCU trap request trigger sources.

TRAPNP

Trap Node Pointer Register

SFR (FE92_H/49_H)

Reset Value: 8254_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VCOLCK		PE		RA		OSCWDT		ESR2		ESR1		ESR0		FA	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
FA	[1:0]	rw	Trap Node Pointer for Flash Access Traps TRAPNP.FA selects the trap request output for an enabled FAT trap request. 00 _B Select request output SCU_TRQ0 (TFR.ACER) 01 _B Select request output SCU_TRQ1 (TFR.SR1) 10 _B Select request output SCU_TRQ2 (TFR.SR0) 11 _B Reserved, do not use this combination
ESR0	[3:2]	rw	Trap Node Pointer for ESR0 Traps TRAPNP.ESR0 selects the trap request output for an enabled ESR0 trap request. 00 _B Select request output SCU_TRQ0 (TFR.ACER) 01 _B Select request output SCU_TRQ1 (TFR.SR1) 10 _B Select request output SCU_TRQ2 (TFR.SR0) 11 _B Reserved, do not use this combination
ESR1	[5:4]	rw	Trap Node Pointer for ESR1 Traps TRAPNP.ESR1 selects the trap request output for an enabled ESR1 trap request. 00 _B Select request output SCU_TRQ0 (TFR.ACER) 01 _B Select request output SCU_TRQ1 (TFR.SR1) 10 _B Select request output SCU_TRQ2 (TFR.SR0) 11 _B Reserved, do not use this combination

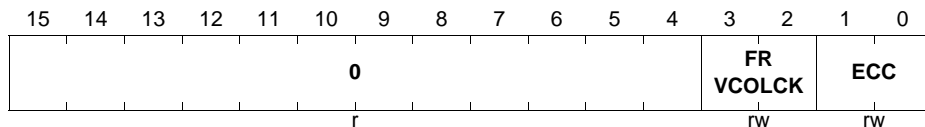
Field	Bits	Type	Description
ESR2	[7:6]	rw	Trap Node Pointer for ESR2 Traps TRAPNP.ESR2 selects the trap request output for an enabled ESR2 trap request. 00 _B Select request output SCU_TRQ0 (TFR.ACER) 01 _B Select request output SCU_TRQ1 (TFR.SR1) 10 _B Select request output SCU_TRQ2 (TFR.SR0) 11 _B Reserved, do not use this combination
OSCWDT	[9:8]	rw	Trap Node Pointer for OSCWDT Traps TRAPNP.OSCWDT selects the trap request output for an enabled OSCWDT trap request. 00 _B Select request output SCU_TRQ0 (TFR.ACER) 01 _B Select request output SCU_TRQ1 (TFR.SR1) 10 _B Select request output SCU_TRQ2 (TFR.SR0) 11 _B Reserved, do not use this combination
RA	[11:10]	rw	Trap Node Pointer for Register Access Traps TRAPNP.RA selects the trap request output for an enabled RAT trap request. 00 _B Select request output SCU_TRQ0 (TFR.ACER) 01 _B Select request output SCU_TRQ1 (TFR.SR1) 10 _B Select request output SCU_TRQ2 (TFR.SR0) 11 _B Reserved, do not use this combination
PE	[13:12]	rw	Trap Node Pointer for Parity Error Traps TRAPNP.PE selects the trap request output for an enabled PET trap request. 00 _B Select request output SCU_TRQ0 (TFR.ACER) 01 _B Select request output SCU_TRQ1 (TFR.SR1) 10 _B Select request output SCU_TRQ2 (TFR.SR0) 11 _B Reserved, do not use this combination
VCOLCK	[15:14]	rw	Trap Node Pointer for VCOLCK Traps TRAPNP.VCOLCK selects the trap request output for an enabled VCOLCK trap request. 00 _B Select request output SCU_TRQ0 (TFR.ACER) 01 _B Select request output SCU_TRQ1 (TFR.SR1) 10 _B Select request output SCU_TRQ2 (TFR.SR0) 11 _B Reserved, do not use this combination

TRAPNP1

Trap Node Pointer 1 Register

SFR (FE94_H/4A_H)

Reset Value:0004_H



Field	Bits	Type	Description
ECC	[1:0]	rw	Trap Node Pointer for ECC Error Traps TRAPNP.ECC selects the trap request output for an enabled ECCT trap request. 00 _B Select request output SCU_TRQ0 (TFR.ACER) 01 _B Select request output SCU_TRQ1 (TFR.SR1) 10 _B Select request output SCU_TRQ2 (TFR.SR0) 11 _B Reserved, do not use this combination
FRVCOLCK	[3:2]	rw	Reserved Should be written with 0
0	[15:4]	r	Reserved Read as 0; should be written with 0.

9.14 Memory Content Protection for RAM Areas

For supervising the content of the on-chip RAM areas (Flash memory is not considered here) two mechanisms are provided:

- Error Correction Control (ECC)
- Parity Checking

For each piece of data written to a RAM area the corresponding protection bits (parity or ECC bits) are generated and stored along with the user data.

The ECC logic supports single error detection (SED) and single error correction (SEC). The FlexRay module also supports double error detection (DED).

For the standard RAM areas, register MCHKCON selects the intended memory protection mode, while RAM areas embedded into peripheral modules provide a fixed protection mode. [Table 9-19](#) summarizes the available modes.

Table 9-19 Available Memory Protection Mechanisms

Memory	Parity	ECC Error Detection	ECC Error Correction	ECC code
Program SRAM (PSRAM)	yes	SED	SEC	4 bits per byte
Data SRAM (DSRAM)	yes	SED	SEC	4 bits per byte
Dual Port SRAM (DPRAM)	yes	SED	SEC	4 bits per byte
Standby RAM (SBRAM)	yes	SED	SEC	4 bits per byte
Instruction Cache (ICACHE)	no	SED/DED	SEC	8 bits per cache set 5 bits for tag
USICx SRAM (UxRAM)	yes	No	No	-
MultiCAN SRAM (MCRAM)	no	SED	SEC	7 bits per 32 bits
FlexRay SRAM (FRRAM)	no	SED/DED (selection inside FR)	SEC	7 bits per 32 bits

Note: Memory Content Protection with Parity or ECC is disabled by default.

The intended protection mode must be selected and enabled before the respective RAM area can be used (see [Section 9.14.1](#)).

The subsequent handling of trap requests is described in section [Chapter 9.13](#).

9.14.1 Protection Mode Selection

After a power-on reset, memory content protection is disabled. The intended protection mode must be selected and enabled before the respective RAM area can be used. Either Parity or ECC protection can be selected for each standard RAM area.

Register **MCHKCON** selects the intended protection mode for the standard RAM areas. By default the ECC protection mode is selected, but not enabled.

ECC Protection Mode

With ECC protection mode selected, the ECC logic generates additional ECC bits which are stored along with each piece of data which is written to the selected RAM area.

Register **ECCCON** enables the checking of previously stored ECC bits.

If enabled, single-bit errors are detected during read operations (SED). These single-bit errors are automatically corrected before sending data to the CPU (SEC). An error is indicated in register **ECCSTAT**.

If disabled, read data are sent to the CPU unchanged and no error flags are set.

Parity Protection Mode

With Parity protection mode selected, the parity logic generates additional parity bits which are stored along with each piece of data which is written to the selected RAM area.

Register **PEEN** enables the checking of previously stored parity bits.

If enabled, parity errors are detected and indicated in register **PECON**. Read data are not modified.

Protection Mode Enabling

To activate RAM content protection, the protection mode must first be selected (register **MCHKCON**).

After a protection mode has been configured for a RAM area, that RAM must be initialized so the correct protection bits are generated and the RAM can be read without error.

CPU memory accesses may produce speculative read operations, in which data is read in advance, in anticipation of its actual use. In some cases, this may result in data accesses outside of the RAM memory regions actually used in the application. For example, the autoincrement mode of the SBRAM interface will access the new location after incrementing the pointer. Therefore, it is strongly recommended to initialize all content protected RAM before use, to avoid unexpected errors.

Note: The sequence to activate one of these mechanisms is described in section "Preparing to activate Memory Content Protection."

MCHKCON

Memory Checking Control Register

ESFR (F0DC_H/6E_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0						M CAN DRA	USIC DRA	0				SEL SB	SEL PS	SEL DS	SEL DP
rw						rw	rw	rw				rw	rw	rw	rw

Field	Bits	Type	Description
SELDP	0	rw	Select Protection Mode for Dual Port Memory 0 _B ECC mode is selected for DPRAM 1 _B Parity mode is selected for DPRAM
SELDS	1	rw	Select Protection Mode for Data SRAM 0 _B ECC mode is selected for DSRAM 1 _B Parity mode is selected for DSRAM
SELPS	2	rw	Select Protection Mode for Program SRAM 0 _B ECC mode is selected for PSRAM 1 _B Parity mode is selected for PSRAM
SELSB	3	rw	Select Protection Mode for Standby Memory 0 _B ECC mode is selected for SBRAM 1 _B Parity mode is selected for SBRAM
USICDRA	8	rw	USIC Direct RAM Access 0 _B Direct RAM access for the USIC is not possible 1 _B Direct RAM access for the USIC is possible
MCANDRA	9	rw	MultiCAN Direct RAM Access 0 _B Direct RAM access for the MultiCAN is not possible 1 _B Direct RAM access for the MultiCAN is possible
0	[7:4], [15:10]	rw	Reserved Should be written with 0.

9.14.2 Parity Error Handling

During write operations parity information is generated and stored along with the data. During read operations this parity information is checked and in case of an error a trap request is generated (register PECON), if enabled. The requests from all RAMs can be combined (register PEEN) and trigger a trap via bit PET in register **TRAPSTAT**.

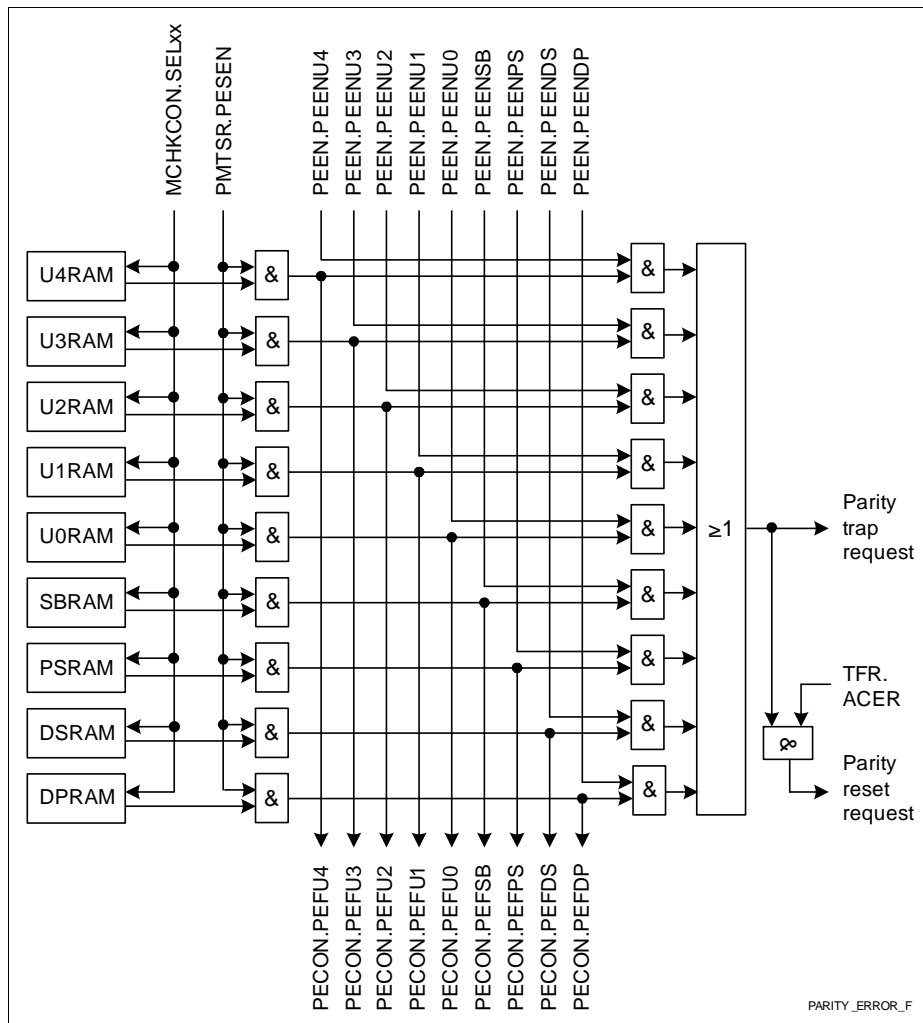


Figure 9-34 Parity Error Control Logic

System Control Unit (SCU)

If a parity error is detected while the trap flag TFR.ACER is set, i.e. during the execution of the associated trap handler routine, a reset request trigger is generated. This is because a second error trap would activate the same handler and, therefore, cannot be handled by the CPU.

Note: The parity trap trigger should activate the Access Error trap (ACER) to support this feature.

9.14.2.1 Parity Software Testing Support

To support testing algorithms for the parity error trap routines a memory parity test logic is implemented for the standard RAM areas (PSRAM, DSRAM, DPRAM, SBRAM).

This logic is controlled by registers PMTPR and PMTSR. If enabled by the respective bit MTEx in register PMTSR, a parity value can be written to any address of the corresponding RAM area through bitfield PWR in register PMTPR. With each read access from that area the parity from the memory parity control is stored in bitfield PRD of register PMTPR.

Table 9-20 lists the valid bits in register PMTPR depending on the memory width.

Table 9-20 Valid Parity Test Bits

Memory	Number of Parity Bits	Valid Bits in PWR/PRD
Dual Port (DP) Memory	2	PWR[1:0]/PRD[9:8]
Data SRAM (DS) Memory	2	PWR[1:0]/PRD[9:8]
Program SRAM (PS) Memory	8	PWR[7:0]/PRD[15:8]
Standby RAM (SB) Memory	2	PWR[1:0]/PRD[9:8]

Test software should be located in external memory and should be written in a way that no pre-fetching is performed.

9.14.2.2 Parity Error Registers

Register PEEN enables the functional parity check mechanism for each RAM area separately.

Note: Bit PESEN in register PMTSR globally enables the parity mechanism.

PEEN

Parity Error Enable Register ESFR (F0C4_H/41_H) Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0						PE EN SB	PE EN U4	PE EN U3	PE EN U2	PE EN U1	PE EN U0	PE EN PS	PE EN DS	PE EN DP	
rw						rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
PEENDP	0	rw	Parity Error Trap Enable for Dual Port Memory 0 _B Disabled 1 _B Trap requested for DPRAM parity errors
PEENDS	1	rw	Parity Error Trap Enable for Data SRAM 0 _B Disabled 1 _B Trap requested for DSRAM parity errors
PEENPS	2	rw	Parity Error Trap Enable for Program SRAM 0 _B Disabled 1 _B Trap requested for PSRAM parity errors
PEENU0	3	rw	Parity Error Trap Enable for USIC0 Memory 0 _B Disabled 1 _B Trap requested for USIC0 memory parity errors
PEENU1	4	rw	Parity Error Trap Enable for USIC1 Memory 0 _B Disabled 1 _B Trap requested for USIC1 memory parity errors
PEENU2	5	rw	Parity Error Trap Enable for USIC2 Memory 0 _B Disabled 1 _B Trap requested for USIC2 memory parity errors

System Control Unit (SCU)

Field	Bits	Type	Description
PEENU3	6	rw	Parity Error Trap Enable for USIC3 Memory 0 _B Disabled 1 _B Trap requested for USIC3 memory parity errors
PEENU4	7	rw	Parity Error Trap Enable for USIC4 Memory 0 _B Disabled 1 _B Trap requested for USIC4 memory parity errors
PEENSB	8	rw	Parity Error Trap Enable for Standby Memory 0 _B Disabled 1 _B Trap requested for SBRAM parity errors
0	[15:9]	rw	Reserved Should be written with 0.

System Control Unit (SCU)

Register PECON controls the functional parity check mechanism.

If enabled the corresponding error flag is set upon the detection of a parity error in the associated RAM area. Otherwise, there is no indication.

Software can clear an error flag by writing 1 to the flag. Writing 0 has no effect.

PECON

Parity Error Control Register ESFR (F0DA_H/6D_H) Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							PEF SB	PEF U4	PEF U3	PEF U2	PEF U1	PEF U0	PEF PS	PEF DS	PEF DP
rwh							rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
PEFDP	0	rwh	Parity Error Flag for Dual Port Memory 0 _B No DPRAM error 1 _B A Parity error is indicated and can trigger a trap request trigger, if enabled for DPRAM
PEFDS	1	rwh	Parity Error Flag for Data SRAM 0 _B No DSRAM error 1 _B A Parity error is indicated and can trigger a trap request trigger, if enabled for DSRAM
PEFPS	2	rwh	Parity Error Flag for Program SRAM 0 _B No PSRAM error 1 _B A Parity error is indicated and can trigger a trap request trigger, if enabled for PSRAM
PEFU0	3	rwh	Parity Error Flag for USIC0 Memory 0 _B No USIC0 memory error 1 _B A Parity error is indicated and can trigger a trap request trigger, if enabled for USIC0 memory
PEFU1	4	rwh	Parity Error Flag for USIC1 Memory 0 _B No USIC1 memory error 1 _B A Parity error is indicated and can trigger a trap request trigger, if enabled for USIC1 memory
PEFU2	5	rwh	Parity Error Flag for USIC2 Memory 0 _B No USIC2 memory error 1 _B A Parity error is indicated and can trigger a trap request trigger, if enabled for USIC2 memory

System Control Unit (SCU)

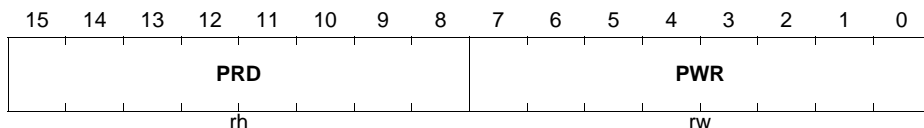
Field	Bits	Type	Description
PEFU3	6	rwh	Parity Error Flag for USIC3 Memory 0_B No USIC3 memory error 1_B A Parity error is indicated and can trigger a trap request trigger, if enabled for USIC3 memory
PEFU4	7	rwh	Parity Error Flag for USIC4 Memory 0_B No USIC4 memory error 1_B A Parity error is indicated and can trigger a trap request trigger, if enabled for USIC4 memory
PEFSB	8	rwh	Parity Error Flag for Standby Memory 0_B No SBRAM error 1_B A Parity error is indicated and can trigger a trap request trigger, if enabled for Standby memory
0	[15:9]	rwh	Reserved Should be written with 0.

PMTPR

Parity Memory Test Pattern Register

ESFR (F0E4_H/72_H)

Reset Value: 0000_H



Field	Bits	Type	Description
PRD	[15:8]	rh	Parity Read Values for Memory Test For each byte of a memory module the parity bits generated during the most recent read access are indicated here.
PWR	[7:0]	rw	Parity Write Values for Memory Test For each byte of a memory module the parity bits corresponding to the next write access are stored here.

PMTSR

Parity Memory Test Select Register

ESFR (F0E6_H/73_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PES EN			0				MT EN SB			0			MT EN PS	MT EN DS	MT EN DP
rw			r				rw			rw			rw	rw	rw

Field	Bits	Type	Description
MTENDP	0	rw	Memory Test Enable Control for Dual Port Memory Controls the test multiplexer for the DPRAM. 0 _B Standard operation 1 _B Test parity bits used (from PMTPR)
MTENDS	1	rw	Memory Test Enable Control for Data SRAM Controls the test multiplexer for the DSRAM. 0 _B Standard operation 1 _B Test parity bits used (from PMTPR)
MTENPS	2	rw	Memory Test Enable Control for Program SRAM Controls the test multiplexer for the PSRAM. 0 _B Standard operation 1 _B Test parity bits used (from PMTPR)
MTENSB	8	rw	Memory Test Enable Control for Standby Memory Controls the test multiplexer for the SBRAM. 0 _B Standard operation 1 _B Test parity bits used (from PMTPR)
PESEN	15	rw	Parity Error Sensitivity Enable 0 _B Parity errors have no effect 1 _B Parity errors are indicated and can trigger a trap, if enabled
0	[7:3]	rw	Reserved Should be written with 0.
0	[14:9]	r	Reserved Read as 0; should be written with 0.

System Control Unit (SCU)

*Note: Only one bit MTENxx should be set at the same time in register PMTSR.
Otherwise the result of the parity software test is not reliable.*

9.14.3 ECC Error Handling

During write operations ECC information is generated and stored along with the data. During read operations this ECC information is checked and in case of an error a trap request is generated (register [ECCSTAT](#)), if enabled. The requests from all RAMs can be combined (register [ECCCON](#)) and trigger a trap via bit ECCT in register [TRAPSTAT](#).

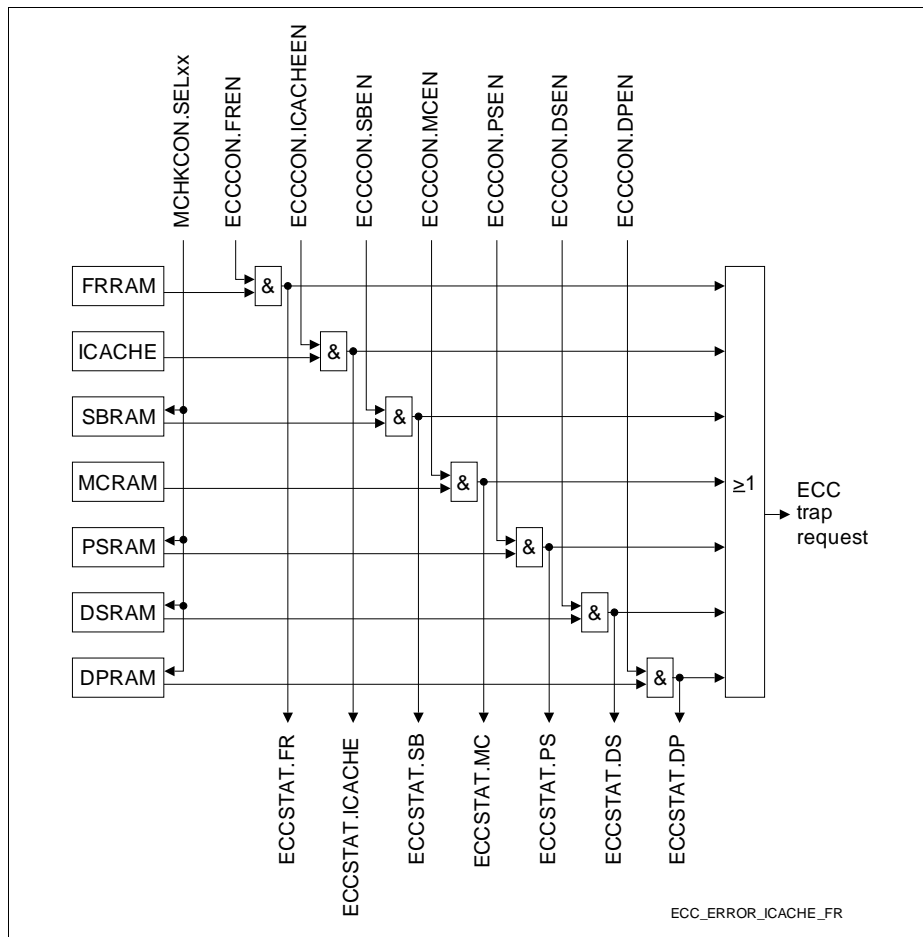


Figure 9-35 ECC Error Control Logic

Note: When using the autoincrement mode to read the SBRAM and having ECC enabled, it is necessary not only to initialize the used addresses but also the one

following the last used address. This problem does not exist if the whole SBRAM is initialized.

Note: After initialization of a RAM (except DPRAM and ICACHE) with enabled ECC read one location from any initialized memory location of the respective RAM to assure correct initial state of the read-control logic.

Note: The ECC error flag of the ECCSTAT register (except DPRAM and ICACHE) can not be cleared, if a memory location with an ECC error is selected and the ECC is enabled. The memory is selected by an active or by the latest read or write access. Therefore, select a memory location without ECC error in the respective memory (e.g. make a read to another address) to assure correct state of the read-control logic and then clear the ECC error flag. Be aware that the new selected address may also have an ECC error.

Note: The handling of Flash ECC errors cannot be done completely in the SCU, but requires actions also in the IMB.

9.14.3.1 ECC Software Testing Support

The ECC error detection can be triggered on purpose to test the detection itself and the associated trap routine. This test option is available for RAMs that can operate with ECC and with parity protection, i.e. the standard RAM areas (DPRAM, DSRAM, PSRAM, SBRAM).

The software based ECC test uses both ECC and parity checking. It can generate a single-bit ECC error by executing the following sequence:

- Select parity mode for the respective RAM (MCHKCON.SELx = 1)
- Read back MCHKCON to allow the parity logic to activate
- Write 2000_H to a location within this RAM (while parity is selected)
- Select ECC mode for the respective RAM (MCHKCON.SELx = 0)
- Read back MCHKCON to allow the ECC logic to activate
- Read from the chosen RAM location (while ECC is selected)

This will generate a single bit ECC error for databit 9:

If ECC operation is enabled (ECCCON.xEN = 1) the corrected data value (2000_H) is read and an ECC error is indicated.

If ECC operation is disabled (ECCCON.xEN = 0) the uncorrected data value (2200_H) is read and no error is indicated.

Note: Due to the structure of the PSRAM this test modifies a complete 8-Byte memory line (...000_B - ...111_B). A non-destructive test, therefore, must save and restore all 4 words of the respective memory line.

9.14.3.2 ECC Registers

ECCCON

ECC Control Register

ESFR (F0A8_H/54_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0									FR EN	SB EN	MC EN	ICAC HE EN	PS EN	DS EN	DP EN
rw									rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
DPEN	0	rw	Enable for Dual Port Memory 0 _B Disabled 1 _B ECC check and error correction for DPRAM enabled
DSEN	1	rw	Enable for Data SRAM 0 _B Disabled 1 _B ECC check and error correction for DSRAM enabled
PSEN	2	rw	Enable for Program SRAM 0 _B Disabled 1 _B ECC check and error correction for PSRAM enabled
ICACHEEN	3	rw	Enable for ICACHE Memory 0 _B Disabled 1 _B ECC check and error correction for ICACHE enabled
MCEN	4	rw	Enable for MultiCAN Memory 0 _B Disabled 1 _B ECC check and error correction for MultiCAN memory enabled
SBEN	5	rw	Enable for Standby Memory 0 _B Disabled 1 _B ECC check and error correction for SBRAM enabled
FREN	6	rw	Enable for FlexRay Memory 0 _B Disabled 1 _B ECC check and error correction for FlexRay memory enabled

System Control Unit (SCU)

Field	Bits	Type	Description
0	[15:7]	rw	Reserved Should be written with 0.

ECCSTAT

ECC Status Register

ESFR (F0AA_H/55_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0									FR	SB	MC	ICACHE	PS	DS	DP
rh									rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
DP	0	rh	Dual Port Memory ECC Error Status 0 _B No DPRAM error 1 _B An ECC error was detected for the DPRAM
DS	1	rh	Data SRAM ECC Error Status 0 _B No DSRAM error 1 _B An ECC error was detected for the DSRAM
PS	2	rh	Program SRAM ECC Error Status 0 _B No PSRAM error 1 _B An ECC error was detected for the PSRAM
ICACHE	3	rh	ICACHE ECC Error Status 0 _B No ICACHE error 1 _B An ECC error was detected for the ICACHE
MC	4	rh	MultiCAN Memory ECC Error Status 0 _B No MultiCAN error 1 _B An ECC error was detected for the MultiCAN memory
SB	5	rh	Standby Memory ECC Error Status 0 _B No SBRAM error 1 _B An ECC error was detected for the SBRAM
FR	6	rh	Flexray Memory ECC Error Status 0 _B No FlexRay error 1 _B An ECC error was detected for the FlexRay memory
0	[15:7]	rh	Reserved Read as 0.

ECCCLRSTAT

ECC Clear Status Register

ESFR (F0DE_H/6F_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0									FR	SB	MC	ICACHE	PS	DS	DP
w									w	w	w	w	w	w	w

Field	Bits	Type	Description
DP	0	w	Clear Dual Port Memory ECC Error Status 0 _B No action 1 _B Setting this bit clears bit ECCSTAT.DP
DS	1	w	Clear Data SRAM ECC Error Status 0 _B No action 1 _B Setting this bit clears bit ECCSTAT.DS
PS	2	w	Clear Program SRAM ECC Error Status 0 _B No action 1 _B Setting this bit clears bit ECCSTAT.PS
ICACHE	3	w	Clear ICACHE ECC Error Status 0 _B No action 1 _B Setting this bit clears bit ECCSTAT.ICACHE
MC	4	w	Clear MultiCAN Memory ECC Error Status 0 _B No action 1 _B Setting this bit clears bit ECCSTAT.MC
SB	5	w	Clear Standby Memory ECC Error Status 0 _B No action 1 _B Setting this bit clears bit ECCSTAT.SB
FR	6	w	Clear Flexray Memory ECC Error Status 0 _B No action 1 _B Setting this bit clears bit ECCSTAT.FR
0	[15:7]	w	Reserved

Note: These bits are always read as 0.

9.15 Register Control

This block handles the register accesses of the SCU and the register access control for all system register that use one of the following protection modes:

- Unprotected Mode
- Write Protection Mode
- Secured Mode

9.15.1 Register Access Control

There are some dedicated registers that control critical system functions and modes. These registers are protected by a special register security mechanism so these vital system functions cannot be changed inadvertently after the executing of the EINIT instruction. However, as these registers control central system behavior they need to be accessed during operation. The system control software gets this access via a special security state machine.

If an access violation is detected a trap trigger request is generated.

This security mechanism controls the following security levels which can be configured via register SLC:

- **Unprotected Mode**
No protection is active. Registers can be written at any time. This mode is entered after the Application Reset.
- **Write Protected Mode**
Protected registers are locked against any write access. Write accesses have no effect on these registers. This mode is entered automatically after the EINIT instruction is executed.
- **Secured Mode**
Protected registers can be written using a special command.
Access in Secured Mode can be achieved by preceding the intended write access with writing "command 4" to register SLC. After writing "command 4" to register SLC the register protection mechanism remains disabled until the next write to a register on the PD+Bus (SFR, ESFR, XSFR area), i.e. accesses to registers (e.g. CSFR) outside this area do not enable the protection again automatically. Therefore, the lock mechanism after writing "command 4" works differently depending on the register address. Normally one single write access to a protected register is enabled. After this write access the protected registers are locked again automatically. Thereafter, "command 4" has to be written again in order to enable the next write to a protected register. The lock mechanism is not enabled again after a write access to a CSFR register or to a LXBus peripheral register (XLOC area, e.g. USIC, CAN, IMB).

Note: In Secured Mode the re-enabling of register protection with respect to the write address after "command 4" can lead to an unexpected, not obvious behaviour of an application:

System Control Unit (SCU)

In case the succeeding write to a protected register is delayed due to an interrupt and the ISR itself uses the “command 4” mechanism. After writing “command 4” inside the ISR the protection is expectedly re-installed instead of released and the following write will lead to an ACER trap within the ISR. An ATOMIC instruction, which couples the unlock with the write to the protected register could be used.

In case the succeeding write is to a register which does not re-enable the protection mechanism again then the write itself will succeed, but in a following “command 4” sequence the write to SLC register re-locks the protection again and the write to a protected register fails.

SCU Registers that are protected by Secured Mode are marked in [Table 9-24](#) as “Sec” protected; protected registers in other modules are summarized in [Table 9-21](#).

Table 9-21 Registers Protected by Secured Mode

Register Name	Module
CPUCON1	CPU
CPUCON2	CPU
MPU_PRD	MPU
MPU_PRA	MPU
MPU_PMr (x = 0 ... 5)	MPU
EBC_EBCMOD0	EBC
EBC_EBCMOD1	EBC
EBC_TCONCSx (x = 0 ... 4)	EBC
EBC_FCONCSx (x = 0 ... 4)	EBC
EBC_ADDRSELx (x = 1 ... 4)	EBC
MCHK_COUNT	MCHK
MCHK_TPRL	MCHK
MCHK_TPRH	MCHK
DBGPRR	OCDS
MEM_KSCCFG	Memory
FL_KSCCFG	Memory
RTC_KSCCFG	RTC
GPT12E_KSCCFG	GPT12
CC2_KSCCFG	CAPCOM2
CAN_KSCCFG	MultiCAN

System Control Unit (SCU)

All registers that are equipped with this protection mechanism have additional to normal access parameters (e.g. read only, bit type r or rh) the access limitations defined by the selected security level. Independently of the security level all protected registers can also be read.

9.15.1.1 Controlling the Security Level

The two registers Security Level Command register (SLC) and Security Level Status register (SLS) control the security level. The SLC register accepts the commands to control the state machine modifying the security level, while the SLS register shows the actual password, the actual security level, and the state of the state machine.

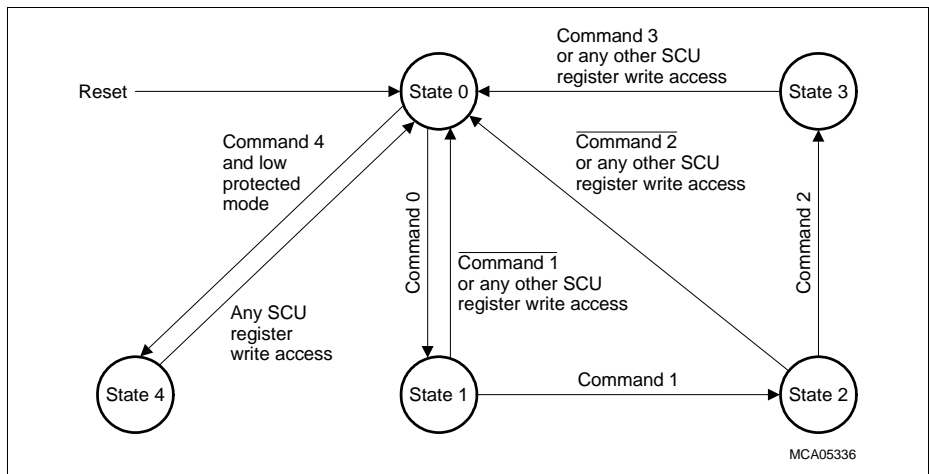


Figure 9-36 State Machine for Security Level Controlling

The following mechanism is used to control the actual security level:

- **Changing the security level**
 can be done by executing the following command sequence:
 “command 0 - command 1 - command 2 - command 3”.
 This sequence establishes a new security level and/or a new password.

Table 9-22 Commands for Security Level Control

Command	Definition	Note
Command 0	AAAA _H	
Command 1	5554 _H	
Command 2	96 _H + ¹⁾ <inverse password>	

Table 9-22 Commands for Security Level Control

Command	Definition	Note
Command 3	000 _B + <new level> + 000 _B + <new password>	
Command 4	8E _H + <inverse password>	Secured Mode only

1) '+' denotes a bit field concatenation

Note: It is recommended to lock all command sequences with an atomic sequence.

9.15.2 Register Protection Registers

Register SLC

This register is the interface for the protection commands.

SLC

Security Level Command RegisterESFR (F0C0_H/60_H)

Reset Value: 0000_H



Field	Bits	Type	Description
COMMAND	[15:0]	rw	Security Level Control Command The commands to control the security level must be written to this register (see table)

Register SLS

This register monitors the status of the register protection.

SLS

Security Level Status Register ESFR (F0C2_H/61_H) **Reset Value: 0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STATE			SL		0			PASSWORD							
rh			rh		r			rh							

Field	Bits	Type	Description
PASSWORD	[7:0]	rh	Current Security Control Password Default after reset = 00 _H
SL	[12:11]	rh	Security Level ¹⁾ 00 _B Unprotected Mode (default) 01 _B Secured Mode 10 _B Reserved, Do not use this combination 11 _B Write Protected Mode
STATE	[15:13]	rh	Current State of Switching State Machine 000 _B Awaiting command 0 or command 4 (default) 001 _B Awaiting command 1 010 _B Awaiting command 2 011 _B Awaiting new security level and password 100 _B Next access granted in Secured Mode 101 _B Reserved, do not use this combination 11X _B Reserved, do not use this combination
0	[10:8]	r	Reserved Read as 0; should be written with 0;

1) While the security level is "unprotected" after reset, it changes to "write protected" after the execution of instruction EINIT.

9.16 Miscellaneous System Registers

This chapter acts as container for various register that are not connected to one specific application topic.

9.16.1 System Registers

9.16.1.1 System Control Register

The following register serve several different system tasks.

SYSCON1

System Control 1 Register

SFR (FF4C_H/A6_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					0						TRC EN	GLC CST	OCD SEN		0
					r						rw	rw	rw		r

Field	Bits	Type	Description
OCDSEN	2	rw	OCDS/Cerberus Enable 0 _B OCDS and Cerberus are still in reset state 1 _B ODSCS and Cerberus are operable
GLCCST	3	rw	Global CAPCOM Start This bit starts all CAPCOM units synchronously if enabled. 0 _B CAPCOM timer start is controlled locally in each unit 1 _B All CAPCOM timers in CC1 and CC2 are started synchronously This bit needs to be cleared via software before setting starts a new CAPCOM start.
TRCEN	4	rw	IP Trace Enable 0 _B IP Trace is disabled 1 _B IP Trace is enabled
0	[1:0], [15:5]	r	Reserved Read as 0; should be written with 0.

9.16.2 Identification Block

For identification of the most important silicon parameters a set of identification registers is defined that provide information on the chip manufacturer, the chip type and its properties.

9.16.2.1 Identification Registers

Register IDMANUF

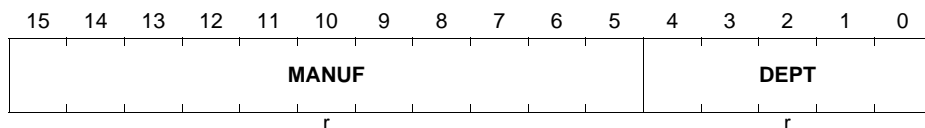
This register contains information about the manufacturer.

IDMANUF

Manufacturer Identification Register

ESFR (F07E_H/3F_H)

Reset Value: 1820_H



Field	Bits	Type	Description
DEPT	[4:0]	r	Department Indicates the department within Infineon. 00 _H AIM MC
MANUF	[15:5]	r	Manufacturer This is the JEDEC normalized manufacturer code. 0C1 _H Infineon Technologies AG

Register IDCHIP

This register contains information about the device.

IDCHIP

Chip Identification Register **ESFR (F07C_H/3E_H)** **Reset Value: XXXX_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHIPID								Revision							
r								r							

Field	Bits	Type	Description
Revision	[7:0]	r	Device Revision Code Identifies the device step. Please refer to the data sheet for the device specific value.
CHIPID	[15:8]	r	Device Identification Identifies the device name. Please refer to the data sheet for the device specific value.

Register IDMEM

This register contains information about the program memory.

IDMEM

Program Memory Identification Register

ESFR (F07A_H/3D_H)

Reset Value: 3XXX_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TYPE				SIZE											
r				rw											

Field	Bits	Type	Description
SIZE	[11:0]	rw	Size of on-chip Program Memory The size of the implemented program memory in terms of 4 K blocks, i.e. memory size = <SIZE>*4 Kbyte. Please refer to the data sheet for the device specific value.
TYPE	[15:12]	r	Type of on-chip Program Memory Identifies the memory type on this silicon. Please refer to the data sheet for the device specific value.

Register IDPROG

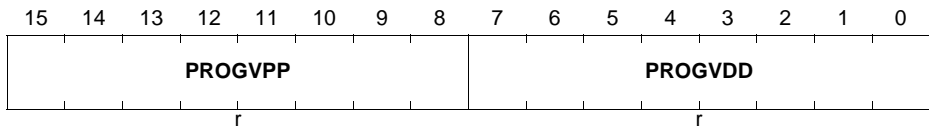
This register is provided for software compatibility reasons only. It contains information about the flash programming voltage. In the XC27x8X devices, the flash programming voltages are generated internally.

IDPROG

Programming Voltage Id. Register

ESFR (F078_H/3C_H)

Reset Value: 1313_H



Field	Bits	Type	Description
PROGVDD	[7:0]	r	Programming VDD Voltage The voltage of the standard power supply required to program or erase (if applicable) the on-chip program memory. Please refer to the data sheet for the device specific value.
PROGVPP	[15:8]	r	Programming VPP Voltage The voltage of the special programming power supply (if existent) required to program or erase (if applicable) the on-chip program memory. Please refer to the data sheet for the device specific value.

Register IDDMPPM

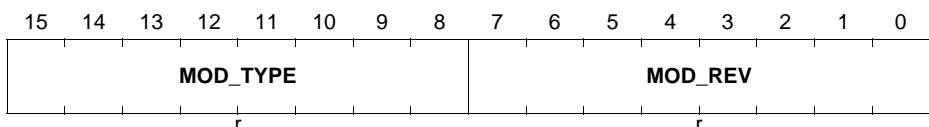
This register contains information about the DMP_M SCU.

IDDMPPM

DMP_M Module Identification Register

SFR (FFE2_H)

Reset Value: 60XX_H



Field	Bits	Type	Description
MOD_REV	[7:0]	r	Module Revision Number Defines the revision number. The value of a module revision starts with 01 _H .
MOD_TYPE	[15:8]	r	Module Identification Number Defines the module identification number (SCU_M = 60 _H)

Register IDDMP1

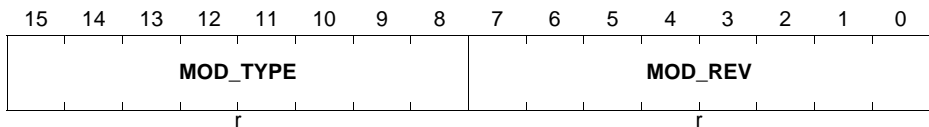
This register contains information about the DMP_1 SCU.

IDDMP1

DMP_1 Module Identification Register

SFR (FFE4_H)

Reset Value: 61XX_H



Field	Bits	Type	Description
MOD_REV	[7:0]	r	Module Revision Number Defines the revision number. The value of a module revision starts with 01 _H .
MOD_TYPE	[15:8]	r	Module Identification Number Defines the module identification number (SCU_1 = 61 _H)

9.16.3 Marker Memory

9.16.3.1 Marker Memory Registers

The marker memory consists of following SFRs located in the DMP_M for free usage of the user software.

MKMEM0

Marker Memory 0 Register SFR (FED0_H/68_H) Reset Value: 0000_H

MKMEM1

Marker Memory 1 Register SFR (FED2_H/69_H) Reset Value: 0000_H



Field	Bits	Type	Description
MARKER	[15:0]	rw	Marker Content

9.17 SCU Register Addresses

The SCU registers are within the (E)SFR space of the XC27x8X. Therefore, their specified addresses equal an offset from zero.

Table 9-23 Registers Address Space

Module	Base Address	End Address	Note
SCU	00 0000 _H	00 FFFE _H	

SCU Register Overview

Table 9-24 Register Overview of SCU

Short Name	Register Long Name	Offset Addr.	Protection ¹⁾	Reset ²⁾
WUOSCCON	Wake-up OSC Control Register	F1AE _H	Sec	Power-on Reset
HPOSCCON	High Precision Oscillator Configuration Register	F1B4 _H	Sec	Power-on Reset
PLLOSCCON	PLL Control Register	F1B6 _H	Sec	Power-on Reset
PLLSTAT	PLL Status Register	F0BC _H	-	Power-on Reset
STATCLR1	PLL Status Clear 1 Register	F0E2 _H	Sec	Power-on Reset
PLLCON0	PLL Configuration 0 Register	F1B8 _H	Sec	Power-on Reset
PLLCON1	PLL Configuration 1 Register	F1BA _H	Sec	Power-on Reset
PLLCON2	PLL Configuration 2 Register	F1BC _H	Sec	Power-on Reset
PLLCON3	PLL Configuration 3 Register	F1BE _H	Sec	Power-on Reset
SYSCON0	System Configuration 0 Register	FF4A _H	Sec	Power-on Reset
STATCLR0	Status Clear 0 Register	F0E0 _H	Sec	Power-on Reset
RTCCLKCON	RTC Clock Control Register	FF4E _H	Sec	Power-on Reset

Table 9-24 Register Overview of SCU

Short Name	Register Long Name	Offset Addr.	Protection¹⁾	Reset ²⁾
EXTCON	External Clock Control Register	FF5E _H	Sec	Power-on Reset
STMREL	STM Reload Register	F1A8 _H	Sec	Power-on Reset
STMCON	STM Control Register	F1AA _H	Sec	Power-on Reset
WUTREL	Wake-up Timer Reload Register	F0B0 _H	Sec	Power-on Reset
WUCR	Wake-up Control Register	F1B0 _H	Sec	Power-on Reset
RSTSTAT0	Reset Status 0 Register	F0B2 _H	-	Power-on Reset
RSTSTAT1	Reset Status 1 Register	F0B4 _H	-	Power-on Reset
RSTSTAT2	Reset Status 2 Register	F0B6 _H	-	Power-on Reset
RSTCON0	Reset Configuration 0 Register	F0B8 _H	Sec	Power-on Reset
RSTCON1	Reset Configuration 1 Register	F0BA _H	Sec	Power-on Reset
RSTCNTCON	Reset Counter Configuration Register	F1B2 _H	Sec	Power-on Reset
SWRSTCON	SW Reset Control Register	F0AE _H	Sec	Power-on Reset
ESREXCON1	ESR 1 External Control Register	FF32 _H	Sec	Power-on Reset
ESREXCON2	ESR 2 External Control Register	FF34 _H	Sec	Power-on Reset
ESREXSTAT1	ESR 1 External Status Register	FF36 _H	-	Power-on Reset
ESREXSTAT2	ESR 2 External Status Register	FF38 _H	-	Power-on Reset
CLRESREXSTAT1	Clear ESR 1 External Status Register	FF3A _H	Sec	Power-on Reset

Table 9-24 Register Overview of SCU

Short Name	Register Long Name	Offset Addr.	Protection ¹⁾	Reset ²⁾
CLRESREXSTAT2	Clear ESR 2 External Status Register	FF3C _H	Sec	Power-on Reset
ESRCFG0	ESR 0 Configuration Register	F100 _H	Sec	Power-on Reset
ESRCFG1	ESR 1 Configuration Register	F102 _H	Sec	Power-on Reset
ESRCFG2	ESR 2 Configuration Register	F104 _H	Sec	Power-on Reset
ESRDAT	ESR Data Register	F106 _H	Sec	Power-on Reset
SWDCON0	SWD Control 0 Register	F080 _H	Sec	Power-on Reset
SWDCON1	SWD Control 1 Register	F082 _H	Sec	Power-on Reset
PVC1CON0	PVC_1 Control for Step 0 Register	F014 _H	Sec	Power-on Reset
PVCMCON0	PVC_M Control for Step 0 Register	F1E4 _H	Sec	Power-on Reset
EVR1CON0	EVR_1 Control 0 Register	F088 _H	Sec	Power-on Reset
EVR1SET15VHP	EVR_1 Setting for 1.5V HP Register	F09E _H	Sec	Power-on Reset
EVRMCON0	EVR_M Control 0 Register	F084 _H	Sec	Power-on Reset
EVRMCON1	EVR_M Control 1 Register	F086 _H	Sec	Power-on Reset
EVRMSET15VHP	EVR_M Setting for 1.5V HP Register	F096 _H	Sec	Power-on Reset
GSCSWREQ	GSC SW Request Register	FF14 _H	Sec	Application Reset
GSCEN	GSC Enable Register	FF16 _H	Sec	Application Reset
GSCSTAT	GSC Status Register	FF18 _H	-	Application Reset

Table 9-24 Register Overview of SCU

Short Name	Register Long Name	Offset Addr.	Protection¹⁾	Reset ²⁾
GSCPERSTATEN	GSC Peripheral Status Enable Register	FF04 _H	Sec	Application Reset
GSCPERSTATEN1	GSC Peripheral Status 1 Enable Register	FF06 _H	Sec	Application Reset
GSCPERSTAT	GSC Peripheral Status Register	FF1A _H	-	Application Reset
GSCPERSTAT1	GSC Peripheral Status 1 Register	FE9A _H	-	Application Reset
STSTAT	Start-up Status Register	F1E0 _H	-	Application Reset
EXISEL	External Interrupt Input Select Register	F1A0 _H	Sec	Application Reset
EXICON0	External Interrupt Input Trigger Control 0 Register	F030 _H	Sec	Application Reset
EXICON1	External Interrupt Input Trigger Control 1 Register	F032 _H	Sec	Application Reset
EXICON2	External Interrupt Input Trigger Control 2 Register	F034 _H	Sec	Application Reset
EXICON3	External Interrupt Input Trigger Control 3 Register	F036 _H	Sec	Application Reset
EXOCON0	External Output Trigger Control 0 Register	FE30 _H	Sec	Application Reset
EXOCON1	External Output Trigger Control 1 Register	FE32 _H	Sec	Application Reset
EXOCON2	External Output Trigger Control 2 Register	FE34 _H	Sec	Application Reset
EXOCON3	External Output Trigger Control 3 Register	FE36 _H	Sec	Application Reset
INTSTAT	Interrupt Status Register	FF00 _H	-	Application Reset
INTCLR	Interrupt Clear Register	FE82 _H	Sec	Application Reset
INTSET	Interrupt Set Register	FE80 _H	Sec	Application Reset

Table 9-24 Register Overview of SCU

Short Name	Register Long Name	Offset Addr.	Protection¹⁾	Reset ²⁾
INTDIS	Interrupt Disable Register	FE84 _H	Sec	Application Reset
INTNP0	Interrupt Node Pointer 0 Register	FE86 _H	Sec	Application Reset
INTNP1	Interrupt Node Pointer 1 Register	FE88 _H	Sec	Application Reset
DMPMIT	DMP_M Interrupt and Trap Trigger Register	FE96 _H	-	Power-on Reset
DMPMITCLR	DMP_M Interrupt and Trap Clear Register	FE98 _H	Sec	Power-on Reset
TCCR	Temperature Compensation Control Register	F1AC _H	Sec	Application Reset
TCLR	Temperature Compensation Level Register	F0AC _H	Sec	Application Reset
WDTREL	WDT Reload Register	F0C8 _H	Sec	Application Reset
WDTCS	WDT Control and Status Register	F0C6 _H	Sec	Application Reset
WDTTIM	WDT Timer Register	F0CA _H	Sec	Application Reset
TRAPSTAT	Trap Status Register	FF02 _H	-	Power-on Reset
TRAPCLR	Trap Clear Register	FE8E _H	Sec	Power-on Reset
TRAPSET	Trap Set Register	FE8C _H	Sec	Application Reset
TRAPDIS	Trap Disable Register	FE90 _H	Sec	Application Reset
TRAPNP	Trap Node Pointer Register	FE92 _H	Sec	Application Reset
TRAPNP1	Trap Node Pointer 1 Register	FE94 _H	Sec	Application Reset

Table 9-24 Register Overview of SCU

Short Name	Register Long Name	Offset Addr.	Protection¹⁾	Reset²⁾
MCHKCON	Memory Checking Control Register	F0DC _H	Sec	Power-on Reset
PEEN	Parity Error Enable Register	F0C4 _H	Sec	Power-on Reset
PECON	Parity Error Control Register	F0DA _H	Sec	Power-on Reset
PMPTR	Parity Memory Test Pattern Register	F0E4 _H	Sec	Application Reset
PMTSR	Parity Memory Test Select Register	F0E6 _H	Sec	Application Reset
ECCCON	ECC Control Register	F0A8 _H	Sec	Application Reset
ECCSTAT	ECC Status Register	F0AA _H	-	Application Reset
ECCCLRSTAT	ECC Clear Status Register	F0DE _H	Sec	Application Reset
SLC	Security Level Command Register	F0C0 _H	-	Application Reset
SLS	Security Level Status Register	F0C2 _H	-	Application Reset
SYSCON1	System Control 1 Register	FF4C _H	Sec	Application Reset
IDMANUF	Manufacturer Identification Register	F07E _H	-	Power-on Reset
IDCHIP	Chip Identification Register	F07C _H	-	Power-on Reset
IDMEM	Program Memory Identification Register	F07A _H	-	Power-on Reset
IDPROG	Programming Voltage Identification Register	F078 _H	-	Power-on Reset
IDDMPM	DMP_M Identification Register	FFE2 _H	-	Power-on Reset
IDDMP1	DMP_1 Identification Register	FFE4 _H	-	Power-on Reset

System Control Unit (SCU)

Table 9-24 Register Overview of SCU

Short Name	Register Long Name	Offset Addr.	Protection ¹⁾	Reset ²⁾
MKMEM0	Marker Memory 0 Register	FED0 _H	Sec	Power-on Reset
MKMEM1	Marker Memory 1 Register	FED2 _H	Sec	Power-on Reset

1) Register write protection mechanism: "Sec" = register security mechanism, "-" = always accessible (no protection), otherwise no access is possible.

2) Reset types are defined in [Chapter 9.4.1.2](#).

10 Parallel Ports

The XC27x8X provides a set of General Purpose Input/Output (GPIO) ports that can be controlled by software and by the on-chip peripheral units:

Table 10-1 Ports of the XC27x8X in PG-LQFP-144

Port	Width	I/O	Connected Modules
P0	8	I/O	EBC (A7...A0), CCU6, USIC, CAN
P1	8	I/O	EBC (A15...A8), CCU6, USIC
P2	14	I/O	EBC (READY, \overline{BHE} , A23...A16, AD15...AD13, D15...D13), CAN, CC2, GPT12E, USIC, DAP/JTAG
P3	8	I/O	CAN, USIC
P4	8	I/O	EBC ($\overline{CS4}$... $\overline{CS0}$), CC2, CAN, GPT12E, USIC
P5	16	I	Analog Inputs, CCU6, DAP/JTAG, GPT12E, CAN
P6	4	I/O	Analog Inputs, ADC, CAN, GPT12E
P7	5	I/O	CAN, GPT12E, SCU, DAP/JTAG, CCU6, ADC, USIC
P8	6	I/O	CCU6, DAP/JTAG, USIC
P9	8	I/O	CCU6, DAP/JTAG, CAN
P10	16	I/O	EBC(ALE, \overline{RD} , \overline{WR} , AD12...AD0, D12...D0), CCU6, USIC, DAP/JTAG, CAN
P11	6	I/O	CCU6, USIC, CAN
P15	8	I	Analog Inputs, GPT12E

*Note: The availability of ports and port pins depends on the selected device type.
This chapter describes the maximum set of ports.*

10.1 General Description

This chapter describes the architecture of the digital control circuit for a single port pin.

10.1.1 Basic Port Operation

There are three types of digital control circuits:

- Digital Input/Output with or without Hardware Override [Figure 10-1](#)
- Digital Input/Output with Analog Input [Figure 10-2](#)
- Digital and Analog Input [Figure 10-3](#)

Port pins marked as Hardware Input (IH) or Hardware Output (OH) in the Pin Definition Table ([Table 10-18](#)) use the hardware override functionality, Port 6 is a Digital I/O and Analog Input port and Ports 5 and 15 are Digital and Analog Inputs. All others port pins are Standard Digital I/Os.

ESRx_INPUTy inputs are directly connected to the ESR output of the pad and not affected by the port input logic. This allows to trigger a wake-up via these pins while the power domain DMP_1 is disabled.

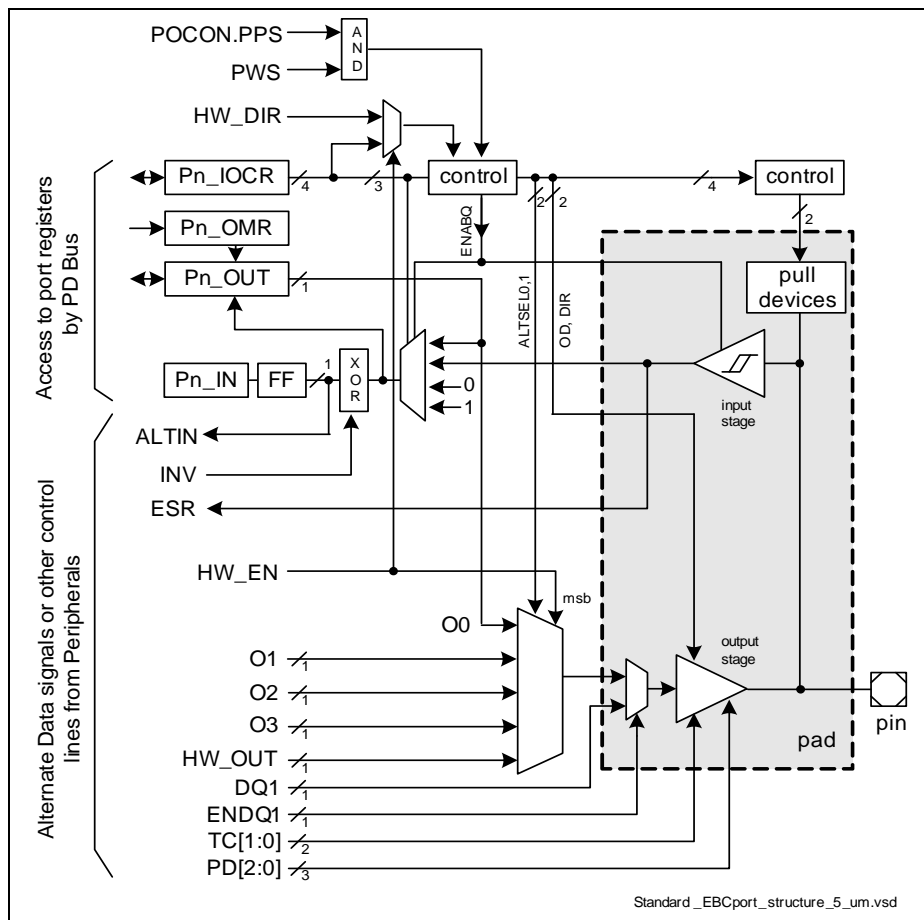
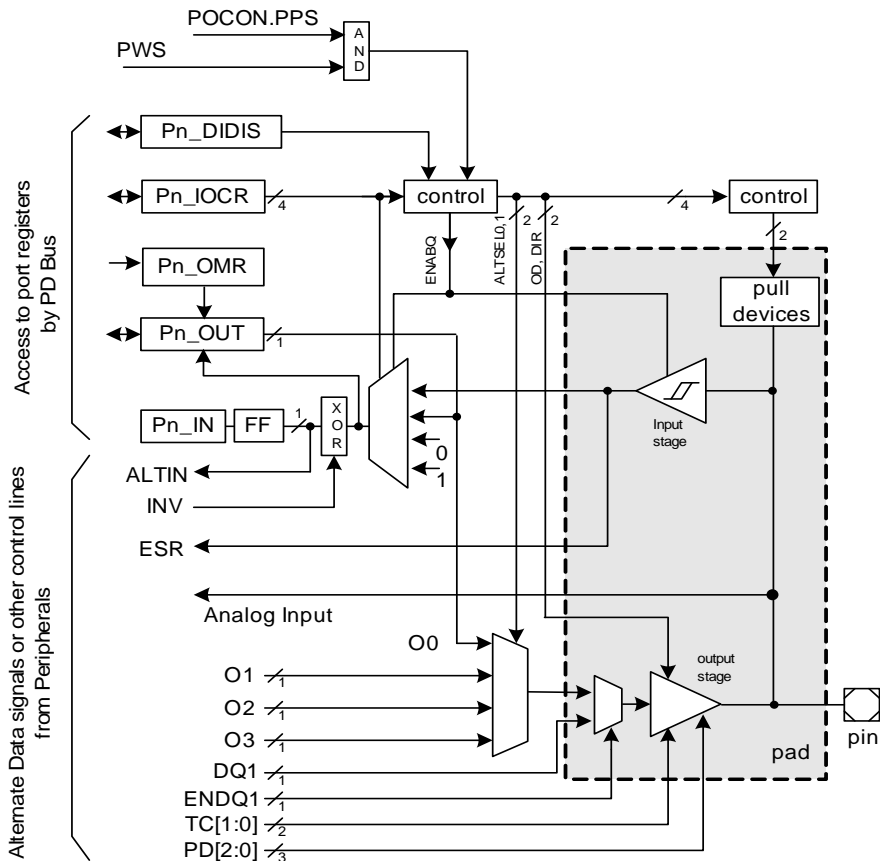


Figure 10-1 Digital Input/Output including Hardware Override Functionality

Note: If HW_EN is activated, INV signal is always zero.

Note: When HW_EN is disabled, the respective ports go to Power Save Mode as all other ports. When HW_EN is active, then the user should set the POCON.PPSx=0.



Analn_DigiIO_port_structure_4_um.vsd

Figure 10-2 Digital Input/Output with Analog Input Functionality

Note: INV signal is derived from Pn_IOC[R].PC[3:2].

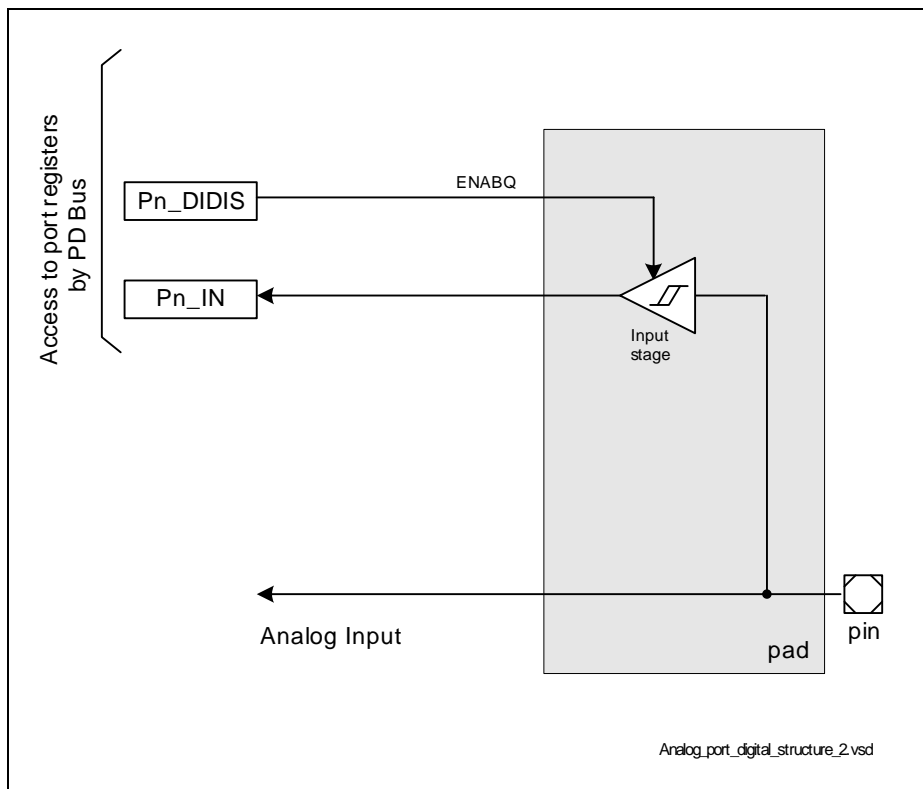


Figure 10-3 Digital and Analog Input Functionality

Note: There is always a standard digital input connected in parallel to each analog input.

10.1.2 Input Stage Control

An input stage consists of a Schmitt trigger, which can be enabled or disabled via software, and an input multiplexer that by default selects the output of the input Schmitt trigger.

A disabled input driver drives high logical level. During and after reset, all input stages are enabled by default.

10.1.3 Output Driver Control

An output stage consists of an output driver, output multiplexer, and register bit fields for their control.

10.1.3.1 Active Mode Behavior

Each output driver can be configured in a push-pull or an open-drain mode, or it can be deactivated (three-stated). An output multiplexer in front of the output driver selects the signal source, choosing either the appropriate bit of the Pn_OUT register, or one of maximum three lines coming from a peripheral unit, see [Figure 10-1](#). The selection is done via the Pn_IOC register. Software can set or clear the bit Pn_OUT.Px, which drives the port pin in case it is selected by the output multiplexer.

An output driver with hardware override can select an additional output signal coming from a peripheral. While the hardware override is activated, this signal has higher priority than all other output signals and can not be deselected by the port. In this case, the peripheral controls the direction of the pin.

In active mode the output is also fed back via the input Schmitt trigger and can be evaluated by on-chip components connected to this input.

10.1.3.2 Power Saving Mode Behavior

In Power Saving Mode (core and IO supply voltages available), the behavior of a pin depends on the setting of the PCONx.PPSx bit. Basically, groups of four pins within a port can be configured to react to Power Save Mode Request or to ignore it. In case a pin group is configured to react to a Power Save Mode Request, each pin within a group reacts according to its own configuration according to the [Table 10-4](#).

10.1.3.3 Reset Behavior

During an Internal Application Reset, all output stages of GPIO pins go to tri-state mode without any pull-up or pull-down devices.

An Application Reset does not change the GPIO configuration but the reset of the internal peripherals can change the data driven on the outputs. Attention must be paid to ensure that no harm is caused to the connected devices by unexpected transitions and output values.

10.1.3.4 Power-fail Behavior

When the core supply fails while the pad supply remains stable, the output stages go into tri-state mode.

10.2 Port Register Description

10.2.1 Pad Driver Control

The pad structure which is used in this device offers the possibility to select the output driver strength and the slew rate. These selections are independent from the output port functionality, such as open-drain, push/pull or input only.

In order to minimize EMI, the driver strength can be adapted to the application requirements by bit fields PDMx. The selection is done in groups of four pins.

The **Port Output Control registers** POCON provide the corresponding control bits. A 4-bit control field configures the driver strength and the edge shape. Word ports consume four control nibbles each, byte ports consume two control nibbles each.

Note: P2_POCON register in the XC27x8X contains an exception regarding the additional strong output driver connected in parallel to the standard output driver of the port pin P2.8. See the respective port section for details.

Px_POCON (x=0-4)

Port x Output Control Register XSFR (E8A0_H+2*x)

Reset Value: 0000_H

Px_POCON (x=6-11)

Port x Output Control Register XSFR (E8A0_H+2*x)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPS 3	PDM3			PPS 2	PDM2			PPS 1	PDM1			PPS 0	PDM0		
rw	rwr			rw	rw			rw	rw			rw	rw		

Field	Bit	Type	Description
PDM0, PDM1, PDM2, PDM3	[2:0], [6:4], [10:8], [14:12]	rw	Port Driver Mode x Code Driver strength ¹⁾ 000 _B Strong driver 001 _B Strong driver 010 _B Strong driver 011 _B Weak driver 100 _B Medium driver 101 _B Medium driver 110 _B Medium driver 111 _B Weak driver Edge Shape ²⁾ Sharp edge mode Medium edge mode Soft edge mode
PPS0, PPS1, PPS2, PPS3	3, 7, 11, 15	rw	Pin Power Save 0 _B Pin behaves like in the Active Mode. Power Save Management is ignored. 1 _B Behavior in the Power Save Mode described in the Table 10-4 .

¹⁾ Defines the current the respective driver can deliver to the external circuitry.

²⁾ Defines the switching characteristics to the respective new output level. This also influences the peak currents through the driver when producing an edge, i.e. when changing the output level.

Mapping of the POCON Registers to Pins and Ports

The table below lists the defined POCON registers and the allocation of control bit fields and port pins.

Table 10-2 Port Output Control Register Allocation

Control Register	Controlled Pins (by Px_POCON.[y:z]) ¹⁾				Port Width
	[15:12]	[11:8]	[7:4]	[3:0]	
P0_POCON	---	---	P0.[7:4]	P0.[3:0]	8
P1_POCON	---	---	P1.[7:4]	P1.[3:0]	8
P2_POCON	CLOCKOUT driver at P2.8 ²⁾	P2.[11:8] + P2.[13:12] ³⁾	P2.[7:4]	P2.[3:0]	14
P3_POCON	---	---	P3.[7:4]	P3.[3:0]	8
P4_POCON	---	---	P4.[7:4]	P4.[3:0]	8
P6_POCON	---	---	---	P6.[3:0]	4
P7_POCON	---	---	P7.4	P7.[3:0]	5
P8_POCON	---	---	P8.[6:4]	P8.[3:1]	6
P9_POCON	---	---	P9.[7:4]	P9.[3:0]	8
P10_POCON	P10.[15:12]	P10.[11:8]	P10.[7:4]	P10.[3:0]	16
P11_POCON	---	---	P11.[5:4]	P11.[3:0]	6

¹⁾ x denotes the port number, while [y:z] represents the bit field range.

²⁾ The control of the strong driver is described in the respective port section, [Chapter 10.3.3](#) for P2.8.

³⁾ The output control of P2.[13:12] deviates from the standard definition, see [Chapter 10.3.3](#).

Note: When assigning functional signals to port pins, please consider the fact that the driver strength is selected for pin groups. Assign functions with similar requirements to pins within the same POCON control group.

10.2.2 Port Output Register

The port output register defines the values of the output pins if the pin is used as general purpose output.

When used as input, the Pn_OUT bits can be used to sample the respective input value continuously and drive the last sampled value while in power saving mode, see [Table 10-4](#).

Pn_OUT (n=0-4)

Port n Output Register

SFR (FFA2_H+2*n)

Reset Value: 0000_H

Pn_OUT (n=6-11)

Port n Output Register

SFR (FFA2_H+2*n)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
Px (x = 0-15)	x	rwh	Port Output Bit x This bit defines the level at the output pin of port Pn, pin x if the output is selected as GPIO output. 0 _B The output level of Pn.x is 0. 1 _B The output level of Pn.x is 1.

10.2.3 Port Output Modification Register

With the port output modification register the port n output register bits get set, cleared, or toggled individually.

P2_OMRH

Port 2 Output Modification Register HighXSFR (E9CA_H) **Reset Value: XXXX_H**

P10_OMRH

Port 10 Output Modification Register HighXSFR (E9EA_H) **Reset Value: XXXX_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PC 15	PC 14	PC 13	PC 12	PC 11	PC 10	PC 9	PC 8	PS 15	PS 14	PS 13	PS 12	PS 11	PS 10	PS 9	PS 8
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Field	Bits	Type	Description
PS_x (x = 8-15)	x-8	W	Port Set Bit x Setting this bit sets or toggles the corresponding bit in the port output register Pn_OUT (see Table 10-3). On a read access, this bit returns an undefined value.
PC_x (x = 8-15)	x	W	Port Clear Bit x Setting this bit clears or toggles the corresponding bit in the port output register Pn_OUT. (see Table 10-3). On a read access, this bit returns an undefined value.

Pn_OMRL (n=0-4)

Port n Output Modification Register LowXSFR (E9C0_H+4*n) **Reset Value: XXXX_H**

Pn_OMRL (n=6-11)

Port n Output Modification Register LowXSFR (E9C0_H+4*n) **Reset Value: XXXX_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PC 7	PC 6	PC 5	PC 4	PC 3	PC 2	PC 1	PC 0	PS 7	PS 6	PS 5	PS 4	PS 3	PS 2	PS 1	PS 0
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Field	Bits	Type	Description
PSx (x = 0-7)	x	w	Port Set Bit x Setting this bit sets or toggles the corresponding bit in the port output register Pn_OUT (see Table 10-3). On a read access, this bit returns an undefined value.
PCx (x = 0-7)	x + 8	w	Port Clear Bit x Setting this bit clears or toggles the corresponding bit in the port output register Pn_OUT. (see Table 10-3). On a read access, this bit returns an undefined value.

Function of the PCx and PSx bit fields

Table 10-3 Function of the Bits PCx and PSx

PCx	PSx	Function
0 or no write access	0 or no write access	Bit Pn_OUT.Px is not changed.
0 or no write access	1	Bit Pn_OUT.Px is set.
1	0 or no write access	Bit Pn_OUT.Px is cleared.
1	1	Bit Pn_OUT.Px is toggled.

Note: If a bit position is not written (one out of two bytes not targeted by a byte write), the corresponding value is considered as 0. Toggling a bit requires one 16-bit write.

10.2.4 Port Input Register

The port input register contains the values currently read at the input pins, also if a port line is assigned as output.

Pn_IN (n=0-11)

Port n Input Register

SFR (FF80_H+2*n)

Reset Value: 0000_H¹⁾

P15_IN

Port 15 Input Register

SFR (FF9E_H)

Reset Value: 0000_H¹⁾

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

¹⁾ Px bits for non implemented I/O lines are always read as 0.

Field	Bits	Type	Description
Px (x = 0-15)	x	rh	Port Input Bit x This bit indicates the level at the input pin of port Pn, pin x. 0 _B The input level of Pn.x is 0. 1 _B The input level of Pn.x is 1.

10.2.5 Port Input/Output Control Registers

The port input/output control registers contain the bit fields to select the digital output and input driver characteristics, such as pull-up/down devices, port direction (input/output), open-drain and alternate output selections. The coding of the options is shown in [Table 10-4](#).

Depending on the port functionality not all of the input/output control registers may be implemented. The structure with one control bit field for each port pin located in different registers offers the possibility to configure port pin functionality of a single pin without accessing some other PCx in the same register by word-oriented writes.

P0_IOCR_x (x=00-07)

Port 0 Input/Output Control Register x XSFR (E800_H+2*x) Reset Value: 0000_H

P1_IOCR_x (x=00-07)

Port 1 Input/Output Control Register x XSFR (E820_H+2*x) Reset Value: 0000_H

P2_IOCR_x (x=00-13)

Port 2 Input/Output Control Register x XSFR (E840_H+2*x) Reset Value: 0000_H

P3_IOCR_x (x=00-07)

Port 3 Input/Output Control Register x XSFR (E860_H+2*x) Reset Value: 0000_H

P4_IOCR_x (x=00-07)

Port 4 Input/Output Control Register x XSFR (E880_H+2*x) Reset Value: 0000_H

P6_IOCR_x (x=00-03)

Port 6 Input/Output Control Register x XSFR (E8C0_H+2*x) Reset Value: 0000_H

P7_IOCR_x (x=00-04)

Port 7 Input/Output Control Register x XSFR (E8E0_H+2*x) Reset Value: 0000_H

P8_IOCR_x (x=01-06)

Port 8 Input/Output Control Register x XSFR (E900_H+2*x) Reset Value: 0000_H

P9_IOCR_x (x=00-07)

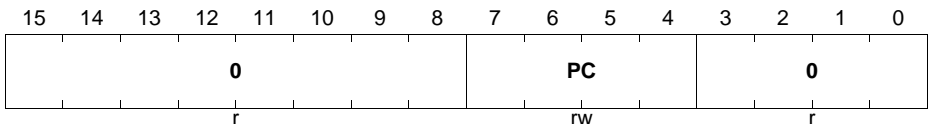
Port 9 Input/Output Control Register x XSFR (E920_H+2*x) Reset Value: 0000_H

P10_IOCR_x (x=00-15)

Port 10 Input/Output Control Register x XSFR (E940_H+2*x) Reset Value: 0000_H

P11_IOCR_x (x=00-05)

Port 11 Input/Output Control Register x XSFR (E960_H+2*x) Reset Value: 0000_H



Field	Bits	Type	Description
PC	[7:4]	rw	Port Input/Output Control Bit see Table 10-4
0	[3:0], [15:8]	r	reserved

Coding of the PC bit field

The coding of the GPIO port behavior is done by the bit fields in the port control registers Pn_IOCRx. There's a control bit field PC for each port pin. The bit fields PC are located in separate control registers in order to allow modifying a port pin (without influencing the others) with simple move operations.

Note: When the pin direction is switched to output and the mode is test mode, the output characteristic must be push-pull only.

Table 10-4 PC Coding

PC[3:0]	I/O	Selected Pull-up/down / Selected Output Function	Behavior in Power Saving Mode ¹⁾
0000 _B	Direct Input	No pull device connected	Input value = Pn_OUT; no pull
0001 _B		Pull-down device connected	Input value = 0; pull-down
0010 _B		Pull-up device connected	Input value = 1; pull-up
0011 _B		No pull device connected. In this mode Pn_OUT samples the pad input value continuously.	Input value = Pn_OUT; Pn_OUT always samples input value while not in power save mode = freeze of input value; no pull
0100 _B	Inverted Input	No pull device connected	Input value = $\overline{\text{Pn_OUT}}$; no pull
0101 _B		Pull-down device connected	Input value = 1; pull-down
0110 _B		Pull-up device connected	Input value = 0; pull-up
0111 _B		No pull device connected In this mode Pn_OUT samples the pad input value continuously.	Input value = $\overline{\text{Pn_OUT}}$; Pn_OUT always samples input value while not in power saving mode = freeze of input value; no pull ²⁾

Table 10-4 PC Coding (cont'd)

PC[3:0]	I/O	Selected Pull-up/down / Selected Output Function	Behavior in Power Saving Mode¹⁾
1000 _B	Output (Direct input) Push- pull	General purpose Output O0	Output driver off. Input Schmitt trigger off. Pn_OUT delivered to the internal logic; no pull
1001 _B		Output function O1	
1010 _B		Output function O2	
1011 _B		Output function O3	
1100 _B	Output (Direct input) Open- drain	General purpose Output O0	
1101 _B		Output function O1	
1110 _B		Output function O2	
1111 _B		Output function O3	

¹⁾ In power saving mode, the input Schmitt trigger is always switched off. A defined input value is driven to the internal circuitry instead of the level detected at the input pin.

²⁾ If the IOCR setting is "inverted input", then an inverted signal Pn_OUT is driven internally. The Pn_OUT register itself always contains the real, non-inverted input value of the pin. See Figure 7-1 and Figure 7-2.

10.2.6 Port Digital Input and Output Disable Register

Ports 5 and 15 have, additionally to the analog input functionality, digital input functionality too. In order to save switching of the internal Schmitt triggers of the digital inputs, they can be disabled by means of Px_DIDIS Register.

Ports 6 has, additionally to the analog input functionality, digital input and output functionality too. In order to save switching of the internal Schmitt triggers of the digital inputs, as well as to avoid errors caused by the digital output drivers and the pull devices, they can be disabled by means of the P6_DIDIS Register for pins used as analog inputs. For all analog inputs of P6 the digital settings are overridden and ineffective, also in power saving mode.

P5_DIDIS

Port 5 Digital Input Disable RegisterSFR (FE8A_H)

Reset Value: 0000_H

P6_DIDIS

Port 6 Digital IO Disable Register SFR (FE4E_H)

Reset Value: 0000_H

P15_DIDIS

Port 15 Digital Input Disable RegisterSFR (FE9E_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bit	Type	Description
Py (y = 0-15)	y	rw	Bit y Digital Input Control 0 _B Digital input stage (schmitt trigger) is enabled. 1 _B Digital input stage (schmitt trigger) is disabled, necessary if pin is used as analog input.

10.3 Port Description

The bit positions in the port registers always start right-aligned. For example, a port comprising only 8 pins only uses the bit positions [7:0] of the corresponding register. The remaining bit positions are filled with 0 (r).

The pad driver mode registers may be different for each port. As a result, they are described independently for each port in the corresponding chapter.

10.3.1 Port 0

Port 0 is an 8-bit GPIO port. The registers of Port 0 are shown in [Figure 10-4](#).

For this port, all pins can be read as GPIO, from the Port Input Register.

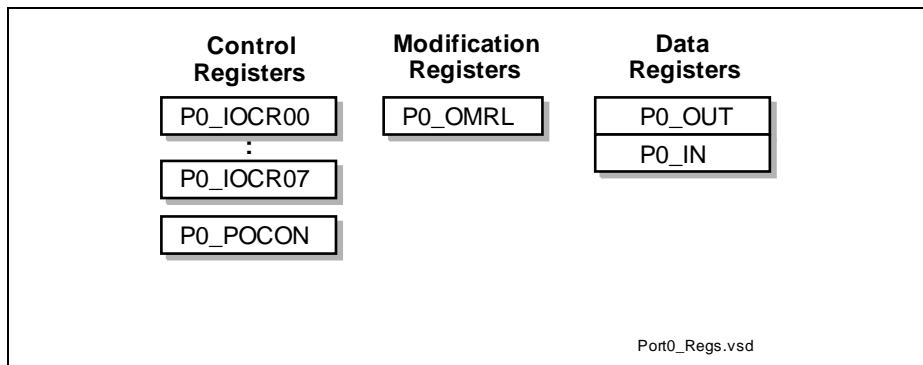


Figure 10-4 Port 0 Register Overview

Table 10-5 Port 0 Registers

Register Short Name	Register Long Name	Address Offset	Reset Value
P0_OUT	Port 0 Output Register	FFA2 _H	0000 _H
P0_IN	Port 0 Input Register	FF80 _H	0000 _H
P0_OMRL	Port 0 Output Modification Register Low	E9C0 _H	XXXX _H
P0_POCON	Port 0 Output Control Register	E8A0 _H	0000 _H
P0_IOCRO0	Port 0 Input/Output Control Register 0	E800 _H	0000 _H
P0_IOCRO1	Port 0 Input/Output Control Register 1	E802 _H	0000 _H
P0_IOCRO2	Port 0 Input/Output Control Register 2	E804 _H	0000 _H
P0_IOCRO3	Port 0 Input/Output Control Register 3	E806 _H	0000 _H
P0_IOCRO4	Port 0 Input/Output Control Register 4	E808 _H	0000 _H
P0_IOCRO5	Port 0 Input/Output Control Register 5	E80A _H	0000 _H
P0_IOCRO6	Port 0 Input/Output Control Register 6	E80C _H	0000 _H
P0_IOCRO7	Port 0 Input/Output Control Register 7	E80E _H	0000 _H

10.3.2 Port 1

Port 1 is an 8-bit GPIO port. The registers of Port 1 are shown in [Figure 10-5](#).

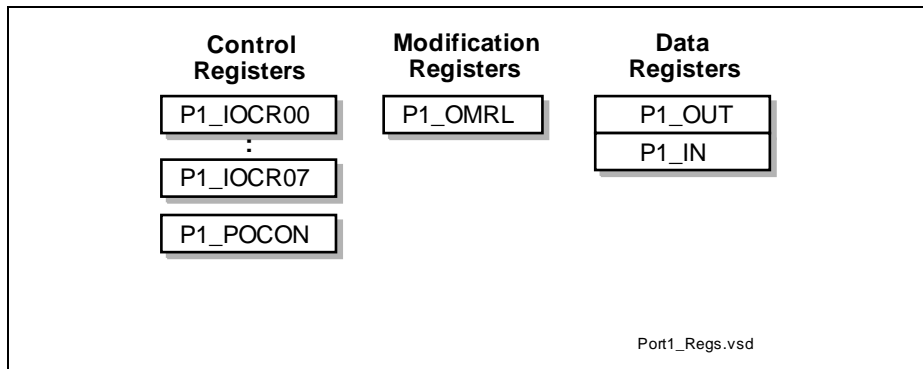


Figure 10-5 Port 1 Register Overview

For this port, all pins can be read as GPIO, from the Port Input Register.

Table 10-6 Port 1 Registers

Register Short Name	Register Long Name	Address Offset	Reset Value
P1_OUT	Port 1 Output Register	FFA4 _H	0000 _H
P1_IN	Port 1 Input Register	FF82 _H	0000 _H
P1_OMRL	Port 1 Output Modification Register Low	E9C4 _H	XXXX _H
P1_POCON	Port 1 Output Control Register	E8A2 _H	0000 _H
P1_IOCRO0	Port 1 Input/Output Control Register 0	E820 _H	0000 _H
P1_IOCRO1	Port 1 Input/Output Control Register 1	E822 _H	0000 _H
P1_IOCRO2	Port 1 Input/Output Control Register 2	E824 _H	0000 _H
P1_IOCRO3	Port 1 Input/Output Control Register 3	E826 _H	0000 _H
P1_IOCRO4	Port 1 Input/Output Control Register 4	E828 _H	0000 _H
P1_IOCRO5	Port 1 Input/Output Control Register 5	E82A _H	0000 _H
P1_IOCRO6	Port 1 Input/Output Control Register 6	E82C _H	0000 _H
P1_IOCRO7	Port 1 Input/Output Control Register 7	E82E _H	0000 _H

10.3.3 Port 2

Port 2 is a 14-bit GPIO port. The registers of Port 2 are shown in [Figure 10-6](#).
For this port, all pins can be read as GPIO, from the Port Input Register.

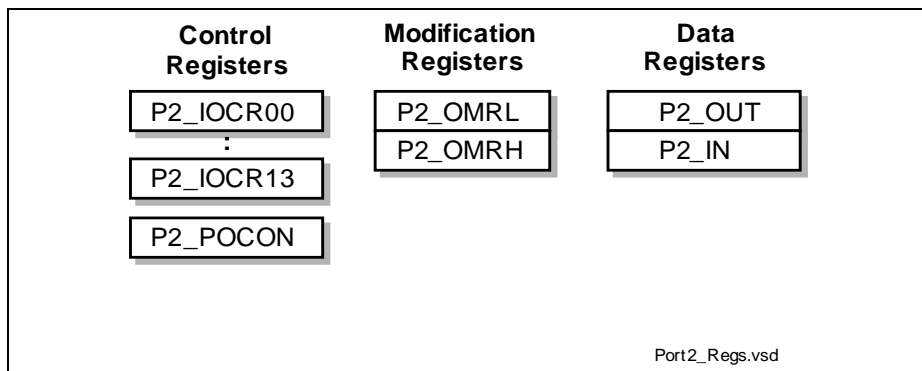


Figure 10-6 Port 2 Register Overview

Table 10-7 Port 2 Registers

Register Short Name	Register Long Name	Address Offset	Reset Value
P2_OUT	Port 2 Output Register	FFA6 _H	0000 _H
P2_IN	Port 2 Input Register	FF84 _H	0000 _H
P2_OMRL	Port 2 Output Modification Register Low	E9C8 _H	XXXX _H
P2_OMRH	Port 2 Output Modification Register High	E9CA _H	XXXX _H
P2_POCON	Port 2 Output Control Register	E8A4 _H	0000 _H
P2_IOCRR0	Port 2 Input/Output Control Register 0	E840 _H	0000 _H
P2_IOCRR1	Port 2 Input/Output Control Register 1	E842 _H	0000 _H
P2_IOCRR2	Port 2 Input/Output Control Register 2	E844 _H	0000 _H
P2_IOCRR3	Port 2 Input/Output Control Register 3	E846 _H	0000 _H
P2_IOCRR4	Port 2 Input/Output Control Register 4	E848 _H	0000 _H
P2_IOCRR5	Port 2 Input/Output Control Register 5	E84A _H	0000 _H
P2_IOCRR6	Port 2 Input/Output Control Register 6	E84C _H	0000 _H
P2_IOCRR7	Port 2 Input/Output Control Register 7	E84E _H	0000 _H
P2_IOCRR8	Port 2 Input/Output Control Register 8	E850 _H	0000 _H
P2_IOCRR9	Port 2 Input/Output Control Register 9	E852 _H	0000 _H

Table 10-7 Port 2 Registers (cont'd)

Register Short Name	Register Long Name	Address Offset	Reset Value
P2_IOCRR10	Port 2 Input/Output Control Register 10	E854 _H	0000 _H
P2_IOCRR11	Port 2 Input/Output Control Register 11	E856 _H	0000 _H
P2_IOCRR12	Port 2 Input/Output Control Register 12	E858 _H	0000 _H
P2_IOCRR13	Port 2 Input/Output Control Register 13	E85A _H	0000 _H

The CLKOUT Pad P2.8

In order to drive high frequency clock signals, a strong driver is connected in parallel to the normal output driver of P2.8. It is enabled instead of the standard driver if bit field P2_POCON.PDM3 = xx1_B.

The strong clock driver only operates in strong driver sharp edge mode, i.e. it is not controlled by the driver-strength settings (P2_POCON.PDM2) for the standard driver.

It has no pull devices but can be switched to input or output via register P2_IOCRR08.

Output Control for Pins P2.[13:12]

Because bit field P2_POCON.PDM3 controls the strong clock driver of P2.8, the driver mode of pins P2.[13:12] is controlled by the bit field P2_POCON.PDM2, together with pins P2.[11:8].

The power saving behavior of pins P2.[13:12] is controlled by bit P2_POCON.PPS3.

10.3.4 Port 3

Port 3 is an 8-bit GPIO port. The registers of Port 3 are shown in [Figure 10-7](#).

For this port, all pins can be read as GPIO, from the Port Input Register.

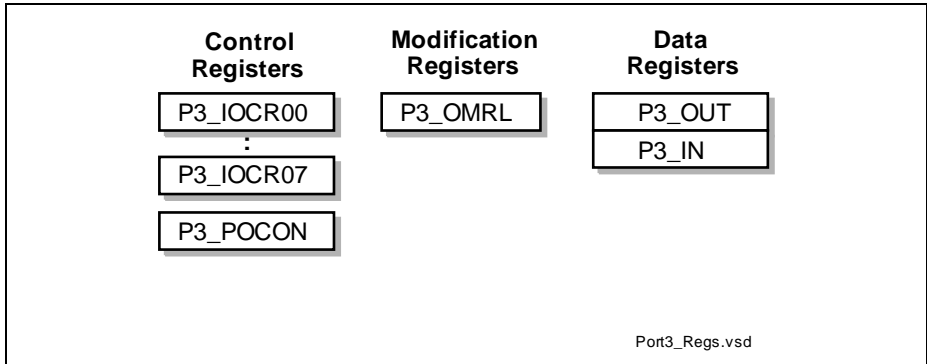


Figure 10-7 Port 3 Register Overview

Table 10-8 Port 3 Registers

Register Short Name	Register Long Name	Address Offset	Reset Value
P3_OUT	Port 3 Output Register	FFA8 _H	0000 _H
P3_IN	Port 3 Input Register	FF86 _H	0000 _H
P3_OMRL	Port 3 Output Modification Register Low	E9CC _H	XXXX _H
P3_POCON	Port 3 Output Control Register	E8A6 _H	0000 _H
P3_IOCRO0	Port 3 Input/Output Control Register 0	E860 _H	0000 _H
P3_IOCRO1	Port 3 Input/Output Control Register 1	E862 _H	0000 _H
P3_IOCRO2	Port 3 Input/Output Control Register 2	E864 _H	0000 _H
P3_IOCRO3	Port 3 Input/Output Control Register 3	E866 _H	0000 _H
P3_IOCRO4	Port 3 Input/Output Control Register 4	E868 _H	0000 _H
P3_IOCRO5	Port 3 Input/Output Control Register 5	E86A _H	0000 _H
P3_IOCRO6	Port 3 Input/Output Control Register 6	E86C _H	0000 _H
P3_IOCRO7	Port 3 Input/Output Control Register 7	E86E _H	0000 _H

10.3.5 Port 4

Port 4 is an 8-bit GPIO port. The registers of Port 4 are shown in [Figure 10-8](#).

For this port, all pins can be read as GPIO, from the Port Input Register.

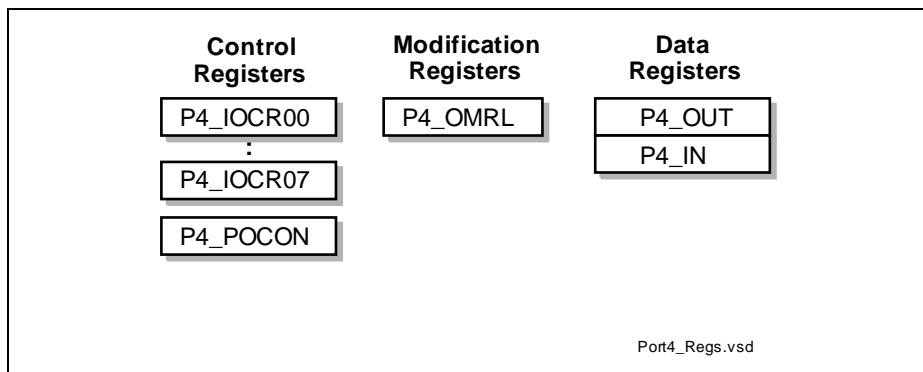


Figure 10-8 Port 4 Register Overview

Table 10-9 Port 4 Registers

Register Short Name	Register Long Name	Address Offset	Reset Value
P4_OUT	Port 4 Output Register	FFAA _H	0000 _H
P4_IN	Port 4 Input Register	FF88 _H	0000 _H
P4_OMRL	Port 4 Output Modification Register Low	E9D0 _H	XXXX _H
P4_POCON	Port 4 Output Control Register	E8A8 _H	0000 _H
P4_IOCRO0	Port 4 Input/Output Control Register 0	E880 _H	0000 _H
P4_IOCRO1	Port 4 Input/Output Control Register 1	E882 _H	0000 _H
P4_IOCRO2	Port 4 Input/Output Control Register 2	E884 _H	0000 _H
P4_IOCRO3	Port 4 Input/Output Control Register 3	E886 _H	0000 _H
P4_IOCRO4	Port 4 Input/Output Control Register 4	E888 _H	0000 _H
P4_IOCRO5	Port 4 Input/Output Control Register 5	E88A _H	0000 _H
P4_IOCRO6	Port 4 Input/Output Control Register 6	E88C _H	0000 _H
P4_IOCRO7	Port 4 Input/Output Control Register 7	E88E _H	0000 _H

10.3.6 Port 5

Port 5 is a 16-bit analog or digital input port.

To use the Port 5 as an analog input, the Schmitt trigger in the input stage must be disabled. This is achieved by setting the corresponding bit in the register P5_DIDIS.

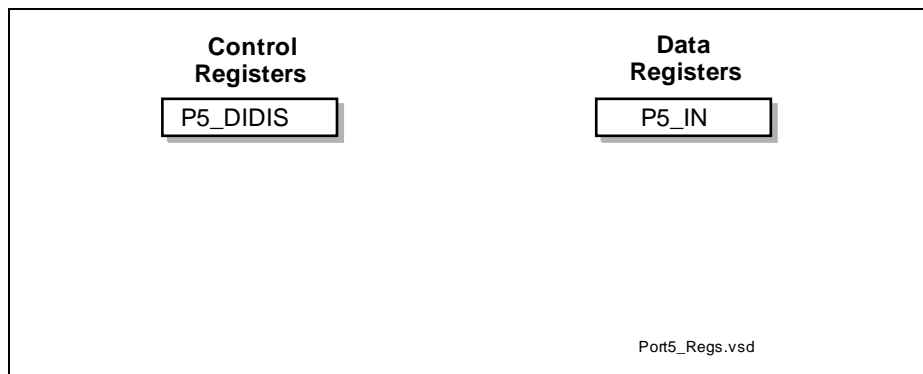


Figure 10-9 Port 5 Register Overview

Table 10-10 Port 5 Registers

Register Short Name	Register Long Name	Address Offset	Reset Value
P5_IN	Port 5 Input Register	FF8A _H	0000 _H
P5_DIDIS	Port 5 Digital Input Disable Register	FE8A _H	0000 _H

10.3.7 Port 6

Port 6 is a 4-bit GPIO and analog input port. The registers of Port 6 are shown in [Figure 10-10](#).

For this port, all pins can be read as GPIO, from the Port Input Register.

When used as analog input, the digital part of the respective pin can be disabled via P6_DIDIS, see [Chapter 10.2.6](#).

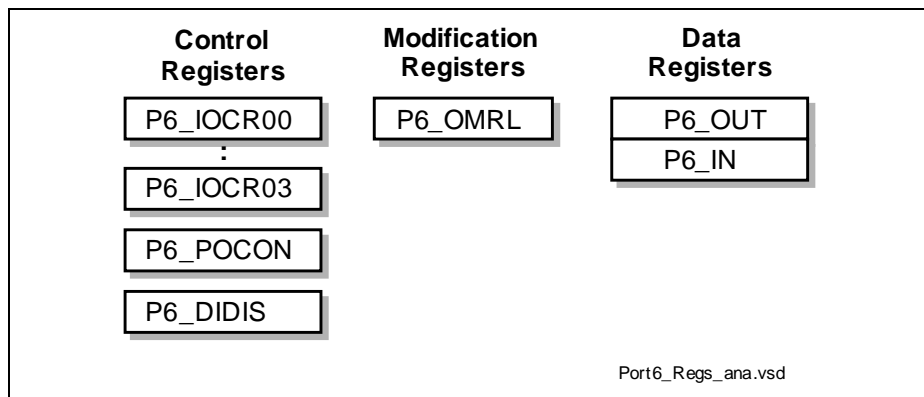


Figure 10-10 Port 6 Register Overview

Table 10-11 Port 6 Registers

Register Short Name	Register Long Name	Address Offset	Reset Value
P6_OUT	Port 6 Output Register	FFAE _H	0000 _H
P6_IN	Port 6 Input Register	FF8C _H	0000 _H
P6_DIDIS	Port 6 Digital IO Disable Register	FE4E _H	0000 _H
P6_OMRL	Port 6 Output Modification Register Low	E9D8 _H	XXXX _H
P6_POCON	Port 6 Output Control Register	E8AC _H	0000 _H
P6_IOCRO0	Port 6 Input/Output Control Register 0	E8C0 _H	0000 _H
P6_IOCRO1	Port 6 Input/Output Control Register 1	E8C2 _H	0000 _H
P6_IOCRO2	Port 6 Input/Output Control Register 2	E8C4 _H	0000 _H
P6_IOCRO3	Port 6 Input/Output Control Register 3	E8C6 _H	0000 _H

Noise reduction for Analog to Digital Converter

As Port 6 shares the same power supply as the Analog to Digital Converter, caution has to be taken with respect to switching noise caused by the Port 6 digital outputs. Switching strong output drivers during the sampling phase may severely reduce the precision of the AD Conversion. If switching during the sample phase can't be avoided, it is advised to do this only with weak or medium output drivers.

If the P6 port is used to control an external analog multiplexer of ADC0, the ADC itself controls the switching of the outputs and does so only while the ADC0 is not in the sampling phase. However, per default the sampling phases of ADC0 and ADC1 are not synchronised and so caution has still to be paid with respect to the ADC1 sampling phase.

10.3.8 Port 7

Port 7 is a 5-bit GPIO port. The port registers of Port 7 are shown in [Figure 10-11](#). For this port, all pins can be read as GPIO, from the Port Input Register.

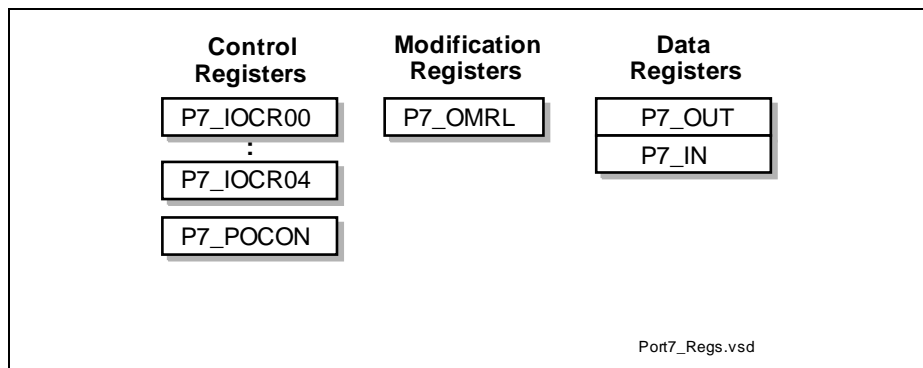


Figure 10-11 Port 7 Register Overview

Table 10-12 Port 7 Registers

Register Short Name	Register Long Name	Address Offset	Reset Value
P7_OUT	Port 7 Output Register	FFB0 _H	0000 _H
P7_IN	Port 7 Input Register	FF8E _H	0000 _H
P7_OMRL	Port 7 Output Modification Register Low	E9DC _H	XXXX _H
P7_POCON	Port 7 Output Control Register	E8AE _H	0000 _H
P7_IOCRR00	Port 7 Input/Output Control Register 0	E8E0 _H	0000 _H
P7_IOCRR01	Port 7 Input/Output Control Register 1	E8E2 _H	0000 _H
P7_IOCRR02	Port 7 Input/Output Control Register 2	E8E4 _H	0000 _H
P7_IOCRR03	Port 7 Input/Output Control Register 3	E8E6 _H	0000 _H
P7_IOCRR04	Port 7 Input/Output Control Register 4	E8E8 _H	0000 _H

10.3.9 Port 8

Port 8 is a 6-bit GPIO port. The registers of Port 8 are shown in [Figure 10-12](#).

For this port, all pins can be read as GPIO, from the Port Input Register.

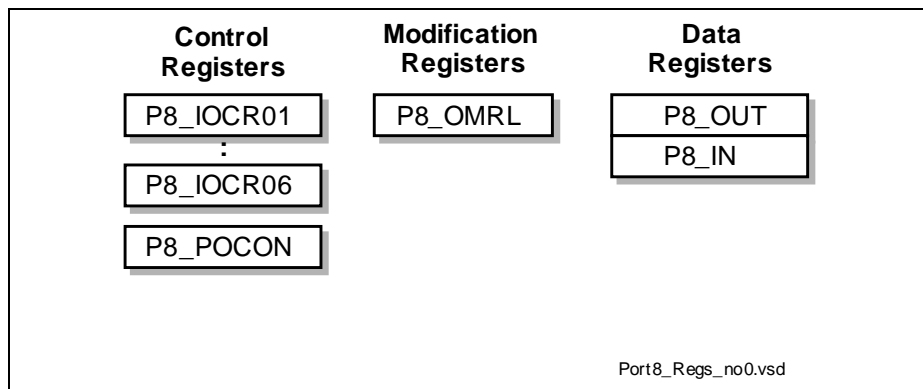


Figure 10-12 Port 8 Register Overview

Table 10-13 Port 8 Registers

Register Short Name	Register Long Name	Address Offset	Reset Value
P8_OUT	Port 8 Output Register	FFB2 _H	0000 _H
P8_IN	Port 8 Input Register	FF90 _H	0000 _H
P8_OMRL	Port 8 Output Modification Register Low	E9E0 _H	XXXX _H
P8_POCON	Port 8 Output Control Register	E8B0 _H	0000 _H
P8_IOCRO1	Port 8 Input/Output Control Register 1	E902 _H	0000 _H
P8_IOCRO2	Port 8 Input/Output Control Register 2	E904 _H	0000 _H
P8_IOCRO3	Port 8 Input/Output Control Register 3	E906 _H	0000 _H
P8_IOCRO4	Port 8 Input/Output Control Register 4	E908 _H	0000 _H
P8_IOCRO5	Port 8 Input/Output Control Register 5	E90A _H	0000 _H
P8_IOCRO6	Port 8 Input/Output Control Register 6	E90C _H	0000 _H

10.3.10 Port 9

Port 9 is an 8-bit GPIO port. The port registers of Port 9 are shown in [Figure 10-13](#). For this port, all pins can be read as GPIO, from the Port Input Register.

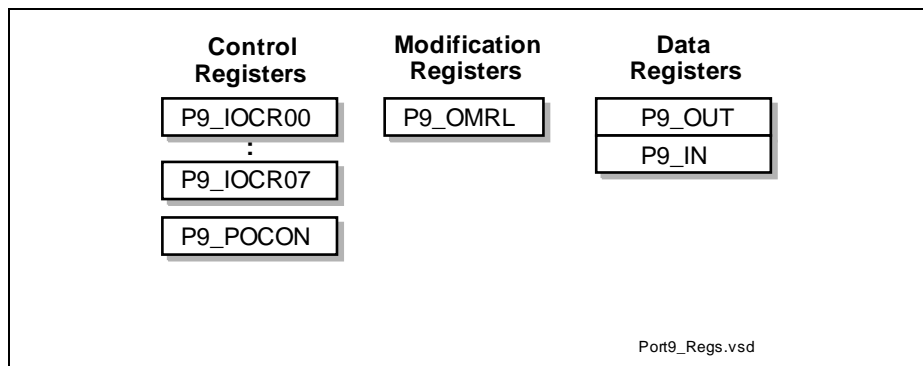


Figure 10-13 Port 9 Register Overview

Table 10-14 Port 9 Registers

Register Short Name	Register Long Name	Address Offset	Reset Value
P9_OUT	Port 9 Output Register	FFB4 _H	0000 _H
P9_IN	Port 9 Input Register	FF92 _H	0000 _H
P9_OMRL	Port 9 Output Modification Register Low	E9E4 _H	XXXX _H
P9_POCON	Port 9 Output Control Register	E8B2 _H	0000 _H
P9_IOCR00	Port 9 Input/Output Control Register 0	E920 _H	0000 _H
P9_IOCR01	Port 9 Input/Output Control Register 1	E922 _H	0000 _H
P9_IOCR02	Port 9 Input/Output Control Register 2	E924 _H	0000 _H
P9_IOCR03	Port 9 Input/Output Control Register 3	E926 _H	0000 _H
P9_IOCR04	Port 9 Input/Output Control Register 4	E928 _H	0000 _H
P9_IOCR05	Port 9 Input/Output Control Register 5	E92A _H	0000 _H
P9_IOCR06	Port 9 Input/Output Control Register 6	E92C _H	0000 _H
P9_IOCR07	Port 9 Input/Output Control Register 7	E92E _H	0000 _H

10.3.11 Port 10

Port 10 is a 16-bit GPIO port. The registers of Port 10 are shown in [Figure 10-14](#).

For this port, all pins can be read as GPIO, from the Port Input Register.

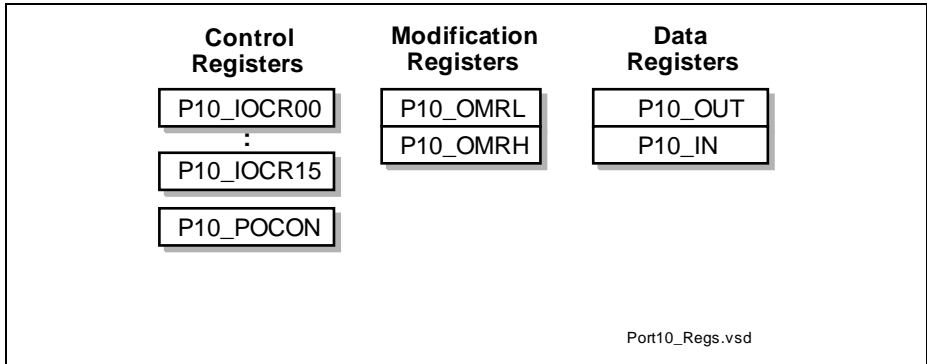


Figure 10-14 Port 10 Register Overview

Table 10-15 Port 10 Registers

Register Short Name	Register Long Name	Address Offset	Reset Value
P10_OUT	Port 10 Output Register	FFB6 _H	0000 _H
P10_IN	Port 10 Input Register	FF94 _H	0000 _H
P10_OMRL	Port 10 Output Modification Register Low	E9E8 _H	XXXX _H
P10_OMRH	Port 10 Output Modification Register High	E9EA _H	XXXX _H
P10_POCON	Port 10 Output Control Register	E8B4 _H	0000 _H
P10_IOCRR0	Port 10 Input/Output Control Register 0	E940 _H	0000 _H
P10_IOCRR1	Port 10 Input/Output Control Register 1	E942 _H	0000 _H
P10_IOCRR2	Port 10 Input/Output Control Register 2	E944 _H	0000 _H
P10_IOCRR3	Port 10 Input/Output Control Register 3	E946 _H	0000 _H
P10_IOCRR4	Port 10 Input/Output Control Register 4	E948 _H	0000 _H
P10_IOCRR5	Port 10 Input/Output Control Register 5	E94A _H	0000 _H
P10_IOCRR6	Port 10 Input/Output Control Register 6	E94C _H	0000 _H
P10_IOCRR7	Port 10 Input/Output Control Register 7	E94E _H	0000 _H
P10_IOCRR8	Port 10 Input/Output Control Register 8	E950 _H	0000 _H
P10_IOCRR9	Port 10 Input/Output Control Register 9	E952 _H	0000 _H

Table 10-15 Port 10 Registers (cont'd)

Register Short Name	Register Long Name	Address Offset	Reset Value
P10_IOC10	Port 10 Input/Output Control Register 10	E954 _H	0000 _H
P10_IOC11	Port 10 Input/Output Control Register 11	E956 _H	0000 _H
P10_IOC12	Port 10 Input/Output Control Register 12	E958 _H	0000 _H
P10_IOC13	Port 10 Input/Output Control Register 13	E95A _H	0000 _H
P10_IOC14	Port 10 Input/Output Control Register 14	E95C _H	0000 _H
P10_IOC15	Port 10 Input/Output Control Register 15	E95E _H	0000 _H

10.3.12 Port 11

Port 11 is a 6-bit GPIO port. The registers of Port 11 are shown in [Figure 10-15](#).
For this port, all pins can be read as GPIO, from the Port Input Register.

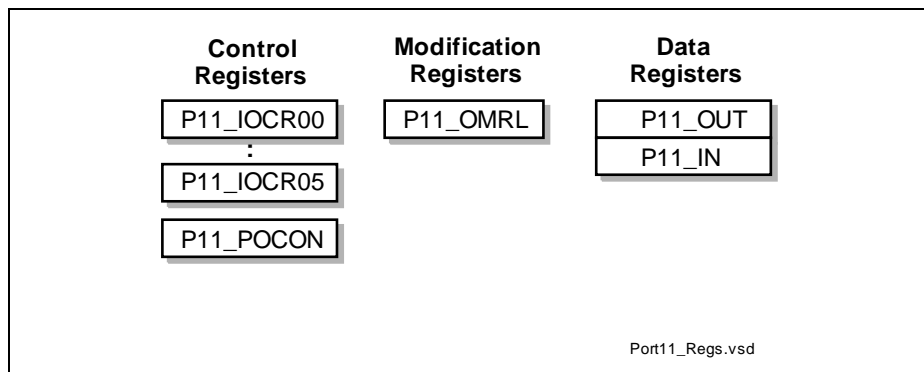


Figure 10-15 Port 11 Register Overview

Table 10-16 Port 11 Registers

Register Short Name	Register Long Name	Address Offset	Reset Value
P11_OUT	Port 11 Output Register	FFB8 _H	0000 _H
P11_IN	Port 11 Input Register	FF96 _H	0000 _H
P11_OMRL	Port 11 Output Modification Register Low	E9EC _H	XXXX _H
P11_POCON	Port 11 Output Control Register	E8B6 _H	0000 _H
P11_IOCRO0	Port 11 Input/Output Control Register 0	E960 _H	0000 _H
P11_IOCRO1	Port 11 Input/Output Control Register 1	E962 _H	0000 _H
P11_IOCRO2	Port 11 Input/Output Control Register 2	E964 _H	0000 _H
P11_IOCRO3	Port 11 Input/Output Control Register 3	E966 _H	0000 _H
P11_IOCRO4	Port 11 Input/Output Control Register 4	E968 _H	0000 _H
P11_IOCRO5	Port 11 Input/Output Control Register 5	E96A _H	0000 _H

10.3.13 Port 15

Port 15 is an 8-bit analog or digital input port.

To use the Port 15 as an analog input, the Schmitt trigger in the input stage must be disabled. This is achieved by setting the corresponding bit in the register P15_DIDIS.

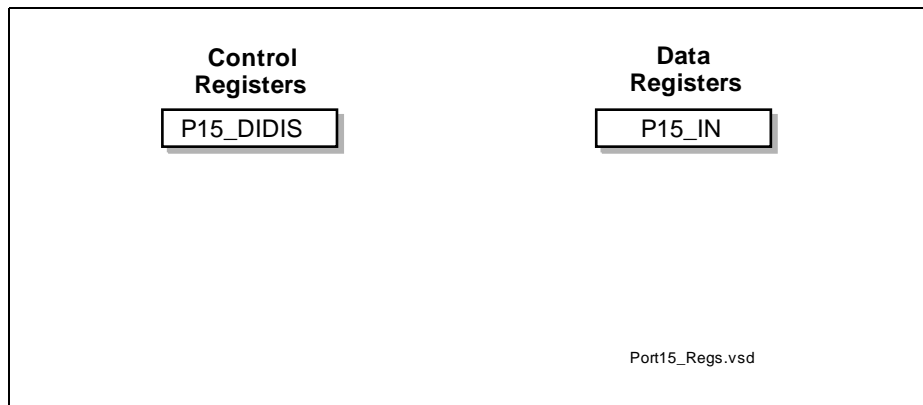


Figure 10-16 Port 15 Register Overview

Table 10-17 Port 15 Registers

Register Short Name	Register Long Name	Address Offset	Reset Value
P15_IN	Port 15 Input Register	FF9E _H	0000 _H
P15_DIDIS	Port 15 Digital Input Disable Register	FE9E _H	0000 _H

10.4 Pin Description

Each port pin of the XC27x8X can serve several functions of different modules. Also, most functions are available on several port pins. This enables an application to select the optimal connections for its specific circumstances.

A pin can output its own port output signal or one of up to three signals coming from the peripherals. Its input signal is available in its own input register and at several peripherals.

Note: Output signals are selected at the respective port pin, input signals are selected at the respective peripheral.

Optionally a pin can be fully controlled by a peripheral, in case the peripheral is enabled (for example, EBC).

Table 10-18 summarizes the various functions of each port and pin of the XC27x8X. The 'Pin' column references to the PG-LQFP-144 package.

Notes to the Pin Definitions table

- **Ctrl.:** The output signal for a port pin is selected via bitfield PC in the associated register Px_IOCry. Output O0 is selected by setting the respective bitfield PC to 1x00_B, output O1 is selected by 1x01_B, etc.
OH output signals and IH input signals are controlled by the hardware override.
- **Type:** Indicates the employed pad type (St=standard pad, Sp=special pad, DP=double pad, In=input pad, DA=digital IO and analog input, PS=power supply) and its power supply domain (A, B, M, 1).

Table 10-18 Pin Definitions and Functions

Pin	Symbol	Ctrl.	Type	Function
3	TESTM	I	In/B	Testmode Enable Enables factory test modes, must be held HIGH for normal operation (connect to V_{DDPB}). An internal pull-up device will hold this pin high when nothing is driving it.

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
4	P7.2	O0 / I	St/B	Bit 2 of Port 7, General Purpose Input/Output
	EMUX0	O1	St/B	External Analog MUX Control Output 0 (ADC1)
	TxDC4	O2	St/B	CAN Node 4 Transmit Data Output
	TxDC5	O3	St/B	CAN Node 5 Transmit Data Output
	CCU62_CCP OS0A	I	St/B	CCU62 Position Input 0
	TDI_C	IH	St/B	JTAG Test Data Input If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it.
5	P8.4	O0 / I	St/B	Bit 4 of Port 8, General Purpose Input/Output
	CCU60_COU T61	O1	St/B	CCU60 Channel 1 Output
	CCU62_CC6 1	O2	St/B	CCU62 Channel 1 Output
	TMS_D	IH	St/B	JTAG Test Mode Selection Input If JTAG pos. D is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it.
	CCU62_CC6 1INB	I	St/B	CCU62 Channel 1 Input
	U4C1_DX1A	I	St/B	USIC4 Channel 1 Shift Clock Input
6	$\overline{\text{TRST}}$	I	In/B	Test-System Reset Input For normal system operation, pin $\overline{\text{TRST}}$ should be held low. A high level at this pin at the rising edge of $\overline{\text{PORST}}$ activates the XC27x8X's debug system. In this case, pin $\overline{\text{TRST}}$ must be driven low once to reset the debug system. An internal pull-down device will hold this pin low when nothing is driving it.

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
7	P8.3	O0 / I	St/B	Bit 3 of Port 8, General Purpose Input/Output
	CCU60_COU T60	O1	St/B	CCU60 Channel 0 Output
	CCU62_CC6 0	O2	St/B	CCU62 Channel 0 Output
	U4C1_SELO 0	O3	St/B	USIC4 Channel 1 Select/Control 0 Output
	TDI_D	IH	St/B	JTAG Test Data Input If JTAG pos. D is selected during start-up, an internal pull-up device will hold this pin low when nothing is driving it.
	CCU62_CC6 0INB	I	St/B	CCU62 Channel 0 Input
8	P7.0	O0 / I	St/B	Bit 0 of Port 7, General Purpose Input/Output
	T3OUT	O1	St/B	GPT12E Timer T3 Toggle Latch Output
	T6OUT	O2	St/B	GPT12E Timer T6 Toggle Latch Output
	TDO_A	OH / IH	St/B	JTAG Test Data Output / DAP1 Input/Output If DAP pos. 0 or 2 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	ESR2_1	I	St/B	ESR2 Trigger Input 1
	RxDC4B	I	St/B	CAN Node 4 Receive Data Input
	U4C1_DX0C	I	St/B	USIC4 Channel 0 Receive Data Input
9	P7.3	O0 / I	St/B	Bit 3 of Port 7, General Purpose Input/Output
	EMUX1	O1	St/B	External Analog MUX Control Output 1 (ADC1)
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	U0C0_DOUT	O3	St/B	USIC0 Channel 0 Shift Data Output
	CCU62_CCP OS1A	I	St/B	CCU62 Position Input 1
	TMS_C	IH	St/B	JTAG Test Mode Selection Input If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin low when nothing is driving it.
	U0C1_DX0F	I	St/B	USIC0 Channel 1 Shift Data Input

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
10	P8.2	O0 / I	St/B	Bit 2 of Port 8, General Purpose Input/Output
	CCU60_CC62	O1	St/B	CCU60 Channel 2 Output
	TxDC1	O2	St/B	CAN Node 1 Transmit Data Output
	U1C1_DOUT	O3	St/B	USIC1 Channel 1 Shift Data output
	CCU60_CC62INB	I	St/B	CCU60 Channel 2 Input
11	P7.1	O0 / I	St/B	Bit 1 of Port 7, General Purpose Input/Output
	EXTCLK	O1	St/B	Programmable Clock Signal Output
	TXDC4	O2	St/B	CAN Node 4 Transmit Data Output
	U4C1_DOUT	O3	St/B	USIC4 Channel 1 Shift Data Output
	U4C1_DX0D	I	St/B	USIC4 Channel 1 Shift Data Input
	CCU62_CTRAPA	I	St/B	CCU62 Emergency Trap Input
	BRKIN_C	I	St/B	OCDS Break Signal Input
12	P7.4	O0 / I	St/B	Bit 4 of Port 7, General Purpose Input/Output
	EMUX2	O1	St/B	External Analog MUX Control Output 2 (ADC1)
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	U0C1_SCLKOUT	O3	St/B	USIC0 Channel 1 Shift Clock Output
	CCU62_CCP OS2A	I	St/B	CCU62 Position Input 2
	TCK_C	IH	St/B	DAP0/JTAG Clock Input If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it. If DAP pos. 2 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	U0C0_DX0D	I	St/B	USIC0 Channel 0 Shift Data Input
	U0C1_DX1E	I	St/B	USIC0 Channel 1 Shift Clock Input

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
13	P8.1	O0 / I	St/B	Bit 1 of Port 8, General Purpose Input/Output
	CCU60_CC61	O1	St/B	CCU60 Channel 1 Output
	U4C1_MCLKOUT	O3	St/B	USIC4 Channel 1 Master Clock Output
	CCU60_CC61INB	I	St/B	CCU60 Channel 1 Input
	RxDC1F	I	St/B	CAN Node 1 Receive Data Input
16	P6.0	O0 / I	DA/A	Bit 0 of Port 6, General Purpose Input/Output
	EMUX0	O1	DA/A	External Analog MUX Control Output 0 (ADC0)
	TxDC2	O2	DA/A	CAN Node 2 Transmit Data Output
	BRKOUT	O3	DA/A	OCDS Break Signal Output
	ADCx_REQG TyG	I	DA/A	External Request Gate Input for ADC0/1
	U1C1_DX0E	I	DA/A	USIC1 Channel 1 Shift Data Input
	ADC1_CH15	I	DA/A	Analog Input Channel 15 for ADC1
17	P6.1	O0 / I	DA/A	Bit 1 of Port 6, General Purpose Input/Output
	EMUX1	O1	DA/A	External Analog MUX Control Output 1 (ADC0)
	T3OUT	O2	DA/A	GPT12E Timer T3 Toggle Latch Output
	U1C1_DOUT	O3	DA/A	USIC1 Channel 1 Shift Data Output
	ADCx_REQT RyE	I	DA/A	External Request Trigger Input for ADC0/1
	RxDC2E	I	DA/A	CAN Node 2 Receive Data Input
	ESR1_6	I	DA/A	ESR1 Trigger Input 6
	ADC1_CH14	I	DA/A	Analog Input Channel 14 for ADC1
18	P6.2	O0 / I	DA/A	Bit 2 of Port 6, General Purpose Input/Output
	EMUX2	O1	DA/A	External Analog MUX Control Output 2 (ADC0)
	T6OUT	O2	DA/A	GPT12E Timer T6 Toggle Latch Output
	U1C1_SCLKOUT	O3	DA/A	USIC1 Channel 1 Shift Clock Output
	U1C1_DX1C	I	DA/A	USIC1 Channel 1 Shift Clock Input
	ADC1_CH13	I	DA/A	Analog Input Channel 13 for ADC1

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
19	P6.3	O0 / I	DA/A	Bit 3 of Port 6, General Purpose Input/Output
	T3OUT	O2	DA/A	GPT12E Timer T3 Toggle Latch Output
	U1C1_SELO0	O3	DA/A	USIC1 Channel 1 Select/Control 0 Output
	U1C1_DX2D	I	DA/A	USIC1 Channel 1 Shift Control Input
	ADCx_REQTRyF	I	DA/A	External Request Trigger Input for ADC0/1
	ADC1_CH12	I	DA/A	Analog Input Channel 12 for ADC1
21	P15.0	I	In/A	Bit 0 of Port 15, General Purpose Input
	ADC1_CH0	I	In/A	Analog Input Channel 0 for ADC1
22	P15.1	I	In/A	Bit 1 of Port 15, General Purpose Input
	ADC1_CH1	I	In/A	Analog Input Channel 1 for ADC1
23	P15.2	I	In/A	Bit 2 of Port 15, General Purpose Input
	ADC1_CH2	I	In/A	Analog Input Channel 2 for ADC1
	T5INA	I	In/A	GPT12E Timer T5 Count/Gate Input
24	P15.3	I	In/A	Bit 3 of Port 15, General Purpose Input
	ADC1_CH3	I	In/A	Analog Input Channel 3 for ADC1
	T5EUDA	I	In/A	GPT12E Timer T5 External Up/Down Control Input
25	P15.4	I	In/A	Bit 4 of Port 15, General Purpose Input
	ADC1_CH4	I	In/A	Analog Input Channel 4 for ADC1
	T6INA	I	In/A	GPT12E Timer T6 Count/Gate Input
26	P15.5	I	In/A	Bit 5 of Port 15, General Purpose Input
	ADC1_CH5	I	In/A	Analog Input Channel 5 for ADC1
	T6EUDA	I	In/A	GPT12E Timer T6 External Up/Down Control Input
27	P15.6	I	In/A	Bit 6 of Port 15, General Purpose Input
	ADC1_CH6	I	In/A	Analog Input Channel 6 for ADC1
28	P15.7	I	In/A	Bit 7 of Port 15, General Purpose Input
	ADC1_CH7	I	In/A	Analog Input Channel 7 for ADC1
29	V _{AREF1}	-	PS/A	Reference Voltage for A/D Converter ADC1

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
30	V _{AREF0}	-	PS/A	Reference Voltage for A/D Converter ADC0
31	V _{AGND}	-	PS/A	Reference Ground for A/D Converters ADC0/1
32	P5.0	I	In/A	Bit 0 of Port 5, General Purpose Input
	ADC0_CH0	I	In/A	Analog Input Channel 0 for ADC0
33	P5.1	I	In/A	Bit 1 of Port 5, General Purpose Input
	ADC0_CH1	I	In/A	Analog Input Channel 1 for ADC0
34	P5.2	I	In/A	Bit 2 of Port 5, General Purpose Input
	ADC0_CH2	I	In/A	Analog Input Channel 2 for ADC0
	TDI_A	I	In/A	JTAG Test Data Input
35	P5.3	I	In/A	Bit 3 of Port 5, General Purpose Input
	ADC0_CH3	I	In/A	Analog Input Channel 3 for ADC0
	T3INA	I	In/A	GPT12E Timer T3 Count/Gate Input
39	P5.4	I	In/A	Bit 4 of Port 5, General Purpose Input
	ADC0_CH4	I	In/A	Analog Input Channel 4 for ADC0
	CCU63_T12 HRB	I	In/A	External Run Control Input for T12 of CCU63
	T3EUDA	I	In/A	GPT12E Timer T3 External Up/Down Control Input
	TMS_A	I	In/A	JTAG Test Mode Selection Input
40	P5.5	I	In/A	Bit 5 of Port 5, General Purpose Input
	ADC0_CH5	I	In/A	Analog Input Channel 5 for ADC0
	CCU60_T12 HRB	I	In/A	External Run Control Input for T12 of CCU60
41	P5.6	I	In/A	Bit 6 of Port 5, General Purpose Input
	ADC0_CH6	I	In/A	Analog Input Channel 6 for ADC0
42	P5.7	I	In/A	Bit 7 of Port 5, General Purpose Input
	ADC0_CH7	I	In/A	Analog Input Channel 7 for ADC0

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
43	P5.8	I	In/A	Bit 8 of Port 5, General Purpose Input
	ADC0_CH8	I	In/A	Analog Input Channel 8 for ADC0
	ADC1_CH8	I	In/A	Analog Input Channel 8 for ADC1
	CCU6x_T12H RC	I	In/A	External Run Control Input for T12 of CCU60/1/2/3
	CCU6x_T13H RC	I	In/A	External Run Control Input for T13 of CCU60/1/2/3
	U2C0_DX0F	I	In/A	USIC2 Channel 0 Shift Data Input
44	P5.9	I	In/A	Bit 9 of Port 5, General Purpose Input
	ADC0_CH9	I	In/A	Analog Input Channel 9 for ADC0
	ADC1_CH9	I	In/A	Analog Input Channel 9 for ADC1
	CC2_T7IN	I	In/A	CAPCOM2 Timer T7 Count Input
45	P5.10	I	In/A	Bit 10 of Port 5, General Purpose Input
	ADC0_CH10	I	In/A	Analog Input Channel 10 for ADC0
	ADC1_CH10	I	In/A	Analog Input Channel 10 for ADC1
	BRKIN_A	I	In/A	OCDS Break Signal Input
	U2C1_DX0F	I	In/A	USIC2 Channel 1 Shift Data Input
	CCU61_T13 HRA	I	In/A	External Run Control Input for T13 of CCU61
46	P5.11	I	In/A	Bit 11 of Port 5, General Purpose Input
	ADC0_CH11	I	In/A	Analog Input Channel 11 for ADC0
	ADC1_CH11	I	In/A	Analog Input Channel 11 for ADC1
47	P5.12	I	In/A	Bit 12 of Port 5, General Purpose Input
48	P5.13	I	In/A	Bit 13 of Port 5, General Purpose Input
	ADC0_CH13	I	In/A	Analog Input Channel 13 for ADC0
	ERU_0B1	I	St/B	External Request Unit Channel 0 Input B1
	CCU63_T13 HRF	I	In/A	External Run Control Input for T13 of CCU63
49	P5.14	I	In/A	Bit 14 of Port 5, General Purpose Input

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
50	P5.15	I	In/A	Bit 15 of Port 5, General Purpose Input
	ADC0_CH15	I	In/A	Analog Input Channel 15 for ADC0
	RxDC2F	I	In/A	CAN Node 2 Receive Data Input
51	P2.12	O0 / I	St/B	Bit 12 of Port 2, General Purpose Input/Output
	U0C0_SELO 4	O1	St/B	USIC0 Channel 0 Select/Control 4 Output
	U0C1_SELO 3	O2	St/B	USIC0 Channel 1 Select/Control 3 Output
	TXDC2	O3	St/B	CAN Node 2 Transmit Data Output
	READY	IH	St/B	External Bus Interface READY Input
	U4C0_DX0A	I	St/B	USIC4 Channel 0 Shift Data Input
52	P2.11	O0 / I	St/B	Bit 11 of Port 2, General Purpose Input/Output
	U0C0_SELO 2	O1	St/B	USIC0 Channel 0 Select/Control 2 Output
	U0C1_SELO 2	O2	St/B	USIC0 Channel 1 Select/Control 2 Output
	U3C1_DOUT	O3	St/B	USIC3 Channel 1 Shift Data Output
	BHE/WRH	OH	St/B	External Bus Interf. High-Byte Control Output Can operate either as Byte High Enable (BHE) or as Write strobe for High Byte (WRH).
53	P11.5	O0 / I	St/B	Bit 5 of Port 11, General Purpose Input/Output
	CCU61_CC6 0	O1	St/B	CCU61 Channel 0 Output
	CCU61_COU T63	O2	St/B	CCU61 Channel 3 Output
	U3C1_SELO 1	O3	St/B	USIC3 Channel 1 Select/Control 1 Output
	CCU61_CC6 0INB	I	St/B	CCU61 Channel 0 Input
	U3C1_DX2B	I	St/B	USIC3 Channel 1 Shift Control Input
	U4C0_DX2A	I	St/B	USIC4 Channel 0 Shift Control Input

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
55	P2.0	O0 / I	St/B	Bit 0 of Port 2, General Purpose Input/Output
	TxDC5	O1	St/B	CAN Node 5 Transmit Data Output
	CCU63_CC60	O2	St/B	CCU63 Channel 0 Output
	AD13	OH / IH	St/B	External Bus Interface Address/Data Line 13
	RxDC0C	I	St/B	CAN Node 0 Receive Data Input
	CCU63_CC60INB	I	St/B	CCU63 Channel 0 Input
	T5INB	I	St/B	GPT12E Timer T5 Count/Gate Input
56	P2.1	O0 / I	St/B	Bit 1 of Port 2, General Purpose Input/Output
	TxDC0	O1	St/B	CAN Node 0 Transmit Data Output
	CCU63_CC61	O2	St/B	CCU63 Channel 1 Output
	AD14	OH / IH	St/B	External Bus Interface Address/Data Line 14
	RxDC5C	I	St/B	CAN Node 5 Receive Data Input
	CCU63_CC61INB	I	St/B	CCU63 Channel 1 Input
	T5EUDB	I	St/B	GPT12E Timer T5 External Up/Down Control Input
	ESR1_5	I	St/B	ESR1 Trigger Input 5
	ERU_0A0	I	St/B	External Request Unit Channel 0 Input A0
57	P11.4	O0 / I	St/B	Bit 4 of Port 11, General Purpose Input/Output
	CCU61_CC62	O1	St/B	CCU61 Channel 2 Output
	U3C1_DOUT	O2	St/B	USIC3 Channel 1 Shift Data Output
	RxDC5B	I	St/B	CAN Node 5 Receive Data Input
	CCU61_CC62INB	I	St/B	CCU61 Channel 2 Input
	U3C1_DX0B	I	St/B	USIC3 Channel 1 Shift Data Input

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
58	P2.2	O0 / I	St/B	Bit 2 of Port 2, General Purpose Input/Output
	TxDC1	O1	St/B	CAN Node 1 Transmit Data Output
	CCU63_CC6 2	O2	St/B	CCU63 Channel 2 Output
	AD15	OH / IH	St/B	External Bus Interface Address/Data Line 15
	CCU63_CC6 2INB	I	St/B	CCU63 Channel 2 Input
	ESR2_5	I	St/B	ESR2 Trigger Input 5
	ERU_1A0	I	St/B	External Request Unit Channel 1 Input A0
59	P11.3	O0 / I	St/B	Bit 3 of Port 11, General Purpose Input/Output
	CCU61_COU T63	O1	St/B	CCU61 Channel 3 Output
	CCU61_COU T62	O2	St/B	CCU61 Channel 2 Output
	TxDC5	O3	St/B	CAN Node 5 Transmit Data Input
	CCU61_T13 HRF	I	St/B	External Run Control Input for T13 of CCU61
	U4C0_DX1A	I	St/B	USIC4 Channel 0 Shift Clock Input
60	P4.0	O0 / I	St/B	Bit 0 of Port 4, General Purpose Input/Output
	CC2_CC24	O3 / I	St/B	CAPCOM2 CC24IO Capture Inp./ Compare Out.
	CS0	OH	St/B	External Bus Interface Chip Select 0 Output
61	P2.3	O0 / I	St/B	Bit 3 of Port 2, General Purpose Input/Output
	U0C0_DOUT	O1	St/B	USIC0 Channel 0 Shift Data Output
	CCU63_COU T63	O2	St/B	CCU63 Channel 3 Output
	CC2_CC16	O3 / I	St/B	CAPCOM2 CC16IO Capture Inp./ Compare Out.
	A16	OH	St/B	External Bus Interface Address Line 16
	ESR2_0	I	St/B	ESR2 Trigger Input 0
	U0C0_DX0E	I	St/B	USIC0 Channel 0 Shift Data Input
	U0C1_DX0D	I	St/B	USIC0 Channel 1 Shift Data Input
	RxDC0A	I	St/B	CAN Node 0 Receive Data Input

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
62	P11.2	O0 / I	St/B	Bit 2 of Port 11, General Purpose Input/Output
	CCU61_CC61	O1	St/B	CCU61 Channel 1 Output
	U3C1_DOUT	O2	St/B	USIC3 Channel 1 Shift Data Output
	U4C0_SELO1	O3	St/B	USIC4 Channel 0 Select/Control 1 Output
	CCU63_CCP OS2A	I	St/B	CCU63 Position Input 2
	CCU61_CC61INB	I	St/B	CCU61 Channel 1 Input
63	P4.1	O0 / I	St/B	Bit 1 of Port 4, General Purpose Input/Output
	U3C0_SELO3	O1	St/B	USIC3 Channel Select/Control 3 Output
	TxDC2	O2	St/B	CAN Node 2 Transmit Data Output
	CC2_CC25	O3 / I	St/B	CAPCOM2 CC25IO Capture Inp./ Compare Out.
	CS1	OH	St/B	External Bus Interface Chip Select 1 Output
	CCU62_CCP OS0B	I	St/B	CCU62 Position Input 0
	T4EUDB	I	St/B	GPT12E Timer T4 External Up/Down Control Input
64	ESR1_8	I	St/B	ESR1 Trigger Input 8
	P2.4	O0 / I	St/B	Bit 4 of Port 2, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	TxDC0	O2	St/B	CAN Node 0 Transmit Data Output
	CC2_CC17	O3 / I	St/B	CAPCOM2 CC17IO Capture Inp./ Compare Out.
	A17	OH	St/B	External Bus Interface Address Line 17
	ESR1_0	I	St/B	ESR1 Trigger Input 0
	U0C0_DX0F	I	St/B	USIC0 Channel 0 Shift Data Input
	RxDC1A	I	St/B	CAN Node 1 Receive Data Input

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
65	P11.1	O0 / I	St/B	Bit 1 of Port 11, General Purpose Input/Output
	CCU61_COU T61	O1	St/B	CCU61 Channel 1 Output
	TxDC0	O2	St/B	CAN Node 0 Transmit Data Output
	U3C1_SELO 0	O3	St/B	USIC3 Channel 1 Select/Control 0 Output
	CCU63_CCP OS1A	I	St/B	CCU63 Position Input 1
	CCU61_CTR APD	I	St/B	CCU61 Emergency Trap Input
	U3C1_DX2A	I	St/B	USIC3 Channel 1 Shift Control Input
66	P11.0	O0 / I	St/B	Bit 0 of Port 11, General Purpose Input/Output
	CCU61_COU T60	O1	St/B	CCU61 Channel 0 Output
	U3C1_SCLK OUT	O2	St/B	USIC3 Channel 1 Shift Clock Output
	U4C0_SCLK OUT	O3	St/B	USIC4 Channel 0 Shift Clock Output
	U4C0_DX1D	I	St/B	USIC4 Channel 0 Shift Clock Input
	CCU63_CCP OS0A	I	St/B	CCU63 Position Input 0
	RxDC0F	I	St/B	CAN Node 0 Receive Data Input
	U3C1_DX1A	I	St/B	USIC3 Channel 1 Shift Clock Input
	ESR1_7	I	St/B	ESR1 Trigger Input 7
67	P2.5	O0 / I	St/B	Bit 5 of Port 2, General Purpose Input/Output
	U0C0_SCLK OUT	O1	St/B	USIC0 Channel 0 Shift Clock Output
	TxDC0	O2	St/B	CAN Node 0 Transmit Data Output
	CC2_CC18	O3 / I	St/B	CAPCOM2 CC18IO Capture Inp./ Compare Out.
	A18	OH	St/B	External Bus Interface Address Line 18
	U0C0_DX1D	I	St/B	USIC0 Channel 0 Shift Clock Input
	ESR1_10	I	St/B	ESR1 Trigger Input 10
	U3C1_DX0D	I	St/B	USIC3 Channel 1 Shift Data Input

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
68	P4.2	O0 / I	St/B	Bit 2 of Port 4, General Purpose Input/Output
	U3C0_SCLK OUT	O1	St/B	USIC3 Channel 0 Shift Clock Output
	TxDC2	O2	St/B	CAN Node 2 Transmit Data Output
	CC2_CC26	O3 / I	St/B	CAPCOM2 CC26IO Capture Inp./ Compare Out.
	CS2	OH	St/B	External Bus Interface Chip Select 2 Output
	T2INA	I	St/B	GPT12E Timer T2 Count/Gate Input
	CCU62_CCP OS1B	I	St/B	CCU62 Position Input 1
	U3C0_DX1B	I	St/B	USIC3 Channel 0 Shift Clock Input
69	P2.6	O0 / I	St/B	Bit 6 of Port 2, General Purpose Input/Output
	U0C0_SELO 0	O1	St/B	USIC0 Channel 0 Select/Control 0 Output
	U0C1_SELO 1	O2	St/B	USIC0 Channel 1 Select/Control 1 Output
	CC2_CC19	O3 / I	St/B	CAPCOM2 CC19IO Capture Inp./ Compare Out.
	A19	OH	St/B	External Bus Interface Address Line 19
	U0C0_DX2D	I	St/B	USIC0 Channel 0 Shift Control Input
	RxDC0D	I	St/B	CAN Node 0 Receive Data Input
	ESR2_6	I	St/B	ESR2 Trigger Input 6
70	P4.4	O0 / I	St/B	Bit 4 of Port 4, General Purpose Input/Output
	U3C0_SELO 2	O1	St/B	USIC3 Channel 0 Select/Control 2 Output
	CC2_CC28	O3 / I	St/B	CAPCOM2 CC28IO Capture Inp./ Compare Out.
	CS4	OH	St/B	External Bus Interface Chip Select 4 Output
	CLKIN2	I	St/B	Clock Signal Input 2
	U3C0_DX2C	I	St/B	USIC3 Channel 0 Shift Control Input

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
71	P4.3	O0 / I	St/B	Bit 3 of Port 4, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	CC2_CC27	O3 / I	St/B	CAPCOM2 CC27IO Capture Inp./ Compare Out.
	CS3	OH	St/B	External Bus Interface Chip Select 3 Output
	RxDC2A	I	St/B	CAN Node 2 Receive Data Input
	T2EUDA	I	St/B	GPT12E Timer T2 External Up/Down Control Input
	CCU62_CCP OS2B	I	St/B	CCU62 Position Input 2
75	P0.0	O0 / I	St/B	Bit 0 of Port 0, General Purpose Input/Output
	U1C0_DOUT	O1	St/B	USIC1 Channel 0 Shift Data Output
	CCU61_CC6 0	O3	St/B	CCU61 Channel 0 IOutput
	A0	OH	St/B	External Bus Interface Address Line 0
	U1C0_DX0A	I	St/B	USIC1 Channel 0 Shift Data Input
	CCU61_CC6 0INA	I	St/B	CCU61 Channel 0 Input
	ESR1_11	I	St/B	ESR1 Trigger Input 11
76	P4.5	O0 / I	St/B	Bit 5 of Port 4, General Purpose Input/Output
	U3C0_DOUT	O1	St/B	USIC3 Channel 0 Shift Data Output
	CC2_CC29	O3 / I	St/B	CAPCOM2 CC29IO Capture Inp./Compare Out.
	CCU61_CCP OS0A	I	St/B	CCU61 Position Input 0
	U3C0_DX0B	I	St/B	USIC3 Channel 0 Shift Data Input
	ESR2_10	I	St/B	ESR2 Trigger Input 10
77	P4.6	O0 / I	St/B	Bit 6 of Port 4, General Purpose Input/Output
	U3C0_DOUT	O1	St/B	USIC3 Channel 0 Shift Data Output
	CC2_CC30	O3 / I	St/B	CAPCOM2 CC30IO Capture Inp./ Compare Out.
	T4INA	I	St/B	GPT12E Timer T4 Count/Gate Input
	CCU61_CCP OS1A	I	St/B	CCU61 Position Input 1

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
78	P2.7	O0 / I	St/B	Bit 7 of Port 2, General Purpose Input/Output
	U0C1_SELO0	O1	St/B	USIC0 Channel 1 Select/Control 0 Output
	U0C0_SELO1	O2	St/B	USIC0 Channel 0 Select/Control 1 Output
	CC2_CC20	O3 / I	St/B	CAPCOM2 CC20IO Capture Inp./ Compare Out.
	A20	OH	St/B	External Bus Interface Address Line 20
	U0C1_DX2C	I	St/B	USIC0 Channel 1 Shift Control Input
	RxDC1C	I	St/B	CAN Node 1 Receive Data Input
	ESR2_7	I	St/B	ESR2 Trigger Input 7
	U4C0_DX0D	I	St/B	USIC4 Channel 0 Shift Data Input
79	P0.1	O0 / I	St/B	Bit 1 of Port 0, General Purpose Input/Output
	U1C0_DOUT	O1	St/B	USIC1 Channel 0 Shift Data Output
	TxDC0	O2	St/B	CAN Node 0 Transmit Data Output
	CCU61_CC61	O3	St/B	CCU61 Channel 1 Output
	A1	OH	St/B	External Bus Interface Address Line 1
	U1C0_DX0B	I	St/B	USIC1 Channel 0 Shift Data Input
	CCU61_CC61INA	I	St/B	CCU61 Channel 1 Input
	U1C0_DX1A	I	St/B	USIC1 Channel 0 Shift Clock Input
80	P2.8	O0 / I	DP/B	Bit 8 of Port 2, General Purpose Input/Output
	U0C1_SCLKOUT	O1	DP/B	USIC0 Channel 1 Shift Clock Output
	EXTCLK	O2	DP/B	Programmable Clock Signal Output¹⁾
	CC2_CC21	O3 / I	DP/B	CAPCOM2 CC21IO Capture Inp./ Compare Out.
	A21	OH	DP/B	External Bus Interface Address Line 21
	U0C1_DX1D	I	DP/B	USIC0 Channel 1 Shift Clock Input

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
81	P4.7	O0 / I	St/B	Bit 7 of Port 4, General Purpose Input/Output
	CC2_CC31	O3 / I	St/B	CAPCOM2 CC31IO Capture Inp./ Compare Out.
	T4EUDA	I	St/B	GPT12E Timer T4 External Up/Down Control Input
	CCU61_CCP OS2A	I	St/B	CCU61 Position Input 2
82	P2.9	O0 / I	St/B	Bit 9 of Port 2, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	TxDC1	O2	St/B	CAN Node 1 Transmit Data Output
	CC2_CC22	O3 / I	St/B	CAPCOM2 CC22IO Capture Inp./ Compare Out.
	A22	OH	St/B	External Bus Interface Address Line 22
	CLKIN1	I	St/B	Clock Signal Input 1
	TCK_A	IH	St/B	DAP0/JTAG Clock Input If JTAG pos. A is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it. If DAP pos. 0 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
83	P0.2	O0 / I	St/B	Bit 2 of Port 0, General Purpose Input/Output
	U1C0_SCLK OUT	O1	St/B	USIC1 Channel 0 Shift Clock Output
	TxDC0	O2	St/B	CAN Node 0 Transmit Data Output
	CCU61_CC6 2	O3	St/B	CCU61 Channel 2 Output
	A2	OH	St/B	External Bus Interface Address Line 2
	U1C0_DX1B	I	St/B	USIC1 Channel 0 Shift Clock Input
	CCU61_CC6 2INA	I	St/B	CCU61 Channel 2 Input

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
84	P10.0	O0 / I	St/B	Bit 0 of Port 10, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	CCU60_CC60	O2	St/B	CCU60 Channel 0 Output
	AD0	OH / IH	St/B	External Bus Interface Address/Data Line 0
	CCU60_CC60INA	I	St/B	CCU60 Channel 0 Input
	ESR1_2	I	St/B	ESR1 Trigger Input 2
	U0C0_DX0A	I	St/B	USIC0 Channel 0 Shift Data Input
	U0C1_DX0A	I	St/B	USIC0 Channel 1 Shift Data Input
85	P3.0	O0 / I	St/B	Bit 0 of Port 3, General Purpose Input/Output
	U2C0_DOUT	O1	St/B	USIC2 Channel 0 Shift Data Output
	ESR1_1	I	St/B	ESR1 Trigger Input 1
	U2C0_DX0A	I	St/B	USIC2 Channel 0 Shift Data Input
	RxDC3B	I	St/B	CAN Node 3 Receive Data Input
	U2C0_DX1A	I	St/B	USIC2 Channel 0 Shift Clock Input
86	P10.1	O0 / I	St/B	Bit 1 of Port 10, General Purpose Input/Output
	U0C0_DOUT	O1	St/B	USIC0 Channel 0 Shift Data Output
	CCU60_CC61	O2	St/B	CCU60 Channel 1 Output
	AD1	OH / IH	St/B	External Bus Interface Address/Data Line 1
	CCU60_CC61INA	I	St/B	CCU60 Channel 1 Input
	U0C0_DX1A	I	St/B	USIC0 Channel 0 Shift Clock Input
	U0C0_DX0B	I	St/B	USIC0 Channel 0 Shift Data Input

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
87	P0.3	O0 / I	St/B	Bit 3 of Port 0, General Purpose Input/Output
	U1C0_SELO0	O1	St/B	USIC1 Channel 0 Select/Control 0 Output
	U1C1_SELO1	O2	St/B	USIC1 Channel 1 Select/Control 1 Output
	CCU61_COUT60	O3	St/B	CCU61 Channel 0 Output
	A3	OH	St/B	External Bus Interface Address Line 3
	U1C0_DX2A	I	St/B	USIC1 Channel 0 Shift Control Input
	RxDC0B	I	St/B	CAN Node 0 Receive Data Input
88	P3.1	O0 / I	St/B	Bit 1 of Port 3, General Purpose Input/Output
	U2C0_DOUT	O1	St/B	USIC2 Channel 0 Shift Data Output
	TxDC3	O2	St/B	CAN Node 3 Transmit Data Output
	U2C0_DX0B	I	St/B	USIC2 Channel 0 Shift Data Input
89	P10.2	O0 / I	St/B	Bit 2 of Port 10, General Purpose Input/Output
	U0C0_SCLKOUT	O1	St/B	USIC0 Channel 0 Shift Clock Output
	CCU60_CC62	O2	St/B	CCU60 Channel 2 Output
	U3C0_SELO1	O3	St/B	USIC3 Channel 0 Select/Control 1 Output
	AD2	OH / IH	St/B	External Bus Interface Address/Data Line 2
	CCU60_CC62INA	I	St/B	CCU60 Channel 2 Input
	U0C0_DX1B	I	St/B	USIC0 Channel 0 Shift Clock Input
	U3C0_DX2B	I	St/B	USIC3 Channel 0 Shift Control Input

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
90	P0.4	O0 / I	St/B	Bit 4 of Port 0, General Purpose Input/Output
	U1C1_SELO0	O1	St/B	USIC1 Channel 1 Select/Control 0 Output
	U1C0_SELO1	O2	St/B	USIC1 Channel 0 Select/Control 1 Output
	CCU61_COUT61	O3	St/B	CCU61 Channel 1 Output
	A4	OH	St/B	External Bus Interface Address Line 4
	U1C1_DX2A	I	St/B	USIC1 Channel 1 Shift Control Input
	RxDC1B	I	St/B	CAN Node 1 Receive Data Input
	ESR2_8	I	St/B	ESR2 Trigger Input 8
92	P2.13	O0 / I	St/B	Bit 13 of Port 2, General Purpose Input/Output
	U2C1_SELO2	O1	St/B	USIC2 Channel 1 Select/Control 2 Output
	CCU63_COUT60	O2	St/B	CCU63 Channel 0 Output
	U4C0_DOUT	O3	St/B	USIC4 Channel 0 Shift Data Output
	U4C0_DX0E	I	St/B	USIC4 Channel 0 Shift Data Input
	RxDC2D	I	St/B	CAN Node 2 Receive Data Input
93	P3.2	O0 / I	St/B	Bit 2 of Port 3, General Purpose Input/Output
	U2C0_SCLKOUT	O1	St/B	USIC2 Channel 0 Shift Clock Output
	TxDC3	O2	St/B	CAN Node 3 Transmit Data Output
	U2C0_DX1B	I	St/B	USIC2 Channel 0 Shift Clock Input

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
94	P2.10	O0 / I	St/B	Bit 10 of Port 2, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	U0C0_SELO3	O2	St/B	USIC0 Channel 0 Select/Control 3 Output
	CC2_CC23	O3 / I	St/B	CAPCOM2 CC23IO Capture Inp./ Compare Out.
	A23	OH	St/B	External Bus Interface Address Line 23
	U0C1_DX0E	I	St/B	USIC0 Channel 1 Shift Data Input
	CAPINA	I	St/B	GPT12E Register CAPREL Capture Input
	U3C1_DX0A	I	St/B	USIC3 Channel 1 Shift Data Input
95	P10.3	O0 / I	St/B	Bit 3 of Port 10, General Purpose Input/Output
	CCU60_COUT60	O2	St/B	CCU60 Channel 0 Output
	AD3	OH / IH	St/B	External Bus Interface Address/Data Line 3
	U0C0_DX2A	I	St/B	USIC0 Channel 0 Shift Control Input
	U0C1_DX2A	I	St/B	USIC0 Channel 1 Shift Control Input
	U3C0_DX0A	I	St/B	USIC3 Channel 0 Shift Data Input
96	P0.5	O0 / I	St/B	Bit 5 of Port 0, General Purpose Input/Output
	U1C1_SCLKOUT	O1	St/B	USIC1 Channel 1 Shift Clock Output
	U1C0_SELO2	O2	St/B	USIC1 Channel 0 Select/Control 2 Output
	CCU61_COUT62	O3	St/B	CCU61 Channel 2 Output
	A5	OH	St/B	External Bus Interface Address Line 5
	U1C1_DX1A	I	St/B	USIC1 Channel 1 Shift Clock Input
	U1C0_DX1C	I	St/B	USIC1 Channel 0 Shift Clock Input
	RXDC3E	I	St/B	CAN Node 3 Receive Data Input

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
97	P3.3	O0 / I	St/B	Bit 3 of Port 3, General Purpose Input/Output
	U2C0_SELO0	O1	St/B	USIC2 Channel 0 Select/Control 0 Output
	U2C1_SELO1	O2	St/B	USIC2 Channel 1 Select/Control 1 Output
	U4C0_SELO0	O3	St/B	USIC4 Channel 0 Select/Control 0 Output
	U2C0_DX2A	I	St/B	USIC2 Channel 0 Shift Control Input
	RxDC3A	I	St/B	CAN Node 3 Receive Data Input
98	P10.4	O0 / I	St/B	Bit 4 of Port 10, General Purpose Input/Output
	U0C0_SELO3	O1	St/B	USIC0 Channel 0 Select/Control 3 Output
	CCU60_COUT61	O2	St/B	CCU60 Channel 1 Output
	U3C0_DOUT	O3	St/B	USIC3 Channel 0 Shift Data Output
	AD4	OH / IH	St/B	External Bus Interface Address/Data Line 4
	U0C0_DX2B	I	St/B	USIC0 Channel 0 Shift Control Input
	U0C1_DX2B	I	St/B	USIC0 Channel 1 Shift Control Input
	ESR1_9	I	St/B	ESR1 Trigger Input 9
99	P3.4	O0 / I	St/B	Bit 4 of Port 3, General Purpose Input/Output
	U2C1_SELO0	O1	St/B	USIC2 Channel 1 Select/Control 0 Output
	U2C0_SELO1	O2	St/B	USIC2 Channel 0 Select/Control 1 Output
	U0C0_SELO4	O3	St/B	USIC0 Channel 0 Select/Control 4 Output
	U2C1_DX2A	I	St/B	USIC2 Channel 1 Shift Control Input
	RxDC4A	I	St/B	CAN Node 4 Receive Data Input

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
100	P10.5	O0 / I	St/B	Bit 5 of Port 10, General Purpose Input/Output
	U0C1_SCLK OUT	O1	St/B	USIC0 Channel 1 Shift Clock Output
	CCU60_COU T62	O2	St/B	CCU60 Channel 2 Output
	U2C0_DOUT	O3	St/B	USIC2 Channel 0 Shift Data Output
	AD5	OH / IH	St/B	External Bus Interface Address/Data Line 5
	U0C1_DX1B	I	St/B	USIC0 Channel 1 Shift Clock Input
101	P3.5	O0 / I	St/B	Bit 5 of Port 3, General Purpose Input/Output
	U2C1_SCLK OUT	O1	St/B	USIC2 Channel 1 Shift Clock Output
	U2C0_SELO 2	O2	St/B	USIC2 Channel 0 Select/Control 2 Output
	U0C0_SELO 5	O3	St/B	USIC0 Channel 0 Select/Control 5 Output
	U2C1_DX1A	I	St/B	USIC2 Channel 1 Shift Clock Input
102	P0.6	O0 / I	St/B	Bit 6 of Port 0, General Purpose Input/Output
	U1C1_DOUT	O1	St/B	USIC1 Channel 1 Shift Data Output
	TxDC1	O2	St/B	CAN Node 1 Transmit Data Output
	CCU61_COU T63	O3	St/B	CCU61 Channel 3 Output
	A6	OH	St/B	External Bus Interface Address Line 6
	U1C1_DX0A	I	St/B	USIC1 Channel 1 Shift Data Input
	CCU61_CTR APA	I	St/B	CCU61 Emergency Trap Input
	U1C1_DX1B	I	St/B	USIC1 Channel 1 Shift Clock Input

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
103	P10.6	O0 / I	St/B	Bit 6 of Port 10, General Purpose Input/Output
	U0C0_DOUT	O1	St/B	USIC0 Channel 0 Shift Data Output
	TxDC4	O2	St/B	CAN Node 4 Transmit Data Output
	U1C0_SELO 0	O3	St/B	USIC1 Channel 0 Select/Control 0 Output
	AD6	OH / IH	St/B	External Bus Interface Address/Data Line 6
	U0C0_DX0C	I	St/B	USIC0 Channel 0 Shift Data Input
	U1C0_DX2D	I	St/B	USIC1 Channel 0 Shift Control Input
	CCU60_CTR APA	I	St/B	CCU60 Emergency Trap Input
104	P3.6	O0 / I	St/B	Bit 6 of Port 3, General Purpose Input/Output
	U2C1_DOUT	O1	St/B	USIC2 Channel 1 Shift Data Output
	TxDC4	O2	St/B	CAN Node 4 Transmit Data Output
	U0C0_SELO 6	O3	St/B	USIC0 Channel 0 Select/Control 6 Output
	U2C1_DX0A	I	St/B	USIC2 Channel 1 Shift Data Input
	U2C1_DX1B	I	St/B	USIC2 Channel 1 Shift Clock Input
105	P10.7	O0 / I	St/B	Bit 7 of Port 10, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	CCU60_COU T63	O2	St/B	CCU60 Channel 3 Output
	CCU63_COU T61	O3	St/B	CCU63 Channel 1 Output
	AD7	OH / IH	St/B	External Bus Interface Address/Data Line 7
	U0C1_DX0B	I	St/B	USIC0 Channel 1 Shift Data Input
	CCU60_CCP OS0A	I	St/B	CCU60 Position Input 0
	RxDC4C	I	St/B	CAN Node 4 Receive Data Input
	T4INB	I	St/B	GPT12E Timer T4 Count/Gate Input

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
106	P0.7	O0 / I	St/B	Bit 7 of Port 0, General Purpose Input/Output
	U1C1_DOUT	O1	St/B	USIC1 Channel 1 Shift Data Output
	U1C0_SELO 3	O2	St/B	USIC1 Channel 0 Select/Control 3 Output
	TxDC3	O3	St/B	CAN Node 3 Transmit Data Output
	A7	OH	St/B	External Bus Interface Address Line 7
	U1C1_DX0B	I	St/B	USIC1 Channel 1 Shift Data Input
	CCU61_CTR APB	I	St/B	CCU61 Emergency Trap Input
107	P3.7	O0 / I	St/B	Bit 7 of Port 3, General Purpose Input/Output
	U2C1_DOUT	O1	St/B	USIC2 Channel 1 Shift Data Output
	U2C0_SELO 3	O2	St/B	USIC2 Channel 0 Select/Control 3 Output
	U0C0_SELO 7	O3	St/B	USIC0 Channel 0 Select/Control 7 Output
	U2C1_DX0B	I	St/B	USIC2 Channel 1 Shift Data Input
111	P1.0	O0 / I	St/B	Bit 0 of Port 1, General Purpose Input/Output
	U1C0_MCLK OUT	O1	St/B	USIC1 Channel 0 Master Clock Output
	U1C0_SELO 4	O2	St/B	USIC1 Channel 0 Select/Control 4 Output
	A8	OH	St/B	External Bus Interface Address Line 8
	ESR1_3	I	St/B	ESR1 Trigger Input 3
	ERU_0B0	I	St/B	External Request Unit Channel 0 Input B0
	CCU62_CTR APB	I	St/B	CCU62 Emergency Trap Input
	T6INB	I	St/B	GPT12E Timer T6 Count/Gate Input

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
112	P9.0	O0 / I	St/B	Bit 0 of Port 9, General Purpose Input/Output
	CCU63_CC60	O1	St/B	CCU63 Channel 0 Output
	CCU63_CC60INA	I	St/B	CCU63 Channel 0 Input
	T6EUDB	I	St/B	GPT12E Timer T6 External Up/Down Control Input
113	P10.8	O0 / I	St/B	Bit 8 of Port 10, General Purpose Input/Output
	U0C0_MCLKOUT	O1	St/B	USIC0 Channel 0 Master Clock Output
	U0C1_SELO0	O2	St/B	USIC0 Channel 1 Select/Control 0 Output
	U2C1_DOUT	O3	St/B	USIC2 Channel 1 Shift Data Output
	AD8	OH / IH	St/B	External Bus Interface Address/Data Line 8
	CCU60_CCP0S1A	I	St/B	CCU60 Position Input 1
	U0C0_DX1C	I	St/B	USIC0 Channel 0 Shift Clock Input
	BRKIN_B	I	St/B	OCDS Break Signal Input
	T3EUDB	I	St/B	GPT12E Timer T3 External Up/Down Control Input
	ESR2_11	I	St/B	ESR2 Trigger Input 11
114	P9.1	O0 / I	DP/B	Bit 1 of Port 9, General Purpose Input/Output
	CCU63_CC61	O1	DP/B	CCU63 Channel 1 Output
	CCU63_CC61INA	I	DP/B	CCU63 Channel 1 Input

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
115	P10.9	O0 / I	DP/B	Bit 9 of Port 10, General Purpose Input/Output
	U0C0_SELO 4	O1	DP/B	USIC0 Channel 0 Select/Control 4 Output
	U0C1_MCLK OUT	O2	DP/B	USIC0 Channel 1 Master Clock Output
	AD9	OH / IH	DP/B	External Bus Interface Address/Data Line 9
	CCU60_CCP OS2A	I	DP/B	CCU60 Position Input 2
	TCK_B	IH	DP/B	DAP0/JTAG Clock Input If JTAG pos. B is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it. If DAP pos. 1 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	T3INB	I	DP/B	GPT12E Timer T3 Count/Gate Input
116	P1.1	O0 / I	St/B	Bit 1 of Port 1, General Purpose Input/Output
	CCU62_COU T62	O1	St/B	CCU62 Channel 2 Output
	U1C0_SELO 5	O2	St/B	USIC1 Channel 0 Select/Control 5 Output
	U2C1_DOUT	O3	St/B	USIC2 Channel 1 Shift Data Output
	A9	OH	St/B	External Bus Interface Address Line 9
	ESR2_3	I	St/B	ESR2 Trigger Input 3
	ERU_1B0	I	St/B	External Request Unit Channel 1 Input B0
	U2C1_DX0C	I	St/B	USIC2 Channel 1 Shift Data Input

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
117	P10.10	O0 / I	St/B	Bit 10 of Port 10, General Purpose Input/Output
	U0C0_SELO0	O1	St/B	USIC0 Channel 0 Select/Control 0 Output
	CCU60_COUT63	O2	St/B	CCU60 Channel 3 Output
	AD10	OH / IH	St/B	External Bus Interface Address/Data Line 10
	U0C0_DX2C	I	St/B	USIC0 Channel 0 Shift Control Input
	U0C1_DX1A	I	St/B	USIC0 Channel 1 Shift Clock Input
	TDI_B	IH	St/B	JTAG Test Data Input If JTAG pos. B is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it.
118	P10.11	O0 / I	St/B	Bit 11 of Port 10, General Purpose Input/Output
	U1C0_SCLKOUT	O1	St/B	USIC1 Channel 0 Shift Clock Output
	BRKOUT	O2	St/B	OCDS Break Signal Output
	U3C0_SELO0	O3	St/B	USIC3 Channel 0 Select/Control 0 Output
	AD11	OH / IH	St/B	External Bus Interface Address/Data Line 11
	U1C0_DX1D	I	St/B	USIC1 Channel 0 Shift Clock Input
	RxDC2B	I	St/B	CAN Node 2 Receive Data Input
	TMS_B	IH	St/B	JTAG Test Mode Selection Input If JTAG pos. B is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it.
	U3C0_DX2A	I	St/B	USIC3 Channel 0 Shift Control Input
119	P9.2	O0 / I	St/B	Bit 2 of Port 9, General Purpose Input/Output
	CCU63_CC62	O1	St/B	CCU63 Channel 2 Output
	CCU63_CC62INA	I	St/B	CCU63 Channel 2 Input
	CAPINB	I	St/B	GPT12E Register CAPREL Capture Input

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
120	P1.2	O0 / I	St/B	Bit 2 of Port 1, General Purpose Input/Output
	CCU62_CC62	O1	St/B	CCU62 Channel 2 Output
	U1C0_SELO6	O2	St/B	USIC1 Channel 0 Select/Control 6 Output
	U2C1_SCLKOUT	O3	St/B	USIC2 Channel 1 Shift Clock Output
	A10	OH	St/B	External Bus Interface Address Line 10
	ESR1_4	I	St/B	ESR1 Trigger Input 4
	ERU_2A0	I	St/B	External Request Unit Channel 2 Input A0
	CCU61_T12HRB	I	St/B	External Run Control Input for T12 of CCU61
	CCU62_CC62INA	I	St/B	CCU62 Channel 2 Input
	U2C1_DX0D	I	St/B	USIC2 Channel 1 Shift Data Input
	U2C1_DX1C	I	St/B	USIC2 Channel 1 Shift Clock Input
121	P10.12	O0 / I	St/B	Bit 12 of Port 10, General Purpose Input/Output
	U1C0_DOUT	O1	St/B	USIC1 Channel 0 Shift Data Output
	TxDC2	O2	St/B	CAN Node 2 Transmit Data Output
	CCU63_COUT62	O3	St/B	CCU63 Channel 2 Output
	TDO_B	OH / IH	St/B	JTAG Test Data Output / DAP1 Input/Output If DAP pos. 1 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	AD12	OH / IH	St/B	External Bus Interface Address/Data Line 12
	U1C0_DX0C	I	St/B	USIC1 Channel 0 Shift Data Input
122	U1C0_DX1E	I	St/B	USIC1 Channel 0 Shift Clock Input
	P9.3	O0 / I	St/B	Bit 3 of Port 9, General Purpose Input/Output
	CCU63_COUT60	O1	St/B	CCU63 Channel 0 Output
	BRKOUT	O2	St/B	OCDS Break Signal Output

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
123	P10.13	O0 / I	St/B	Bit 13 of Port 10, General Purpose Input/Output
	U1C0_DOUT	O1	St/B	USIC1 Channel 0 Shift Data Output
	TxDC3	O2	St/B	CAN Node 3 Transmit Data Output
	U1C0_SELO 3	O3	St/B	USIC1 Channel 0 Select/Control 3 Output
	WR/WRL	OH	St/B	External Bus Interface Write Strobe Output Active for each external write access, when $\overline{\text{WR}}$, active for ext. writes to the low byte, when $\overline{\text{WRL}}$.
	U1C0_DX0D	I	St/B	USIC1 Channel 0 Shift Data Input
124	P1.3	O0 / I	St/B	Bit 3 of Port 1, General Purpose Input/Output
	CCU62_COU T63	O1	St/B	CCU62 Channel 3 Output
	U1C0_SELO 7	O2	St/B	USIC1 Channel 0 Select/Control 7 Output
	U2C0_SELO 4	O3	St/B	USIC2 Channel 0 Select/Control 4 Output
	A11	OH	St/B	External Bus Interface Address Line 11
	ESR2_4	I	St/B	ESR2 Trigger Input 4
	ERU_3A0	I	St/B	External Request Unit Channel 3 Input A0
125	P9.4	O0 / I	St/B	Bit 4 of Port 9, General Purpose Input/Output
	CCU63_COU T61	O1	St/B	CCU63 Channel 1 Output
	U2C0_DOUT	O2	St/B	USIC2 Channel 0 Shift Data Output
	CCU62_COU T63	O3	St/B	CCU62 Channel 3 Output

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
126	P9.5	O0 / I	St/B	Bit 5 of Port 9, General Purpose Input/Output
	CCU63_COU T62	O1	St/B	CCU63 Channel 2 Output
	U2C0_DOUT	O2	St/B	USIC2 Channel 0 Shift Data Output
	CCU62_COU T62	O3	St/B	CCU62 Channel 2 Output
	U2C0_DX0E	I	St/B	USIC2 Channel 0 Shift Data Input
	CCU60_CCP OS2B	I	St/B	CCU60 Position Input 2
128	P10.14	O0 / I	St/B	Bit 14 of Port 10, General Purpose Input/Output
	U1C0_SELO 1	O1	St/B	USIC1 Channel 0 Select/Control 1 Output
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	U3C0_SCLK OUT	O3	St/B	USIC3 Channel 0 Shift Clock Output
	$\overline{\text{RD}}$	OH	St/B	External Bus Interface Read Strobe Output
	ESR2_2	I	St/B	ESR2 Trigger Input 2
	U0C1_DX0C	I	St/B	USIC0 Channel 1 Shift Data Input
	RxDC3C	I	St/B	CAN Node 3 Receive Data Input
	U3C0_DX1A	I	St/B	USIC3 Channel 0 Shift Clock Input
129	P1.4	O0 / I	St/B	Bit 4 of Port 1, General Purpose Input/Output
	CCU62_COU T61	O1	St/B	CCU62 Channel 1 Output
	U1C1_SELO 4	O2	St/B	USIC1 Channel 1 Select/Control 4 Output
	U2C0_SELO 5	O3	St/B	USIC2 Channel 0 Select/Control 5 Output
	A12	OH	St/B	External Bus Interface Address Line 12
	U2C0_DX2B	I	St/B	USIC2 Channel 0 Shift Control Input
	RxDC5A	I	St/B	CAN Node 5 Receive Data Input

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
130	P10.15	O0 / I	St/B	Bit 15 of Port 10, General Purpose Input/Output
	U1C0_SELO2	O1	St/B	USIC1 Channel 0 Select/Control 2 Output
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	U1C0_DOUT	O3	St/B	USIC1 Channel 0 Shift Data Output
	ALE	OH	St/B	External Bus Interf. Addr. Latch Enable Output
	U0C1_DX1C	I	St/B	USIC0 Channel 1 Shift Clock Input
131	P1.5	O0 / I	St/B	Bit 5 of Port 1, General Purpose Input/Output
	CCU62_COUT60	O1	St/B	CCU62 Channel 0 Output
	U1C1_SELO3	O2	St/B	USIC1 Channel 1 Select/Control 3 Output
	BRKOUT	O3	St/B	OCDS Break Signal Output
	A13	OH	St/B	External Bus Interface Address Line 13
	U2C0_DX0C	I	St/B	USIC2 Channel 0 Shift Data Input
132	P9.6	O0 / I	St/B	Bit 6 of Port 9, General Purpose Input/Output
	CCU63_COUT63	O1	St/B	CCU63 Channel 3 Output
	CCU63_COUT62	O2	St/B	CCU63 Channel 2 Output
	CCU62_COUT61	O3	St/B	CCU62 Channel 1 Output
	CCU63_CTRAPA	I	St/B	CCU63 Emergency Trap Input
	CCU60_CCP0S1B	I	St/B	CCU60 Position Input 1

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
133	P1.6	O0 / I	St/B	Bit 6 of Port 1, General Purpose Input/Output
	CCU62_CC61	O1 / I	St/B	CCU62 Channel 1 Output
	U1C1_SELO2	O2	St/B	USIC1 Channel 1 Select/Control 2 Output
	U2C0_DOUT	O3	St/B	USIC2 Channel 0 Shift Data Output
	A14	OH	St/B	External Bus Interface Address Line 14
	U2C0_DX0D	I	St/B	USIC2 Channel 0 Shift Data Input
	CCU62_CC61INA	I	St/B	CCU62 Channel 1 Input
	U4C1_DX0A	I	St/B	USIC4 Channel 1 Shift Data Input
134	P9.7	O0 / I	St/B	Bit 7 of Port 9, General Purpose Input/Output
	CCU62_COUT60	O1	St/B	CCU62 Channel 0 Output
	CCU62_COUT63	O2	St/B	CCU62 Channel 3 Output
	CCU63_CTRAPB	I	St/B	CCU63 Emergency Trap Input
	U2C0_DX1D	I	St/B	USIC2 Channel 0 Shift Clock Input
	CCU60_CCP0S0B	I	St/B	CCU60 Position Input 0
135	P1.7	O0 / I	St/B	Bit 7 of Port 1, General Purpose Input/Output
	CCU62_CC60	O1	St/B	CCU62 Channel 0 Output
	U1C1_MCLKOUT	O2	St/B	USIC1 Channel 1 Master Clock Output
	U2C0_SCLKOUT	O3	St/B	USIC2 Channel 0 Shift Clock Output
	A15	OH	St/B	External Bus Interface Address Line 15
	U2C0_DX1C	I	St/B	USIC2 Channel 0 Shift Clock Input
	CCU62_CC60INA	I	St/B	CCU62 Channel 0 Input
	RxDC4E	I	St/B	CAN Node 4 Receive Data Input

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
136	XTAL2	O	Sp/M	Crystal Oscillator Amplifier Output
137	XTAL1	I	Sp/M	Crystal Oscillator Amplifier Input To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Voltages on XTAL1 must comply to the core supply voltage V_{DDIM} .
	ESR2_9	I	St/B	ESR2 Trigger Input 9
138	PORST	I	In/B	Power On Reset Input A low level at this pin resets the XC27x8X completely. A spike filter suppresses input pulses <10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 120 ns. An internal pull-up device will hold this pin high when nothing is driving it.
139	ESR1	O0 / I	St/B	External Service Request 1 After power-up, an internal weak pull-up device holds this pin high when nothing is driving it.
	RxDC0E	I	St/B	CAN Node 0 Receive Data Input
	U1C0_DX0F	I	St/B	USIC1 Channel 0 Shift Data Input
	U1C0_DX2C	I	St/B	USIC1 Channel 0 Shift Control Input
	U1C1_DX0C	I	St/B	USIC1 Channel 1 Shift Data Input
	U1C1_DX2B	I	St/B	USIC1 Channel 1 Shift Control Input
	U2C1_DX2C	I	St/B	USIC2 Channel 1 Shift Control Input

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
140	<u>ESR2</u>	O0 / I	St/B	External Service Request 2 After power-up, an internal weak pull-up device holds this pin high when nothing is driving it.
	RxDC1E	I	St/B	CAN Node 1 Receive Data Input
	CCU60_CTR APC	I	St/B	CCU60 Emergency Trap Input
	CCU61_CTR APC	I	St/B	CCU61 Emergency Trap Input
	CCU62_CTR APC	I	St/B	CCU62 Emergency Trap Input
	CCU63_CTR APC	I	St/B	CCU63 Emergency Trap Input
	U1C1_DX0D	I	St/B	USIC1 Channel 1 Shift Data Input
	U1C1_DX2C	I	St/B	USIC1 Channel 1 Shift Control Input
	U2C1_DX0E	I	St/B	USIC2 Channel 1 Shift Data Input
	U2C1_DX2B	I	St/B	USIC2 Channel 1 Shift Control Input
141	<u>ESR0</u>	O0 / I	St/B	External Service Request 0 After power-up, ESR0 operates as open-drain bidirectional reset with a weak pull-up.
	U1C0_DX0E	I	St/B	USIC1 Channel 0 Shift Data Input
	U1C0_DX2B	I	St/B	USIC1 Channel 0 Shift Control Input
142	P8.6	O0 / I	St/B	Bit 6 of Port 8, General Purpose Input/Output
	CCU60_COU T63	O1	St/B	CCU60 Channel 3 Output
	MCHK_MAT CH	O3	St/B	Memory Checker Match Output
	CCU60_CTR APB	I	St/B	CCU60 Emergency Trap Input
	<u>BRKIN_D</u>	I	St/B	OCDS Break Signal Input
	CCU62_CTR APD	I	St/B	CCU62 Emergency Trap Input
	U4C1_DX2A	I	St/B	USIC4 Channel 1 Shift Control Input

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
143	P8.5	O0 / I	St/B	Bit 5 of Port 8, General Purpose Input/Output
	CCU60_COU T62	O1	St/B	CCU60 Channel 2 Output
	CCU62_CC6 2	O2	St/B	CCU62 Channel 2 Output
	U4C1_SCLK OUT	O3	St/B	USIC4 Channel 1 Shift Clock Output
	U4C1_DX1C	I	St/B	USIC4 Channel 1 Shift Clock Input
	TCK_D	IH	St/B	DAP0/JTAG Clock Input If JTAG pos. D is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it.
	CCU62_CC6 2INB	I	St/B	CCU62 Channel 2 Input
15	V_{DDIM}	-	PS/M	Digital Core Supply Voltage for Domain M Decouple with a ceramic capacitor, see Data Sheet for details.
14, 54, 91, 127	V_{DDI1}	-	PS/1	Digital Core Supply Voltage for Domain 1 Decouple with a ceramic capacitor, see Data Sheet for details. All V_{DDI1} pins must be connected to each other.
20	V_{DDPA}	-	PS/A	Digital Pad Supply Voltage for Domain A Connect decoupling capacitors to adjacent V_{DDP}/V_{SS} pin pairs as close as possible to the pins. <i>Note: The A/D Converters and ports P5, P6 and P15 are fed from supply voltage V_{DDPA}.</i>

Table 10-18 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
2, 36, 38, 72, 74, 108, 110, 144	V_{DDPB}	-	PS/B	Digital Pad Supply Voltage for Domain B Connect decoupling capacitors to adjacent V_{DDP}/V_{SS} pin pairs as close as possible to the pins. <i>Note: The on-chip voltage regulators and all ports except P5, P6 and P15 are fed from supply voltage V_{DDPB}.</i>
1, 37, 73, 109	V_{SS}	-	PS/--	Digital Ground All V_{SS} pins must be connected to the ground-line or ground-plane. <i>Note: Also the exposed pad is connected internally to V_{SS}. To improve the EMC behavior, it is recommended to connect the exposed pad to the board ground.</i> <i>For thermal aspects, please refer to the Data Sheet. Board layout examples are given in an application note.</i>

¹⁾ To generate the reference clock output for bus timing measurement, f_{SYS} must be selected as source for EXTCLK and P2.8 must be selected as output pin. Also the high-speed clock pad must be enabled. This configuration is referred to as reference clock output signal CLKOUT.

11 Dedicated Pins

Most of the input/output or control signals of the XC27x8X are realized as alternate functions of parallel port pins. There is, however, a number of signals that use separate pins, including the oscillator, special control signals and, of course, the power supply.

Table 11-1 summarizes the dedicated pins of the XC27x8X.

Table 11-1 XC27x8X Dedicated Pins

Pin(s)	Function
$\overline{\text{PORST}}$	Power-On Reset Input
$\overline{\text{ESR0}}$	External Service Request Input 0
$\overline{\text{ESR1}}$	External Service Request Input 1
$\overline{\text{ESR2}}$	External Service Request Input 2
XTAL1, XTAL2	Oscillator Input/Output (main oscillator)
$\overline{\text{TESTM}}$	Test Mode Enable
$\overline{\text{TRST}}$	Test-System Reset Input
$V_{\text{AREFX}}, V_{\text{AGND}}$	Reference voltages for the Analog/Digital Converter(s)
V_{DDIM}	Digital Core Supply for Domain M
V_{DDI1}	Digital Core Supply for Domain 1
V_{DDPA}	Power Supply Input for Domain A including ADCs
V_{DDPB}	Power Supply Input for Domain B
V_{SS}	Digital Ground

The Power-On Reset Input $\overline{\text{PORST}}$ allows to put the XC27x8X into reset condition either at power-up or upon external events like a hardware failure or manual reset.

The External Service Request Inputs $\overline{\text{ESR0}}$, $\overline{\text{ESR1}}$, and $\overline{\text{ESR2}}$ can be used for several system-related functions:

- trigger interrupt or trap (Class A or Class B) requests via an external signal (e.g. a power-fail signal)
- generate wake-up request signals
- generate hardware reset requests ($\overline{\text{ESR0}}$ is bidirectional by default, $\overline{\text{ESR1}}$ and $\overline{\text{ESR2}}$ can optionally output a reset signal)
- data/control input for CCU6x, MultiCAN, and USIC ($\overline{\text{ESR1}}$ or $\overline{\text{ESR2}}$)
- software-controlled input/output signal

The Oscillator Input XTAL1 and Output XTAL2 connect the internal **Main Oscillator** to the external crystal. The oscillator provides an inverter and a feedback element. The standard external oscillator circuitry comprises the crystal, two low end capacitors and

Dedicated Pins

series resistor to limit the current through the crystal. The main oscillator is intended for the generation of a high-precision operating clock signal for the XC27x8X.

An external clock signal may be fed to the input XTAL1, leaving XTAL2 open. The current logic state of input XTAL1 can be read via a status flag, so XTAL1 can be used as digital input if neither the oscillator interface nor the clock input is required.

Note: Pin XTAL1 belongs to the core power domain DMP_M. All input signals, therefore, must be within the core voltage range.

The Test Mode Input $\overline{\text{TESTM}}$ puts the XC27x8X into test mode, which is used during the production tests of the device. In test mode, the XC27x8X behaves different from normal operation. Therefore, pin $\overline{\text{TESTM}}$ must be held high (connect to V_{DDPB}) for normal operation in an application system.

The Test Reset Input $\overline{\text{TRST}}$ puts the XC27x8X's debug system into reset state. During normal operation this input should be held low. For debugging purposes the on-chip debugging system can be enabled by driving pin $\overline{\text{TRST}}$ high at the rising edge of $\overline{\text{PORST}}$.

The Analog Reference Voltage Supply pins V_{AREFX} and V_{AGND} provide separate reference voltage for the on-chip Analog/Digital-Converter(s). This reduces the noise that is coupled to the analog input signals from the digital logic sections and so improves the stability of the conversion results, when V_{AREF} and V_{AGND} are properly decoupled from V_{DD} and V_{SS} . Also, because conversion results are generated in relation to the reference voltages, ratiometric conversions are easily achieved.

Note: Channel 0 of each module can be used as an alternate reference voltage input.

The Digital Core Supply pins $V_{\text{DDIM}}/V_{\text{DDI1}}$ serve two purposes: While the on-chip EVVRs provide the power for the core logic of the XC27x8X these pins connect the EVVRs to their external buffer capacitors. For external supply, the core voltage is applied to these pins. The respective $V_{\text{DDI}}/V_{\text{SS}}$ pairs should be decoupled as close to the pins as possible. Use ceramic capacitors and observe their values recommended in the respective Data Sheet.

The Power Supply Inputs $V_{\text{DDPA}}/V_{\text{DDPB}}$ provide the power supply for all the analog and digital logic of the XC27x8X. Each power domain (DMP_A and DMP_B) can be supplied with an arbitrary voltage within the specified voltage range (please refer to the corresponding Data Sheets). These pins supply the output drivers as well as the on-chip EVVRs (V_{DDPB}), except for external core voltage supply. The respective $V_{\text{DDP}}/V_{\text{SS}}$ pairs should be decoupled as close to the pins as possible.

Dedicated Pins

The Ground Reference pins V_{SS} provide the ground reference voltage for the power supplies as well as the reference voltage for the input signals.

Note: All V_{DDx} pins and all V_{SS} pins must be connected to the power supplies and ground, respectively.

12 External Bus Controller (EBC)

The EBC enables the C166SV2 CPU access to chip external and internal peripherals and memories. The access can be of program fetch type or data exchange. If used to interface to the chip external world the external bus is also referred to as EXTBUS if used with internal (local) components it is also referred to as LXBUS.

12.1 Summary of Features

The EBC functional and timing behavior is widely configurable so that it can be tailored to fit into a large range of applications.

- Demultiplexed and multiplexed mode of operation
- Up to 24 address lines
- 8-bit or 16-bit data bus
- Synchronous and asynchronous ready
- Up to 8 bus channels
- Address window programmable for up to 7 channels
- Bus timing and function programmable for each channel

12.2 Overview

The function and timing characteristics of the EBC are controlled by a set of configuration registers.

The basic and general behavior is programmed via the mode selection registers EBCMOD0 and EBCMOD1.

The EBC supports up to eight ($x=0\dots7$) bus channels linked to a dedicated chip select (\overline{CSx}). Each channel is programmable by a dedicated set of registers. The FCONCSx registers specify the functional characteristics while the TCONCSx registers specify the cycle timing. The address area assigned to a channel is definable for seven channels by the ADDRSEL(1...7) registers. The remaining uncovered address areas are assigned to CS0.

External \overline{CSx} signals can be used in order to save external glue logic. Access to non timing deterministic external devices is supported by a particular READY functionality.

The external bus timing is related to the reference CLock OUTput (CLKOUT) signal. All bus signals are generated in relation to the rising edge of this clock. The external bus protocol is compatible with those of the C166 family. However, the external bus timing is improved in terms of wait state granularity and signal flexibility.

12.3 Naming Conventions

For description of EBC timing and functions the following bus signal names will be used.

Control signals:

- **ALE** - Address Latch Enable (high active). Indicates that the applied address is valid.
- **\overline{CS}** - Chip select.
- **$\overline{WR}/\overline{WRL}$** - Write Strobe, Write Low Byte Strobe (low active). Configured either to a general write request or a write request for the low byte.
- **$\overline{BHE}/\overline{WRH}$** - Byte High Enable, Write High Byte Strobe (low active). Configured either to an enable for the high byte or a write request for the high byte.
- **\overline{RD}** - Read Strobe (low active).
- **READY** - Ready to indicate end of actions (programmable polarity).

Bus signals:

- **A** or **ADDR** - Address bus.
- **D** or **DATA** - Data bus.
- **AD** - Shared Data/Address[15:0] bus.

12.4 Timing Description

Bus characteristics can be programmed to the following access modes:

- 16-bit data bus with address not multiplexed
- 16-bit data bus with address multiplexed
- 8-bit data bus with address not multiplexed
- 8-bit data bus with address multiplexed

Multiplexed mode means that the data bus is used in a time multiplex mode for address (16 LSB only) and for data. In demultiplexed mode the data bus is used for data only and an additional address bus must be made available.

EBC timing is programmed in so called "bus phases". The final timing at the device pins depends on:

- Length of a bus phase (bound to system clock)
- Signal delay between EBC core and device pins

Therefore to calculate the required bus phases the system clock speed and timing values provided in the XC27x8X data sheet must be considered.

12.4.1 Bus Phases

The EBC timing is defined by six different timing phases (A-F). These phases influence the control signals needed for any access sequence to a bus device.

At the beginning of a phase the output signals change within a defined output delay time. The particular delay times are specified in the XC27x8X data book. After the output delay the values of the control output signals are stable within this phase. Each phase can occupy a programmable number of CLKOUT cycles.

A Phase - $\overline{\text{CS}}$ Change Phase

The A phase can take 0-3 clocks. It is used for tristating databus drivers from the previous cycle (tristate wait states after chip select switch).

A phase cycles are not inserted at every access cycle, but only when changing the $\overline{\text{CS}}$. If an access using one $\overline{\text{CS}}$ ($\overline{\text{CSx}}$) ends and the next access with a different $\overline{\text{CS}}$ ($\overline{\text{CSy}}$) is started, then A phase cycles are performed according to the bits set in the **first** $\overline{\text{CS}}$ ($\overline{\text{CSx}}$). This feature is used to optimize wait states with devices having a long turn-off delay at their databus drivers, such as EPROMs and flash memories.

The A phase cycles are inserted while the addresses and ALE of the next cycle are already applied.

If there are some idle cycles between two accesses, these clocks are taken into account and the A phase is shortened accordingly. For example, if there are three tristate cycles programmed and two idle cycles occur, then the A phase takes only one clock.

B Phase - Address Setup / ALE Phase

The B phase can take 1-2 clocks. It is used for addressing devices before giving a command, and defines the length of time that ALE is active. In multiplexed bus mode, the address is applied for latching.

C Phase - Delay Phase

The C phase is similar to the A and B phases but ALE is already low. It can take 0-3 clocks. In multiplexed bus mode, the address is held in order to be latched safely. Phase C cycles can be used to delay the command signals (RW delay).

D Phase - Write Data Setup / Mux Tristate Phase

The D phase can take 0-1 clocks. It is used to tristate the address on the multiplexed bus when a read cycle is performed. For all write cycles, it is used to ensure that the data are valid on the bus before the command is applied.

E Phase - $\overline{\text{RD}}/\overline{\text{WR}}$ Command Phase

The E phase is the command or access phase, and takes 1-32 clocks. Read data are fetched, write data are put onto the bus, and the command signals are active. Read data are registered with the terminating clock of this phase.

The READY function lengthens this phase, too. READY-controlled access cycles may have an unlimited cycle time.

F Phase - Address / Write Data Hold Phase

The F phase is at the end of an access. It can take 0-3 clocks.

Addresses and write data are held while the command is inactive. The number of wait states inserted during the F phase is independently programmable for read and write accesses. The F phase is used to program tristate wait states on the bidirectional data bus in order to avoid bus conflicts.

12.4.2 Demultiplexed Bus

General timing diagrams of a read and a write demultiplexed access are shown below.

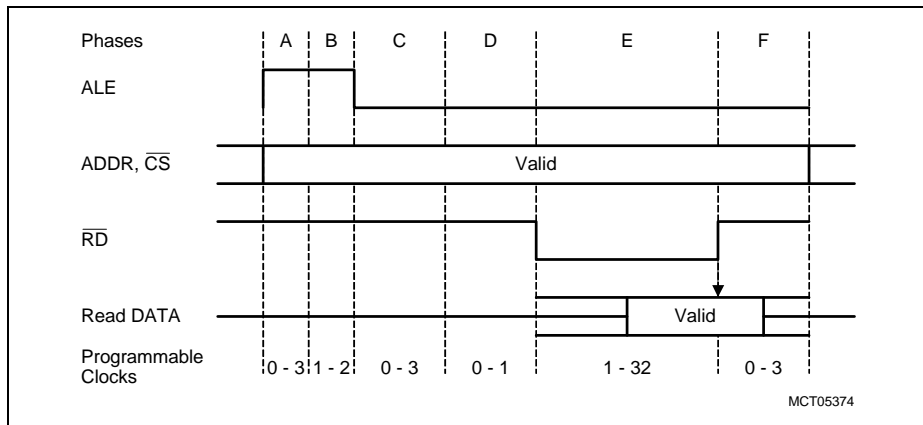


Figure 12-1 Demultiplexed Bus Read

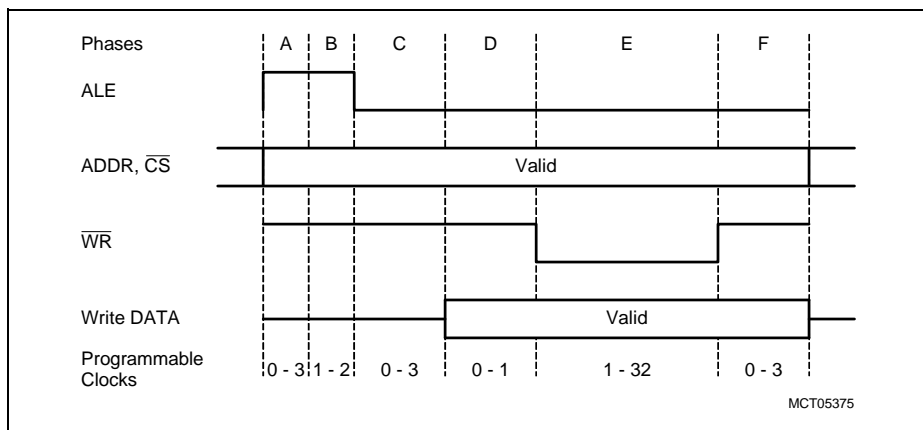


Figure 12-2 Demultiplexed Bus Write

- A phase: Addresses valid, ALE high, no command. \overline{CS} switch tristate wait states
- B phase: Addresses valid, ALE high, no command. ALE length
- C phase: Addresses valid, ALE low, no command. R/W delay
- D phase: Write data valid, ALE low, no command. Data valid for write cycles
- E phase: Command (read or write) active. Access time
- F phase: Command inactive, address hold. Read data tristate time, write data hold time

12.4.3 Multiplexed Bus

General timing diagrams of a read and a write multiplexed access are shown below.

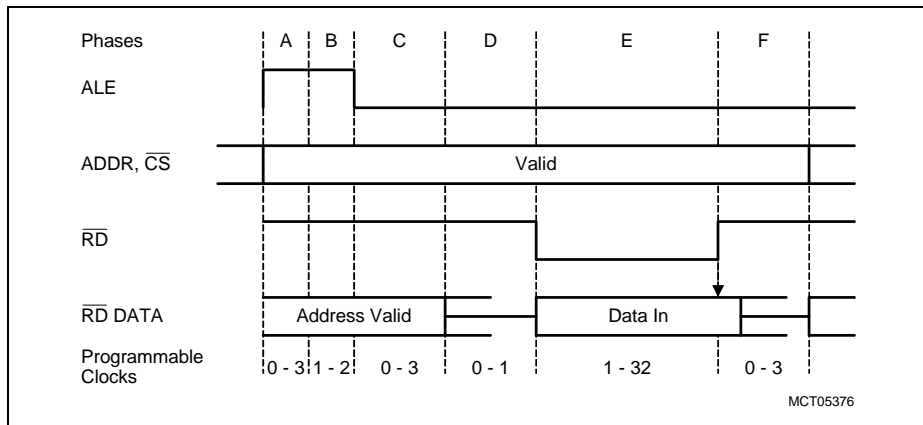


Figure 12-3 Multiplexed Bus Read

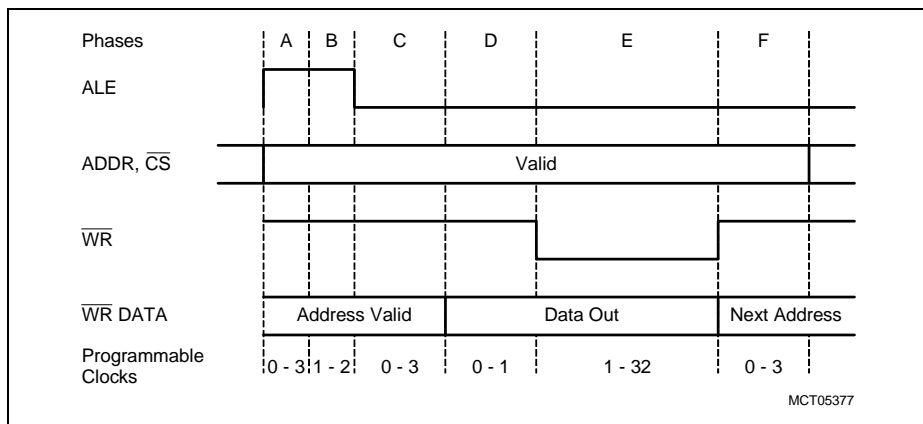


Figure 12-4 Multiplexed Bus Write

- A phase: addresses valid, ALE high, no command. \overline{CS} switch tristate wait states
- B phase: addresses valid, ALE high, no command. ALE length
- C phase: addresses valid, ALE low, no command. Address hold, R/W delay
- D phase: address tristate for read cycles, data valid for write cycles, ALE low, no command
- E phase: command (read or write) active. Access time

- F phase: command inactive, address hold. Read data tristate time, write data hold time.

12.4.4 Fastest Access Cycles

The fastest possible bus cycle in a system depends also on the pad timing. Therefore, the number of required cycles for a bus access depends on the current system frequency. The minimum bus cycles shown below cannot be achieved at very high system frequencies.

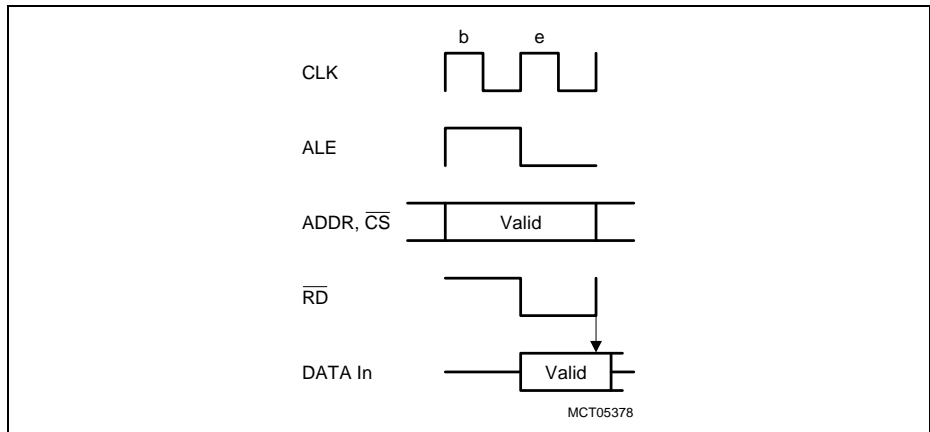


Figure 12-5 Fastest Read Cycle Demultiplexed Bus

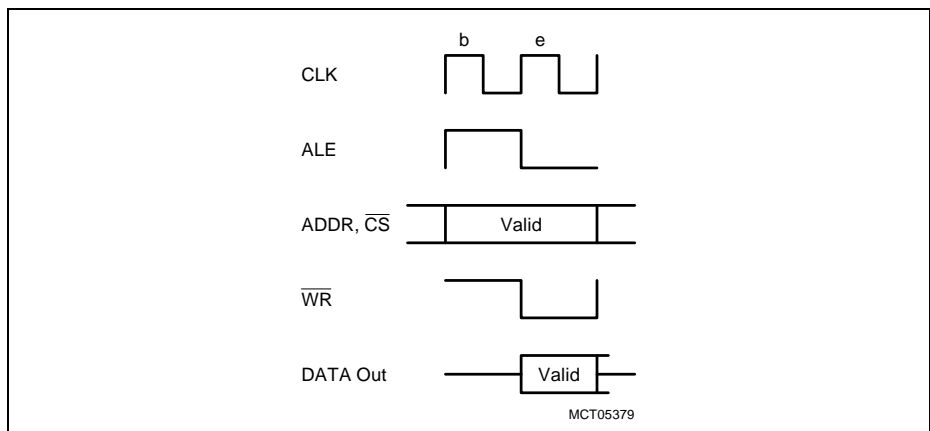


Figure 12-6 Fastest Write Cycle Demultiplexed Bus

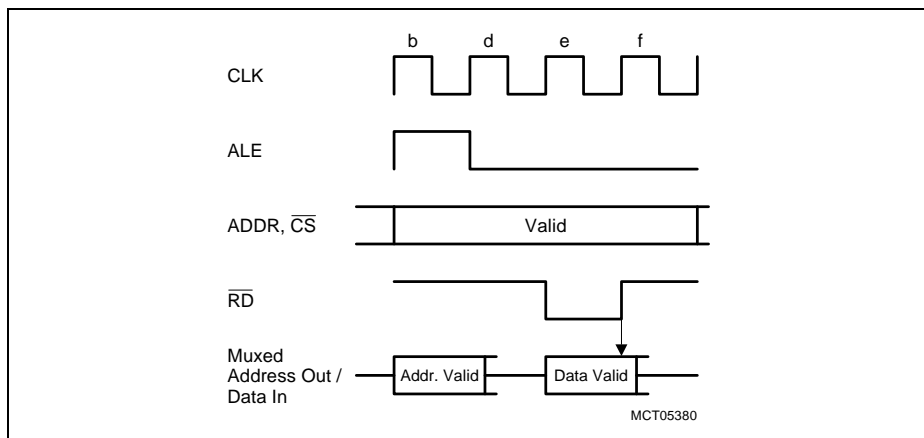


Figure 12-7 Fastest Read Cycle Multiplexed Bus

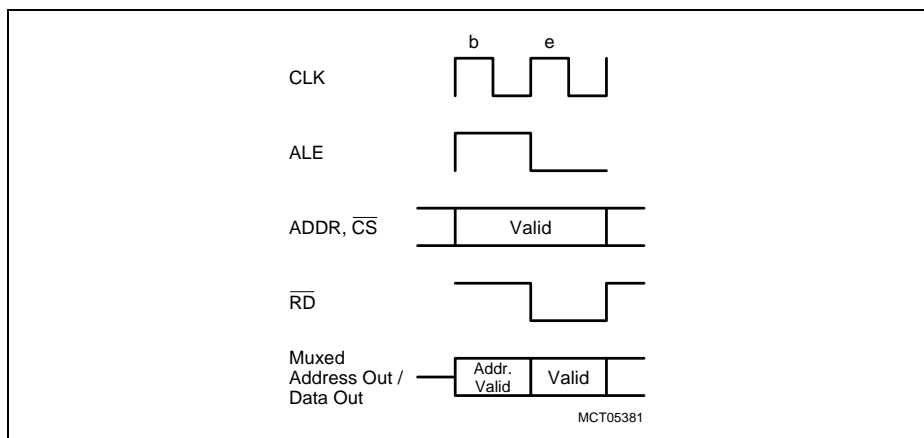


Figure 12-8 Fastest Write Cycle Multiplexed Bus

12.5 Address Windows

The EBC provides up to 8 logical bus channels. For 7 of these (assigned to $\overline{CS1} \dots \overline{CS7}$) the allocated address window can be programmed by the ADDRSEL(1...7) registers. The remaining channel (assigned to $\overline{CS0}$) has no address select register assigned and covers the remaining EBC address space.

Note that not the complete XC27x8X address space can be accessed by the EBC. For an overview on allocation of the complete address space please refer to the "Memory Organization" chapter.

12.5.1 Window Allocation

The size and start address of an address window is defined according to [Table 12-1](#). The size of the window is chosen by ADDRSELx.RGSZ. Depending on the size the relevant bits of ADDRSELx.RGSAD (marked with 'R') are used to select the corresponding window start address. The lower bits of ADDRSELx.RGSAD (marked 'x') are disregarded.

A programmed address windows must additionally be enabled by setting the corresponding FCONCSx.ENCs bit.

Table 12-1 Address Range and Size for ADDRSELx

ADDRSELx		Address Window	
Range Size RGSZ	Relevant (R) Bits of RGSAD	Selected Address Range	Range Start Address A[23:0] Selected with R-bits of RGSAD
3 ... 0	15 ... 4	Size	A23 ... A0
0000	RRRR RRRR RRRR	4 Kbytes	RRRR RRRR RRRR 0000 0000 0000
0001	RRRR RRRR RRRx	8 Kbytes	RRRR RRRR RRR0 0000 0000 0000
0010	RRRR RRRR RRxx	16 Kbytes	RRRR RRRR RR00 0000 0000 0000
0011	RRRR RRRR Rxxx	32 Kbytes	RRRR RRRR R000 0000 0000 0000
0100	RRRR RRRR xxxx	64 Kbytes	RRRR RRRR 0000 0000 0000 0000
0101	RRRR RRRx xxxx	128 Kbytes	RRRR RRR0 0000 0000 0000 0000
0110	RRRR RRxx xxxx	256 Kbytes	RRRR RR00 0000 0000 0000 0000
0111	RRRR Rxxx xxxx	512 Kbytes	RRRR R000 0000 0000 0000 0000
1000	RRRR xxxx xxxx	1 Mbytes	RRRR 0000 0000 0000 0000 0000
1001	RRRx xxxx xxxx	2 Mbytes	RRR0 0000 0000 0000 0000 0000
1010	RRxx xxxx xxxx	4 Mbytes	RR00 0000 0000 0000 0000 0000
1011	Rxxx xxxx xxxx	8 Mbytes	R000 0000 0000 0000 0000 0000
11xx	xxxx xxxx xxxx	reserved	---- ---- ---- ---- ---- ----

12.5.2 Window Overlap

Since it is possible to program overlapping address areas an arbitration scheme is defined to handle these cases. For each access directed to the EBC it compares the current address with all address select registers of enabled windows. This comparison is done in three levels.

Priority 1:

Registers ADDRSELx [x = 2, 4, 6] of enabled windows are evaluated first. Upon a match the access starts on the respective channel. Overlap of windows within this group will lead to undefined behavior.

Priority 2:

Registers ADDRSELy [y = 1, 3, 5, 7] of enabled windows are evaluated in this step. Upon a match the access starts on the respective channel. Overlap of windows within this group will lead to undefined behavior. Overlaps with priority 1 ADDRSELx are only allowed for the (x,y) pairs (2,1), (4,3) and (6, 5).

Priority 3:

If channel 0 is enabled the access is directed to it. Otherwise no bus action occurs.

12.6 Ready Controlled Bus Access

In cases, where the response time of a peripheral is not constant, or where the programmable wait states are not enough, the XC27x8X EBC provides the so called READY controlled bus access scheme.

In this scheme bus accesses are terminated by the READY input signal. During phase E the EBC first counts a programmable number of clock cycles (1...32) and then starts in the last wait cycle to monitor the internal READY line ("READY Int" in [Figure 12-9](#)) to determine the actual end of the current bus cycle. The external device drives READY active in order to indicate that data has been latched (write cycle) or is available (read cycle).

A READY controlled bus cycle requires one synchronization cycle to terminate. Programmed phase F cycles include this synchronization cycle. Therefore setting TCONCSx phase F to 0 clock cycles will have the same effect as setting to 1 clock cycle.

12.6.1 Enabling the Ready Control

The READY pin is enabled by setting the bit RDYDIS in EBCMOD0 to '0' in order to activate the corresponding port pin. The polarity of the READY is also defined inside the EBCMOD0 register by the RDYPOL bit.

For a specific address window the READY function is enabled via the RDYEN bit in the FCONCSx register. By programming of FCONCSx.RDYMODO the READY is handled either in synchronous or in asynchronous mode (see also [Figure 12-9](#)).

When the READY function is enabled for a specific address window, each bus cycle within this window must be cleanly terminated with an active READY signal. Otherwise the EBC will be completely blocked by this pending access.

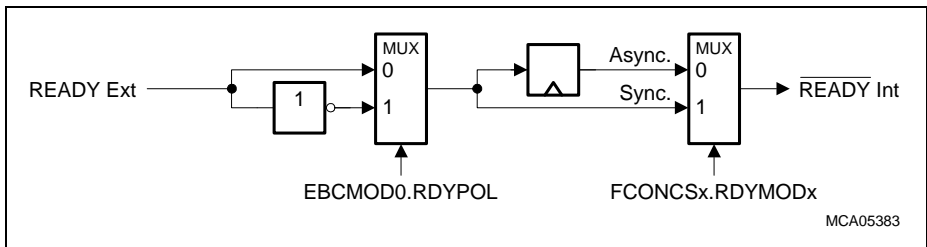


Figure 12-9 External to internal READY conversion

12.6.2 Synchronous and Asynchronous READY

The synchronous READY provides the fastest bus cycles, but requires setup and hold times to be met. The CLKOUT signal should be enabled and may be used by the peripheral logic to control the READY timing in this case.

External Bus Controller (EBC)

The asynchronous READY is less restrictive, but requires one additional wait state caused by the internal synchronization. As the asynchronous READY is sampled earlier programmed wait states may be necessary to provide proper bus cycles

A READY signal (especially asynchronous READY) that has been activated by an external device should be deactivated in response to the trailing (rising) edge of the respective command ($\overline{\text{RD}}$ or $\overline{\text{WR}}$).

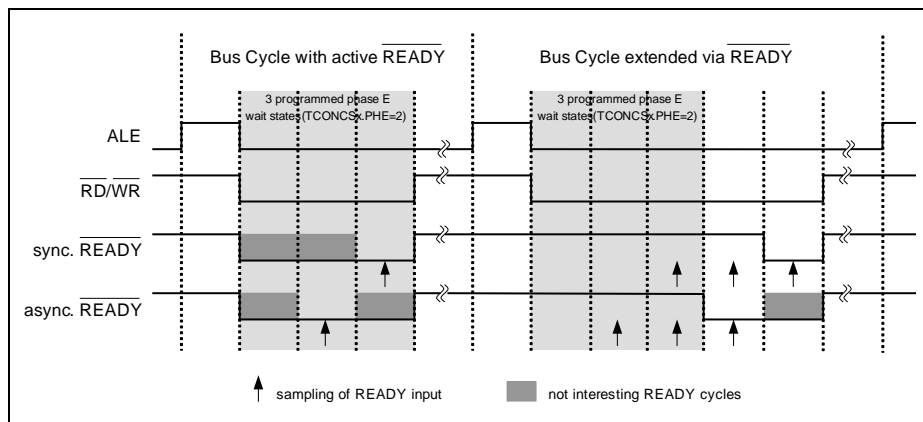


Figure 12-10 Ready controlled bus cycles

12.6.3 Combining the READY function with predefined wait states

Typically an external wait state or READY control logic takes a while to generate the READY signal when a cycle was started. After a predefined number of clock cycles the XC27x8X will start checking its READY line to determine the end of the bus cycle.

When using the READY function with so-called 'normally-ready' peripherals, it may lead to erroneous bus cycles, if the READY line is sampled too early. These peripherals pull their READY output active, while they are idle. When they are accessed, they drive READY inactive until the bus cycle is complete, then drive it active again. If, however, the peripheral drives READY inactive a little late, after the first sample point of the XC27x8X, the controller samples an active READY and terminates the current bus cycle too early. By inserting predefined wait states the first READY sample point can be shifted to a time, where the peripheral has safely controlled the READY line.

12.7 EBC Idle State

When the external bus interface of the EBC is enabled, but no internal or external access is currently executed, the EBC is idle. As long as only on-chip resources such as RAM, peripherals (excluding LXBUS peripherals connected via EBC), registers, etc. are used, the external bus interface does not change (see table 12-2).

The external control signals (\overline{RD} and \overline{WR} or $\overline{WRL}/\overline{WRH}$ if enabled) remain inactive (high) during EBC idle state.

Table 12-2 Status of the External Bus Outputs During EBC Idle State

Pins	Status of Pins During EBC Idle
AD15...AD0	tristate (floating)
A15...A0	undefined address (if used for the bus interface)
A23...A16	undefined segment address (on selected pins)
$\overline{CS7}...\overline{CS0}$	inactive (high)
\overline{BHE}	level corresponding to last external access
ALE	inactive (low)
\overline{RD} , \overline{WR} , \overline{WRL} , \overline{WRH}	inactive (high)

12.8 Register Description

The EBC registers are located in the internal IO area. Registers located there use the shorthand XSFR.

Table 12-3 Registers Address Space

Module	Base Address	End Address	Note
EBC	00EE00 _H	00EEFF _H	

12.8.1 EBC Mode Registers

The two mode registers control the XC27x8X EXTBUS pin usage and configuration. Disabled EXTBUS pins may be usable as general purpose IO as described in the "Parallel Ports" chapter.

EBCMOD0

EBC Mode Register 0

XSFR(00_H)

Reset value: XXXX_H¹⁾

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDY POL	RDY DIS	ALE DIS	BYT DIS	WR CFG	EBC DIS	SLA VE	ARB EN	CSPEN				SAPEN			
rw	rw	rw	rw	rw	rw	rw	rw	rw				rw			

¹⁾Value is modified by startup software depending on selected startup mode. When starting from internal memory value will be 5400_H

Field	Bits	Type	Description
RDYPOL	15	rw	READY Pin Polarity 0 _B READY is active low 1 _B READY is active high
RDYDIS	14	rw	READY Pin Disable 0 _B READY enabled 1 _B READY disabled
ALEDIS	13	rw	ALE Pin Disable 0 _B ALE enabled 1 _B ALE disabled
BYTDIS	12	rw	BHE Pin Disable 0 _B BHE enabled 1 _B BHE disabled
WRCFG¹⁾	11	rw	Configuration for Pins WR/WRL, BHE/WRH 0 _B WR and BHE 1 _B WRL and WRH

External Bus Controller (EBC)

Field	Bits	Type	Description
EBCDIS	10	rw	EBC Pins Disable 0 _B EBC is using the pins for external bus 1 _B EBC pins disabled
SLAVE	9	rw	SLAVE Mode Enable Functionality not available. Must be written 0.
ARBEN	8	rw	BUS Arbitration Pins Enable Functionality not available. Must be written 0.
CSPEN	[7:4]	rw	CSx Pins Enable (only external CSx) 0 _H All external Chip Select pins disabled. 1 _H $\overline{CS0}$ pin enabled 2 _H $\overline{CS1}$ and $\overline{CS0}$ pin enabled ... 5 _H Five \overline{CSx} pins enabled: $\overline{CS4}$ - $\overline{CS0}$ other bit combinations not supported (reserved)
SAPEN	[3:0]	rw	Segment Address Pins Enable 0 _H All segment address pins disabled 1 _H One: A[16] enabled ... 8 _H Eight: A[23:16] enabled other bit combinations not supported (reserved)

1) A change of the bit content is not valid before the next external bus access cycle.

Byte Write Configurations

For 16-bit data bus configurations the byte write characteristics are programmable by bitfield WRCFG. The following table illustrates the related signals function.

Table 12-4 Byte Write Configurations

written byte		WRCFG=0			WRCFG=1		
low	high	\overline{WR}	BHE	ADDR[0]	\overline{WRL}	\overline{WRH}	ADDR[0]
-	-	inactive	don't care	0/1	inactive	inactive	0/1
write	-	active	inactive	0	active	inactive	0/1
-	write	active	active	1	inactive	active	0/1
write	write	active	active	0	active	active	0/1

EBCMOD1

EBC Mode Register 1

XSFR(02_H)

Reset value: 00XX_H¹⁾

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								WRP DIS	DHP DIS	ALP DIS	A0P DIS	APDIS			
r	r	r	r	r	r	r	r	rw	rw	rw	rw	rw			

1) Value is modified by startup software depending on selected startup mode. When starting from internal memory value will be 003F_H

Field	Bits	Type	Description
0	[15:8]	r	Reserved Read as 0, should be written 0
WRPDIS	7	rw	WR/WRL Pin Disable 0 _B <u>WR/WRL</u> pin enabled 1 _B <u>WR/WRL</u> pin disabled
DHPDIS	6	rw	Data High Port Pins Disable 0 _B Address/Data bus pins 15-8 enabled 1 _B Address/Data bus pins 15-8 disabled.
ALPDIS	5	rw	Address Low Pins Disable 0 _B Address bus pins 7-0 generally enabled (depending on APDIS/A0PDIS) 1 _B Address bus pins 7-0 disabled.
A0PDIS	4	rw	Address Bit 0 Pin Disable 0 _B Address bus pin 0 enabled 1 _B Address bus pin 0 disabled.
APDIS	[3:0]	rw	Address Port Pins Disable 0 _H Address bus pins A15-A1 enabled 1 _H Pin A15 disabled, A14-A1 enabled 2 _H Pins A15-A14 disabled, A13-A1 enabled 3 _H Pins A15-A13 disabled, A12-A1 enabled ... E _H Pins A15-A2 disabled, A1 enabled F _H Address bus pins 15-1 disabled.

12.8.2 Timing Control Registers

The timing control registers are used to program the cycle timing for the different access phases. The timing control registers may be reprogrammed during code fetches from the affected address window. The new settings become valid for the following access.

TCONCS0

Timing Control for CS0

XSFR(10_H)

Reset value: 7C3D_H

TCONCSx (x=1-4)

Timing Control for CSx

XSFR(10_H+x*8)

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	WRPHF	RDPHF					PHE			PHD	PHC	PHB		PHA	
r	rw	rw					rw			rw	rw	rw		rw	

Field	Bits	Type	Description
0	15	r	Reserved Read as 0, should be written 0
WRPHF	[14:13]	rw	Write Phase F 00 _B 0 clock cycles ... 11 _B 3 clock cycles
RDPHF	[12:11]	rw	Read Phase F 00 _B 0 clock cycles ... 11 _B 3 clock cycles
PHE	[10:6]	rw	Phase E 00 _H 1 clock cycle ... 1F _H 32 clock cycles
PHD	5	rw	Phase D 0 _B 0 clock cycles 1 _B 1 clock cycle
PHC	[4:3]	rw	Phase C 00 _B 0 clock cycles ... 11 _B 3 clock cycles
PHB	2	rw	Phase B 0 _B 1 clock cycle 1 _B 2 clock cycles
PHA	[1:0]	rw	Phase A 00 _B 0 clock cycles ... 11 _B 3 clock cycles

12.8.3 Function Control Registers

The Function Control registers are used to control the bus and ready functionality for a selected address window. It can be distinguished between 8 and 16 bit bus and multiplexed and demultiplexed accesses. Furthermore it can be defined whether the address window (and its chip select signal \overline{CS}_x) is generally enabled or not.

FCONCS0

Function Control for CS0

XSFR(12_H)

Reset value: 0011_H

FCONCSx (x = 1-4)

Function Control for CSx

XSFR(12_H+x*8)

Reset value: 00XX_H¹⁾

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	BTYP	0	RDY MOD	RDY EN	EN CS	
r	r	r	r	r	r	r	r	r	r	rw	r	rw	rw	rw	

1) Value is modified by startup software depending on selected startup mode. When starting from internal memory value will be 0000_H

Field	Bits	Type	Description
0	[15:6]	r	Reserved Read as 0, should be written 0
BTYP	[5:4]	rw	Bus Type Selection 00 _B 8 bit Demultiplexed 01 _B 8 bit Multiplexed 10 _B 16 bit Demultiplexed 11 _B 16 bit Multiplexed
0	3	r	Reserved Read as 0, should be written 0
RDYMOD	2	rw	Ready Mode 0 _B asynchronous READY 1 _B synchronous READY
RDYEN	1	rw	Ready enable 0 _B access time is controlled by bitfield PHEx 1 _B access time is controlled by bitfield PHEx and READY signal
ENCS	0	rw	Enable Chip Select 0 _B disable 1 _B enable

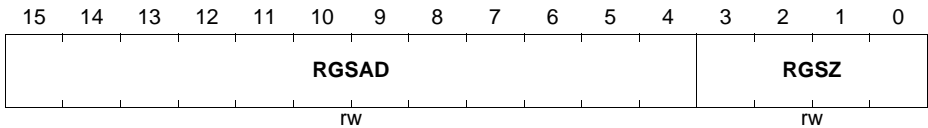
External Bus Controller (EBC)

Note: The specific ENCSx bits in the FCONCSx registers enable the related address windows and bus functions and the corresponding chip select signal CSx. Additionally it depends on the definition of bitfield CSPEN in register EBCMOD0 how many CSx pins are made available for the external system. If an address window is enabled but no external pin is available for the CSx, the bus cycle is executed without assertion of the external chip select signal.

12.8.4 Address Window Selection Registers

ADDRSELx (x = 1 - 4)

Address Range/Size for CSx XSFR(16_H+x*8) Reset value: 0000_H



Field	Bits	Type	Description
RGSAD	[15:4]	rw	Range Start Address Address Range Start Address Selection
RGSZ	[3:0]	rw	Range Size Address Range Size Selection (see Table 12-1)

12.9 EBC Implementation

The External Bus Controller within the XC27x8X affects the behavior of other device components. This section summarizes particular effects like parallel ports pin allocation and shutdown behavior. Additionally the LXBUS integration with its specific registers is detailed here.

12.9.1 Pin allocation for the EBC

If enabled, the EBC takes priority over other programmed port assignments. Depending on the bus mode, a variable number of port pins is used for the bus interface.

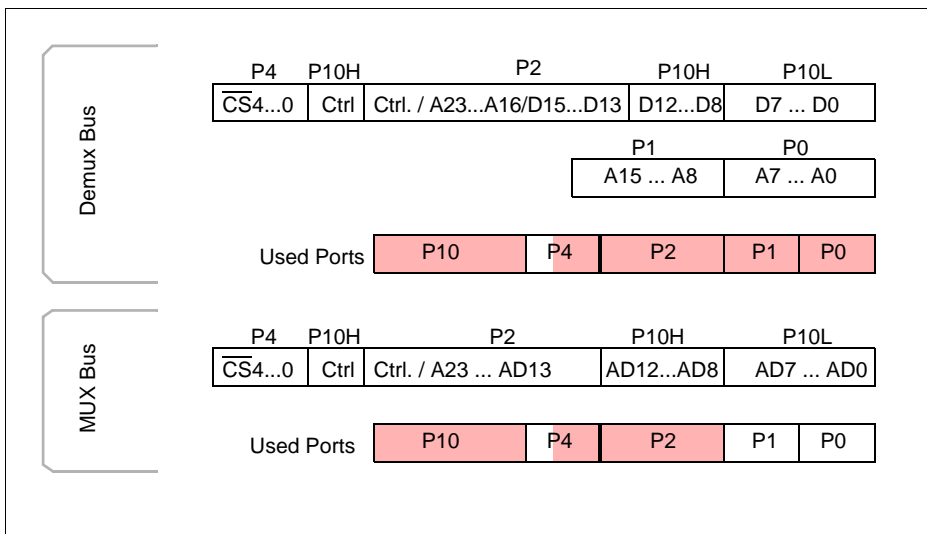


Figure 12-11 External Bus Summary

With the shown assignment of bus signals to ports the following bus interface options can be realized, depending on the used device package:

Table 12-5 Possible Bus Interfaces

Package	Addr.Width	Data Width	BHE	CS	Demux	READY
144-Pin	24 bits	8/16 bits	YES	≤5	YES	YES
100-Pin	24 bits	8/16 bits	YES	≤4	YES	YES

12.9.2 Unused Registers

The XC27x8X external chip select signals are limited due to chip packaging. According to this limitation the corresponding EBC channels are not available. The channels $x=(5, 6)$ with related set of registers ADDRSEL x , TCONCS x , FCONCS x are therefore not available for use. For software compatibility reasons the corresponding register address space must not be read or written.

12.9.3 Access Control to LXBUS Modules

In the XC27x8X the EBC channel 7 is reserved for access to chip internal LXBUS peripherals. In general accesses to LXBUS are not visible on the external bus EXTBUS. During LXBUS cycles the EXTBUS remains enabled but is driven to inactive states (control signals) or switched into the read mode (busses).

12.9.4 Shutdown Control

In case of a shutdown request from the SCU the EBC ensures that all the different functions of the EBC are in a non-active state before the whole chip is switched to a power save mode. A running bus cycle is finished, still requested bus cycles are executed. Only when this shutdown sequence is terminated, the shutdown acknowledge is generated from EBC (and from other modules, as described for SCU) and the chip can enter the requested mode.

12.9.5 Dedicated Registers

The dedicated EBC registers are located in the internal IO area. Registers located there use the shorthand XSFR.

12.9.5.1 Registers dedicated to LXBUS modules

For accesses to the LXBUS peripherals $\overline{CS7}$ and its control registers ADDRSEL7, TCONCS7 and FCONCS7 are used. The selection of LXBUS is chip internally controlled with $\overline{CS7}$.

TCONCS7

The LXBUS cycle timing is controlled with register TCONCS7. It uses the shortest possible timing with two clock cycles for one bus cycle. But this minimum timing will be lengthened with waitstate(s) controlled by the modules using the \overline{READY} function. This timing is reflected by the reset value of TCONCS7.

TCONCS7

Timing Control for CS7

XSFR(48_H)

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	WRPHF	RDPHF					PHE			PHD	PHC	PHB		PHA	
r	r	r					r			r	r	r		r	

Field	Bits	Type	Description
0	15	r	Reserved Read as 0, should be written 0
WRPHF	[14:13]	r	Write Phase F 0 _B 0 clock cycles ... 11 _B 3 clock cycles
RDPHF	[12:11]	r	Read Phase F 0 _B 0 clock cycles ... 11 _B 3 clock cycles
PHE	[10:6]	r	Phase E 0 _H 1 clock cycle ... 1F _H 32 clock cycles
PHD	5	r	Phase D 0 _B 0 clock cycles 1 _B 1 clock cycle
PHC	[4:3]	r	Phase C 00 _B 0 clock cycles ... 11 _B 3 clock cycles
PHB	2	r	Phase B 0 _B 1 clock cycle 1 _B 2 clock cycles
PHA	[1:0]	r	Phase A 00 _B 0 clock cycles ... 11 _B 3 clock cycles

FCONCS7

The value of this dedicated bus function control register is selected according to the requirements of the internally attached modules: 16-bit demultiplexed bus, access time controlled with synchronous READY.

FCONCS7

Function Control for CS7

XSFR(4A_H)

Reset value: 0027_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	BTYP		0	RDY MOD	RDY EN	EN CS
r	r	r	r	r	r	r	r	r	r		r	r	r	r	r

Field	Bits	Type	Description
0	[15:6]	r	Reserved Read as 0, should be written 0
BTYP	[5:4]	r	Bus Type Selection 00 _B 8 bit Demultiplexed 01 _B 8 bit Multiplexed 10 _B 16 bit Demultiplexed 11 _B 16 bit Multiplexed
0	3	r	Reserved Read as 0, should be written 0
RDYMOD	2	r	Ready Mode 0 _B asynchronous READY 1 _B synchronous READY
RDYEN	1	r	Ready enable 0 _B access time is controlled by bitfield PHEx 1 _B access time is controlled by bitfield PHEx and READY signal
ENCS	0	r	Enable Chip Select 0 _B disable 1 _B enable

Register ADDRSEL7

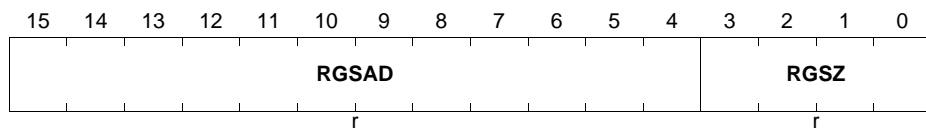
The value of the dedicated address select register allocates the address range 20'0000_H to 20'FFFF_H in the external IO area for the attached chip internal modules.

ADDRSEL7

Address Range/Size for CS7

XSFR(4E_H)

Reset value: 2004_H



Field	Bits	Type	Description
RGSAD	[15:4]	r	Range Start Address Address Range Start Address Selection
RGSZ	[3:0]	r	Range Size Address Range Size Selection (see Table 12-1)

13 On-Chip Debug Support (OCDS)

The XC27x8X includes an OCDS system, which provides convenient debugging, controlled directly by an external tool via debug interface pins.

OCDS Components

- **Debug Interface**
- **Cerberus**
- **OCDS Module**

On-Chip Debug Support (OCDS)

The OCDS system ([Figure 13-1](#)) supports a broad range of debug features including breakpoints and the tracing of memory locations. A typical application of the OCDS is to debug user software running on the XC27x8X in a real time system environment.

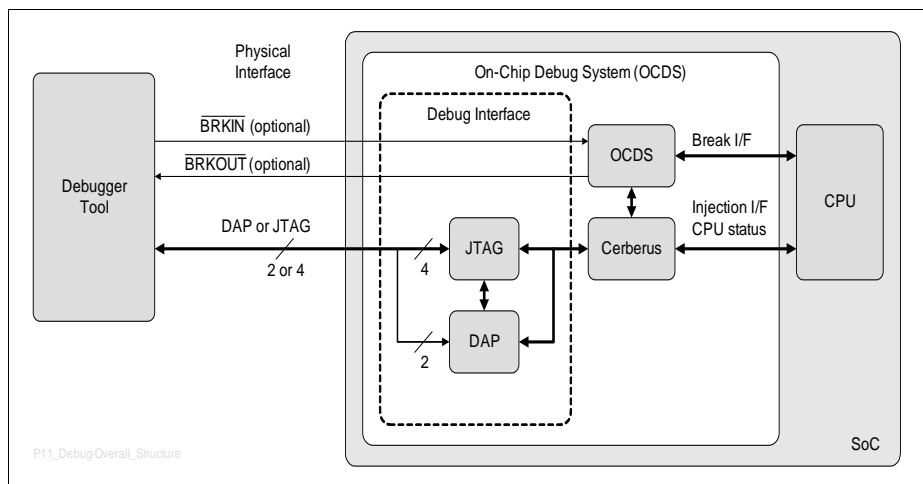


Figure 13-1 OCDS Block Diagram

The OCDS is controlled by an external tool via the **Debug Interface**. The physical interface is either DAP or JTAG plus an optional break interface with one or two pins. The break interface supports very low latency triggers between XC27x8X and tool and/or system environment if needed. The memory mapped OCDS registers are accessible via the DAP/JTAG interface using Cerberus. In addition there is a limited set of special Cerberus debug IO instructions. As an alternative the OCDS can be controlled by a debug monitor program, which communicates with the tool over a user interface like CAN. The OCDS system interacts with the CPU through an injection interface to allow execution of Cerberus-generated instructions, and through a break port.

OCDS System Features

- Hardware, software and external pin breakpoints
- Trigger action can be CPU-halt, monitor call, data transfer and/or $\overline{\text{BRKOUT}}$ signal
- Read/write access to the whole address space
- Single stepping
- Non intrusive debugging (no debug monitor needed)
- Debug also possible over user interface like CAN (with debug monitor)
- DAP or JTAG interface and optional break interface
- Injection of arbitrary CPU instructions
- Fast memory tracing through transfer to external bus (if available)

13.1 Debug Interface

The Debug Interface allows to access OCDS resources. Data can be transferred to/from all on- and off-chip memories and memory mapped control registers.

Features and Functions

- Independent interface for OCDS
- DAP (Device Access Port) or alternatively JTAG
- Break interface for external trigger input and signaling of internal triggers
- Generic memory access functionality
- Independent data transfer channel for e.g. programming of flash memory

The Debug Interface consists of:

- **DAP Interface**
- Alternatively **JTAG Interface** based on the IEEE 1149.1 JTAG standard
- Two additional XC27x8X specific signals - **OCDS Break-Interface**

Attention: *The DAP/JTAG clock frequency must be below the current CPU frequency.*

DAP Interface

The DAP interface is a device access port standardized for the latest Infineon microcontrollers. It reduces the pin count to two pins and offers high noise immunity and robustness.

This interface consists of the signals:

- **DAP0** - clock
- **DAP1** - Serial data input/output

JTAG Interface

The JTAG interface is a standardized and dedicated port, primarily provided for boundary scan board tests.

This interface consists of the JTAG IEEE.1149.1-2001 standard signals:

- **TDI** - Serial data input
- **TDO** - Serial data output
- **TCK** - JTAG clock
- **TMS** - State machine control signal

OCDS Break-Interface

Two optional additional signals provide a direct trigger interface between the Debugger and XC27x8X **OCDS Module**:

- **BRKIN** (BReaK IN request) allows to trigger directly one of the **Debug Actions**.
- **BRKOUT** (BReaK OUT signal) can be activated by OCDS to notify the external world that some predefined debug event has happened.

13.1.1 Routing of Debug Signals

The signals used to connect an external debugger via the JTAG interface and the break interface usually conflict with the requirements to have as many IO pins as possible for the application. In the XC27x8X, these signals are only provided as alternate functions (no dedicated pins). To minimize the impact caused by the debug interface pins, these signals can be mapped to various positions. Thus, each application can select the variant with the least impact. This is controlled via the Debug Pin Routing Register **DBGPRR**. Pin BRKOUT can be assigned to pins P6.0, P10.11, P1.5, or P9.3 as a standard alternate output signal via the respective IOC register.

13.1.1.1 Register DBGPRR

This register controls the pin routing of the DAP/JTAG pins. The routing options are controlled with the register **DBGPRR**, which is set during start-up as described in **Section 1.3.2**.

The bit field description of **DBGPRR includes all routing options for all derivatives of the family with DAP/JTAG Interface. For derivatives with lower pin count packages, unavailable positions shall be treated as reserved.**

DBGPRR

Debug Pin Routing Register ESFR (F06E_H/37_H) Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRS TL	TRS TS	TRS TGT	DBG EN	JTAG DAP	DPR E	DPR BRKIN	DPR TCK	DPR TMS	DPR TDI	DPR TDO					
rh	rh	rw	rw	rw	r	rw	rw	rw	rw	rw		rw			rw

Field	Bits	Type	Description
DPRTDO	[1:0]	rw	Pin Routing for DAP1/TDO 00 _B P7.0 01 _B P10.12 10 _B Reserved 11 _B Reserved
DPRTDI	[3:2]	rw	Pin Routing for TDI 00 _B P5.2 01 _B P10.10 10 _B P7.2 11 _B P8.3
DPRTMS	[5:4]	rw	Pin Routing for TMS 00 _B P5.4 01 _B P10.11 10 _B P7.3 11 _B P8.4
DPRTCK	[7:6]	rw	Pin Routing for DAP0/TCK 00 _B P2.9 01 _B P10.9 10 _B P7.4 11 _B P8.5
DPRBRKIN	[9:8]	rw	Pin Routing for BRKIN 00 _B P5.10 01 _B P10.8 10 _B P7.1 11 _B P8.6
DPRE	10	rw	Port 13 Routing for DAP/JTAG DAP0/TCK P13.6, DAP1/TDO P13.8, TMS P13.3, TDI P13.5. Will overrule all other routing settings for these pins. 0 _B Port 13 is not used. 1 _B Port 13 is used
JTAG_DAP	11	rw	Selection of Debug Interface 0 _B DAP is used 1 _B JTAG is used
DBGEN	12	rw	Enable for selected Debug Interface 0 _B Interface is disabled 1 _B Interface is enabled

Field	Bits	Type	Description
TRSTGT	13	rw	Gating of TRST Pin 0_B DAP/JTAG reset is internally held active 1_B TRST pin is routed to DAP/JTAG reset
TRSTS	14	rh	TRST Pin Value Current value of TRST pin
TRSTL	15	rh	Latched TRST Pin Start-up Value Value of TRST pin latched by PORST release

13.2 OCDS Module

The application of the OCDS Module is to debug user software running on the CPU in the customer's system. This is done with an external debugger, which controls the OCDS Module via the independent [Debug Interface](#).

Features

- Hardware, software and external pin breakpoints
- Hardware trigger generation for breakpoints and external pin output
 - Four single address or two address ranges for instruction or data
 - Combination of instruction (range) and data address (range)
 - Combination of data address (range) and data value (range)
 - Task ID, optional in combination with address (range) for instruction or data
 - Masked comparisons for addresses and data
- The OCDS can also be configured by a debug monitor program
- Single stepping with monitor or CPU halt
- Higher priority interrupts can still be served if CPU is halted
- Instruction pointer visible in Halt Mode

Basic Concept

The on chip debug concept is split up into two parts. The first part covers the generation of debug events and the second part defines what actions are taken when a debug event is generated.

- Debug events:
 - [Hardware Breakpoints](#)
 - [Software Breakpoints](#)
 - [Break Pin Input](#) activated
- Debug event actions:
 - [Halt Mode](#) of the CPU
 - [Call a Monitor](#)
 - [Triggered Transfer](#)

– **Activate External Pin**

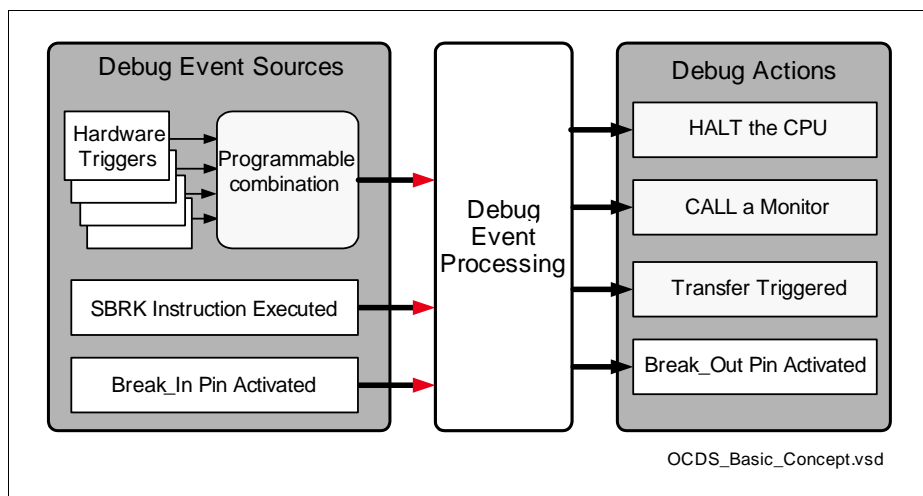


Figure 13-2 OCDS Concept: Block Diagram

13.2.1 Debug Events

The Debug Events can come from a few different sources.

Hardware Breakpoints

The Hardware Breakpoint is a debug-event, raised when a single or a combination of multiple trigger-signals are matching with the programmed conditions. The following hardware trigger sources can be used:

Table 13-1 Hardware Triggers

Trigger Source	Size
Task Identifier	16 bits
Instruction Pointer	24 bits
Data address of reads (two buses monitored)	2 × 24 bits
Data address of writes	24 bits
Data value (reads or writes)	16 bits

Software Breakpoints

A special SBRK (Software BReak) instruction is defined with opcode 0x8C00. It can be used for instance by a debugger to temporarily replace code held in RAM in order to implement Software Breakpoints. When the SBRK instruction has been decoded and it reaches the execute stage, the whole pipeline is canceled including the SBRK instruction. This implies that the next instruction will be fetched from the address the SBRK was found at.

The further behavior is dependent on how OCDS has been programmed:

- if the OCDS is enabled and the software breakpoints are also enabled, then the CPU goes into **Halt Mode**
- if the OCDS is disabled or the software breakpoints are disabled, then the Software Break Trap (SBRKTRAP) is executed - Class A Trap, number 08_H

Break Pin Input

An external debug break pin ($\overline{\text{BRKIN}}$) is provided to allow the debugger to asynchronously interrupt the processor.

13.2.2 Debug Actions

When the OCDS is enabled and a debug event is generated, one of the following actions is taken:

Triggered Transfer

One of the actions that can be specified to occur on a debug event being raised is to trigger the **Cerberus**:

- to execute a Data Transfer. This can be used in critical routines where the system cannot be interrupted to transfer a memory location
- to inject an instruction to the CPU, using this mechanism, an arbitrary instruction can be injected into the XC27x8X pipeline

Halt Mode

Upon this Action the OCDS Module sends a Break-Request to the CPU.

The CPU accepts this request, if the OCDS Break Level is higher than current CPU priority level. In case a Break-Request is accepted, the system suspends execution with halting the instruction flow.

The Halt Mode can be still interrupted by higher priority user interrupts. It then relies on the external debugger system to interrogate the target purely through reading and updating via the debug interface.

Call a Monitor

One of the possible actions to be taken when a debug event is raised is to call a Monitor Program. This quick entry to a Monitor allows a flexible debug environment to be defined which is capable of satisfying many of the requirements for efficient debugging of a real time system. In the common case the Monitor has the highest priority and can not be interrupted by any other requesting source.

It is also possible to have an Interruptible Monitor Program. In such a case safety critical code can be still served while the Monitor (Debugger) is active, which gives a maximum flexibility to the user.

Activate External Pin

This action activates the external pin BRKOUT of the **OCDS Break-Interface**. It can be used in critical routines where the system cannot be interrupted to signal to the external world that a particular event has happened. Note that the code execution timing is not affected.

13.3 Cerberus

Cerberus is the module which provides and controls all the operations necessary to interact between the external debugger (via the **Debug Interface**), the **OCDS Module** and the internal system of XC27x8X.

Features

- DAP/JTAG interface is used as control and data channel
- Generic read/write functionality (RW mode) with access to the whole address space
- Reading and writing of general-purpose registers (GPRs)
- Injection of arbitrary instructions
- External host controls all transactions
- All transactions are available at normal run time and in halt mode
- Priority of transactions can be configured
- Full support for communication between the monitor and debugger
- Optional error protection
- Tracing memory locations through transferring values to the external bus
- Analysis register for internal bus locking situations

The target application of Cerberus is to use the DAP/JTAG interface as an independent port for on-chip debug support. The external debugger can access the OCDS registers and arbitrary memory locations with the injection mechanism.

13.3.1 Functional Overview

Cerberus is operated by an external debugger across the DAP/JTAG interface. The Debugger uses Cerberus IO Instructions to perform bidirectional data-transfers. Cerberus has two main modes of operation:

Read/Write (RW) Mode

RW Mode is the most common way to operate Cerberus. This mode is used to read and write memory locations or to inject instructions into the CPU pipeline. The injection interface to the CPU is actively used in this mode.

All Cerberus IO Instructions can be used in RW mode. The access to any memory location is performed with injected instructions, as a PEC transfer.

Communication (COM) Mode

In COM mode the debugger communicates with a monitor program running on the CPU. The difference to **Read/Write (RW) Mode** is that the read or write request is not actively executed. It just sets request bits in a CPU accessible status register to signal the monitor, that the debugger wants to send or receive a value. The monitor has to poll this status register, e.g. triggered by a timer interrupt.

COM Mode is the default mode after reset. It can be used to exchange keys with the application software of a locked (RW Mode disabled) device and to unlock RW Mode only in case of matching keys.

13.4 Emulation Device

The XC27x8X can be emulated using an Emulation Device with an additional 5 pin trace interface. This interface outputs program flow trace information in the compressed MCDS (Multi-Core Debug Solution) format. For availability of such an emulator please contact your Infineon tool partner.

13.5 Boundary-Scan

The XC27x8X eases board-level analysis in the application system by providing Boundary-Scan according to the IEEE standard 1149.1. It supports testing of the interconnections between several devices mounted on a PCB.

Boundary-Scan is accomplished via the JTAG module, using standard JTAG instructions (IEEE1149.1). The Boundary-Scan chain of a device is described in a BSDL file, which is available from your Infineon contact.

Note: Some devices have the same JTAG ID, but require a different BSDL file, due to a different pad to pin bonding in the package.

*Note: For Boundary-Scan to operate properly, the JTAG interface must use the default pins. The reset value of register **DBGPRR** ensures this.*

Initialization of Boundary-Scan

The following sequence is defined to activate Boundary-Scan mode:

- Set $\overline{\text{PORST}} = 1$; $\overline{\text{TRST}} = 1$; $\overline{\text{TESTM}} = 1$
- Negative Pulse on $\overline{\text{PORST}}$
- Wait for Power Domain to startup.
- Negative pulse on $\overline{\text{TRST}}$ to reset the JTAG controller.

Now the test access port for Boundary-Scan is enabled. The Boundary-Scan test can be used for board test with instructions like PRELOAD and EXTEST.

14 Startup Configuration and Bootstrap Loading

After startup, the XC27x8X executes code out of an on-chip or off-chip program memory. The initial code source can be selected (refer to the next [Chapter 14.1](#) and [Chapter 14.3](#) to find out how) between the following options:

- **Internal Start** Mode: executes code out of the on-chip program Flash.
- **External Start** Mode: executes code out of an off-chip memory connected to the External Bus Interface.
- **Bootstrap Loading** Modes: execute code out of the on-chip program SRAM (PSRAM). This code is downloaded beforehand via a selectable serial interface.

14.1 Startup Mode Selection

After any startup the currently valid startup configuration is indicated in bitfield HWCFG of register SCU_STSTAT. The startup configurations and modes supported in XC27x8X are described in [Chapter 14.3](#).

A startup configuration can be selected basically in two ways:

1. Via an externally applied hardware configuration upon a Power-on reset
The hardware configuration is applied to the dedicated $\overline{\text{TRST}}$ -pin and to Port 10 pins (P10[6:0]).
The hardware that activates a startup configuration during reset may be simple pull resistors for systems that use this feature upon every reset. You may want to use a switchable solution (via jumpers or an external signal) for systems that only temporarily use a hardware configuration.
2. By executing the following software sequence (using SCU_SWRSTCON and SCU_RSTCON1 registers):
 - a) Write respective configuration value (refer to [Table 14-2](#) and [Table 14-3](#)) to bitfield SCU_SWRSTCON.SWCFG;
 - b) Assign desired type of reset to the software request trigger by writing into SCU_RSTCON1.SW bitfield (by default SCU_RSTCON1.SW=00_B meaning no reset generated by software request trigger)
 - c) Set Software Boot Configuration bit: SCU_SWRSTCON.SWBOOT = 1;
 - d) Trigger a software reset by activating Software Reset Request: SCU_SWRSTCON.SWRSTREQ = 1.

Additionally, several specific cases of startup configuration handling must be noted:

1. Application reset triggered by hardware request (for example WDT, ESRx) - $\overline{\text{TRST}}$ and P10 pins are not evaluated but the same startup configuration is used as after the previous reset;
2. Application or Internal Application reset triggered by software (with setting SCU_SWRSTCON.SWRSTREQ=1) - can have different consequences:

Startup Configuration and Bootstrap Loading

- a) if Software Boot Configuration is selected (SCU_SWRSTCON.SWBOOT=1) - the startup configuration (SCU_STSTAT.HWCFG) is updated from SCU_SWRSTCON.SWCFG bitfield;
 - b) otherwise - the same startup configuration is used as after the previous reset.
3. Internal Application reset triggered by hardware request - only TRST pin is evaluated (refer to [Page 14-6](#)):
- a) if TRST=0 - Internal Start from Flash is selected, no debugging is possible;
 - b) otherwise - the same startup configuration is used as after the previous reset.

14.2 Device Status after Startup

The main parameters of XC27x8X-status at the point of time when the first user instruction is executed are summarized below.

14.2.1 Registers modified by the Startup Procedure

Table 14-1 shows the XC27x8X registers which are initialized during the startup procedure with values different from their reset-content (defined into respective register-descriptions).

There are two groups of registers regarding the way they are affected by startup procedure:

1. registers initialized after any startup;
2. registers initialized after startup triggered by a power-on in DMP_1 power domain;

Note: Power-on in DMP_M domain means power-on event also in DMP_1.

The registers in **Table 14-1** are grouped in accordance to the above differentiation.

Two additional points regarding register-content after startup must be taken into account:

- The register-modifications shown in **Table 14-1** happen independently on the startup mode currently selected, which means also in [Internal Start](#) mode.
 Next to these, in other modes - [External Start](#) and [Bootstrap Loading \(Chapter 14.5, Chapter 14.6\)](#) - more registers are additionally modified during startup, as described into respective Specific Settings chapters for any of the modes.
- The values seen in some bits after startup can be affected not only by the reset procedure itself but also by other events during and even before the last startup - for example an Emergency Event can change the clock-system status.
 Therefore occasional exceptions are possible from the above values (as well as from the default register content after reset), mainly for some clock control/status flags. For more information on such special cases and their handling - refer to XC27x8X Programmer's Guide.

Startup Configuration and Bootstrap Loading

Table 14-1 XC27x8X Registers installed by the Startup Procedure

Register	Value	Comments
1. After any startup:		
TRAPDIS	039F _H	All SCU-controlled traps disabled except PET and RAT
RSTCON1	UU: 10uu:U _H	Internal Application Reset request generated by WDT
IMBCTRL	556C _H	In External or Bootstrap Loader mode with protected Flash
	A56C _H	In Internal Start mode or Flash not protected
R8..R15	XXXX	GPRs from Local Bank 1 - used by startup procedure
1A. Upon startup from Internal Flash:		
VECSEC	00C0 _H	Vector table - in Segment 192 (C0 _H), Internal Flash0
1B. Upon startup in Bootstrap Loader mode:		
VECSEC	00E0 _H	Vector table - in Segment 224 (E0 _H), Program SRAM
1C. Upon startup from external memory:		
VECSEC	0000 _H	Vector table - in Segment 0, External memory area
2. After power-on in DMP_1:		
IMBCTRH	UU: uu00:U _H	Flash access allowed with fSYS up to 80MHz
PLLCON0	0F00 _H	PLL in Normal Mode, N-divider = 16
PLLCON3	0007 _H	K2-divider = 8
SYSCON0	0002 _H	The PLL output (fPLL) used as system clock
WUOSCCON	0000 _H	Wake up Oscillator enabled with fWU approx. 500kHz
HPOSCCON	U:u0uu: UU _H	PLLSTAT.FINDIS bit will not be set in an OSCWDT emergency case
PLLOSCCON	XXXX _H	Device-specific value (chip-to-chip trimming)
EVRMCON0	0100 _H	EVR_M Control 0 register
EVR1CON0	0D00 _H	EVR_1 Control 0 register
EVR1SET15VHP	401B _H	EVR_1 Setting for 1.5V HP register
EVR1SET10V	405B _H	EVR_1 Setting for 1.0V register
EVR1SET15VLP	40DB _H	EVR_1 Setting for 1.5V LP register
PVCMCON0	2544 _H	PVC_M Control for Step 0 register
PVC1CON0	2544 _H	PVC_1 Control for Step 0 register

Startup Configuration and Bootstrap Loading

Table 14-1 XC27x8X Registers installed by the Startup Procedure

Register	Value	Comments
3A. After functional (not power-on) reset with STMEM0.SFAR=0 (f_{SYS} up to 80MHz):		
IMBCTR _H	UU: uu00:U _H	Flash access allowed with f_{SYS} up to 80MHz
3B. After functional (not power-on) reset with STMEM0.SFAR=1 (f_{SYS} above 80MHz):		
IMBCTR _H	UU: uu01:U _H	Flash access allowed with f_{SYS} up to f_{SYSMAX}

14.2.2 System Frequency after Startup

The system clock which is active when the first user instruction is executed, depends on the currently selected startup mode and the last startup trigger:

- after power-on in all modes except CAN Bootstrap Loader (**Chapter 14.6.4**) - 10MHz (nominal value) from the XC27x8X internal oscillator (doubled frequency);
- after power-on in CAN Bootstrap Loader (**Chapter 14.6.4**) - the frequency of an external crystal connected to XTAL-pins, 4MHz minimum;
- after any functional (not power-on) reset - the clock system configuration is not changed by device startup, respectively the system frequency remains as before the reset.

*Note: XC27x8X allows system frequency up to f_{SYSMAX} (refer to Data Sheet), for which a special handling is needed - refer to **Chapter 14.3.2**.*

14.2.3 Watchdog Timer handling

The Watchdog Timer (WDT) in XC27x8X is always enabled by the startup procedure and configured to generate Internal Application Reset.

Therefore, the user software must:

- if WDT-usage is foreseen by the code - service it for a first time within approx. 65500 system clock cycles after startup;
- otherwise - disable it within the same time frame as above but before to execute End of Init (EINIT).

The reset requested by WDT serves as response to a device malfunction, due to which malfunction user software can not be anymore executed correctly - respectively the WDT is not regularly served. This reset causes a new device startup followed by user software restart.

The Internal Application Reset - default for WDT - affects not all the modules in XC27x8X - refer to "Module Reset Behavior" in SCU Chapter. The unaffected modules do not change their state, so if this state is "wrong" it will not be recovered to "correct" due to Internal Application Reset, also when triggered by WDT. Therefore, the default

Startup Configuration and Bootstrap Loading

WDT configuration and usage can resolve well purely software malfunction but not other failures - for example in clock- or power- system.

One reset-request which puts all the XC27x8X modules into a known - and correctly functioning - initial state is from PORST-pin. Therefore, if an application requires that correct device restart upon WDT reset is guaranteed, the implementation must be done according to the next [Chapter 14.2.3.1](#).

14.2.3.1 Triggering Power-on Reset by WDT

This feature requires that $\overline{\text{ESRx}}$ pin is dedicated to it, e.g. not available for another functionality.

The following must be done by the user to have power-on reset triggered by WDT:

- in hardware: tie the selected $\overline{\text{ESRx}}$ ($x=1,2$) pin to $\overline{\text{PORST}}$ pin of the device;
- in software: at its very beginning, install 1110_B into bits[3:0] of the respective ESRCFGx register ($x=1,2$).

Note: Keep the WDT reset configuration as installed by startup procedure - Internal Application Reset.

With the above preparation, any Internal Application Reset - including triggered by WDT - will drive the selected $\overline{\text{ESRx}}$ pin low so leading to power-on and a next device restart.

Attention: When using this solution, Internal Application reset is no more available as separate reset type. Respectively upon this reset all the device resources will be initialized as upon power-on and any previous information will be lost.

Therefore, when controlling this feature by WDT do not assign Internal Application Reset to any other trigger if prevention of previous information/status is needed.

For additional information on this feature - refer to Application Note AP16146 .

14.2.4 Startup Error state

To prevent possible negative consequences for the device and/or the system, upon unrecoverable error during startup XC27x8X is put onto a stable, passive and neutral to the external world state - power-save mode with DMP_1 shut down and DMP_M powered with 1V.

This state can be exited with power-on reset only.

14.3 Supported Startup Modes and Options

XC27x8X supports variety of startup modes, allowing the user to make selections in three aspects:

Startup Configuration and Bootstrap Loading

- main functionality - where from the user code will be started (on-chip Flash, PSRAM, external memory);
- optionally - a way for initial code-downloading into PSRAM before to start it:
 - from an external host via a communication interface - UART, CAN, SSC;
- debug-related - either debugging will be possible, and if Yes - which debug-interface to use (JTAG, DAP, selectable pin-assignments).

Following from the above differentiation, the startup modes in XC27x8X are divided into several groups, described in [Chapter 14.3.1](#), [Chapter 14.3.2](#) and [Chapter 14.3.3](#).

14.3.1 Basic Startup Modes

These modes (refer to [Table 14-2](#)) have no debug support and no special features.

Table 14-2 Basic XC27x8X Startup Modes

Startup Mode	STSTAT.HWCFG Value ¹⁾	Configuration pins ²⁾							
		TRST	P10 [6 : 0]						
Internal Start from Flash	00 _H	0	x	x	x	x	x	x	x
UART Bootloader 2.x ³⁾	02 _H	1	x	x	x	x	0	1	0
UART Bootloader 7.x ⁴⁾	06 _H	1	x	x	x	x	1	1	0
SSC Bootloader	09 _H	1	x	x	x	1	0	0	1
CAN Bootloader	0D _H	1	x	x	x	1	1	0	1
UART Enhanced Bootloader 2.x ³⁾	10 _H	1	0	0	1	0	0	0	0
External Start	70 _H	1	1	1	1	0	0	0	0

1) Bitfield HWCFG can be loaded from Port 10 or from bitfield SWCFG in register SWRSTCON.

2) x means that the level on the corresponding pin is irrelevant.

3) 2.x means: TxD (transmit data) at P2.3 pin, RxD (receive data) at P2.4 pin.

4) 7.x means: TxD (transmit data) at P7.3 pin, RxD (receive data) at P7.4 pin.

The XC27x8X functionality in different modes - Internal start, External start, Bootstrap loading - is described further in [Chapter 14.4](#), [Chapter 14.5](#), [Chapter 14.6](#) respectively.

0-pin Configuration

This is a new feature for XC27x8X, meaning usage of no General-purpose Input-output (GPIO) pins - including no assignment of any alternate function to a pin - to select the startup configuration which is supposed to the most used one - Internal Start from Flash.

One dedicated pin - $\overline{\text{TRST}}$ - is used as a checkpoint, as follows:

- $\overline{\text{TRST}}=0$ during reset - no other pins (also from Port 10) are evaluated, the user code is started from Internal Flash memory - refer to the first row in [Table 14-2](#);

Startup Configuration and Bootstrap Loading

- $\overline{\text{TRST}}=1$ during reset - some of the Port 10 pins are evaluated to determine the further device-functioning. The number of P10 pins used for that purpose varies from 3 up to 7- refer to [Table 14-2](#) and [Table 14-3](#).

14.3.2 Startup Modes with Debug Support

These startup selections (refer to [Table 14-3](#)) lead to user-code start either from Internal Flash or from External memory. So from functional point of view they are similar to two from the [Basic Startup Modes](#) in [Table 14-2](#), but additionally these selections allow an external tool (debugger) to be connected and used during the development process.

Table 14-3 XC27x8X Startup Mode Configurations with debug support

Startup Mode	Debug Interface	STSTAT.HWCFG Value ¹⁾	CFG pins P10 [6:0] ²⁾ TRST=1							
Internal Start from Flash	JTAG pos.B	03 _H	x	x	x	x	0	1	1	
	DAP pos.1	04 _H	x	x	x	x	1	0	0	
	from Flash ³⁾	07 _H	x	x	x	x	1	1	1	
	DAP pos.0	01 _H	x	x	x	0	0	0	1	
	DAP pos.2	05 _H	x	x	x	0	1	0	1	
	JTAG pos.C	40 _H	1	0	0	0	0	0	0	
	JTAG pos.D	50 _H	1	0	1	0	0	0	0	
External Start	from Flash ³⁾	60 _H	1	1	0	0	0	0	0	

1) Bitfield HWCFG can be loaded from Port 10 or from bitfield SWCFG in register SWRSTCON.

2) x means that the level on the corresponding pin is irrelevant.

3) A defined location in Flash (C0'01F0_H) must contain a value (2 Bytes) for DBGPRR register and the next word-location (C0'01F2_H) must contain the inverse value.

From the 16-bit value in Flash the four most-significant bits are don't care - they are handled by the startup procedure itself.

If the inverse-condition does not match - the value is considered as invalid and JTAG pins at position A are configured by default.

The variety of startup configurations ([Table 14-3](#)) in this case serve to select the type (DAP or JTAG) and pin-location of the debug interface which will be enabled. Besides of this selection - done either via P10-pins or by SWRSTCON.HWCFG-bitfield - two basic conditions exist for debug-interface handling:

- debug interface configuration is a part of the complete device startup configuration. Therefore debug interface enabling/disabling/(re)configuration takes place only when the startup configuration (e.g. the startup mode selection) is updated in some of the ways described in [Chapter 14.1](#).

Startup Configuration and Bootstrap Loading

For example, upon an application reset triggered by hardware source (let say WDT) the debug interface will not be touched.

- debug interface will be always disabled, if Internal Start is selected and the on-chip Flash is protected

The exact meaning - interface types and pin-assignments - of different debug interface selections is shown in [Table 14-4](#). The last column of this table shows the value, which must be written into Flash location C0 01F0_H, if Debug Interface Configuration from Flash has been selected as startup option (refer to [Table 14-3](#)).

Table 14-4 Debug-selections in XC27x8X: interface types and pin assignments

Debug Interface		Pins used for Debugging:		DBGPRR value in Flash addr. C0 01F0 _H
Type	Position	main interface (obligatory)	BRKIN (optional)	
DAP	pos.0	P2.9, P7.0	P5.10	1000 _H
	pos.1	P10.9, P10.12	P10.8	1155 _H
	pos.2	P7.0, P7.4	P7.1	12AA _H
JTAG	pos.A	P2.9, P5.2, P5.4, P7.0	P5.10	1800 _H
	pos.B	P10.9, P10.10, P10.11, P10.12	P10.8	1955 _H
	pos.C	P7.0, P7.2, P7.3, P7.4	P7.1	1AAA _H
	pos.D	P8.3, P8.4, P8.5, P10.12	P8.6	1BFF _H
not available	---	---	---	0000 _H

There are two types of interface signals/pins related to debugging:

Main Debug Interface

These are 2 (in case of DAP) or 4 (in case of JTAG) pins listed in the third column of [Table 14-4](#).

If debugging is enabled, these pins are always assigned to the debug-interface, therefore the application software must never use any of them.

Optional Break Interface

The Break Interface of XC27x8X Debug System includes two signals: BRKIN and BRKOUT.

The usage of this interface is optional, also selectively either only one out of the two signals or both of them can be utilized.

Startup Configuration and Bootstrap Loading

The Break Interface usage requires additional preparation which will be done - when requested - by the external debugger once the main interface is available.

As long as this preparation and the activation of "Break-In"/"Break-Out" feature has not happened, the respective pin(s) selected to host (potentially) BRKIN/BRKOUT-signal(s) can be still used for other functionality by the application software.

The two Break-signals/pins are handled some differently to each other:

- BRKIN - the exact pin which will be used (in case) for this purpose is determined uniquely by the startup selection - refer to the BRKIN-column in [Table 14-4](#).
- BRKOUT - no pin-selection for this signal is done during startup.
Few pins are potentially available for BRKOUT-selection - done by the external tool before to activate the "Break-Out" feature:
 - P6.0;
 - P10.11 - can not be used, if JTAG interface at position B is selected.

14.3.3 Special Startup Features

XC27x8X supports some special features, which allow the user software to influence the device startup, providing additional functionality next to the above (in [Chapter 14.3.1](#) and [Chapter 14.3.2](#)) described.

Attention: *The correct usage of these features requires good and detailed understanding of the XC27x8X structure, behavior and programming. The special startup features are dedicated to advanced users, being familiar with device as a whole and especially with the System Control Unit - both as hardware (described in SCU Chapter of this User Manual) and how to control it properly by software (described in the XC27x8X Programmer's Guide).*

14.3.3.1 Supplementary Startup Information from/to the User

The special startup features require/provide additional information from/to the application software, using a dedicated register inside the System Control Unit - STMEM0.

STMEM0 Register

The SCU_STMEM0 register is located in DMP_M power-supply domain and is Security-protected.

The following startup information can be exchanged with application software using this register:

- the user software can influence the next device startup by writing into STMEM0 bits[15:5]
The supported features are described in [Chapter 14.3.3.2](#), [Chapter 14.3.3.3](#).
- if STMEM0[4]=0 after startup - this startup has been triggered by a Functional (i.e. Application or Internal Application) Reset;
In such a case the emergency-status flags indicated in SCU_SYSCON0 bits[15:12] upon device startup can be read by user software from SCU_STMEM0 bits[3:0] as follows:
 - bit[0] - OSCWDT Emergency Event Source status
 - bit[1] - VCOLCK Emergency Event Source status
 - bit[2] - PVC1 Emergency Event Source status
 - bit[3] - Clock Select status
- if STMEM0[4]=1 after startup - this startup has been triggered by a Power-On;
In such a case, additional information is provided by SCU_STMEM0[3] bit:
 - STMEM0[3]=0 - Power-On in DMP_1 domain only
 - STMEM0[3]=1 - Power-On in both DMP_1 and DMP_M domains

Startup Configuration and Bootstrap Loading

STMEM0

Startup Memory 0 Register

ESFR (F0A0_H/50_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USSET	0	RINDP	RINDS	RINPS	0				0	SFAR			STSIND		
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Typ	Description
STSIND	[4:0]	rw	Startup Status Indication to the user: <i>Note: The values not described here are reserved.</i> 0xxx _B Functional reset - bits[3:0] show status flags (refer to the text description) 10000 _B Power-on in DMP_1 domain only 11000 _B Power-on in DMP_M and DMP_1 domains 1x1xx _B Reserved 1xx1x _B Reserved 1xxx1 _B Reserved
SFAR	5	rw	System Frequency upon Application Reset: 0 _B up to 80MHz 1 _B above 80MHz
0	6,[10:7]	rw	Reserved , must be written with reset value 0
RINPS	11	rw	Initialization of the PSRAM: 0 _B not requested 1 _B will be performed upon startup
RINDS	12	rw	Initialization of the DSRAM: 0 _B not requested 1 _B will be performed upon startup
RINDP	13	rw	Initialization of the DPRAM: 0 _B not requested 1 _B will be performed upon startup
0	14	rw	Reserved , must be written with reset value 0
USSET	15	rw	RAM Initialization upon startup: 0 _B not requested 1 _B requested in STMEM0 [13:11]

14.3.3.2 Support for running at system frequency above 80MHz

XC27x8X can run at system frequency up to f_{SYSMAX} (refer to data Sheet) - faster than other devices from the family for which devices the upper limit is 80MHz.

To achieve this higher frequency, Flash modules need to be configured, which configuration can be done in two ways:

- by the startup procedure when executed upon a functional (not power-on) reset with **STMEM0.SFAR=1**;
- by a special configuration function (user software) implemented in accordance to the XC27x8X Programmer's Guide.

In any case, before to increase the system frequency above 80MHz, the **STMEM0.SFAR** bit must be set to 1.

Attention: *Immediately after a power-on reset, the clock-system is always configured to 10MHz and the device is ready to run at frequency up to 80MHz but not above.*

14.3.3.3 Preparing to activate Memory Content Protection

XC27x8X supports two mechanisms for Memory Content protection: ECC (Error Correction Code) and Parity, both are disabled by default.

Any of these mechanisms can be only activated by the user, using the sequence shown at **Figure 14-1**. The processing according to this sequence includes:

- upon power-on of the device (indicated by **STMEM0[4]=1**, **STMEM0[15]** will be 0 in this case) - RAM initialization is needed:
 - optionally - if the application will run with system clock faster than 10MHz (system frequency after power-on) - the clock reconfiguration can be done still here to use increased speed for a faster RAM initialization;
 - if parity will be used for some memory - write 1 into the respective bit(s) of SCU_MCHKCON register (by default ECC is the selected protection type);
 - install request for RAMs initialization by setting **STMEM0[15:11]=10111_B**;
It is also possible to set selectively only some of the bits[13:11] corresponding to the memories in which the Content Protection will be activated (refer to **STMEM0**-description and **Figure 14-1**). This will not bring too much - in sense of a faster startup - because all the memories are initialized in parallel and the time-variation if processing one only or all the RAMs will be not so big.
 - trigger an application reset to cause a new device startup
During this new device startup the RAMs are initialized as requested in **STMEM0[13:11]**.
- if **STMEM0[15]=1** after startup - meaning RAMs have been just initialized:
 - read one location from any initialized memory to assure correct initial state of the read-control logic

Startup Configuration and Bootstrap Loading

- assure error-flags are reset - clear SCU_ECCSTAT (by writing ones to SCU_ECCCLRSTAT) if ECC used or SCU_PECON (by writing one to itself) if parity used
- enable ECC (in SCU_ECCCON register) or parity (in SCU_PECON and SCU_PMTSR.PESEN) as required by the application
- enable ECC- or parity- traps in SCU_TRAPDIS register if required by the application

Note: Depending on the application structure this can be done either here or later as part of the further system initialization.

- clear RAM-initialization request - **STMEM0**[15:11]=00000_B;
- continue with further system initialization (if any) and starting the application
- if **STMEM0**[15]=0 after functional reset (not power-on) - RAM initialization is not needed and the request is not active:
 - enable ECC/parity as required by the application - this is needed because some control registers are reset upon any startup;
 - continue with further system initialization (if any) and starting the application.

The read-operations from initialized memories produce no errors, the data delivered is:

- if ECC is active - 0600_H;
- if parity is active - 3000_H.

Startup Configuration and Bootstrap Loading

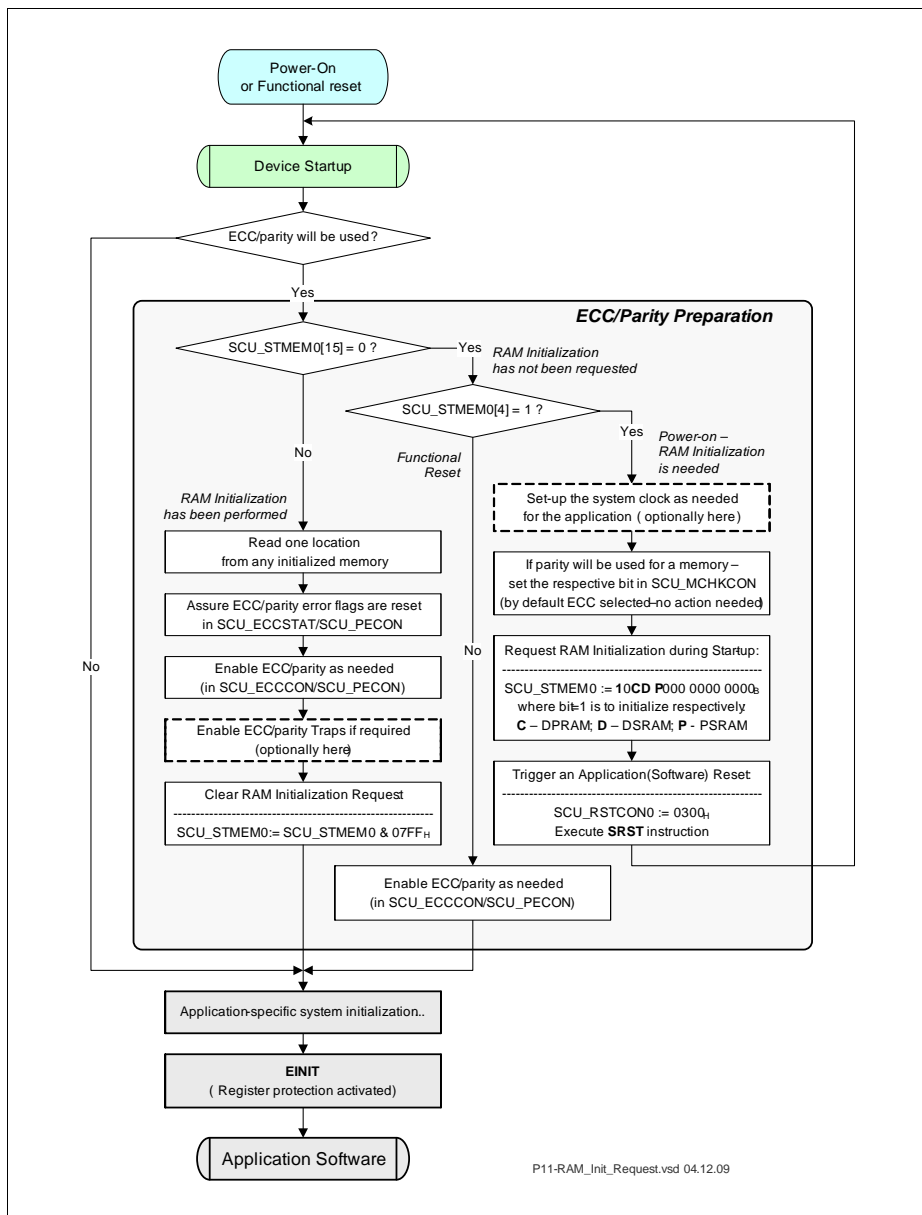


Figure 14-1 Software sequence to prepare ECC/Parity usage

Startup Configuration and Bootstrap Loading

14.4 Internal Start

When internal start mode is configured, the XC27x8X immediately begins executing code out of the on-chip Flash memory (first instruction from location C0'0000_H).

Because internal start mode without debug-support is expected to be the configuration used in most cases, this mode can be selected by pulling low the dedicated (e.g. not available for application-purposes) $\overline{\text{TRST}}$ -pin only - so-called **0-pin Configuration**.

If debug-support is needed - additional configuration options are available, refer to **Chapter 14.3.2**.

Note: A read-protected Flash is readable for applications started in Internal mode without disabling the protection.

14.5 External Start

When external start mode is configured, the XC27x8X begins executing code out of an off-chip memory (first instruction from location 00'0000_H), connected to the XC27x8X's external bus interface.

The External Bus Controller is adjusted to the employed external memory by evaluating additional configuration pins.

Seven pins of P10 are used to select the EBC mode (P10.[10:8]), the address width (P10.[12:11]), and the number of chip select lines (P10.[14:13]). The following tables summarize the available options.

Startup Configuration and Bootstrap Loading

Table 14-5 EBC Configuration: EBC Mode

EBC Startup Mode	Cfg. Pins P10[10:8]			Pins Used by the EBC (see the next Tables for further pins used)
8-Bit Data, Multiplexed	0	0	0	P2.0 ... P2.2, P10.0 ... P10.15
8-Bit Data, Demultiplexed	0	0	1	P0.0 ... P0.7, P1.0 ... P1.7, P2.0 ... P2.2, P10.0 ... P10.7, P10.13, P10.14
16-Bit Data, MUX, $\overline{\text{BHE}}$ mode	0	1	0	P2.0 ... P2.2, P2.11, P10.0 ... P10.15
16-Bit Data, MUX, $\overline{\text{WRH}}$ mode	0	1	1	P2.0 ... P2.2, P2.11, P10.0 ... P10.15
16-Bit Data, DeMUX, $\overline{\text{BHE}}$ mode, A0	1	0	0	P0.0 ... P0.7, P1.0 ... P1.7, P2.0 ... P2.2, P2.11, P10.0 ... P10.14
16-Bit Data, DeMUX, $\overline{\text{WRH}}$ mode, A0	1	0	1	P0.0 ... P0.7, P1.0 ... P1.7, P2.0 ... P2.2, P2.11, P10.0 ... P10.14
16-Bit Data, DeMUX, $\overline{\text{BHE}}$ mode, A1	1	1	0	P0.1 ... P0.7, P1.0 ... P1.7, P2.0 ... P2.2, P2.11, P10.0 ... P10.14
16-Bit Data, DeMUX, $\overline{\text{WRH}}$ mode, A1	1	1	1	P0.1 ... P0.7, P1.0 ... P1.7, P2.0 ... P2.2, P2.11, P10.0 ... P10.14

Table 14-6 EBC Configuration: Address Width

Available Address Lines	Cfg. Pins P10[12:11]		Additional Address Pins
A15 ... A0	0	0	None
A17 ... A0	0	1	P2.3, P2.4
A19 ... A0	1	0	P2.3 ... P2.6
A23 ... A0	1	1	P2.3 ... P2.10

Table 14-7 EBC Configuration: Chip Select Lines

Available Chip Select Lines	Cfg. Pins P10[14:13]		Used Pins
$\overline{\text{CS0}} \dots \overline{\text{CS4}}$	0	0	P4.0 ... P4.4
$\overline{\text{CS0}}$	0	1	P4.0
$\overline{\text{CS0}} \dots \overline{\text{CS1}}$	1	0	P4.0, P4.1
None	1	1	None

Startup Configuration and Bootstrap Loading

14.5.1 Specific Settings

When the XC27x8X has entered External Start mode, the configuration is automatically set according to [Table 14-8](#) and [Table 14-9](#).

Note, that the startup procedure does not configure any address window within ADDRSELx registers. Therefore, even if some CS signal is configured (refer to [Table 14-7](#)), the startup procedure only makes the proper settings to assure the adequate pin-functionality in regard to the selected EBC mode. The user software must take care:

- to configure the address window (in ADDRSELx register) for the $\overline{\text{CSx}}$ pin(s) which will be used;
- to enable those pins by setting FCONCSx.ENCS.

Table 14-8 External start mode-Specific State in EBC Registers

Configuration at P10[10:8]	EBCMOD0 [15:8]	EBCMOD1	FCONCSx ¹⁾	Comment (EBC Mode)
000 _B	50 _H	001F _H	0011 _H	8-Bit Multiplexed
001 _B	70 _H	0040 _H	0001 _H	8-Bit Demultiplexed
010 _B	40 _H	0000 _H	0031 _H	16-Bit MUX, $\overline{\text{BHE}}$
011 _B	48 _H	0000 _H	0031 _H	16-Bit MUX, $\overline{\text{WRH}}$
100 _B	60 _H	0000 _H	0021 _H	16-Bit DeMUX, $\overline{\text{BHE}}$, A0
101 _B	68 _H	0000 _H	0021 _H	16-Bit DeMUX, $\overline{\text{WRH}}$, A0
110 _B	60 _H	0010 _H	0021 _H	16-Bit DeMUX, $\overline{\text{BHE}}$, A1
111 _B	68 _H	0010 _H	0021 _H	16-Bit DeMUX, $\overline{\text{WRH}}$, A1

1) Which FCONCSx registers are affected is dependant on the configuration at P10[14:13] as follows:

11_B or 01_B - FCONCS0 is affected

10_B - FCONCS0 and FCONCS1 are affected

00_B - FCONCS0..FCONCS4 are affected

The other (unaffected) FCONCS registers retain their default values - refer to the EBC Chapter of this Manual.

Table 14-9 External start mode-Specific State in EBCMOD0[7:0]

Configuration at P10[14:13]	Configuration at P10[12:11]			
	00B (0 Segm.)	01B (2 Segm.)	10B (4 Segm.)	11B (8 Segm.)
00 _B (5 CS)	50 _H	52 _H	54 _H	58 _H
01 _B (1 CS)	10 _H	12 _H	14 _H	18 _H
10 _B (2 CS)	20 _H	22 _H	24 _H	28 _H
11 _B (0 CS)	00 _H	02 _H	04 _H	08 _H

14.6 Bootstrap Loading

Bootstrap Loading is the technique of transferring code to the XC27x8X via a certain interface (usually serial) before the regular code execution out of non-volatile program memory commences. Instead, the XC27x8X executes the previously received code.

This boot-code may be complete (e.g. temporary software for testing or calibration), amend existing code in non-volatile program memory (e.g. with product-specific data or routines), or load additional code (e.g. using higher or more secure protocols). A possible application for bootstrap loading is the programming of virgin Flash memory at the end of a production line, with no external memory or internal Flash required for the initialization code.

The BSL mechanism may be used for standard system startup as well as only for special occasions like system maintenance (firmware update) or end-of-line programming or testing.

The XC27x8X supports bootstrap loading using several protocols/modes:

- Standard UART protocol, loading 32 bytes (see [Section 14.6.2.1](#))
- UART protocol, Enhanced bootstrap loader transferring arbitrary number of bytes (see [Section 14.6.2.2](#))
- Synchronous serial protocol (see [Section 14.6.3](#))
- CAN protocol (see [Section 14.6.4](#))

For a summary of these modes, see also [Table 14-16](#).

14.6.1 General Functionality

Even though each bootstrap loader has its particular functionality, the general handling is the same for all of them.

Entering a Bootstrap Loader

Bootstrap loaders are enabled by selecting a specific startup configuration (see [Section 14.1](#)).

The required configuration patterns are described in [Table 14-16](#) for the bootstrap loaders, and are summarized in [Table 14-2](#).

Startup Configuration and Bootstrap Loading**Loading the Startup Code**

After establishing communication, the BSL enters a loop to receive the respective number of bytes. These bytes are stored sequentially into the on-chip PSRAM, starting at location E0'0000_H. To execute the loaded code the BSL then points register VECSEG to location E0'0000_H, i.e. the first loaded instruction, and then jumps to this instruction.

The loaded code may be the final application code or another, more sophisticated, loader routine that adds a transmission protocol to enhance the integrity of the loaded code or data. It may also contain a code sequence to change the system configuration and enable the bus interface to store the received data into external memory.

This process may go through several iterations or may directly execute the final application.

Exiting Bootstrap Loader Mode

The watchdog timer and the debug system are disabled as long as the Bootstrap loader is active. Watchdog timer and debug system are released automatically when the BSL terminates after having received the last byte from the host.

If 2nd level loaders are used, the loader routine should deactivate the watchdog timer via instruction DISWDT to allow for an extended download period.

The XC27x8X will start executing out of user memory as externally configured after a non-BSL reset .

Interface to the Host

The bootstrap loader communicates with the external host over a predefined set of interface pins. These interface pins are automatically enabled and controlled by the bootstrap loader. The host must connect to these predefined interface pins.

Table 14-16 indicates the interface pins that are used in each bootstrap loader mode.

14.6.2 Bootstrap Loaders using UART Protocol

XC27x8X users have different possibilities to download code/data in which the communication is based on UART (Universal Asynchronous Receiver and Transmitter) protocol.

14.6.2.1 Standard UART Bootstrap Loader

The standard UART bootstrap loader transfers program code/data via channel 0 of USIC0 (U0C0) into the PSRAM. The U0C0 receiver is only enabled after the identification byte has been transmitted. A half duplex connection to the host is, therefore, sufficient to feed the BSL.

Data is transferred from the external host to the XC27x8X using asynchronous eight-bit data frames without parity (1 start bit, 1 stop bit). The number of data bytes to be received in standard UART boot mode is fixed to 32 bytes, which allows up to 16 two-byte instructions.

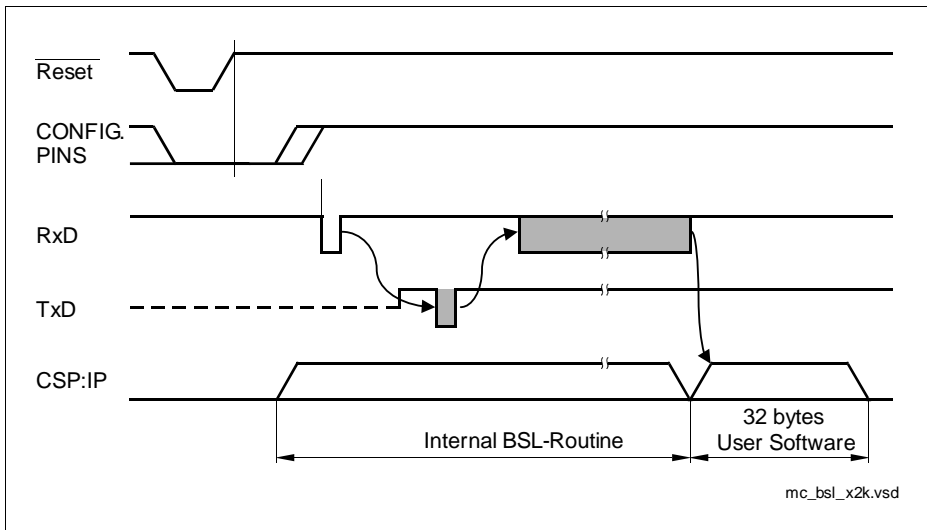


Figure 14-2 Bootstrap Loader Sequence

The XC27x8X scans the RxD line to receive a zero byte after entering UART BSL mode and the respective initialization. The zero byte is considered as containing one start bit, eight 0 data bits and one stop bit. From the duration of this zero byte it calculates the corresponding baudrate factor with respect to the current CPU clock, initializes the serial interface U0C0 accordingly and switches pin TxD to output. Using this baudrate, an identification byte (D5_H) is returned to the host that provides the loaded data.

Startup Configuration and Bootstrap Loading

Once the identification byte is transmitted, the BSL enters a loop to receive 32 bytes via U0C0. These bytes are stored sequentially into locations E0'0000_H through E0'001F_H of the internal PSRAM and then executed.

Note: For loading more code, two possibilities exist:

- via a 2nd-level loader - see below
- using the **Enhanced UART Bootstrap Loader** - refer to **Section 14.6.2.2**

Second Level Bootloader

Most probably the initially loaded routine will load additional code or data, as an average application is likely to require substantially more instructions than could fit into 32 bytes. This second receive loop may directly use the pre-initialized interface U0C0 to receive data and store it to arbitrary user-defined locations.

The example code below shows how to fit such a 2nd-level loader into the available 32 bytes. This is possible due to the pre-initialized serial channel and the pre-set registers (see **Table 14-10**).

;Example for Secondary UART Bootstrap Loader Routine

```

;-----
TargetStart LIT  '0E00020H'           ;Definition of target area:
TargetEnd   LIT  '0E001FFH'           ;480 bytes in this example
StartOfCode LIT  '0E00100H'           ;Continue executing here...
                                           ;...after download

Level2Loader:
    DISWDT                               ;No WDT for further download
    MOV     DPP0,#(PAG TargetStart)
    MOV     R10, #(DPP0:TargetStart);Set pointer to target area

Level2MainLoop:
    MOV     [R1],R3                      ;Clear RIF for new byte

Level2RecLoop:
    MOV     R4, [R0]                     ;Access PSR
    JNB     R4.14,Level2RecLoop          ;Wait for RIF
    MOVB    [R10],[R2]                   ;Copy new byte to target
    CMPI1   R10, #POF (TargetEnd);All bytes received??
    JMPR    cc_NE,Level2MainLoop        ;Repeat for complete area

Level2Terminate:
    JMPS    SEG StartOfCode, SOF StartOfCode

```

Startup Configuration and Bootstrap Loading

Specific Settings

The following configuration is automatically set when the XC27x8X has entered Standard UART BSL mode:

Table 14-10 Standard UART BSL-Specific State

Item	Value	Comments
U0C0_CCR	0002 _H	ASC mode selected for USIC0 Channel 0
U0C0_PCRL	0401 _H	1 stop bit, three RxD-samples at point 4
U0C0_SCTRL	0002 _H	Passive data level = 1
U0C0_SCTRH	0707 _H	8 data bits
U0C0_FDRL	43FF _H	Normal divider mode 1:1 selected
U0C0_BRGH	0XXX _H	Measured PDIV value (zero-byte) in bits[9:0]
U0C0_BRGL	1C00 _H	Normal mode, FDIV, 8 clocks/bit
U0C0_DX0CR	0003 _H	Data input selection
DPP1	0081 _H	Points to USIC0 base address ¹⁾
R0	4044 _H	Pointer to U0C0_PSR ¹⁾
R1	4048 _H	Pointer to U0C0_PSCR ¹⁾
R2	405C _H	Pointer to U0C0_RBUF ¹⁾
R3	4000 _H	Mask to clear RIF ¹⁾
In Bootloader 7.x mode:		
P7_IOCRO3	00B0 _H	P7.3 is push/pull output (TxD)
P7_IOCRO4	0020 _H	P7.4 is input with pull-up (RxD)
In Bootloader 2.x mode:		
P2_IOCRO3	00B0 _H	P2.3 is push/pull output (TxD)
P2_IOCRO4	0020 _H	P2.4 is input with pull-up (RxD)

1) This register setting is provided for a 2nd-level loader routine (see at [Page 14-21](#)).

The identification byte identifies the device to be booted. The following codes are defined:

55_H: 8xC166.

A5_H: Previous versions of the C167 (obsolete).

B5_H: Previous versions of the C165.

C5_H: C167 derivatives.

D5_H: All devices equipped with identification registers (including the XC27x8X).

Startup Configuration and Bootstrap Loading

Note: The identification byte $D5_H$ does not directly identify a specific derivative. This information can, in this case, be obtained from the identification registers.

14.6.2.2 Enhanced UART Bootstrap Loader

The enhanced UART bootstrap loader transfers program code/data via Channel 0 of USIC0 Module (U0C0) into PSRAM.

Data is transferred from the external host to the XC27x8X using asynchronous eight-bit data frames without parity (1 start bit, 1 stop bit). The length of the code/data is not fixed as in the **Standard UART Bootstrap Loader** but can be arbitrary up to the PSRAM total size minus 256 bytes. Also the code execution can start from arbitrary PSRAM address, as well as the initial baudrate can be changed - e.g. increased for faster transfer of long code/data blocks.

The initial steps of this bootloader are the same as of the **Standard UART Bootstrap Loader**. XC27x8X first scans the Rx_D line to receive a zero byte, i.e. one start bit, eight 0 data bits and one stop bit. From the duration of this zero byte it calculates the corresponding baudrate factor with respect to the current CPU clock, initializes the serial interface U0C0 accordingly and switches pin Tx_D to output. Using this baudrate, an identification byte (DA_H) is returned to the host.

The next steps in this mode are to process the so-called Bootloader Header as follows:

1. XC27x8X sends the current PDIV divider from U0C0_BRGH register - the 10-bit value is sent in 2 bytes

Note: In this bootloader, the multi-byte values are sent in high-to-low order.

2. XC27x8X receives and sends back to the host a Header_Code (1B)
3. XC27x8X receives and sends back to the host number of bytes to be transferred Code_Length (3B)
4. XC27x8X receives and sends back to the host the start address STADD for code-execution (3B)
 - the segment address (highest STADD byte) must equal $E0_H$ for XC27x8X
5. XC27x8X receives and sends back to the host a value for PDIV divider (2B, bits[9:0] effective only)
 - if the new value is different from the current - the new one is written into U0C0_BRGH register and a zero confirmation byte is sent back to the host with baudrate already changed
6. XC27x8X receives and sends back to the host a Trailer_Code (1B)
 - a) if both the Header_Code and Trailer_Code are equal to the XC27x8X identification byte (DA_H) - the Bootloader sends to the Host a zero byte and continues further;
 - b) if the above condition is not true - the Bootloader sends an identification byte (DA_H) to the host and restarts Header processing again from point 1.

Startup Configuration and Bootstrap Loading

Once the Header is successfully processed according to the above steps, the Bootstrap loader receives Code_Length bytes and stores them sequentially starting from the beginning of PSRAM at address E0'0000_H.

Attention: The user must care, that the number of Bytes sent is not bigger than available in the device PSRAM minus 256 and does not exceed 65280.

The Bootstrap loader starts code-execution after the last byte is received and stored. The execution is started from address STADD as received within the header.

Specific Settings

The following configuration is automatically set when the XC27x8X has entered Enhanced UART BSL mode:

Table 14-11 Enhanced UART BSL-Specific State

Item	Value	Comments
U0C0_CCR	0002 _H	ASC mode selected for USIC0 Channel 0
U0C0_PCRL	0401 _H	1 stop bit, three RxD-samples at point 4
U0C0_SCTRL	0002 _H	Passive data level = 1
U0C0_SCTRH	0707 _H	8 data bits
U0C0_FDRL	43FF _H	Normal divider mode 1:1 selected
U0C0_BRGH	0XXX _H	PDIV-value as sent by the host inside header
U0C0_BRGL	1C00 _H	Normal mode, FDIV, 8 clocks/bit
U0C0_DX0CR	0003 _H	Data input selection
P2_IOCRO3	00B0 _H	P2.3 is push/pull output (TxD)
P2_IOCRO4	0020 _H	P2.4 is input with pull-up (RxD)

The identification byte identifies the device to be booted. XC27x8X is the first microcontroller family supporting Enhanced UART BSL mode, the code defined for it is DA_H.

Note: The identification byte does not directly identify a specific derivative. This information can, in this case, be obtained from the identification registers.

14.6.2.3 Choosing the Baudrate for the BSL

The calculation of the serial baudrate for U0C0 from the length of the first zero byte that is received, allows the operation of the bootstrap loader of the XC27x8X with a wide range of baudrates. However, the upper and lower limits have to be kept, in order to ensure proper data transfer.

The XC27x8X uses bitfield PDIV to measure the length of the initial zero byte. The quantization uncertainty of this measurement implies the deviation from the real baudrate.

For a correct data transfer from the host to the XC27x8X the maximum deviation between the internal initialized baudrate for U0C0 and the real baudrate of the host should be below 2.5%. The deviation (F_B , in percent) between host baudrate and XC27x8X baudrate can be calculated via [Equation \(14.1\)](#):

$$F_B = \left| \frac{B_{Contr} - B_{Host}}{B_{Contr}} \right| \times 100\% \quad F_B \leq 2.5\% \quad (14.1)$$

Note: Function (F_B) does not consider the tolerances of oscillators and other devices supporting the serial communication.

This baudrate deviation is a nonlinear function depending on the system clock and the baudrate of the host. The maxima of the function (F_B) increase with the host baudrate due to the smaller baudrate prescaler factors and the implied higher quantization error (see [Figure 14-3](#)).

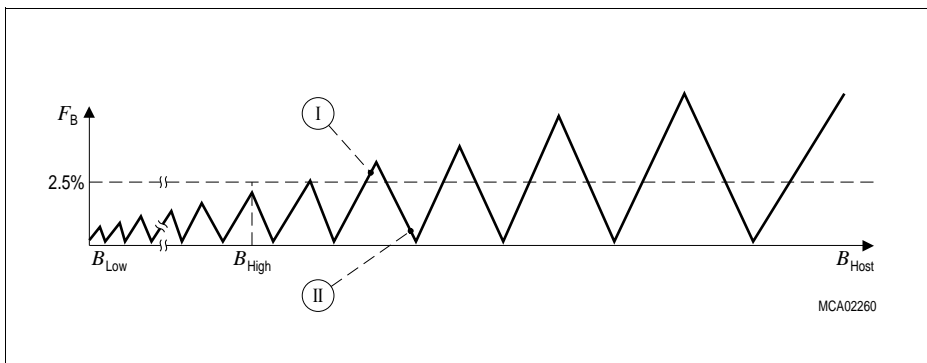


Figure 14-3 Baudrate Deviation between Host and XC27x8X

Startup Configuration and Bootstrap Loading

The minimum baudrate (B_{Low} in [Figure 14-3](#)) is determined by the maximum count capacity of bitfield PDIV, when measuring the zero byte, i.e. it depends on the system clock. The minimum baudrate is obtained by using the maximum PDIV count 2^{10} in the baudrate formula. Baudrates below B_{Low} would cause PDIV to overflow. In this case U0C0 cannot be initialized properly and the communication with the external host is likely to fail.

The maximum baudrate (B_{High} in [Figure 14-3](#)) is the highest baudrate where the deviation still does not exceed the limit, i.e. all baudrates between B_{Low} and B_{High} are below the deviation limit. B_{High} marks the baudrate up to which communication with the external host will work properly without additional tests or investigations.

Higher baudrates, however, may be used as long as the actual deviation does not exceed the indicated limit. A certain baudrate (marked I) in [Figure 14-3](#) may e.g. violate the deviation limit, while an even higher baudrate (marked II) in [Figure 14-3](#) stays very well below it. Any baudrate can be used for the bootstrap loader provided that the following three prerequisites are fulfilled:

- the baudrate is within the specified operating range for U0C0
- the external host is able to use this baudrate
- the computed deviation error is below the limit.

Note: When the bootstrap loader mode is entered after a power reset, the bootstrap loader will begin to operate with $f_{SYS} = f_{IO SC} \times 2$ (approximately 10 MHz) which will limit the maximum baudrate for U0C0.

Higher levels of the bootstrapping sequence can then switch the clock generation mode in order to achieve higher baudrates for the download.

14.6.3 Synchronous Serial Channel Bootstrap Loader

The Synchronous Serial Channel (SSC) bootstrap loader transfers program code/data from an external serial EEPROM via channel 0 of USIC0 (U0C0) into the PSRAM. The XC27x8X is the master, so no additional elements (except for the EEPROM) are required.

The SSC bootstrap loading is a convenient way for initial and basic (go/fail) testing during software development - it allows many various code-versions to be easily started on the target system by re-programming a serial EEPROM.

During SSC bootstrap loading data is transferred from the external EEPROM to the XC27x8X using synchronous eight-bit data frames with MSB first. The number of data bytes to be received in SSC boot mode is user-selectable. The serial clock rate is set to $f_{SYS}/10$, which results in 1 MHz after a power reset.

Once SSC BSL mode is entered and the respective initialization done, the XC27x8X first reads the header from the first addresses (00...0) of the target EEPROM.

This header consists of two items:

- The memory identification byte: $D5_H$
- The data size field: 1, 2 or 3 bytes, depending on the EEPROM's addressing mode (8-bit, 16-bit or 24-bit, see [Section 14.6.3.1](#))

If both items are valid the BSL enters a loop to read the number of bytes defined by the data size field via U0C0.

These bytes are stored sequentially into PSRAM starting at location $E0'0000_H$ and are then executed. Therefore, the size of the PSRAM in the respective derivative determines the real maximum block size to be downloaded.

Attention: The user must care, that the data-size is not bigger than available in the device PSRAM minus 256 and does not exceed 32512.

An invalid header (identification byte $\neq D5_H$, data size field = 0 or greater than allowed) is indicated by toggling the \overline{CS} line low 3 times. This helps debugging during the system setup phase.

Startup Configuration and Bootstrap Loading

14.6.3.1 Supported EEPROM Types

The XC27x8X's SSC bootstrap loader assumes an SPI-compatible EEPROM (25xxx series). It supports devices with 8-bit, 16-bit as well as 24-bit addressing. The connected EEPROM type is determined by examining the received header bytes, as indicated in [Table 14-12](#).

*Note: The data size **n** is in bytes.*

Table 14-12 Determining the EEPROM Type

SSC Frame		EEPROM with 8-bit addressing connected		EEPROM with 16-bit addressing connected		EEPROM with 24-bit addressing connected	
N	data	P11-send	P11-receive	P11-send	P11-receive	P11-send	P11-receive
1	03 _H	Read command	XX _H default level	Read command	XX _H default level	Read command	XX _H default level
2	00 _H	Address	XX _H	Address_H	XX _H	Address_H	XX _H
3	00 _H	dummy	D5 _H :Ident. B	Address_L	XX _H	Address_M	XX _H
4	00 _H	dummy	Size n	dummy	D5 _H :Ident. B	Address_L	XX _H
5	00 _H	dummy	Data Byte 1	dummy	Size n ,high B	dummy	D5 _H :Ident. B
6	00 _H	dummy	Data Byte 2	dummy	Size n ,low B	dummy	Size n ,high B
7	00 _H	dummy	Data Byte 3	dummy	Data Byte 1	dummy	Size n ,mid B
8	00 _H	dummy	Data Byte 4	dummy	Data Byte 2	dummy	Size n ,low B
9	...	dummy	Data Byte 5	dummy	Data Byte 3	dummy	Data Byte 1
...			... n		... n		... n

Note: The value of the returned default bytes (indicated as XX_H) depends on the employed EEPROM type.

14.6.3.2 Specific Settings

When the XC27x8X has entered the SSC BSL mode, the following configuration is automatically set:

Table 14-13 SSC BSL-Specific State

Item	Value	Comments
U0C0_CCR	0001 _H	SSC mode selected for USIC0 Channel 0
U0C0_PCRL	0011 _H	SSC master mode, frequency from fPPP
U0C0_PCRH	8000 _H	MCLK generation is enabled
U0C0_SCTRL	0103 _H	MSB first, passive data level=1
U0C0_SCTRH	073F _H	8 data bits, infinite frame
U0C0_DX0CR	0015 _H	Data input selection
U0C0_FDRL	43FF _H	Normal divider mode 1:1 selected
U0C0_BRGL	0000 _H	Normal mode, FDIV - default value after reset
U0C0_BRGH	8004 _H	Passive levels MCLK/SCLK=0, PDIV=4
P2_IOCRO3	00D0 _H	P2.3 is open-drain output (MTSR)
P2_IOCRO4	0020 _H	P2.4 is input with pull-up (MRST)
P2_IOCRO5	00D0 _H	P2.5 is open-drain output (SCLK)
P2_IOCRO6	00C0 _H	P2.6 is open-drain output (SLS)

14.6.4 CAN Bootstrap Loader

The CAN bootstrap loader transfers program code/data via node 0 of the MultiCAN module into the PSRAM. Data is transferred from the external host to the XC27x8X using eight-byte data frames. The number of data frames to be received is programmable and determined by the 16-bit data message count value DMSGC.

The communication between XC27x8X and external host is based on the following three CAN standard frames:

- Initialization frame - sent by the external host to the XC27x8X
- Acknowledge frame - sent by the XC27x8X to the external host
- Data frame(s) - sent by the external host to the XC27x8X

The initialization frame is used in the XC27x8X for baud rate detection. After a successful baud rate detection is reported to the external host by sending the acknowledge frame, data is transmitted using data frames. [Table 14-14](#) shows the parameters and settings for the three utilized CAN standard frames.

Note: The CAN bootstrap loader requires a point-to-point connection with the host, i.e. the XC27x8X must be the only CAN node connected to the network. A crystal with at least 4 MHz is required for CAN bootstrap loader operation.

Initialization Phase

The first BSL task is to determine the CAN baud rate at which the external host is communicating. Therefore the external host must send initialization frames continuously to the XC27x8X. The first two data bytes of the initialization frame must include a 2-byte baud rate detection pattern (5555_H), an 11-bit (sent in 2 bytes) identifier ACKID¹⁾ for the acknowledge frame, a 16-bit data message count value DMSGC, and an 11-bit (2-byte) identifier DMSGID¹⁾ to be used by the data frame(s).

The CAN baud rate is determined by analyzing the received baud rate detection pattern (5555_H) and the baud rate registers of the MultiCAN module are set accordingly. The XC27x8X is now ready to receive CAN frames with the baud rate of the external host.

Acknowledge Phase

In the acknowledge phase, the bootstrap loader waits until it receives the next correctly recognized initialization frame from the external host, and acknowledges this frame by generating a dominant bit in its ACK slot. Afterwards, the bootstrap loader transmits an acknowledge frame back to the external host, indicating that it is now ready to receive data frames. The acknowledge frame uses the message identifier ACKID that has been received with the initialization frame.

¹⁾ The CAN bootstrap loader copies the two identifier bytes received in the initialization frame directly to register MOAR. Therefore, the respective fields in the initialization frame must contain the intended identifier padded with two dummy bits at the lower end and extended with bitfields IDE (=0_B) and PRI (=01_B) at the upper end.

Startup Configuration and Bootstrap Loading

To summarize: the external host must send initialization frames (the content as above defined) continuously until an acknowledge frame is received back from the XC27x8X having the same message identifier as sent by the host in data bytes 2/3 from the initialization frame, then the **Data Transmission Phase** begins.

Data Transmission Phase

In the data transmission phase, data frames are sent by the external host and received by the XC27x8X. The data frames use the 11-bit data message identifier DMSGID that has been sent with the initialization frame. Eight data bytes are transmitted with each data frame. The first data byte is stored in PSRAM at E0'0000_H. Consecutive data bytes are stored at incrementing addresses.

Both communication partners evaluate the data message count DMSGC until the requested number of CAN data frames has been transmitted. After the reception of the last CAN data frame, the bootstrap loader finishes and executes the loaded code.

Timing Parameters

There are no general restrictions for CAN timings of the external host. During the initialization phase the external host transmits initialization frames. If no acknowledge frame is sent back within a certain time as defined in the external host (e.g. after a dedicated number of initialization frame transmissions), the external host can decide that the XC27x8X is not able to establish the CAN boot communication link.

Table 14-14 CAN Bootstrap Loader Frames

Frame Type	Parameter	Description
Initialization Frame	Identifier	11-bit, don't care
	DLC = 8	Data length code, 8 bytes within CAN frame
	Data bytes 0/1	Baud rate detection pattern (5555 _H)
	Data bytes 2/3	Acknowledge message identifier ACKID (complete register contents)
	Data bytes 4/5	Data message count DMSGC, 16-bit
	Data bytes 6/7	Data message identifier DMSGID (complete register contents)
Acknowledge Frame	Identifier	Acknowledge message identifier ACKID as received by data bytes [3:2] of the initialization frame
	DLC = 4	Data length code, 4 bytes within CAN frame
	Data bytes 0/1	Contents of bit-timing register
	Data bytes 2/3	Copy of acknowledge identifier from initialization frame

Startup Configuration and Bootstrap Loading

Table 14-14 CAN Bootstrap Loader Frames (cont'd)

Frame Type	Parameter	Description
Data frame	Identifier	Data message identifier DMSGID as sent by data bytes [7:6] of the initialization frame
	DLC = 8	Data length code, 8 bytes within CAN frame
	Data bytes 0 to 7	Data bytes, assigned to increasing destination (PSRAM) addresses

14.6.4.1 Specific Settings

When the XC27x8X has entered the CAN BSL mode, the following configuration is automatically set:

Table 14-15 CAN BSL-Specific State

Item	Value	Comments
P2_IOCRO5	00A0 _H	P2.5 is push/pull output (TxD)
P2_IOCRO6	0020 _H	P2.6 is input with pull-up (RxD)
SCU_HPOSCCON	0030 _H	OSC_HP enabled, External Crystal/Clock mode
SCU_SYSCON0	0001 _H	OSC_HP selected as system clock
CAN_MOCTR0L	0008 _H	Message Object 0 Control, low
CAN_MOCTR0H	00A0 _H	Message Object 0 Control, high
CAN_MOCTR1L	0000 _H	Message Object 1 Control, low
CAN_MOCTR1H	0F28 _H	Message Object 1 Control, high
CAN_MOFCTR1H	0400 _H	Message Object Function Control, high
CAN_MOAMR0H	1FFF _H	Message Object 0 - Acceptance Mask bit set
CAN_NPCRO	0003 _H	Data input selection

Startup Configuration and Bootstrap Loading

14.6.5 Summary of Bootstrap Loader Modes

This table summarizes the external hardware provisions that are required to activate a bootstrap loader in a system.

Table 14-16 Configuration Data for Bootstrap Loader Modes

Bootstrap Loader Mode	Configuration on P10.[7:0] ¹⁾	Receive Line from Host	Transmit Line to Host	Transferred Data	Supported Host Speed
Standard UART	xxxx x110 _B	RxD = P7.4	TxD = P7.3	32 bytes	2.4 - 19.2 kbaud
	xxxx x010 _B	RxD = P2.4	TxD = P2.3		
Enhanced UART	x001 0000 _B	RxD = P2.4	TxD = P2.3	l bytes ²⁾	2.4-19.2 kbaud at start, then changeable by Header
Sync. Serial	xxxx 1001 _B	MRST = P2.4	MTSR = P2.3 SCLK = P2.5 SLS = P2.6	m bytes ³⁾	--- (controlled by XC27x8X)
MultiCAN	xxxx 1101 _B	RxDC0 = P2.6	TxDC0 = P2.5	8 × n bytes ⁴⁾	125 - 500 kBaud

1) x means that the level on the corresponding pin is irrelevant.

2) l = Code_Length sent by the host, the values allowed are 1...(PSRAM_size-256) but not bigger than 65280.

3) m = data size read from EEPROM, the values allowed are 1...(PSRAM_size-256) but not bigger than 32512.

4) n = DMSGC, Data Message Count sent by the host with Initialization frame, the values allowed are 1...(PSRAM_size-256)/8.

15 Instruction Set Summary

This chapter briefly summarizes the XC27x8X's instructions ordered by instruction classes. This provides a basic understanding of the XC27x8X's instruction set, the power and versatility of the instructions and their general usage.

A detailed description of each single instruction, including its operand data type, condition flag settings, addressing modes, length (number of bytes) and object code format is provided in the **"Instruction Set Manual"** for the XC27x8X Derivatives. This manual also provides tables ordering the instructions according to various criteria, to allow quick references.

Summary of Instruction Classes

Grouping the various instruction into classes aids in identifying similar instructions (e.g. SHR, ROR) and variations of certain instructions (e.g. ADD, ADDB). This provides an easy access to the possibilities and the power of the instructions of the XC27x8X.

Note: The used mnemonics refer to the detailed description.

Table 15-1 Arithmetic Instructions

Addition of two words or bytes:	ADD	ADDB
Addition with Carry of two words or bytes:	ADDC	ADDCB
Subtraction of two words or bytes:	SUB	SUBB
Subtraction with Carry of two words or bytes:	SUBC	SUBCB
16 × 16 bit signed or unsigned multiplication:	MUL	MULU
16/16 bit signed or unsigned division:	DIV	DIVU
32/16 bit signed or unsigned division:	DIVL	DIVLU
1's complement of a word or byte:	CPL	CPLB
2's complement (negation) of a word or byte:	NEG	NEGB

Table 15-2 Logical Instructions

Bitwise ANDing of two words or bytes:	AND	ANDB
Bitwise ORing of two words or bytes:	OR	ORB
Bitwise XORing of two words or bytes:	XOR	XORB

Table 15-3 Compare and Loop Control Instructions

Comparison of two words or bytes:	CMP	CMPB
Comparison of two words with post-increment by either 1 or 2:	CMP11	CMP12
Comparison of two words with post-decrement by either 1 or 2:	CMPD1	CMPD2

Table 15-4 Boolean Bit Manipulation Instructions

Manipulation of a maskable bit field in either the high or the low byte of a word:	BFLDH	BFLDL
Setting a single bit (to '1'):	BSET	–
Clearing a single bit (to '0'):	BCLR	–
Movement of a single bit:	BMOV	–
Movement of a negated bit:	BMOVN	–
ANDing of two bits:	BAND	–
ORing of two bits:	BOR	–
XORing of two bits:	BXOR	–
Comparison of two bits:	BCMP	–

Table 15-5 Shift and Rotate Instructions

Shifting right of a word:	SHR	–
Shifting left of a word:	SHL	–
Rotating right of a word:	ROR	–
Rotating left of a word:	ROL	–
Arithmetic shifting right of a word (sign bit shifting):	ASHR	–

Table 15-6 Prioritize Instruction

Determination of the number of shift cycles required to normalize a word operand (floating point support):	PRIOR	–
--	-------	---

Table 15-7 Data Movement Instructions

Standard data movement of a word or byte:	MOV	MOVB
Data movement of a byte to a word location with either sign or zero byte extension:	MOVBS	MOVBZ

Note: The data movement instructions can be used with a big number of different addressing modes including indirect addressing and automatic pointer in-/decrementing.

Table 15-8 System Stack Instructions

Pushing of a word onto the system stack:	PUSH	–
Popping of a word from the system stack:	POP	–
Saving of a word on the system stack, and then updating the old word with a new value (provided for register bank switching):	SCXT	–

Table 15-9 Jump Instructions

Conditional jumping to an either absolutely, indirectly, or relatively addressed target instruction within the current code segment:	JMPA	JMPI	JMPR
Unconditional jumping to an absolutely addressed target instruction within any code segment:	JMPS	–	–
Conditional jumping to a relatively addressed target instruction within the current code segment depending on the state of a selectable bit:	JB	JNB	–
Conditional jumping to a relatively addressed target instruction within the current code segment depending on the state of a selectable bit with a post-inversion of the tested bit in case of jump taken (semaphore support):	JBC	JNBS	–

Table 15-10 Call Instructions

Conditional calling of an either absolutely or indirectly addressed subroutine within the current code segment:	CALLA	CALLI
Unconditional calling of a relatively addressed subroutine within the current code segment:	CALLR	–
Unconditional calling of an absolutely addressed subroutine within any code segment:	CALLS	–
Unconditional calling of an absolutely addressed subroutine within the current code segment plus an additional pushing of a selectable register onto the system stack:	PCALL	–
Unconditional branching to the interrupt or trap vector jump table in code segment <VECSEG>:	TRAP	–

Table 15-11 Return Instructions

Returning from a subroutine within the current code segment:	RET	–
Returning from a subroutine within any code segment:	RETS	–
Returning from a subroutine within the current code segment plus an additional popping of a selectable register from the system stack:	RETP	–
Returning from an interrupt service routine:	RETI	–

Table 15-12 System Control Instructions

Resetting the XC27x8X via software:	SRST	–
Entering the Idle mode:	IDLE	–
No function, do not use ¹⁾ :	PWRDN	–
Servicing the Watchdog Timer:	SRVWDT	–
Disabling the Watchdog Timer:	DISWDT	–
Enabling the Watchdog Timer (can only be executed in WDT enhanced mode):	ENWDT	–
Signifying the end of the initialization routine (switches the register security mechanism to “protected” and disables the effect of any later execution of a DISWDT instruction in WDT compatibility mode):	EINIT	–

¹⁾ Instruction PWRDN is used to enter Power Down mode in previous 16-bit architectures. In the XC27x8X devices, however, PWRDN has no effect and is executed like a NOP instruction.

Table 15-13 Miscellaneous

Null operation which requires 2 Bytes of storage and the minimum time for execution:	NOP	–
Definition of an unseparable instruction sequence:	ATOMIC	–
Switch ‘reg’, ‘bitoff’ and ‘bitaddr’ addressing modes to the Extended SFR space:	EXTR	–
Override the DPP addressing scheme using a specific data page instead of the DPPs, and optionally switch to ESFR space:	EXTP	EXTPR
Override the DPP addressing scheme using a specific segment instead of the DPPs, and optionally switch to ESFR space:	EXTS	EXTSR

Note: The ATOMIC and EXT instructions provide support for uninterruptable code sequences e.g. for semaphore operations. They also support data addressing beyond the limits of the current DPPs (except ATOMIC), which is advantageous for bigger memory models in high level languages.*

Table 15-14 MAC-Unit Instructions

Multiply (and Accumulate):	CoMUL	CoMAC
Add/Subtract:	CoADD	CoSUB
Shift right/Shift left:	CoSHR	CoSHL
Arithmetic Shift right:	CoASHR	–
Load Accumulator:	CoLOAD	–
Store MAC register:	CoSTORE	–
Compare values:	CoCMP	–
Minimum/Maximum:	CoMIN	CoMAX
Absolute value:	CoABS	–
Rounding:	CoRND	–
Move data:	CoMOV	–
Negate accumulator:	CoNEG	–
Null operation:	CoNOP	–

Protected Instructions

Some instructions of the XC27x8X which are critical for the functionality of the controller are implemented as so-called Protected Instructions. These protected instructions use the maximum instruction format of 32 bits for decoding, while the regular instructions only use a part of it (e.g. the lower 8 bits) with the other bits providing additional information like involved registers. Decoding all 32 bits of a protected doubleword instruction increases the security in cases of data distortion during instruction fetching. Critical operations like a software reset are therefore only executed if the complete instruction is decoded without an error. This enhances the safety and reliability of a microcontroller system.

16 General Purpose Timer Units (GPT12)

The General Purpose Timer Unit blocks GPT1 and GPT2 have very flexible multifunctional timer structures which may be used for timing, event counting, pulse width measurement, pulse generation, frequency multiplication, and other purposes.

They incorporate five 16-bit timers that are grouped into the two timer blocks GPT1 and GPT2. Each timer in each block may operate independently in a number of different modes such as Gated timer or Counter Mode, or may be concatenated with another timer of the same block.

Each block has alternate input/output functions and specific interrupts associated with it. Input signals can be selected from several sources by register PISEL.

The GPT module is clocked with clock f_{GPT} .

Block GPT1 contains three timers/counters: The core timer T3 and the two auxiliary timers T2 and T4. The maximum resolution is $f_{\text{GPT}}/4$. The auxiliary timers of GPT1 may optionally be configured as reload or capture registers for the core timer. These registers are listed in [Section 16.1.7.1](#).

The following list summarizes the supported features:

- $f_{\text{GPT}}/4$ maximum resolution
- 3 independent timers/counters
- Timers/counters can be concatenated
- 4 operating modes:
 - Timer Mode
 - Gated Timer Mode
 - Counter Mode
 - Incremental Interface Mode
- Reload and Capture functionality
- Separate interrupts

Block GPT2 contains two timers/counters: The core timer T6 and the auxiliary timer T5. The maximum resolution is $f_{\text{GPT}}/2$. An additional Capture/Reload register (CAPREL) supports capture and reload operation with extended functionality. These registers are listed in [Section 16.2.8.1](#).

The core timer T6 may be concatenated with timers of the CAPCOM units (T7 and T8).

The following list summarizes the supported features:

- $f_{\text{GPT}}/2$ maximum resolution
- 2 independent timers/counters
- Timers/counters can be concatenated
- 3 operating modes:
 - Timer Mode
 - Gated Timer Mode
 - Counter Mode

General Purpose Timer Units (GPT12)

- Extended capture/reload functions via 16-bit capture/reload register CAPREL
- Separate interrupt

General Purpose Timer Units (GPT12)

16.1 Timer Block GPT1

From a programmer's point of view, the GPT1 block is composed of a set of SFRs as summarized below. Those portions of port and direction registers which are used for alternate functions by the GPT1 block are shaded.

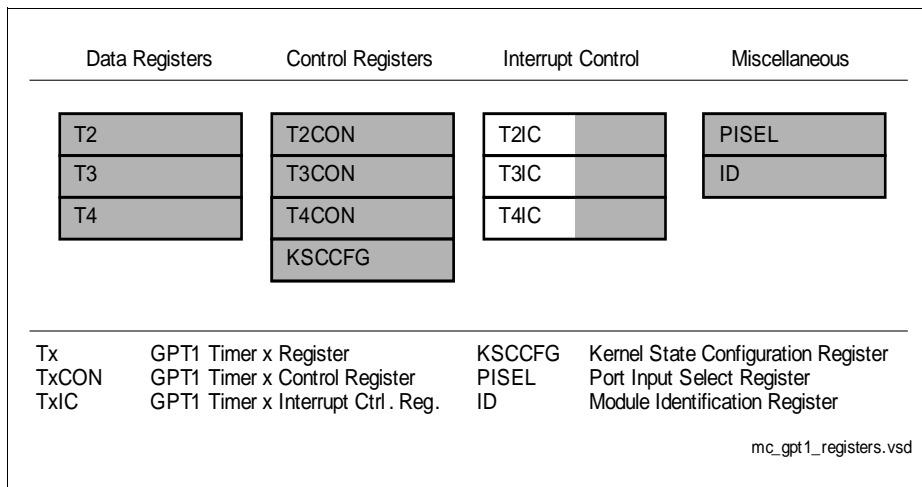


Figure 16-1 SFRs Associated with Timer Block GPT1

All three timers of block GPT1 (T2, T3, T4) can run in one of 4 basic modes: Timer Mode, Gated Timer Mode, Counter Mode, or Incremental Interface Mode. All timers can count up or down. Each timer of GPT1 is controlled by a separate control register TxCON.

Each timer has an input pin TxIN (alternate pin function) associated with it, which serves as the gate control in Gated Timer Mode, or as the count input in Counter Mode. The count direction (up/down) may be programmed via software or may be dynamically altered by a signal at the External Up/Down control input TxEUD (alternate pin function). An overflow/underflow of core timer T3 is indicated by the Output Toggle Latch T3OTL, whose state may be output on the associated pin T3OUT (alternate pin function). The auxiliary timers T2 and T4 may additionally be concatenated with the core timer T3 (through T3OTL) or may be used as capture or reload registers for the core timer T3.

The current contents of each timer can be read or modified by the CPU by accessing the corresponding timer count registers T2, T3, or T4, located in the non-bitaddressable SFR space (see [Section 16.1.7.1](#)). When any of the timer registers is written to by the CPU in the state immediately preceding a timer increment, decrement, reload, or capture operation, the CPU write operation has priority in order to guarantee correct results.

The interrupts of GPT1 are controlled through the Interrupt Control Registers TxIC. These registers are not part of the GPT1 block.

General Purpose Timer Units (GPT12)

The input and output lines of GPT1 are connected to pins. The control registers for the port functions are located in the respective port modules.

Note: The timing requirements for external input signals can be found in [Section 16.1.5](#), [Section 16.5.1](#) summarizes the module interface signals, including pins.

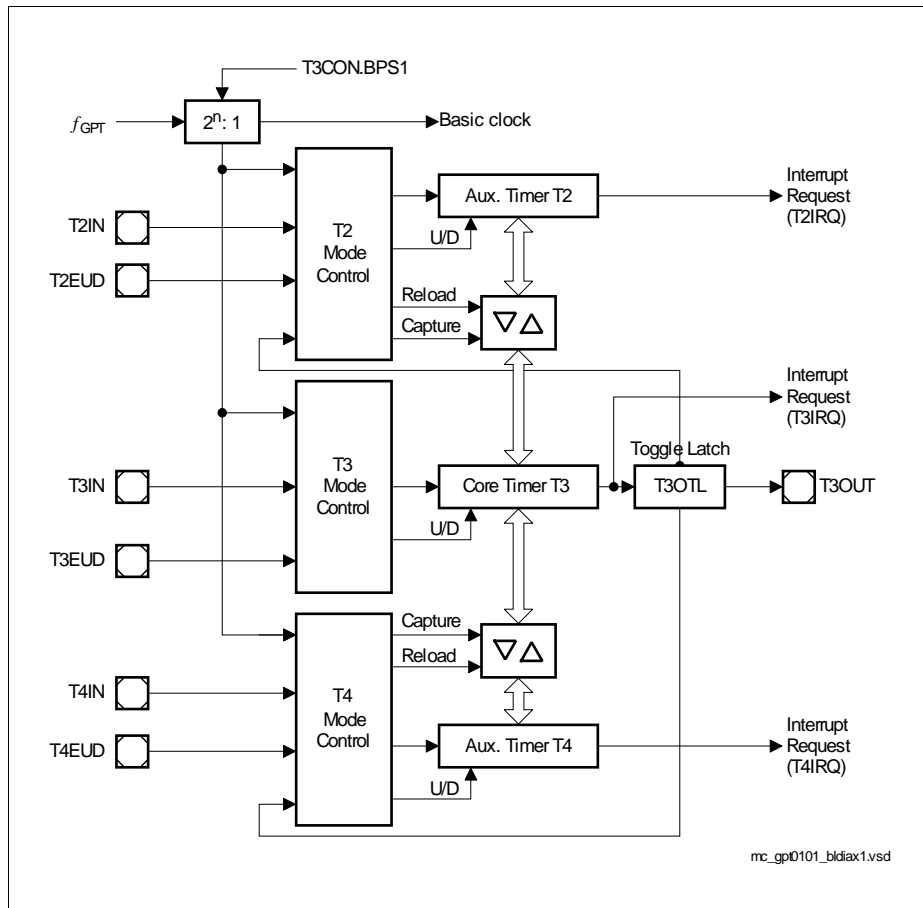


Figure 16-2 GPT1 Block Diagram (n = 2 ... 5)

16.1.1 GPT1 Core Timer T3 Control

The current contents of the core timer T3 are reflected by its count register T3. This register can also be written to by the CPU, for example, to set the initial start value.

The core timer T3 is configured and controlled via its bitaddressable control register T3CON.

Timer T3 Run Control

The core timer T3 can be started or stopped by software through bit T3R (Timer T3 Run Bit). This bit is relevant in all operating modes of T3. Setting bit T3R will start the timer, clearing bit T3R stops the timer.

In Gated Timer Mode, the timer will only run if T3R = 1 and the gate is active (high or low, as programmed).

Note: When bit T2RC or T4RC in timer control register T2CON or T4CON is set, bit T3R will also control (start and stop) the auxiliary timer(s) T2 and/or T4.

Count Direction Control

The count direction of the GPT1 timers (core timer and auxiliary timers) can be controlled either by software or by the external input pin TxEUD (Timer Tx External Up/Down Control Input). These options are selected by bits TxUD and TxUDE in the respective control register TxCON. When the up/down control is provided by software (bit TxUDE = 0), the count direction can be altered by setting or clearing bit TxUD. When bit TxUDE = 1, pin TxEUD is selected to be the controlling source of the count direction. However, bit TxUD can still be used to reverse the actual count direction, as shown in [Table 16-5](#). The count direction can be changed regardless of whether or not the timer is running.

Note: When pin TxEUD is used as external count direction control input, it must be configured as input.

Timer T3 Output Toggle Latch

The overflow/underflow signal of timer T3 is connected to a block named 'Toggle Latch', shown in the Timer Mode diagrams. **Figure 16-3** illustrates the details of this block. An overflow or underflow of T3 will clock two latches: The first latch represents bit T3OTL in control register T3CON. The second latch is an internal latch toggled by T3OTL's output. Both latch outputs are connected to the input control blocks of the auxiliary timers T2 and T4. The output level of the shadow latch will match the output level of T3OTL, but is delayed by one clock cycle. When the T3OTL value changes, this will result in a temporarily different output level from T3OTL and the shadow latch, which can trigger the selected count event in T2 and/or T4.

When software writes to T3OTL, both latches are set or cleared simultaneously. In this case, both signals to the auxiliary timers carry the same level and no edge will be detected. Bit T3OE (overflow/underflow output enable) in register T3CON enables the state of T3OTL to be monitored via an external pin T3OUT. When T3OTL is linked to an external port pin (must be configured as output), T3OUT can be used to control external HW. If T3OE = 1, pin T3OUT outputs the state of T3OTL. If T3OE = 0, pin T3OUT outputs a high level (as long as the T3OUT alternate function is selected for the port pin).

The trigger signals can serve as an input for the counter function or as a trigger source for the reload function of the auxiliary timers T2 and T4.

As can be seen from **Figure 16-3**, when latch T3OTL is modified by software to determine the state of the output line, also the internal shadow latch is set or cleared accordingly. Therefore, no trigger condition is detected by T2/T4 in this case.

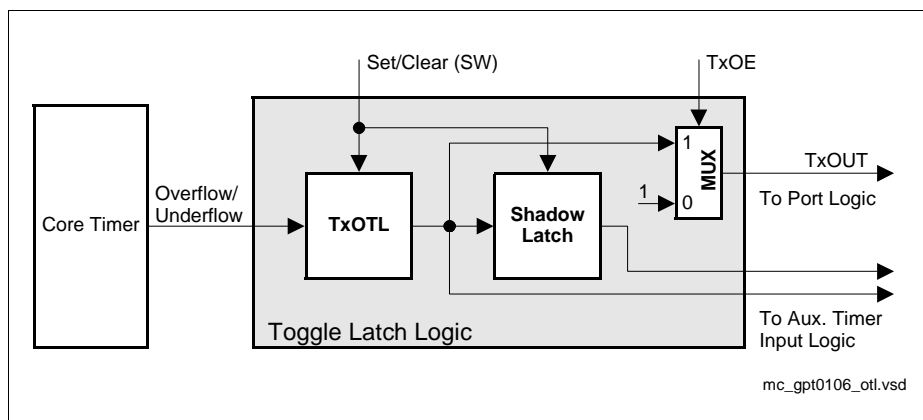


Figure 16-3 Block Diagram of the Toggle Latch Logic of Core Timer T3 (x = 3)

16.1.2 GPT1 Core Timer T3 Operating Modes

Timer T3 can operate in one of several modes.

Timer T3 in Timer Mode

Timer mode for the core timer T3 is selected by setting bitfield T3M in register T3CON to 000_B. In Timer Mode, T3 is clocked with the module's input clock f_{GPT} divided by two programmable prescalers controlled by bitfields BPS1 and T3I in register T3CON. Please see [Section 16.1.5](#) for details on the input clock options.

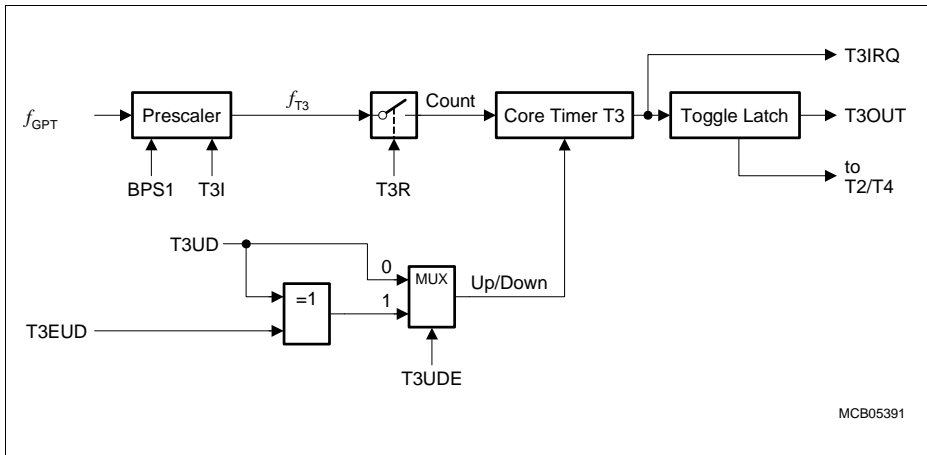
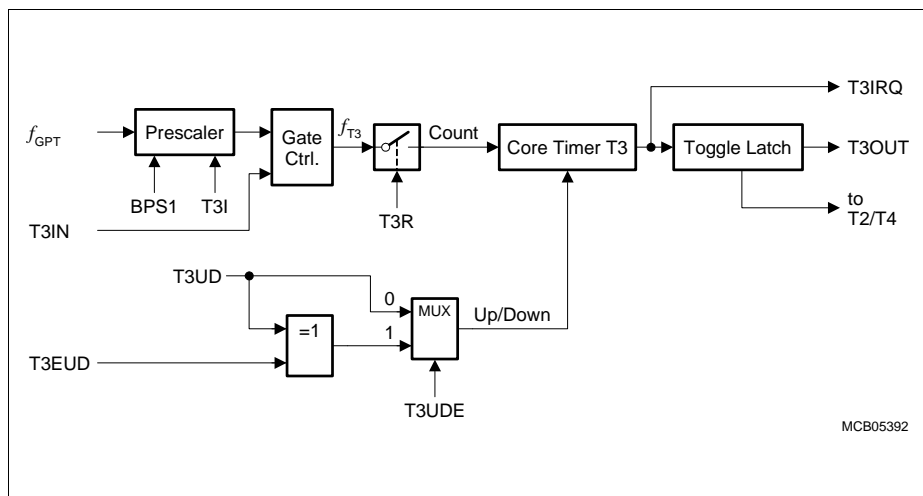


Figure 16-4 Block Diagram of Core Timer T3 in Timer Mode

Timer T3 in Gated Timer Mode

Gated Timer Mode for the core timer T3 is selected by setting bitfield T3M in register T3CON to 010_B or 011_B. Bit T3M.0 (T3CON.3) selects the active level of the gate input. The same options for the input frequency are available in Gated Timer Mode as in Timer Mode (see [Section 16.1.5](#)). However, the input clock to the timer in this mode is gated by the external input pin T3IN (Timer T3 External Input).

To enable this operation, the associated pin T3IN must be configured as input.



MCB05392

Figure 16-5 Block Diagram of Core Timer T3 in Gated Timer Mode

If T3M = 010_B, the timer is enabled when T3IN shows a low level. A high level at this line stops the timer. If T3M = 011_B, line T3IN must have a high level in order to enable the timer. Additionally, the timer can be turned on or off by software using bit T3R. The timer will only run if T3R is 1 and the gate is active. It will stop if either T3R is 0 or the gate is inactive.

Note: A transition of the gate signal at pin T3IN does not cause an interrupt request.

Timer T3 in Counter Mode

Counter Mode for the core timer T3 is selected by setting bitfield T3M in register T3CON to 001_B. In Counter Mode, timer T3 is clocked by a transition at the external input pin T3IN. The event causing an increment or decrement of the timer can be a positive, a negative, or both a positive and a negative transition at this line. Bitfield T3I in control register T3CON selects the triggering transition (see [Table 16-7](#)).

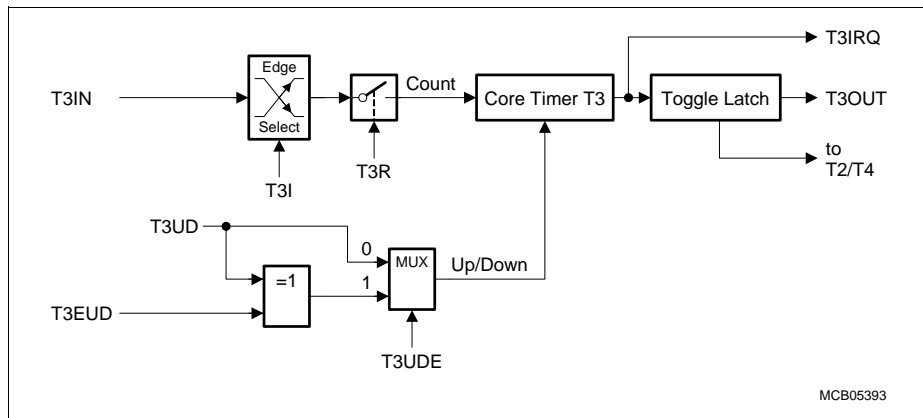


Figure 16-6 Block Diagram of Core Timer T3 in Counter Mode

For Counter Mode operation, pin T3IN must be configured as input. The maximum input frequency allowed in Counter Mode depends on the selected prescaler value. To ensure that a transition of the count input signal applied to T3IN is recognized correctly, its level must be held high or low for a minimum number of module clock cycles before it changes. This information can be found in [Section 16.1.5](#).

Timer T3 in Incremental Interface Mode

Incremental interface mode for the core timer T3 is selected by setting bitfield T3M in register T3CON to 110_B or 111_B. In Incremental Interface Mode, the two inputs associated with core timer T3 (T3IN, T3EUD) are used to interface to an incremental encoder. T3 is clocked by each transition on one or both of the external input pins to provide 2-fold or 4-fold resolution of the encoder input.

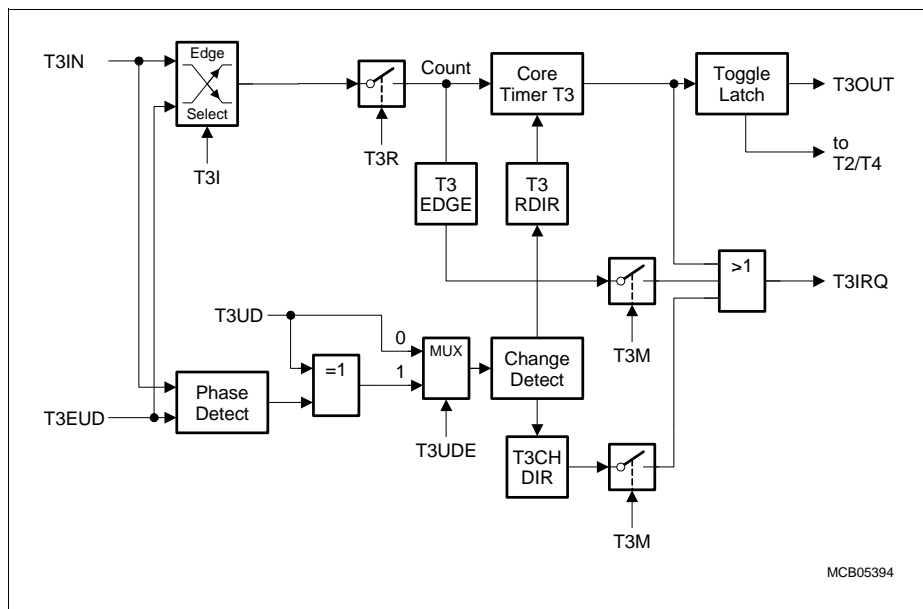


Figure 16-7 Block Diagram of Core Timer T3 in Incremental Interface Mode

Bitfield T3I in control register T3CON selects the triggering transitions (see [Table 16-9](#)). The sequence of the transitions of the two input signals is evaluated and generates count pulses as well as the direction signal. So T3 is modified automatically according to the speed and the direction of the incremental encoder and, therefore, its contents always represent the encoder's current position.

The interrupt request (T3IRQ) generation mode can be selected: In Rotation Detection Mode (T3M = 110_B), an interrupt request is generated each time the count direction of T3 changes. In Edge Detection Mode (T3M = 111_B), an interrupt request is generated each time a count edge for T3 is detected. Count direction, changes in the count direction, and count requests are monitored by status bits T3RDIR, T3CHDIR, and T3EDGE in register T3CON.

The incremental encoder can be connected directly to the XC27x8X without external interface logic. In a standard system, however, comparators will be employed to convert

General Purpose Timer Units (GPT12)

the encoder's differential outputs (such as A, \bar{A}) to digital signals (such as A). This greatly increases noise immunity.

Note: The third encoder output T0, which indicates the mechanical zero position, may be connected to an external interrupt input and trigger a reset of timer T3 (for example via PEC transfer from ZEROS).

If input T4IN is available, T0 can be connected there and clear T3 automatically without requiring an interrupt.

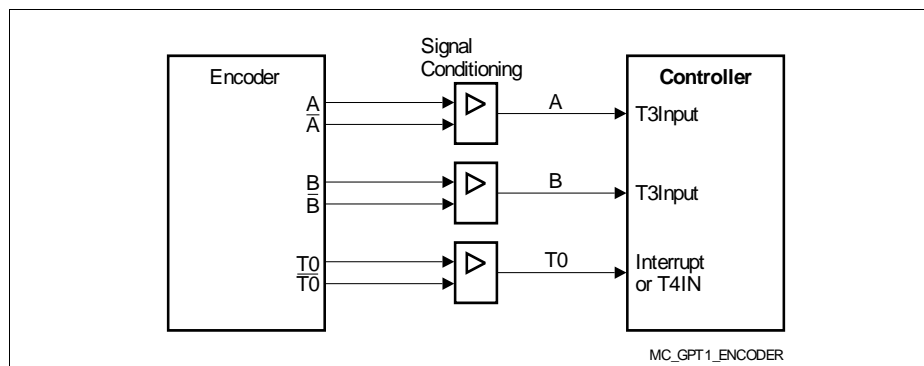


Figure 16-8 Connection of the Encoder to the XC27x8X

For incremental interface operation, the following conditions must be met:

- Bitfield T3M must be 110_B or 111_B.
- Both pins T3IN and T3EUD must be configured as input.
- Pin T4IN must be configured as input, if used for T0.
- Bit T3UDE must be 1 to enable automatic external direction control.

The maximum count frequency allowed in Incremental Interface Mode depends on the selected prescaler value. To ensure that a transition of any input signal is recognized correctly, its level must be held high or low for a minimum number of module clock cycles before it changes. This information can be found in [Section 16.1.5](#).

As in Incremental Interface Mode two input signals with a 90° phase shift are evaluated, their maximum input frequency can be half the maximum count frequency.

In Incremental Interface Mode, the count direction is automatically derived from the sequence in which the input signals change, which corresponds to the rotation direction of the connected sensor. [Table 16-1](#) summarizes the possible combinations.

Table 16-1 GPT1 Core Timer T3 (Incremental Interface Mode) Count Direction

Level on Respective other Input	T3IN Input		T3EUD Input	
	Rising ↑	Falling ↓	Rising ↑	Falling ↓
High	Down	Up	Up	Down
Low	Up	Down	Down	Up

Figure 16-9 and **Figure 16-10** give examples of T3's operation, visualizing count signal generation and direction control. They also show how input jitter is compensated, which might occur if the sensor rests near to one of its switching points.

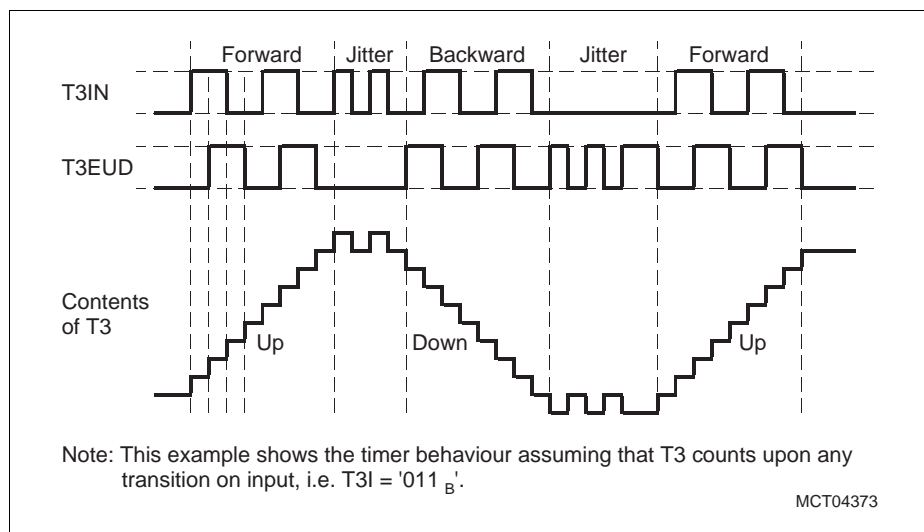


Figure 16-9 Evaluation of Incremental Encoder Signals, 2 Count Inputs

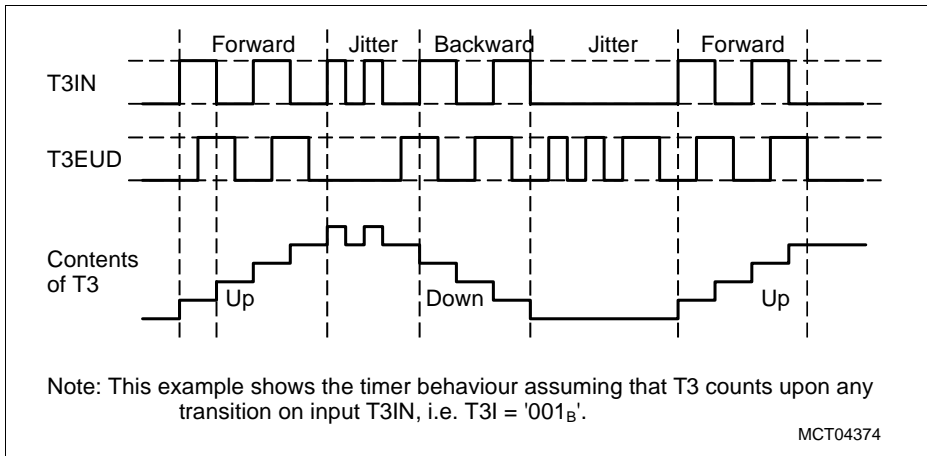


Figure 16-10 Evaluation of Incremental Encoder Signals, 1 Count Input

Note: Timer T3 operating in Incremental Interface Mode automatically provides information on the sensor's current position. Dynamic information (speed, acceleration, deceleration) may be obtained by measuring the incoming signal periods (see [“Combined Capture Modes” on Page 16-58](#)).

16.1.3 GPT1 Auxiliary Timers T2/T4 Control

Auxiliary timers T2 and T4 have exactly the same functionality. They can be configured for Timer Mode, Gated Timer Mode, Counter Mode, or Incremental Interface Mode with the same options for the timer frequencies and the count signal as the core timer T3. In addition to these 4 counting modes, the auxiliary timers can be concatenated with the core timer, or they may be used as reload or capture registers in conjunction with the core timer. The start/stop function of the auxiliary timers can be remotely controlled by the T3 run control bit. Several timers may thus be controlled synchronously.

The current contents of an auxiliary timer are reflected by its count register T2 or T4, respectively. These registers can also be written to by the CPU, for example, to set the initial start value.

The individual configurations for timers T2 and T4 are determined by their bitaddressable control registers T2CON and T4CON, which are organized identically. Note that functions which are present in all 3 timers of block GPT1 are controlled in the same bit positions and in the same manner in each of the specific control registers.

Note: The auxiliary timers have no output toggle latch and no alternate output function.

Timer T2/T4 Run Control

Each of the auxiliary timers T2 and T4 can be started or stopped by software in two different ways:

- Through the associated timer run bit (T2R or T4R). In this case it is required that the respective control bit TxRC = 0.
- Through the core timer's run bit (T3R). In this case the respective remote control bit must be set (TxRC = 1).

The selected run bit is relevant in all operating modes of T2/T4. Setting the bit will start the timer, clearing the bit stops the timer.

In Gated Timer Mode, the timer will only run if the selected run bit is set and the gate is active (high or low, as programmed).

Note: If remote control is selected T3R will start/stop timer T3 and the selected auxiliary timer(s) synchronously.

Count Direction Control

The count direction of the GPT1 timers (core timer and auxiliary timers) is controlled in the same way, either by software or by the external input pin TxEUD. Please refer to the description in [Table 16-5](#).

Note: When pin TxEUD is used as external count direction control input, it must be configured as input.

16.1.4 GPT1 Auxiliary Timers T2/T4 Operating Modes

The operation of the auxiliary timers in the basic operating modes is almost identical with the core timer's operation, with very few exceptions. Additionally, some combined operating modes can be selected.

Timers T2 and T4 in Timer Mode

Timer mode for an auxiliary timer Tx is selected by setting its bitfield TxM in register TxCON to 000_B.

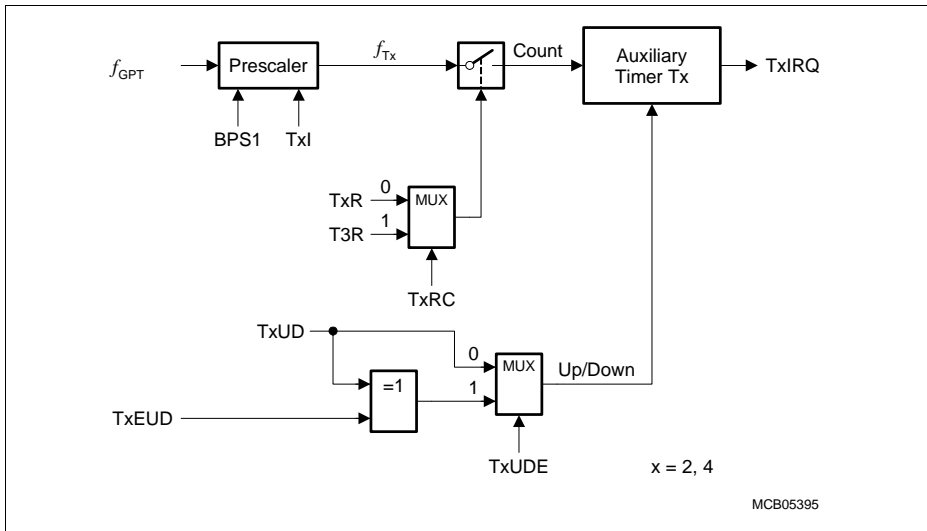


Figure 16-11 Block Diagram of an Auxiliary Timer in Timer Mode

General Purpose Timer Units (GPT12)

Timers T2 and T4 in Gated Timer Mode

Gated Timer Mode for an auxiliary timer Tx is selected by setting bitfield TxM in register TxCON to 010_B or 011_B. Bit TxM.0 (TxCON.3) selects the active level of the gate input.

Note: A transition of the gate signal at line TxIN does not cause an interrupt request.

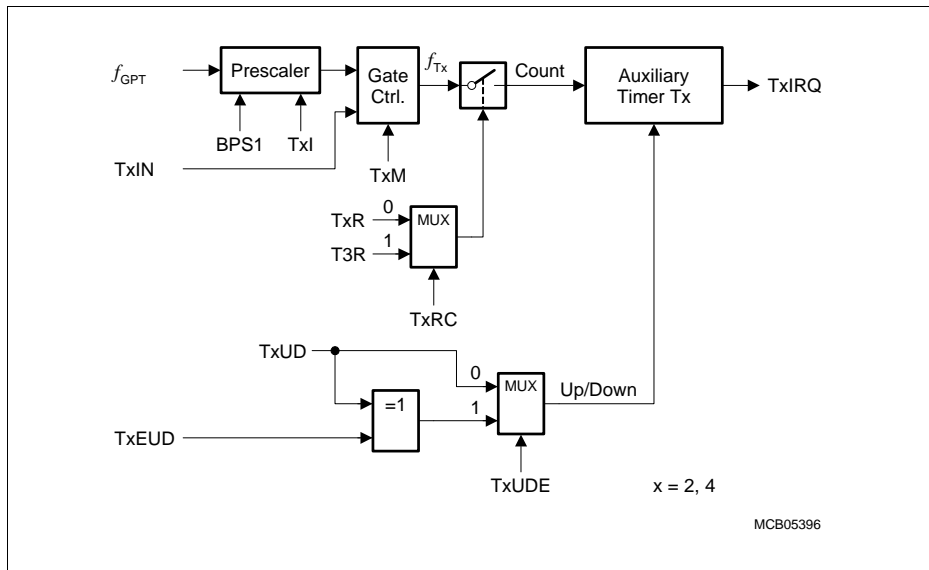


Figure 16-12 Block Diagram of an Auxiliary Timer in Gated Timer Mode

Note: There is no output toggle latch for T2 and T4.

Start/stop of an auxiliary timer can be controlled locally or remotely.

Timers T2 and T4 in Counter Mode

Counter Mode for an auxiliary timer Tx is selected by setting bitfield TxM in register TxCON to 001_B. In Counter Mode, an auxiliary timer can be clocked either by a transition at its external input line TxIN, or by a transition of timer T3's toggle latch T3OTL. The event causing an increment or decrement of a timer can be a positive, a negative, or both a positive and a negative transition at either the respective input pin or at the toggle latch. Bitfield TxI in control register TxCON selects the triggering transition (see [Table 16-8](#)).

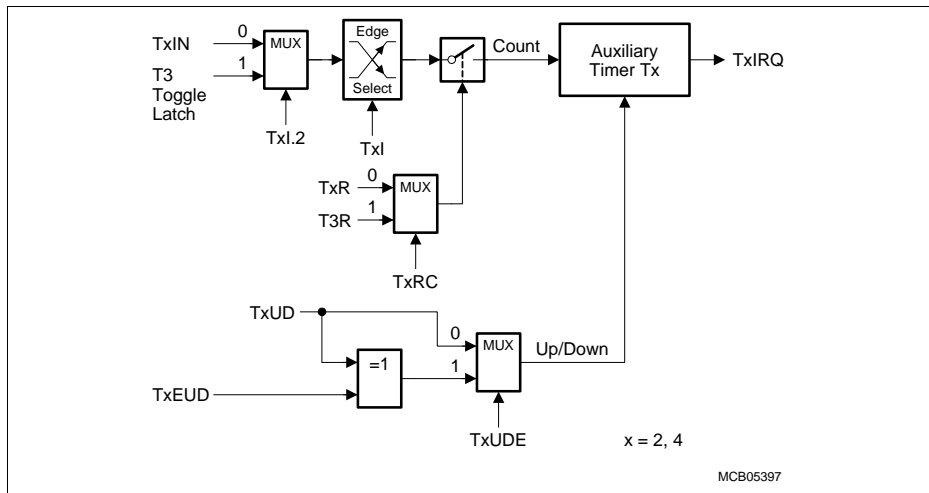


Figure 16-13 Block Diagram of an Auxiliary Timer in Counter Mode

Note: Only state transitions of T3OTL which are caused by the overflows/underflows of T3 will trigger the counter function of T2/T4. Modifications of T3OTL via software will NOT trigger the counter function of T2/T4.

For counter operation, pin TxIN must be configured as input. The maximum input frequency allowed in Counter Mode depends on the selected prescaler value. To ensure that a transition of the count input signal applied to TxIN is recognized correctly, its level must be held high or low for a minimum number of module clock cycles before it changes. This information can be found in [Section 16.1.5](#).

General Purpose Timer Units (GPT12)

Timer Concatenation

Using the toggle bit T3OTL as a clock source for an auxiliary timer in Counter Mode concatenates the core timer T3 with the respective auxiliary timer. This concatenation forms either a 32-bit or a 33-bit timer/counter, depending on which transition of T3OTL is selected to clock the auxiliary timer.

- **32-bit Timer/Counter:** If both a positive and a negative transition of T3OTL are used to clock the auxiliary timer, this timer is clocked on every overflow/underflow of the core timer T3. Thus, the two timers form a 32-bit timer.
- **33-bit Timer/Counter:** If either a positive or a negative transition of T3OTL is selected to clock the auxiliary timer, this timer is clocked on every second overflow/underflow of the core timer T3. This configuration forms a 33-bit timer (16-bit core timer + T3OTL + 16-bit auxiliary timer).

As long as bit T3OTL is not modified by software, it represents the state of the internal toggle latch, and can be regarded as part of the 33-bit timer.

The count directions of the two concatenated timers are not required to be the same. This offers a wide variety of different configurations.

T3, which represents the low-order part of the concatenated timer, can operate in Timer Mode, Gated Timer Mode or Counter Mode in this case.

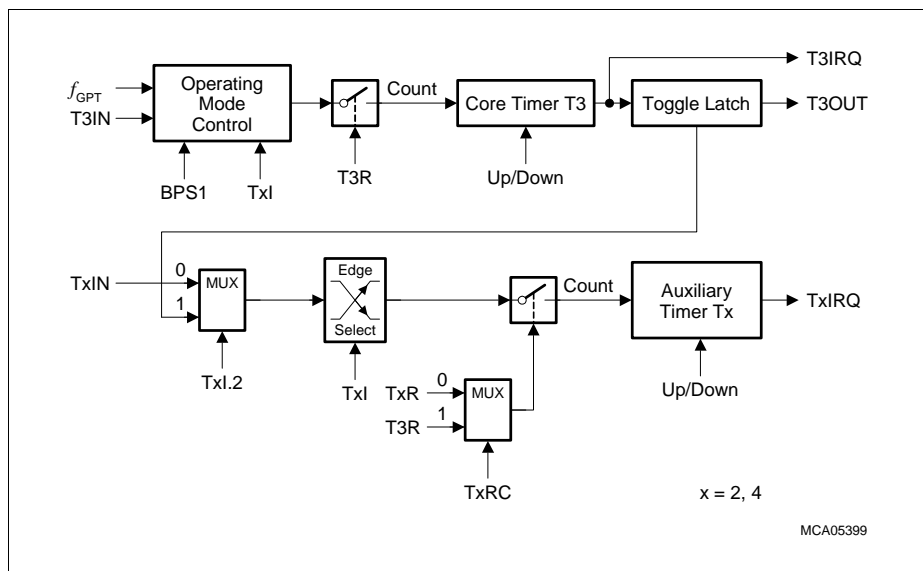


Figure 16-14 Concatenation of Core Timer T3 and an Auxiliary Timer

Timers T2 and T4 in Capture Mode

Capture mode for an auxiliary timer Tx is selected by setting bitfield TxM in the respective register TxCON to 101_B. In capture mode, the contents of the core timer T3 are latched into an auxiliary timer register in response to a signal transition at the respective auxiliary timer's external input pin TxIN. The capture trigger signal can be a positive, a negative, or both a positive and a negative transition.

The two least significant bits of bitfield TxI select the active transition (see [Table 16-8](#)). Bit 2 of TxI is irrelevant for capture mode and must be cleared (TxI.2 = 0).

Note: When programmed for capture mode, the respective auxiliary timer (T2 or T4) stops independently of its run flag T2R or T4R.

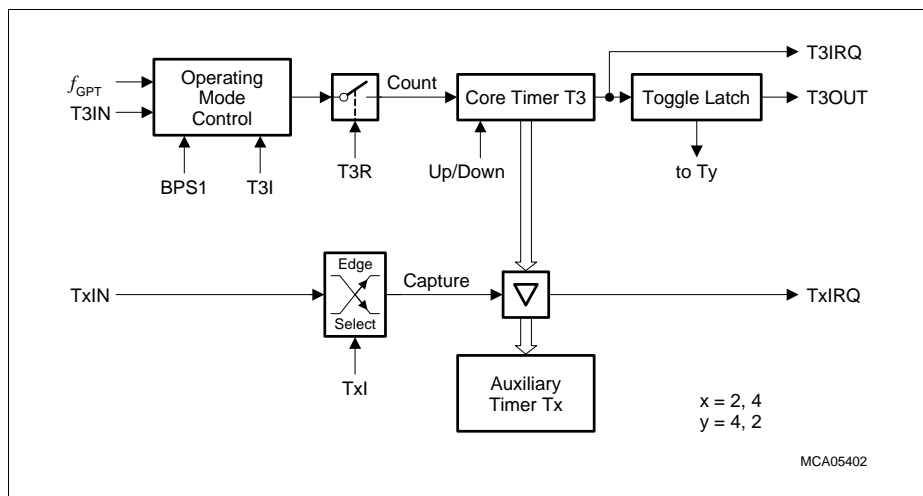


Figure 16-15 GPT1 Auxiliary Timer in Capture Mode

Upon a trigger (selected transition) at the corresponding input pin TxIN the contents of the core timer are loaded into the auxiliary timer register and the associated interrupt request flag TxIR will be set.

For capture mode operation, the respective timer input pin TxIN must be configured as input. To ensure that a transition of the capture input signal applied to TxIN is recognized correctly, its level must be held high or low for a minimum number of module clock cycles, detailed in [Section 16.1.5](#).

Timers T2 and T4 in Incremental Interface Mode

Incremental interface mode for an auxiliary timer Tx is selected by setting bitfield TxM in the respective register TxCON to 110_B or 111_B. In Incremental Interface Mode, the two inputs associated with an auxiliary timer Tx (TxIN, TxEUD) are used to interface to an incremental encoder. Tx is clocked by each transition on one or both of the external input pins to provide 2-fold or 4-fold resolution of the encoder input.

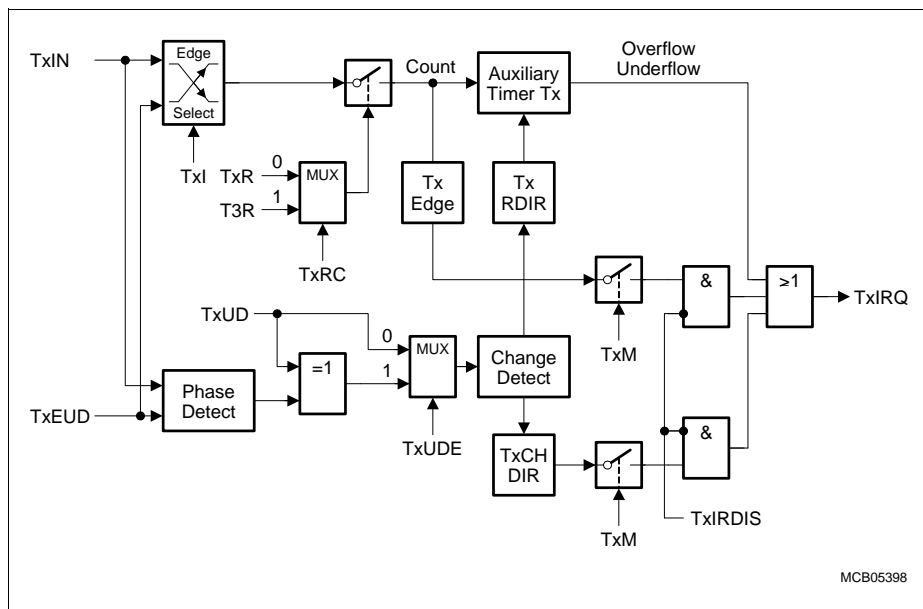


Figure 16-16 Block Diagram of an Auxiliary Timer in Incremental Interface Mode

The operation of the auxiliary timers T2 and T4 in Incremental Interface Mode and the interrupt generation are the same as described for the core timer T3. The descriptions, figures and tables apply accordingly.

*Note: Timers T2 and T4 operating in Incremental Interface Mode automatically provide information on the sensor's current position. For dynamic information (speed, acceleration, deceleration) see **"Combined Capture Modes" on Page 16-58**.*

General Purpose Timer Units (GPT12)

Timers T2 and T4 in Reload Mode

Reload Mode for an auxiliary timer Tx is selected by setting bitfield TxM in the respective register TxCON to 100_B. In reload mode, the core timer T3 is reloaded with the contents of an auxiliary timer register, triggered by one of two different signals. The trigger signal is selected the same way as the clock source for Counter Mode (see [Table 16-8](#)), i.e. a transition of the auxiliary timer's input TxIN or the toggle latch T3OTL may trigger the reload.

Note: When programmed for reload mode, the respective auxiliary timer (T2 or T4) stops independently of its run flag T2R or T4R.

The timer input pin TxIN must be configured as input if it shall trigger a reload operation.

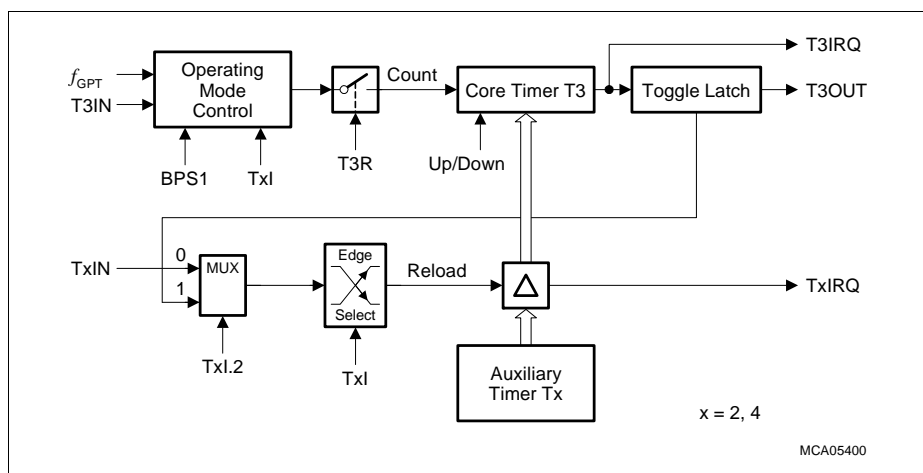


Figure 16-17 GPT1 Auxiliary Timer in Reload Mode

Upon a trigger signal, T3 is loaded with the contents of the respective timer register (T2 or T4) and the respective interrupt request flag (T2IR or T4IR) is set.

Note: When a T3OTL transition is selected for the trigger signal, the interrupt request flag T3IR will also be set upon a trigger, indicating T3's overflow or underflow. Modifications of T3OTL via software will NOT trigger the counter function of T2/T4.

To ensure that a transition of the reload input signal applied to TxIN is recognized correctly, its level must be held high or low for a minimum number of module clock cycles, detailed in [Section 16.1.5](#).

The reload mode triggered by the T3 toggle latch can be used in a number of different configurations. The following functions can be performed, depending on the selected active transition:

General Purpose Timer Units (GPT12)

- If both a positive and a negative transition of T3OTL are selected to trigger a reload, the core timer will be reloaded with the contents of the auxiliary timer each time it overflows or underflows. This is the standard reload mode (reload on overflow/underflow).
- If either a positive or a negative transition of T3OTL is selected to trigger a reload, the core timer will be reloaded with the contents of the auxiliary timer on every second overflow or underflow.
- Using this "single-transition" mode for both auxiliary timers allows to perform very flexible Pulse Width Modulation (PWM). One of the auxiliary timers is programmed to reload the core timer on a positive transition of T3OTL, the other is programmed for a reload on a negative transition of T3OTL. With this combination the core timer is alternately reloaded from the two auxiliary timers.

Figure 16-18 shows an example for the generation of a PWM signal using the "single-transition" reload mechanism. T2 defines the high time of the PWM signal (reloaded on positive transitions) and T4 defines the low time of the PWM signal (reloaded on negative transitions). The PWM signal can be output on pin T3OUT if T3OE = 1. With this method, the high and low time of the PWM signal can be varied in a wide range.

Note: The output toggle latch T3OTL is accessible via software and may be changed, if required, to modify the PWM signal.

However, this will NOT trigger the reloading of T3.

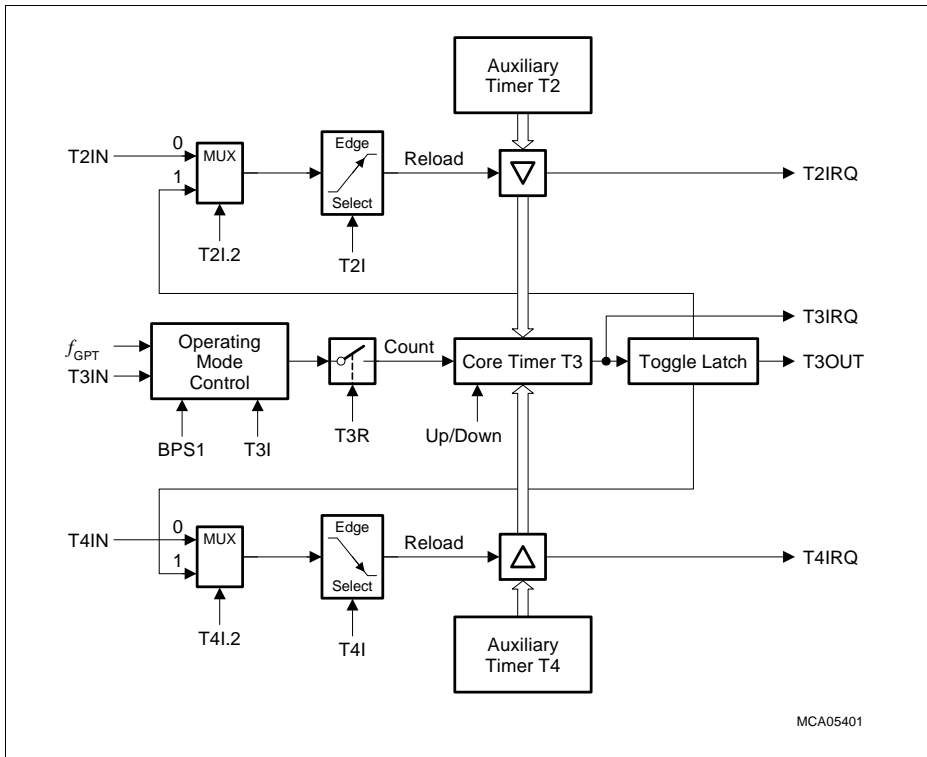


Figure 16-18 GPT1 Timer Reload Configuration for PWM Generation

Note: Although possible, selecting the same reload trigger event for both auxiliary timers should be avoided. In such a case, both reload registers would try to load the core timer at the same time. If this combination is selected, T2 is disregarded and the contents of T4 is reloaded.

General Purpose Timer Units (GPT12)

16.1.5 GPT1 Clock Signal Control

All actions within the timer block GPT1 are triggered by transitions of its basic clock. This basic clock is derived from the system clock by a basic block prescaler, controlled by bitfield BPS1 in register T3CON (see [Figure 16-2](#)). The count clock can be generated in two different ways:

- **Internal count clock**, derived from GPT1's basic clock via a programmable prescaler, is used for (gated) Timer Mode.
- **External count clock**, derived from the timer's input pin(s), is used for Counter Mode.

For both ways, the basic clock determines the maximum count frequency and the timer's resolution:

Table 16-2 Basic Clock Selection for Block GPT1

Block Prescaler ¹⁾	BPS1 = 01 _B	BPS1 = 00 _B ²⁾	BPS1 = 11 _B	BPS1 = 10 _B
Prescaling Factor for GPT1: F(BPS1)	F(BPS1) = 4	F(BPS1) = 8	F(BPS1) = 16	F(BPS1) = 32
Maximum External Count Frequency	$f_{\text{GPT}}/8$	$f_{\text{GPT}}/16$	$f_{\text{GPT}}/32$	$f_{\text{GPT}}/64$
Input Signal Stable Time	$4 \times t_{\text{GPT}}$	$8 \times t_{\text{GPT}}$	$16 \times t_{\text{GPT}}$	$32 \times t_{\text{GPT}}$

1) Please note the non-linear encoding of bitfield BPS1.

2) Default after reset.

Note: When initializing the GPT1 block, and the block prescaler BPS1 in register T3CON needs to be set to a value different from its reset value (00_B), it must be initialized first before any mode involving external trigger signals is configured. These modes include counter, incremental interface, capture, and reload mode. Otherwise, unintended count/capture/reload events may occur.

In this case (e.g. when changing BPS1 during operation of the GPT1 block), disable related interrupts before modification of BPS1, and afterwards clear the corresponding service request flags and re-initialize those registers (T2, T3, T4) that might be affected by a count/capture/reload event.

Internal Count Clock Generation

In Timer Mode and Gated Timer Mode, the count clock for each GPT1 timer is derived from the GPT1 basic clock by a programmable prescaler, controlled by bitfield TxI in the respective timer's control register TxCON.

General Purpose Timer Units (GPT12)

The count frequency f_{Tx} for a timer Tx and its resolution r_{Tx} are scaled linearly with lower clock frequencies, as can be seen from the following formula:

$$f_{Tx} = \frac{f_{GPT}}{F(BPS1) \times 2^{<TxI>}} \quad r_{Tx}[\mu s] = \frac{F(BPS1) \times 2^{<TxI>}}{f_{GPT}[MHz]} \quad (16.1)$$

The effective count frequency depends on the common module clock prescaler factor $F(BPS1)$ as well as on the individual input prescaler factor $2^{<TxI>}$. **Table 16-6** summarizes the resulting overall divider factors for a GPT1 timer that result from these cascaded prescalers.

Table 16-3 lists GPT1 timer's parameters (such as count frequency, resolution, and period) resulting from the selected overall prescaler factor and the module clock f_{GPT} . Note that some numbers may be rounded.

Table 16-3 GPT1 Timer Parameters

Module Clock $f_{GPT} = 10 \text{ MHz}$			Overall Prescaler Factor	Module Clock $f_{GPT} = 40 \text{ MHz}$		
Frequency	Resolution	Period		Frequency	Resolution	Period
2.5 MHz	400 ns	26.21 ms	4	10.0 MHz	100 ns	6.55 ms
1.25 MHz	800 ns	52.43 ms	8	5.0 MHz	200 ns	13.11 ms
625.0 kHz	1.6 μs	104.9 ms	16	2.5 MHz	400 ns	26.21 ms
312.5 kHz	3.2 μs	209.7 ms	32	1.25 MHz	800 ns	52.43 ms
156.25 kHz	6.4 μs	419.4 ms	64	625.0 kHz	1.6 μs	104.9 ms
78.125 kHz	12.8 μs	838.9 ms	128	312.5 kHz	3.2 μs	209.7 ms
39.06 kHz	25.6 μs	1.678 s	256	156.25 kHz	6.4 μs	419.4 ms
19.53 kHz	51.2 μs	3.355 s	512	78.125 kHz	12.8 μs	838.9 ms
9.77 kHz	102.4 μs	6.711 s	1024	39.06 kHz	25.6 μs	1.678 s
4.88 kHz	204.8 μs	13.42 s	2048	19.53 kHz	51.2 μs	3.355 s
2.44 kHz	409.6 μs	26.84 s	4096	9.77 kHz	102.4 μs	6.711 s

External Count Clock Input

The external input signals of the GPT1 block are sampled with the GPT1 basic clock (see **Figure 16-2**). To ensure that a signal is recognized correctly, its current level (high or low) must be held active for at least one complete sampling period, before changing. A signal transition is recognized if two subsequent samples of the input signal represent different levels. Therefore, a minimum of two basic clock periods are required for the sampling of an external input signal. Thus, the maximum frequency of an input signal must not be higher than half the basic clock.

General Purpose Timer Units (GPT12)

Table 16-4 summarizes the resulting requirements for external GPT1 input signals.

Table 16-4 GPT1 External Input Signal Limits

GPT1 Basic Clock = 10 MHz		Input Frequ. Factor	GPT1 Divider BPS1	Input Phase Duration	GPT1 Basic Clock = 40 MHz	
Max. Input Frequency	Min. Level Hold Time				Max. Input Frequency	Min. Level Hold Time
1.25 MHz	400 ns	$f_{\text{GPT}}/8$	01 _B	$4 \times t_{\text{GPT}}$	5.0 MHz	100 ns
625.0 kHz	800 ns	$f_{\text{GPT}}/16$	00 _B	$8 \times t_{\text{GPT}}$	2.5 MHz	200 ns
312.5 kHz	1.6 μs	$f_{\text{GPT}}/32$	11 _B	$16 \times t_{\text{GPT}}$	1.25 MHz	400 ns
156.25 kHz	3.2 μs	$f_{\text{GPT}}/64$	10 _B	$32 \times t_{\text{GPT}}$	625.0 kHz	800 ns

These limitations are valid for all external input signals to GPT1, including the external count signals in Counter Mode and Incremental Interface Mode, the gate input signals in Gated Timer Mode, and the external direction signals.

16.1.6 Interrupt Control for GPT1 Timers

When a timer overflows from $FFFF_H$ to 0000_H (when counting up), or when it underflows from 0000_H to $FFFF_H$ (when counting down), its interrupt request flag in register GPT12E_T2IC, GPT12E_T3IC, or GPT12E_T4IC will be set. This will cause an interrupt to the respective timer interrupt vector or trigger a PEC service, if the respective interrupt enable bit is set.

There is an interrupt control register for each of the three timers (T2, T3, T4). All interrupt control registers GPT12E_T2IC, GPT12E_T3IC, and GPT12E_T4IC have the same structure described in section Interrupt Control.

In **Reload Mode**, upon a trigger signal, T3 is loaded with the contents of the respective timer (T2 or T4) and the respective interrupt request flag in register GPT12E_T2IC or GPT12E_T4IC is set.

In **Incremental Interface Mode**, the interrupt request generation can be selected as follows:

- In Rotation Detection Mode ($T3M = 110_B$), an interrupt request is generated each time the count direction of T3 changes.
- In Edge Detection Mode ($T3M = 111_B$), an interrupt request is generated each time a count edge for T3 is detected.

In **Capture Mode**, upon a trigger (selected transition) at the corresponding input pin the content of the core timer T3 are loaded into the auxiliary timer register Tx and the associated interrupt request flag in register GPT12E_T2IC or GPT12E_T4IC will be set.

16.1.7 GPT1 Registers

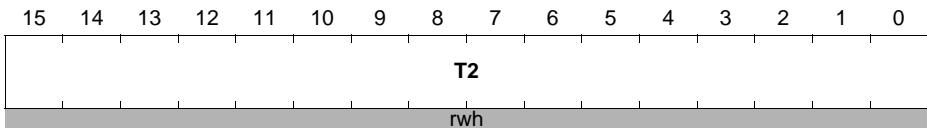
16.1.7.1 GPT1 Timer Registers

GPT12E_T2

Timer T2 Count Register

SFR (FE40_H/20_H)

Reset Value: 0000_H



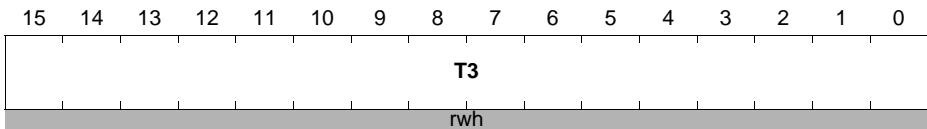
Field	Bits	Typ	Description
T2	[15:0]	rwh	Timer T2 Current Value Contains the current value of the timer T2

GPT12E_T3

Timer T3 Count Register

SFR (FE42_H/21_H)

Reset Value: 0000_H



Field	Bits	Typ	Description
T3	[15:0]	rwh	Timer T3 Current Value Contains the current value of the timer T3

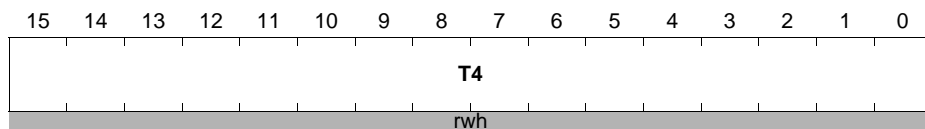
General Purpose Timer Units (GPT12)

GPT12E_T4

Timer T4 Count Register

SFR (FE44_H/22_H)

Reset Value: 0000_H



Field	Bits	Typ	Description
T4	[15:0]	rwh	Timer T4 Current Value Contains the current value of the timer T4

16.1.7.2 GPT1 Timer Control Registers

GPT1 Core Timer T3 Control Register

GPT12E_T3CON

Timer T3 Control Register

SFR (FF42_H/A1_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T3 R DIR	T3 CH DIR	T3 EDG E	BPS1		T3 OTL	T3 OE	T3 UDE	T3 UD	T3 R	T3M			T3I		
rh	rwh	rwh	rw		rwh	rw	rw	rw	rw	rw			rw		

Field	Bits	Type	Description
T3I	[2:0]	rw	Timer T3 Input Parameter Selection Depends on the operating mode, see respective sections for encoding: Table 16-6 for Timer Mode and Gated Timer Mode Table 16-7 for Counter Mode Table 16-9 for Incremental Interface Mode
T3M	[5:3]	rw	Timer T3 Mode Control 000 _B Timer Mode 001 _B Counter Mode 010 _B Gated Timer Mode with gate active low 011 _B Gated Timer Mode with gate active high 100 _B Reserved. Do not use this combination 101 _B Reserved. Do not use this combination 110 _B Incremental Interface Mode (Rotation Detection Mode) 111 _B Incremental Interface Mode (Edge Detection Mode)
T3R	6	rw	Timer T3 Run Bit 0 _B Timer T3 stops 1 _B Timer T3 runs
T3UD	7	rw	Timer T3 Up/Down Control¹⁾ 0 _B Timer T3 counts up 1 _B Timer T3 counts down <i>Note: This bit only controls count direction of T3 if bit T3UDE = 0.</i>

General Purpose Timer Units (GPT12)

Field	Bits	Type	Description
T3UDE	8	rw	Timer T3 External Up/Down Enable¹⁾ 0_B Count direction is controlled by bit T3UD; input T3EUD is disconnected 1_B Count direction is controlled by input T3EUD
T3OE	9	rw	Overflow/Underflow Output Enable 0_B Alternate Output Function Disabled 1_B State of T3 toggle latch is output on pin T3OUT
T3OTL	10	rwh	Timer T3 Overflow Toggle Latch Toggles on each overflow/underflow of T3. Can be set or cleared by software (see separate description)
BPS1	[12:11]	rw	GPT1 Block Prescaler Control Selects the basic clock for block GPT1 (see also Section 16.1.5) 00_B $f_{GPT}/8$ 01_B $f_{GPT}/4$ 10_B $f_{GPT}/32$ 11_B $f_{GPT}/16$
T3EDGE	13	rwh	Timer T3 Edge Detection Flag The bit is set each time a count edge is detected. T3EDGE must be cleared by software. 0_B No count edge was detected 1_B A count edge was detected
T3CHDIR	14	rwh	Timer T3 Count Direction Change Flag This bit is set each time the count direction of timer T3 changes. T3CHDIR must be cleared by software. 0_B No change of count direction was detected 1_B A change of count direction was detected
T3RDIR	15	rh	Timer T3 Rotation Direction Flag 0_B Timer T3 counts up 1_B Timer T3 counts down
0	[31:16]	r	Reserved Read as 0; should be written with 0.

1) See [Table 16-14](#) for encoding of bits T3UD and T3UDE.

General Purpose Timer Units (GPT12)

GPT1 Auxiliary Timers T2/T4 Control Registers

GPT12E_T2CON

Timer T2 Control Register

SFR (FF40_H/A0_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T2 R DIR	T2 CH DIR	T2 EDG E	T2 IR DIS	0		T2 RC	T2 UDE	T2 UD	T2 R	T2M			T2I		
rh	rwh	rwh	rw	r		rw	rw	rw	rw	rw			rw		

Field	Bits	Type	Description
T2I	[2:0]	rw	Timer T2 Input Parameter Selection Depends on the operating mode, see respective sections for encoding: Table 16-6 for Timer Mode and Gated Timer Mode Table 16-8 for Counter Mode Table 16-9 for Incremental Interface Mode
T2M	[5:3]	rw	Timer T2 Mode Control (Basic Operating Mode) 000 _B Timer Mode 001 _B Counter Mode 010 _B Gated Timer Mode with gate active low 011 _B Gated Timer Mode with gate active high 100 _B Reload Mode 101 _B Capture Mode 110 _B Incremental Interface Mode (Rotation Detection Mode) 111 _B Incremental Interface Mode (Edge Detection Mode)
T2R	6	rw	Timer T2 Run Bit 0 _B Timer T2 stops 1 _B Timer T2 runs <i>Note: This bit only controls timer T2 if bit T2RC = 0.</i>
T2UD	7	rw	Timer T2 Up/Down Control¹⁾ 0 _B Timer T2 counts up 1 _B Timer T2 counts down <i>Note: This bit only controls count direction of T2 if bit T2UDE = 0.</i>

General Purpose Timer Units (GPT12)

Field	Bits	Type	Description
T2UDE	8	rw	Timer T2 External Up/Down Enable¹⁾ 0_B Count direction is controlled by bit T2UD; input T2EUD is disconnected 1_B Count direction is controlled by input T2EUD
T2RC	9	rw	Timer T2 Remote Control 0_B Timer T2 is controlled by its own run bit T2R 1_B Timer T2 is controlled by the run bit T3R of core timer T3, not by bit T2R
T2IRDIS	12	rw	Timer T2 Interrupt Disable 0_B Interrupt generation for T2CHDIR and T2EDGE interrupts in Incremental Interface Mode is enabled 1_B Interrupt generation for T2CHDIR and T2EDGE interrupts in Incremental Interface Mode is disabled
T2EDGE	13	rwh	Timer T2 Edge Detection The bit is set each time a count edge is detected. T2EDGE must be cleared by software. 0_B No count edge was detected 1_B A count edge was detected
T2CHDIR	14	rwh	Timer T2 Count Direction Change The bit is set each time the count direction of timer T2 changes. T2CHDIR must be cleared by software. 0_B No change in count direction was detected 1_B A change in count direction was detected
T2RDIR	15	rh	Timer T2 Rotation Direction 0_B Timer T2 counts up 1_B Timer T2 counts down
0	[11:10], [31:16]	r	Reserved Read as 0; should be written with 0.

1) See [Table 16-14](#) for encoding of bits T2UD and T2UDE.

General Purpose Timer Units (GPT12)

GPT12E_T4CON

Timer T4 Control Register

SFR (FF44_H/A2_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T4 R DIR	T4 CH DIR	T4 EDG E	T4 IR DIS	CLR T3 EN	CLR T2 EN	T4 RC	T4 UDE	T4 UD	T4 R	T4M			T4I		
rh	rwh	rwh	rw	rw	rw	rw	rw	rw	rw	rw			rw		

Field	Bits	Type	Description
T4I	[2:0]	rw	Timer T4 Input Parameter Selection Depends on the operating mode, see respective sections for encoding: Table 16-6 for Timer Mode and Gated Timer Mode Table 16-6 for Counter Mode Table 16-9 for Incremental Interface Mode
T4M	[5:3]	rw	Timer T4 Mode Control (Basic Operating Mode) 000 _B Timer Mode 001 _B Counter Mode 010 _B Gated Timer Mode with gate active low 011 _B Gated Timer Mode with gate active high 100 _B Reload Mode 101 _B Capture Mode 110 _B Incremental Interface Mode (Rotation Detection Mode) 111 _B Incremental Interface Mode (Edge Detection Mode)
T4R	6	rw	Timer T4 Run Bit 0 _B Timer T4 stops 1 _B Timer T4 runs <i>Note: This bit only controls timer T4 if bit T4RC = 0.</i>
T4UD	7	rw	Timer T4 Up/Down Control¹⁾ 0 _B Timer T4 counts up 1 _B Timer T4 counts down <i>Note: This bit only controls count direction of T4 if bit T4UDE = 0.</i>

General Purpose Timer Units (GPT12)

Field	Bits	Type	Description
T4UDE	8	rw	Timer T4 External Up/Down Enable¹⁾ 0 _B Count direction is controlled by bit T4UD; input T4EUD is disconnected 1 _B Count direction is controlled by input T4EUD
T4RC	9	rw	Timer T4 Remote Control 0 _B Timer T4 is controlled by its own run bit T4R 1 _B Timer T4 is controlled by the run bit T3R of core timer T3, but not by bit T4R
CLRT2EN	10	rw	Clear Timer T2 Enable Enables the automatic clearing of timer T2 upon a falling edge of the selected T4EUD input. 0 _B No effect of T4EUD on timer T2 1 _B A falling edge on T4EUD clears timer T2
CLRT3EN	11	rw	Clear Timer T3 Enable Enables the automatic clearing of timer T3 upon a falling edge of the selected T4IN input. 0 _B No effect of T4IN on timer T3 1 _B A falling edge on T4IN clears timer T3
T4IRDIS	12	rw	Timer T4 Interrupt Disable 0 _B Interrupt generation for T4CHDIR and T4EDGE interrupts in Incremental Interface Mode is enabled 1 _B Interrupt generation for T4CHDIR and T4EDGE interrupts in Incremental Interface Mode is disabled
T4EDGE	13	rwh	Timer T4 Edge Detection The bit is set each time a count edge is detected. T4EDGE has to be cleared by software. 0 _B No count edge was detected 1 _B A count edge was detected
T4CHDIR	14	rwh	Timer T4 Count Direction Change The bit is set each time the count direction of timer T4 changes. T4CHDIR must be cleared by software. 0 _B No change in count direction was detected 1 _B A change in count direction was detected
T4RDIR	15	rh	Timer T4 Rotation Direction 0 _B Timer T4 counts up 1 _B Timer T4 counts down

General Purpose Timer Units (GPT12)

Field	Bits	Type	Description
0	[31:16]	r	Reserved Read as 0; should be written with 0.

1) See [Table 16-14](#) for encoding of bits T4UD and T4UDE.

Encoding of GPT1 Timer Count Direction Control

Table 16-5 GPT1 Timer Count Direction Control

Pin TxEUD	Bit TxUDE	Bit TxUD	Count Direction	Bit TxRDIR
X	0	0	Count Up	0
X	0	1	Count Down	1
0	1	0	Count Up	0
1	1	0	Count Down	1
0	1	1	Count Down	1
1	1	1	Count Up	0

Timer Mode and Gated Timer Mode: Encoding of GPT1 Overall Prescaler Factor

**Table 16-6 GPT1 Overall Prescaler Factors for Internal Count Clock
(Timer Mode and Gated Timer Mode)**

Individual Prescaler for Tx	Common Prescaler for Module Clock ¹⁾			
	BPS1 = 01 _B	BPS1 = 00 _B	BPS1 = 11 _B	BPS1 = 10 _B
Txl = 000 _B	4	8	16	32
Txl = 001 _B	8	16	32	64
Txl = 010 _B	16	32	64	128
Txl = 011 _B	32	64	128	256
Txl = 100 _B	64	128	256	512
Txl = 101 _B	128	256	512	1024
Txl = 110 _B	256	512	1024	2048
Txl = 111 _B	512	1024	2048	4096

1) Please note the non-linear encoding of bitfield BPS1.

Counter Mode: Encoding of GPT1 Input Edge Selection

Table 16-7 GPT1 Core Timer T3 Input Edge Selection(Counter Mode)

T3I	Triggering Edge for Counter Increment/Decrement
000 _B	None. Counter T3 is disabled
001 _B	Positive transition (rising edge) on T3IN
010 _B	Negative transition (falling edge) on T3IN
011 _B	Any transition (rising or falling edge) on T3IN
1XX _B	Reserved. Do not use this combination

Table 16-8 GPT1 Auxiliary Timers T2/T4 Input Edge Selection(Counter Mode)

T2I/T4I	Triggering Edge for Counter Increment/Decrement
X00 _B	None. Counter Tx is disabled
001 _B	Positive transition (rising edge) on TxIN
010 _B	Negative transition (falling edge) on TxIN
011 _B	Any transition (rising or falling edge) on TxIN
101 _B	Positive transition (rising edge) of T3 toggle latch T3OTL
110 _B	Negative transition (falling edge) of T3 toggle latch T3OTL
111 _B	Any transition (rising or falling edge) of T3 toggle latch T3OTL

Incremental Interface Mode: Encoding of Input Edge Selection

**Table 16-9 GPT1 Core Timer T3 Input Edge Selection
(Incremental Interface Mode)**

T3I	Triggering Edge for Counter Increment/Decrement
000 _B	None. Counter T3 stops.
001 _B	Any transition (rising or falling edge) on T3IN.
010 _B	Any transition (rising or falling edge) on T3EUD.
011 _B	Any transition (rising or falling edge) on any T3 input (T3IN or T3EUD).
1XX _B	Reserved. Do not use this combination.

16.1.7.3 GPT1 Timer Interrupt Control Registers

There is an interrupt control register for each of the three timers (T2, T3, T4). All interrupt control registers GPT12E_T2IC, GPT12E_T3IC, and GPT12E_T4IC have the same structure described in section Interrupt Control.

General Purpose Timer Units (GPT12)

16.2 Timer Block GPT2

From a programmer's point of view, the GPT2 block is represented by a set of SFRs as summarized below. Those portions of port and direction registers which are used for alternate functions by the GPT2 block are shaded.

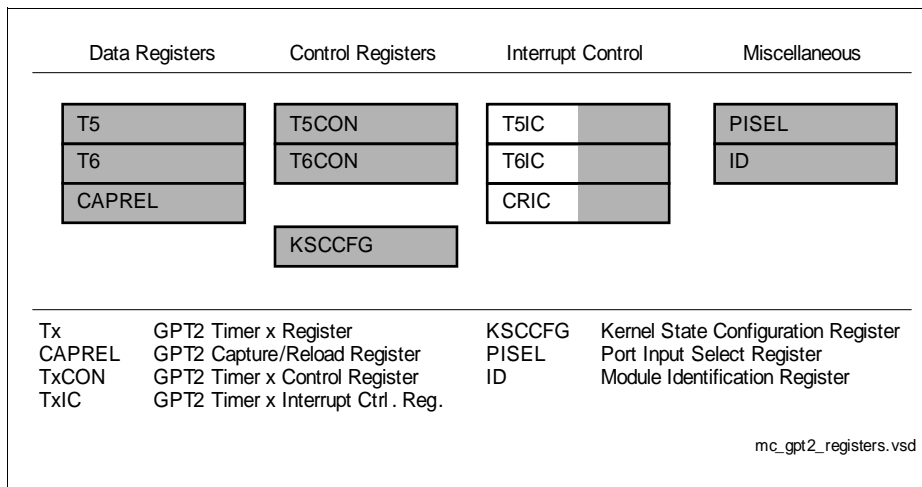


Figure 16-19 SFRs Associated with Timer Block GPT2

Both timers of block GPT2 (T5, T6) can run in one of 3 basic modes: Timer Mode, Gated Timer Mode, or Counter Mode. All timers can count up or down. Each timer of GPT2 is controlled by a separate control register TxCON.

Each timer has an input pin TxIN (alternate pin function) associated with it, which serves as the gate control in Gated Timer Mode, or as the count input in Counter Mode. The count direction (up/down) may be programmed via software or may be dynamically altered by a signal at the External Up/Down control input TxEUD (alternate pin function). An overflow/underflow of core timer T6 is indicated by the Output Toggle Latch T6OTL, whose state may be output on the associated pin T6OUT (alternate pin function). The auxiliary timer T5 may additionally be concatenated with core timer T6 (through T6OTL).

The Capture/Reload register CAPREL can be used to capture the contents of timer T5, or to reload timer T6. A special mode facilitates the use of register CAPREL for both functions at the same time. This mode allows frequency multiplication. The capture function is triggered by the input pin CAPIN, or by GPT1 timer's T3 input lines T3IN and T3EUD. The reload function is triggered by an overflow or underflow of timer T6. Overflows/underflows of timer T6 may also clock the timers of the CAPCOM units.

The current contents of each timer can be read or modified by the CPU by accessing the corresponding timer count registers T5 or T6, located in the non-bitaddressable SFR

General Purpose Timer Units (GPT2)

space (see [Section 16.2.8.1](#)). When any of the timer registers is written to by the CPU in the state immediately preceding a timer increment, decrement, reload, or capture operation, the CPU write operation has priority in order to guarantee correct results.

The interrupts of GPT2 are controlled through the Interrupt Control Registers TxIC. These registers are not part of the GPT2 block.

The input and output lines of GPT2 are connected to pins. The control registers for the port functions are located in the respective port modules.

Note: The timing requirements for external input signals can be found in [Section 16.2.6](#), [Section 16.5.1](#) summarizes the module interface signals, including pins.

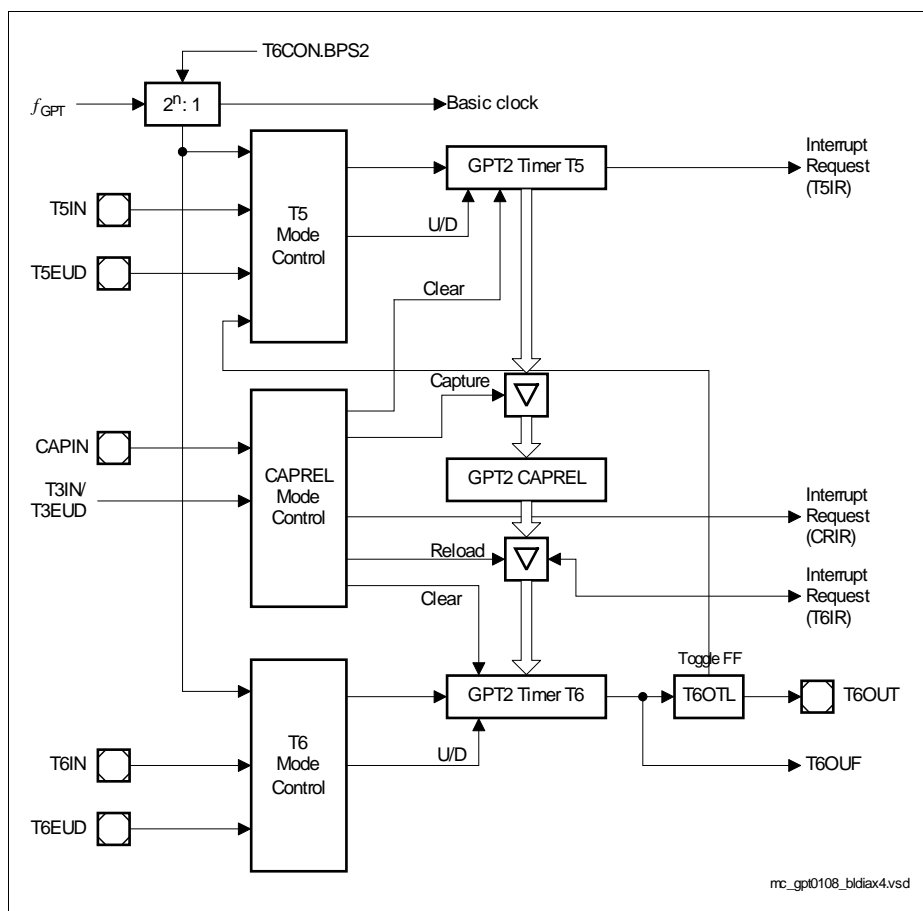


Figure 16-20 GPT2 Block Diagram

16.2.1 GPT2 Core Timer T6 Control

The current contents of the core timer T6 are reflected by its count register T6. This register can also be written to by the CPU, for example, to set the initial start value.

The core timer T6 is configured and controlled via its bitaddressable control register T6CON.

Timer T6 Run Control

The core timer T6 can be started or stopped by software through bit T6R (timer T6 run bit). This bit is relevant in all operating modes of T6. Setting bit T6R will start the timer, clearing bit T6R stops the timer.

In Gated Timer Mode, the timer will only run if T6R = 1 and the gate is active (high or low, as programmed).

Note: When bit T5RC in timer control register T5CON is set, bit T6R will also control (start and stop) the Auxiliary Timer T5.

Count Direction Control

The count direction of the GPT2 timers (core timer and auxiliary timer) can be controlled either by software or by the external input pin TxEUD (Timer Tx External Up/Down Control Input). These options are selected by bits TxUD and TxUDE in the respective control register TxCON. When the up/down control is provided by software (bit TxUDE = 0), the count direction can be altered by setting or clearing bit TxUD. When bit TxUDE = 1, pin TxEUD is selected to be the controlling source of the count direction. However, bit TxUD can still be used to reverse the actual count direction, as shown in [Table 16-14](#). The count direction can be changed regardless of whether or not the timer is running.

Note: When pin TxEUD is used as external count direction control input, it must be configured as input.

Timer T6 Output Toggle Latch

The overflow/underflow signal of timer T6 is connected to a block named 'Toggle Latch', shown in the Timer Mode diagrams. **Figure 16-21** illustrates the details of this block. An overflow or underflow of T6 will clock two latches: The first latch represents bit T6OTL in control register T6CON. The second latch is an internal latch toggled by T6OTL's output. Both latch outputs are connected to the input control block of the auxiliary timer T5. The output level of the shadow latch will match the output level of T6OTL, but is delayed by one clock cycle. When the T6OTL value changes, this will result in a temporarily different output level from T6OTL and the shadow latch, which can trigger the selected count event in T5.

When software writes to T6OTL, both latches are set or cleared simultaneously. In this case, both signals to the auxiliary timers carry the same level and no edge will be detected. Bit T6OE (overflow/underflow output enable) in register T6CON enables the state of T6OTL to be monitored via an external pin T6OUT. When T6OTL is linked to an external port pin (must be configured as output), T6OUT can be used to control external HW. If T6OE = 1, pin T6OUT outputs the state of T6OTL. If T6OE = 0, pin T6OUT outputs a high level (while it selects the timer output signal).

As can be seen from **Figure 16-21**, when latch T6OTL is modified by software to determine the state of the output line, also the internal shadow latch is set or cleared accordingly. Therefore, no trigger condition is detected by T5 in this case.

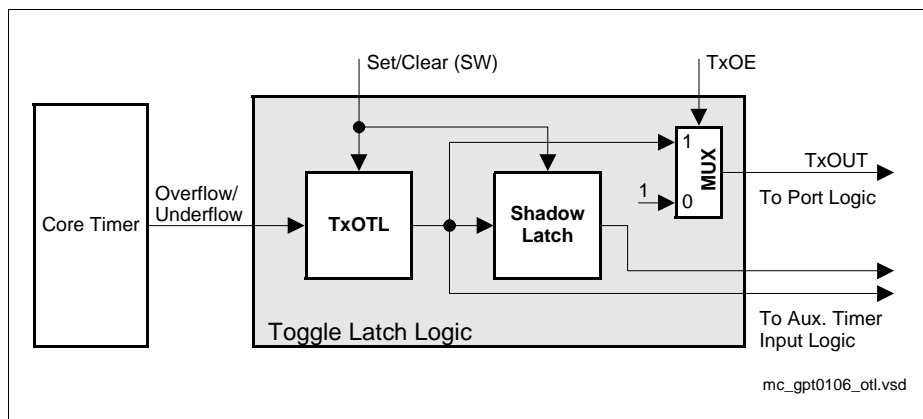


Figure 16-21 Block Diagram of the Toggle Latch Logic of Core Timer T6 (x = 6)

Note: T6 is also used to clock the timers in the CAPCOM units. For this purpose, there is a direct internal connection between the T6 overflow/underflow line and the CAPCOM timers (signal T6OUF).

16.2.2 GPT2 Core Timer T6 Operating Modes

Timer T6 can operate in one of several modes.

Timer T6 in Timer Mode

Timer mode for the core timer T6 is selected by setting bitfield T6M in register T6CON to 000_B. In this mode, T6 is clocked with the module's input clock f_{GPT} divided by two programmable prescalars controlled by bitfields BPS2 and T6I in register T6CON. Please see [Section 16.2.6](#) for details on the input clock options.

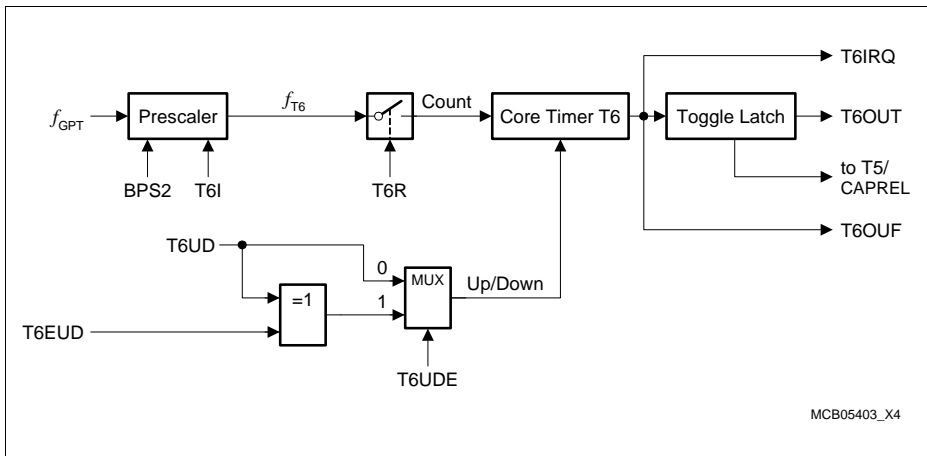


Figure 16-22 Block Diagram of Core Timer T6 in Timer Mode

Timer T6 in Gated Timer Mode

Gated Timer Mode for the core timer T6 is selected by setting bitfield T6M in register T6CON to 010_B or 011_B. Bit T6M.0 (T6CON.3) selects the active level of the gate input. The same options for the input frequency are available in Gated Timer Mode as in Timer Mode (see [Section 16.2.6](#)). However, the input clock to the timer in this mode is gated by the external input pin T6IN (Timer T6 External Input).

To enable this operation, the associated pin T6IN must be configured as input.

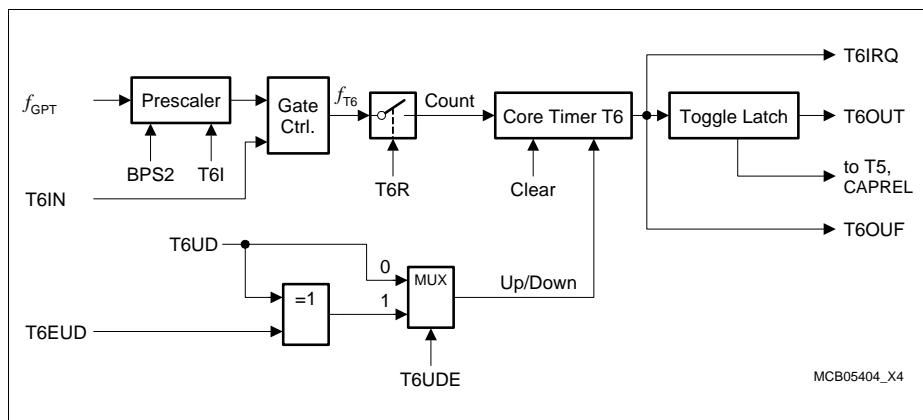


Figure 16-23 Block Diagram of Core Timer T6 in Gated Timer Mode

If T6M = 010_B, the timer is enabled when T6IN shows a low level. A high level at this line stops the timer. If T6M = 011_B, line T6IN must have a high level in order to enable the timer. Additionally, the timer can be turned on or off by software using bit T6R. The timer will only run if T6R is 1 and the gate is active. It will stop if either T6R is 0 or the gate is inactive.

Note: A transition of the gate signal at pin T6IN does not cause an interrupt request.

Timer T6 in Counter Mode

Counter Mode for the core timer T6 is selected by setting bitfield T6M in register T6CON to 001_B . In Counter Mode, timer T6 is clocked by a transition at the external input pin T6IN. The event causing an increment or decrement of the timer can be a positive, a negative, or both a positive and a negative transition at this line. Bitfield T6I in control register T6CON selects the triggering transition (see [Table 16-16](#)).

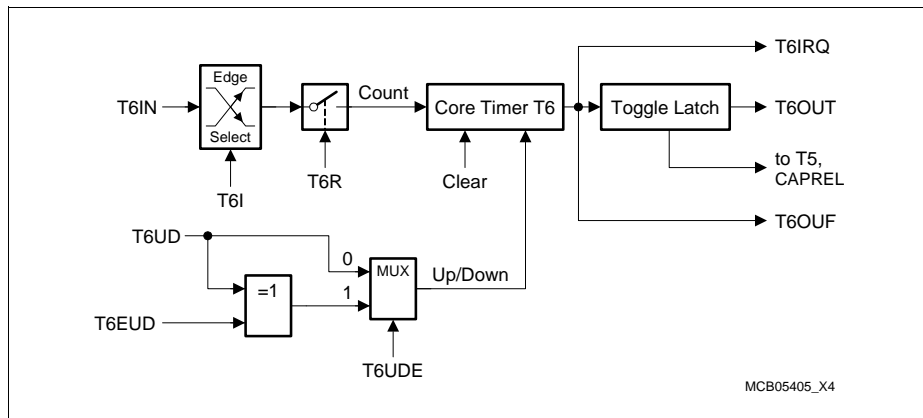


Figure 16-24 Block Diagram of Core Timer T6 in Counter Mode

For Counter Mode operation, pin T6IN must be configured as input. The maximum input frequency allowed in Counter Mode depends on the selected prescaler value. To ensure that a transition of the count input signal applied to T6IN is recognized correctly, its level must be held high or low for a minimum number of module clock cycles before it changes. This information can be found in [Section 16.2.6](#).

16.2.3 GPT2 Auxiliary Timer T5 Control

Auxiliary timer T5 can be configured for Timer Mode, Gated Timer Mode, or Counter Mode with the same options for the timer frequencies and the count signal as the core timer T6. In addition to these 3 counting modes, the auxiliary timer can be concatenated with the core timer. The contents of T5 may be captured to register CAPREL upon an external or an internal trigger. The start/stop function of the auxiliary timers can be remotely controlled by the T6 run control bit. Several timers may thus be controlled synchronously.

The current contents of the auxiliary timer are reflected by its count register T5. This register can also be written to by the CPU, for example, to set the initial start value.

The individual configurations for timer T5 are determined by its bitaddressable control register T5CON. Some bits in this register also control the function of the CAPREL register. Note that functions which are present in all timers of block GPT2 are controlled in the same bit positions and in the same manner in each of the specific control registers.

Note: The auxiliary timer has no output toggle latch and no alternate output function.

Timer T5 Run Control

The auxiliary timer T5 can be started or stopped by software in two different ways:

- Through the associated timer run bit (T5R). In this case it is required that the respective control bit T5RC = 0.
- Through the core timer's run bit (T6R). In this case the respective remote control bit must be set (T5RC = 1).

The selected run bit is relevant in all operating modes of T5. Setting the bit will start the timer, clearing the bit stops the timer.

In Gated Timer Mode, the timer will only run if the selected run bit is set and the gate is active (high or low, as programmed).

Note: If remote control is selected T6R will start/stop timer T6 and the auxiliary timer T5 synchronously.

16.2.4 GPT2 Auxiliary Timer T5 Operating Modes

The operation of the auxiliary timer in the basic operating modes is almost identical with the core timer's operation, with very few exceptions. Additionally, some combined operating modes can be selected.

Timer T5 in Timer Mode

Timer Mode for the auxiliary timer T5 is selected by setting its bitfield T5M in register T5CON to 000_B.

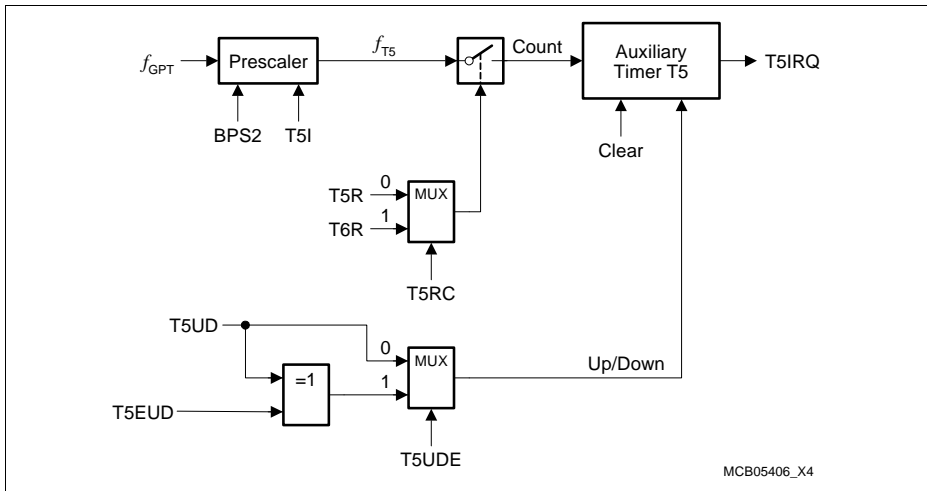


Figure 16-25 Block Diagram of Auxiliary Timer T5 in Timer Mode

General Purpose Timer Units (GPT12)

Timer T5 in Gated Timer Mode

Gated Timer Mode for the auxiliary timer T5 is selected by setting bitfield T5M in register T5CON to 010_B or 011_B. Bit T5M.0 (T5CON.3) selects the active level of the gate input.

Note: A transition of the gate signal at line T5IN does not cause an interrupt request.

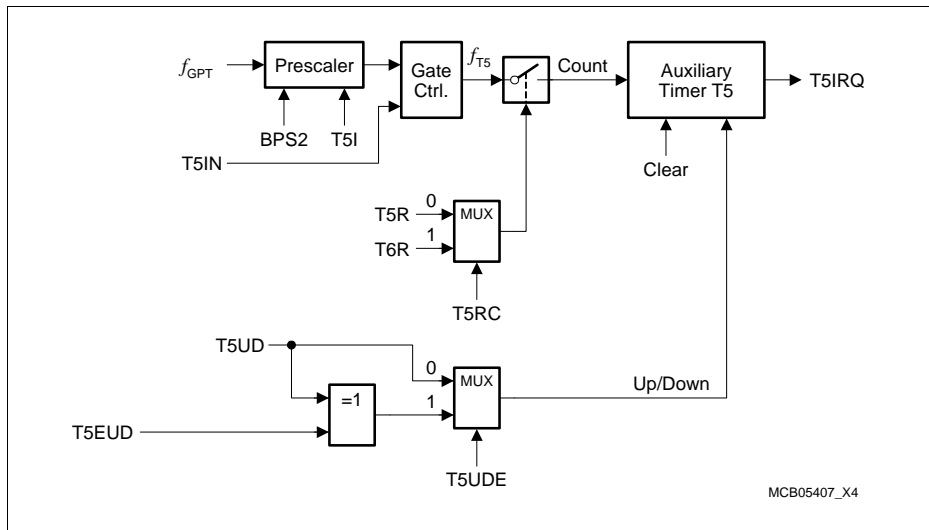


Figure 16-26 Block Diagram of Auxiliary Timer T5 in Gated Timer Mode

Note: There is no output toggle latch for T5.

Start/stop of the auxiliary timer can be controlled locally or remotely.

General Purpose Timer Units (GPT12)

Timer T5 in Counter Mode

Counter Mode for auxiliary timer T5 is selected by setting bitfield T5M in register T5CON to 001_B. In Counter Mode, the auxiliary timer can be clocked either by a transition at its external input line T5IN, or by a transition of timer T6's toggle latch T6OTL. The event causing an increment or decrement of a timer can be a positive, a negative, or both a positive and a negative transition at either the respective input pin or at the toggle latch. Bitfield T5I in control register T5CON selects the triggering transition (see [Table 16-17](#)).

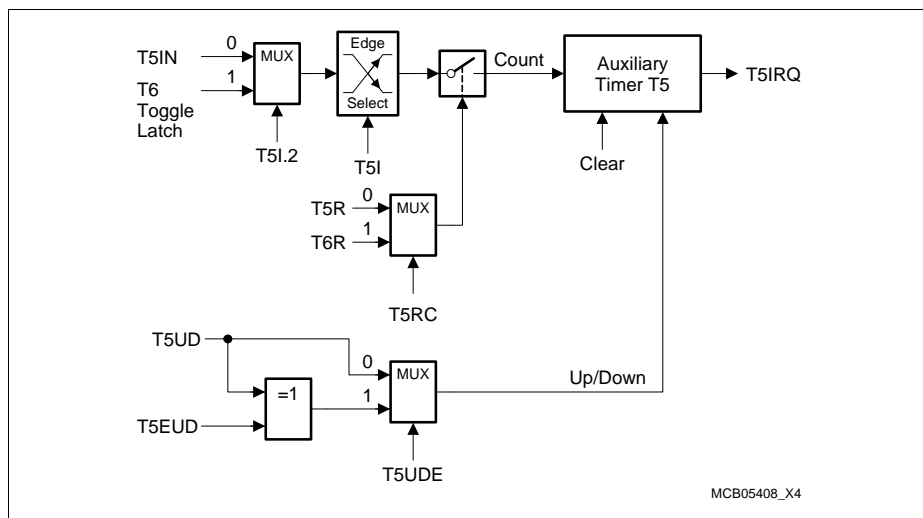


Figure 16-27 Block Diagram of Auxiliary Timer T5 in Counter Mode

Note: Only state transitions of T6OTL which are caused by the overflows/underflows of T6 will trigger the counter function of T5. Modifications of T6OTL via software will NOT trigger the counter function of T5.

For counter operation, pin T5IN must be configured as input. The maximum input frequency allowed in Counter Mode depends on the selected prescaler value. To ensure that a transition of the count input signal applied to T5IN is recognized correctly, its level must be held high or low for a minimum number of module clock cycles before it changes. This information can be found in [Section 16.2.6](#).

Timer Concatenation

Using the toggle bit T6OTL as a clock source for the auxiliary timer in Counter Mode concatenates the core timer T6 with the auxiliary timer T5. This concatenation forms either a 32-bit or a 33-bit timer/counter, depending on which transition of T6OTL is selected to clock the auxiliary timer.

General Purpose Timer Units (GPT12)

- **32-bit Timer/Counter:** If both a positive and a negative transition of T6OTL are used to clock the auxiliary timer, this timer is clocked on every overflow/underflow of the core timer T6. Thus, the two timers form a 32-bit timer.
- **33-bit Timer/Counter:** If either a positive or a negative transition of T6OTL is selected to clock the auxiliary timer, this timer is clocked on every second overflow/underflow of the core timer T6. This configuration forms a 33-bit timer (16-bit core timer + T6OTL + 16-bit auxiliary timer).
 As long as bit T6OTL is not modified by software, it represents the state of the internal toggle latch, and can be regarded as part of the 33-bit timer.

The count directions of the two concatenated timers are not required to be the same. This offers a wide variety of different configurations.

T6, which represents the low-order part of the concatenated timer, can operate in Timer Mode, Gated Timer Mode or Counter Mode in this case.

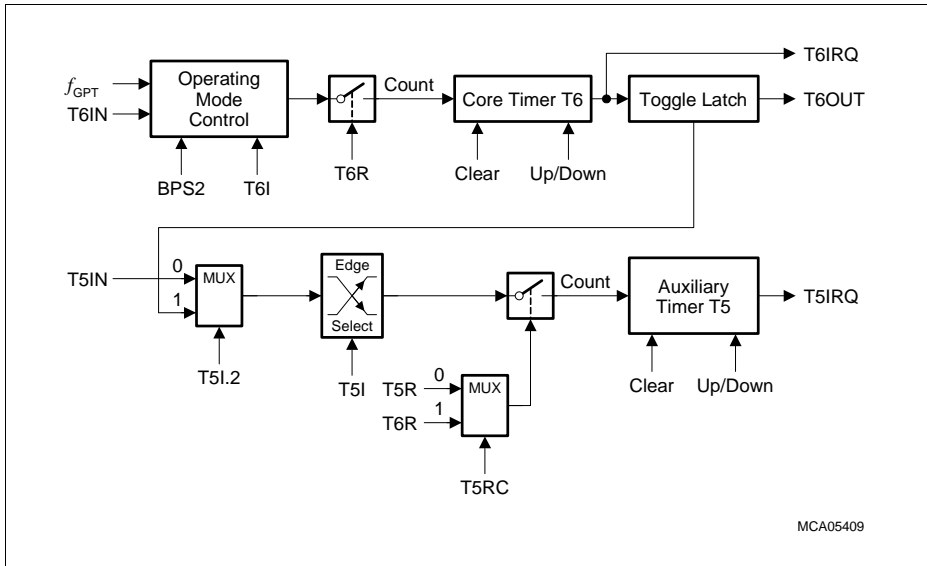


Figure 16-28 Concatenation of Core Timer T6 and Auxiliary Timer T5

16.2.5 GPT2 Register CAPREL Operating Modes

The Capture/Reload register CAPREL can be used to capture the contents of timer T5, or to reload timer T6. A special mode facilitates the use of register CAPREL for both functions at the same time. This mode allows frequency multiplication. The capture function is triggered by CAPIN, by T3IN and T3EUD, or by read GPT1 timers. The reload function is triggered by an overflow or underflow of timer T6.

In addition to the capture function, the capture trigger signal can also be used to clear the contents of timers T5 and T6 individually.

The functions of register CAPREL are controlled via several bit(field)s in the timer control registers T5CON and T6CON.

Capture/Reload Register CAPREL in Capture Mode

Capture mode for register CAPREL is selected by setting bit T5SC in control register T5CON (set bitfield CI in register T5CON to a non-zero value to select a trigger signal). In capture mode, the contents of the auxiliary timer T5 are latched into register CAPREL in response to a signal transition at the selected external input pin(s). Bit CT3 selects the external input line CAPIN or the input lines T3IN and/or T3EUD of GPT1 timer T3 as the source for a capture trigger. Either a positive, a negative, or both a positive and a negative transition at line CAPIN can be selected to trigger the capture function, or transitions on input T3IN or input T3EUD or both inputs, T3IN and T3EUD. The active edge is controlled by bitfield CI in register T5CON. [Table 16-10](#) summarizes these options.

Table 16-10 CAPREL Register Input Edge Selection

CT3	CI	Triggering Signal/Edge for Capture Mode
X	00 _B	None. Capture Mode is disabled.
0	01 _B	Positive transition (rising edge) on CAPIN. ¹⁾
0	10 _B	Negative transition (falling edge) on CAPIN.
0	11 _B	Any transition (rising or falling edge) on CAPIN.
1	01 _B	Any transition (rising or falling edge) on T3IN.
1	10 _B	Any transition (rising or falling edge) on T3EUD.
1	11 _B	Any transition (rising or falling edge) on T3IN or T3EUD.

1) Rising edge must be selected if capturing is triggered by the internal GPT1 read signals (see register PISEL and [“Combined Capture Modes” on Page 16-58](#)).

General Purpose Timer Units (GPT12)

Incremental Interface Mode, in order to derive dynamic information (speed, acceleration) from the input signals.

For capture mode operation, the selected pins CAPIN, T3IN, or T3EUD must be configured as input. To ensure that a transition of a trigger input signal applied to one of these inputs is recognized correctly, its level must be held high or low for a minimum number of module clock cycles, detailed in [Section 16.2.6](#).

Capture/Reload Register CAPREL in Reload Mode

Reload mode for register CAPREL is selected by setting bit T6SR in control register T6CON. In reload mode, the core timer T6 is reloaded with the contents of register CAPREL, triggered by an overflow or underflow of T6. This will not activate the interrupt request line CRIRQ associated with the CAPREL register. However, interrupt request line T6IRQ will be activated, indicating the overflow/underflow of T6.

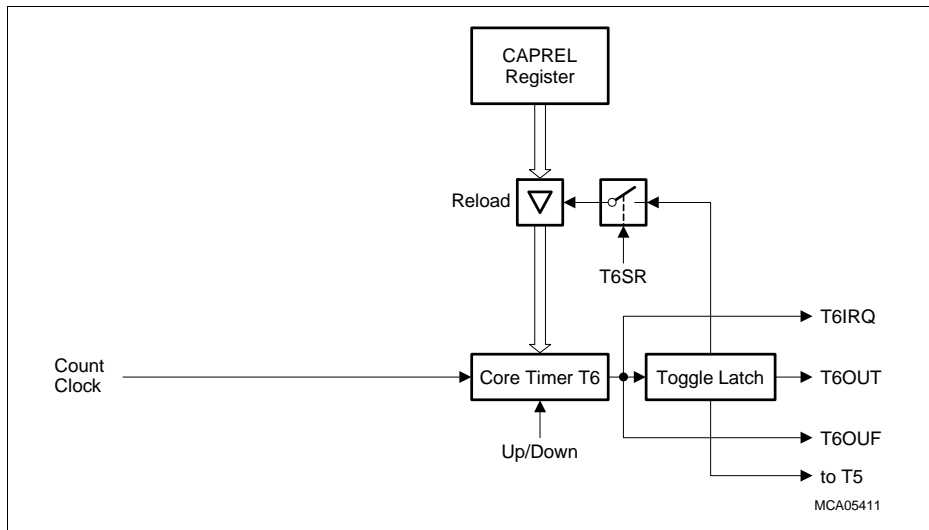


Figure 16-30 Capture/Reload Register CAPREL in Reload Mode

General Purpose Timer Units (GPT12)

Capture/Reload Register CAPREL in Capture-And-Reload Mode

Since the reload function and the capture function of register CAPREL can be enabled individually by bits T5SC and T6SR, the two functions can be enabled simultaneously by setting both bits. This feature can be used to generate an output frequency that is a multiple of the input frequency.

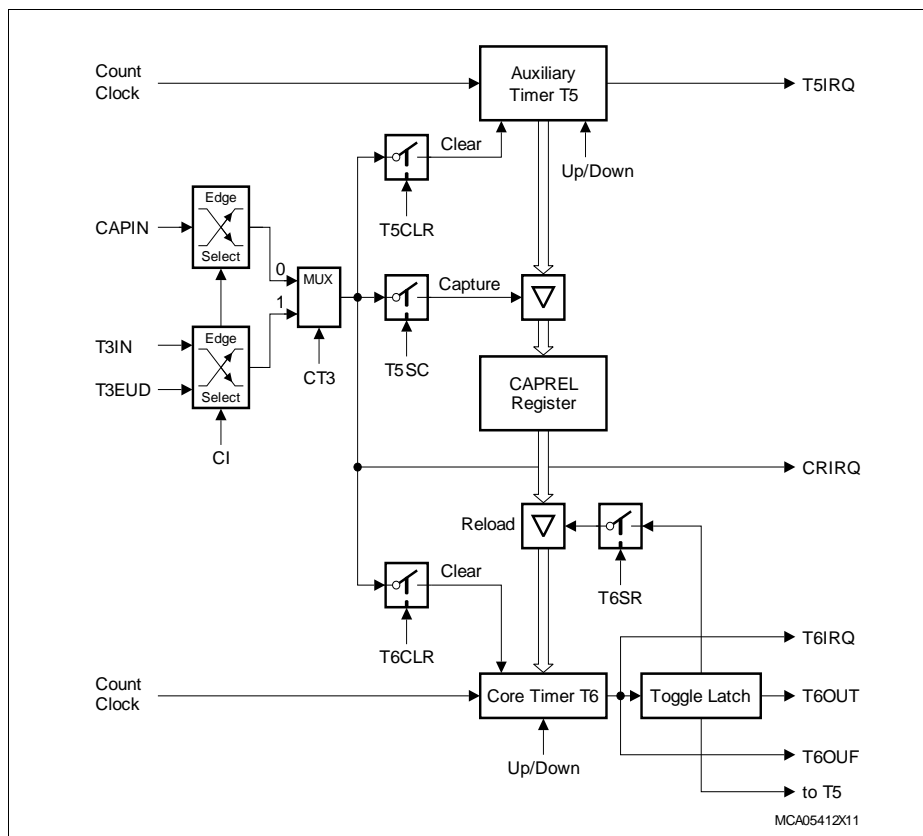


Figure 16-31 Capture/Reload Register CAPREL in Capture-And-Reload Mode

This combined mode can be used to detect consecutive external events which may occur aperiodically, but where a finer resolution, that means, more 'ticks' within the time between two external events is required.

For this purpose, the time between the external events is measured using timer T5 and the CAPREL register. Timer T5 runs in Timer Mode counting up with a frequency of e.g. $f_{GPT}/32$. The external events are applied to pin CAPIN. When an external event occurs,

General Purpose Timer Units (GPT12)

the contents of timer T5 are latched into register CAPREL and timer T5 is cleared (T5CLR = 1). Thus, register CAPREL always contains the correct time between two events, measured in timer T5 increments. Timer T6, which runs in Timer Mode counting down with a frequency of e.g. $f_{GPT}/4$, uses the value in register CAPREL to perform a reload on underflow. This means, the value in register CAPREL represents the time between two underflows of timer T6, now measured in timer T6 increments. Since (in this example) timer T6 runs 8 times faster than timer T5, it will underflow 8 times within the time between two external events. Thus, the underflow signal of timer T6 generates 8 'ticks'. Upon each underflow, the interrupt request line T6IRQ will be activated and bit T6OTL will be toggled. The state of T6OTL may be output on pin T6OUT. This signal has 8 times more transitions than the signal which is applied to pin CAPIN.

Note: The underflow signal of Timer T6 can furthermore be used to clock one or more of the timers of the CAPCOM units, which gives the user the possibility to set compare events based on a finer resolution than that of the external events. This connection is accomplished via signal T6OUF.

Capture Correction

A certain deviation of the output frequency is generated by the fact that timer T5 will count actual time units (e.g. T5 running at 1 MHz will count up to the value $64_H/100_D$ for a 10 kHz input signal), while T6OTL will only toggle upon an underflow of T6 (i.e. the transition from 0000_H to $FFFF_H$). In the above mentioned example, T6 would count down from 64_H , so the underflow would occur after 101 timing ticks of T6. The actual output frequency then is 79.2 kHz, instead of the expected 80 kHz.

This deviation can be compensated for by using T6 overflows. In this case, T5 counts down and T6 counts up. Upon a signal transition on pin CAPIN, the count value in T5 is captured into CAPREL and T5 is cleared to 0000_H . In its next clock cycle, T5 underflows to $FFFF_H$, and continues to count down with the following clocks. T6 is reloaded from CAPREL upon an overflow, and continues to count up with its following clock cycles (8 times faster in the above example). In this case, T5 and T6 count the same number of steps with their respective internal count frequency.

In the above example, T5 running at 1 MHz will count down to the value $FF9C_H/-100_D$ for a 10 kHz input signal applied at CAPIN, while T6 counts up from $FF9C_H$ through $FFFF_H$ to 0000_H . So the overflow occurs after 100 timing ticks of T6, and the actual output frequency at T6OUT then is the expected 80 kHz.

However, in this case CAPREL does not directly contain the time between two CAPIN events, but rather its 2's complement. Software will have to convert this value, if it is required for the operation.

Combined Capture Modes

For incremental interface applications in particular, several timer features can be combined to obtain dynamic information such as speed, acceleration, or deceleration. The current position itself can be obtained directly from the timer register (T2, T3, T4).

The time information to determine the dynamic parameters is generated by capturing the contents of the free-running timer T5 into register CAPREL. Two trigger sources for this event can be selected:

- Capture trigger on sensor signal transitions
- Capture trigger on position read operations

Capturing on sensor signal transitions is available for timer T3 inputs. This mode is selected by setting bit CT3 and selecting the intended signal(s) via bitfield CI in register T5CON. CAPREL then indicates the time between two selected transitions (measured in T5 counts).

Capturing on position read operations is available for timers T2, T3, and T4. This mode is selected by clearing bit CT3 and selecting the rising edge via bitfield CI in register T5CON. Bitfield ISCAPIN in register PISEL then selects either a read access from T3 or a read access from any of T2 or T3 or T4. CAPREL then indicates the time between two read accesses.

These operating modes directly support the measurement of position and rotational speed. Acceleration and deceleration can then be determined by evaluating subsequent speed measurements.

General Purpose Timer Units (GPT12)

16.2.6 GPT2 Clock Signal Control

All actions within the timer block GPT2 are triggered by transitions of its basic clock. This basic clock is derived from the module clock f_{GPT} by a basic block prescaler, controlled by bitfield BPS2 in register T6CON (see [Figure 16-20](#)). The count clock can be generated in two different ways:

- **Internal count clock**, derived from GPT2's basic clock via a programmable prescaler, is used for (gated) Timer Mode.
- **External count clock**, derived from the timer's input pin(s), is used for Counter Mode.

For both ways, the basic clock determines the maximum count frequency and the timer's resolution:

Table 16-11 Basic Clock Selection for Block GPT2

Block Prescaler ¹⁾	BPS2 = 01 _B	BPS2 = 00 _B ²⁾	BPS2 = 11 _B	BPS2 = 10 _B
Prescaling Factor for GPT2: F(BPS2)	F(BPS2) = 2	F(BPS2) = 4	F(BPS2) = 8	F(BPS2) = 16
Maximum External Count Frequency	$f_{GPT}/4$	$f_{GPT}/8$	$f_{GPT}/16$	$f_{GPT}/32$
Input Signal Stable Time	$2 \times t_{GPT}$	$4 \times t_{GPT}$	$8 \times t_{GPT}$	$16 \times t_{GPT}$

1) Please note the non-linear encoding of bitfield BPS2.

2) Default after reset.

Note: When initializing the GPT2 block, and the block prescaler BPS2 in T6CON needs to be set to a value different from its reset value (00_B), it must be initialized first before any mode involving external trigger signals is configured. These modes include counter, capture, and reload mode. Otherwise, unintended count/capture/reload events may occur.
In this case (e.g. when changing BPS2 during operation of the GPT2 block), disable related interrupts before modification of BPS2, and afterwards clear the corresponding service request flags and re-initialize those registers (T5, T6, CAPREL) that might be affected by a count/capture/reload event.

Internal Count Clock Generation

In Timer Mode and Gated Timer Mode, the count clock for each GPT2 timer is derived from the GPT2 basic clock by a programmable prescaler, controlled by bitfield TxI in the respective timer's control register TxCON.

General Purpose Timer Units (GPT12)

The count frequency f_{Tx} for a timer Tx and its resolution r_{Tx} are scaled linearly with lower clock frequencies, as can be seen from the following formula:

$$f_{Tx} = \frac{f_{GPT}}{F(BPS2) \times 2^{<Tx>}} \quad r_{Tx}[\mu s] = \frac{F(BPS2) \times 2^{<Tx>}}{f_{GPT}[MHz]} \quad (16.2)$$

The effective count frequency depends on the common module clock prescaler factor $F(BPS2)$ as well as on the individual input prescaler factor $2^{<Tx>}$. **Table 16-15** summarizes the resulting overall divider factors for a GPT2 timer that result from these cascaded prescalers.

Table 16-12 lists GPT2 timer's parameters (such as count frequency, resolution, and period) resulting from the selected overall prescaler factor and the module clock f_{GPT} . Note that some numbers may be rounded.

Table 16-12 GPT2 Timer Parameters

System Clock = 10 MHz			Overall Divider Factor	System Clock = 40 MHz		
Frequency	Resolution	Period		Frequency	Resolution	Period
5.0 MHz	200 ns	13.11 ms	2	20.0 MHz	50 ns	3.28 ms
2.5 MHz	400 ns	26.21 ms	4	10.0 MHz	100 ns	6.55 ms
1.25 MHz	800 ns	52.43 ms	8	5.0 MHz	200 ns	13.11 ms
625.0 kHz	1.6 μs	104.9 ms	16	2.5 MHz	400 ns	26.21 ms
312.5 kHz	3.2 μs	209.7 ms	32	1.25 MHz	800 ns	52.43 ms
156.25 kHz	6.4 μs	419.4 ms	64	625.0 kHz	1.6 μs	104.9 ms
78.125 kHz	12.8 μs	838.9 ms	128	312.5 kHz	3.2 μs	209.7 ms
39.06 kHz	25.6 μs	1.678 s	256	156.25 kHz	6.4 μs	419.4 ms
19.53 kHz	51.2 μs	3.355 s	512	78.125 kHz	12.8 μs	838.9 ms
9.77 kHz	102.4 μs	6.711 s	1024	39.06 kHz	25.6 μs	1.678 s
4.88 kHz	204.8 μs	13.42 s	2048	19.53 kHz	51.2 μs	3.355 s

External Count Clock Input

The external input signals of the GPT2 block are sampled with the GPT2 basic clock (see **Figure 16-20**). To ensure that a signal is recognized correctly, its current level (high or low) must be held active for at least one complete sampling period, before changing. A signal transition is recognized if two subsequent samples of the input signal represent different levels. Therefore, a minimum of two basic clock periods are required for the sampling of an external input signal. Thus, the maximum frequency of an input signal must not be higher than half the basic clock.

General Purpose Timer Units (GPT12)

Table 16-13 summarizes the resulting requirements for external GPT2 input signals.

Table 16-13 GPT2 External Input Signal Limits

GPT2 Basic Clock = 10 MHz		Input Frequ. Factor	GPT2 Divider BPS2	Input Phase Duration	GPT2 Basic Clock = 40 MHz	
Max. Input Frequency	Min. Level Hold Time				Max. Input Frequency	Min. Level Hold Time
2.5 MHz	200 ns	$f_{\text{GPT}}/4$	01 _B	$2 \times t_{\text{GPT}}$	10.0 MHz	50 ns
1.25 MHz	400 ns	$f_{\text{GPT}}/8$	00 _B	$4 \times t_{\text{GPT}}$	5.0 MHz	100 ns
625.0 kHz	800 ns	$f_{\text{GPT}}/16$	11 _B	$8 \times t_{\text{GPT}}$	2.5 MHz	200 ns
312.5 kHz	1.6 μs	$f_{\text{GPT}}/32$	10 _B	$16 \times t_{\text{GPT}}$	1.25 MHz	400 ns

These limitations are valid for all external input signals to GPT2, including the external count signals in Counter Mode and the gate input signals in Gated Timer Mode.

16.2.7 Interrupt Control for GPT2 Timers and CAPREL

When a timer overflows from $FFFF_H$ to 0000_H (when counting up), or when it underflows from 0000_H to $FFFF_H$ (when counting down), its interrupt request flag in register GPT12E_T5IC or GPT12E_T6IC will be set. This will cause an interrupt to the respective timer interrupt vector or trigger a PEC service, if the respective interrupt enable bit is set.

Whenever a transition according to the selection in bit field CI is detected at pin CAPIN, interrupt request flag in register GPT12E_CRIC is set. Setting any request flag will cause an interrupt to the respective timer or CAPREL interrupt vector or trigger a PEC service, if the respective interrupt enable bit is set.

There is an interrupt control register for each of the two timers (T5, T6) and for the CAPREL register. All interrupt control registers have the same structure described in section Interrupt Control.

16.2.8 GPT2 Registers

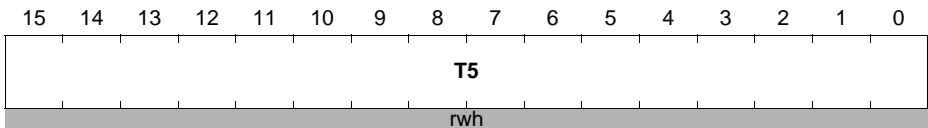
16.2.8.1 GPT2 Timer Registers

GPT12E_T5

Timer 5 Count Register

SFR (FE46_H/23_H)

Reset Value: 0000_H



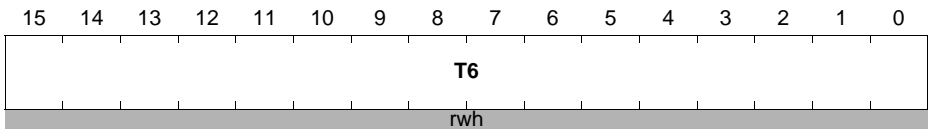
Field	Bits	Typ	Description
T5	[15:0]	rwh	Timer T5 Current Value Contains the current value of the timer T5

GPT12E_T6

Timer T6 Count Register

SFR (FE48_H/24_H)

Reset Value: 0000_H



Field	Bits	Typ	Description
T6	[15:0]	rwh	Timer T6 Current Value Contains the current value of the timer T6

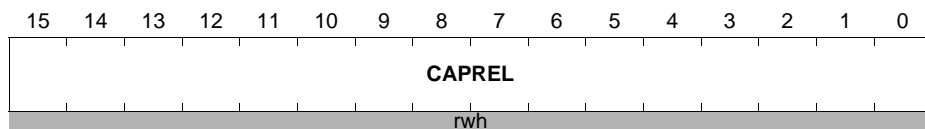
General Purpose Timer Units (GPT12)

GPT12E_CAPREL

Capture/Reload Register

SFR (FE4A_H/25_H)

Reset Value: 0000_H



Field	Bits	Typ	Description
CAPREL	[15:0]	rwh	Current reload value or Captured value Contains the current value of the CAPREL register

16.2.8.2 GPT2 Timer Control Registers

GPT2 Core Timer T6 Control Register

GPT12E_T6CON

Timer T6 Control Register

SFR (FF48_H/A4_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T6 SR	T6 CLR	-	BPS2	T6 OTL	T6 OE	T6 UDE	T6 UD	T6R	T6M			T6I			
rw	rw	-	rw	rwh	rw	rw	rw	rw		rw			rw		

Field	Bits	Type	Description
T6I	[2:0]	rw	Timer T6 Input Parameter Selection Depends on the operating mode, see respective sections for encoding: Table 16-15 for Timer Mode and Gated Timer Mode Table 16-16 for Counter Mode
T6M	[5:3]	rw	Timer T6 Mode Control (Basic Operating Mode) 000 _B Timer Mode 001 _B Counter Mode 010 _B Gated Timer Mode with gate active low 011 _B Gated Timer Mode with gate active high 100 _B Reserved. Do not use this combination. 101 _B Reserved. Do not use this combination. 110 _B Reserved. Do not use this combination. 111 _B Reserved. Do not use this combination.
T6R	6	rw	Timer T6 Run Bit 0 _B Timer T6 stops 1 _B Timer T6 runs
T6UD	7	rw	Timer T6 Up/Down Control¹⁾ 0 _B Timer T6 counts up 1 _B Timer T6 counts down <i>Note: This bit only controls count direction of T6 if bit T6UDE = 0.</i>

General Purpose Timer Units (GPT12)

Field	Bits	Type	Description
T6UDE	8	rw	Timer T6 External Up/Down Enable¹⁾ 0_B Count direction is controlled by bit T6UD; input T6EUD is disconnected 1_B Count direction is controlled by input T6EUD
T6OE	9	rw	Overflow/Underflow Output Enable 0_B Alternate Output Function Disabled 1_B State of timer T6 toggle latch is output on pin T6OUT
T6OTL	10	rwh	Timer T6 Overflow Toggle Latch Toggles on each overflow/underflow of timer T6. Can be set or reset by software (see separate description)
BPS2	[12:11]	rw	GPT2 Block Prescaler Control Selects the basic clock for block GPT2 (see also Section 16.2.6) 00_B $f_{GPT}/4$ 01_B $f_{GPT}/2$ 10_B $f_{GPT}/16$ 11_B $f_{GPT}/8$
T6CLR	14	rw	Timer T6 Clear Enable Bit 0_B Timer T6 is not cleared on a capture event 1_B Timer T6 is cleared on a capture event
T6SR	15	rw	Timer T6 Reload Mode Enable 0_B Reload from register CAPREL disabled 1_B Reload from register CAPREL enabled

1) See [Table 16-14](#) for encoding of bits T6UD and T6UDE.

GPT2 Auxiliary Timer T5 Control Registers

GPT12E_T5CON

Timer 5 Control Register

SFR (FF46_H/A3_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T5 SC	T5 CLR	CI	-	CT3	T5 RC	T5 UDE	T5 UD	T5R	T5M			T5I			
rw	rw	rw	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
T5I	[2:0]	rw	Timer T5 Input Parameter Selection Depends on the operating mode, see respective sections for encoding: Table 16-15 for Timer Mode and Gated Timer Mode Table 16-17 for Counter Mode
T5M	[5:3]	rw	Timer T5 Mode Control (Basic Operating Mode) 000 _B Timer Mode 001 _B Counter Mode 010 _B Gated Timer Mode with gate active low 011 _B Gated Timer Mode with gate active high 100 _B Reserved. Do not use this combination 101 _B Reserved. Do not use this combination 110 _B Reserved. Do not use this combination 111 _B Reserved. Do not use this combination
T5R	6	rw	Timer T5 Run Bit 0 _B Timer T5 stops 1 _B Timer T5 runs <i>Note: This bit only controls timer T5 if bit T5RC = 0.</i>
T5UD	7	rw	Timer T5 Up/Down Control¹⁾ 0 _B Timer T5 counts up 1 _B Timer T5 counts down <i>Note: This bit only controls count direction of T5 if bit T35DE = 0.</i>
T5UDE	8	rw	Timer T5 External Up/Down Enable¹⁾ 0 _B Count direction is controlled by bit T5UD; input T5EUD is disconnected 1 _B Count direction is controlled by input T5EUD

General Purpose Timer Units (GPT12)

Field	Bits	Type	Description
T5RC	9	rw	Timer T5 Remote Control 0 _B Timer T5 is controlled by its own run bit T5R 1 _B Timer T5 is controlled by the run bit T6R of core timer T6, not by bit T5R
CT3	10	rw	Timer T3 Capture Trigger Enable 0 _B Capture trigger from input line CAPIN 1 _B Capture trigger from T3 input lines T3IN and/or T3EUD
CI	[13:12]	rw	Register CAPREL Capture Trigger Selection²⁾ 00 _B Capture disabled 01 _B Positive transition (rising edge) on CAPIN ³⁾ or any transition on T3IN 10 _B Negative transition (falling edge) on CAPIN or any transition on T3EUD 11 _B Any transition (rising or falling edge) on CAPIN or any transition on T3IN or T3EUD
T5CLR	14	rw	Timer T5 Clear Enable Bit 0 _B Timer T5 is not cleared on a capture event 1 _B Timer T5 is cleared on a capture event
T5SC	15	rw	Timer T5 Capture Mode Enable 0 _B Capture into register CAPREL disabled 1 _B Capture into register CAPREL enabled

1) See [Table 16-14](#) for encoding of bits T5UD and T5UDE.

2) To define the respective trigger source signal, also bit CT3 must be regarded (see [Table 16-10](#)).

3) Rising edge must be selected if capturing is triggered by the internal GPT1 read signals (see register PISEL and [“Combined Capture Modes” on Page 16-58](#)).

Encoding of Timer Count Direction Control

Table 16-14 GPT2 Timer Count Direction Control

Pin TxEUD	Bit TxUDE	Bit TxUD	Count Direction
X	0	0	Count Up
X	0	1	Count Down
0	1	0	Count Up
1	1	0	Count Down
0	1	1	Count Down
1	1	1	Count Up

Timer Mode and Gated Timer Mode: Encoding of Overall Prescaler Factor

**Table 16-15 GPT2 Overall Prescaler Factors for Internal Count Clock
(Timer Mode and Gated Timer Mode)**

Individual Prescaler for Tx	Common Prescaler for Module Clock ¹⁾			
	BPS2 = 01 _B	BPS2 = 00 _B	BPS2 = 11 _B	BPS2 = 10 _B
Txl = 000 _B	2	4	8	16
Txl = 001 _B	4	8	16	32
Txl = 010 _B	8	16	32	64
Txl = 011 _B	16	32	64	128
Txl = 100 _B	32	64	128	256
Txl = 101 _B	64	128	256	512
Txl = 110 _B	128	256	512	1024
Txl = 111 _B	256	512	1024	2048

1) Please note the non-linear encoding of bitfield BPS2.

Counter Mode: Encoding of Input Edge Selection

Table 16-16 GPT2 Core Timer T6 Input Edge Selection(Counter Mode)

T6I	Triggering Edge for Counter Increment/Decrement
000 _B	None. Counter T6 is disabled
001 _B	Positive transition (rising edge) on T6IN
010 _B	Negative transition (falling edge) on T6IN
011 _B	Any transition (rising or falling edge) on T6IN
1XX _B	Reserved. Do not use this combination

Table 16-17 GPT2 Auxiliary Timer T5 Input Edge Selection(Counter Mode)

T5I	Triggering Edge for Counter Increment/Decrement
X00 _B	None. Counter T5 is disabled
001 _B	Positive transition (rising edge) on T5IN
010 _B	Negative transition (falling edge) on T5IN
011 _B	Any transition (rising or falling edge) on T5IN
101 _B	Positive transition (rising edge) of T6 toggle latch T6OTL
110 _B	Negative transition (falling edge) of T6 toggle latch T6OTL
111 _B	Any transition (rising or falling edge) of T6 toggle latch T6OTL

16.2.8.3 GPT2 Timer and CAPREL Interrupt Control Registers

There is an interrupt control register for each of the three timers (T2, T3, T4). All interrupt control registers GPT12E_T5IC, GPT12E_T6IC, and GPT12E_CIC have the same structure described in section Interrupt Control.

General Purpose Timer Units (GPT12)

16.3 Miscellaneous GPT12 Registers

The following registers are not assigned to a specific timer block. They control general functions and/or give general information.

Register GPT12E_PISEL selects timer input signal from several sources under software control.

GPT12E_PISEL

Port Input Select Register

SFR (FE4C_H/26_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ISCAPIN	IST6 EUD	IST6 IN	IST5 EUD	IST5 IN	IST4EUD	IST4IN	IST3EUD	IST3IN	IST2 EUD	IST2 IN					
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Typ	Description
IST2IN	0	rw	Input Select for T2IN 0 _B Signal T2INA is selected 1 _B Signal T2INB is selected
IST2EUD	1	rw	Input Select for T2EUD 0 _B Signal T2EUDA is selected 1 _B Signal T2EUDB is selected
IST3IN	[3:2]	rw	Input Select for T3IN 00 _B Signal T3INA is selected 01 _B Signal T3INB is selected 10 _B Signal T3INC is selected 11 _B Signal T3IND is selected
IST3EUD	[5:4]	rw	Input Select for T3EUD 00 _B Signal T3EUDA is selected 01 _B Signal T3EUDB is selected 10 _B Signal T3EUDC is selected 11 _B Signal T3EUDD is selected
IST4IN	[7:6]	rw	Input Select for T4IN 00 _B Signal T4INA is selected 01 _B Signal T4INB is selected 10 _B Signal T4INC is selected 11 _B Signal T4IND is selected

General Purpose Timer Units (GPT12)

Field	Bits	Typ	Description
IST4EUD	[9:8]	rw	Input Select for T4EUD 00 _B Signal T4EUDA is selected 01 _B Signal T4EADB is selected 10 _B Signal T4EUDC is selected 11 _B Signal T4EUDD is selected
IST5IN	10	rw	Input Select for T5IN 0 _B Signal T5INA is selected 1 _B Signal T5INB is selected
IST5EUD	11	rw	Input Select for T5EUD 0 _B Signal T5EUDA is selected 1 _B Signal T5EADB is selected
IST6IN	12	rw	Input Select for T6IN 0 _B Signal T6INA is selected 1 _B Signal T6INB is selected
IST6EUD	13	rw	Input Select for T6EUD 0 _B Signal T6EUDA is selected 1 _B Signal T6EADB is selected
ISCAPIN	[15:14]	rw	Input Select for CAPIN 00 _B Signal CAPINA is selected 01 _B Signal CAPINB is selected 10 _B Signal CAPINC (Read trigger from T3) is selected 11 _B Signal CAPIND (Read trigger from T2 or T3 or T4) is selected

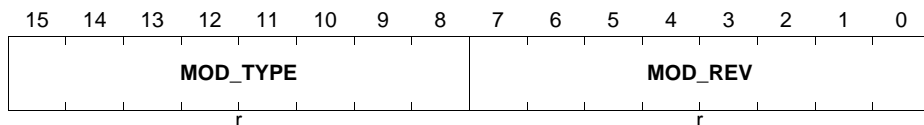
Note: PISEL's reset value represents the connections available in previous versions.

General Purpose Timer Units (GPT12)

Register GPT12E_ID indicates the module version.

GPT12E_ID

Module Identification Register MEM (FFE6_H) Reset Value: 58XXXX_H



Field	Bits	Type	Description
MOD_REV	[7:0]	r	Module Revision Number MOD_REV defines the revision number. The value of a module revision starts with 01 _H (first revision).
MOD_TYPE	[15:8]	r	Module Identification Number This bitfield defines the module identification number (58 _H = GPT12E).

General Purpose Timer Units (GPT12)

Register GPT12E_KSCCFG controls the overall operation of the GPT12 module.

GPT12E_KSCCFG

Kernel State Configuration Register

SFR(FE1C_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BP COM	0	COMCFG	BP SUM	0	SUMCFG	BP NOM	0	NOMCFG	0	BP MOD EN	MOD EN				
w	r	rw	w	r	rw	w	r	rw	r	w	rw				

Field	Bits	Type	Description
MODEN	0	rw	<p>Module Enable</p> <p>This bit enables the module kernel clock and the module functionality.</p> <p>0_B The module is switched off. It does not react on mode control actions and the module clock is switched off immediately (without stop condition). The module does not react on read accesses and ignores write accesses.</p> <p>1_B The module is switched on and can operate. After writing 1 to MODEN, it is recommended to read register KSCCFG to avoid pipeline effects in the control block before accessing other GPT registers.</p> <p><i>Note: This bit is reset by an application reset.</i></p>
BPMODEN	1	w	<p>Bit Protection for MODEN</p> <p>This bit enables the write access to the bit MODEN. It always reads 0. It is only active during the write access cycle.</p> <p>0_B MODEN is not changed.</p> <p>1_B MODEN is updated with the written value.</p> <p><i>Note: This bit is reset by an application reset.</i></p>

General Purpose Timer Units (GPT12)

Field	Bits	Type	Description
NOMCFG	[5:4]	rw	Normal Operation Mode Configuration This bit field defines the kernel mode applied in normal operation mode. 0X _B The module is switched on. 1X _B The module is switched off. This field is taken into account for CR = 00 or 11. <i>Note: This bit is reset by an application reset.</i>
BPNO	7	w	Bit Protection for NOMCFG This bit enables the write access to the bit field NOMCFG. It always reads 0. It is only active during the write access cycle. 0 _B NOMCFG is not changed. 1 _B NOMCFG is updated with the written value. <i>Note: This bit is reset by an application reset.</i>
SUMCFG	[9:8]	rw	Suspend Mode Configuration This bit field defines the kernel mode applied in suspend mode. 0X _B The module is switched on. 1X _B The module is switched off. This field is taken into account for CR = 01. <i>Note: This bit is reset by a debug reset.</i>
BPSUM	11	w	Bit Protection for SUMCFG This bit enables the write access to the bit field SUMCFG. It always reads 0. It is only active during the write access cycle. 0 _B SUMCFG is not changed. 1 _B SUMCFG is updated with the written value. <i>Note: This bit is reset by a debug reset.</i>
COMCFG	[13:12]	rw	Clock Off Mode Configuration This bit field defines the kernel mode applied in clock off mode. 0X _B The module is switched on. 1X _B The module is switched off. This field is taken into account for CR = 10. <i>Note: This bit is reset by an application reset.</i>

General Purpose Timer Units (GPT12)

Field	Bits	Type	Description
BPCOM	15	w	Bit Protection for COMCFG This bit enables the write access to the bit field COMCFG. It always reads 0. It is only active during the write access cycle. 0 _B COMCFG is not changed. 1 _B COMCFG is updated with the written value. <i>Note: This bit is reset by an application reset.</i>
0	[3:2], 6, 10, 14	r	Reserved; returns 0 if read; should be written with 0;

General Purpose Timer Units (GPT12)

16.4 Register Table

Table 16-18 shows all registers which are required for programming of the GPT12E module. It summarizes the GPT12E kernel registers and the module external registers and defines their addresses and reset values.

Table 16-18 GPT12E Module Register Summary

Name	Description	Address		Reset Value
		16-Bit	8-Bit	
General Purpose Timer Unit (GPT12E)				
GPT12E_ID	GPT12E Module ID Register	FFE6 _H	F3 _H	58XXXX _H
GPT12E_PISEL	Input Signal Selection	FE4C _H	26 _H	0000 _H
GPT12E_T2CON	GPT12E Timer T2 Control Register	FF40 _H	A0 _H	0000 _H
GPT12E_T3CON	GPT12E Timer T3 Control Register	FF42 _H	A1 _H	0000 _H
GPT12E_T4CON	GPT12E Timer T4 Control Register	FF44 _H	A2 _H	0000 _H
GPT12E_T5CON	GPT12E Timer T5 Control Register	FF46 _H	A3 _H	0000 _H
GPT12E_T6CON	GPT12E Timer T6 Control Register	FF48 _H	A4 _H	0000 _H
GPT12E_CAPREL	GPT12E Capture/Reload Register	FE4A _H	25 _H	0000 _H
GPT12E_T2	GPT12E Timer T2 Register	FE40 _H	20 _H	0000 _H
GPT12E_T3	GPT12E Timer T3 Register	FE42 _H	21 _H	0000 _H
GPT12E_T4	GPT12E Timer T4 Register	FE44 _H	22 _H	0000 _H
GPT12E_T5	GPT12E Timer T5 Register	FE46 _H	23 _H	0000 _H
GPT12E_T6	GPT12E Timer T6 Register	FE48 _H	24 _H	0000 _H
GPT12E_T2IC	GPT12E Timer T2 Interrupt Control Register	FF60 _H	B0 _H	0000 _H
GPT12E_T3IC	GPT12E Timer T3 Interrupt Control Register	FF62 _H	B1 _H	0000 _H
GPT12E_T4IC	GPT12E Timer T4 imer T6 Interrupt Control Register	FF64 _H	B2 _H	0000 _H
GPT12E_T5IC	GPT12E Timer T5 Interrupt Control Register	FF66 _H	B3 _H	0000 _H
GPT12E_T6IC	GPT12E Timer T6 Interrupt Control Register	FF68 _H	B4 _H	0000 _H
GPT12E_CRIC	GPT12E CAPREL Interrupt Control Register	FF6A _H	B5 _H	0000 _H

16.5 Implementation of the GPT12 Module

This chapter describes the implementation of the GPT12 module in the XC27x8X device.

General Purpose Timer Units (GPT12)

16.5.1 Module Connections

Besides the described intra-module connections, the timer unit blocks GPT1 and GPT2 are connected to their environment in two basic ways:

- **Internal connections** interface the timers with on-chip resources such as clock generation unit, interrupt controller, or other timers.
The GPT module is clocked with the XC27x8X system clock, so $f_{GPT} = f_{SYS}$.
- **External connections** interface the timers with external resources via port pins.

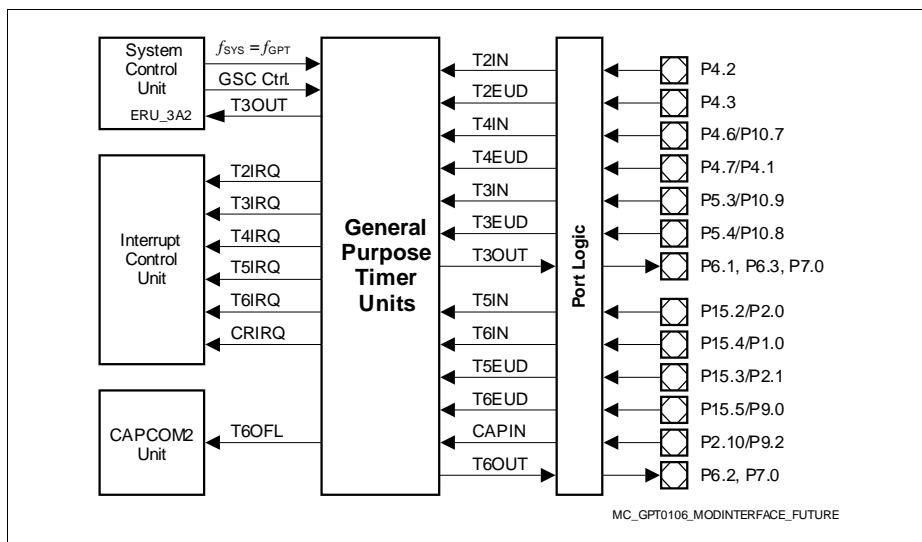


Figure 16-32 GPT Module Interfaces

Note: The GPT12E output signal 'T6OFL' is connected to the CAPCOM2 input 'TOUF' and to the GSC.

The following table shows the digital connections of the GPT12 module with other modules or pins in the XC27x8X device.

Table 16-19 GPT Digital Connections in XC27x8X

Signal	from/to Module	I/O to GPT	Can be used to/as
T2INA	P4.2	I	count input signals for timer T2
T2INB	0	I	
T2EUDA	P4.3	I	direction input signals for timer T2
T2EUSB	0	I	

General Purpose Timer Units (GPT12)

Table 16-19 GPT Digital Connections in XC27x8X (cont'd)

Signal	from/to Module	I/O to GPT	Can be used to/as
T2IRQ	ICU	O	interrupt request from timer T2
T3INA	P5.3	I	count input signals for timer T3
T3INB	P10.9	I	
T3INC	0	I	
T3IND	0	I	
T3EUDA	P5.4	I	direction input signals for timer T3
T3EADB	P10.8	I	
T3EUDC	0	I	
T3EUDD	0	I	
T3OUT	P6.1	O	count output signal for timer T3
	P6.3	O	
	P7.0	O	
	ERU_3A2 (SCU)	O	
T3IRQ	ICU	O	interrupt request from timer T3
T4INA	P4.6	I	count input signals for timer T4
T4INB	P10.7	I	
T4INC	0	I	
T4IND	0	I	
T4EUDA	P4.7	I	direction input signals for timer T4
T4EADB	P4.1	I	
T4EUDC	0	I	
T4EUDD	0	I	
T4IRQ	ICU	O	interrupt request from timer T4
T5INA	P15.2	I	count input signals for timer T5
T5INB	P2.0	I	
T5EUDA	P15.3	I	direction input signals for timer T5
T5EADB	P2.1	I	
T5IRQ	ICU	O	interrupt request from timer T5
T6INA	P15.4	I	count input signals for timer T6
T6INB	P1.0	I	

General Purpose Timer Units (GPT12)

Table 16-19 GPT Digital Connections in XC27x8X (cont'd)

Signal	from/to Module	I/O to GPT	Can be used to/as
T6EUDA	P15.5	I	direction input signals for timer T6
T6EADB	P9.0	I	
T6OUT	P6.2	O	count output signal for timer T6
	P7.0	O	
T6IRQ	ICU	O	interrupt request from timer T6
T6OFL	CC2_TOUF, SCU (GSC)	O	over/under-flow signal from timer T6
CAPINA	P2.10	I	input capture signals
CAPINB	P9.2	I	
CAPINC	Read trigger from T3	I	
CAPIND	Read trigger from T2 or T3 or T4	I	
CRIRQ	ICU	O	interrupt request from capture control

General Purpose Timer Units (GPT12)

Port Control

Port pins to be used for timer input signals must be switched to input (bitfield PC in the respective port control register must be 0xxx_B) and must be selected via register PISEL.

Port pins to be used for timer output signals must be switched to output and the alternate timer output signal must be selected (bitfield PC in the respective port control register must be 1xxx_B).

For the inputs assigned to Ports 5 and 15 (uni-directional input ports), the digital input must be enabled by the digital input control registers (PxDIDIS).

Note: The P5/P15 inputs are directly enabled after reset by the default values of registers P5DIDIS and P15DIDIS.

Note: For a description of the port control registers, please refer to chapter "Parallel Ports".

Interrupts

The GPT12 has six interrupt request lines.

Interrupt nodes to be used for timer interrupt requests must be enabled and programmed to a specific interrupt level.

Debug Details

While the module GPT is disabled, its registers can still be read. While disabled the following registers can be written: PISEL, T5CON.

17 Analog to Digital Converter

The Analog to Digital Converter module (ADC) of the XC27x8X uses the successive approximation method to convert analog input values (voltages) to discrete digital values.

Two kernels (ADC0, ADC1) operate on a user-selectable number of input channels, either separately or in a synchronized way.

The input channels can be selected and arbitrated flexibly.

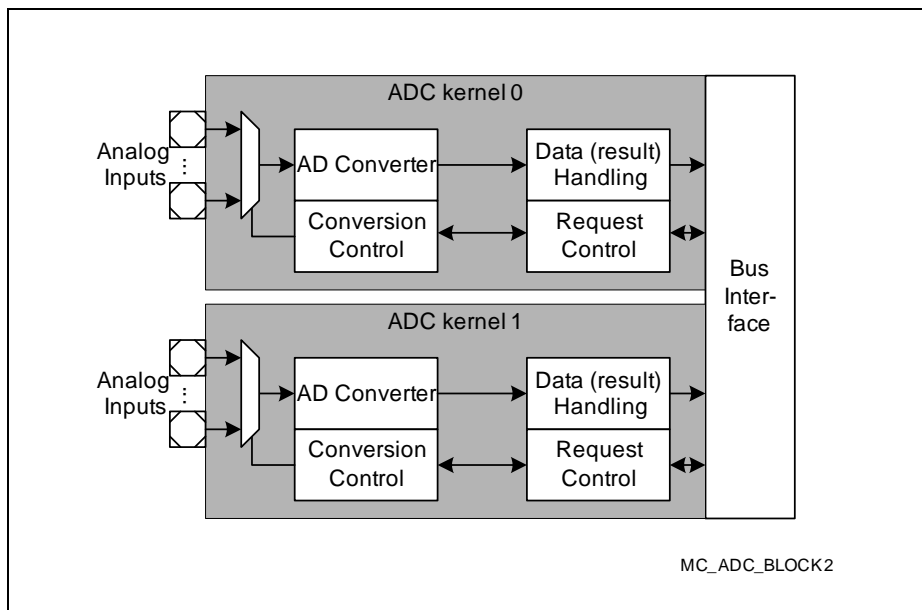


Figure 17-1 ADC Module Block Diagram

You will find the following major sections within this chapter:

- **“Introduction and Basic Structure” on Page 17-4**
- **“Configuration of General Functions” on Page 17-12**
- **“Conversion Request Generation” on Page 17-24**
- **“Request Source Arbitration” on Page 17-47**
- **“Analog Input Channel Configuration” on Page 17-53**
- **“Conversion Result Handling” on Page 17-64**
- **“Synchronization of Conversions” on Page 17-90**
- **“Safety Features” on Page 17-96**
- **“External Multiplexer Control” and “Interrupt Handling” on Page 17-101ff**
- **“Implementation” on Page 17-117** (including a register summary)

The following features describe the functionality of an ADC kernel:

- Input voltage range from 0 V up to analog supply voltage ($V_{DDPA} = 3.0 \text{ V to } 5.5 \text{ V}$)
- Standard (V_{AREF}) and alternate (CH0) reference voltage source selectable for each channel to support ratiometric measurements and different signal scales
- Up to 16 analog input channels
- External analog multiplexer control, including adjusted sample time and scan support
- Conversion speed and sample time adjustable to adapt to sensors and reference
- Conversion time below $1 \mu\text{s}$ (depending on result width and sample time)
- Flexible source selection and arbitration
 - Single-channel conversion (single or repeated)
 - Configurable auto scan conversions (single or repeated)
 - Programmable arbitrary conversion sequence (single or repeated)
 - Conversions triggered by software, timer events, or external events
 - Wait-for-start mode for maximum throughput or
Cancel-inject-restart mode for reduced conversion delay
 - Synchronized conversion starts of both ADC kernels for parallel sampling and conversion of analog inputs, e.g. for phase current measurements in AC drives
- Powerful result handling
 - Selectable result width of 8/10/12
 - 8 independent result registers, can be combined to build result FIFOs
 - Configurable limit checking against programmable border values
 - Data rate reduction through adding a selectable number of conversion results
 - Enhanced filter unit, e.g. for anti-aliasing filtering by a moving average
- Flexible interrupt generation (PEC support) based on selectable events
- Built-in safety features
 - Broken wire detection with programmable default levels
 - Multiplexer test mode to verify signal path integrity
- Support of suspend and power saving modes

Table 17-1 Abbreviations used in ADC chapter

Abbreviation	Meaning
ADC	Analog to Digital Converter
DNL	Differential Non-Linearity (error)
FIFO	First-In-First-Out data buffer mechanism
INL	Integral Non-Linearity (error)
LSB _n	Least Significant Bit: finest granularity of the analog value in digital format, represented by one least significant bit of the conversion result with n bits resolution (measurement range divided in 2 ⁿ equally distributed steps)
PEC	Peripheral Event Controller
SCU	System Control Unit of the device
TUE	Total Unadjusted Error

17.1 Introduction and Basic Structure

A set of functional units can be configured according to the requirements of a given application. These units build a path from the input signals to the digital results.

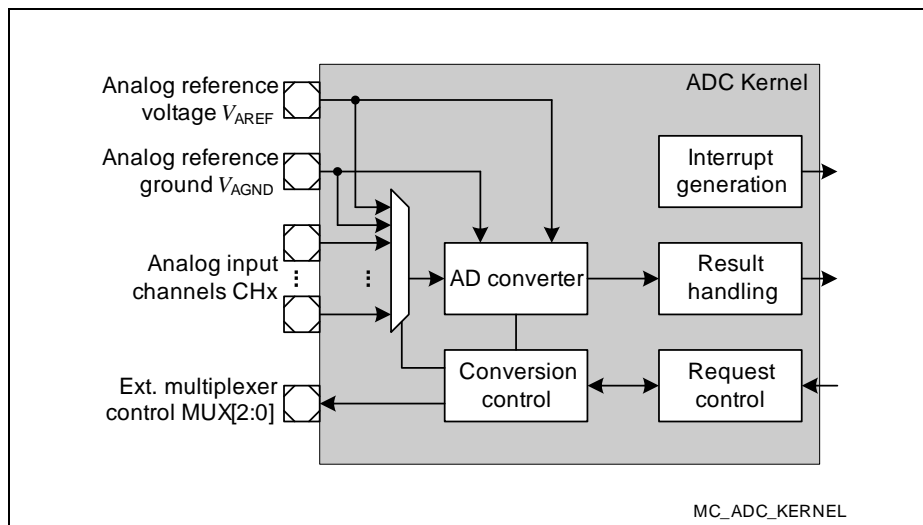


Figure 17-2 ADC Kernel Block Diagram

Conversion Modes and Request Sources

Analog/Digital conversions can be requested by several request sources and can be executed in several conversion modes. The request sources can be enabled concurrently with configurable priorities.

- **Fixed Channel Conversion (single or continuous)**
A specific channel source (request source 0) requests conversions of one selectable channel (once or repeatedly)
- **Auto Scan Conversion (single or continuous)**
A channel scan source (request source 1) requests auto scan conversions of a configurable linear sequence of all available channels (once or repeatedly)
- **Channel Sequence Conversion (single or continuous)**
An arbitrary sequence source (request source 2) requests queued conversions of up to 4 arbitrarily selectable channels (once or repeatedly)

The conversion modes can be used concurrently by the available request sources, i.e. conversions in different modes can be enabled at the same time. Each source can be enabled separately and can be triggered by external events, such as edges of PWM or timer signals, or pin transitions. Read more in [Section 17.5](#)

Request Source Control

Because all request sources can be enabled at the same time, an arbiter resolves concurrent conversion requests from different sources. Each source can be triggered by external signals, by on-chip signals, or by software.

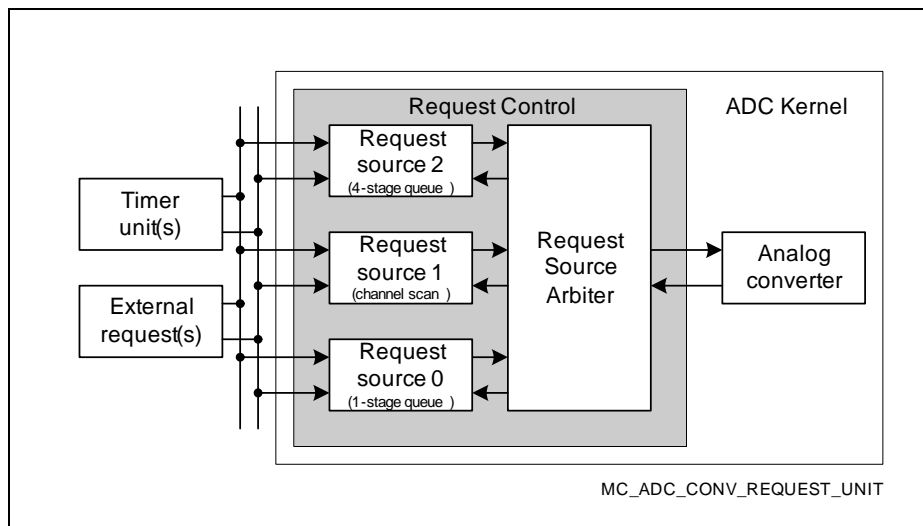


Figure 17-3 Conversion Request Unit

Requests with higher priority can either cancel a running lower-priority conversion (cancel-inject-repeat mode) or be converted immediately after the currently running conversion (wait-for-start mode). If the target result register has not been read, a conversion can be deferred (wait-for-read mode).

Certain channels can also be synchronized with the other ADC kernel, so 2 signals can be converted in parallel.

Input Channel Selection

The analog input multiplexer selects one of the available analog inputs (CH0 - CHx¹⁾) to be converted. Three sources can select a linear sequence, an arbitrary sequence, or a specific channel. The priorities of these sources can be configured.

Additional external analog multiplexers can be controlled automatically, if more separate input channels are required than are built in.

1) The availability of input channels depends on the package of the used product type. A summary can be found in [Section 17.13.3](#).

Analog to Digital Converter

Note: Not all analog input channels are necessarily available in all packages, due to pin limitations. Please refer to the implementation description in [Section 17.13](#).

Conversion Control

Conversion parameters, such as sample phase duration, reference voltage, or result resolution can be configured for 2 input classes. Each channel can be individually assigned to one of these input classes.

The input channels can, thus, be adjusted to the type of sensor (or other analog sources) connected to the ADC.

This unit also controls the built-in multiplexer and external analog multiplexers (via signals EMUX[2:0]) if selected.

Analog/Digital Converter

The selected input channel is converted to a digital value by first sampling the voltage on the selected input and then generating the selected number of result bits.

For 12-bit conversions, post-calibration is executed after converting the channel.

For broken wire detection (see [Section 17.10.1](#)), the converter network can be preloaded before sampling the selected input channel.

Result Handling

The conversion results of each analog input channel can be directed to one of 8 result registers to be stored there. A result register can be used by a group of channels or by a single channel.

The wait-for-read mode avoids data loss due to result overwrite by blocking a conversion until the previous result has been read.

Data reduction (e.g. for digital anti-aliasing filtering) can automatically add up to 4 conversion results before interrupting the CPU.

Also, result registers can be concatenated to build FIFO structures that store a number of conversion results without overwriting previous data. This increases the allowed CPU latency for retrieving conversion data from the ADC.

An enhanced filter structure can combine a selectable series of conversion results. This supports applications with increased requirements (e.g. knock detection).

Interrupt Generation

Several ADC events can issue interrupt requests to the CPU:

- **Source events** indicate the completion of a conversion sequence in the corresponding request source. This event can be used to trigger the setup of a new sequence.

Analog to Digital Converter

- **Channel events** indicate the completion of a conversion for a certain channel. This can be combined with limit checking, so interrupt are generated only if the result is within a defined range of values.
- **Result events** indicate the availability of new result data in the corresponding result register. If data reduction mode is active, events are generated only after a complete accumulation sequence.

Each interrupt request can be assigned to one of four interrupt nodes. This allows grouping the requests according to the requirements of the application.

Safety Features

Safety-aware applications are supported with two mechanisms that help to ensure the integrity of a signal path.

Broken-wire-detection (BWD) preloads the converter network with a selectable level before sampling the input channel. The result will then reflect the preload value if the input signal is no more connected. If buffer capacitors are used, a certain number of conversions may be required to reach the failure indication level.

Multiplexer test mode (MTM) connects an additional pull-down device to an input channel. A subsequent conversion can then confirm the expected modified signal level. This allows to check the proper connection of a signal source (sensor) to the multiplexer.

17.2 Electrical Models

Each conversion of an analog input voltage to a digital value consists of two consecutive phases:

- During the sample phase, the input voltage is sampled and stored.
The input signal path is a simplified model for this.
- During the conversion phase the stored voltage is converted to a digital result.
The reference voltage path is a simplified model for this.

Input Signal Path

The ADC of the XC27x8X uses a switched capacitor field represented by C_{AIN} (small parasitic capacitances are present at each input pin). During the sample phase, the capacitor field C_{AIN} is connected to the selected analog input CHx via the input multiplexer (modeled by ideal switches and series resistors R_{AIN}).

The switch to CHx is closed during the sample phase and connects the capacitor field to the input voltage V_{AINx} .

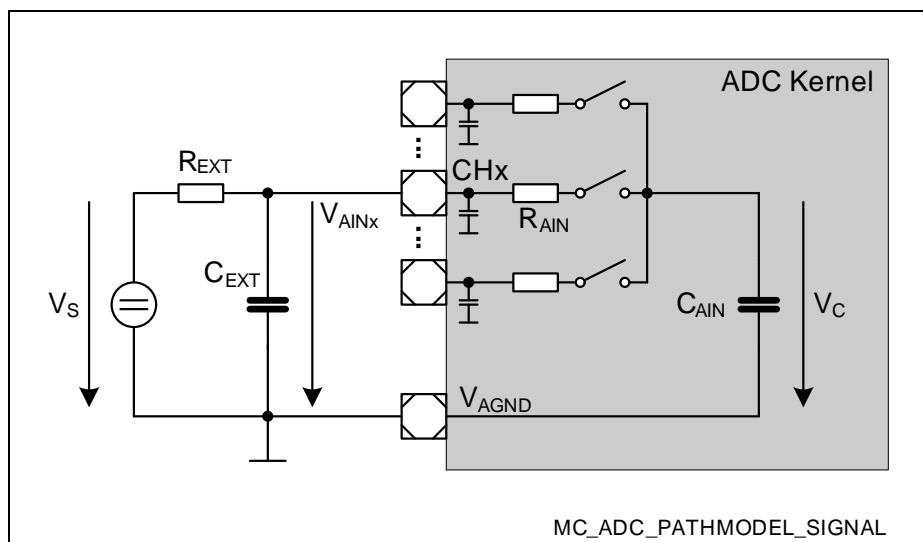


Figure 17-4 Signal Path Model

A simplified model for the analog input signal path is given in [Figure 17-4](#). An analog voltage source (value V_S) with an internal impedance of R_{EXT} delivers the analog input that should be converted.

During the sample phase the corresponding switch is closed and the capacitor field C_{AIN} is charged. Due to the low-pass behavior of the resulting RC combination, the voltage

V_C to be actually converted does not immediately follow V_S . The value R_{EXT} of the analog voltage source and the desired precision of the conversion strongly define the required length of the sample phase.

To reduce the influence of R_{EXT} and to filter input noise, it is recommended to introduce a fast external blocking capacitor C_{EXT} at the analog input pin of the ADC. Like this, mainly C_{EXT} delivers the charge during the sample phase. This structure allows a significantly shorter sample phase than without a blocking capacitor, because the low-pass time constant defining the sample time is mainly given by the values of R_{AIN} and C_{AIN} .

Additionally, the capacitor C_{AIN} is automatically precharged to a voltage of approximately the half of the standard reference voltage V_{AREF} to minimize the average difference between V_{AINx} and V_C at the beginning of a sample phase. Due to varying parameters and parasitic effects, the precharge voltage of C_{AIN} is typically smaller than $V_{AREF} / 2$.

On the other hand, the charge redistribution between C_{EXT} and C_{AIN} leads to a voltage change of V_{AINx} during the sample phase. In order to keep this voltage change lower than 1 LSB_{n1} , it is recommended to use an external blocking capacitor C_{EXT} in the range of at least $2^{n1} \times C_{AIN}$.

The resulting low-pass filter of R_{EXT} and C_{EXT} should be dimensioned in a way to allow V_{AINx} to follow V_S between two sample phases of the same analog input channel.

Please note that, especially at high temperatures, the analog input structure of an ADC can lead to a leakage current and introduces an error due to a voltage drop over R_{EXT} . The ADC input leakage current increases if the input voltage level is close to the analog supply ground V_{SS} or to the analog power supply V_{DDPA} . It is recommended to use an operating range for the input voltage between approximately 3% and 97% of V_{DDPA} to reduce the input leakage current of the respective ADC channel.

Furthermore, the leakage is influenced by an overload condition at adjacent analog inputs. During an overload condition, an input voltage exceeding the supply range is applied at an input and the built-in protection circuit limits the resulting input voltage. This leads to an overload current through the protection circuit that is translated (by a coupling factor) into an additional leakage at adjacent inputs.

Reference Path

During the conversion phase, parts of the capacitor field C_{AIN} are switched to a reference input (V_{AREF} or CH0) or to V_{AGND} . Using CH0 as alternate reference source allows conversions of 5.0 V and 3.3 V based analog input signals with the same ADC kernel. Stable and noise-free reference and analog supply voltages support accurate conversion results. Because noise can also be introduced from other modules (e.g. switching pins), it is strongly recommended to carefully decouple analog from digital signal domains.

The switching of parts of C_{AIN} requires a dynamic current at the selected reference input. The impedance R_{AREF} of the reference voltage source V_R has to be low enough to supply the reference current during the conversion phase. An external blocking capacitor C_{AREF} can supply the peak currents and minimize the current to be delivered by the reference source.

Due to the charge redistribution between C_{AREF} and parts of C_{AIN} , the voltage V_{AREF} decreases during the conversion phase. In order to limit the error introduced by this effect to $1/2 \text{ LSB}_n$, the external blocking capacitor C_{AREF} for the reference input should be at least $2^n \times C_{AIN}$.

The reference current I_{AREF} introduces a voltage drop at R_{AREF} that should not be neglected for the calculation of the overall accuracy. The average reference current during a conversion depends on the reference voltage level and the time t_{CONV} between two conversion starts: $I_{AREF} = C_{AIN} \times V_{AREF} / t_{CONV}$.

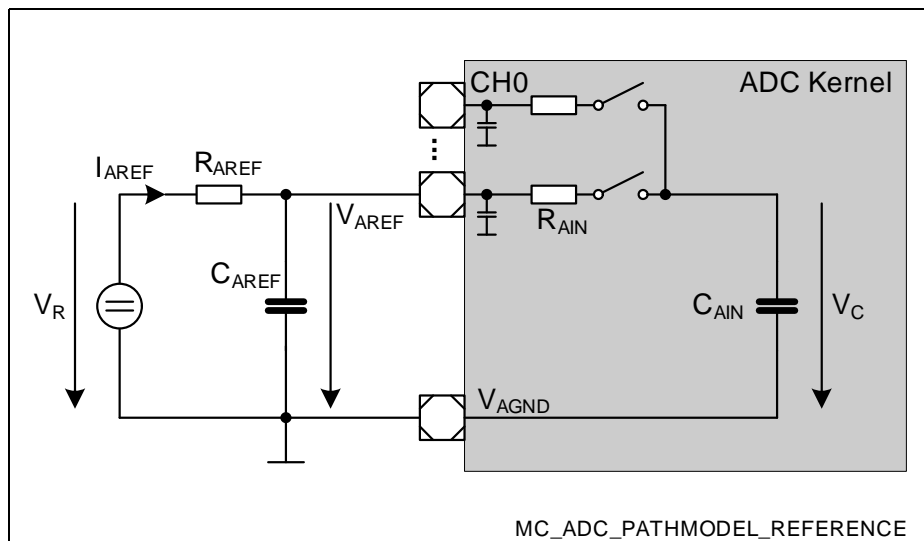


Figure 17-5 Reference Path Model

17.3 Transfer Characteristics and Error Definitions

The transfer characteristic of the ADC describes the association of analog input voltages to the 2^n discrete digital result values (n bits resolution). Each digital result value (in the range of 0 to 2^n-1) represents an input voltage range defined by the reference voltage range divided by 2^n . This range (called quantization step or code width) represents the granularity (called LSB_n) of the ADC. The discrete character of the digital result generates a system-inherent quantization uncertainty of $\pm 0.5 \text{ LSB}_n$ for each conversion result.

The ideal transfer curve has the first digital transition (between 0 and 1) when the analog input reaches 0.5 LSB_n . The quantization steps are equally distributed over the input voltage range.

Analog input voltages below or above the reference voltage limits lead to a saturation of the digital result at 0 or 2^n-1 .

The real transfer curve can exhibit certain deviations from the ideal transfer curve:

- The **offset error** is the deviation of the real transfer line from the ideal transfer line at the lowest code. This refers to best-fit lines through all possible codes, for both cases.
- The **gain error** is the deviation of the slope of the real transfer line from the slope of the ideal transfer line. This refers to best-fit lines through all possible codes, for both cases.
- The **differential non-linearity error** (DNL) is the deviation of the real code width (variation of the analog input voltage between two adjacent digital conversion results) from the ideal code width. A DNL value of -1 LSB_n indicates a missing code.
- The **integral non-linearity error** (INL) is the deviation of the real transfer curve from an adjusted ideal transfer curve (same offset and gain error as the real curve, but equal code widths).
- The **total unadjusted error** (TUE) describes the maximum deviation between a real conversion result and the ideal transfer characteristics over a given measurement range. Since some of these errors noted above can compensate each other, the TUE value generally is much less than the sum of the individual errors.

The TUE also covers production process variations and internal noise effects (if switching noise is generated by the system, this generally leads to an increased TUE value).

17.4 Configuration of General Functions

While many parameters can be selected individually for each channel, source, etc, some adjustments are valid for the whole ADC kernel.

17.4.1 Mode Control

The mode control concept for system control tasks, such as power saving, or suspend request for debugging, allows to program the module behavior under different device operating conditions. The behavior of an ADC kernel can be programmed for each of the device operating modes, that are requested by the global state control part of the SCU. It is advantageous that the ADC kernels of an ADC module show an identical behavior regarding the device operating modes (e.g. to avoid that a non-suspended kernel waits for a suspended kernel to start a synchronized conversion). Register **ADC0_KSCFG** defines the behavior of both kernels of the ADC module in the following device operating modes:

- **Normal operation:**
This operating mode is the default operating mode when neither a suspend request nor a clock-off request are pending. The module clock is not switched off, the ADC registers can be read or written. The kernel behavior is defined by KSCFG.NOMCFG.
- **Suspend mode:**
This operating mode is requested when a suspend request (issued by a debugger) is pending in the device. The module clock is not switched off and the ADC registers can be read or written. The kernel behavior is defined by KSCFG.SUMCFG.
- **Clock-off mode:**
This operating mode is requested for power saving purposes. The module clock is switched off automatically when all kernels of the ADC module reached their specified state in a stop mode. In this case, ADC registers can not be accessed. The kernel behavior is defined by KSCFG.COMCFG.

The following internal ADC actions can be influenced by mode control:

- A current conversion of an analog value:
If the request control unit has found a pending conversion request, the conversion can be started. This start has to be enabled by the mode control. If the current kernel mode allows the conversion start (run modes 0 and 1), it will be executed. If the kernel mode does not allow a start (stop modes 0 and 1), the conversion is not started. The start request is not cancelled, but frozen. A “frozen” conversion is started as programmed if the kernel mode is changed to a run mode again.
- An arbiter round:
The start of a new arbiter round has to be enabled by the kernel modes. In stop mode 1, a new arbiter round will not start.

The behavior of an ADC kernel can be programmed for each of the device operating modes (normal operation, suspend mode, clock-off mode). Therefore, an ADC kernel supports four kernel modes, as shown in **Table 17-2**.

Register KSCFG selects the mode control behavior.

It is common for all ADC kernels and is located in the address range of ADC0.

ADC0_KSCFG

Kernel State Configuration Register

XSFR(0C_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BP COM	0	COMCFG	BP SUM	0	SUMCFG	BP NOM	0	NOMCFG	0	BP MOD EN	MOD EN				
w	r	rw	w	r	rw	w	r	rw	r	w	rw				

Field	Bits	Type	Description
MODEN	0	rw	Module Enable Generally enables the module kernel clock and the module functionality. 0 _B The module clock is switched off immediately (without stop condition). The module does not react to mode control actions or read access and ignores write access (except KSCFG). 1 _B The module is switched on and can operate. To avoid pipeline effects, it is recommended to read register KSCFG after setting MODEN before accessing other ADC registers.
BPMODEN	1	w	Bit Protection for MODEN 0 _B Bit MODEN is not changed. 1 _B MODEN is updated with the written value.
NOMCFG	[5:4]	rw	Kernel Configuration in Normal Operation Mode 00 _B Run mode 0 is selected. 01 _B Run mode 1 is selected. 10 _B Stop mode 0 is selected. 11 _B Stop mode 1 is selected. The coding is described in Table 17-2 .
BP NOM	7	w	Bit Protection for NOMCFG 0 _B Bitfield NOMCFG is not changed. 1 _B NOMCFG is updated with the written value.
SUMCFG	[9:8]	rw	Kernel Configuration in Suspend Mode Same coding as NOMCFG

Field	Bits	Type	Description
BPSUM	11	w	Bit Protection for SUMCFG 0 _B Bitfield SUMCFG is not changed. 1 _B SUMCFG is updated with the written value.
COMCFG	[13:12]	rw	Kernel Configuration in Clock Off Mode Same coding as NOMCFG
BPCOM	15	w	Bit Protection for COMCFG 0 _B Bitfield COMCFG is not changed. 1 _B COMCFG is updated with the written value.
0	[3:2], 6, 10, 14	r	Reserved; returns 0 if read; should be written with 0;

Note: The protection bits BPxxx enable the write access to their associated bitfields when set. Selected bitfields can be modified by a simple write access without requiring a read-modify-write sequence. They are only active during a write access and are read as 0.

Bitfields SUMCFG and BPSUM are reset by a debug reset, all other bitfields are reset by an application reset.

Table 17-2 ADC Kernel Behavior

Kernel Mode	Kernel Behavior	Code
Run mode 0	Kernel operation as specified, no impact on data transfer (same behavior for run mode 0 and run mode 1)	00 _B
Run mode 1		01 _B
Stop mode 0	A currently running AD conversion is completely finished and the result is treated. Pending conversion request to start a new conversion are not taken into account (but not deleted). They start conversions after entering a run mode as programmed. The arbiter continues as programmed.	10 _B
Stop mode 1	Like stop mode 0, but the arbiter is stopped after it has finished its arbitration round. Additionally, bitfield GLOBSTR.ANON is considered being 00 _B when the kernel has reached the defined stop condition (the bitfield itself is not changed).	11 _B

Generally, bitfield KSCFG.NOMCFG should be configured for run mode 0 as default setting for standard operation. If the ADC kernels should not react to a suspend request (and to continue operation as in normal mode), bitfield KSCFG.SUMCFG has to be configured with the same value as KSCFG.NOMCFG. If the ADC kernels should show a different behavior and stop operation when a specific stop condition is reached, the code for stop mode 0 or stop mode 1 has to be written to KSCFG.SUMCFG.

Analog to Digital Converter

A similar mechanism applies for the clock-off mode with the possibility to program the desired behavior by bitfield KSCFG.COMCFG.

Note: The stop mode selection strongly depends on the application needs and it is very unlikely that different stop modes are required in parallel in the same application. As a result, only one stop mode type (either 0 or 1) should be used in the bitfields in register KSCFG. Do not mix stop mode 0 and stop mode 1 and avoid transitions from stop mode 0 to stop mode 1 (or vice versa) for the ADC module.

If the module clock is disabled by KSCFG.MODEN = 0 or in clock-off mode when the stop condition is reached (in stop mode 0 or 1), the module can not be accessed by read or write operations (except register KSCFG that can always be accessed). As a consequence, it cannot be configured.

Please note that bit KSCFG.MODEN should only be set by SW while all configuration fields are configured for run mode 0.

17.4.2 Module Identification

The ID register is a read-only register which is used for ADC module identification purposes. It provides 8 bits for module identification and 8 bits for revision numbering.

ID

Module Identification Register **XSFR(08_H)** **Reset Value: 33XX_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOD_NUMBER								MOD_REV							
r								r							

Field	Bits	Type	Description
MOD_REV	[7:0]	r	Module Revision Number MOD_REV defines the revision number. The value of a module revision starts with 01 _H (first revision).
MOD_NUMBER	[15:8]	r	Module Type Identifies the module itself (33 _H = ADC).

17.4.3 General Clocking Scheme and Control

The different parts of an ADC kernel are driven by clock signals that are based on the clock f_{ADC} of the bus that is used to access the ADC module. The ADC in the XC27x8X device is connected to the system clock, so $f_{ADC} = f_{SYS}$.

- The analog clock f_{ADCI} is used as internal clock for the converter and defines the conversion length and the sample time (selected by bitfield DIVA).
See [Section 17.7.4](#).
- The digital clock f_{ADCD} is used for the arbiter and defines the duration of an arbiter round (selected by bitfield DIVD)
- All other digital structures (such as interrupts, etc.) are directly driven by the module clock f_{ADC} .

Timing parameters are programmed in register [GLOBCTR](#).

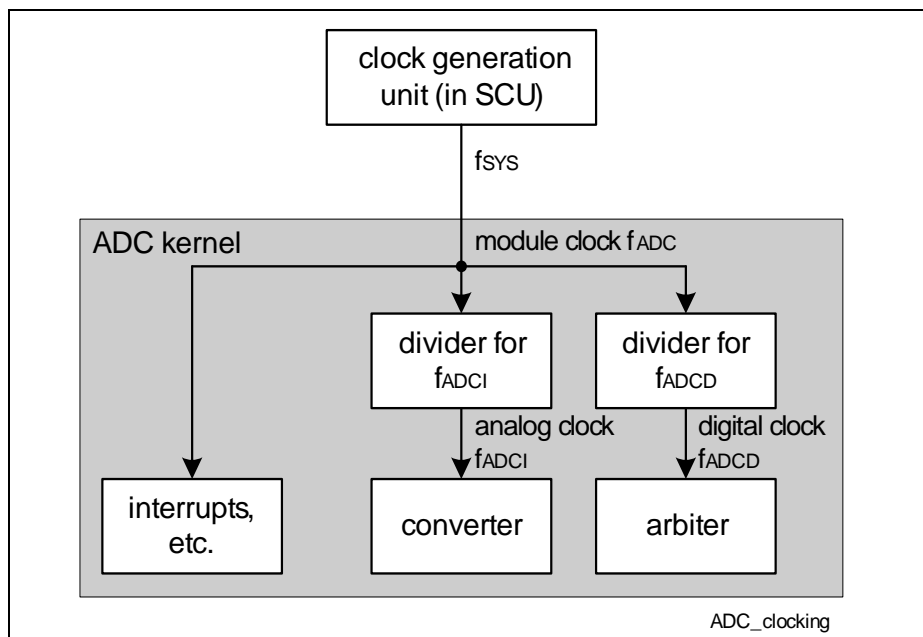


Figure 17-6 Clocking Scheme

Note: If the clock generation for the converter of the ADC falls below a minimum value or is stopped during a running conversion, the conversion result can be corrupted. For correct ADC results, the frequency of f_{ADCI} must not exceed the defined range. Please, refer to the range indicated in the respective Data Sheet.

Analog to Digital Converter

The Global Control Register defines the basic timing parameters and the basic operating mode of the converter unit.

GLOBCTR

Global Control Register

XSFR(10_H)

Reset Value: 00FF_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ARB M		0		ARBRND		ANON		DIVD				DIVA			
rw		rw		rw		rw		rw				rw			

Field	Bits	Type	Description
DIVA	[5:0]	rw	Divider Factor for the Analog Internal Clock Defines the frequency of the basic converter clock f_{ADCI} (base clock for conversion and sample phase). $00_H \quad f_{ADCI} = f_{ADC} / 2$ $01_H \quad f_{ADCI} = f_{ADC} / 2$ $02_H \quad f_{ADCI} = f_{ADC} / 3$... $3F_H \quad f_{ADCI} = f_{ADC} / 64$
DIVD	[7:6]	rw	Divider Factor for Digital Arbiter Clock Defines the frequency of the arbiter clock f_{ADCD} (each arbitration slot lasts one period). $00_B \quad f_{ADCD} = f_{ADC}$ (recommended for min. arb. time) $01_B \quad f_{ADCD} = f_{ADC} / 2$ $10_B \quad f_{ADCD} = f_{ADC} / 3$ $11_B \quad f_{ADCD} = f_{ADC} / 4$
ANON	[9:8]	rw	Analog Part Switched On Defines the converter operating mode for a stand-alone kernel or a master kernel. The actual mode is detected by bitfield GLOBSTR.ANON . The coding is defined in Section 17.4.4 .
ARBRND	[11:10]	rw	Arbitration Round Length Defines the number of arbitration slots per arb. round (arbitration round length = t_{ARB}). ¹⁾ $00_B \quad 4 \text{ arbitration slots per round } (t_{ARB} = 4 / f_{ADCD})$ $01_B \quad 8 \text{ arbitration slots per round } (t_{ARB} = 8 / f_{ADCD})$ $10_B \quad 16 \text{ arbitration slots per round } (t_{ARB} = 16 / f_{ADCD})$ $11_B \quad 20 \text{ arbitration slots per round } (t_{ARB} = 20 / f_{ADCD})$

Field	Bits	Type	Description
0	[14:12]	rw	Reserved for Future Use Reserved for future use, must be written with 000 _B .
ARBM	15	rw	Arbitration Mode <div> <div>0_B</div> <div>The arbiter runs permanently. This setting is required for a synchronization slave (see Section 17.9.1) and for equidistant sampling using the signal ARBCNT (see Section 17.9.2).</div> </div> <div> <div>1_B</div> <div>The arbiter only runs if at least one conversion request of an enabled request source is pending. This setting ensures a reproducible latency from an incoming request to the conversion start, if the converter is idle. Synchronized conversions are not supported.</div> </div>

- 1) The default setting of 4 arbitration slots is sufficient for correct arbitration. The duration of an arbitration round can be increased if required to synchronize requests.

The Global Configuration Register controls the calibration features (start-up calibration and post-calibration) and the general general multiplexer test mode.

GLOBCFG

Global Configuration Register **XSFR(DE_H)** **Reset Value: 0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MTM EN	0				MTMCH			0	DP CAL	SU CAL			0		
rw	r				rw			r	rw	rw			r		

Field	Bits	Type	Description
SUCAL	5	rw	Start-Up Calibration The 0-1 transition of bit SUCAL starts the start-up calibration phase of the analog part (indicated by GLOBSTR.CAL) required for 12-bit conversions. <div> <div>0_B</div> <div>No action</div> </div> <div> <div>1_B</div> <div>Start the start-up calibration phase Start conversions only after the start-up calibration is complete.</div> </div>

Analog to Digital Converter

Field	Bits	Type	Description
DPCAL	6	rw	Disable Post-Calibration Controls the automatic post-calibration required for 12-bit conversions. 0 _B The automatic post-calibration is enabled 1 _B No post-calibration
MTMCH	[12:8]	rw	Multiplexer Test Mode Channel Defines the number of the channel for the multiplexer test mode enabled by bit MTMEN.
MTMEN	15	rw	Multiplexer Test Mode Enable Enables the multiplexer test mode for the channel selected by bitfield MTMCH. 0 _B No test mode (standard conversions) 1 _B Multiplexer test mode enabled (selected channel is connected to ground via a resistor)
0	[4:0], 7, [14:13]	r	Reserved returns 0 if read; should be written with 0;

Analog to Digital Converter

The Global Status Register indicates the current status of a conversion.

GLOBSTR

Global Status Register

XSFR(12_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		CSRC			SYN RUN	ANON		CHNR				CAL	SAM PLE	BU SY	
r		rh			rh	rh		rh				rh	rh	rh	

Field	Bits	Type	Description
BUSY	0	rh	Analog Part Busy Indicates the converter's activity. 0 _B The converter is idle 1 _B A conversion is currently running
SAMPLE	1	rh	Sample Phase Indication 0 _B The converter is idle or converting 1 _B The input signal is being sampled
CAL	2	rh	Calibration Phase 0 _B Start-up calibration is done, conversions can be started 1 _B Start-up calibration is currently running
CHNR	[7:3]	rh	Channel Number Indicates the current or last converted analog input channel. This bitfield is updated when a conversion is started.
ANON	[9:8]	rh	Analog Part Switched On Defines the operating mode of the converter. This bitfield reflects bitfield GLOBCTR .ANON of the synchronization master (see Section 17.9). For a stand-alone ADC kernel (no synchronization) this refers to the local GLOBCTR. The coding is defined in Section 17.4.4 .
SYNRUN	10	rh	Synchronous Conversion Running Indicates that a synchronized (= parallel) conversion is currently running. 0 _B Normal conversion or no conversion running 1 _B A synchronized conversion is running (cannot be cancelled by higher priority requests!)

Field	Bits	Type	Description
CSRC	[13:11]	rh	Currently Converted Request Source Indicates the arbitration slot number of the current (BUSY = 1) or of the last (BUSY = 0) conversion. This bitfield is updated when a conversion is started. 000 _B Current/last conversion for request source 0 001 _B Current/last conversion for request source 1 010 _B Current/last conversion for request source 2 Other combinations are reserved.
0	[15:14]	r	Reserved returns 0 if read; should be written with 0;

17.4.4 Module Activation and Power Saving Modes

The converter of the ADC supports specific power down modes allowing an automatic reduction of the power consumption between two conversions. The actual power mode of a converter depends on the configuration and the current activity of both kernels. The following modes are determined by bitfield **GLOBSTR.ANON**:

- **ANON = 11_B: Normal Operation**
The converter is permanently active, conversions are started immediately.
Requires no wakeup time.
- **ANON = 10_B: Fast Standby mode**
The converter enters a power reduction mode after each conversion. It automatically returns to normal operation if a conversion is requested. Fast standby mode reduces the overall power consumption for the ADC supply.
Requires the standard wakeup time (see below).
- **ANON = 01_B: Slow Standby mode**
The converter enters a power save mode after each conversion if the other kernel is also in slow standby mode or is off. It automatically returns to normal operation if a conversion is requested. Slow standby mode enables the lowest overall power consumption for the ADC supply.
Requires the extended wakeup time (see below).
- **ANON = 00_B: Converter switched Off** (default after reset)
The converter is switched off if the other kernel is also off or in slow standby mode. Furthermore, digital logic blocks are set to their initial state. If the arbiter is currently running, it completes the actual arbitration round and then stops.
To start a conversion, select one of the active modes for ANON.
Requires the extended wakeup time (see below).

The actual wake-up time for a kernel also depends on the current mode of the other kernel. **Table 17-3** summarizes the resulting timing for all combinations of ANON. The minimum power consumption is achieved if at least one kernel can enter slow standby mode (shaded area). If the behaviour of the other kernel is not known, the longer wakeup time must be respected.

Table 17-3 Effective Kernel Power Modes (ADC0 / ADC1)

	ADC1 = 00 _B	ADC1 = 01 _B	ADC1 = 10 _B	ADC1 = 11 _B
ADC0 = 00 _B	Off / Off	Off / Slow	Off / Fast	Off / Normal
ADC0 = 01 _B	Slow / Off	Slow / Slow ¹⁾	Fast / Fast	Fast / Normal
ADC0 = 10 _B	Fast / Off	Fast / Fast	Fast / Fast	Fast / Normal
ADC0 = 11 _B	Normal / Off	Normal / Fast	Normal / Fast	Normal / Normal

1) Slow Standby mode is only entered while the other kernel is currently not active.

Wakeup Time from Analog Powerdown

When the converter is activated, it needs a certain wakeup time to settle before a conversion can be properly executed. This wakeup time must be added to the intended sample time. The required time depends on the operating mode.

In Fast Standby mode the standard wakeup time is approximately 5 μs , in Slow Standby mode the extended wakeup time is approximately 15 μs .

Exact numbers can be found in the respective Data Sheets.

Note: The extended wakeup time is also required after initially enabling the converter.

17.5 Conversion Request Generation

The conversion request unit of the ADC kernel autonomously handles the generation of conversion requests. Three request sources can generate requests for the conversion of an analog channel. The arbiter resolves concurrent requests and selects the channel to be converted next.

Upon a trigger event, the request source requests the conversion of a certain analog input channel or a sequence of channels.

- **Software triggers**
directly activate the respective request source.
- **External triggers**
synchronize the request source activation with external events, such as a trigger pulse from a timer generating a PWM signal or from a port pin.

Application software selects the trigger, the channel(s) to be converted, and the request source priority. A request source can also be activated directly by software without requiring an external trigger.

The arbiter regularly scans the request sources for pending conversion requests and selects the conversion request with the highest priority. This conversion request is then forwarded to the converter to start the conversion of the requested channel.

Each request source can operate in single-shot or in continuous mode:

- **In single-shot mode,**
the programmed conversion (sequence) is requested once after being triggered. A subsequent conversion (sequence) must be triggered again.
- **In continuous mode,**
the programmed conversion (sequence) is automatically requested repeatedly after being triggered once.

For each request source, external triggers are generated from one of 8 selectable trigger inputs (REQTRx[H:A]) and from one of 8 selectable gating inputs (REQGTx[H:A]). The available trigger signals for the XC27x8X are listed in [Section 17.13.4](#).

Note: [Figure 17-3 “Conversion Request Unit” on Page 17-5](#) summarizes the request sources.

Two types of requests sources are available:

- **A channel scan source** can issue conversion requests for a coherent sequence of input channels. This sequence begins with the highest enabled channel number and continues towards lower channel numbers. All available channels¹⁾ can be enabled for the scan sequence. Each channel is converted once per sequence.
A scan source converts a series of input channels permanently or on a regular time

¹⁾ The availability of input channels depends on the package of the used product type. A summary can be found in [Section 17.13.3](#).

Analog to Digital Converter

base. For example, if programmed with low priority, some input channels can be scanned in a background task to update information that is not time-critical.

Request source 1 is a channel scan source.

- **A queued source** can issue conversion requests for an arbitrary sequence of input channels. The channel numbers for this sequence can be freely programmed. This supports application-specific conversion sequences that cannot be covered by a channel scan source. Also, multiple conversions of the same channel within a sequence are supported.

A queued source converts a series of input channels permanently or on a regular time base. For example, if programmed with medium priority, some input channels can be converted upon a specified event (e.g. synchronized to a PWM). Conversions of lower priority sources are suspended in the meantime.

- Request source 2 is a 4-stage queued source.

- Request source 0 is a single source, implemented as a 1-stage queued source.

A single source can issue conversion requests for a single input channel. The channel number can be freely programmed.

A single source converts the selected input channel permanently or on a regular time base. For example, if programmed with high priority, a certain channel can be injected into another sequence controlled either by software or by a hardware-triggered.

17.5.1 Channel Scan Request Source Handling

Each analog input channel can be included in or excluded from the scan sequence (see bits in register [CRCR1](#)). The programmed register value remains unchanged by an ongoing scan sequence. The scan sequence starts with the highest enabled channel number and continues towards lower channel numbers.

Upon a load event, the request pattern is transferred to the pending bits (see register [CRPR1](#)). The pending conversion requests indicate which input channels are to be converted in an ongoing scan sequence. Each conversion start that was triggered by the scan request source, automatically clears the corresponding pending bit. If the last conversion triggered by the scan source is finished and all pending bits are cleared, the current scan sequence is considered finished and a request source event is generated.

A conversion request is only issued to the request source arbiter if at least one pending bit is set.

If the arbiter aborts a conversion triggered by the scan request source due to higher priority requests, the corresponding pending bit is automatically set. This ensures that an aborted conversion is not lost but takes part in the next arbitration round.

The trigger and gating unit generates load events from the selected external (outside the ADC) trigger and gating signals. For example, a timer unit can issue a request signal to synchronize conversions to PWM events.

Load events start a scan sequence and can be generated either via software or via the selected hardware triggers.

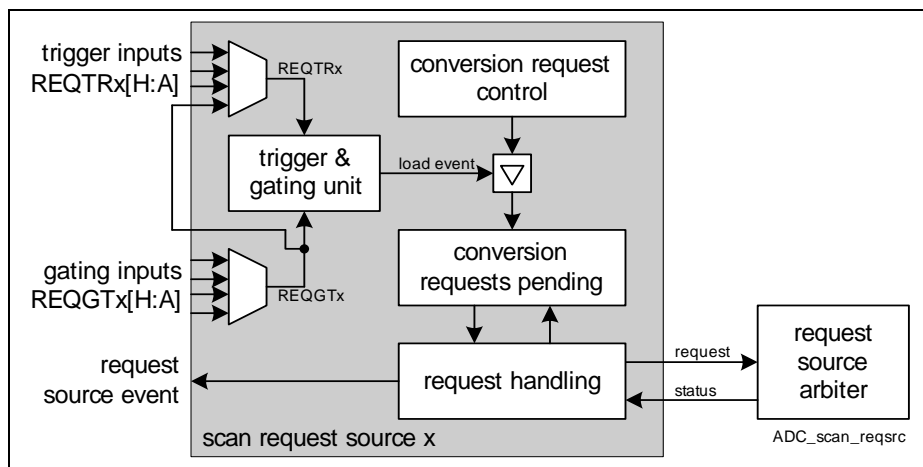


Figure 17-7 Scan Request Source

Scan Source Operation

Configure the scan request source by executing the following actions:

- Select the input channels for the sequence by programming **CRCR1**
- If hardware trigger or gating is desired, select the appropriate trigger¹⁾ and gating inputs and the proper signal transitions by programming **RSIR1**. Enable the trigger and select the gating mode by programming **CRM1**.
- Define the load event operation (handling of pending bits, autoscan mode) by programming **CRM1**.
A load event with bit LDM = 0 copies the content of **CRCR1** to **CRPR1** (overwrite mode). This starts a new scan sequence and aborts any pending conversions from a previous scan sequence.
A load event with bit LDM = 1 OR-combines the content of **CRCR1** to **CRPR1** (combine mode). This starts a scan sequence that includes pending conversions from a previous scan sequence.
- Enable the corresponding arbitration slot (1) to accept conversion requests from the channel scan source (see register **ASENR**).

Start a channel scan sequence by generating a load event:

- If a hardware trigger is selected and enabled, generate the configured transition at the selected input signal, e.g. from a timer or an input pin.
- Generate a software load event by setting **CRM1.LDEV** = 1.
- Generate a load event by writing the scan pattern directly to the pending bits in **CRPR1**. The pattern is copied to **CRCR1** and a load event is generated automatically.
In this case, a scan sequence can be defined and started with a single data write action, e.g. under PEC control.

Note: If autoscan is enabled, a load event is generated automatically each time a request source event occurs when the scan sequence has finished. This permanently repeats the defined scan sequence (autoscan).

Stop or abort an ongoing scan sequence by executing the following actions:

- If external gating is enabled, switch the gating signal to the defined inactive level. This does not modify the conversion pending bits, but only prevents issuing conversion requests to the arbiter.
- Disable the corresponding arbitration slot (1) in the arbiter. This does not modify the contents of the conversion pending bits, but only prevents the arbiter from accepting requests from the request handling block.
- Disable the channel scan source by clearing bitfield **ENGT** = 00_B. Clear the pending request bits by setting bit **CRM1.CLRPND** = 1.

1) Please refer to "**Hardware Trigger Selection**" on Page 17-45.

Scan Request Source Events and Interrupts

A request source event of a scan source occurs if the last conversion of a scan sequence is finished (all pending bits = 0). A request source event interrupt can be generated based on a request source event according to the structure shown in [Figure 17-8](#). If a request source event is detected, it sets the corresponding indication flag in register **EVINFR**. These flags can also be set by writing a 1 to the corresponding bit position, whereas writing 0 has no effect. Additionally, a gated event flag **EVINCR.EVINGFx** indicates that a request source interrupt has been activated. The indication flags can be cleared by SW by writing a 1 to the corresponding bit position in register **EVINCR**.¹⁾

The service request output SRx that is selected by the request source event interrupt node pointer bitfields in register **EVINPRO** becomes activated each time the related request source event is detected (and enabled by **CRMRx.ENS**) or the related bit position in register **EVINFR** is written with a 1 (this write action simulates a request source event).

Additionally, a gated event indication flag **EVINCR.EVINGFx** (after the gating with the enable bit) becomes set if a service request output becomes activated due to a request source event.

The request source events and the result events share the same registers. The request source event is located at the bit position in register **EVINFR**:

- Event 1: Request source event of the channel scan source 1 (in arbitration slot 1)

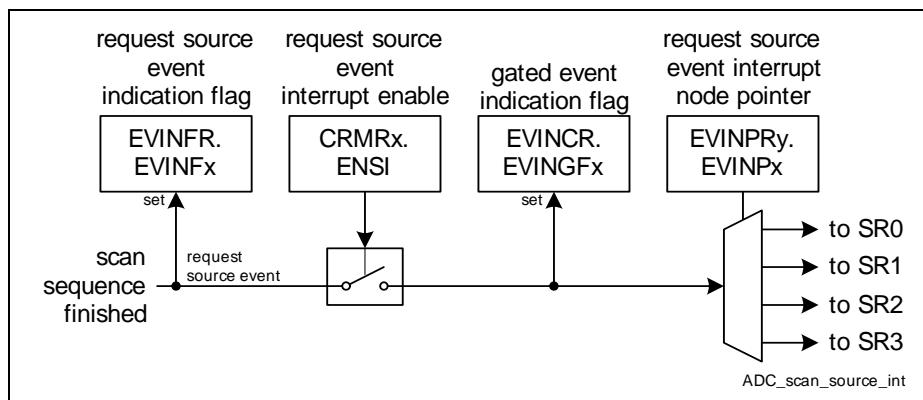


Figure 17-8 Interrupt Generation of a Scan Request Source

1) Please refer to ["Interrupt Request Handling"](#) on [Page 17-106](#).

Analog to Digital Converter

The Conversion Request Mode Register configures the operating mode of the channel scan request source.

CRMR1

Conversion Request 1 Mode Register

XSFR(EC_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0						LD EV	CLR PND	REQ GT	0	LD M	SC AN	EN SI	EN TR	ENGT	
r						w	w	rh	r	rw	rw	rw	rw	rw	

Field	Bits	Type	Description
ENGT	[1:0]	rw	Enable Gate Selects the gating functionality for source 1. 00 _B No conversion requests are issued 01 _B Conversion requests are issued if at least one pending bit is set 10 _B Conversion requests are issued if at least one pending bit is set and REQGTx = 1. 11 _B Conversion requests are issued if at least one pending bit is set and REQGTx = 0. <i>Note: REQGTx is the selected gating signal.</i>
ENTR	2	rw	Enable External Trigger 0 _B External trigger disabled 1 _B The selected edge at the selected trigger input signal REQTR generates the load event
ENSI	3	rw	Enable Source Interrupt 0 _B No request source interrupt 1 _B A request source interrupt is generated upon a request source event (last pending conversion is finished)
SCAN	4	rw	Autoscan Enable 0 _B No autoscan 1 _B Autoscan functionality enabled: a request source event automatically generates a load event

Field	Bits	Type	Description
LDM	5	rw	Load Event Mode Defines the transfer mechanism upon a load event. 0 _B Overwrite mode: Upon a load event, the bits of CRCR1 are copied to CRPR1 1 _B Combine mode: Upon a load event, the bits of CRCR1 are logical OR combined to the bits of CRPR1
REQGT	7	rh	Request Gate Level Monitors the level at the selected REQGT input. 0 _B The gate input is low 1 _B The gate input is high
CLRPND	8	w	Clear Pending Bits 0 _B No action 1 _B The bits in register CRPR1 are cleared
LDEV	9	w	Generate Load Event 0 _B No action 1 _B A load event is generated
0	6, [15:10]	r	Reserved returns 0 if read; should be written with 0;

Analog to Digital Converter

The Conversion Request 1 Control Register selects the channels to be converted by request source 1 (channel scan source). Its bits are used to update the pending register CRPR1, when the load event occurs.

Note: Writes to register CRPR1 also update CRCR1 and generate a load event.

CRCR1

Conversion Request 1 Control Register

XSFR(E8_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH 15	CH 14	CH 13	CH 12	CH 11	CH 10	CH 9	CH 8	CH 7	CH 6	CH 5	CH 4	CH 3	CH 2	CH 1	CH 0
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
CHx (x = 0 - 15)	x	rwh	Channel x Request Bit Each bit corresponds to one analog input channel, the channel number CHx is defined by the bit position x in this register. 0 _B No request 1 _B Analog channel CHx will be requested for conversion by this channel scan source

Note: Not all channels are available in all products.

Therefore, only the conversion request bits with corresponding channels are valid.

Analog to Digital Converter

The Conversion Request Pending Register indicates which channels of request source 1 (channel scan source) are requesting a conversion. Its bits are updated from pending register CCR1, when the load event occurs.

Note: Writes to register CRPR1 also update CCR1 and generate a load event.

CRPR1

Conversion Request 1 Pending Register

XSFR(EA_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHP 15	CHP 14	CHP 13	CHP 12	CHP 11	CHP 10	CHP 9	CHP 8	CHP 7	CHP 6	CHP 5	CHP 4	CHP 3	CHP 2	CHP 1	CHP 0
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
CHPx (x = 0 - 15)	x	rwh	Channel Pending Bit x <u>Write view:</u> A write to this address targets the bits in register CCR1. <u>Read view:</u> Each bit corresponds to one analog channel, the channel number CHx is defined by the bit position in the register. 0 _B No request 1 _B Analog channel CHx is requested for conversion by this channel scan source

Note: Not all channels are available in all products.

Therefore, only the request pending bits with corresponding channels are valid.

17.5.2 Queued Request Source Handling

A queued request source supports short conversion sequences of arbitrary channels (contrary to a scan request source with a fixed conversion order for the enabled channels). The programmed sequence is stored in a queue buffer (based on a FIFO mechanism). The requested channel numbers are entered via the queue input, while queue stage 0 defines the channel to be converted next.

A conversion request is only issued to the request source arbiter if a valid entry is stored in queue stage 0.

If the arbiter aborts a conversion triggered by a queued request source due to higher priority requests, the corresponding conversion parameters are automatically saved in the backup stage. This ensures that an aborted conversion is not lost but takes part in the next arbitration round (before stage 0).

The trigger and gating unit generates trigger events from the selected external (outside the ADC) trigger and gating signals. For example, a timer unit can issue a request signal to synchronize conversions to PWM events.

Trigger events start a queued sequence and can be generated either via software or via the selected hardware triggers. The occurrence of a trigger event is indicated by bit QSRx.EV. This flag is cleared when the corresponding conversion is started or by writing to bit QMRx.CEV.

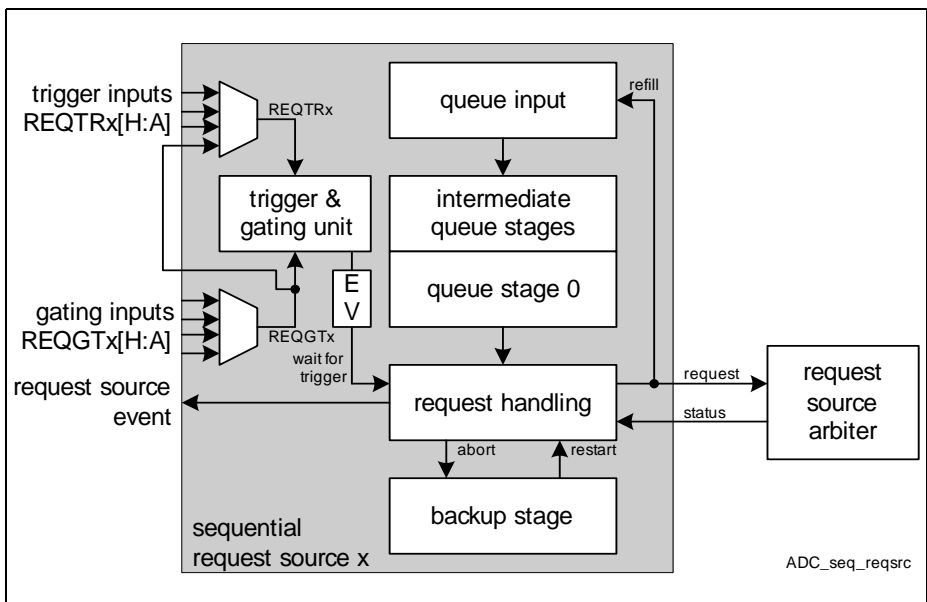


Figure 17-9 Queued Request Source

Analog to Digital Converter

A sequence is defined by entering conversion requests into the queue input register (**QINR0**, **QINR2**). Each entry selects the channel to be converted and can enable an external trigger, generation of an interrupt, and an automatic refill (i.e. keep this entry in the queue after conversion). The entries are stored in the queue buffer stages.

The content of stage 0 (**Q0R0**, **Q0R2**) selects the channel to be converted next. When the requested conversion is started, the contents of this queue stage is invalidated and copied to the backup stage. Then the next queue entry can be handled (if available).

Note: The contents of the queue stages cannot be modified directly, but only by writing to the queue input or by flushing the queue.

If all queue entries have automatic refill selected, the defined conversion sequence can be repeated without re-programming.

Properties of the 2 Queued Request Sources

The ADC of the XC27x8X provides two queued request sources with different buffer size:

- Queued request source 2 provides 4 buffer stages and can handle sequences of up to 4 input channel entries. It supports short application-specific conversion sequences, especially for timing-critical sequences containing also multiple conversions of the same channel.
- Queued request source 0 provides a single-stage buffer and can handle a single input channel entry. It supports software-controlled conversion requests or hardware-triggered conversions of a single input channel (to “inject” a single conversion into a running sequence).

Queued Source Operation

Configure the queued request source by executing the following actions:

- Define the sequence by writing the entries to the queue input **QINR0** or **QINR2**. Initialize the complete sequence before enabling the request source, because with enabled refill feature, software writes to QINRx are not allowed.
- If hardware trigger or gating is desired, select the appropriate trigger¹⁾ and gating inputs and the proper transitions by programming **RSIR0** or **RSIR2**. Enable the trigger and select the gating mode by programming bitfield ENGT in register **QMR0** or **QMR2**.
- Enable the corresponding arbitration slot (0 or 2) to accept conversion requests from the queued source (see register **ASENR**).

Start a queued sequence by generating a trigger event:

- If a hardware trigger is selected and enabled, generate the configured transition at the selected input signal, e.g. from a timer or an input pin.
- Generate a software trigger event by setting QMRx.TREV = 1.
- Write a new entry to the queue input of an empty queue. This leads to a (new) valid queue entry that is forwarded to queue stage 0 and starts a conversion request (if enabled by QMRx.ENG and without waiting for an external trigger).

Note: If the refill mechanism is activated, a processed entry is automatically reloaded into the queue. This permanently repeats the respective sequence (autoscan). In this case, do not write to the queue input while the queued source is running. Write operations to a completely filled queue are ignored.

Stop or abort an ongoing queued sequence by executing the following actions:

- If external gating is enabled, switch the gating signal to the defined inactive level. This does not modify the queue entries, but only prevents issuing conversion requests to the arbiter.
- Disable the corresponding arbitration slot (0 or 2) in the arbiter. This does not modify the queue entries, but only prevents the arbiter from accepting requests from the request handling block.
- Disable the queued source by clearing bitfield ENGT = 00_B.
 - Invalidate the next pending queue entry by setting bit QMRx.CLRV = 1. If the backup stage contains a valid entry, this one is invalidated, otherwise stage 0 is invalidated.
 - Remove all entries from the queue by setting bit QMRx.FLUSH = 1.

1) Please refer to **"Hardware Trigger Selection"** on Page 17-45.

Queue Request Source Events and Interrupts

A request source event of a queued source occurs when a conversion is finished. A request source event interrupt can be generated based on a request source event according to the structure shown in [Figure 17-10](#). If a request source event is detected, it sets the corresponding indication flag in register [EVINFR](#). These flags can also be set by writing a 1 to the corresponding bit position, whereas writing 0 has no effect. The indication flags can be cleared by SW by writing a 1 to the corresponding bit position in register [EVINCR](#).¹⁾

The interrupt enable bit is taken from stage 0 for a normal sequential conversion, or from the backup stage for a repeated conversion after an abort.

The service request output line SRx that is selected by the request source event interrupt node pointer bitfields in register [EVINPRO](#) becomes activated each time the related request source event is detected (and enabled by Q0Rx.ENS1, or QBURx.ENS1 respectively) or the related bit position in register [EVINFR](#) is written with a 1 (this write action simulates a request source event).

Additionally, a gated event indication flag [EVINCR.EVINGFx](#) (after the gating with the enable bit) becomes set if a service request output becomes activated due to a request source event.

The request source events and the result events share the same registers. The request source event is located at the bit position in register [EVINFR](#):

- Event 0: Request source event of queued source 0 (in arbitration slot 0)
- Event 2: Request source event of queued source 2 (in arbitration slot 2)

1) Please refer to [“Interrupt Request Handling” on Page 17-106](#).

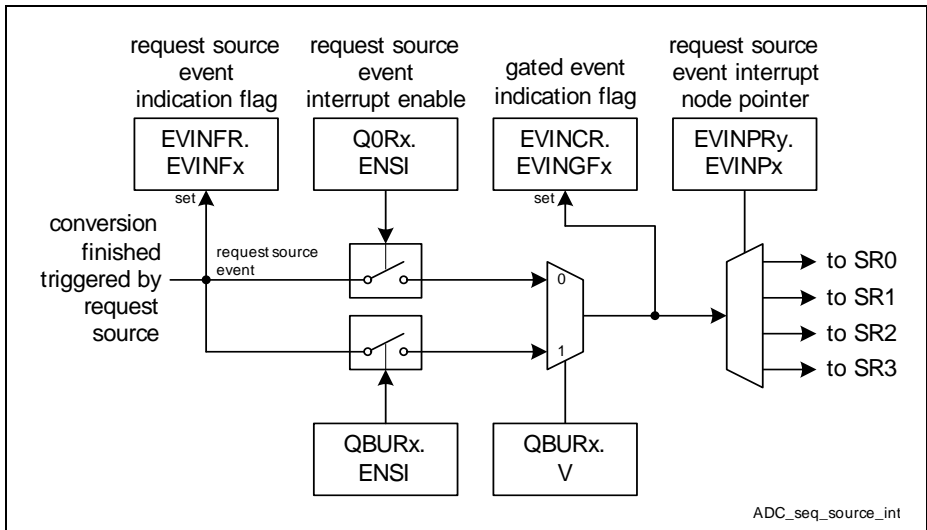


Figure 17-10 Interrupt Generation of a Queued Request Source

Analog to Digital Converter

The Queue Mode Register configures the operating mode of a queued request source.

QMR0

Queue 0 Mode Register

XSFR(E0_H)

Reset Value: 0000_H

QMR2

Queue 2 Mode Register

XSFR(F0_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				CEV	FLU SH	TR EV	CLR V	0				EN TR	ENGT		
r				w	w	w	w	r				rw	rw		

Field	Bits	Type	Description
ENGT	[1:0]	rw	Enable Gate Selects the gating functionality for source 0/2. 00 _B No conversion requests are issued 01 _B Conversion requests are issued if a valid conversion request is pending in the queue 0 register or in the backup register 10 _B Conversion requests are issued if a valid conversion request is pending in the queue 0 register or in the backup register and REQGTx = 1 11 _B Conversion requests are issued if a valid conversion request is pending in the queue 0 register or in the backup register and REQGTx = 0 <i>Note: REQGTx is the selected gating signal.</i>
ENTR	2	rw	Enable External Trigger 0 _B External trigger disabled 1 _B The selected edge at the selected trigger input signal REQTR generates the trigger event
CLRV	8	w	Clear Valid Bit 0 _B No action 1 _B The next pending valid queue entry in the sequence and the event flag EV are cleared. If there is a valid entry in the queue backup register (QBUR.V = 1), this entry is cleared, otherwise the entry in queue register 0 is cleared.

Analog to Digital Converter

Field	Bits	Type	Description
TREV	9	w	Trigger Event 0 _B No action 1 _B Generate a trigger event by software
FLUSH	10	w	Flush Queue 0 _B No action 1 _B Clear all queue entries (including backup stage) and the event flag EV. The queue contains no more valid entry.
CEV	11	w	Clear Event Flag 0 _B No action 1 _B Clear bit EV
0	[7:3], [15:12]	r	Reserved returns 0 if read; should be written with 0;

*Note: Before SW modifies the queue content by QMR.CLRV or QMR.FLUSH, all HW actions related to this queue have to be finished. Therefore, the arbitration slot has to be disabled and SW has to wait for at least two arbitration rounds (to be sure that this request source can no longer be an arbitration winner). Then, it has to check **GLOBSTR.CRSC** and **GLOBSTR.BUSY** to be sure that a conversion triggered by this request source is no longer running. Then SW can read QBURx and Q0Rx and can start modification of the queue content.*

Analog to Digital Converter

The Queue Status Register indicates the current status of the queued source. The filling level and the empty information refer to the queue intermediate stages (if available) and to the queue register 0. An aborted conversion stored in the backup stage is not indicated by these bits (therefore, see QBURx.V).

QSR0

Queue 0 Status Register

XSFR(E2_H)

Reset Value: 0020_H

QSR2

Queue 2 Status Register

XSFR(F2_H)

Reset Value: 0020_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0						EV	REQ GT	0	EMP TY	0			FILL		
r						rh	rh	r	rh	r			rh		

Field	Bits	Type	Description
FILL	[1:0]	rh	Filling Level for Queue 2 Indicates the number of valid queue entries. It is incremented each time a new entry is written to QINRx or by an enabled refill mechanism. It is decremented each time a requested conversion has been started. A new entry is ignored if the filling level has reached its maximum value. 00 _B There is 1 (if EMPTY = 0) or no (if EMPTY = 1) valid entry in the queue 01 _B There are 2 valid entries in the queue 10 _B There are 3 valid entries in the queue 11 _B There are 4 valid entries in the queue <i>Note: In QSR0 (queued source 0), this bitfield is 00_B.</i>
EMPTY	5	rh	Queue Empty 0 _B There are valid entries in the queue (see FILL) 1 _B No valid entries (queue is empty)
REQGT	7	rh	Request Gate Level Monitors the level at the selected REQGT input. 0 _B The gate input is low 1 _B The gate input is high

Field	Bits	Type	Description
EV	8	rh	Event Detected Indicates that an event has been detected while at least one valid entry has been in the queue (queue register 0 or backup stage). Once set, this bit is cleared automatically when the requested conversion is started. 0 _B No trigger event 1 _B A trigger event has been detected
0	[4:2], 6, [15:9]	r	Reserved returns 0 if read; should be written with 0;

Analog to Digital Converter

The Queue Input Register is the entry point for conversion requests of a queued request source.

QINR0

Queue 0 Input Register

XSFR(E6_H)

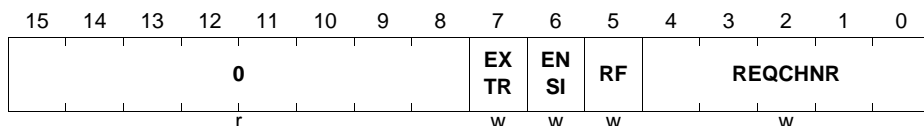
Reset Value: 0000_H

QINR2

Queue 2 Input Register

XSFR(F6_H)

Reset Value: 0000_H



Field	Bits	Type	Description
REQCHNR	[4:0]	w	Request Channel Number Defines the channel number to be converted
RF	5	w	Refill 0 _B No refill: this queue entry is converted once and then invalidated 1 _B Automatic refill: this queue entry is automatically reloaded into QINRx when the related conversion is started
ENSI	6	w	Enable Source Interrupt 0 _B No request source interrupt 1 _B A request source event interrupt is generated upon a request source event (related conversion is finished)
EXTR	7	w	External Trigger Enables the external trigger functionality. 0 _B A valid queue entry immediately leads to a conversion request. 1 _B A valid queue entry waits for a trigger event to occur before issuing a conversion request.
0	[15:8]	r	Reserved returns 0 if read; should be written with 0;

Note: Registers QINRx share addresses with registers QBURx.

Write operations target the control bits in register QINRx. Read operations return the status bits from register QBURx.

Analog to Digital Converter

The queue registers 0 monitor the status of the pending request (queue stage 0).

Q0R0

Queue 0 Register 0

XSFR(E4_H)

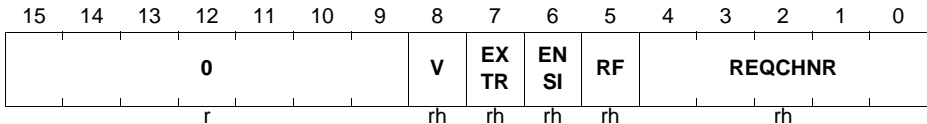
Reset Value: 0000_H

Q0R2

Queue 2 Register 0

XSFR(F4_H)

Reset Value: 0000_H



Field	Bits	Type	Description
REQCHNR	[4:0]	rh	Request Channel Number Stores the channel number to be converted.
RF	5	rh	Refill Selects the handling of handled requests. <div> <div>0_B</div> <div>The request is discarded after the conversion start.</div> </div> <div> <div>1_B</div> <div>The request is automatically refilled into the queue after the conversion start.</div> </div>
ENSI	6	rh	Enable Source Interrupt <div> <div>0_B</div> <div>No request source interrupt</div> </div> <div> <div>1_B</div> <div>A request source event interrupt is generated upon a request source event (related conversion is finished)</div> </div>
EXTR	7	rh	External Trigger Enables external trigger events. <div> <div>0_B</div> <div>A valid queue entry immediately leads to a conversion request</div> </div> <div> <div>1_B</div> <div>The request handler waits for a trigger event</div> </div>
V	8	rh	Request Channel Number Valid Indicates a valid queue entry in queue register 0. <div> <div>0_B</div> <div>No valid queue entry</div> </div> <div> <div>1_B</div> <div>The queue entry is valid and leads to a conversion request</div> </div>
0	[15:9]	r	Reserved returns 0 if read; should be written with 0;

Analog to Digital Converter

The Queue Backup Registers monitor the status of an aborted queued request.

QBUR0

Queue 0 Backup Register

XSFR(E6_H)

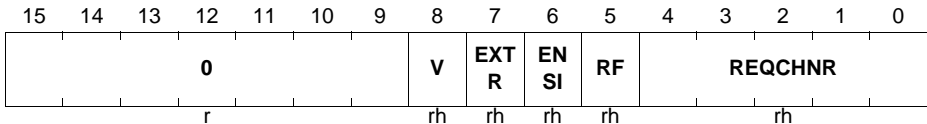
Reset Value: 0000_H

QBUR2

Queue 2 Backup Register

XSFR(F6_H)

Reset Value: 0000_H



Field	Bits	Type	Description
REQCHNR	[4:0]	rh	Request Channel Number The channel number of the aborted conversion that has been requested by this request source
RF	5	rh	Refill The refill control bit of the aborted conversion
ENSI	6	rh	Enable Source Interrupt The enable source interrupt control bit of the aborted conversion
EXTR	7	rh	External Trigger The external trigger control bit of the aborted conversion
V	8	rh	Request Channel Number Valid Indicates if the entry (REQCHNR, RF, TR, ENSI) in the queue backup register is valid. Bit V is set when a running conversion (that has been requested by this request source) is aborted, it is cleared when the aborted conversion is restarted. 0 _B Backup register not valid 1 _B Backup register contains a valid entry. This will be requested before a valid entry in queue register 0 (stage 0) will be requested.
0	[15:9]	r	Reserved returns 0 if read; should be written with 0;

Note: Registers QBURx share addresses with registers QINRx.

Read operations return the status bits from register QBURx. Write operations target the control bits in register QINRx.

17.5.3 Hardware Trigger Selection

Each request source can be activated either by software or by a hardware trigger signal. The hardware triggers can be derived from several module signals or port inputs. Selectable gating signals additionally enable/disable these triggers.

Registers RSIRx select the inputs for the hardware trigger and gating inputs for each request source. For a list of the available input signals, please refer to the implementation chapter, [Section 17.13.4](#).

RSIR0

Request Source 0 Input Register XSFR(00_H) **Reset Value: 0000_H**

RSIR1

Request Source 1 Input Register XSFR(02_H) **Reset Value: 0000_H**

RSIR2

Request Source 2 Input Register XSFR(04_H) **Reset Value: 0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRI	0	R EN	F EN	0	TRSEL		GTI	0	TM EN	0	GTSEL				
rh	r	rw	rw	r	rw		rh	r	rw	r	rw				

Field	Bits	Type	Description
GTSEL	[2:0]	rw	Gating Input Selection for Source x Selects the input signal used for request gating in request source x. 000 _B Select input signal REQGTxA 001 _B Select input signal REQGTxB ... 111 _B Select input signal REQGTxH
TMEN	4	rw	Timer Mode Enable of Source x Enables the timer mode for equidistant sampling (see Section 17.9.2). 0 _B The timer mode is disabled. The standard gating mechanism can be used. 1 _B The timer mode for equidistant sampling is enabled. The standard gating mechanism has to be enabled permanently (no influence of gating signal).

Field	Bits	Type	Description
GTI	7	rh	Request Gate Level of Source x Monitors the level at the selected REQGTx input. 0 _B The gate input is low 1 _B The gate input is high
TRSEL	[10:8]	rw	Trigger Input Selection for Source x Selects the input signal used for request triggering in request source x. 000 _B Select input signal REQTRxA 001 _B Select input signal REQTRxB ... 111 _B Select input signal REQTRxH
FEN	12	rw	Falling Edge Enable for Trigger of Source x 0 _B No trigger upon a falling edge 1 _B A falling edge on the selected REQTRx input generates a trigger event
REN	13	rw	Rising Edge Enable for Trigger of Source x 0 _B No trigger upon a rising edge 1 _B A rising edge on the selected REQTRx input generates a trigger event
TRI	15	rh	Trigger Input Level of Source x Monitors the level at the selected REQTRx input. 0 _B The trigger input is low 1 _B The trigger input is high
0	3, [6:5], 11, 14	r	Reserved returns 0 if read; should be written with 0.

17.6 Request Source Arbitration

The request source arbiter regularly polls the request sources, one after the other, for pending conversion requests. Each request source is assigned to a certain time slot within an arbitration round, called arbitration slot. The duration of an arbitration slot and the number of slots in an arbitration round are user-configurable via register **GLOBALCTR**.

The priority of each request source is user-configurable via register **RSPRO**, so the arbiter can select the next channel to be converted, in the case of concurrent requests from multiple sources, according to the application requirements.

A disabled or unused arbitration slot is considered empty and does not take part in the arbitration. After reset, all slots are disabled and must be enabled (register **ASENR**) to take part in the arbitration process.

Figure 17-11 summarizes the arbitration sequence. An arbitration round consists of one arbitration slot for each available request source. The synchronization source is always evaluated in the last slot and has a higher priority than all other sources. Additional arbitration slots can be inserted to adjust the timing to other products (not required for the XC27x8X). At the end of each arbitration round, the arbiter has determined the highest priority conversion request.

If a conversion is started in an arbitration round, this arbitration round does not deliver an arbitration winner. In the XC27x8X, the following request sources are available:

- Arbitration slot 0: **1-stage queued source**, single input channel
- Arbitration slot 1: **N-channel scan source**, sequences in defined order
- Arbitration slot 2: **4-stage sequential source**, 4-stage sequences in arbitrary order
- Last arbitration slot: **Synchronization source**, synchronized conversion requests from another ADC kernel (always handled with the highest priority in a synchronization slave kernel).

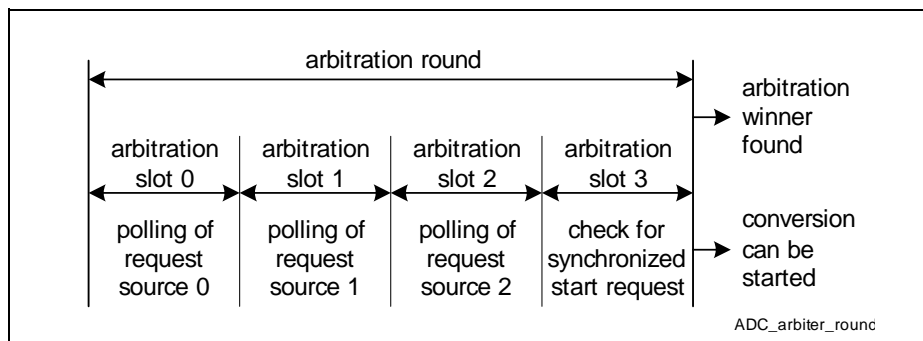


Figure 17-11 Arbitration Round

17.6.1 Arbiter Timing

The timing of the arbiter (i.e. of an arbitration round) is determined by the number of arbitration slots within an arbitration round and by the duration of an arbitration slot.

An arbitration round consist of 4, 8, 16, or 20 arbitration slots (defined by bitfield **GLOBCTR.ARBND**). 4 slots are sufficient for the XC27x8X, more can be programmed to obtain the same arbiter timing for different products.

The duration of an arbitration slot is configurable $t_{\text{Slot}} = (\text{DIVD}+1) / f_{\text{ADC}}$.

The duration of an arbitration round, therefore, is $t_{\text{ARB}} = N \times t_{\text{Slot}}$ (N = number of slots).

The period of the arbitration round introduces a timing granularity to detect an incoming conversion request signal and the earliest point to start the related conversion. This granularity can introduce a jitter of maximum one arbitration round. The jitter can be reduced by minimizing the period of an arbitration round.

To achieve a reproducible reaction time (constant delay without jitter) between the trigger event of a conversion request (e.g. by a timer unit or due to an external event) and the start of the related conversion, mainly the following two options exist. For both options, the converter has to be idle and other conversion requests must not be pending for at least one arbiter round before the trigger event occurs:

- If bit **GLOBCTR.ARB** = 0, the **arbiter runs permanently**. In this mode, synchronized conversions of more than one ADC kernel are possible.
The trigger for the conversion triggers has to be generated synchronously to the arbiter timing. Incoming triggers should have exactly n-times the granularity of the arbiter ($n = 1, 2, 3, \dots$). In order to allow some flexibility, the duration of an arbitration slot can be programmed in cycles of f_{ADC} .
- If bit **GLOBCTR.ARB** = 1, the **arbiter stops after an arbitration round** when no conversion request have been found pending any more. The arbiter is started again if at least one enabled request source indicates a pending conversion request. The trigger of a conversion request does need not to be synchronous to the arbiter timing. In this mode, parallel conversions are not possible for synchronization slave kernels.

Analog to Digital Converter

The Arbitration Slot Enable Register enables/disables the arbitration slots to control whether or not conversion requests are considered.

ASENR

Arbitration Slot Enable Register

XSFR(18_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						0							AS EN2	AS EN1	AS EN0
						r							rw	rw	rw

Field	Bits	Type	Description
ASENx (x = 0 - 2)	x	rw	Arbitration Slot x Enable Enables the associated arbitration slot of an arbiter round. The request source bits are not modified by write actions to ASENR. 0 _B The corresponding arbitration slot is disabled and considered as empty. Pending conversion requests from the associated request source are disregarded. 1 _B The corresponding arbitration slot is enabled. Pending conversion requests from the associated request source are arbitrated.
0	[15:3]	r	Reserved returns 0 if read; should be written with 0;

Note: If the arbiter shall not be running continuously (ARBM = 1), no conversion request of the request source for arbitration slot x must be active. Clear conversion requests of the related request source before disabling an arbitration slot.

17.6.2 Request Source Priority and Conversion Start Mode

Each request source has a configurable priority, so the arbiter can resolve concurrent conversion requests from different sources. The request with the highest priority is selected for conversion. These priorities can be adapted to the requirements of a given application (see register [RSPR0](#)).

The **Conversion Start Mode** determines the handling of the conversion request that has won the arbitration.

The Request Source Priority Register defines the request source priority and the conversion start mode for each request source.

Note: Only change priority and conversion start mode settings of a request source while this request source is disabled, and a currently running conversion requested by this source is finished.

RSPR0

Request Source Priority Register 0

XSFR(14 _H)														Reset Value: 0000 _H	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				CSM 2	0	PRI0 2	CSM 1	0	PRI0 1	CSM 0	0	PRI0 0			
r				rw	r	rw	rw	r	rw	rw	r	rw	rw		

Field	Bits	Type	Description
PRI00, PRI01, PRI02	[1:0], [5:4], [9:8]	rw	Priority of Request Source x Arbitration priority of request source x (in slot x) 00 _B Lowest priority is selected. ... 11 _B Highest priority is selected.
CSM0, CSM1, CSM2	3, 7, 11	rw	Conversion Start Mode of Request Source x 0 _B Wait-for-start mode 1 _B Cancel-inject-repeat mode
0	2, 6, 10, [15:12]	r	Reserved returns 0 if read; should be written with 0;

Conversion Start Mode

When the arbiter has selected the request to be converted next, the handling of this channel depends on the current activity of the converter:

- Converter is currently idle: the conversion of the arbitration winner is started immediately.
- Current conversion has same or higher priority: the current conversion is completed, the conversion of the arbitration winner is started after that.
- Current conversion has lower priority: the action is user-configurable:
 - **Wait-for-start mode:** the current conversion is completed, the conversion of the arbitration winner is started after that. This mode provides maximum throughput, but can produce a jitter for the higher priority conversion.

Example in [Figure 17-12](#):

Conversion A is requested (t1) and started (t2). Conversion B is then requested (t3), but started only after completion of conversion A (t4).

- **Cancel-inject-repeat mode:** the current conversion is aborted, the conversion of the arbitration winner is started after the abortion ($1 \dots 3 f_{\text{ADCI}}$ cycles).

The aborted conversion request is restored in the corresponding request source and takes part again in the next arbitration round. This mode provides minimum jitter for the higher priority conversions, but reduces the overall throughput.

Example in [Figure 17-12](#):

Conversion A is requested (t6) and started (t7). Conversion B is then requested (t8) and started (t9), while conversion A is aborted but requested again. When conversion B is complete (t10), conversion A is restarted.

Exception: If both requests target the same result register with wait-for-read mode active (see [Section 17.8.2](#)), the current conversion cannot be aborted.

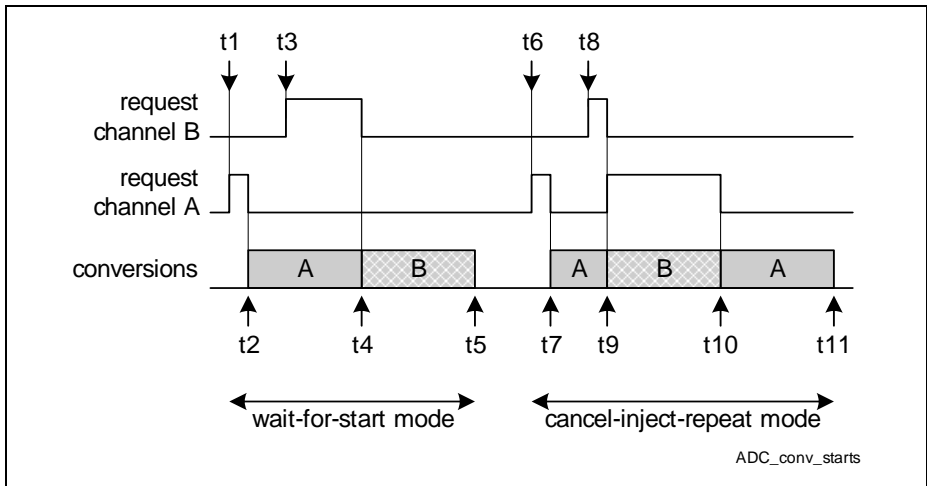


Figure 17-12 Conversion Start Modes

The conversion start mode can be individually programmed for each request source by bits in register **RSPRO** and is applied to all channels requested by the source. In this example, channel A is issued by a request source with a lower priority than the request source requesting the conversion of channel B.

17.7 Analog Input Channel Configuration

For each analog input channel, a number of parameters can be configured that control the conversion of this channel. After a channel has won the arbitration, its parameters are applied to the converter. The channel control registers (CHCTR_x on [Page 17-54](#)) define the following parameters:

- **Conversion parameters:** The input class defines sample time and data width. Each channel is assigned to one of two input classes.
- **Reference selection:** The conversion can use the standard reference (V_{AREF}) or the alternate reference (CH0). The conversion result of an input channel refers to a reference voltage (full scale digital result value if the analog input voltage equals the reference voltage¹⁾). Selecting the alternate reference e.g. allows to connect 3.3 V based sensors to the ADC in a 5.0 V system (the other input channels refers to the standard reference voltage).
Please note that low reference voltages lead to small granularity. As a consequence, the resulting TUE increases due to noise effects.
- **Result target:** The conversion result can be stored in one of 8 result registers.
- **Channel event handling:** Channel events can be restricted to results inside or outside a defined area of values (limit checking). For each channel event an interrupt node can be selected.
- **Synchronous conversion request:** Each channel can trigger a synchronized conversion in the other kernel.

In addition to the general channel control, the ADC kernel supports a mechanism (named alias feature, see [Section 17.7.3](#)) to redirect a conversion request to another channel number.

If more analog inputs are required than input pins are available, external analog multiplexers can be added. These external multiplexers can be automatically controlled by the ADC logic. This is described in [Section 17.11](#).

1) Because the compensated ideal transfer curve of the ADC has its first code transition when the input value reaches 0.5 LSB_n , the full scale digital result value is reached when the input value is 1.5 LSB_n below the reference voltage.

17.7.1 Channel Parameters

Each analog input channel is configured by its associated channel control register. The sample time and the result width are selected via an input class.

The Channel Control Registers select the control parameters for each input channel.

CHCTR_x (x = 0 - 15)

Channel x Control Register **XSFR(20_H + x * 2)** **Reset Value: 0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	RESR SEL		ICL SEL		REF SEL		SYN C	LCC		BNDB SEL		BNDA SEL			
r	rw		rw		rw		rw	rw		rw		rw			

Field	Bits	Type	Description
BNDASEL	[1:0]	rw	Boundary A Selection Defines the boundary A register for limit checking. 00 _B Use register LCBR0 01 _B Use register LCBR1 10 _B Use register LCBR2 11 _B Use register LCBR3
BNDBSEL	[3:2]	rw	Boundary B Selection Defines the boundary B register for limit checking. 00 _B Use register LCBR0 01 _B Use register LCBR1 10 _B Use register LCBR2 11 _B Use register LCBR3
LCC	[6:4]	rw	Limit Check Control Defines the condition under which a channel event is generated (see Section 17.7.2 on Page 17-57). 000 _B Never 001 _B Result outside area I 010 _B Result outside area II 011 _B Result outside area III 100 _B Always (boundaries disregarded) 101 _B Result within area I 110 _B Result within area II 111 _B Result within area III

Analog to Digital Converter

Field	Bits	Type	Description
SYNC	7	rw	Synchronization Request Selects a synchronized (parallel) conversion with the other ADC kernel. 0 _B No synchronization request 1 _B Select a synchronized conversion for this channel <i>Note: Only taken into account for a potential master (SYNCTR.STSEL = 00_B), considered as 0 otherwise.</i>
REFSEL	[9:8]	rw	Reference Input Selection Defines the reference source for this channel. 00 _B Select the standard reference input V_{AREF} 01 _B Select the alternative reference input CH0 10 _B reserved, do not use 11 _B reserved, do not use
ICLSEL	[11:10]	rw	Input Class Selection Defines the channel-specific parameters. 00 _B Select input class 0 01 _B Select input class 1 10 _B reserved, do not use 11 _B reserved, do not use
RESRSEL	[14:12]	rw	Result Register Selection Selects the target for the conversion result(s). 000 _B Use result register 0 001 _B Use result register 1 ... 111 _B Use result register 7
0	15	r	Reserved returns 0 if read; should be written with 0;

Note: Not all channels are available in all products.

Therefore, only the channel control registers with corresponding channels are valid.

Analog to Digital Converter

An input class defines the length of the sample phase and the resolution of the conversion. Two input classes can be defined and each channel is assigned to one of them. This supports applications with different input circuitries (impedance, RC input filter).

The default settings select the minimum sample phase length of $2f_{\text{ADCI}}$ cycles and a result width of 10 bits.

The Input Class Registers select the sample time and the resolution for each input class.

INPCR_x (x = 0 - 1)

Input Class Register x

XSFR(C0_H + x * 2)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0						DW		STC							
r						rw		rw							

Field	Bits	Type	Description
STC	[7:0]	rw	Sample Time Control Number of additional clock cycles to be added to the minimum sample phase of 2 analog clock cycles: $t_{\text{SAMPLE}} = (2 + \text{STC}) / f_{\text{ADCI}}$ For conversions of external channels, this value can be replaced by EMSAMPLE in register EMCTR .
DW	[9:8]	rw	Data Width Defines the number of converted bits for the result. The conversion results are left aligned in the result bitfields. Bit positions that are not converted are 0. 00 _B The result is 10 bits wide (bits 11 ... 2) 01 _B The result is 12 bits wide (bits 11 ... 0) 10 _B The result is 8 bits wide (bits 11 ... 4) Else: reserved, do not use
0	[15:10]	r	Reserved returns 0 if read; should be written with 0;

17.7.2 Limit Checking

The limit checking mechanism automatically compares each conversion result to two boundary values (boundary A and boundary B). For each channel, the user can select these boundaries from a set of 4 programmable values (**LCBR0** to **LCBR3**).

A channel event is then generated depending on the two comparisons. The conditions are selected via bitfield LCC in the respective channel control register.

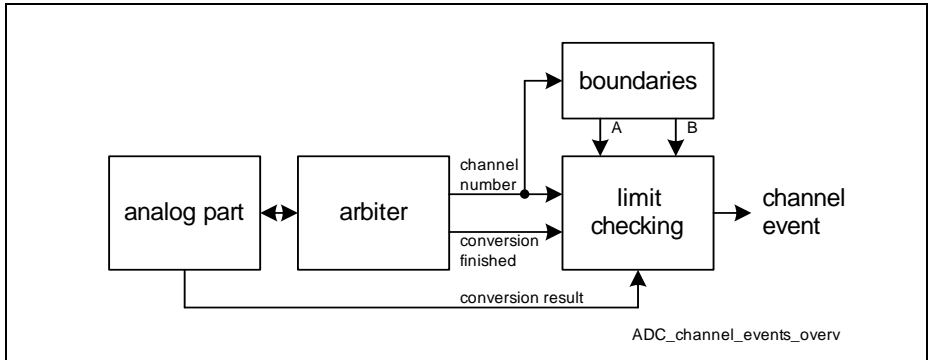


Figure 17-13 Channel Event Generation

The two selectable boundaries split the conversion result range into three areas:

- Area I: Conversion result below or equal to both boundaries.
- Area II: Conversion result above one boundary and below/equal to other boundary.
- Area III: Conversion result above both boundaries.

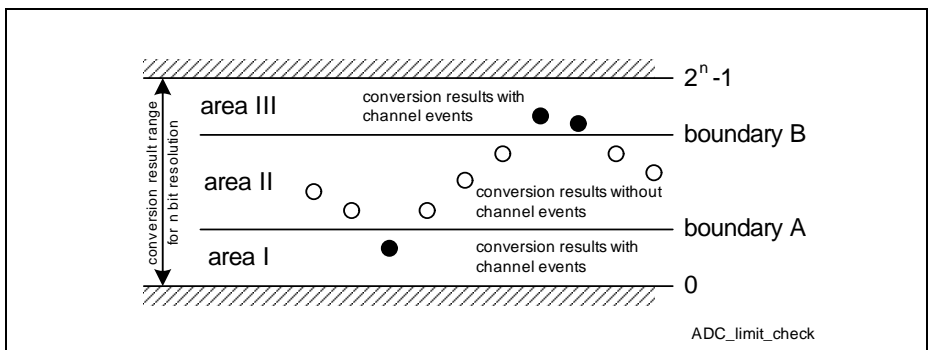


Figure 17-14 Limit Checking

The shown example for limit checking generates channel events only if the conversion results are outside the normal operating range defined by area II (LCC = 010_B).

Analog to Digital Converter

If only two areas are required, use the same boundary register for boundary A and boundary B. In this case, area II is empty and two result ranges are available. Avoid $LCC = x10_B$ in this case.

Typical applications for limit checking are monitoring tasks (temperature, pressure, current, etc.) where the real value of a result is less important than its range. As long as the measured values are within their defined valid range, no CPU action is required. A channel event should be generated only if the conversion result is outside the valid range to indicate a critical condition (over-temperature, loss of pressure, etc.).

The CPU load is minimized if the conversions of the analog input signals to be monitored are part of an auto-scan sequence autonomously triggered on a regular time base. Under normal conditions the CPU load here is zero.

Note: In the case of an over-current protection, the channel event can be used to disable PWM generation to reduce the current (in the XC27x8X, an interrupt output line of the ADC module is connected to a corresponding input of the CCU6x units to allow fast reactions without CPU intervention).

Analog to Digital Converter

The Limit Check Boundary Registers define compare values (boundaries) for the limit checking unit. The reset values of the boundaries are defined as 10%, 90%, 33% and 66% of the complete result range.

LCBR0

Limit Check Boundary Register 0 XSFR(84_H) **Reset Value: 0198_H**

LCBR1

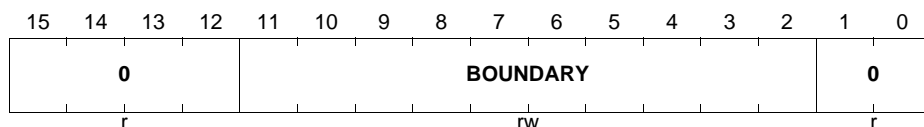
Limit Check Boundary Register 1 XSFR(86_H) **Reset Value: 0E64_H**

LCBR2

Limit Check Boundary Register 2 XSFR(88_H) **Reset Value: 0554_H**

LCBR3

Limit Check Boundary Register 3 XSFR(8A_H) **Reset Value: 0AA8_H**



Field	Bits	Type	Description
BOUNDARY	[11:2]	rw	Boundary for Limit Checking This value is compared to the actual conversion result. ¹⁾
0	[1:0], [15:12]	r	Reserved returns 0 if read; should be written with 0;

- 1) For 8-bit conversion results, bits 2 and 3 of the boundary value are compared with 00_B.
 For 12-bit conversion results, bits 0 and 1 of the result value are compared with 00_B.

Note: The boundary values use the same representation as the result values, i.e. they are left-adjusted on bit 11.

17.7.3 Alias Feature

The alias feature re-directs conversion requests for channels CH0 or CH1 to other channel numbers. This means that CH0/CH1 are converted with the channel parameters of the referenced channel instead of with their own. The re-direction feature serves several purposes:

- The same signal can be measured twice and the two results (original and re-directed) can be stored in separate result registers. This allows triggering both conversions quickly one after the other while data loss is avoided, independent from the CPU interrupt latency.
 The sensor signal is connected to only one input (instead of two). This can save input pins in low-cost applications and reduces the input leakage to be considered in the error calculation.
- Even if the analog input CH0 is used as alternate reference (see [Figure 17-15](#)), the internal trigger and data handling features for channel CH0 can be used.
- The channel settings for both conversions (of the same signal) can be different in terms of boundary values, interrupts, etc.
- If a queued conversion request source has been set up, a conversion request for channels CH0 or CH1 can be easily re-directed to other input channels without flushing the queue.

Figure 17-15 shows an example where the sensor signal is connected to one input channel (CHx) but two conversions are triggered (for CHx and CH0). The alias feature re-directs the conversion request for CH0 to CHx, but taking into account the settings for CH0. Although the same analog input (CHx) has been measured, the conversion results can be stored and retrieved from result registers RESRx (conversion triggered for CHx) and RESR0 (conversion triggered for CH0). Additionally, different interrupts or limit boundaries can be selected, enabled or disabled.

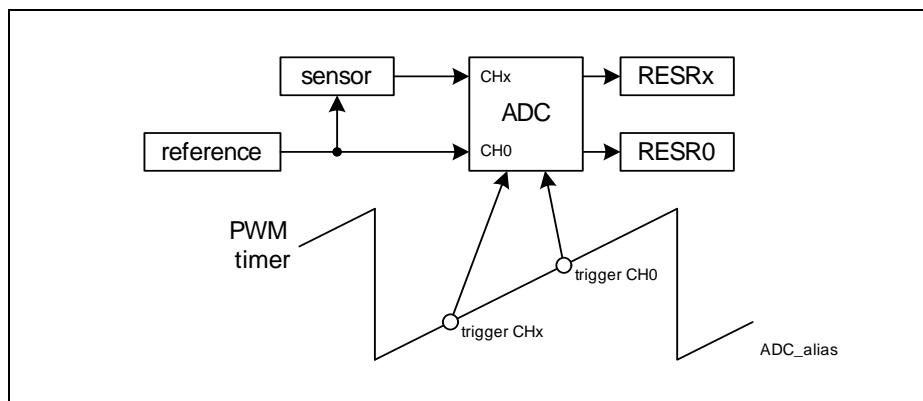


Figure 17-15 Alias Feature

Analog to Digital Converter

In typical low-cost AC-drive applications, only one common current sensor is used to determine the phase currents. Depending on the applied PWM pattern, the measured value has different meanings and the sample points have to be precisely located in the PWM period.

The Alias Register specifies replacement channel numbers for CH0 and CH1, i.e. CH0 and CH1 will use the respective channel numbers when requested.

The programmed alias channel number controls the analog input multiplexer (of the converter). The original channel number controls all other internal actions and the synchronization request.

ALR0

Alias Register 0

XSFR(1C_H)

Reset Value: 0100_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		ALIAS1						0		ALIAS0					
r		rw						r		rw					

Field	Bits	Type	Description
ALIAS0	[4:0]	rw	Alias Value for CH0 Conversion Requests Replacement channel number for channel CH0. The conversion is done with the settings defined for CH0.
ALIAS1	[12:8]	rw	Alias Value for CH1 Conversion Requests Replacement channel number for channel CH1. The conversion is done with the settings defined for CH1.
0	[7:5], [15:13]	r	Reserved returns 0 if read; should be written with 0;

17.7.4 Conversion Timing

The total time required for a conversion depends on several user-definable factors:

- The ADC conversion clock frequency, where $f_{\text{ADCI}} = f_{\text{ADC}} / (\text{DIVA}+1)^{1)}$
- The selected sample time, where $t_{\text{S}} = (2 + \text{STC}) \times t_{\text{ADCI}}$
(STC = additional sample time, see also [Section 17.4.3](#))
- The selected result width N (8/10/12 bits)
- The post-calibration time PC, if selected (PC = 2, otherwise 0)
- Synchronization steps done at module clock speed

The conversion time is the sum of sample time, conversion steps, and synchronization. It can be computed with the following formula:

$$t_{\text{CN}} = (2 + \text{STC} + \text{N} + 1 \times \text{PC}) \times t_{\text{ADCI}} + 2 \times t_{\text{ADC}}$$

The frequency at which conversions are triggered also depends on several configurable factors:

- The selected conversion time, according to the input class definitions. For conversions using an external multiplexer, also the extended sample times count.
- Delays induced by cancelled conversions that must be repeated.
- Delays due to equidistant sampling of other channels.
- The configured arbitration cycle time.
- The frequency of external trigger signals, if enabled.

1) The minimum prescaler factor is 2.

17.7.5 Channel Events and Interrupts

A channel event interrupt can be generated based on a channel event according to the structure shown in **Figure 17-16**. If a channel event is detected, it sets the corresponding indication flag in register **CHINFR**. These flags can also be set by writing a 1 to the corresponding bit position, whereas writing 0 has no effect. The indication flags can be cleared by SW by writing a 1 to the corresponding bit position in register **CHINCR**.

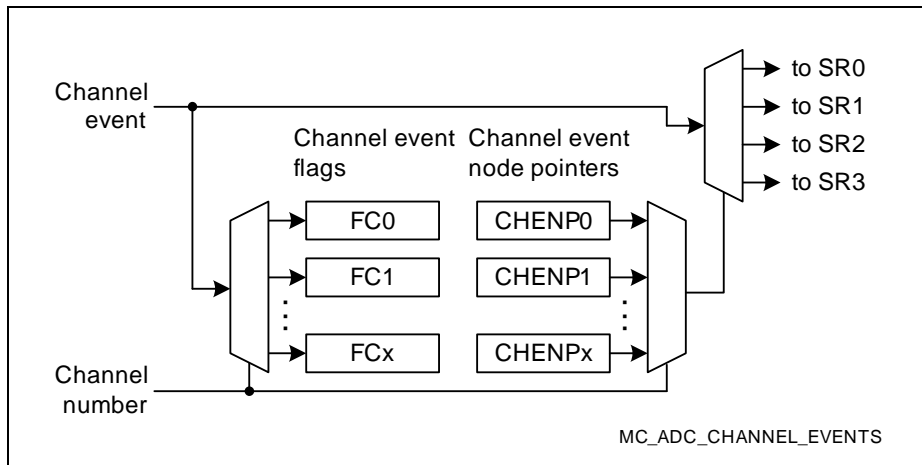


Figure 17-16 Channel Event Interrupt Generation

The service request output line SRx that is selected by the channel node pointer bitfields in registers **CHINPRO** etc., is activated each time the related channel event is detected or the related bit position in register **CHINFR** is written with a 1.

17.8 Conversion Result Handling

The conversion results of each analog input channel can be stored in one of 8 conversion result registers (selected by bitfield RESRSEL in the associated channel control register CHCTR_x). This structure provides different locations for the conversion results of different groups of channels. Depending on the application needs (data reduction, auto-scan, alias feature, result FIFO, etc.), the user can distribute the conversion results to minimize CPU load or to be more tolerant against interrupt latency.

17.8.1 Storage of Conversion Results

Each result register has an individual data valid flag (VF_x) associated with it. This flag indicates when “new” valid data has been stored in the corresponding result register and can be read out.

Depending of the result register read view (see below), the corresponding valid flag is automatically cleared when the result is read or remains set.

- Automatically clearing the valid flag provides an easy handshake between result generation and retrieval. This also supports wait-for-read mode.
- Leaving the valid flag set supports debugging by delivering the result value without disturbing the handshake with the application.

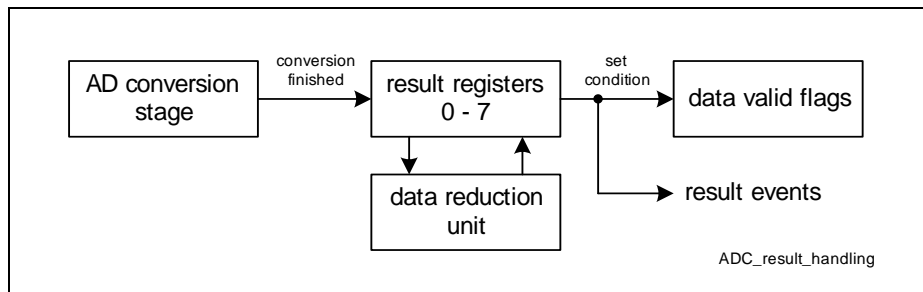


Figure 17-17 Conversion Result Storage

Conversion result handling comprises the following functions:

- Storage of conversion results to user-configurable registers
- Wait-for-read mode to avoid loss of data if several channels share one result register (see [Section 17.8.2](#))
- Result event interrupts (see [Section 17.8.4](#))
- Concatenate result registers to build result FIFO buffers (see [Section 17.8.3](#))
- Data reduction or anti-aliasing filtering (see [Section 17.8.5](#))

Up to 4 result values can be added in each result register. This reduces the frequency of interrupts generated by the ADC.

Conversion results are left-aligned on bit 11. Depending on the number of added results, the data width is extended up to bit 13.

- Standard application read view **RESRx (x = 0-7)**:
Bits 15-12 indicate the channel number whose conversion triggered the result event.
Bits 11-0 return the result. Reading the result automatically clears the valid flag.
This view is useful only without data reduction.
- Standard debugger read view **RESRVx (x = 0-7)**:
Same as standard application read view, but the corresponding valid bit is not cleared when the result register is read.
- Accumulated application read view **RESRAx (x = 0-7)**:
Returns the accumulated results. No channel number is inserted.
Reading the result automatically clears the valid flag.
- Accumulated debugger read view **RESRAVx (x = 0-7)**:
Same as accumulated standard read view, but the corresponding valid bit is not cleared when the result register is read.

Each result register can be accessed via its 4 different read views, and is associated with a corresponding result control register (**RCRx (x = 0 - 7)**). The valid flags can be read either individually from the corresponding RCRx or altogether from the valid flag register VFR.

The result status shadow register **RSSR** stores the result register number and the channel number of the result value having been read last.

Analog to Digital Converter

The accumulated read views of the result registers deliver the accumulated conversion result generated by the data reduction feature.

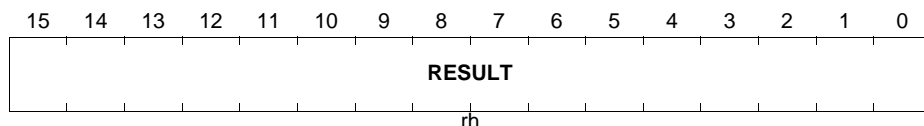
The corresponding valid flag is cleared when register RESRAX is read (application view), whereas it is left unchanged when reading RESRAVx (debugger view).

RESRAx (x = 0-7)

Result Register x, View A **XSFR(50_H + 2 * x)** **Reset Value: 0000_H**

RESRAVx (x = 0-7)

Result Register x, View AV **XSFR(70_H + 2 * x)** **Reset Value: 0000_H**



Field	Bits	Type	Description
RESULT	[15:0]	rh	Conversion Result Sum of accumulated conversion results. The number of valid bits (12/13/14) depends on the selected data preprocessing mode.

Analog to Digital Converter

The Result Status Shadow Register is updated when an application view result register is read. It provides result register number and channel number of the most recent read access.

RSSR

Result Status Shadow Register XSFR(82_H) Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		RRNR		0						CHNR					
r		rh		r						rh					

Field	Bits	Type	Description
CHNR	[4:0]	rh	Channel Number Indicates the channel number related to the latest result that has been read out.
RRNR	[14:12]	rh	Result Register Number Indicates the result register for the information stored in CHNR.
0	[11:5], 15	r	Reserved returns 0 if read; should be written with 0;

Note: The accumulated views of the result registers only return the conversion result value. If required, the application can read the channel number from bitfield CHNR after reading RESRAX.

Analog to Digital Converter

The Result Control Registers control the behavior of the result registers and monitor their status.

RCRx (x = 0 - 7)

Result Control Register x **XSFR(B0_H + 2 * x)** **Reset Value: 0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		VF		0		DRC		0		WFR	FEN	IEN	0		DRCTR
r		rh		r		rh		r	rw	rw	rw	r	rw		

Field	Bits	Type	Description
DRCTR	[1:0]	rw	Data Reduction Control Defines the number of accumulated conversion results for data reduction. The data reduction counter DRC is loaded with this value. 00 _B Accumulate 1 conversion result value (data reduction mode is disabled) 01 _B Accumulate 2 conversion result values 10 _B Accumulate 3 conversion result values 11 _B Accumulate 4 conversion result values
IEN	4	rw	Interrupt Enable 0 _B No result event interrupt 1 _B Generate an interrupt upon a result event
FEN	5	rw	FIFO Enable Controls the FIFO functionality for result register x (see Section 17.8.3) 0 _B Standard result register or FIFO input register 1 _B FIFO functionality enabled, i.e. this register builds a part of the FIFO
WFR	6	rw	Wait-for-Read Mode Enables wait-for-read mode for result register x. 0 _B Overwrite mode 1 _B Wait-for-read mode enabled

Field	Bits	Type	Description
DRC	[9:8]	rh	Data Reduction Counter Counts the conversion results still to be accumulated for the final result of the data reduction. The valid flag is set and a result event is generated when this bitfield becomes 0 (by decrementing or by reload). Bitfield DRC can be cleared by writing a 1 to bit position x in register VFR . 00 _B Accumulation complete, the final result is available in the result register 01 _B 1 more result to be added 10 _B 2 more results to be added 11 _B 3 more results to be added
VF	12	rh	Valid Flag Indicates valid contents in result register x. 0 _B No new valid data available 1 _B Result register x contains valid data and has not yet been read This flag can also be read from the general valid flag register VFR-
0	[3:2], 7, [11:10], [15:13]	r	Reserved returns 0 if read; should be written with 0;

Analog to Digital Converter

The Valid Flag Register summarizes the flags indicating that the corresponding result register contents are valid. These flags can also be read from the individual result control registers RCRx.

VFR

Valid Flag Register

XSFR(80_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								VF	VF	VF	VF	VF	VF	VF	VF
								7	6	5	4	3	2	1	0
								rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
VFx (x = 0 - 7)	x	rwh	Valid Flag for Result Register x Indicates that the contents of result register x is valid, i.e. has been updated but not yet read. Read access: 0 _B No new valid data available 1 _B Result register x contains valid data and has not yet been read Write access: 0 _B No effect 1 _B Clear this valid flag and bitfield DRC in register RCRx (overrides a hardware set action)
0	[15:8]	r	Reserved returns 0 if read; should be written with 0;

17.8.2 Wait-for-Read Mode

The wait-for-read mode is a feature to prevent data loss due to overwriting a result register with a new conversion result before the CPU (or PEC) has read the previous data. For example, auto-scan conversion sequences or other sequences with “relaxed” timing requirements are likely to use the same result register. However, the results come from different input channels, so an overwrite would destroy the result from the previous conversion¹⁾.

Wait-for-read mode automatically suspends the start of a conversion for this channel until the current result has been read. So a conversion or a conversion sequence can be requested by a hardware or software trigger, while each conversion is only started after the previous one has been read. This automatically aligns the conversion sequence with the CPU capability to read the formerly converted result (interrupt latency).

If wait-for-read mode is enabled for a result register (bit WFR = 1 in the corresponding result control register), a request source does not generate a conversion request while the targeted result register contains valid data (indicated by the valid flag VFx = 1) or if a currently running conversion targets the same result register.

If two request sources target the same result register with wait-for-read mode selected, a higher priority source cannot interrupt a lower priority conversion request started before the higher priority source has requested its conversion. Cancel-inject-repeat mode does not work in this case. If the higher priority request targets a different result register, the lower priority conversion can be cancelled and repeated afterwards.

1) Repeated conversions of a single channel that use a separate result register will not destroy other results, but rather update their own previous result value. This way, always the actual signal data is available in the result register.

17.8.3 Result FIFO Buffer

Result registers can either be used as direct target for conversion results (see bitfield RESRSEL in register CHCTR_x) or it can be concatenated with other result registers of the same ADC kernel to form a result FIFO buffer (first-in-first-out buffer mechanism). A result FIFO stores several measurement results that can be read out later with a “relaxed” CPU response timing. It is possible to set up more than one FIFO buffer structure with the available result registers.

Result FIFO structures of two or more registers are built by concatenating result registers to their following “neighbor” result register (see [Figure 17-18](#)) by setting bit RCR_x.FEN = 1.

Conversion results are stored to the register with the highest index of a group. Software reads the values from the register with the lowest index of a group.

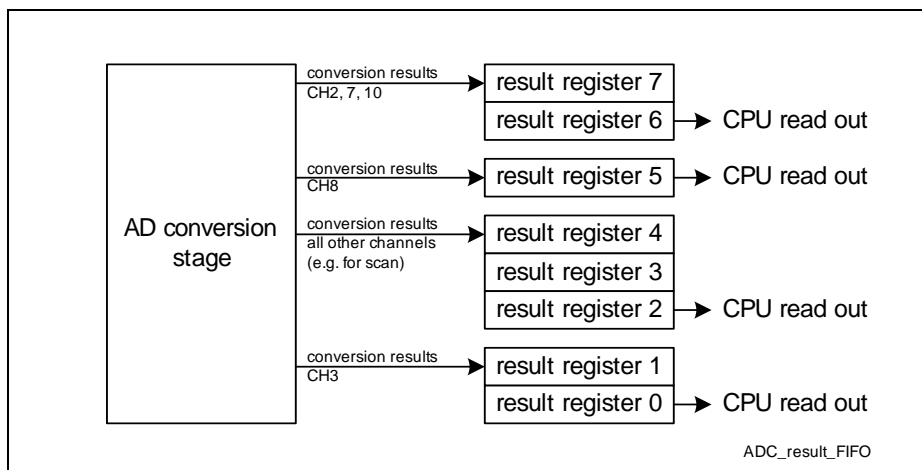


Figure 17-18 Result FIFO Buffers

In the example shown the result registers have been configured in the following way:

- 2-stage buffer consisting of result registers 7-6
- dedicated result register 5
- 3-stage buffer consisting of result registers 4-3-2
- 2-stage buffer consisting of result registers 1-0

[Table 17-4](#) summarizes the required configuration of result registers if they are combined to build result FIFO buffers.

Table 17-4 Properties of Result FIFO Registers

Function	Input Stage	Intermed. Stage	Output Stage
Result target	YES	no	no
Application read	no	no	YES
Data reduction mode	YES	no	no
Wait-for-read mode	YES	no	no
Result event interrupt	no	no	YES
FIFO enable bit (FEN)	0	1	1
Registers in example	7, 4, 1	3	6, 2, 0

Note: If enabled, a result interrupt is generated for each data word in the FIFO.

17.8.4 Result Events and Interrupts

A result event interrupt can be generated based on a result event according to the structure shown in [Figure 17-19](#). If a result event is detected, it sets the corresponding indication flag in register [EVINFR](#). These flags can also be set by writing a 1 to the corresponding bit position, whereas writing 0 has no effect. The indication flags can be cleared by SW by writing a 1 to the corresponding bit position in register [EVINCR](#).

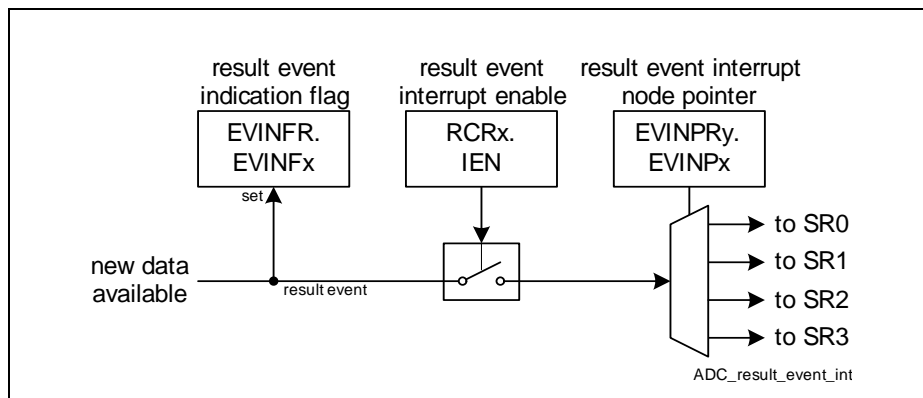


Figure 17-19 Result Event Interrupt Generation

The service request output line SRx that is selected by the result event interrupt node pointer bitfields in registers [EVINPR8](#) or [EVINPR12](#) issues an interrupt each time the related result event is detected or the related bit position in register [EVINFR](#) is written with a 1.

The result events and the request source events share the same registers. The result events are located at the following bit positions in register [EVINFR](#):

- Event 8: Result event of result register 0.
- Event 9: Result event of result register 1.
- ...
- Event 15: Result event of result register 7.

17.8.5 Data Reduction and Filtering

Data reduction automatically accumulates a series of conversion results before generating a result interrupt. This can remove some noise from the input signal and reduces the CPU load required to unload the conversion data from the ADC.

The standard data reduction mode accumulates result values within arbitrary result registers.

The enhanced data reduction filter additionally pre-processes the result values by applying filter algorithms (such as moving average).

Standard Data Reduction Mode

The data reduction mode can be used as digital filter for anti-aliasing or decimation purposes. It accumulates a maximum of 4 conversion results to generate a final result.

Each result register can be individually enabled for data reduction, controlled by bitfield DRCTR in registers **RCRx** ($x = 0 - 7$). The data reduction counter DRC indicates the actual status of the accumulation.

Note: Conversions for other result registers can be inserted between conversions to be accumulated.

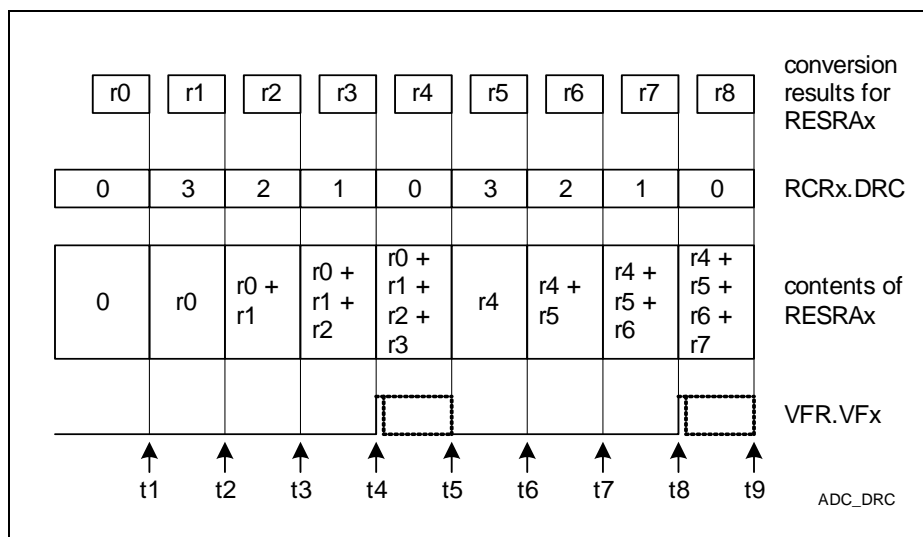


Figure 17-20 Standard Data Reduction Filter

This example shows a data reduction sequence of 4 accumulated conversion results. Eight conversion results (r0 ... r7) are accumulated and produce 2 final results.

Analog to Digital Converter

When a conversion is complete and stores data to a result register that has data reduction mode enabled, the data handling is controlled by the data reduction counter DRC:

- If $DRC = 0$ (t_1 , t_5 , t_9 in the example), the conversion result is stored to the register. DRC is loaded with the contents of bitfield RCRx.DRCTR (i.e. the accumulation begins).
- If $DRC > 0$ (t_2 , t_3 , t_4 and t_6 , t_7 , t_8 in the example), the conversion result is added to the value in the result register. DRC is decremented by 1.
- If DRC becomes 0, either decremented from 1 (t_4 and t_8 in the example) or loaded from DRCTR, the valid bit for the respective result register is set and a result register event occurs.

The final result must be read before the next data reduction sequence starts (before t_5 or t_9 in the example). This automatically clears the valid flag.

Note: Software can clear the data reduction counter DRC by clearing the corresponding valid flag (via [VFR](#)).

The response time to read the final data reduction results can be increased by associating the adjacent result register to build a result FIFO (see [Figure 17-21](#)). In this case, the final result of a data reduction sequence is loaded to the adjacent register. The value can be read from this register until the next data reduction sequence is finished (t_8 in the 2nd example).

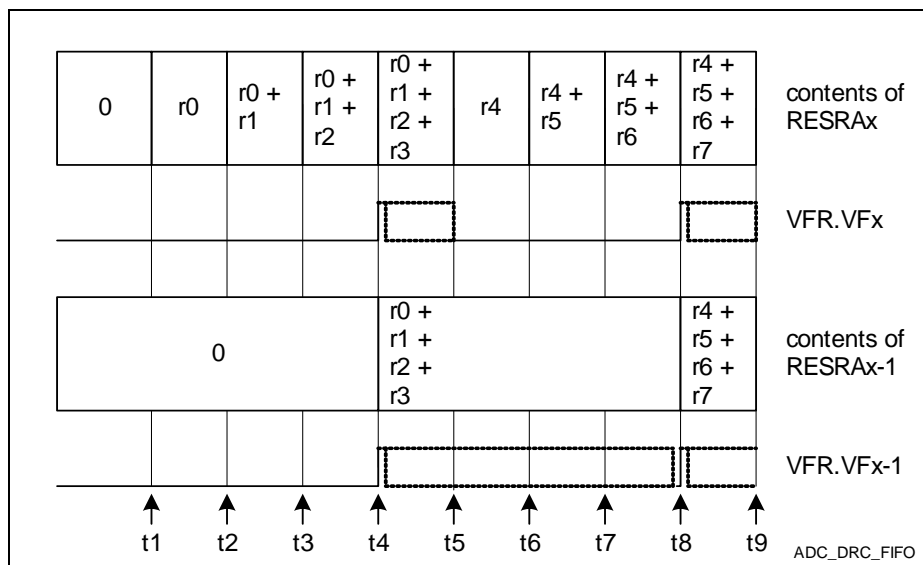


Figure 17-21 Standard Data Reduction Filter with Result FIFO

Enhanced Data Reduction Unit

The additional enhanced Data Reduction Unit adds multiple conversion results according to a certain algorithm and provides them to the CPU at a reduced service request rate.

Two filter blocks accept input data from a selectable conversion result register. The filter blocks can also be concatenated. A service request can be generated, when the result of a filter operation is stored in one of the final result registers. Each filter block supports typical digital filter operations such as moving average calculations with intermediate results.

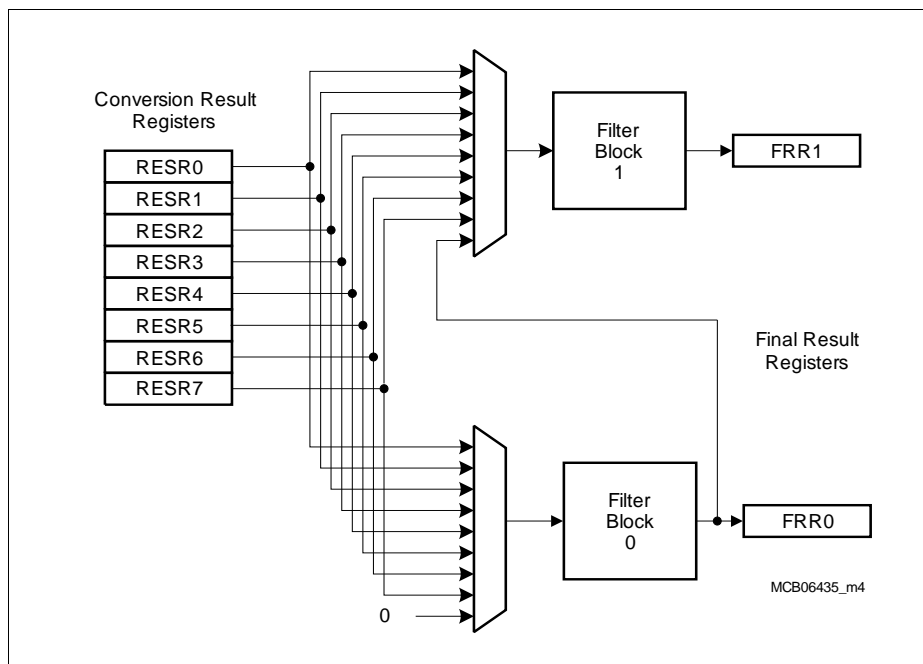


Figure 17-22 Enhanced Data Reduction Filter Blocks

A filter block consists of an adder and several data registers for calculating filter output data from the filter input data. The Current Result Register CRR_n is used to add a set of conversion results. When the set of results has been added, the intermediate result in CRR_n is shifted to the Intermediate Result Register IRR_{1n}. The three intermediate result registers of filter block 0 build a pipeline, i.e. the value in IRR₂₀ moves to IRR₃₀, the value in IRR₁₀ moves to IRR₂₀, the value in CCR₀ moves to IRR₁₀. The Final Result Register FRR_n stores the sum that is computed from the contents of the current result register and the intermediate result register(s).

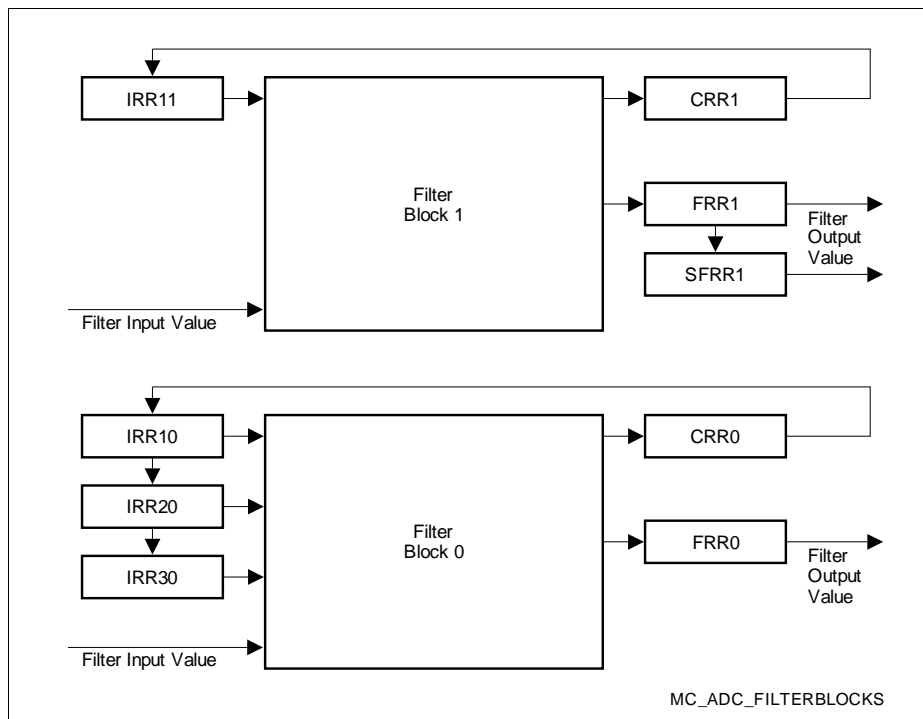


Figure 17-23 Filter Block Structure

All result registers of a filter block can be read at any time.

A filter block can be used for data-reduction or anti-aliasing filtering of the conversion results (n indicates the number of the filter block). It performs a combination of data reduction by adding and a moving average operation.

- A continuous A/D conversion is running on channel x .
- The filter input selection is set to channel x ($FCRn.INSEL = 1000_B + x$).
- The addition length is controlled by $FCRn.ADDL$ defining how many conversion results are added to build one intermediate result (intermediate cycle).
- The moving average length is controlled by $FCRn.MAVL$ defining how many intermediate results are taken into account for a moving average to build the final result (final result cycle).

Note: The enhanced filter is especially advantageous for knock-detection applications. These applications will preferably use 10-bit conversions due to reasons of speed and/or resolution requirements.

Therefore, all input values to the enhanced filter block are 10 bits wide.

Intermediate results are calculated by adding a programmable number of conversion results in register CRRn. After that, CRRn contains a new intermediate result and the calculation of the next final result value by moving average is started. Then CRRn is cleared automatically after the final result cycle to be prepared for the first conversion result of the next intermediate cycle.

Before the filter operation of continuous conversion results of channel x is started, the filter block n has to be cleared (writing SRFn.RSTF = 1) after programming the filter control bitfields.

Final results are calculated when an intermediate cycle has been finished. The new intermediate result (stored in CRRn) and the contents of the intermediate registers IRRnx are added to build the final result in FRRn. The number of intermediate results taking part in the moving average operation to build the final result is programmable, the maximum is given by:

- Filter block 0: $FRR0 := CRR0 + IRR10 + IRR20 + IRR30$
- Filter block 1: $FRR1 := CRR1 + IRR11$

At the end of the final result cycle, the contents of IRR2n are transferred into IRR3n, then the contents of IRR1n into IRR2n, then the contents of CRRn into IRR10 (for filter block 1). The former contents of IRR3n are lost.

Bit field FCRn.MAVL determines the number of intermediate results that are used for the final result calculation. For filter block 1 only two bit combinations is valid and the intermediate result registers IRR2n and IRR3n are not available and handled as if they were 0.

Each update of a result register FRRn with a new final result value generates a filter block n service request.

The two filter blocks can be concatenated by selecting the output of filter 0 as the input for filter 1.

All selections are configured in the filter control registers (**FCRn (n = 0-1)**).

Because the filter blocks repeatedly accumulate data values, the width of the employed registers depends on their position within the filter chain (see **Table 17-5**).

Table 17-5 Data Width of Result Registers

Register Long Name	Short Name	Result Width
Filter 0 Current Result Register	CRRH/L0	13 bits (8 × 10-bit input values)
Filter 0 Intermediate Result Register 1	IRR10	
Filter 0 Intermediate Result Register 2	IRR20	
Filter 0 Intermediate Result Register 3	IRR30	
Filter 0 Final Result Register (result in Q15 format)	FRR0	15 bits (4 × 13-bit intermediate results)
Filter 1 Current Result Register	CRRH/L1	18 bits (8 × 15-bit results from Filter 0)
Filter 1 Intermediate Result Register 1	IRR11H/L	
Filter 1 Final Result Register (lower 15 bits of result in Q15 format)	FRR1	20 bits (2 × 18-bit intermediate results)
Filter 1 Shifted Final Result Register (upper 15 bits of result in Q15 format)	SFRR1	Parts of this internal result can be read via FRR1 and SFRR1.

Note: Register SFRR1 provides another view of the final result in register FRR1, shifted right by 5 bit positions. This allows access to the result data within a 16-bit word (Q15 format) for further digital data handling.

Analog to Digital Converter

The Filter n Control Register configures the operation parameters for the respective filter block.

FCRn (n = 0-1)

Filter n Control Register

XSFR(280_H + n*10_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IEN	0	INP			INSEL			0		MAVL		0		ADDL	
rw	r	rw			rw			r		rw		r		rw	

Field	Bits	Type	Description
ADDL	[2:0]	rw	Addition Length Determines the number of filter input values that are added to obtain one intermediate result. 000 _B Each filter input value is considered as intermediate result 001 _B 2 filter input values are accumulated ... 111 _B 8 filter input values are accumulated
MAVL	[5:4]	rw	Moving Average Length Determines the number of intermediate results that are added to obtain one final result. 00 _B No moving average: FRRn.FR = CRRn.CR 01 _B Moving average of 2 values: FRRn.FR = CRRn.CR + IRR1n.IR 10 _B Moving average of 3 values: FRRn.FR = CRRn.CR + IRR1n.IR + IRR2n.IR 11 _B Moving average of 4 values: FRRn.FR = CRRn.CR + IRR1n.IR + IRR2n.IR + IRR3n.IR <i>Note: Bit combinations 10_B and 11_B are not available in filter block 1 and must not be selected there.</i>

Field	Bits	Type	Description
INSEL	[11:8]	rw	Input Selection Enables the filter block and selects its input value. 0000 _B The filter block is disabled 0001 _B Input from any result register 0010 _B Filter block 0: Filter block disabled (as 0000 _B) Filter block 1: Input from register FRR0 value, concatenates filter block 0 with filter block 1 0011 _B Reserved 01XX _B Reserved 1000 _B Input from conversion result register 0 ... 1111 _B Input from conversion result register 7
INP	[13:12]	rw	Interrupt Node Pointer Selects the service request output to be activated when a final result of filter block n is available while bit IEN is set. 00 _B Service request output SR0 selected 01 _B Service request output SR1 selected 10 _B Service request output SR2 selected 11 _B Service request output SR3 selected
IEN	15	rw	Interrupt Enable Enables the generation of a new final result service request of filter block n. 0 _B No service request 1 _B Service request generation enabled
0	3, [7:6], 14	r	Reserved Read as 0. Should be written with 0.

Analog to Digital Converter

The Status Register of Filter n provides the interrupt flag of a filter block as well as control bits for this flag and a reset trigger for all filter registers.

SRFn (n = 0-1)

Status Register Filter n

XSFR(28E_H + n*10_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				RST F	0	CIR QF	SIRQ F	0							IRQF
r				w	r	w	w					r			rh

Field	Bits	Type	Description
IRQF	0	rh	Interrupt Request Flag for Filter Indicates that a filter sequence has been finished and a new final result is available. 0 _B Filter sequence not yet finished 1 _B A final result is available Bit IRQF must be cleared by software (SIRQF = 1). Interrupt requests are also generated (if enabled) while IRQ = 1.
SIRQF	8	w	Set Interrupt Request Flag for Filter 0 _B No action 1 _B Set bit IRQF and generate an interrupt if IEN = 1
CIRQF	9	w	Clear Interrupt Request Flag for Filter 0 _B No action 1 _B Clear bit IRQF
RSTF	11	w	Reset Filter 0 _B No action 1 _B Clear all filter registers, except for bitfield CRRHn.AC that is loaded with the value of FCRn.ADDL
0	[7:1], 10, [15:12]	r	Reserved returns 0 if read; should be written with 0;

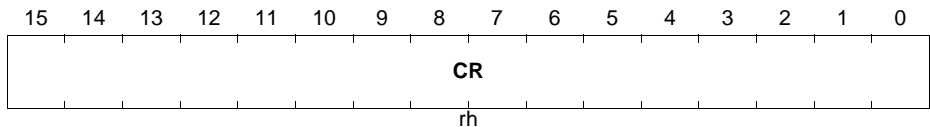
Analog to Digital Converter

The Current Result Register (CRRHn and CRRLn) stores the current result of filter n along with further status information of filter block n.

CRRLn (n = 0-1)

Filter n Current Result Low Reg. XSFR(282_H + n*10_H)

Reset Value: 0000_H

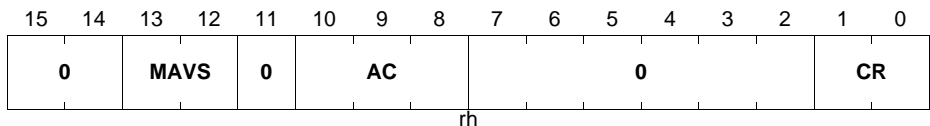


Field	Bits	Type	Description
CR	[15:0]	rh	Current Result Right-aligned current result value Filter 0: bits [12:0] Filter 1: bits [15:0] (+ CRRH.CR) CR is cleared when writing SRFn.RSTF = 1.

CRRHn (n = 0-1)

Filter n Current Result High Reg. XSFR(284_H + n*10_H)

Reset Value: 0000_H



Field	Bits	Type	Description
CR	[1:0]	rh	Current Result Upper part of right-aligned current result value Filter 0: n.a. Filter 1: bits [17:16] CR is cleared when writing SRFn.RSTF = 1.
AC	[10:8]	rh	Addition Count Indicates the number of remaining additions of filter input values before the next intermediate result register transfer occurs. AC is loaded with the value of FCRn.ADDL for a new addition sequence, also when writing SRFn.RSTF = 1.

Analog to Digital Converter

Field	Bits	Type	Description
MAVS	[13:12]	rh	Moving Average State Indicates the number of remaining intermediate register transfers before the next final result. MAVS = 0 indicates the end of a filter calculation operation. Since the filter calculation is executed very fast in comparison to a conversion, MAVS > 0 can be interpreted only as a kind of calculation busy flag. Therefore, it is recommended to read a valid filter result from register FRRn only when the corresponding interrupt request flag SRFn.IRQF is set. MAVS is reset when writing SRFn.RSTF = 1.
0	[7:2], 11, [15:14]	r	Reserved Read as 0. Should be written with 0.

The Intermediate Result Registers IRRyn store the intermediate results y of filter n.

IRRy0 (y = 1-3)

Filter 0 Intermediate Result Reg. y XSFR(284_H + 2*y)

Reset Value: 0000_H

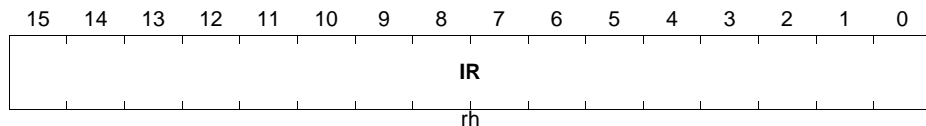
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0			IR												
r			rh												

Field	Bits	Type	Description
IR	[12:0]	rh	Intermediate Result Right-aligned intermediate result. IR is cleared when writing SRFn.RSTF = 1.
0	[15:13]	r	Reserved Read as 0. Should be written with 0.

IRR11L

Filter 1 Intermediate Result Reg. 1 Low XSFR(296_H)

Reset Value: 0000_H

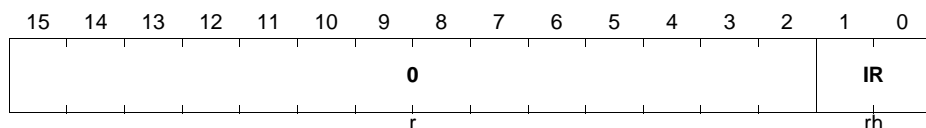


Field	Bits	Type	Description
IR	[15:0]	rh	Intermediate Result Low Right-aligned intermediate result value bits [15:0] (+ IRR11H.IR) IR is reset when writing SRFn.RSTF = 1.

IRR11H

Filter 1 Intermediate Result Reg. 1 High XSFR(298_H)

Reset Value: 0000_H



Field	Bits	Type	Description
IR	[1:0]	rh	Intermediate Result Upper part of right-aligned intermediate result value bits [17:16]. IR is reset when writing SRFn.RSTF = 1.
0	[15:2]	r	Reserved Read as 0. Should be written with 0.

Analog to Digital Converter

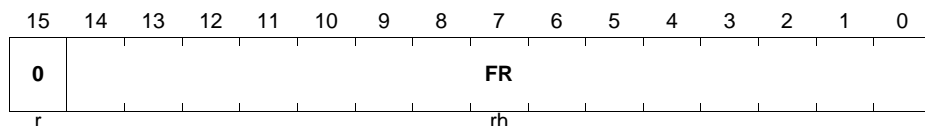
The Final Result Registers FRRn provide the final results of filter block n in Q15 format. FRR1 contains the lower 15 bits of the 20-bit final result.

FRR0

Filter 0 Final Result Register **XSFR(28C_H)** **Reset Value: 0000_H**

FRR1

Filter 1 Final Result Register **XSFR(29C_H)** **Reset Value: 0000_H**



Field	Bits	Type	Description
FR	[14:0]	rh	Intermediate Result Contains the final result for filter n in Q15 format. FRR0: complete 15-bit result of filter block 0 FRR1: the lower 15 bits of the 20-bit result of filter 1 FR is cleared when writing SRFn.RSTF = 1.
0	15	r	Reserved Read as 0. Should be written with 0.

Analog to Digital Converter

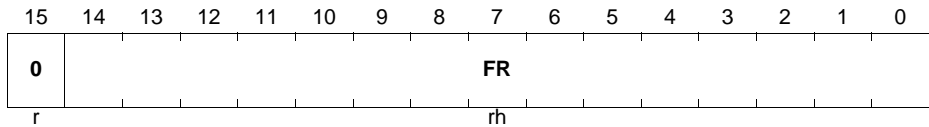
The Shifted Final Result Register SFRRn provides the upper 15 bits of the final 20-bit result of filter block 1 (shifted right by 5 bit positions). This supports 16-bit data operations for further treatment (Q15 format).

SFRR1

Filter 1 Shifted Final Result Register

XSFR(29A_H)

Reset Value: 0000_H



Field	Bits	Type	Description
FR	[14:0]	rh	Final Result Contains the upper 15 bits of the final 20-bit result of filter block 1. FR is cleared when writing SRFn.RSTF = 1.
0	15	r	Reserved returns 0 if read; should be written with 0;

17.9 Synchronization of Conversions

The conversions of an ADC kernel can be scheduled either self-timed according to the kernel's configuration or triggered by external (outside the ADC) signals:

Synchronized conversions support parallel conversion of 2 channels. This optimizes e.g. the control of electrical drives.

Equidistant sampling supports conversions in a fixed raster with minimum jitter. This optimizes e.g. filter algorithms or audio applications.

17.9.1 Synchronized Conversions for Parallel Sampling

The independent ADC kernels implemented in the XC27x8X can be synchronized for simultaneous measurements of analog input channels. While no parallel conversion is requested, the kernels can work independently.

The synchronization mechanism for parallel conversions ensures that the sample phases of the related channels start simultaneously. Different values for the resolution and the sample phase length of each kernel for a parallel conversion are supported.

A parallel conversion can be requested individually for each input channel (one or more). In the example shown in [Figure 17-24](#), input channels CH3 of the ADC kernels ADC0 and ADC1 are converted synchronously, whereas other input channels do not lead to parallel conversions.

One kernel operates as synchronization master, the other kernel operates as synchronization slave. Each kernel can play either role. Master and slave kernel form a "conversion group" to control parallel sampling:

- **The synchronization master** ADC kernel can request a synchronized conversion of a certain channel (SYNC = 1 in the corresponding channel control register), which is also requested in the connected slave ADC kernel.
Wait-for-read mode is supported for the master.
- **The synchronization slave** ADC kernel reacts to incoming synchronized conversion requests from the master. While no synchronized conversions are requested, the slave kernel can execute "local" conversions.
 - The slave timing must be configured according to the master timing (DIVA, DIVD, ARBRND in register [GLOBCTR](#)) to enable parallel conversions.
 - A parallel conversion request is always handled with highest priority and cancel-inject-repeat mode.
 - Wait-for-read mode is ignored in the slave. Previous results may be overwritten in particular, if the same result register is used by other conversions.
- The arbiter must run permanently (bit [GLOBCTR.ARB](#)M = 0) for the synchronization slave.
Initialize the slave before the master to have the arbiters run synchronously.
- Once started, a parallel conversion cannot be aborted.

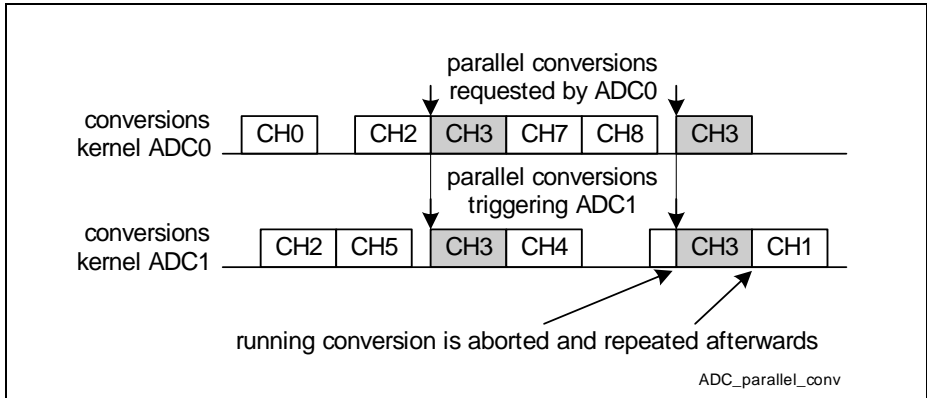


Figure 17-24 Parallel Conversions

The shown example uses synchronized conversions for channel CH3. The other channel conversions are controlled by their own kernels. ADC0 is the master, ADC1 is the slave. The synchronization master controls the slave by providing the control information **GLOBCTR.ANON** (see [Figure 17-25](#)) and the requested channel number. Bitfields **SYNCTR.STSEL** select the source of the ANON information, and must be configured accordingly for master (00_B) and slave (01_B).

The ready signals indicate when a kernel is ready to start the sample phase of a parallel conversion. Bit **SYNCTR.EVALR1** = 1 enables the control by the ready signal.

Note: Synchronized conversions request the same channel number, defined by the master. Using the alias feature (see [Section 17.7.3](#)), analog signals from different input channels can be converted. This is advantageous if e.g. CH0 is used as alternate reference.

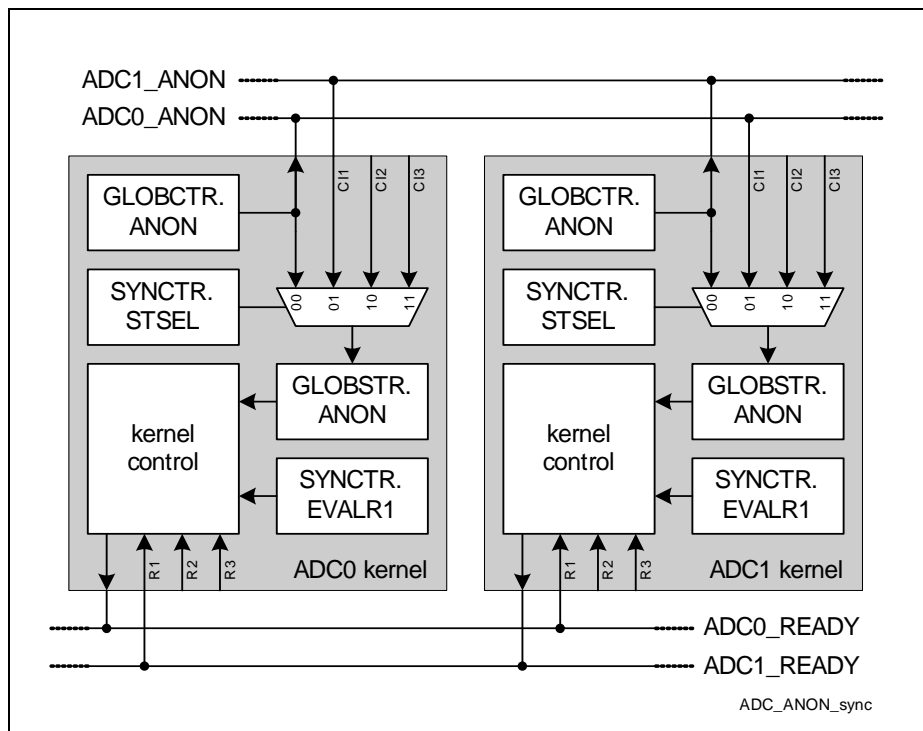


Figure 17-25 Synchronization via ANON and Ready Signals

Analog to Digital Converter

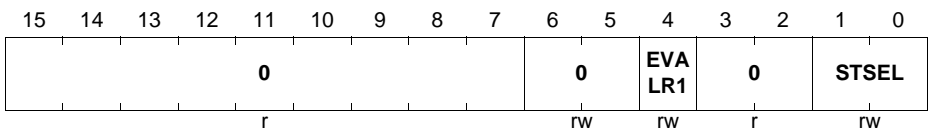
The Synchronization Control Register controls the synchronization of kernels for parallel conversions.

Note: Program register SYNCTR only while bitfield GLOBSTR.ANON = 00_B in all ADC kernels of the conversion group. Set the master's bitfield ANON to 11_B afterwards. It is recommended to avoid power saving modes (ANON = 01_B or 10_B) for parallel conversions.

SYNCTR

Synchronization Control Register XSFR(1A_H)

Reset Value: 0000_H



Field	Bits	Type	Description
STSEL	[1:0]	rw	Start Selection Controls the synchronization mechanism of the ADC kernel. 00 _B Kernel is synchronization master: Use own bitfield GLOBCTR.ANON 01 _B Kernel is synchronization slave: Use the control information at input C11 instead (see Figure 17-25). 10 _B Reserved, do not use (kernel is switched off) 11 _B Reserved, do not use (kernel is switched off)
EVALR1	4	rw	Evaluate Ready Input R1 Enables the ready input signal for a kernel of a conversion group. 0 _B No ready input control 1 _B Ready input R1 is considered for the start of a parallel conversion of this conversion group
0	[6:5]	r	Reserved for Future Use returns 0 if read; must be written with 0;
0	[3:2], [15:7]	r	Reserved returns 0 if read; should be written with 0;

17.9.2 Equidistant Sampling

To optimize the input data e.g. for filter or audio applications, conversions can be executed in a fixed timing raster. Conversions for equidistant sampling are triggered by an external signal (e.g. a timer). To generate the trigger signal synchronous to the arbiter, the ADC provides an output signal (ARBCNT) that is activated once per arbitration round and serves as timing base for the trigger timer. In this case, the arbiter must run permanently (GLOBCTR.ARB_M = 0). If the timer has an independent time base, the arbiter can be stopped while no requests are pending. The preface time must be longer than one arbitration round.

Select timer mode (RSIRx.TMEN = 1) for the intended source of equidistant conversions. In timer mode, a request of this source is triggered and arbitrated, but only started when the trigger signal is removed (see [Figure 17-26](#)) and the converter is idle.

To ensure that the converter is idle and the start of conversion can be controlled by the trigger signal, the equidistant conversion requests must receive highest priority. The preface time between request trigger and conversion start must be long enough for a currently active conversion to finish.

The frequency of signal REQTRx defines the sampling rate and its high time defines the preface time interval where the corresponding request source takes part in the arbitration.

Depending on the used request source, equidistant sampling is also supported for a sequence of channels. It is also possible to do equidistant sampling for more than one request source in parallel if the preface times and the equidistant conversions do not overlap.

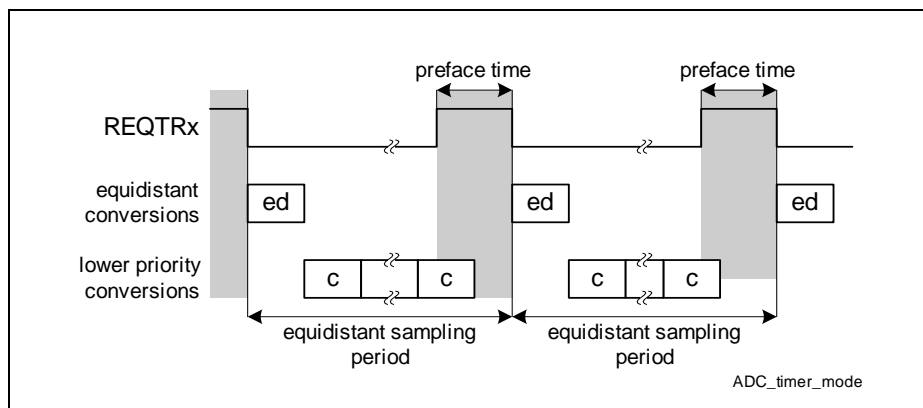


Figure 17-26 Timer Mode for Equidistant Sampling

17.10 Safety Features

Safety-aware applications must ensure that their analog signal inputs are safely connected to the respective signal sources. Two mechanisms are provided to check conversion results for plausibility:

- **Broken Wire Detection** pre-loads the capacitance of the converter to a selectable value. If the signal source is disconnected, the pre-load value will be converted instead of the source signal.
- **Multiplexer Test Mode** intermediately connects a pulldown device to an input channel. Conversions results can then be compared to result without pulldown.

17.10.1 Broken Wire Detection

To support self-test in safety-aware applications, the broken wire detection mechanism helps to check the connection of sensors or other voltage sources to the analog ADC inputs.

Broken wire detection can be individually enabled for each input channel CHx by setting bit ENx = 1 in register **BWDENR**. If enabled, a preparation phase is added before each conversion of an input channel, which pre-loads the capacitor field C_{AIN} to a selectable level before sampling and converting this channel.

For pre-loading an arbitrary channel can be selected (defined by **BWDCFG**.CHP). Broken wire detection preferably uses V_{AGND} and/or V_{AREF} , to use the maximum or the minimum voltage of the measurement range. These reference voltages can be selected via special channel numbers, see **"Analog Connections" on Page 17-121**.

Selecting the reference voltages by two channel numbers each provides compatibility with other products of the XC27x8X Derivatives.

The broken wire detection mechanism applies a voltage outside the expected result value range of the connected sensor. If the actual digital conversion result is located outside the expected measurement range (e.g. by using limit checking) with enabled broken wire detection, a defective connection has been detected. It is recommended to ensure enough margin between the voltage applied during the preparation phase and the sensors output range to minimize the effects of parasitics and leakage.

Note: The length of the complete analog to digital conversion is increased by the length of the preparation phase (same as the sample phase) if the broken wire detection is enabled. This influences the timing of conversion sequences.

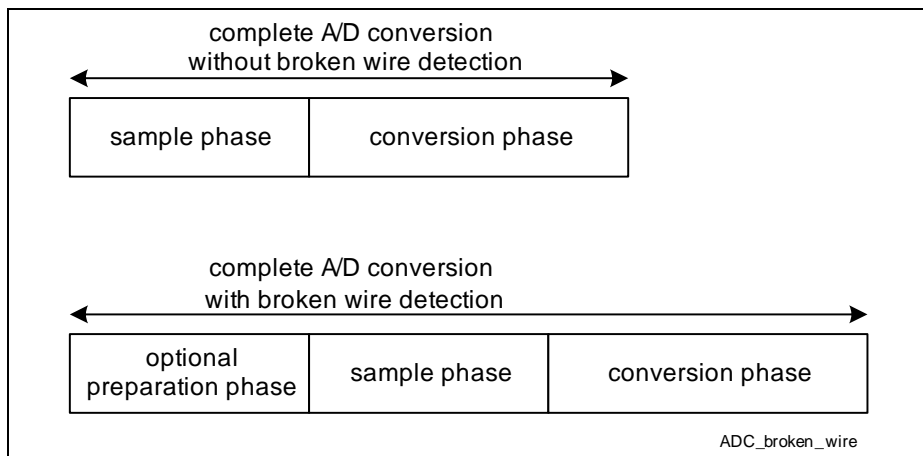


Figure 17-27 Broken Wire Detection

Analog to Digital Converter

The Broken Wire Detection Enable Register selects broken wire detection for channels CH15 ... CH0. The channel used for the preparation phase is selected in register **BWDCFGR**.

BWDENR

Broken Wire Detection Enable Reg. XSFR(C8_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	EN	EN	EN	EN	EN	EN	EN	EN	EN	EN	EN	EN	EN	EN	EN
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ENx (x = 0 - 15)	x	rw	Broken Wire Detection Enable for Channel CHx 0 _B Normal operation 1 _B Broken wire detection is enabled (pre-load)

Note: Not all channels are available in all products.

Therefore, only the BWD enable bits with corresponding channels are valid.

The Broken Wire Detection Configuration Register selects a channel for the additional preparation phase.

The channels for which broken wire detection is active, are selected via register **BWDENR**.

BWDCFGR

Broken Wire Detection Configuration Register

XSFR(CA_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0											CHP				
r											rw				

Field	Bits	Type	Description
CHP	[4:0]	rw	Channel Number for Preparation Phase Defines the channel to be used for the preparation phase for the broken wire detection.
0	[15:5]	r	Reserved returns 0 if read; should be written with 0;

Analog to Digital Converter

Note: Channels CH16 and CH24 both select the analog reference ground V_{AGND} , channels CH17 and CH25 both select the analog reference voltage V_{AREF} . This provides compatibility with other products of the XC27x8X Derivatives.

17.10.2 Multiplexer Test Mode

Multiplexer test mode is a specific test mode that can be enabled during run time to check the connection to the respective sensor. This is done by connecting a static load R_{MTM} to the selected input channel. The resulting voltage divider reduces the measured voltage by placing an additional load on that channel.

The test result to be expected results from the source impedance and previous result data without pulldown.

Multiplexer test mode for channel 7 is enabled by setting bit MTM7 in register **EMENR**.

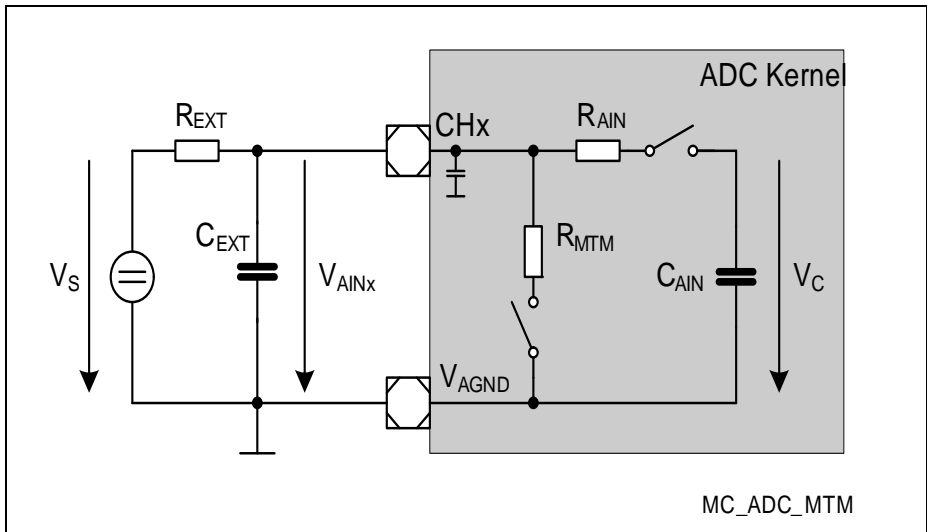


Figure 17-28 Multiplexer Test Mode

17.11 External Multiplexer Control

If an application requires more analog inputs channels than available on the XC27x8X, external analog multiplexers can be added to extend the number of analog channels. The three output signals EMUX[2:0] can control 1-out-of-8 external multiplexers.

Registers **EMCTR** and **EMENR** configure the control behavior of the external multiplexers. Bitfield EMUX selects the actual external channel. This selection can either be controlled by software (write to bitfield SETEMUX, applied with next conversion start) or automatically by the scan function.

The external multiplexer support can be enabled for each available input channel and supports several modes (selected in register **EMENR**):

- **Software control** without any HW control (EMUXEN = 0):
 Automatic control of the external multiplexer is disabled, bitfield EMUX is always updated by write actions to bitfield SETEMUX. Bitfield EMSAMPLE has no effect on the sample time.
- **Hardware control without scan** (EMUXEN = 1, SCANEN = 0):
 Bitfield EMUX is updated from bitfield SETEMUX with each conversion start of the channel selected by EMUXCHNR. Bitfield EMSAMPLE controls the sample time for the first conversion with a new EMUX value.
- **Hardware control with scan** (EMUXEN = 1, SCANEN = 1):
 Bitfield EMUX is updated after each conversion of the channel selected by EMUXCHNR. If EMUX = 0 it is reloaded from bitfield SETEMUX, otherwise it is decremented by 1. Bitfield EMSAMPLE controls the sample time for each conversion of the selected channel. Two multiplexer control schemes can be selected:
 - **Single-input scan** (TROEN = 0):
 An autoscan sequence converting the channel selected by EMUXCHNR leads to one conversion of the multiplexed channel (trigger option disabled). Bitfield EMUX is update for each completed auto scan sequence.
 The scan sequence in the example (**Figure 17-29**, assuming SETEMUX = 010_B) is:
 4-32-2-1-0--4-31-2-1-0--4-30-2-1-0--4-32-2-1-0--...
 - **Multi-input scan** (TROEN = 1):
 When the channel selected by EMUXCHNR is converted, a new conversion request is triggered as long as bitfield EMUX > 0. In a scan request source, this sets the corresponding pending bit. In a queued request source, this sets the valid bit of the backup stage.
 All inputs of the external multiplexer are scanned during a single autoscan sequence, beginning with the channel selected by bitfield SETEMUX.
 The scan sequence in the example (**Figure 17-29**, assuming SETEMUX = 010_B) is:
 4-32-31-30-2-1-0--4-32-31-30-2-1-0--...

Note: It is recommended to write the start value of the first scan sequence to SETEMUX while EMUXEN = 0.

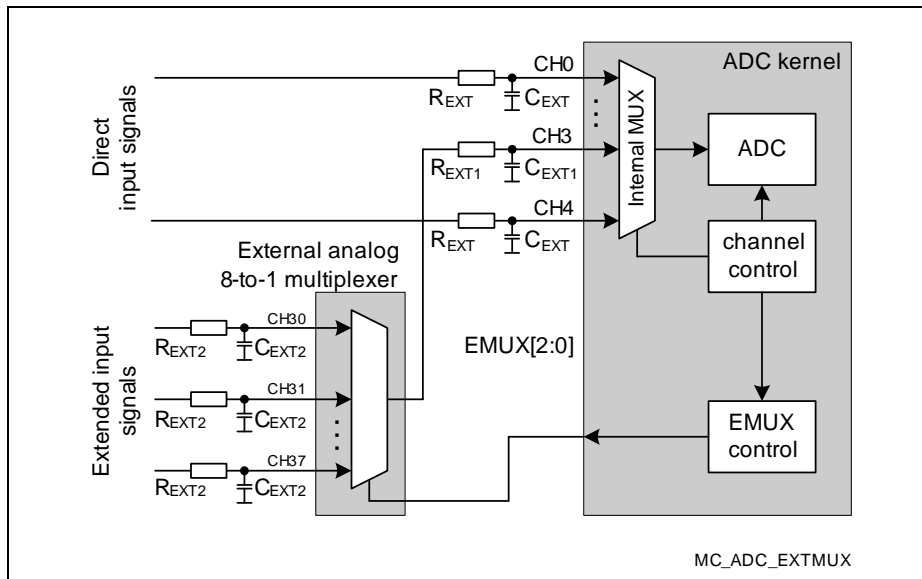


Figure 17-29 External Analog Multiplexer Example

In the shown example, an external multiplexer is connected to channel CH3 (the additional analog inputs are designated CH30 ... CH37).

Many applications will use buffer capacitors or even RC filters on the analog inputs. If an external multiplexer is used, local filters are likely to be placed at its inputs ($R_{EXT2} \cdot C_{EXT2}$ on CH3x in [Figure 17-29](#)). For applications where the external multiplexer is located far from the ADC analog input, it is recommended to add an RC filter directly at the analog input of the ADC ($R_{EXT1} \cdot C_{EXT1}$ on CH3 in [Figure 17-29](#)).

Note: Each RC filter limits the bandwidth of the analog input signal.

The RC filters used with an external multiplexer change the impedance for the corresponding analog input channel, compared to other channels. This can be compensated by using another input class selecting a longer sample phase. The sample phase must be long enough to let the input signal settle.

When the external multiplexer switches (EMUX[2:0] changes), the required sample time to let the input settle is even longer. This is automatically compensated by applying the alternative sample phase length (selected by bitfield [EMCTR.EMSAMPLE](#)) instead of the one given by the input class for the first conversion after EMUX[2:0] has changed. If

Analog to Digital Converter

this first conversion is aborted due to a higher priority request, the repeated conversion also uses the value of EMSAMPLE.

The External Multiplexer Enable Register defines which analog input channel is used to control the settings of an external analog multiplexer and defines its operating mode. It also contains bit MTM7 to control the multiplexer test mode for CH7.

EMENR

External Multiplexer Enable Register

XSFR(D6_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MTM7				0				EMUXEN	SCANEN	TROEN			EMUXCHNR		
rw				r				rw	rw	rw			rw		

Field	Bits	Type	Description
EMUXCHNR	[4:0]	rw	Channel Number for External Multiplexer Selects the input channel for which an external multiplexer shall be controlled (if enabled, i.e. EMUXEN = 1). <i>Note: Not all channels are available in all products.</i>
TROEN	5	rw	Trigger Option Enable Selects the scan mode behavior of the external multiplexer (if enabled). 0 _B Single-input scan: convert one external channel per scan sequence 1 _B Multi-input scan: convert a series of external channels per scan sequence
SCANEN	6	rw	Scan Enable Enables the automatic handling of the external multiplexer during scan sequences. 0 _B Hardware control without scan 1 _B Hardware control with scan: bitfield EMUX is automatically modified during scan sequences

Field	Bits	Type	Description
EMUXEN	7	rw	External Multiplexer Control Enable Enables the automatic control of the external multiplexer. 0_B Software control: an external multiplexer is controlled by software only 1_B Hardware control: the external multiplexer is automatically controlled by the ADC's hardware
MTM7	15	rw	Multiplexer Test Mode CH7 Enables the multiplexer test mode for input CH7 0_B No multiplexer test mode 1_B Multiplexer test mode is enabled
0	[14:8]	r	Reserved Read as 0; should be written with 0.

The External Multiplexer Control Register controls an external analog multiplexer and defines the alternative sample phase length for external conversions.

EMCTR

External Multiplexer Control Register

XSFR(D0_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EMSAMPLE								0	EMUX			0	SETEMUX		
rw								r	rh			r	rw		

Field	Bits	Type	Description
SETEMUX	[2:0]	rw	Setting of External Multiplexer Defines the update value for bitfield EMUX. The update options depend on the selected operating mode.
EMUX	[6:4]	rh	Current Setting for External Multiplexer Selects an input on the external multiplexer via outputs EMUX[2:0]. Bitfield EMUX is updated from bitfield SETEMUX. The update options depend on the selected operating mode.

Field	Bits	Type	Description
EMSAMPLE	[15:8]	rw	External Multiplexer Sampling Time Defines the alternative sample phase length for external multiplexer control. This value replaces the standard sample time configuration (STC in register INPCR _x , Page 17-56) for conversions where the external multiplexer setting has changed.
0	3, 7	r	Reserved returns 0 if read; should be written with 0;

17.12 Interrupt Request Handling

Interrupts can be generated by several types of events. The ADC kernel provides 4 independent service request output signals (ADCx_SR[3:0]) connected to interrupt nodes. Three types of events can generate interrupt requests:

- **Request source events:** indicate that a request source completed the requested conversion sequence. For a scan source, the event is generated when the complete defined set of channels has been arbitrated. For a sequential source, the user can define where inside a conversion sequence a request source event is generated. Request source events indicate that a conversion sequence has reached a defined state and software can access the related set of results.
- **Channel events:** indicate that a conversion is finished. Optionally, channel events can be generated only for conversion result within a programmable value range. Channel events preferably indicate analog input values inside or outside a nominal operating range. This offloads the CPU load from background tasks, i.e. an interrupt is only required if the specified conversion result range is met or exceeded.
- **Result events:** indicate a new valid result in a result register. Usually, this triggers a read action by the CPU (or PEC). Optionally, result events can be generated only at a reduced rate if data reduction or enhanced filtering is active. Using a result FIFO increases the tolerable CPU (PEC) interrupt latency for retrieving the result data. For example, a single PEC channel can read the results for a complete auto-scan sequence, if all channels of the sequence target the same result register and the transfers are triggered by result events.

Each ADC event is indicated by a dedicated flag that can be cleared by software. If an interrupt is enabled for a certain event, the interrupt is generated for each event, independent of the status of the corresponding event indication flag. This ensures efficient PEC handling of ADC events (the ADC event can generate an interrupt without the need to clear the indication flag).

Node pointers assign each events to one of the 4 service request output signals SRx. Depending on the relevance of the event for the application, ADC events can be grouped to the service requests. Less important events can share an interrupt node, more important events can be assigned to a dedicated interrupt node.

Note: A conversion can lead to three interrupts, one of each type, if all are enabled.

In this case, the ADC module first triggers the request source event interrupt, then the channel event interrupt, followed by the result event interrupt (all within a few f_{ADC} clock cycles).

Request source events and result events are both handled with a set of event indication registers. Channel events are handled by a separate set of channel event registers.

Analog to Digital Converter

The Event Indication Flag Register EVINFR monitors both the detected request source events (flags EVINF0 - EVINF2) and the result events (flags EVINF8 - EVINF15).

EVINFR

Event Indication Flag Register XSFR(A0_H) Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EVIN F15	EVIN F14	EVIN F13	EVIN F12	EVIN F11	EVIN F10	EVIN F9	EVIN F8			0			EVIN F2	EVIN F1	EVIN F0
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh			r			rwh	rwh	rwh

Field	Bits	Type	Description
EVINF_x (x = 0 - 2)	x	rwh	Event Indication Flag for Request Source x Indicates a request source event from source x. 0 _B No source request event 1 _B Source x has generate a request source event
EVINF_x (x = 8 - 15)	x	rwh	Event Indication Flag for Result Register x - 8 Indicates a result event from result register x-8. 0 _B No result event 1 _B Result register x-8 has generated a result event
0	[7:3]	r	Reserved returns 0 if read; should be written with 0;

Note: Writing 1 to a bit of this register sets the corresponding bit and generates the associated interrupt request. Writing a 0 has no effect.

*Bits of register EVINFR can be cleared by writing to the corresponding bits of register **EVINCR**.*

Analog to Digital Converter

Writing a 1 to a bit position in the Event Indication Clear Register EVINCR clears the corresponding event indication flag EVIN_{Fx} in register **EVINFR**. If a request source or result event is detected when the corresponding bit position is written with a 1, flag EVIN_{Fx} is cleared.

EVINCR

Event Indication Clear Register XSFR(A2_H) Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EVIN C15	EVIN C14	EVIN C13	EVIN C12	EVIN C11	EVIN C10	EVIN C9	EVIN C8			0			EVIN GF2	EVIN GF1	EVIN GF0
w	w	w	w	w	w	w	w			r			rwh	rwh	rwh

Field	Bits	Type	Description
EVINGF_x (x = 0 - 2)	x	rwh	Event Indication Gated Flag for Request Src. x Read access: 0 _B No source event interrupt request 1 _B A service request output has been activated due to an event of request source x. <i>Note: Advantageous to indicate the last conversion of queued sequence.</i> Write access: 0 _B No action 1 _B Bits EVIN _{Fx} and EVINGF _x are cleared
EVINC_x (x = 8 - 15)	x	w	Clear Event Indication Flag for Result Reg. x-8 0 _B No action 1 _B Bit EVIN _{Fx} is cleared
0	[7:3]	r	Reserved returns 0 if read; should be written with 0;

Analog to Digital Converter

The Channel Event Indication Flag Register CHINFR monitors the detected channel events for channels 0 ... 15 .

CHINFR

Channel Event Indication Flag RegisterXSFR(90_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHIN F15	CHIN F14	CHIN F13	CHIN F12	CHIN F11	CHIN F10	CHIN F9	CHIN F8	CHIN F7	CHIN F6	CHIN F5	CHIN F4	CHIN F3	CHIN F2	CHIN F1	CHIN F0
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
CHINFR_x (x = 0 - 15)	x	rwh	Channel x Event Indication Flag Indicates a channel event for channel x. 0 _B No channel event 1 _B Channel x has generated a channel event

Note: Writing 1 to a bit of this register sets the corresponding bit and generates the associated interrupt request. Writing a 0 has no effect.

*Bits of register CHINFR can be cleared by writing to the corresponding bits of register **CHINCR**.*

Analog to Digital Converter

Writing a 1 to a bit position in the channel indication clear register CHINCR clears the corresponding channel event indication flag CHINFRx in register **CHINFR**. If a channel event is detected when the corresponding bit position is written with a 1, flag CHINFRx is cleared.

CHINCR

Channel Event Indication Clear Register

XSFR(92_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHIN C15	CHIN C14	CHIN C13	CHIN C12	CHIN C11	CHIN C10	CHIN C9	CHIN C8	CHIN C7	CHIN C6	CHIN C5	CHIN C4	CHIN C3	CHIN C2	CHIN C1	CHIN C0
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Field	Bits	Type	Description
CHINCRx (x = 0 - 15)	x	w	Clear Channel Indication Flag 0 _B No action 1 _B Flag CHINFR.x is cleared

Note: Not all channels are available in all products.

Therefore, only the indication flags and clear bits with corresponding channels are valid.

Analog to Digital Converter

Interrupt node pointers assign an event to one of the 4 service requests of an ADC kernel. The grouping of events for a certain service request can, therefore, be configured according to the requirements of a given application.

The Event Interrupt Node Pointer Register 0 assigns the request source events to a service request output SR[3:0].

EVINPRO

Event Interrupt Node Pointer Register 0

XSFR(A8_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0						EVINP2		0		EVINP1		0		EVINP0	
r						rw		r		rw		r		rw	

Field	Bits	Type	Description
EVINP0, EVINP1, EVINP2	[1:0], [5:4], [9:8]	rw	Interrupt Node Pointer for Request Source x Selects a service request output for an event of request source x. 00 _B Assign to output SR0 ... 11 _B Assign to output SR3
0	[3:2], [7:6], [15:10]	r	Reserved returns 0 if read; should be written with 0;

Analog to Digital Converter

The Event Interrupt Node Pointer Registers 8 and 12 assign the result events to a service request output SR[3:0].

EVINPR8

Event Interrupt Node Pointer Register 8

XSFR(AC_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	EVINP11	0	EVINP10	0	EVINP9	0	EVINP8	0	EVINP7	0	EVINP6	0	EVINP5	0	EVINP4
r	rw	r	rw	r	rw	r	rw	r	rw	r	rw	r	rw	r	rw

Field	Bits	Type	Description
EVINP8, EVINP9, EVINP10, EVINP11	[1:0], [5:4], [9:8], [13:12]	rw	Interrupt Node Pointer for Result Event x-8 Selects a service request output for an event of request register x-8. 00 _B Assign to output SR0 ... 11 _B Assign to output SR3
0	[3:2], [7:6], [11:10], [15:14]	r	Reserved returns 0 if read; should be written with 0;

EVINPR12

Event Interrupt Node Pointer Register 12

XSFR(AE_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	EVINP15	0	EVINP14	0	EVINP13	0	EVINP12	0	EVINP11	0	EVINP10	0	EVINP9	0	EVINP8
r	rw	r	rw	r	rw	r	rw	r	rw	r	rw	r	rw	r	rw

Field	Bits	Type	Description
EVINP12, EVINP13, EVINP14, EVINP15	[1:0], [5:4], [9:8], [13:12]	rw	Interrupt Node Pointer for Result Event x-8 Selects a service request output for an event of request register x-8. 00 _B Assign to output SR0 ... 11 _B Assign to output SR3
0	[3:2], [7:6], [11:10], [15:14]	r	Reserved returns 0 if read; should be written with 0;

Analog to Digital Converter

The Channel Interrupt Node Pointer Registers assign each channel event to a service request output SR[3:0].

CHINPR0

Channel Intr. Node Pointer Reg. 0 XSFR(98_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	CHINP3	0	CHINP2	0	CHINP1	0	CHINP0	0	CHINP3	0	CHINP2	0	CHINP1	0	CHINP0
r	rw	r	rw	r	rw	r	rw	r	rw	r	rw	r	rw	r	rw

Field	Bits	Type	Description
CHINP0, CHINP1, CHINP2, CHINP3	[1:0], [5:4], [9:8], [13:12]	rw	Interrupt Node Pointer for Channel x Selects a service request output for a channel event from channel x. 00 _B Assign to output SR0 ... 11 _B Assign to output SR3
0	[3:2], [7:6], [11:10], [15:14]	r	Reserved returns 0 if read; should be written with 0;

CHINPR4

Channel Intr. Node Pointer Reg. 4 XSFR(9A_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	CHINP7	0	CHINP6	0	CHINP5	0	CHINP4	0	CHINP3	0	CHINP2	0	CHINP1	0	CHINP0
r	rw	r	rw	r	rw	r	rw	r	rw	r	rw	r	rw	r	rw

Field	Bits	Type	Description
CHINP4, CHINP5, CHINP6, CHINP7	[1:0], [5:4], [9:8], [13:12]	rw	Interrupt Node Pointer for Channel x Selects a service request output for a channel event from channel x. 00 _B Assign to output SR0 ... 11 _B Assign to output SR3

Field	Bits	Type	Description
0	[3:2], [7:6], [11:10], [15:14]	r	Reserved returns 0 if read; should be written with 0;

CHINPR8

Channel Intr. Node Pointer Reg. 8 XSFR(9C_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	CHINP11	0	CHINP10	0	CHINP9	0	CHINP8	0	CHINP7	0	CHINP6	0	CHINP5	0	CHINP4
r	rw	r	rw	r	rw	r	rw	r	rw	r	rw	r	rw	r	rw

Field	Bits	Type	Description
CHINP8, CHINP9, CHINP10, CHINP11	[1:0], [5:4], [9:8], [13:12]	rw	Interrupt Node Pointer for Channel x Selects a service request output for a channel event from channel x. 00 _B Assign to output SR0 ... 11 _B Assign to output SR3
0	[3:2], [7:6], [11:10], [15:14]	r	Reserved returns 0 if read; should be written with 0;

CHINPR12

Channel Interrupt Node Pointer Register 12

XSFR(9E_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	CHINP15	0	CHINP14	0	CHINP13	0	CHINP12	0	CHINP11	0	CHINP10	0	CHINP9	0	CHINP8
r	rw	r	rw	r	rw	r	rw	r	rw	r	rw	r	rw	r	rw

Field	Bits	Type	Description
CHINP12, CHINP13, CHINP14, CHINP15	[1:0], [5:4], [9:8], [13:12]	rw	Interrupt Node Pointer for Channel x Selects a service request output for a channel event from channel x. 00 _B Assign to output SR0 ... 11 _B Assign to output SR3
0	[3:2], [7:6], [11:10], [15:14]	r	Reserved returns 0 if read; should be written with 0;

Note: Not all channels are available in all products.

Therefore, only the node pointers with corresponding channels are valid.

17.13 Implementation

This section describes the implementation of the ADC kernels in the XC27x8X device.

- [“Address Map” on Page 17-117](#)
- [“Interrupt Control Registers” on Page 17-120](#)
- [“Analog Connections” on Page 17-121](#)
- [“Digital Connections” on Page 17-124](#)

17.13.1 Address Map

The ADC register locations are indicated as offset values in the register descriptions. The exact register address is given by the offset of the register (given in [Table 17-7](#)) plus the kernel base address (given in [Table 17-6](#)) of the module.

Table 17-6 Registers Address Space

Module	Base Address	End Address	Note
ADC0	E000 _H	E0FF _H	
ADC1	E100 _H	E1FF _H	

Table 17-7 ADC Module Register Summary

Short Name	Description	Offset ¹⁾	See Page
General Registers			
ID	Module Identification Register	08 _H	Page 17-15
KSCFG ²⁾	Kernel State Configuration Register	0C _H	Page 17-13
GLOBCTR	Global Control Register	10 _H	Page 17-17
GLOBCFG	Global Configuration Register	DE _H	Page 17-18
GLOBSTR	Global Status Register	12 _H	Page 17-20
RSIR0	Request Source 0 Input Select Register	00 _H	Page 17-45
RSIR1	Request Source 1 Input Select Register	02 _H	Page 17-45
RSIR2	Request Source 2 Input Select Register	04 _H	Page 17-45
Arbiter Registers			
ASENR	Arbitration Slot Enable Register	18 _H	Page 17-49
RSPR0	Request Source Priority Register 0	14 _H	Page 17-50
Channel-Related Registers			
CHCTR0-15	Channel Control Register 0-15	20 _H -3E _H	Page 17-54

Table 17-7 ADC Module Register Summary (cont'd)

Short Name	Description	Offset¹⁾	See Page
INPCR0	Input Class Register 0	C0 _H	Page 17-56
INPCR1	Input Class Register 1	C2 _H	Page 17-56
LCBR0	Limit Checking Boundary Register 0	84 _H	Page 17-59
LCBR1	Limit Checking Boundary Register 1	86 _H	Page 17-59
LCBR2	Limit Checking Boundary Register 2	88 _H	Page 17-59
LCBR3	Limit Checking Boundary Register 3	8A _H	Page 17-59
CHINFR	Channel Event Indication Flag Register	90 _H	Page 17-109
CHINCR	Channel Event Indication Clear Register	92 _H	Page 17-110
CHINPR0	Channel Interrupt Node Pointer Register 0	98 _H	Page 17-114
CHINPR4	Channel Interrupt Node Pointer Register 4	9A _H	Page 17-114
CHINPR8	Channel Interrupt Node Pointer Register 8	9C _H	Page 17-115
CHINPR12	Channel Interrupt Node Pointer Register 12	9E _H	Page 17-115
ALR0	Alias Register 0	1C _H	Page 17-61

Result Registers

RESR0-7	Result Register 0-7, normal view	40 _H -4E _H	Page 17-66
RESRA0-7	Result Register 0-7, view A	50 _H -5E _H	Page 17-67
RESRV0-7	Result Register 0-7, view V	60 _H -6E _H	Page 17-66
RESRAV0-7	Result Register 0-7, view AV	70 _H -7E _H	Page 17-67
VFR	Valid Flag Register	80 _H	Page 17-71
RSSR	Result Status Shadow Register	82 _H	Page 17-68
RCR0-7	Result Control Register 0-7	B0 _H -BE _H	Page 17-69
EVINFR	Event Indication Flag Register	A0 _H	Page 17-107
EVINCR	Event Indication Clear Register	A2 _H	Page 17-108
EVINPR0	Event Interrupt Node Pointer Register 0	A8 _H	Page 17-111
EVINPR8	Event Interrupt Node Pointer Register 8	AC _H	Page 17-112
EVINPR12	Event Interrupt Node Pointer Reg. 12	AE _H	Page 17-112

Request Source 0 Registers

QMR0	Queue 0 Mode Register	E0 _H	Page 17-38
QSR0	Queue 0 Status Register	E2 _H	Page 17-40
QOR0	Queue 0 Register 0	E4 _H	Page 17-43

Table 17-7 ADC Module Register Summary (cont'd)

Short Name	Description	Offset ¹⁾	See Page
QBUR0	Queue 0 Backup Register	E6 _H	Page 17-44
QINR0	Queue 0 Input Register	shared	Page 17-42

Request Source 1 Registers

CRCR1	Conversion Request 1 Control Register	E8 _H	Page 17-31
CRPR1	Conversion Request 1 Pending Register	EA _H	Page 17-32
CRMR1	Conversion Request 1 Mode Register	EC _H	Page 17-29

Request Source 2 Registers

QMR2	Queue 2 Mode Register	F0 _H	Page 17-38
QSR2	Queue 2 Status Register	F2 _H	Page 17-40
Q0R2	Queue 2 Register 0	F4 _H	Page 17-43
QBUR2	Queue 2 Backup Register	F6 _H	Page 17-44
QINR2	Queue 2 Input Register	shared	Page 17-42

Additional Feature Registers

SYNCTR	Synchronization Control Register	1A _H	Page 17-93
EMENR	External Multiplexer Enable Register	D6 _H	Page 17-103
EMCTR	External Multiplexer Control Register	D0 _H	Page 17-104
BWDENR	Broken Wire Detection Enable Register	C8 _H	Page 17-98
BWDCFGR	Broken Wire Detection Configuration Register	CA _H	Page 17-98

Enhanced Filter Registers

FCR0	Functional Control Register Filter 0	280 _H	Page 17-82
SRF0	Status Register Filter 0	28E _H	Page 17-84
CRRLO	Current Result Register Low Filter 0	282 _H	Page 17-85
CRRHO	Current Result Register High Filter 0	284 _H	Page 17-85
IRR10	Intermediate Result Register 1 Filter 0	286 _H	Page 17-86
IRR20	Intermediate Result Register 2 Filter 0	288 _H	Page 17-86
IRR30	Intermediate Result Register 3 Filter 0	28A _H	Page 17-86
FRR0	Final Result Register Filter 0	28C _H	Page 17-88
FCR1	Functional Control Register Filter 1	290 _H	Page 17-82
SRF1	Status Register Filter 1	29E _H	Page 17-84
CRR11	Current Result Register Low Filter 1	292 _H	Page 17-85

Table 17-7 ADC Module Register Summary (cont'd)

Short Name	Description	Offset ¹⁾	See Page
CRRH1	Current Result Register High Filter 1	294 _H	Page 17-85
IRR11L	Intermediate Result Register 1 Filter 1 Low	296 _H	Page 17-87
IRR11H	Intermediate Result Register 1 Filter 1 High	298 _H	Page 17-87
FRR1	Final Result Register Filter 1	29C _H	Page 17-88
SFRR1	Shifted Final Result Register Filter 1	29A _H	Page 17-89

1) Short 8-bit addresses are not available for kernel registers of this module.

2) Register KSCFG is available only in the address range of ADC0, named ADC0_KSCFG.

Note: Register bits marked "w" always deliver 0 when read.

The offsets 06_H, 16_H, C4_H, C6_H, 8C_H, 8E_H, A4_H, A6_H, and AA_H are reserved for future use and must not be accessed.

17.13.2 Interrupt Control Registers

The interrupt control registers are located in the SFR area. They are described in the general interrupt chapter.

Table 17-8 ADC Interrupt Control Registers

Short Name	Description
ADC_0IC	Interrupt Control Register for SR0 of ADC0
ADC_1IC	Interrupt Control Register for SR1 of ADC0
ADC_2IC	Interrupt Control Register for SR2 of ADC0
ADC_3IC	Interrupt Control Register for SR3 of ADC0
ADC_4IC	Interrupt Control Register for SR0 of ADC1
ADC_5IC	Interrupt Control Register for SR1 of ADC1
ADC_6IC	Interrupt Control Register for SR2 of ADC1
ADC_7IC	Interrupt Control Register for SR3 of ADC1

Note: Various events can be assigned to one on these interrupt nodes. Please refer to ["Interrupt Request Handling" on Page 17-106](#)

17.13.3 Analog Connections

The analog input multiplexer selects the input channel to be converted from the signals available in this product.

The exact number of analog input channels and the available connection to port pins depend on the employed product type. A summary of channels enclosing all versions of the XC27x8X can be found in [Table 17-9](#) and [Table 17-10](#). For the exact number and association, please refer to the corresponding Data Sheet(s).

In addition to real input channels, also the reference voltages can be selected via on-chip connections. This is mainly used for broken wire detection ([Section 17.10.1](#)).

Each ADC kernel has its own reference input lines V_{AGND} and V_{AREF} . Depending on the package, these input lines can be available as independent pins for high pin count packages or can be combined for low pin count packages.

The respective voltage supply lines of both converters are connected together.

Table 17-9 ADC0 Analog Connections in XC27x8X

Signal	from/to Module	I/O to ADC0	Can be used to/as, connected to
Power supply and standard reference			
V_{DDPA}	see pinning chapter	I	analog power supply
V_{SS}		I	analog power supply
V_{AREF0}		I	positive analog reference
V_{AGND}		I	negative analog reference
Analog input channels			
CH0	P5.0	I	analog input channel 0
CH1	P5.1	I	analog input channel 1
CH2	P5.2	I	analog input channel 2
CH3	P5.3	I	analog input channel 3
CH4	P5.4	I	analog input channel 4
CH5	P5.5	I	analog input channel 5
CH6	P5.6	I	analog input channel 6
CH7	P5.7	I	analog input channel 7
CH8	P5.8	I	analog input channel 8 overlaid with ADC1 channel 8
CH9	P5.9	I	analog input channel 9 overlaid with ADC1 channel 9

Analog to Digital Converter

Table 17-9 ADC0 Analog Connections in XC27x8X (cont'd)

Signal	from/to Module	I/O to ADC0	Can be used to/as, connected to
CH10	P5.10	I	analog input channel 10 overlaid with ADC1 channel 10
CH11	P5.11	I	analog input channel 11 overlaid with ADC1 channel 11
CH12	P5.12	I	analog input channel 12
CH13	P5.13	I	analog input channel 13
CH14	P5.14	I	analog input channel 14
CH15	P5.15	I	analog input channel 15
CH16	V _{AGND}	I	analog input channel 16 (internal conn. to V _{AGND})
CH17	V _{AREF}	I	analog input channel 17 (internal conn. to V _{AREF})
CH24	V _{AGND}	I	analog input channel 24 (internal conn. to V _{AGND})
CH25	V _{AREF}	I	analog input channel 25 (internal conn. to V _{AREF})
Other channels	n.c.	I	not available, do not request for conversion

Table 17-10 ADC1 Analog Connections in XC27x8X

Signal	from/to Module	I/O to ADC1	Can be used to/as, connected to
--------	----------------	-------------	---------------------------------

Power supply and standard reference

V _{DDPA}	see pinning chapter	I	analog power supply
V _{SS}		I	
V _{AREF1}		I	positive analog reference
V _{AGND}		I	negative analog reference

Analog input channels

CH0	P15.0	I	analog input channel 0
CH1	P15.1	I	analog input channel 1
CH2	P15.2	I	analog input channel 2
CH3	P15.3	I	analog input channel 3
CH4	P15.4	I	analog input channel 4
CH5	P15.5	I	analog input channel 5

Table 17-10 ADC1 Analog Connections in XC27x8X (cont'd)

Signal	from/to Module	I/O to ADC1	Can be used to/as, connected to
CH6	P15.6	I	analog input channel 6
CH7	P15.7	I	analog input channel 7
CH8	P5.8	I	analog input channel 8 (overlaid with ADC0_CH8)
CH9	P5.9	I	analog input channel 9 (overlaid with ADC0_CH9)
CH10	P5.10	I	analog input channel 10 (overlaid with ADC0_CH10)
CH11	P5.11	I	analog input channel 11 (overlaid with ADC0_CH11)
CH12		I(O)	analog input channel 12
CH13		I(O)	analog input channel 13
CH14		I(O)	analog input channel 14
CH15		I(O)	analog input channel 15
CH16	V_{AGND}	I	analog input channel 16 (internal conn. to V_{AGND})
CH17	V_{AREF}	I	analog input channel 17 (internal conn. to V_{AREF})
CH24	V_{AGND}	I	analog input channel 24 (internal conn. to V_{AGND})
CH25	V_{AREF}	I	analog input channel 25 (internal conn. to V_{AREF})
Other channels	n.c.	I	not available, do not request for conversion

17.13.4 Digital Connections

The following table shows the digital connections of the ADC kernels with other modules or pins in the XC27x8X device.

The following sections refer to the inter-module connections, whereas the connections of the service request outputs SR[3:0] of each kernel to the interrupt control registers is given in [Section 17.13.2](#).

Note: The functional inputs of the ADC that are marked "I(s)" are additionally synchronized to f_{SYS} before they can affect the module internal logic. The resulting delay of $2/f_{SYS}$ and an uncertainty of $1/f_{SYS}$ have to be taken into account for precise timing calculation. An edge of an input signal can only be correctly detected if the high phase and the low phase of the input signal are both longer than $1/f_{SYS}$.

The functional inputs of the ADC that are marked "I" are already considered as synchronous to f_{SYS} .

Table 17-11 ADC0 Digital Connections in XC27x8X

Signal	from/to Module	I/O to ADC0	Can be used to/as, connected to
Arbiter Timing			
ARBCNT	CCU60_T12HRE, CCU60_T13HRE, CCU61_T12HRE, CCU61_T13HRE	O	time base for equidistant sampling for CCU60, CCU61
External multiplexer control			
EMUX[0]	P6.0	O	control of external analog multiplexer(s)
EMUX[1]	P6.1	O	control of external analog multiplexer(s)
EMUX[2]	P6.2	O	control of external analog multiplexer(s)
Request Source 0			
REQGT0A	CCU60_COUT63	I	CCU60
REQGT0B	CCU61_COUT63	I	CCU61
REQGT0C	CCU62_COUT63	I	CCU62
REQGT0D	CCU63_COUT63	I	CCU63
REQGT0E	ERU_PDOUT0	I (s)	ERU
REQGT0F	ERU_PDOUT1	I (s)	ERU
REQGT0G	P6.0	I (s)	external pin
REQGT0H	CCU60_CC60	I (s)	CCU60

Table 17-11 ADC0 Digital Connections in XC27x8X (cont'd)

Signal	from/to Module	I/O to ADC0	Can be used to/as, connected to
REQTR0A	CC2_CC16	I	CC
REQTR0B	ERU_TOUT1	I	ERU
REQTR0C	CCU61_SR3	I	CCU61
REQTR0D	0	I	
REQTR0E	P6.1	I (s)	external pin
REQTR0F	P6.3	I (s)	external pin
REQTR0G	ADC0_REQGT0	I (s)	extend input selection for triggering by using gating inputs (with ENGT = 0X)
REQTR0H	ADC0_SR3	I (s)	service request output 3 of ADC0
REQTR0	-	O	selected trigger signal for source 0
REQGT0	ADC0_REQTR0G	O	selected gating signal for source 0

Request Source 1

REQGT1A	CCU60_COUT63	I	CCU60
REQGT1B	CCU61_COUT63	I	CCU61
REQGT1C	CCU62_COUT63	I	CCU62
REQGT1D	CCU63_COUT63	I	CCU63
REQGT1E	ERU_PDOUT0	I (s)	ERU
REQGT1F	ERU_PDOUT1	I (s)	ERU
REQGT1G	P6.0	I (s)	external pin
REQGT1H	CCU60_CC61	I (s)	CCU60
REQTR1A	CC2_CC17	I	CC2
REQTR1B	ERU_TOUT1	I	ERU
REQTR1C	CCU61_SR3	I	CCU61
REQTR1D	0	I	
REQTR1E	P6.1	I (s)	external pin
REQTR1F	P6.3	I (s)	external pin
REQTR1G	ADC0_REQGT1	I (s)	extend input selection for triggering by using gating inputs (with ENGT = 0X)
REQTR1H	ADC0_SR3	I (s)	service request output 3 of ADC0
REQTR1	-	O	selected trigger signal for source 1

Table 17-11 ADC0 Digital Connections in XC27x8X (cont'd)

Signal	from/to Module	I/O to ADC0	Can be used to/as, connected to
REQGT1	ADC0_REQTR1G	O	selected gating signal for source 1
Request Source 2			
REQGT2A	CCU60_COUT63	I	CCU60
REQGT2B	CCU61_COUT63	I	CCU61
REQGT2C	CCU62_COUT63	I	CCU62
REQGT2D	CCU63_COUT63	I	CCU63
REQGT2E	ERU_PDOUT0	I (s)	ERU
REQGT2F	ERU_PDOUT1	I (s)	ERU
REQGT2G	P6.0	I (s)	external pin
REQGT2H	CCU60_CC62	I (s)	CCU60
REQTR2A	CC2_CC18	I	CC2
REQTR2B	ERU_TOUT1	I	ERU
REQTR2C	CCU61_SR3	I	CCU61
REQTR2D	0	I	
REQTR2E	P6.1	I (s)	external pin
REQTR2F	P6.3	I (s)	external pin
REQTR2G	ADC0_REQGT2	I (s)	extend input selection for triggering by using gating inputs (with ENGT = 0X)
REQTR2H	ADC0_SR3	I (s)	service request output 3 of ADC0
REQTR2	-	O	selected trigger signal for source 2
REQGT2	ADC0_REQTR2G	O	selected gating signal for source 2
Service Request Outputs¹⁾			
SR3	CCU60_CCPOS2C	O	CCU60 Hall input trigger REQTRxH trigger inputs
SR3	CCU62_CCPOS2C	O	CCU62 Hall input trigger

1) All service request outputs (SR0, SR1, SR2, SR3) are connected to the interrupt controller.

Table 17-12 ADC1 Digital Connections in XC27x8X

Signal	from/to Module	I/O to ADC1	Can be used to/as, connected to
Arbiter Timing			
ARBCNT	CCU62_T12HRE, CCU62_T13HRE, CCU63_T12HRE, CCU63_T13HRE	O	time base for equidistant sampling for CCU62, CCU63
External multiplexer control			
EMUX[0]	P7.2	O	control of external analog multiplexer(s)
EMUX[1]	P7.3	O	control of external analog multiplexer(s)
EMUX[2]	P7.4	O	control of external analog multiplexer(s)
Request source 0			
REQGT0A	CCU60_COUT63	I	CCU60
REQGT0B	CCU61_COUT63	I	CCU61
REQGT0C	CCU62_COUT63	I	CCU62
REQGT0D	CCU63_COUT63	I	CCU63
REQGT0E	ERU_PDOUT0	I (s)	ERU
REQGT0F	ERU_PDOUT1	I (s)	ERU
REQGT0G	P6.0	I (s)	external pin
REQGT0H	CCU63_CC60	I (s)	CCU63
REQTR0A	CC2_CC24	I	CC2
REQTR0B	ERU_TOUT1	I	ERU
REQTR0C	CCU62_SR3	I	CCU62
REQTR0D	0	I	
REQTR0E	P6.1	I (s)	external pin
REQTR0F	P6.3	I (s)	external pin
REQTR0G	ADC1_REQGT0	I (s)	extend input selection for triggering by using gating inputs (with ENGT = 0X)
REQTR0H	ADC1_SR3	I (s)	service request output 3 of ADC1
REQTR0	-	O	selected trigger signal for source 0
REQGT0	ADC1_REQTR0G	O	selected gating signal for source 0
Request source 1			

Table 17-12 ADC1 Digital Connections in XC27x8X (cont'd)

Signal	from/to Module	I/O to ADC1	Can be used to/as, connected to
REQGT1A	CCU60_COUT63	I	CCU60
REQGT1B	CCU61_COUT63	I	CCU61
REQGT1C	CCU62_COUT63	I	CCU62
REQGT1D	CCU63_COUT63	I	CCU63
REQGT1E	ERU_PDOUT0	I (s)	ERU
REQGT1F	ERU_PDOUT1	I (s)	ERU
REQGT1G	P6.0	I (s)	external pin
REQGT1H	CCU63_CC61	I	CCU63
REQTR1A	CC2_CC25	I	CC2
REQTR1B	ERU_TOUT1	I	ERU
REQTR0C	CCU62_SR3	I	CCU62
REQTR1D	0	I	
REQTR1E	P6.1	I (s)	external pin
REQTR1F	P6.3	I (s)	external pin
REQTR1G	ADC1_REQGT1	I (s)	extend input selection for triggering by using gating inputs (with ENGT = 0X)
REQTR1H	ADC1_SR3	I (s)	service request output 3 of ADC1
REQTR1	-	O	selected trigger signal for source 1
REQGT1	ADC1_REQTR1G	O	selected gating signal for source 1

Request source 2

REQGT2A	CCU60_COUT63	I	CCU60
REQGT2B	CCU61_COUT63	I	CCU61
REQGT2C	CCU62_COUT63	I	CCU62
REQGT2D	CCU63_COUT63	I	CCU63
REQGT2E	ERU_PDOUT0	I (s)	ERU
REQGT2F	ERU_PDOUT1	I (s)	ERU
REQGT2G	P6.0	I (s)	external pin
REQGT2H	CCU63_CC62	I	CCU63
REQTR2A	CC2_CC26	I	CC2
REQTR2B	ERU_TOUT1	I	ERU

Table 17-12 ADC1 Digital Connections in XC27x8X (cont'd)

Signal	from/to Module	I/O to ADC1	Can be used to/as, connected to
REQTR2C	CCU62_SR3	I	CCU62
REQTR2D	0	I	
REQTR2E	P6.1	I (s)	external pin
REQTR2F	P6.3	I (s)	external pin
REQTR2G	ADC1_REQGT2	I (s)	extend input selection for triggering by using gating inputs (with ENGT = 0X)
REQTR2H	ADC1_SR3	I (s)	service request output 3 of ADC1
REQTR2	-	O	selected trigger signal for source 2
REQGT2	ADC1_REQTR2G	O	selected gating signal for source 2

Service Request Outputs¹⁾

SR3	CCU61_CCPOS2C	O	CCU61 Hall input trigger
SR3	CCU63_CCPOS2C	O	CCU63 Hall input trigger

1) All service request outputs (SR0, SR1, SR2, SR3) are connected to the interrupt controller.

18 Real Time Clock

The Real Time Clock (RTC) module of the XC27x8X basically consists of a chain of prescalers and timers. Its count clock is derived from the auxiliary oscillator or from the prescaled main oscillator. The RTC serves various purposes:

- 48-bit timer for long term measurements
- System clock to determine the current time and date
(the RTC's structure supports the direct representation of time and date)
- Cyclic time based interrupt (can be generated by any timer of the chain)

A number of programming options as well as interrupt request signals adjust the operation of the RTC to the application's requirements. The RTC can continue its operation while the XC27x8X is in certain power-saving modes, such that real time date and time information is provided.

Control Registers		Data Registers		Counter Registers		Interrupt Control	
RTC_CON	E	RTC_T14REL	E	RTC_T14	E	RTC_ISNC	E
RTCCLKCON		RTC_RELH	E	RTC_RTCH	E	RTC_IC	E
RTC_KSCCFG	E	RTC_RELL	E	RTC_RTCL	E		

RTC_CON	Real Time Clock Control Register	RTC_T14	Timer T14 Count Register
RTCCLKCON	RTC Clock Control Register	RTC_T14REL	Timer T14 Reload Register
RTC_ISNC	Interrupt Subnode Control Reg.	RTC_RTCH/L	RTC Count Registers, High/Low
RTC_IC	RTC Interrupt Control Register	RTC_RELH/L	RTC Reload Registers High/Low
RTC_KSCCFG	Kernel State Configuration Reg.		

mc_rtcregx2k.vsd

Figure 18-1 SFRs Associated with the RTC Module

The RTC module consists of a chain of 3 divider blocks:

- a selectable 8:1 divider (on - off)
- the reloadable 16-bit timer T14
- the 32-bit RTC timer block (accessible via RTC_RTCH and RTC_RTCL), made of:
 - the reloadable 10-bit timer CNT0
 - the reloadable 6-bit timer CNT1
 - the reloadable 6-bit timer CNT2
 - the reloadable 10-bit timer CNT3

All timers count upwards. Each of the five timers can generate an interrupt request. All requests are combined to a common node request.

Note: The RTC registers are only affected by a power reset in order to maintain the correct system time even when system or application resets are executed.

18.1 Defining the RTC Time Base

The timer chain of the RTC is clocked with the count clock signal f_{RTC} which is derived from internal sources (oscillators or PLL) or external sources (pins). The currently active clock source is selected by bitfield RTCCLKSEL in register RTCCLKCON. Optionally prescaled by a factor of 32 and/or 8, this is the basic RTC clock. Depending on the operating mode, timer T14 may provide the count increments used by the application and thus determine the input frequency of the RTC timer, that is, the RTC time base (see also [Table 18-2](#)).

The RTC is also supplied with the system clock f_{SYS} of the XC27x8X. This clock signal is used to control the RTC's logic blocks and its bus interface. To synchronize properly to the count clock, the system clock must run at least four times faster than the count clock, this means $f_{\text{SYS}} \geq 4 \times f_{\text{CNT}}$.

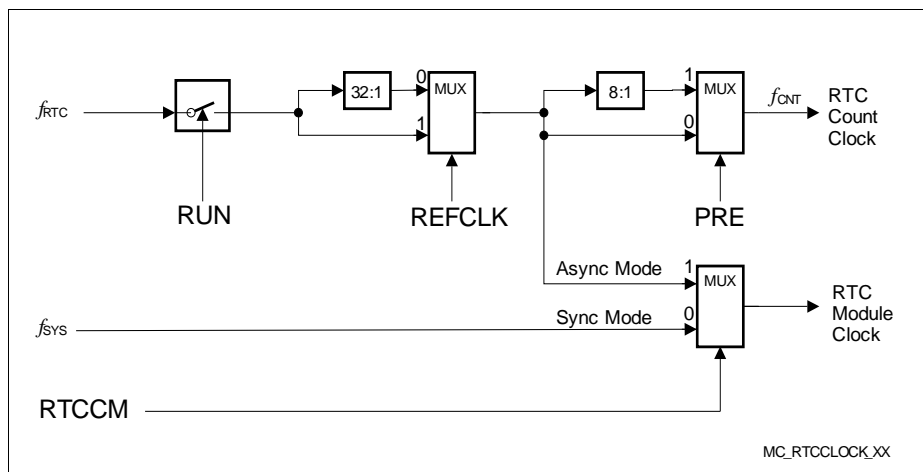


Figure 18-2 RTC Clock Supply Block Diagram

For an example, [Table 18-1](#) lists the interrupt period range and the T14 reload values (for a time base of 1 s and 1 ms):

Table 18-1 RTC Time Base Examples

Oscillator Frequency	T14 Intr. Period		Reload Value A		Reload Value B	
	Min.	Max.	T14REL	Base	T14REL	Base
32.768 kHz	30.52 μ s	16.0 s	8000 _H /F000 _H	1.000 s	FFDF _H /FFFC _H	1.007 ms/ 0.977 ms

Note: Select one value from the reload value pairs, depending if the 8:1 prescaler is disabled/enabled.

Asynchronous Operation

When the system clock frequency becomes lower than $4 \times f_{\text{CNT}}$ proper synchronization is not possible and count events may be missed. This can be the case, when the XC27x8X reduces the system frequency to save power consumption.

In these cases the RTC can be switched to Asynchronous Mode (by clearing bit RTCCM in register RTCCLKCON). In this mode the count registers are directly controlled by the count clock independent of the system clock (hence the name). Asynchronous operation ensures correct time-keeping even during power-save modes.

However, as no synchronization between the count registers and the bus interface can be maintained in asynchronous mode, the RTC registers cannot be written. Read accesses may interfere with count events and, therefore, must be verified (e.g. by reading the same value with three consecutive read accesses).

Note: The access restrictions in asynchronous mode are only meaningful if the system clock is not switched off, of course.

Switching Clocking Modes

The clocking mode of the RTC (synchronous or asynchronous) is selected via bit RTCCM in register RTCCLKCON. After reset, the RTC operates in Synchronous Mode (RTCCM = 1).

The selected clocking mode also affects the access to RTC registers. Bit ACCPOS in register RTC_CON indicates if full register access is possible (ACCPOS = 1, default after reset) or not (ACCPOS = 0). This also indicates the current clocking mode.

Attention: Software should poll bit ACCPOS to determine the proper transition to the intended clocking mode.

After switching to Asynchronous Mode (RTCCM = 0), bit ACCPOS = 0 indicates proper operation in Asynchronous Mode. In this case the system clock can be stopped or reduced.

Note: The clock source for asynchr. mode operation must be selected before switching to asynchr. mode and must only be changed in synchronous mode.

After switching to Synchronous Mode, (RTCCM = 1), bit ACCPOS = 1 indicates proper operation in Synchronous Mode. In this case the RTC registers can again be accessed properly (read and write).

Note: The RTC might lose a counting event (edge of f_{CNT}) when switching from synchronous mode to asynchronous mode while the 8:1 prescaler is disabled. For these applications it is, therefore, recommended to set up the RTC with the 8:1 prescaler enabled.

Increased RTC Accuracy through Software Correction

The accuracy of the XC27x8X's RTC is determined by the oscillator frequency and by the respective prescaling factor (excluding or including T14 and the 8:1 prescaler). The accuracy limit generated by the prescaler is due to the quantization of a binary counter (where the average is zero), while the accuracy limit generated by the oscillator frequency is due to the difference between the ideal and real frequencies (and therefore accumulates over time). This effect is predictable and can be compensated. The total accuracy of the RTC can be further increased via software for specific applications that demand a high time accuracy.

The key to the improved accuracy is knowledge of the exact oscillator frequency. The relation of this frequency to the expected ideal frequency is a measure of the RTC's deviation. The number of cycles, N, after which this deviation causes an error of ± 1 cycle can be easily computed. So, the only action is to correct the count by ± 1 after each series of N cycles. The correction may be made cyclically, for instance, within an interrupt service routine, or by evaluating a formula when the RTC registers are read (for this the respective "last" RTC value must be available somewhere).

Note: For the majority of applications, however, the standard accuracy provided by the RTC's structure will be more than sufficient.

Adjusting the current RTC value would require reading and then writing the complete 48-bit value. This can only be accomplished by three successive accesses each. To avoid the hassle of reading/writing multi-word values, the RTC incorporates a correction option to simply add or suppress one count pulse.

This is done by setting bit T14INC or T14DEC, respectively, in register RTC_CON. This will add an extra count pulse (T14INC) upon the next count event, or suppress the next count event (T14DEC). The respective bit remains set until its associated action has been performed and is automatically cleared by hardware after this event.

Note: Setting both bits, T14INC and T14DEC, at the same time will have no effect on the count values.

18.2 RTC Run Control

If the RTC shall operate bit RUN in register RTC_CON must be set (default after reset). Bit RUN can be cleared, for example, to exclude certain operation phases from time keeping.

Note: A valid count clock f_{RTC} is required for proper RTC operation, of course.

The RTC is reset by a power reset, a system/application reset does not affect the RTC registers and its operation (RTC_IC will be reset, however). The initialization software must ensure the proper RTC operating mode.

Initialization and Disabling of the RTC

Upon a Power-on Reset, register RTC_CON adopts its reset value of 8003_H, which enables the RTC and both prescalers (factor = $8 \times 32 = 256$).

The RTC's clocking mode (synchronous/asynchronous) is selected bit RTCCM in register RTCCLKCON. Upon a Power-on Reset, register RTCCLKCON adopts its reset value of 0006_H, which selects synchronous operation mode and the WUT as the clock source.

For an application reset that is followed by an initialization of the RTC module, the following steps are recommended:

- select synchronous RTC clocking mode, i.e. set bit RTCCLKCON.RTCCM
- select the intended (running) clock source
- make sure that bit ACCPOS is set, before writing to RTC registers
- initialize the RTC

When the RTC module is not used and shall be disabled after a Power-on Reset, the following steps are recommended:

- stop the RTC by clearing its run bit RTC_CON.RUN
- disable the RTC module by clearing its enable bit RTC_KSCCFG.MODEN.

When the RTC module operates in asynchronous mode and shall stop in a power saving mode, software must make sure that no active clock signal is selected by the RTC clock multiplexer.

The RTC control register RTC_CON selects the basic operation of the RTC module.

RTC_CON

RTC Control Register

ESFR (F110_H/88_H)

Reset Value: 8003_H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACC POS	-	-	-	-	-	-	-	-	-	-	-	REF CLK	T14 INC	T14 DEC	PRE	RUN
rh	-	-	-	-	-	-	-	-	-	-	-	rw	rwh	rwh	rw	rw

Field	Bits	Type	Description
ACCPOS	15	rh	RTC Register Access Possible 0 _B No write access is possible, only asynchronous reads 1 _B Registers can be read and written
REFCLK	4	rw	RTC Input Source Prescaler (32:1) Disable 0 _B Input Prescaler enabled 1 _B Input Prescaler disabled
T14INC	3	rwh	Increment Timer T14 Value Setting this bit to 1 adds one count pulse upon the next count event, thus incrementing T14. This bit is cleared by hardware after incrementation.
T14DEC	2	rwh	Decrement Timer T14 Value Setting this bit to 1 suppresses the next count event, thus decrementing T14. This bit is cleared by hardware after decrementation.
PRE	1	rw	RTC Input Source Prescaler (8:1) Enable 0 _B Prescaler disabled 1 _B Prescaler enabled
RUN	0	rw	RTC Run Bit 0 _B RTC stopped 1 _B RTC runs

18.3 RTC Operating Modes

The RTC can be configured for several operating modes according to the purpose it is meant to serve. These operating modes are configured by selecting appropriate reload values and interrupt signals.

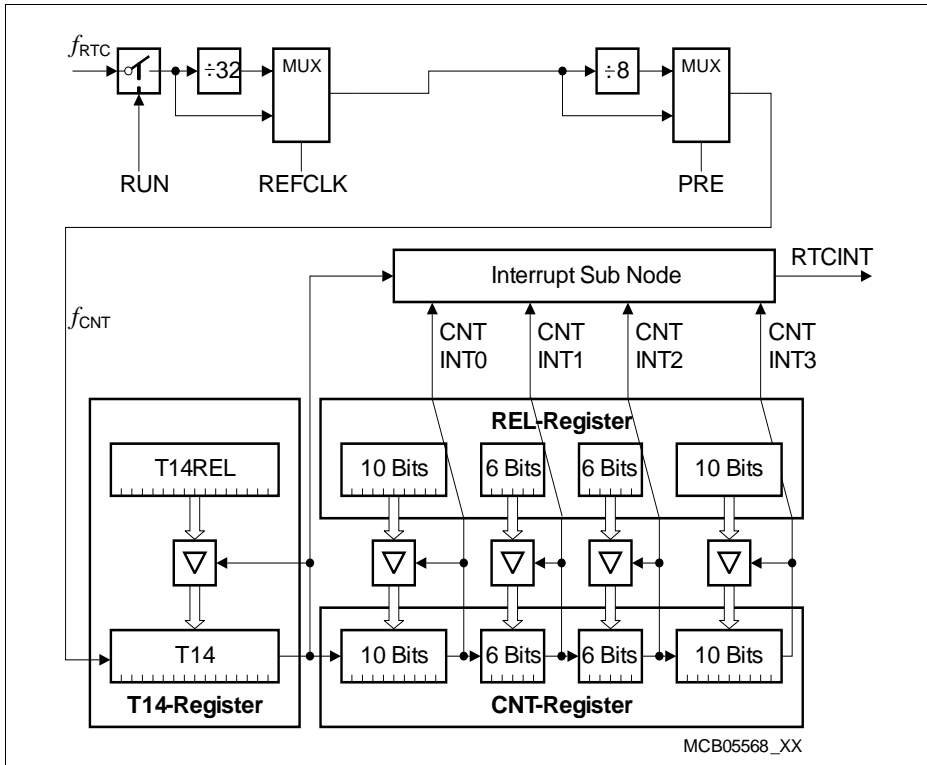


Figure 18-3 RTC Block Diagram

RTC Register Access

The actual value of the RTC is indicated by the three registers T14, RTCL, and RTCH. As these registers are concatenated to build the RTC counter chain, internal overflows occur while the RTC is running. When reading or writing the RTC value, such internal overflows must be taken into account to avoid reading/writing corrupted values.

Care must be taken, when reading the timer(s), as this requires up to three read accesses to the different registers with an inherent time delay between the accesses. An

Real Time Clock

overflow from T14 to RTCL and/or from RTCL to RTCH might occur between the accesses, which needs to be taken into account appropriately.

For example, reading/writing 0000_H from/to RTCH and then accessing RTCL could produce a corrupted value as RTCL may overflow before it can be accessed. In this case, RTCH would be 0001_H. The same precautions must be taken for T14 and T14REL.

Timer T14 and its reload register are accessed via dedicated locations. The four RTC counters CNT3 ... CNT0 are accessed via the two 16-bit RTC timer registers, RTCH and RTCL. The associated four reload values REL3 ... REL0 are accessed via the two 16-bit RTC reload registers, RELH and RELL.

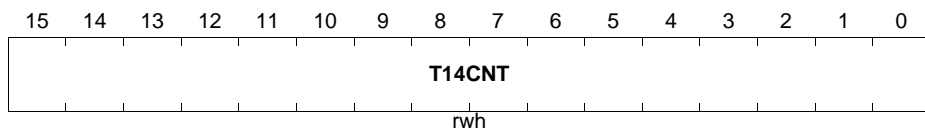
Prescaler T14 and T14 Reload Registers

RTC_T14

T14 Count Register

ESFR(F0D2_H/69_H)

Reset Value: 0000_H



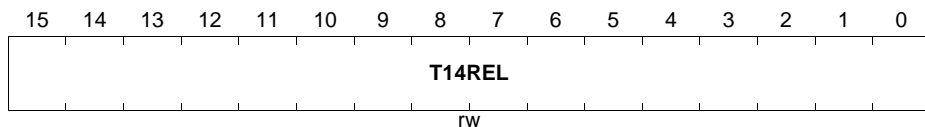
Field	Bits	Typ	Description
T14CNT	[15:0]	rwh	T14 counter

RTC_T14REL

T14 Reload Register

ESFR(F0D0_H/68_H)

Reset Value: 0000_H



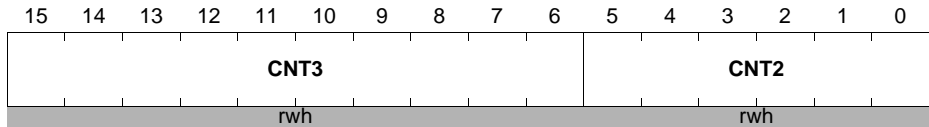
Field	Bits	Typ	Description
T14REL	[15:0]	rw	T14 reload value

RTC_RTCH

RTC Timer High Register

ESFR (F0D6_H/6B_H)

Reset Value: 0000_H



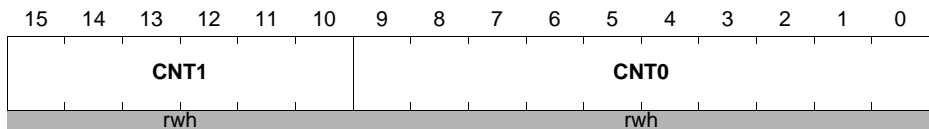
Field	Bits	Type	Description
CNT3	[15:6]	rwh	RTC Timer Count Section CNT3 An overflow of bitfield CNT3 triggers an interrupt request.??
CNT2	[5:0]	rwh	RTC Timer Count Section CNT2 An overflow of bitfield CNT2 triggers a count pulse to count section CNT3 followed by a reload of CNT2 from bitfield REL2. In addition, an interrupt request is triggered.

RTC_RTCL

RTC Timer Low Register

ESFR (F0D4_H/6A_H)

Reset Value: 0000_H



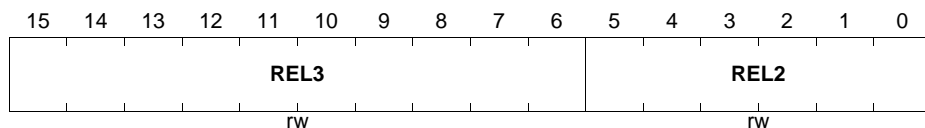
Field	Bits	Type	Description
CNT1	[15:10]	rwh	RTC Timer Count Section CNT1 An overflow of bitfield CNT1 triggers a count pulse to the next count section CNT2 followed by a reload of CNT1 from bitfield REL1. In addition, an interrupt request is triggered.
CNT0	[9:0]	rwh	RTC Timer Count Section CNT0 An overflow of bitfield CNT0 triggers a count pulse to the next count section CNT1 followed by a reload of CNT0 from bitfield REL0. In addition, an interrupt request is triggered.

RTC_RELH

RTC Reload High Register

ESFR (F0CE_H/67_H)

Reset Value: 0000_H



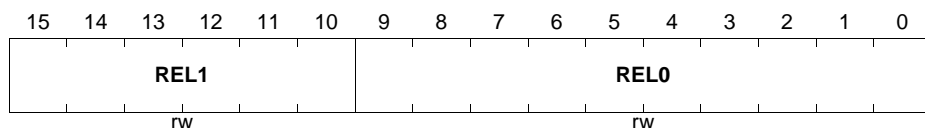
Field	Bits	Type	Description
REL3	[15:6]	rw	RTC Reload Value REL3 This bitfield is copied to bitfield CNT3 upon an overflow of count section CNT3.
REL2	[5:0]	rw	RTC Reload Value REL2 This bitfield is copied to bitfield CNT2 upon an overflow of count section CNT2.

RTC_RELL

RTC Reload Low Register

ESFR (F0CC_H/66_H)

Reset Value: 0000_H



Field	Bits	Type	Description
REL1	[15:10]	rw	RTC Reload Value REL1 This bitfield is copied to bitfield CNT1 upon an overflow of count section CNT1.
REL0	[9:0]	rw	RTC Reload Value REL0 This bitfield is copied to bitfield CNT0 upon an overflow of count section CNT0.

Note: The registers of the RTC receive their reset values only upon a power reset.

18.4 48-bit Timer Operation

The concatenation of timers T14 and COUNT0 ... COUNT3 can be regarded as a 48-bit timer which is clocked with the RTC input frequency, optionally divided by the prescaler. The reload registers T14REL, REL1, and RELH must be cleared to produce a true binary 48-bit timer. However, any other reload value may be used. Reload values other than zero must be used carefully, due to the individual sections of the RTC timer with their own individual overflows and reload values.

The maximum usable timespan is 2^{48} ($\approx 10^{14}$) T14 input clocks. Assuming no prescaler, this would equal more than 200 years at a count frequency of 32 kHz.

18.5 System Clock Operation

A real time system clock can be maintained that keeps on running also during power saving modes (optionally) that maintain a suitable clock signal and supply voltage and indicates the current time and date. This is possible because the RTC module is only reset and cleared by a power reset.

The resolution for this clock information is determined by the input clock of timer T14. By selecting appropriate reload values each cascaded timer can represent directly a part of the current time and/or date. Due to its width, T14 can adjust the RTC to the intended range of operation (time or date). The maximum usable timespan is achieved when T14REL is loaded with 0000_H and so T14 divides by 2^{16} .

System Clock Example

The RTC count clock is 32.768 kHz. By selecting appropriate reload values the RTC timers directly indicate the current time (see [Figure 18-4](#) and [Table 18-2](#)).

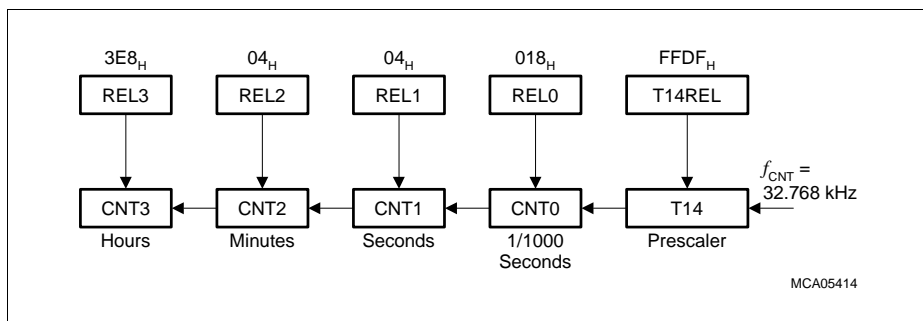


Figure 18-4 RTC Configuration Example

Note: This setup can generate an interrupt request every millisecond, every second, every minute, every hour, or every day.

Real Time Clock

Each timer in the chain divides the clock by ($2^{\text{timer_width}} - \text{reload_value}$) : 1, as the timers count up. **Table 18-2** shows the reload values which must be chosen for a specific scenario (i.e. operating mode of the RTC).

Table 18-2 Reload Value Scenarios

		REL3	REL2	REL1	REL0	T14REL
Time of Day (Figure 18-4)	Formula	$2^{10} - 24$	$2^6 - 60$	$2^6 - 60$	$2^{10} - 1000$	$2^{16} - 33$
	Rel. Value	3E8 _H	04 _H	04 _H	018 _H	FFDF _H
	Function	h	m	s	1/1000 s	Prescaler
	Intr. Period	day	hour	minute	second	millisec. ¹⁾
Day of the Week	Formula	$2^{10} - 7$	$2^6 - 24$	$2^6 - 60$	$2^{10} - 60$	$2^{16} - 32768$
	Rel. Value	3F9 _H	28 _H	04 _H	3C4 _H	8000 _H
	Function	day	h	m	s	Prescaler
	Intr. Period	week	day	hour	minute	second

1) T14 errors in the first example (ms) can be compensated either by choosing an adapted value for REL0, or by using software correction.

18.6 Cyclic Interrupt Generation

The RTC module can generate an interrupt request whenever one of the timers overflows and is reloaded. This interrupt request may be used, for example, to provide a system time tick independent of the CPU frequency without loading the general purpose timers. The interrupt cycle time can be adjusted by choosing appropriate reload values and by enabling the appropriate interrupt request.

In this mode, the other operating modes can be combined. For example, a reload value of T14REL = F9C0_H ($2^{16} - 1600$) generates a T14 interrupt request every 50 ms. Still the subsequent timers can be configured to represent the time or build a binary counter, however with a different time base.

18.7 RTC Interrupt Generation

The overflow signals of each timer of the RTC timer chain can generate an interrupt request. The RTC's interrupt subnode control register ISNC combines these requests to activate the common RTC interrupt request line RTC_IRQ.

Each timer overflow sets its associated request flag in register ISNC. Individual enable bits for each request flag determine whether this request also activates the common interrupt line. The enabled requests are ORed together on this line (see [Figure 18-5](#)). The common interrupt request signal is delayed by 2 system clock cycles due to synchronization.

The interrupt handler can determine the source of an interrupt request via the specific request flags and must clear them after appropriate processing (not cleared by hardware). The common node request bit is automatically cleared when the interrupt handler is vectored to.

Note: If only one source is enabled, no additional software check is required, of course. Both the individual request and the common interrupt node must be enabled.

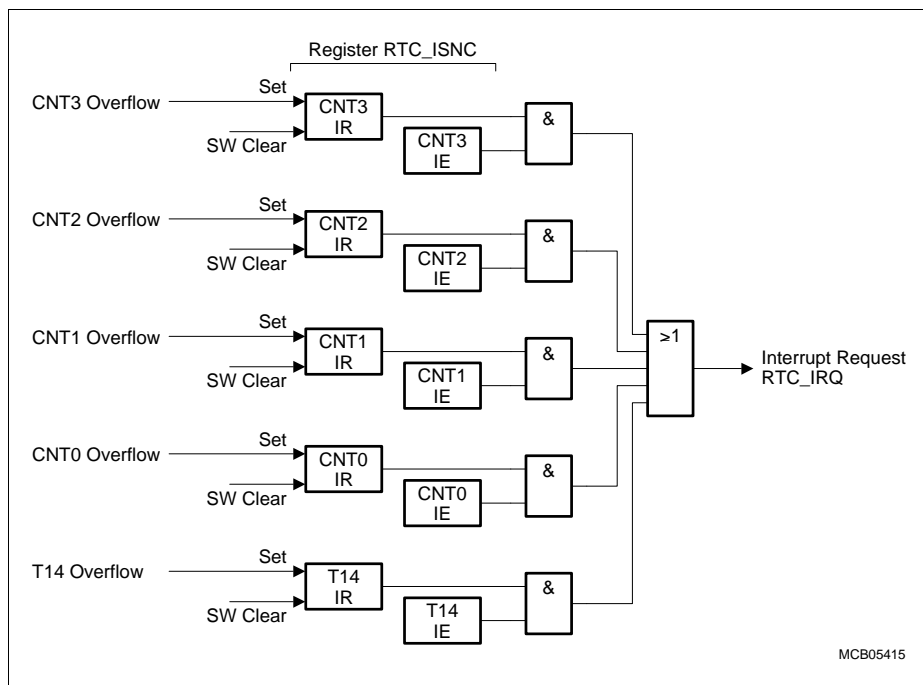


Figure 18-5 Interrupt Block Diagram

RTC_ISNC

RTC Interrupt Subnode Ctrl. Reg.ESFR (F10C_H/86_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	CNT 3IR	CNT 3IE	CNT 2IR	CNT 2IE	CNT 1IR	CNT 1IE	CNT 0IR	CNT 0IE	T14 IR	T14 IE
-	-	-	-	-	-	rwh	rw	rwh	rw	rwh	rw	rwh	rw	rwh	rw

Field	Bits	Type	Description
CNTxIR (x = 0-3)	2*x + 3	rwh	Section CNTx Interrupt Request Flag 0 _B No request pending 1 _B This source has raised an interrupt request
CNTxIE (x = 0-3)	2*x + 2	rw	Section CNTx Interrupt Enable Control Bit 0 _B Interrupt request is disabled 1 _B Interrupt request is enabled
T14IR	1	rwh	T14 Overflow Interrupt Request Flag 0 _B No request pending 1 _B This source has raised an interrupt request
T14IE	0	rw	T14 Overflow Interrupt Enable Control Bit 0 _B Interrupt request is disabled 1 _B Interrupt request is enabled

Note: The interrupt request flags in register ISNC must be cleared by software. They are not cleared automatically when the service routine is entered.

RTC_IC

RTC Interrupt Ctrl. Reg.

ESFR (F19C_H/CE_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	GPX	RTC IR	RTC IE		ILVL			GLVL	
-	-	-	-	-	-	-	rw	rwh	rw		rw			rw	

Field	Bits	Type	Description
GPX	8	rw	Group Priority Extension
RTCIR	7	rwh	RTC Interrupt Request Flag
RTCIE	6	rw	RTC Interrupt Enable Control Bit
ILVL	[5:2]	rw	Interrupt Priority Level
GLVL	[1:0]	rw	Group Priority Extension

Note: Please refer to the general Interrupt Control Register description for an explanation of the control fields.

Register RTC_IC is not part of the RTC module and is reset with any application reset.

18.8 Miscellaneous Registers

RTC_KSCCFG

RTC Kernel State Configuration Register

ESFR(F010_H)

Reset Value: 0001_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BP COM	0	COMCFG	BP SUM	0	SUMCFG	BP NOM	0	NOMCFG	0	BP MOD EN	MOD EN				
w	r	rw	w	r	rw	w	r	rw	r	w	rw				

Field	Bits	Type	Description
MODEN	0	rw	Module Enable This bit enables the module kernel clock and the module functionality. 0 _B The module clock is switched off immediately (without stop condition). The module does not react to mode control actions or read access and ignores write access (except KSCCFG). 1 _B The module is switched on and can operate. To avoid pipeline effects, it is recommended to read register KSCCFG after setting MODEN before accessing other RTC registers.
BPMODEN	1	w	Bit Protection for MODEN 0 _B Bit MODEN is not changed. 1 _B MODEN is updated with the written value.
NOMCFG	[5:4]	rw	Kernel Configuration in Normal Operation Mode 0X _B The module is switched on. 1X _B The module is switched off.
BPNO	7	w	Bit Protection for NOMCFG 0 _B Bitfield NOMCFG is not changed. 1 _B NOMCFG is updated with the written value.
SUMCFG	[9:8]	rw	Kernel Configuration in Suspend Mode Same coding as NOMCFG
BPSUM	11	w	Bit Protection for SUMCFG 0 _B Bitfield SUMCFG is not changed. 1 _B SUMCFG is updated with the written value.
COMCFG	[13:12]	rw	Kernel Configuration in Clock Off Mode Same coding as NOMCFG

Field	Bits	Type	Description
BPCOM	15	w	Bit Protection for COMCFG 0 _B Bitfield COMCFG is not changed. 1 _B COMCFG is updated with the written value.
0	[3:2], 6, 10, 14	r	Reserved; returns 0 if read; should be written with 0;

Note: The protection bits BPxxx enable the write access to their associated bitfields when set. Selected bitfields can be modified by a simple write access without requiring a read-modify-write sequence. They are only active during a write access and are read as 0.

Bitfield SUMCFG is reset by a debug reset, all other bitfields are reset by an application reset.

RTC_ID

RTC Identification Register MEM (FFF8_H/FCH) Reset Value: 5AXX_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOD_TYPE								MOD_REV							
r								r							

Field	Bits	Typ	Description
MOD_REV	[7:0]	r	Module Revision Number MOD_REV defines the revision number. The value of a module revision starts with 01 _H (first revision).
MOD_TYPE	[15:8]	r	Module Type This bit field defines the module identification number (5A _H = RTC).

19 Capture/Compare Unit

The XC27x8X provides a Capture/Compare (CAPCOM2) unit which provides 16 capture/compare channels, which interact with 2 timers. A CAPCOM channel can **capture** the contents of a timer on specific internal or external events, or it can **compare** a timer's contents with given values, and modify output signals in case of a match.

Data Registers	Control Registers	Interrupt Control
CC2_T7/T7REL	CC2_T78CON	CC2_T7IC
CC2_T8/T8REL		CC2_T8IC
CC16-CC19	CC2_M4	CC16IC-CC19IC
CC20-CC23	CC2_M5	CC20IC-CC23IC
CC24-CC27	CC2_M6	CC24IC-CC27IC
CC28-CC31	CC2_M7	CC28IC-CC31IC
	CC2_SEE	
	CC2_SEM	
	CC2_DRM	
	CC2_IOC	
CC2_OUT	CC2_ID	
	CC2_KSCCFG	
CC2_CC16...31	CAPCOM2 Capture/Compare Register 16...31	
CC2_CC16IC...31IC	CAPCOM2 Interrupt Control Register 16...31	
CC2_M4...7	CAPCOM2 Mode Control Register 4...7	
CC2_T78CON	CAPCOM2 Timer Control Register	
CC2_T7, T8	CAPCOM2 Timer Register	
CC2_T7/8REL	CAPCOM2 Timer Reload Register	
CC2_T7IC, T8IC	CAPCOM2 Timer x Interrupt Control Register	
CC2_SEE	CAPCOM2 Single Event Enable Register	
CC2_SEM	CAPCOM2 Single Event Mode Register	
CC2_DRM	CAPCOM2 Double-Register Compare Mode Register	
CC2_OUT	CAPCOM2 Output Register	
CC2_IOC	CAPCOM2 Input/Output Control Register	
CC2_KSCCFG	CAPCOM2 Kernel State Configuration Register	
CC2_ID	CAPCOM2 Module Identification Register	
	cc2_registers.vsd	

Figure 19-1 SFRs Associated with the CAPCOM2 Unit

The two timers of CAPCOM2 are named T7 and T8 and the 16 channels of CAPCOM2 are named CC16...31.

With this mechanism, the CAPCOM2 unit supports generation and control of timing sequences on up to 16 channels with a minimum of software intervention.

From the programmer's point of view, the term 'CAPCOM unit' refers to a set of registers which are associated with this peripheral (see also [Figure 19-1](#)), including the port pins that may be used for alternate input/output functions, and their control bits.

19.1 Functional Overview

The CAPCOM2 unit is typically used to handle high speed IO tasks such as pulse and waveform generation, pulse width modulation, or recording of the time when a specific event occurs. It also supports the implementation of up to 16 software-controlled interrupt events.

The CAPCOM2 Unit consists of two 16-bit timers (T7/T8), each with its own reload register (TxREL), and a bank of sixteen dual-purpose 16-bit capture/compare registers (CCy).

The input clock for the CAPCOM timers is programmable to several prescaled values of the module input clock (f_{CC}), or it can be derived from the overflow/underflow of timer T6. T7 may also operate in counter mode (from an external input), clocked by external events.

Each capture/compare register may be programmed individually for capture or compare operation, and each register may be allocated to either of the two timers. Each capture/compare register has one signal associated with it, which serves as an input signal for the capture operation or as an output signal for the compare operation.

The capture operation causes the current timer contents to be copied into the respective capture/compare register, triggered by an event (transition) on the associated input signal. This event also activates the associated interrupt request line.

The compare operation may cause an output signal transition on the associated output signal, when the allocated timer increments to the value stored in a capture/compare register. The compare match event also activates the associated interrupt request line. In Double-register compare mode a pair of registers controls one common output signal.

The compare output signals are available via a dedicated output register. The output path can be selected.

For the switching of the output signals two timing schemes (see [Section 19.1.10](#)) can be selected:

In **Staggered Mode** the output signals are switched consecutively in 8 steps, which distributes the switching steps over a certain time. In staggered mode, the maximum resolution is $8 t_{CC}$.

In **Non-Staggered Mode** the output signals are switched immediately at the same time. In non-staggered mode, the maximum resolution is $1 t_{CC}$.

[Figure 19-2](#) shows the basic structure of the CAPCOM2 unit.

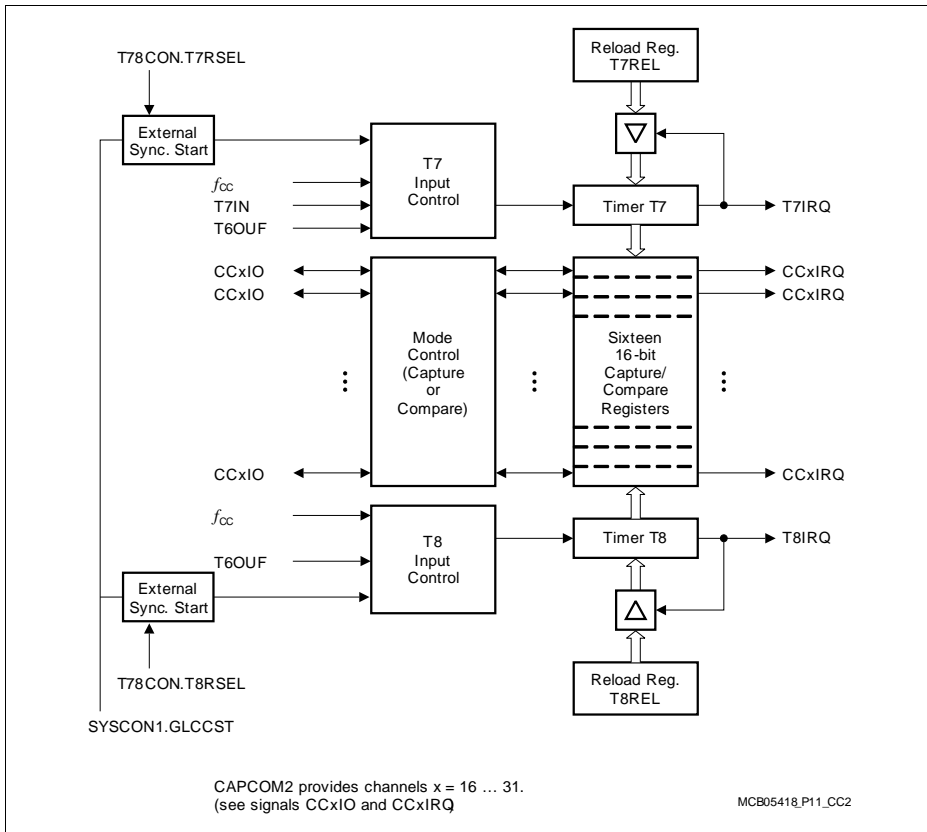


Figure 19-2 CAPCOM2 Unit Block Diagram

There is a possibility to start both timers T7 and T8 synchronously with the CAPCOM6 timers, by setting the bit SYSCON1.GLCCST.

19.1.1 The CAPCOM Timers

The primary use of the timers T7 and T8 is to provide two independent time bases for the capture/compare channels of each unit. The maximum resolution is $8 t_{CC}$ in staggered mode, and $1 t_{CC}$ in non-staggered mode.

The basic structure of the timers, illustrated in [Figure 19-3](#), is identical, except for the input pin (see mark).

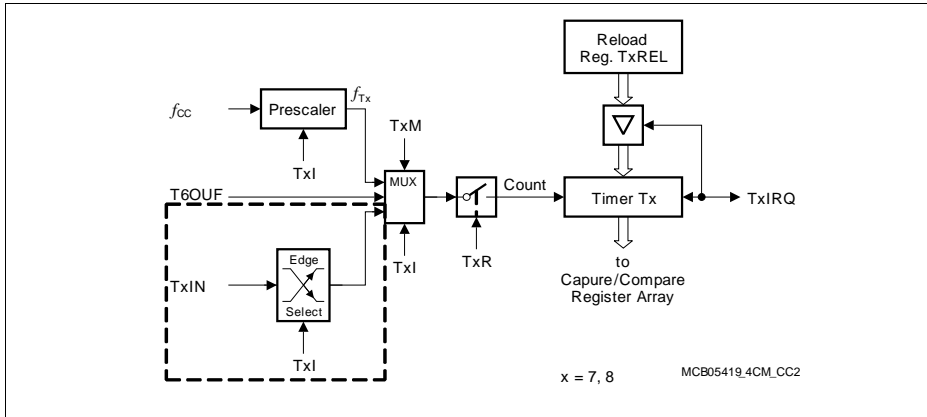


Figure 19-3 Block Diagram of a CAPCOM Timer

The functions of the CAPCOM timers are controlled via the bit-addressable control register **CC2_T78CON**. The high-byte of CC2_T78CON controls T8, the low-byte of CC2_T78CON controls T7. The control options are identical for all timers (except for external input).

In all modes, the timers are always counting upward. The current timer values are accessible for the CPU in the timer registers Tx, which are non bit-addressable registers. When the CPU writes to a register Tx in the state immediately before the respective timer increment or reload is to be performed, the CPU write operation has priority and the increment or reload is disabled to guarantee correct timer operation.

The timer run flags TxR allow the starting and stopping of the timers. The following description of the timer modes and operation always applies to the enabled state of the timers, i.e. the respective run flag is assumed to be set.

Timer Mode

In Timer Mode ($TxM = 0$), the input clock for a CAPCOM timer is derived from f_{CC} , divided by a programmable prescaler. Each timer has its own individual prescaler, controlled through the individual bitfields TxI in the timer control register CC2_T78CON. The input frequency f_{Tx} for a timer Tx and its resolution r_{Tx} are determined by the following formulas:

Staggered Mode:

$$f_{Tx}[\text{MHz}] = \frac{f_{CC}[\text{MHz}]}{2^{(<TxI> + 3)}} \quad r_{Tx}[\mu\text{s}] = \frac{2^{(<TxI> + 3)}}{f_{CC}[\text{MHz}]} \quad (19.1)$$

Non-Staggered Mode:

$$f_{Tx}[\text{MHz}] = \frac{f_{CC}[\text{MHz}]}{2^{<TxI>}} \quad r_{Tx}[\mu\text{s}] = \frac{2^{<TxI>}}{f_{CC}[\text{MHz}]} \quad (19.2)$$

When a timer overflows from FFFF_H to 0000_H, it is reloaded with the value stored in its respective reload register TxREL. The reload value determines the period P_{Tx} between two consecutive overflows of Tx as follows:

Staggered Mode:

$$P_{Tx}[\mu\text{s}] = \frac{(2^{16 - <TxREL>} \times 2^{(<TxI> + 3)})}{f_{CC}[\text{MHz}]} \quad (19.3)$$

Non-Staggered Mode:

$$P_{Tx}[\mu\text{s}] = \frac{(2^{16 - <TxREL>} \times 2^{<TxI>})}{f_{CC}[\text{MHz}]} \quad (19.4)$$

After a timer has been started by setting its run flag (TxR), the first increment will occur within the time interval which is defined by the selected timer resolution. All further increments occur exactly after the time defined by the timer resolution.

Examples for timer input frequencies, resolution and periods, which result from the selected prescaler option in TxI when using a 40 MHz clock, are listed in [Table 19-1](#) below. The numbers for the timer periods are based on a reload value of 0000_H. Note that some numbers may be rounded.

Table 19-1 Timer Tx Input Clock Selection for Timer Mode, $f_{CC} = 40 \text{ MHz}$

Txl	Prescaler	Input Frequency	Resolution	Period
Staggered Mode				
000 _B	8	5 MHz	200 ns	13.11 ms
001 _B	16	2.5 MHz	400 ns	26.21 ms
010 _B	32	1.25 MHz	800 ns	52.43 ms
011 _B	64	625 kHz	1.6 μs	104.86 ms
100 _B	128	312.5 kHz	3.2 μs	209.72 ms
101 _B	256	156.25 kHz	6.4 μs	419.43 ms
110 _B	512	78.125 kHz	12.8 μs	838.86 ms
111 _B	1024	39.0625 kHz	25.6 μs	1677.72 ms
Non-Staggered Mode				
000 _B	1	40 MHz	25 ns	1.6384 ms
001 _B	2	20 MHz	50 ns	3.2768 ms
010 _B	4	10 MHz	100 ns	6.5536 ms
011 _B	8	5 MHz	200 ns	13.11 ms
100 _B	16	2.5 MHz	400 ns	26.21 ms
101 _B	32	1.25 MHz	800 ns	52.43 ms
110 _B	64	625 kHz	1.6 μs	104.86 ms
111 _B	128	312.5 kHz	3.2 μs	209.72 ms

Counter Mode

In Counter Mode ($\text{TxFM} = 1$), the input clock of a CAPCOM timer is either derived from an associated external input pin, T7IN, or from the over-/underflows of GPT timer T6.

Using an external signal connected to pin TxIN as a counting signal is only possible for timer T7. The only counter option for timer T8 is using the over-/underflows of the GPT timer T6 (selected by $\text{Txl} = 000_{\text{B}}$).

Bitfields T7I are used to select either a positive, a negative, or both a positive and a negative transition of the external signal at pin T7IN to trigger an increment of timer T7. Please note that certain criteria must be met for the external signal and the port pin programming for this mode in order to operate properly. These conditions are detailed in [Chapter 19.1.11](#).

Timer Overflow and Reload

When a CAPCOM timer contains the value $FFFF_H$ at the time a new count trigger occurs, a timer interrupt request is generated, and the timer is loaded with the contents of its associated reload register TxREL. The timer then resumes incrementing with the next count trigger starting from the reloaded value.

The reload registers TxREL are not bit-addressable. After reset, they contain the value 0000_H .

19.1.2 Timer Interrupt

Upon a timer overflow the corresponding timer interrupt request flag TxIR for the respective timer will be set. This flag can be used to generate an interrupt or trigger a PEC service request, when enabled by the respective interrupt enable bit TxIE.

Each timer has its own bit-addressable interrupt control register CC2_TxIC and its own interrupt vector. The organization of the interrupt control registers TxIC is identical with the other interrupt control registers.

19.1.3 Capture/Compare Channels

The 16-bit capture/compare registers **CC2_CCy (y=16-31)** are used as data registers for capture or compare operations with respect to timers T7 and T8. The capture/compare registers are not bit-addressable.

The functions of the 16 capture/compare registers of a unit are controlled by 4 bit-addressable 16-bit mode control registers, named **CC2_M4 ... CC2_M7**, which are all organized identically. Each register contains the bits for mode selection and timer allocation for four capture/compare registers.

Each of the registers CCy may be individually programmed for capture mode or for one of 4 different compare modes, and may be allocated individually to one of the two timers of the CAPCOM unit.

A special **Double-Register Compare Mode** combines two registers to act on one common output signal. When capture or compare operations are disabled for one of the CCy registers, it may be used for general purpose variable storage.

Table 19-2 Selection of Capture Modes and Compare Modes

Mode	MODy	Selected Operating Mode
Disabled	000 _B	Disable Capture and Compare Modes The respective CAPCOM register may be used for general variable storage.
Capture	001 _B	Capture on Positive Transition (Rising Edge) at Pin CCyIO
	010 _B	Capture on Negative Transition (Falling Edge) at Pin CCyIO
	011 _B	Capture on Positive and Negative Transition (Both Edges) at Pin CCyIO
Compare	100 _B	Compare Mode 0: Interrupt Only Several interrupts per timer period. Can enable double-register compare mode for Bank2 registers.
	101 _B	Compare Mode 1: Toggle Output Pin on each Match Several compare events per timer period. Can enable double-register compare mode for Bank1 registers.
	110 _B	Compare Mode 2: Interrupt Only Only one interrupt per timer period.
	111 _B	Compare Mode 3: Set Output Pin on each Match Reset output pin on each timer overflow; only one interrupt per timer period.

Capture/Compare Unit

The detailed discussion of the capture and compare modes is valid for all the capture/compare channels, so registers, bits and pins are only referenced by a placeholder.

19.1.4 Capture Mode

In Capture Mode, the current contents of a CAPCOM timer are copied (captured) into the respective capture/compare register in response to an external event. This is used, for example, to record the time at which an external event has occurred, or to measure the distance between two external events in timer increments.

The event to cause a capture of a timer's contents can be programmed to be either the positive, the negative, or both the positive and the negative transition of the external signal connected to the input pin. This triggering transition is selected by bitfield MODy in the respective mode control register. When the selected external signal transition occurs, the selected timer's contents is copied into the capture/compare register and the respective interrupt request line CCyIRQ is activated. This can cause an interrupt or PEC service request, when enabled.

Note: A capture input can be used as an additional external interrupt input. The capture operation can be disregarded in this case.

Either the contents of timer T7 or T8 can be captured, selected by the timer allocation control bit ACCy in the respective mode control register.

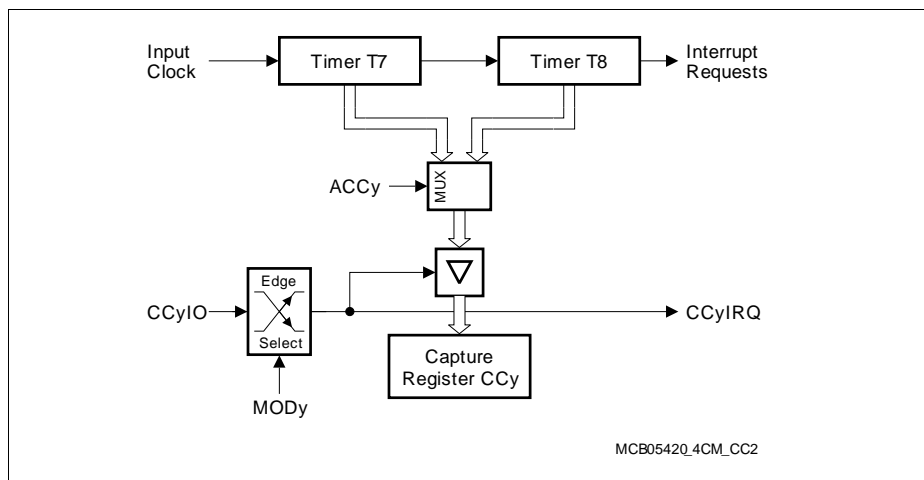


Figure 19-4 Capture Mode Block Diagram

For capture operation, the respective pin must be programmed for input. To ensure that a transition of the input signal is recognized correctly, its level must be held high or low

for a minimum number of module clock cycles before it changes. This information can be found in [Section 19.1.11](#).

19.1.5 Compare Modes

The compare modes allow triggering of events (interrupts and/or output signal transitions) or generation of pulse trains with minimum software overhead. In all compare modes, the 16-bit value stored in a capture/compare register CCy (in the following also referred to as 'compare value') is continuously compared with the contents of the allocated timer (T7 or T8). If the current timer contents match the compare value, the interrupt request line associated with register CCy is activated and, depending on the compare mode, an output signal can be generated at the corresponding output pin CCyIO.

Four different compare modes are available, which can be selected individually for each of the capture/compare registers by bitfield MODy in the respective mode control register. Modes 0 and 2 do not influence the output signals. In the following, each mode is described in detail.

In addition to these 'single-register' modes, a 'double-register' compare mode enables two registers to operate on the same pin. This feature can further reduce software overhead, as two different compare values can be programmed to control a sequence of transitions for a signal. See [Section 19.1.6](#) for details for this operation.

In all Compare Modes, the comparator performs an 'equal to' comparison. This means, a match is only detected when the timer contents are equal to the contents of a compare register. In addition, the comparator is only enabled in the clock cycle directly after the timer was incremented by hardware. This is done to prevent repeated matches if the timer does not operate with the highest possible input clock (either in timer or counter mode). In this case, the timer contents would remain at the same value for several or up to thousands of cycles. This operation has the side-effect, that software modifications of the timer contents will have no effect regarding the comparator. If a timer is set by software to the same value stored in one of the compare registers, no match will be detected. If a compare register is set to a value smaller than the current timer contents, no action will take place.

For the exact operation of the port output function, please see [Section 19.1.8](#).

When two or more compare registers are programmed to the same compare value¹⁾, their corresponding interrupt request flags will be set and the selected output signals will be generated after the allocated timer is incremented to this compare value. Further compare events on the same compare value are disabled²⁾ until the timer is incremented

1) In staggered mode these interrupts and output signals are generated sequentially (see [Section 19.1.10](#)).

2) Even if more compare cycles are executed before the timer increments (lower timer frequency) a given compare value only results in one single compare event.

again or written to by software. After a reset, compare events for register CCy will only become enabled, if the allocated timer has been incremented or written to by software and one of the compare modes described in the following has been selected for this register.

19.1.5.1 Compare Mode 0

This is an interrupt-only mode which can be used for software timing purposes. In this mode, the interrupt request line CCyIRQ is activated each time a match is detected between the contents of the compare register CCy and the allocated timer. A match means, the contents of the timer are equal to ('=') the contents of the compare register. Several of these compare events are possible within a single timer period, if the compare value in register CCy is updated during the timer period. The corresponding port signal CCyIO is not affected by compare events in this mode and can be used as general purpose IO.

Note: If compare mode 0 is programmed for one of the bank2 registers the double-register compare mode may be enabled for this register (see [Chapter 19.1.6](#)).

19.1.5.2 Compare Mode 1

This is a compare mode which influences the associated output signal. Besides this, the basic operation is as in compare mode 0. Each time a match is detected between the contents of the compare register CCy and the allocated timer, the interrupt request line CCyIRQ is activated. In addition, the associated output signal is toggled. Several of these compare events are possible within a single timer period, if the compare value in register CCy is updated during the timer period.

Note: If compare mode 1 is programmed for one of the bank1 registers the double-register compare mode may be enabled for this register (see [Section 19.1.6](#)).

For the exact operation of the port output signal, please see [Section 19.1.8](#).

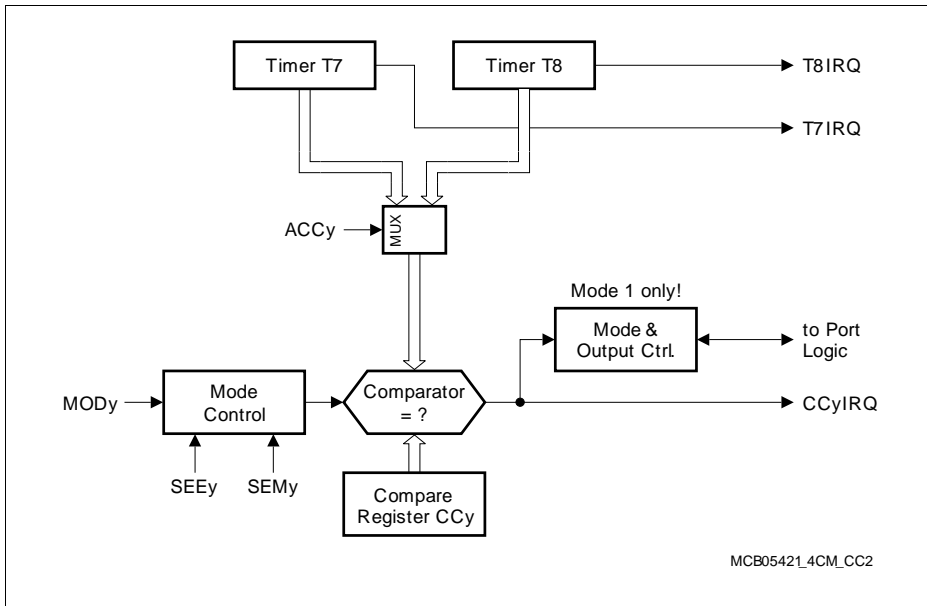


Figure 19-5 Compare Mode 0 and 1 Block Diagram

Note: The signal remains unaffected in compare mode 0.

Figure 19-6 illustrates a few example cases for compare modes 0 and 1.

In all examples, the reload value of the used timer is set to FFF9_H . When the timer overflows, it starts counting from this value upwards.

In Case 1, register CCy contains the value FFFC_H . When the timer reaches this value, a match is detected, and the interrupt request line CCyIRQ is activated. In compare mode 0, this is all that will happen. In compare mode 1, additionally the associated port output is toggled, causing an inversion of the output signal. If the contents of register CCy are not changed, this operation will take place each time the timer reaches the programmed compare value.

In Case 2, software reloads the compare register CCy with FFFF_H after the first match with FFFC_H has occurred. As the timer continues to count up, it finally reaches this new compare value, and a new match is detected, activating the interrupt request line (both modes) and toggling the output signal (compare mode 1). If then the compare value is left unchanged, the next match will occur when the timer reaches FFFF_H again. This example illustrates, that further compare matches are possible within the current timer period (this is in contrast to compare modes 2 and 3).

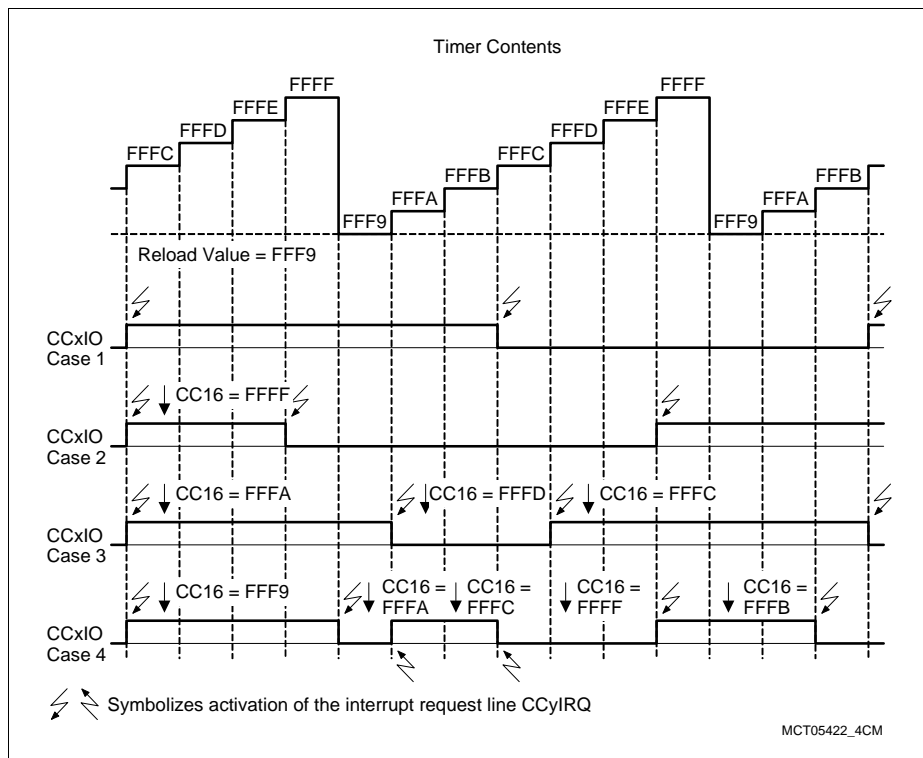


Figure 19-6 Examples for Compare Modes 0 and 1

In Case 3, a new compare value, higher than the current timer contents, causes a new match within the current timer period. The compare register is reloaded with $FFFA_H$ after the first match (at $FFFC_H$). However, the timer has already passed this value. Thus, it will take until the timer reaches $FFFA_H$ in the following timer period to cause the desired compare match. Reloading register CCy now with a value higher than the current timer contents will cause the next match within this period.

In Case 4, the compare values are equal to the timer reload value or to the maximum count value, $FFFF_H$.

19.1.5.3 Compare Mode 2

Compare mode 2 is an interrupt-only mode similar to compare mode 0. The main difference is that only one compare match, corresponding to one interrupt request, is possible within a given timer period.

When a match is detected in compare mode 2 for the first time within a count period of the allocated timer, the interrupt request line CCyIRQ is activated. In addition, all further compare matches within the current timer period are disabled, even if a new compare value, higher than the current timer contents, would be written to the register. This blocking is only released when the allocated timer overflows. A new compare value written to the compare register after the first match will only go into effect within the following timer period.

19.1.5.4 Compare Mode 3

Compare mode 3 is based on compare mode 2, but additionally influences the associated port pin. Only one compare event is possible within one timer period.

When a match is detected in compare mode 3 for the first time within a count period of the allocated timer, the interrupt request line CCyIRQ is activated, and the associated output signal is set to 1. In addition, all further compare matches within the current timer period are disabled, even if a new compare value, higher than the current timer contents, would be written to the register. This blocking is only released when the allocated timer overflows. A new compare value written to the compare register after the first match will only go into effect within the following timer period.

The overflow signal is also used to reset the associated output signal to 0.

Special attention has to be paid when the compare value is set equal to the timer reload value. In this case, the compare match signal would try to set the output signal, while the timer overflow tries to reset the output signal. This conflict is avoided such that the state of the output signal is left unchanged in this case.

Note: When the compare value is changed from a value above the current timer contents to a value below the current timer contents, the new value is not recognized before the next timer period.

For the exact operation of the port output signal, please see [Section 19.1.8](#).

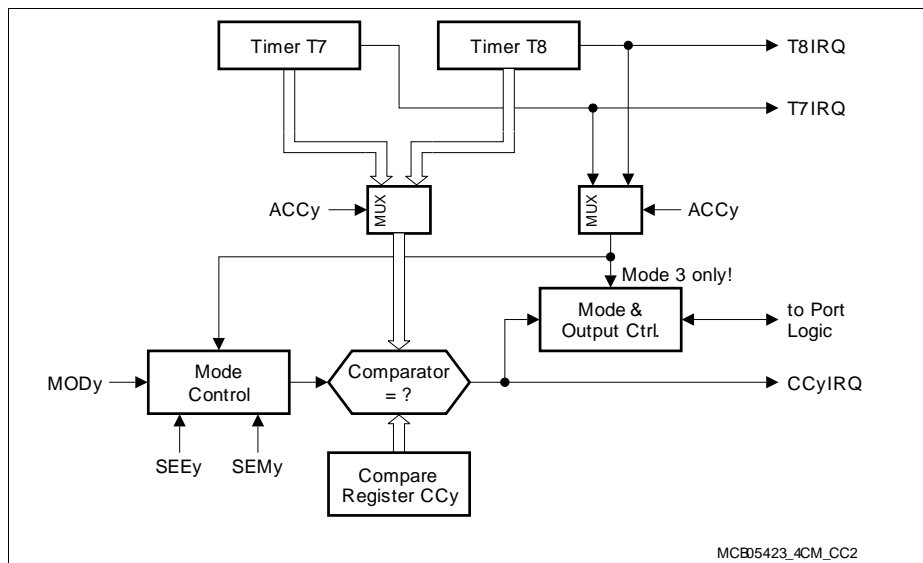


Figure 19-7 Compare Mode 2 and 3 Block Diagram

Note: The port signal remains unaffected in compare mode 2.

Figure 19-8 illustrates a few timing examples for compare modes 2 and 3.

In all examples, the reload value of the used timer is set to $FFF9_H$. When the timer overflows, it starts counting from this value upwards.

In Case 1, register CCy contains the value $FFFC_H$. When the timer reaches this value, a match is detected, and the interrupt request line CCyIRQ is activated. In compare mode 2, this is all that will happen. In compare mode 3, additionally the associated port output is set to 1. The timer continues to count, and finally reaches its overflow. At this point, the port output is reset to 0 again. Note that, although not shown in the diagrams, the overflow signal of the timer also activates the associated interrupt request line TxIRQ. If the contents of register CCy are not changed, the port output will be set again during the following timer period, and reset again when the timer overflows. This operation is ideal for the generation of a pulse width modulated (PWM) signal with a minimum of software overhead. The pulse width is varied by changing the compare value accordingly.

In Case 2, the compare operation is blocked after the first match within a timer period. After the first match at $FFFC_H$, the interrupt request is generated and the port output is set. In addition, further compare matches are disabled. If now a new compare value is written to register CCy, no interrupt request and no port output influence will take place, although the new compare value is higher than the current timer contents. Only after the

Capture/Compare Unit

overflow of the timer, the compare logic is enabled again, and the next match will be detected at $FFFF_H$. One can see, that this operation is ideal for PWM generation, as software can write a new compare value regardless of whether this value is higher or lower than the current timer contents. It is assured that the new value (usually written to the compare register in the appropriate interrupt service routine) will only go into effect during the following timer period.

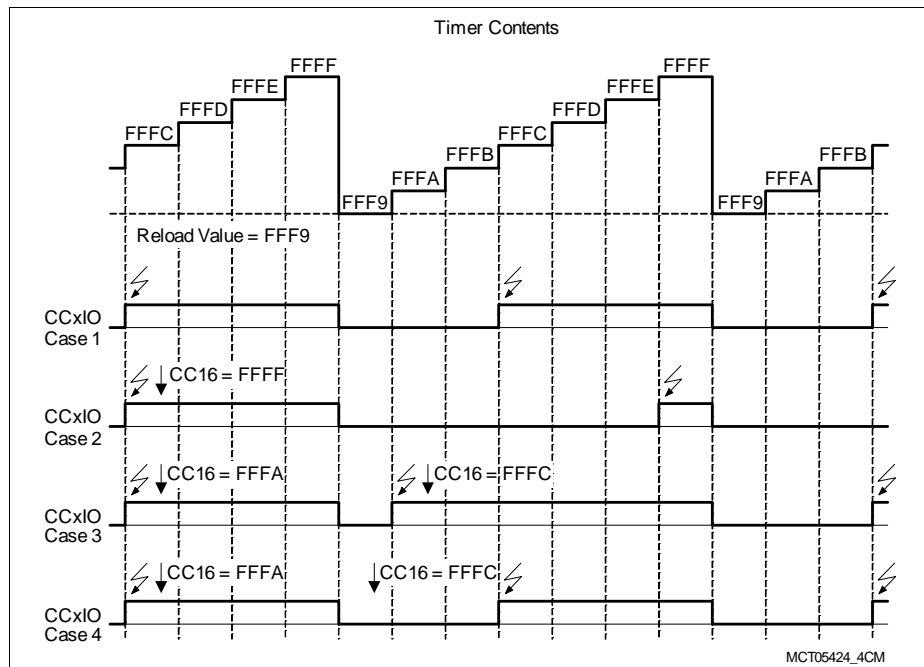


Figure 19-8 Timing Example for Compare Modes 2 and 3

Note: In compare mode 2, only interrupt requests are generated, in mode 3, also the output signals are generated.

In Case 3, further examples for the operation of the compare match blocking are illustrated.

In Case 4, a new compare value is written to a compare register before the first match within the timer period. One can see that, of course, the originally programmed compare match (at $FFFA_H$) will not take place. The first match will be detected at $FFFC_H$. However, it is important to note that the reprogramming of the compare register took place asynchronously - this means, the register was written to without any regard to the current contents of the timer. This is dangerous in the sense that the effect of such an asynchronous reprogramming is not easily predictable. If the timer would have already

Capture/Compare Unit

reached the originally programmed compare value of $FFFA_H$ by the time the software wrote to the register, a match would have been detected and the reprogramming would go into effect during the next timer period.

The examples in **Figure 19-9** show special cases for compare modes 2 and 3. Case 1 illustrates the effect when the compare value is equal to the reload value of the timer. An interrupt is generated in both modes. In mode 3, the output signal is not affected - it remains at the high level. Setting the compare value equal to the reload value easily enables a 100% duty cycle signal for PWM generation. The important advantage here is that the compare interrupt is still generated and can be used to reload the next compare value. Thus, no special treatment is required for this case (see Case 3).

Cases 2, 4, and 5 show different options for the generation of a 0% duty cycle signal. Case 2 shows an asynchronous reprogramming of the compare value equal to the reload value. At the end of the current timer period, a compare interrupt will be generated, which enables software to set the next compare value. The disadvantage of this method is that at least two timer periods will pass until a new regular compare value can go into effect. The compare match with the reload value $FFF9_H$ will block further compare matches during that timer period. This is additionally illustrated by Case 4.

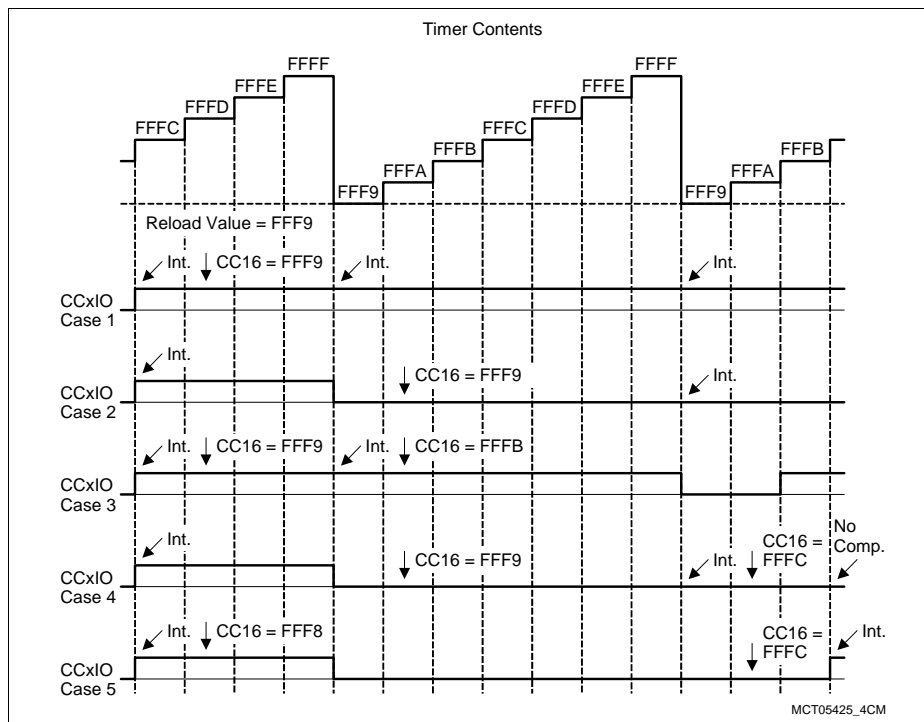


Figure 19-9 Special Cases in Compare Modes 2 and 3

Case 5 shows an option to get around this problem. Here, the compare register is reloaded with $FFF8_H$, a value which is lower than the timer reload value. Thus, the timer will never reach this value, and no compare match will be detected. The output signal will be set to 0 after the first timer overflow. However, after the second overflow, software now reloads the compare register with a regular compare value. As no compare blocking has taken place (since there was no compare match), the newly written compare value will go into effect during the current timer period.

19.1.6 Double-Register Compare Mode

The Double-Register Compare Mode makes it possible to further reduce software overhead for a number of applications. In this mode, two compare registers work together to control one output. This mode is selected via the DRM register, or by a special combination of compare modes for the two registers.

For double-register compare mode, the 16 capture/compare registers of a CAPCOM unit are regarded as two banks of 8 registers each. The lower eight registers form bank1,

while the upper eight registers form bank2. For double-register mode, a bank1 register and a bank2 register form a register pair. Both registers of this register pair operate on the pin associated with the bank1 register.

The relationship between the bank1 and bank2 register of a pair and the effected output pins for double-register compare mode is listed in [Table 19-3](#).

Table 19-3 CAPCOM2 Register Pairs for Double-Register Compare Mode

Register Pair		Used Output Pin	Control Bitfield in CC2_DRM
Bank 1	Bank 2		
CC16	CC24	CC16IO	DR0M
CC17	CC25	CC17IO	DR1M
CC18	CC26	CC18IO	DR2M
CC19	CC27	CC19IO	DR3M
CC20	CC28	CC20IO	DR4M
CC21	CC29	CC21IO	DR5M
CC22	CC30	CC22IO	DR6M
CC23	CC31	CC23IO	DR7M

The double-register compare mode can be programmed individually for each register pair. Double-register compare mode can be selected via a certain combination of compare modes for the two registers of a pair. The bank1 register must be programmed for mode 1 (with port influence), while the bank2 register must be programmed for mode 0 (interrupt-only).

Double-register compare mode can be controlled (this means, enabled or disabled) for each register pair via the associated control bitfield DRxM in register CC2_DRM.

Double-register compare mode can be controlled individually for each of the register pairs.

In the block diagram of the double-register compare mode ([Figure 19-10](#)), a bank2 register will be referred to as CCz, while the corresponding bank1 register will be referred to as CCy.

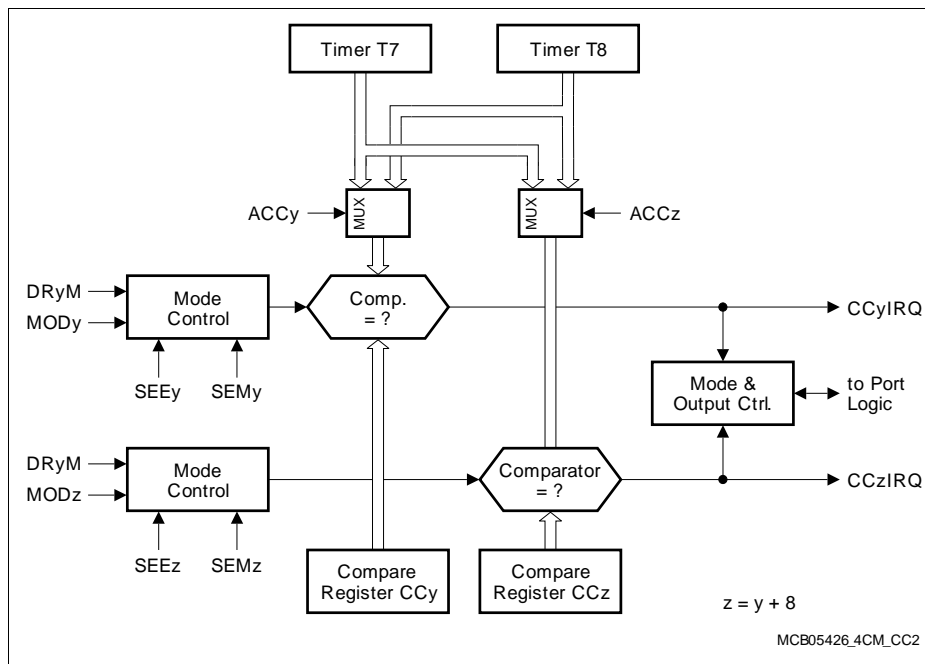


Figure 19-10 Double-Register Compare Mode Block Diagram

When a match is detected for one of the two registers in a register pair (CCy or CCz), the associated interrupt request line (CCyIRQ or CCzIRQ) is activated, and pin CCyIO, corresponding to the bank1 register CCy, is toggled. The generated interrupt always corresponds to the register that caused the match.

Note: If a match occurs simultaneously for both register CCy and register CCz of the register pair, pin CCyIO will be toggled only once, but two separate compare interrupt requests will be generated.

Each of the two registers of a pair can be individually allocated to one of the two timers in the CAPCOM unit. This offers a wide variety of applications, as the two timers can run in different modes with different resolution and frequency. However, this might require sophisticated software algorithms to handle the different timer periods.

Note: The signals CCzIO (which do not serve for double-register compare mode) may be used for general purpose IO.

19.1.7 CAPCOM Interrupts

Upon a capture or compare event, the interrupt request flag CCyIR for the respective capture/compare register CCy is automatically set. This flag can be used to generate an interrupt or trigger a PEC service request when enabled by the interrupt enable bit CCyIE.

Capture interrupts can be regarded as external interrupt requests with the additional feature of recording the time at which the triggering event occurred.

Each of the capture/compare registers (CCy) has its own bitaddressable interrupt control register CC2_CCyIC and its own interrupt vector allocated. These registers are organized in the same way as all other interrupt control registers.

19.1.8 Compare Output Signal Generation

This section discusses the interaction between the CAPCOM Unit and the Port Logic. The block diagram illustrated in [Figure 19-11](#) details the logic of the block “Mode & Output Control”, shown in [Figure 19-5](#), [Figure 19-7](#), and [Figure 19-10](#).

Each output signal is stored in its associated bit of the compare output register CC2_OUT. The individual bits are updated each time an associated compare event occurs. The bits of these registers are connected to the respective port pins as an alternate output function of a port line.

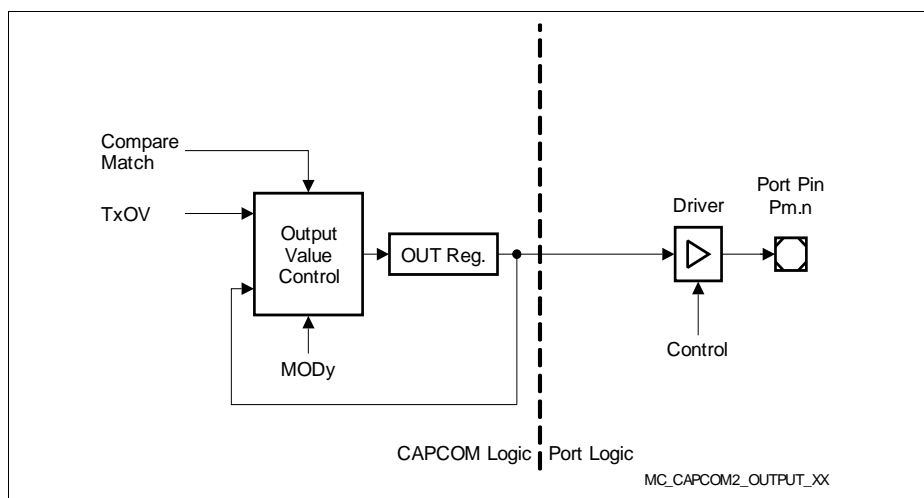


Figure 19-11 Port Output Block Diagram for Compare Modes

Note: A compare output signal is visible at the pin only in compare modes 1 or 3.

The output signal of a compare event can either be a 1, a 0, the complement of the current level, or the previous level. The block 'Output Value Control' determines the correct new level based on the compare event, the timer overflow signal, and the current state of the OUT register bit. For the output toggle function (e.g. in compare mode 1), the state of the OUT register bit is read, inverted, and then written back.

19.1.9 Single Event Mode

If an application requires that one and only one compare event needs to take place (within a certain time frame), single event operation helps to reduce software overhead and to eliminate the need for fast reaction upon events.

In order to achieve a single event operation without this feature, software would have to either disable the compare mode or write a new value, which is outside of the count range of the timer, into the compare register, after the programmed compare match has taken place. Thus, usually an interrupt service routine is required to perform this operation. Interrupt response time may be critical if the timer period is very short - the disable operation needs to be completed before the timer would reach the same value again.

The single event operation eliminates the need for software to react after the first compare match. The complete operation can be set up before the event, and no action is required after the event. The hardware takes care of generating only one event, and then disabling all further compare matches.

This option is programmed via the Single Event Mode register **CC2_SEM** and the Single Event Enable register **CC2_SEE**. Each register provides one bit for each CCy register of a unit.

To setup a single event operation for a CCy register, software first programs the desired compare operation and compare value, and then sets the respective bit in register **CC2_SEM** to enable the single event mode. At last, the respective event enable bit in register **CC2_SEE** is set.

When the programmed compare match occurs, all operations of the selected compare mode take place. In addition, hardware automatically disables all further compare matches and reset the event enable bit in register **CC2_SEE** to 0. As long as this bit is cleared, any compare operation is disabled. To setup a new event, this bit must first be set again.

19.1.10 Staggered and Non-Staggered Operation

The CAPCOM2 unit can run in one of two basic operation modes: Staggered Mode and Non-Staggered Mode. The selection between these modes is performed via register **IOC**.

In staggered mode, a CAPCOM operation cycle consists of 8 module clock cycles, and the outputs of the compare events of the different registers are staggered, that is, the

outputs for compare matches with the same compare value are not switched at the same time, but with a fixed time delay. This operation helps to reduce noise and peak power consumption caused by simultaneous switching outputs.

In non-staggered Mode, a CAPCOM operation cycle is equal to one module clock cycle, and all compare outputs for compare events with the same compare value are switched in the same clock cycle. This mode offers a faster operation and increased resolution of the CAPCOM unit, 8 times higher than in staggered mode.

Staggered Mode

Figure 19-12 illustrates the staggered mode operation for CAPCOM2. In this example, all CCy registers are programmed for compare mode 3.

Registers CC16, CC17, and CC18 are all programmed for a compare value of $FFFE_H$. When the timer increments to $FFFE_H$, the comparator detects a match for all of the three registers. The output CC16IO of register CC16 is switched to 1 one cycle after the comparator match. However, the outputs CC17IO and CC18IO are not switched at the same time, but one, respectively two cycles later. This staggering of the outputs continues for all registers including register CC23. The number of the register indicates the delay of the output signal in clock cycles - the output of register CC23 is switched 7 cycles later than the one of register CC16. In the example, the compare value for register CC13 is set to $FFFD_H$. Thus, the output is switched in the last clock cycle of the CAPCOM cycle in which the timer reached $FFFD_H$.

When the timer overflows, all compare outputs are reset to 0 (compare mode 3). Again, the staggering of the output signals can be seen from **Figure 19-12**.

Looking at registers CC24 through CC31 shows that their outputs are switched in parallel to the respective outputs of registers CC16 through CC23. In fact, the staggering is performed in parallel for the upper and the lower register bank. In this way, it is assured, that both compare signals of a register pair in double-register compare mode operate simultaneously.

Note: This is a general description and only refers to channels connected to pins.

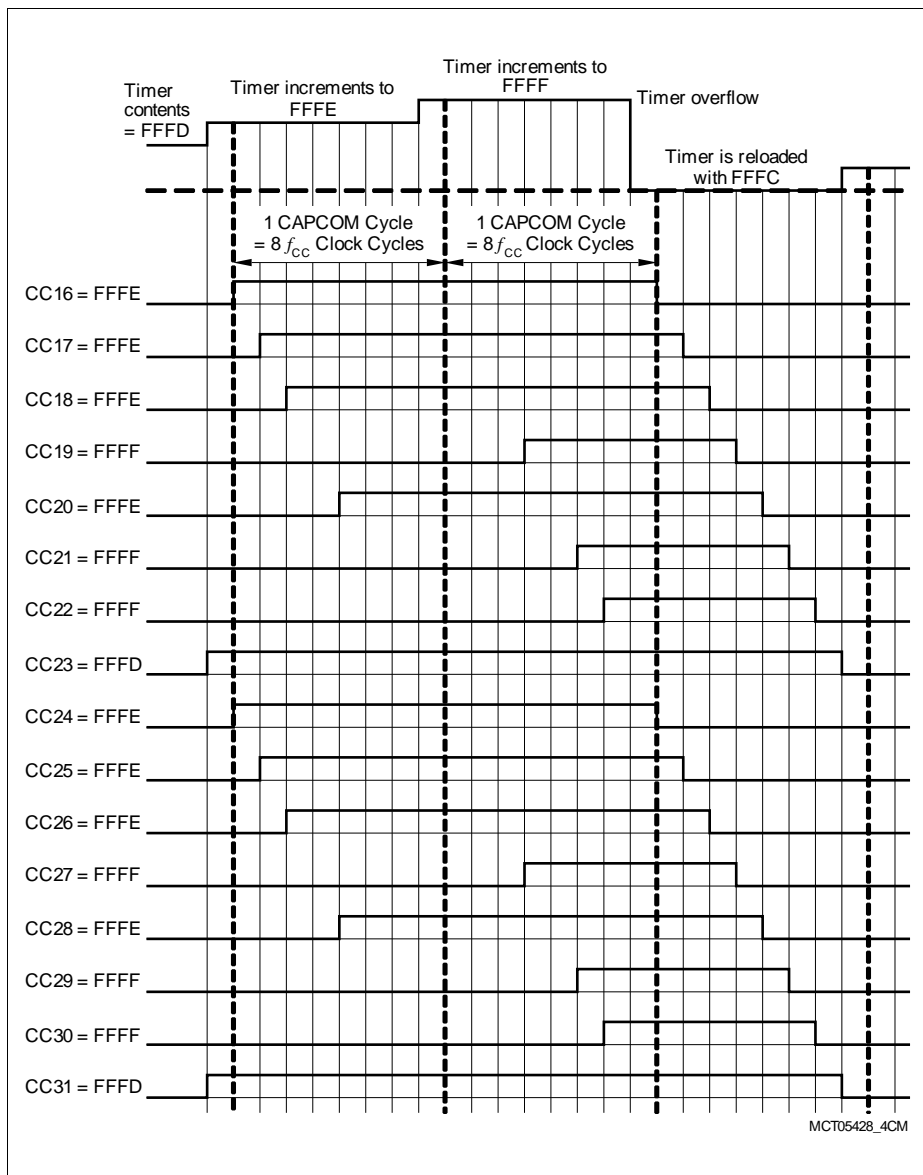


Figure 19-12 Staggered Mode Operation

Non-Staggered Mode

To gain maximum speed and resolution with a CAPCOM unit, it can be switched to non-staggered mode. In this mode, one CAPCOM operation cycle is equal to one module clock cycle. Timer increment and the comparison of its new contents with the contents of the compare register takes place within one clock cycle. The appropriate output signals are switched in the following clock cycle (in parallel to the next possible timer increment and comparison).

Figure 19-13 illustrates the non-staggered mode for CAPCOM2 unit. Note that when the timer overflows, it also takes one additional clock cycle to switch the output signals.

Note: This is a general description and only refers to channels connected to pins.

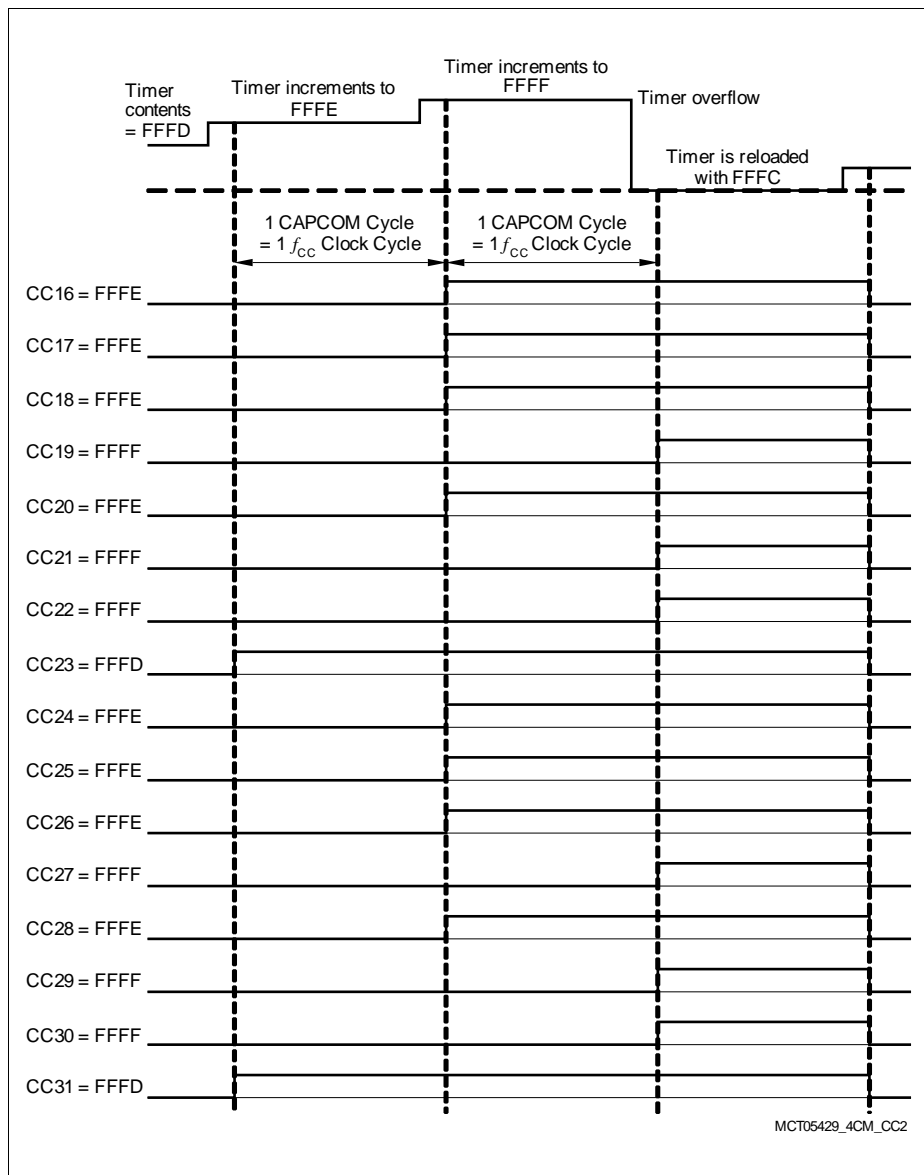


Figure 19-13 Non-Staggered Mode Operation

19.1.11 External Input Signal Requirements

The external input signals of a CAPCOM2 unit are sampled by the CAPCOM2 logic based on the module clock and the basic operation mode (staggered or non-staggered mode). To assure that a signal level is recognized correctly, its high or low level must be held active for at least one complete sampling period.

The duration of a sampling period is one module clock cycle in non-staggered mode, and 8 module clock cycles in staggered mode. To recognize a signal transition, the signal needs to be sampled twice. If the level of the first sampling is different to the level detected during the second sampling, a transition is recognized. Therefore, a minimum of two sampling periods are required for the sampling of an external input signal. Thus, the maximum frequency of an input signal must not be higher than half the module clock frequency in non-staggered mode, and a $1/16^{\text{th}}$ of the module clock frequency in staggered mode.

Table 19-4 summarizes the requirements and limits for external input signals.

Table 19-4 CAPCOM2 External Input Signal Limits

	Non-Staggered Mode	Staggered Mode
Maximum Input Frequency	$f_{CC} / 2$	$f_{CC} / 16$
Minimum Input Signal Level Duration	$1 / f_{CC}$	$8 / f_{CC}$

In order to use an external signal as a count or capture input, the port pin to which it is connected must be configured as input.

Note: For example for test purposes a pin used as a count or capture input may be configured as output. Software or an other peripheral may control the respective signal and thus trigger count or capture events.

In order to cause a compare output signal to be seen by the external world, the associated port pin must be configured as output. For compare output signals the output of register CC2_OUT is used as an alternate output function of a port.

19.2 CAPCOM2 Registers

The following table presents a summary of the registers provided in the CAPCOM2 module.

Table 19-5 CAPCOM2 Module Register Summary

Name	Description	Address		Reset Value
		16-Bit	8-Bit	

Capture / Compare Unit 2 (CAPCOM2)

CC2_ID	CAPCOM2 Identification Register	FFEE _H	-	50XX _H
CC2_M4	CAPCOM2 Mode Control Register 4	FF22 _H	91 _H	0000 _H
CC2_M5	CAPCOM2 Mode Control Register 5	FF24 _H	92 _H	0000 _H
CC2_M6	CAPCOM2 Mode Control Register 6	FF26 _H	93 _H	0000 _H
CC2_M7	CAPCOM2 Mode Control Register 7	FF28 _H	94 _H	0000 _H
CC2_SEE	CAPCOM2 Single Event Enable Register	FE2A _H	15 _H	0000 _H
CC2_SEM	CAPCOM2 Single Event Mode Register	FE28 _H	14 _H	0000 _H
CC2_DRM	CAPCOM2 Double Register Mode Register	FF2A _H	95 _H	0000 _H
CC2_OUT	CAPCOM2 Output Register	FF2C _H	96 _H	0000 _H
CC2_T7	CAPCOM2 Timer 7 Register	F050 _H	28 _H	0000 _H
CC2_T8	CAPCOM2 Timer 8 Register	F052 _H	29 _H	0000 _H
CC2_T7REL	CAPCOM2 Timer 7 Reload Register	F054 _H	2A _H	0000 _H
CC2_T8REL	CAPCOM2 Timer 8 Reload Register	F056 _H	2B _H	0000 _H
CC2_T78CON	CAPCOM2 Timer 7/8 Control Register	FF20 _H	90 _H	0000 _H
CC2_IOC	CAPCOM2 I/O Control Register	F066 _H	33 _H	0000 _H
CC2_CC16	CAPCOM2 Register 16	FE60 _H	30 _H	0000 _H
CC2_CC17	CAPCOM2 Register 17	FE62 _H	31 _H	0000 _H
CC2_CC18	CAPCOM2 Register 18	FE64 _H	32 _H	0000 _H
CC2_CC19	CAPCOM2 Register 19	FE66 _H	33 _H	0000 _H
CC2_CC20	CAPCOM2 Register 20	FE68 _H	34 _H	0000 _H
CC2_CC21	CAPCOM2 Register 21	FE6A _H	35 _H	0000 _H
CC2_CC22	CAPCOM2 Register 22	FE6C _H	36 _H	0000 _H
CC2_CC23	CAPCOM2 Register 23	FE6E _H	37 _H	0000 _H
CC2_CC24	CAPCOM2 Register 24	FE70 _H	38 _H	0000 _H

Table 19-5 CAPCOM2 Module Register Summary (cont'd)

Name	Description	Address		Reset Value
		16-Bit	8-Bit	
CC2_CC25	CAPCOM2 Register 25	FE72 _H	39 _H	0000 _H
CC2_CC26	CAPCOM2 Register 26	FE74 _H	3A _H	0000 _H
CC2_CC27	CAPCOM2 Register 27	FE76 _H	3B _H	0000 _H
CC2_CC28	CAPCOM2 Register 28	FE78 _H	3C _H	0000 _H
CC2_CC29	CAPCOM2 Register 29	FE7A _H	3D _H	0000 _H
CC2_CC30	CAPCOM2 Register 30	FE7C _H	3E _H	0000 _H
CC2_CC31	CAPCOM2 Register 31	FE7E _H	3F _H	0000 _H
CC2_T7IC	CAPCOM2 Timer 7 Interrupt Control Register	FF6C _H	BD _H	0000 _H
CC2_T8IC	CAPCOM2 Timer 8 Interrupt Control Register	FF6E _H	BE _H	0000 _H
CC2_CC16IC	CAPCOM2 Register 16 Interrupt Control Register Shared Interrupt node, see ISSR register	F1C0 _H	B0 _H	0000 _H
CC2_CC17IC	CAPCOM2 Register 17 Interrupt Control Register Shared Interrupt node, see ISSR register	F1C2 _H	B1 _H	0000 _H
CC2_CC18IC	CAPCOM2 Register 18 Interrupt Control Register Shared Interrupt node, see ISSR register	F1C4 _H	B2 _H	0000 _H
CC2_CC19IC	CAPCOM2 Register 19 Interrupt Control Register Shared Interrupt node, see ISSR register	F1C6 _H	B3 _H	0000 _H
CC2_CC20IC	CAPCOM2 Register 20 Interrupt Control Register Shared Interrupt node, see ISSR register	F1C8 _H	B4 _H	0000 _H
CC2_CC21IC	CAPCOM2 Register 21 Interrupt Control Register Shared Interrupt node, see ISSR register	F1CA _H	B5 _H	0000 _H
CC2_CC22IC	CAPCOM2 Register 22 Interrupt Control Register Shared Interrupt node, see ISSR register	F1CC _H	B6 _H	0000 _H
CC2_CC23IC	CAPCOM2 Register 23 Interrupt Control Register Shared Interrupt node, see ISSR register	F1CE _H	B7 _H	0000 _H

Table 19-5 CAPCOM2 Module Register Summary (cont'd)

Name	Description	Address		Reset Value
		16-Bit	8-Bit	
CC2_CC24IC	CAPCOM2 Register 24 Interrupt Control Register Shared Interrupt node, see ISSR register	F1D0 _H	B8 _H	0000 _H
CC2_CC25IC	CAPCOM2 Register 25 Interrupt Control Register Shared Interrupt node, see ISSR register	F1D2 _H	B9 _H	0000 _H
CC2_CC26IC	CAPCOM2 Register 26 Interrupt Control Register Shared Interrupt node, see ISSR register	F1D4 _H	BA _H	0000 _H
CC2_CC27IC	CAPCOM2 Register 27 Interrupt Control Register Shared Interrupt node, see ISSR register	F1D6 _H	BB _H	0000 _H
CC2_CC28IC	CAPCOM2 Register 28 Interrupt Control Register Shared Interrupt node, see ISSR register	F1D8 _H	BC _H	0000 _H
CC2_CC29IC	CAPCOM2 Register 29 Interrupt Control Register Shared Interrupt node, see ISSR register	F1DA _H	C2 _H	0000 _H
CC2_CC30IC	CAPCOM2 Register 30 Interrupt Control Register Shared Interrupt node, see ISSR register	F1DC _H	C6 _H	0000 _H
CC2_CC31IC	CAPCOM2 Register 31 Interrupt Control Register Shared Interrupt node, see ISSR register	F1DE _H	CA _H	0000 _H

19.2.1 Identification Register

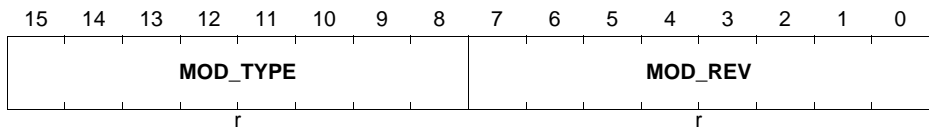
For module type and revision identification the CAPCOM2 unit provides a specific read-only identification register.

CC2_ID

CAPCOM2 Identification Register

MEM (FFEE_H)

Reset Value: 50XX_H



Field	Bits	Typ	Description
MOD_REV	[7:0]	r	Module Revision Number Defines the revision number. The value of a module revision starts with 01 _H (first revision).
MOD_TYPE	[15:8]	r	Module Identification Number Defines the module identification number (50 _H = CAPCOM2).

19.2.2 Timer 7/8 Registers

CC2_T7

CAPCOM2 Timer 7 Register **ESFR (F050_H/28_H)** **Reset Value: 0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T7															
rw															

Field	Bits	Typ	Description
T7	[15:0]	rw	Timer 7 Current Value Current value of the Timer 7

CC2_T8

CAPCOM2 Timer 8 Register **ESFR (F052_H/29_H)** **Reset Value: 0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T8															
rw															

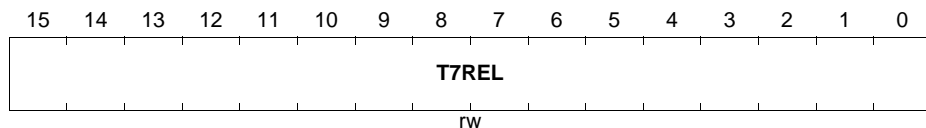
Field	Bits	Typ	Description
T8	[15:0]	rw	Timer 8 Current Value Current value of the Timer 8

CC2_T7REL

CAPCOM2 Timer 7 Reload Register

ESFR (F054_H/2A_H)

Reset Value: 0000_H



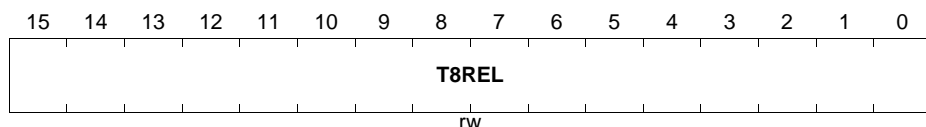
Field	Bits	Typ	Description
T7REL	[15:0]	rw	Timer 7 Reload Value Reload value of the Timer 7

CC2_T8REL

CAPCOM2 Timer 8 Reload Register

ESFR (F056_H/2B_H)

Reset Value: 0000_H



Field	Bits	Typ	Description
T8REL	[15:0]	rw	Timer 8 Reload Value Reload value of the Timer 8

19.2.3 Timer 7/8 Control Register

CC2_T78CON

CAPCOM2 Timer 7/8 Control Register

SFR (FF20_H/90_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	T8R	T8RSEL	T8M		T8I		-	T7R	T7RSEL	T7M		T7I			
-	rw	rw	rw		rw		-	rw	rw	rw		rw			

Field	Bits	Typ	Description
T7I, T8I	[2:0], [10:8]	rw	Timer/Counter Tx Input Selection Timer Mode (TxM = 0): Input frequency $f_{Tx} = f_{CC}/2^{(<TxI>+3)}$ or $f_{CC}/2^{(<TxI>)}$, depending on (non-)staggered mode, see Table 19-1 Counter Mode (TxM = 1): 000 _B Overflow/Underflow of GPT Timer T6 001 _B Positive (rising) edge on pin TxIN 010 _B Negative (falling) edge on pin TxIN 011 _B Any edge (rising and falling) on pin TxIN 1XX _B Reserved. Do not use this combination! <i>Note: For timer T8 the only option in counter mode is 000_B. T8 stop in all other cases.</i>
T7M, T8M	3, 11	rw	Timer / Counter x Mode Selection 0 _B Timer Mode 1 _B Counter Mode
T7R, T8R	6, 14	rw	Timer / Counter x Run Control 0 _B Timer/Counter x is disabled. 1 _B Timer/Counter x is enabled.
T7RSEL	[5:4]	rw	Timer T7 External Run Selection Bit field T7RSEL defines the event of signal T7HR that can set the run bit T7R by HW. 00 _B The external setting of T7R is disabled. 01 _B Bit T7R is set if a rising edge of signal T7HR is detected. 10 _B Bit T7R is set if a falling edge of signal T7HR is detected. 11 _B Bit T7R is set if an edge of signal T7HR is detected.

Field	Bits	Typ	Description
T8RSEL	[13:12]	rw	Timer T8 External Run Selection Bit field T8RSEL defines the event of signal T8HR that can set the run bit T8R by HW. 00 _B The external setting of T8R is disabled. 01 _B Bit T8R is set if a rising edge of signal T8HR is detected. 10 _B Bit T8R is set if a falling edge of signal T8HR is detected. 11 _B Bit T8R is set if an edge of signal T8HR is detected.

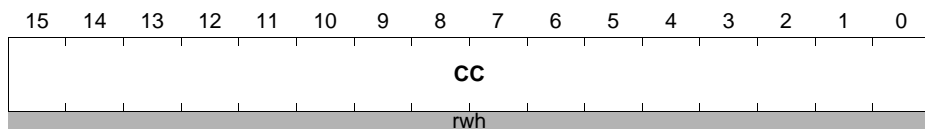
19.2.4 Capture/Compare Registers

CC2_CCy (y=16-31)

CAPCOM2 Capture/Compare Register y

SFR (FE60_H-32+2*y / 30_H-16+y)

Reset Value: 0000_H



Field	Bits	Typ	Description
CC	[15:0]	rwh	Capture Register Value Current value of the Capture/Compare register y

19.2.5 Capture/Compare Mode Registers

CC2_M4

CAPCOM2 Mode Control Register 4

SFR (FF22_H/91_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACC 19	MOD19		ACC 18	MOD18		ACC 17	MOD17		ACC 16	MOD16					
rw	rw		rw	rw		rw	rw		rw	rw					

Field	Bits	Type	Description
ACCy (y=16-19)	4*y-61	rw	Allocation Bit for CAPCOM Register CCy (y = 16-19) 0 _B CCy allocated to Timer T7 1 _B CCy allocated to Timer T8
MODy (y=16-19)	[4*y-62:4*y-64]	rw	Mode Selection for CAPCOM Register CCy (y = 16-19) See Table 19-2 .

CC2_M5

CAPCOM2 Mode Control Register 5

SFR (FF24_H/92_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACC 23	MOD23		ACC 22	MOD22		ACC 21	MOD21		ACC 20	MOD20					
rw	rw		rw	rw		rw	rw		rw	rw					

Field	Bits	Type	Description
ACCy (y=20-23)	4*y-77	rw	Allocation Bit for CAPCOM Register CCy (y = 20-23) 0 _B CCy allocated to Timer T7 1 _B CCy allocated to Timer T8
MODy (y=20-23)	[4*y-78:4*y-80]	rw	Mode Selection for CAPCOM Register CCy (y = 20-23) See Table 19-2 .

CC2_M6

CAPCOM2 Mode Control Register 6

SFR (FF26_H/93_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACC 27	MOD27			ACC 26	MOD26			ACC 25	MOD25			ACC 24	MOD24		
rw	rw			rw	rw			rw	rw			rw	rw		

Field	Bits	Type	Description
ACC_y (y=24-27)	4*y-93	rw	Allocation Bit for CAPCOM Register CC_y (y = 24-28) 0 _B CC _y allocated to Timer T7 1 _B CC _y allocated to Timer T8
MOD_y (y=24-27)	[4*y-94:4*y-96]	rw	Mode Selection for CAPCOM Register CC_y (y = 24-27) See Table 19-2 .

CC2_M7

CAPCOM2 Mode Control Register 7

SFR (FF28_H/94_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACC 31	MOD31			ACC 30	MOD30			ACC 29	MOD29			ACC 28	MOD28		
rw	rw			rw	rw			rw	rw			rw	rw		

Field	Bits	Type	Description
ACC_y (y=28-31)	4*y-109	rw	Allocation Bit for CAPCOM Register CC_y (y = 28-31) 0 _B CC _y allocated to Timer T7 1 _B CC _y allocated to Timer T8
MOD_y (y=28-31)	[4*y-110:4*y-112]	rw	Mode Selection for CAPCOM Register CC_y (y = 28-31) See Table 19-2 .

19.2.6 Compare Output Register

The CAPCOM2's compare output serves two registers in parallel, the port output register for binary compatibility and a separate one for enhanced functionality. The CAPCOM2 compare output and the port output latch is muxed in the port logic.

Compare output is visible at the pin if compare mode 1 or 3 is programmed in the CAPCOM2.

CC2_OUT

CAPCOM2 Compare Output Register

SFR (FF2C _H /96 _H)															
Reset Value: 0000 _H															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CC	CC	CC	CC	CC	CC	CC	CC	CC	CC	CC	CC	CC	CC	CC	CC
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IO	IO	IO	IO	IO	IO	IO	IO	IO	IO	IO	IO	IO	IO	IO	IO
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
CCyIO (y=16-31)	y-16	rwh	Compare Output for Channel y Alternative port output for the associated port pin

19.2.7 Double-Register Compare Mode Register

CC2_DRM

CAPCOM2 Double-Register Compare Mode Register

SFR (FF2A_H/95_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DR7M		DR6M		DR5M		DR4M		DR3M		DR2M		DR1M		DR0M	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
DRxM (x=0-7)	[2*x+1:2*x]	rw	Double Register x Compare Mode Selection 00 _B DRM is controlled via the combination of compare modes 1 and 0 (compatibility mode) 01 _B DRM disabled regardless of compare modes 10 _B DRM enabled regardless of compare modes 11 _B Reserved <i>Note: "x" indicates the register pair index in a bank.</i>

19.2.8 IOC Register

CC2_IOC

CAPCOM2 I/O Control Register ESFR (F066_H/33_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						-						0	ST AG	0	-
						-						r	rw	rw	-

Field	Bits	Typ	Description
0	1	rw	Reserved read as '0', do not set this bit
STAG	2	rw	Staggered Mode Control 0 _B CAPCOM operates in Staggered Mode 1 _B CAPCOM operates in Non-Staggered Mode
0	3	r	Reserved read as '0', do not set this bit
0	[15:4]	r	Reserved read as '0'

19.2.9 Single Event Mode Register

CC2_SEM

CAPCOM2 Single Event Mode Control Register

SFR (FE28_H/14_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEM	SEM	SEM	SEM	SEM	SEM	SEM	SEM	SEM	SEM	SEM	SEM	SEM	SEM	SEM	SEM
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW	rW

Field	Bits	Type	Description
SEMy (y = 16-31)	y-16	rW	Single Event Mode Control 0 _B Single Event Mode disabled for channel y 1 _B Single Event Mode enabled for channel y

CC2_SEE

CAPCOM2 Single Event Enable Register

SFR (FE2A_H/15_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEE	SEE	SEE	SEE	SEE	SEE	SEE	SEE	SEE	SEE	SEE	SEE	SEE	SEE	SEE	SEE
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
SEEy (y = 16-31)	y-16	rwh	Single Event Enable Control 0 _B Single Event disabled for channel y 1 _B Single Event enabled for channel y <i>Note: This bit is cleared by hardware after the event has occurred.</i>

19.2.10 KSCCFG Register

CC2_KSCCFG

CAPCOM2 Kernel State Configuration Register

SFR(FE24_H/12_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BP COM	0	COMCFG	BP SUM	0	SUMCFG	BP NOM	0	NOMCFG	0			BP MOD EN	MOD EN		
w	r	rw	w	r	rw	w	r	rw				r	w	rw	

Field	Bits	Type	Description
MODEN	0	rw	<p>Module Enable</p> <p>This bit enables the module kernel clock and the module functionality.</p> <p>0_B The module is switched off. It does not react on mode control actions and the module clock is switched off immediately (without stop condition). The module does not react on read accesses and ignores write accesses.</p> <p>1_B The module is switched on and can operate. After writing 1 to MODEN, it is recommended to read register KSCCFG to avoid pipeline effects in the control block before accessing other CAPCOM2 registers.</p> <p><i>Note: This bit is reset by an application reset.</i></p>
BPMODEN	1	w	<p>Bit Protection for MODEN</p> <p>This bit enables the write access to the bit MODEN. It always reads 0. It is only active during the write access cycle.</p> <p>0_B MODEN is not changed.</p> <p>1_B MODEN is updated with the written value.</p> <p><i>Note: This bit is reset by an application reset.</i></p>

Field	Bits	Type	Description
NOMCFG	[5:4]	rw	Normal Operation Mode Configuration This bit field defines the kernel mode applied in normal operation mode. 0X _B The module is switched on. 1X _B The module is switched off. This field is taken into account for CR = 00 or 11. <i>Note: This bit is reset by an application reset.</i>
BPNO	7	w	Bit Protection for NOMCFG This bit enables the write access to the bit field NOMCFG. It always reads 0. It is only active during the write access cycle. 0 _B NOMCFG is not changed. 1 _B NOMCFG is updated with the written value. <i>Note: This bit is reset by an application reset.</i>
SUMCFG	[9:8]	rw	Suspend Mode Configuration This bit field defines the kernel mode applied in suspend mode. 0X _B The module is switched on. 1X _B The module is switched off. This field is taken into account for CR = 01. <i>Note: This bit is reset by a debug reset.</i>
BPSUM	11	w	Bit Protection for SUMCFG This bit enables the write access to the bit field SUMCFG. It always reads 0. It is only active during the write access cycle. 0 _B SUMCFG is not changed. 1 _B SUMCFG is updated with the written value. <i>Note: This bit is reset by a debug reset.</i>
COMCFG	[13:12]	rw	Clock Off Mode Configuration This bit field defines the kernel mode applied in clock off mode. 0X _B The module is switched on. 1X _B The module is switched off. This field is taken into account for CR = 10. <i>Note: This bit is reset by an application reset.</i>

Field	Bits	Type	Description
BPCOM	15	w	Bit Protection for COMCFG This bit enables the write access to the bit field COMCFG. It always reads 0. It is only active during the write access cycle. 0 _B COMCFG is not changed. 1 _B COMCFG is updated with the written value. <i>Note: This bit is reset by an application reset.</i>
0	[3:2], 6, 10, 14	r	Reserved; returns 0 if read; should be written with 0;

19.3 Module Implementation

This section describes the connections of the CAPCOM unit to its environment.

19.3.1 Interfaces of the CAPCOM2 Unit

The CAPCOM2 unit is connected to its environment in different ways. These connections are summarized in [Table 19-6](#).

Internal Connections

The overflow/underflow signal T6OFL of GPT2 timer T6 is connected to the CAPCOM2 input T6OUF, providing an optional clock source for the CAPCOM timers.

Synchronous starting is supported by bit SCU_SYSCON1.GLCCST.

Compare output signals can trigger A/D conversions, trigger serial transmissions (USIC), and generate request signals for the external request unit (ERU).

The 18 interrupt request lines of the CAPCOM2 unit are connected to the interrupt control block. The channel interrupt request lines share interrupt nodes with other sources. The selection is done using register SCU_ISSR.

The CAPCOM2 module is clocked with the XC27x8X system clock, so $f_{CC} = f_{SYS}$.

External Connections

Sixteen (twelve in 100-pin package) capture/compare signals of the CAPCOM2 unit are connected with input/output ports of the XC27x8X. Depending on the selected direction, these ports may accept capture trigger signals from the external system or issue compare output signals to external circuitry.

Note: Capture trigger signals may also be derived from output pins. In this case, software can generate the trigger edges, for example.

Timer T7 can be clocked by an external signal.

Table 19-6 CAPCOM2 Connections in XC27x8X

Signal	from/to Module	I/O to CAPCOM2	Can be used to/as
T7IN	P5.9	I	Timer 7 input from port
T8IN	CCU60_SR2	I	CCU60 interrupt request
T6OUF	T6OFL (GPT12)	I	GPT12 timer T6 overflow
T7HR	GLCCST (SCU)	I	Global CAPCOM start
T8HR	GLCCST (SCU)	I	Global CAPCOM start
CC16IO	P2.3	I	Capture/Compare input
	P2.3 ADC0_REQTR0A	O	Capture/Compare output ADC0 request trigger

Table 19-6 CAPCOM2 Connections in XC27x8X (cont'd)

Signal	from/to Module	I/O to CAPCOM2	Can be used to/as
CC17IO	P2.4	I	Capture/Compare input
	P2.4 ADC0_REQTR1A	O	Capture/Compare output ADC0 request trigger
CC18IO	P2.5	I	Capture/Compare input
	P2.5 ADC0_REQTR2A	O	Capture/Compare output ADC0 request trigger
CC19IO	P2.6	I	Capture/Compare input
	P2.6	O	Capture/Compare output
CC20IO	P2.7	I	Capture/Compare input
	P2.7	O	Capture/Compare output
CC21IO	P2.8	I	Capture/Compare input
	P2.8	O	Capture/Compare output
CC22IO	P2.9	I	Capture/Compare input
	P2.9	O	Capture/Compare output
CC23IO	P2.10	I	Capture/Compare input
	P2.10 ERU_3A3	O	Capture/Compare output External Request Select input
CC24IO	P4.0	I	Capture/Compare input
	P4.0 U0C0_DX2E ADC1_REQTR0A	O	Capture/Compare output USIC0 Channel 0 time slot ADC1 request trigger
CC25IO	P4.1	I	Capture/Compare input
	P4.1 U1C0_DX2E ADC1_REQTR1A	O	Capture/Compare output USIC1 Channel 0 time slot ADC1 request trigger
CC26IO	P4.2	I	Capture/Compare input
	P4.2 U2C0_DX2E ADC1_REQTR2A	O	Capture/Compare output USIC2 Channel 0 time slot ADC1 request trigger
CC27IO	P4.3	I	Capture/Compare input
	P4.3	O	Capture/Compare output

Table 19-6 CAPCOM2 Connections in XC27x8X (cont'd)

Signal	from/to Module	I/O to CAPCOM2	Can be used to/as
CC28IO	P4.4	I	Capture/Compare input
	P4.4 ERU_OGU03 U4C0_DX2E	O	Capture/Compare output Interrupt trigger source USIC4 Channel 0 time slot
CC29IO	P4.5	I	Capture/Compare input
	P4.5 ERU_OGU13	O	Capture/Compare output Interrupt trigger source
CC30IO	P4.6	I	Capture/Compare input
	P4.6 ERU_OGU23	O	Capture/Compare output Interrupt trigger source
CC31IO	P4.7	I	Capture/Compare input
	P4.7 ERU_OGU33	O	Capture/Compare output Interrupt trigger source

20 Capture/Compare Unit 6 (CCU6)

The CCU6 is a high-resolution 16-bit capture and compare unit with application specific modes, mainly for AC drive control. Special operating modes support the control of Brushless DC-motors using Hall sensors or Back-EMF detection. Furthermore, block commutation and control mechanisms for multi-phase machines are supported. It also supports inputs to start several timers synchronously, an important feature in devices with several CCU6 modules.

This chapter is structured as follows:

- Introduction (see [Section 20.1](#))
including the register overview (see [Section 20.1.3](#))
- Operating T12 (see [Section 20.2](#))
including T12 related registers (see [Section 20.2.8](#))
and capture/compare control registers (see [Section 20.2.9](#))
- Operating T13 (see [Section 20.3](#))
including T13 related registers (see [Section 20.3.6](#))
- Trap handling (see [Section 20.4](#))
- Multi-Channel mode (see [Section 20.5](#))
- Hall sensor mode (see [Section 20.6](#))
- Modulation control registers (see [Section 20.7](#))
- Interrupt handling (see [Section 20.8](#))
including interrupt registers (see [Section 20.8.2](#))
- General module operation (see [Section 20.9](#))
including general registers (see [Section 20.9.3](#))
- Module implementation (see [Section 20.10](#))

20.1 Introduction

The CCU6 unit is made up of a Timer T12 Block with three capture/compare channels and a Timer T13 Block with one compare channel. The T12 channels can independently generate PWM signals or accept capture triggers, or they can jointly generate control signal patterns to drive AC-motors or inverters.

A rich set of status bits, synchronized updating of parameter values via shadow registers, and flexible generation of interrupt request signals provide means for efficient software-control.

*Note: The capture/compare module itself is named CCU6 (capture/compare unit 6).
A capture/compare channel inside this module is named CC6x.*

20.1.1 Feature Set Overview

This section gives an overview over the different building blocks and their main features.

Timer 12 Block Features

- Three capture/compare channels, each channel can be used either as capture or as compare channel
- Generation of a three-phase PWM supported (six outputs, individual signals for high-side and low-side switches)
- 16-bit resolution, maximum count frequency = peripheral clock
- Dead-time control for each channel to avoid short-circuits in the power stage
- Concurrent update of T12 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Start can be controlled by external events
- Capability of counting external events
- Many interrupt request sources
- Hysteresis-like control mode

Timer 13 Block Features

- One independent compare channel with one output
- 16-bit resolution, maximum count frequency = peripheral clock
- Concurrent update of T13 registers
- Can be synchronized to T12
- Interrupt generation at period-match and compare-match
- Single-shot mode supported
- Start can be controlled by external events
- Capability of counting external events

Additional Specific Functions

- Block commutation for Brushless DC-drives implemented
- Position detection via Hall-sensor pattern
- Noise filter supported for position input signals
- Automatic rotational speed measurement and commutation control for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$)
- Control modes for multi-channel AC-drives
- Output levels can be selected and adapted to the power stage

20.1.2 Block Diagram

The Timer T12 can operate in capture and/or compare mode for its three channels. The modes can also be combined (e.g. a channel operates in compare mode, whereas another channel operates in capture mode). The Timer T13 can operate in compare mode only. The multi-channel control unit generates output patterns which can be modulated by T12 and/or T13. The modulation sources can be selected and combined for the signal modulation.

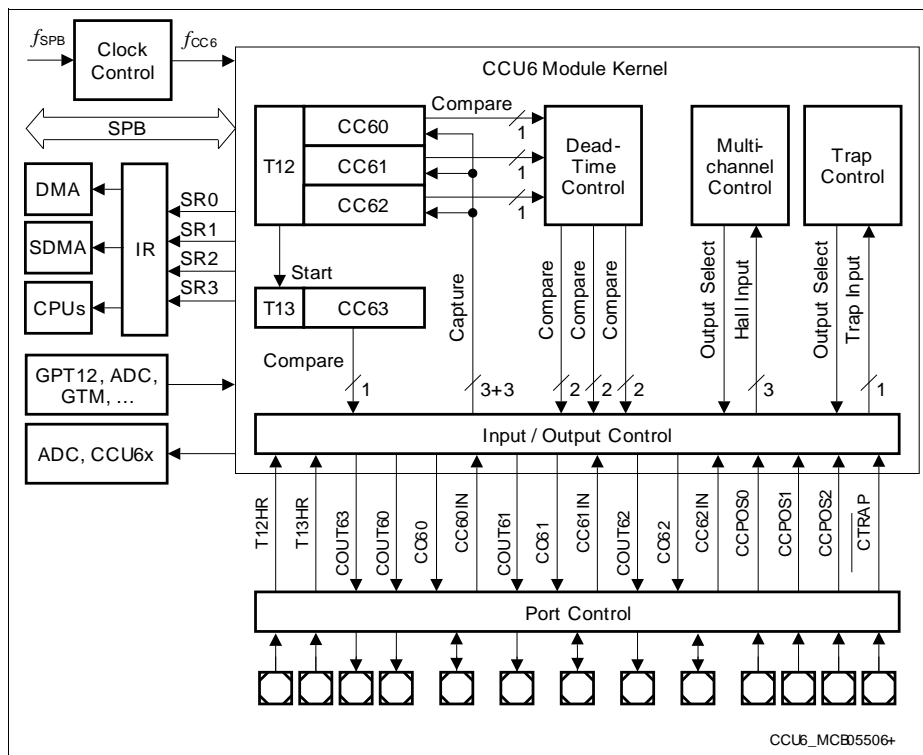


Figure 20-1 CCU6 Block Diagram

20.1.3 Register Overview

For the generation of the overall register table, the prefix "CCU6x_" has to be added to the register names in this table to identify the registers of different CCU6 modules that are implemented. In this naming convention, x indicates the module number.

Table 20-1 shows all registers required for programming of a CCU6 module. It summarizes the CCU6 kernel registers and defines the offset and the reset values. 8-bit short addresses are not available for this module.

T12 related Registers	Cap/Com Control Registers	Interrupt Status/ Control Registers	General Registers
T12	CMPSTAT	IS	KSCFG
T12PR	CMPMODIF	ISS	KSCSR
T12DTC	T12MSEL	ISR	PISELH
CC60R	TCTR0	INP	PISELL
CC60SR	TCTR2	IEN	ID
CC61R	TCTR4	0IC	
CC61SR		1IC	
CC62R		2IC	
CC62SR		3IC	
	Modulation Control Registers		
	MODCTR		
	TRPCTR		
	PSLR		
	MCMCTR		
	MCMOUTS		
	MCMOUT		
T13 related Registers			
T13			
T13PR			
CC63R			
CC63SR			

CCU6_regs2

Figure 20-2 CCU6 Registers

Table 20-1 CCU6 Module Register Summary

Short Name	Description	Offset	Reset Value	See Page
General Registers				
ID	Module Identification Register	08 _H	54XX _H	Page 20-107
PISELL	Module Port Input Select Register	04 _H	0000 _H	Page 20-107
PISELH	Module Port Input Select Register	06 _H	0000 _H	Page 20-109
KSCFG	Kernel State Configuration Register	00 _H	0000 _H	Page 20-112
KSCSR	Kernel State Control Sensitivity Register	0E _H	0000 _H	Page 20-114

Timer T12 related Registers

T12	Timer 12 Counter Register	10 _H	0000 _H	Page 20-32
T12PR	Timer 12 Period Register	12 _H	0000 _H	Page 20-32
T12DTC	Dead-Time Control Register for Timer T12	14 _H	0000 _H	Page 20-35
CC60R	Capture/Compare Register Channel CC60	18 _H	0000 _H	Page 20-33
CC61R	Capture/Compare Register Channel CC61	1A _H	0000 _H	Page 20-33
CC62R	Capture/Compare Register Channel CC62	1C _H	0000 _H	Page 20-33
CC60SR	Capture/Compare Shadow Register Channel CC60	20 _H	0000 _H	Page 20-34
CC61SR	Capture/Compare Shadow Register Channel CC61	22 _H	0000 _H	Page 20-34
CC62SR	Capture/Compare Shadow Register Channel CC62	24 _H	0000 _H	Page 20-34

Capture/Compare Control Registers

CMPSTAT	Compare State Register	28 _H	0000 _H	Page 20-37
CMPMODIF	Compare State Modification Register	2A _H	0000 _H	Page 20-39
T12MSEL	T12 Capture/Compare Mode Select Register	46 _H	0000 _H	Page 20-40
TCTR0	Timer Control Register 0	2C _H	0000 _H	Page 20-41

Table 20-1 CCU6 Module Register Summary (cont'd)

Short Name	Description	Offset	Reset Value	See Page
TCTR2	Timer Control Register 2	2E _H	0000 _H	Page 20-44
TCTR4	Timer Control Register 4	26 _H	0000 _H	Page 20-47

Timer T13 related Registers

T13	Timer 13 Counter Register	30 _H	0000 _H	Page 20-62
T13PR	Timer 13 Period Register	32 _H	0000 _H	Page 20-63
CC63R	Compare Register for Timer 13	34 _H	0000 _H	Page 20-64
CC63SR	Compare Shadow Register for Timer 13	36 _H	0000 _H	Page 20-64

Modulation Control Registers

MODCTR	Modulation Control Register	40 _H	0000 _H	Page 20-78
TRPCTR	Trap Control Register	42 _H	0000 _H	Page 20-80
PSLR	Passive State Level Register	44 _H	0000 _H	Page 20-83
MCMOUTS	Multi-Channel Mode Output Shadow Register	4A _H	0000 _H	Page 20-86
MCMOUT	Multi-Channel Mode Output Register	4C _H	0000 _H	Page 20-87
MCMCTR	Multi-Channel Mode Control Register	4E _H	0000 _H	Page 20-84

Interrupt Status and Node Registers

IS	Interrupt Status Register	50 _H	0000 _H	Page 20-91
ISS	Interrupt Status Set Register	52 _H	0000 _H	Page 20-94
ISR	Interrupt Status Reset Register	54 _H	0000 _H	Page 20-96
INP	Interrupt Node Pointer Register	56 _H	3940 _H	Page 20-101
IEN	Interrupt Node Pointer Register	58 _H	0000 _H	Page 20-98

Note: In the case of a write access to addresses inside the address range (that is covered by the same chip select signal), but that are not the addresses explicitly mentioned for the module, the write access is not taken into account for the module. The same principle is valid for read accesses. In case of a read access to another address, the module does not react.

20.2 Operating Timer T12

The timer T12 block is the main unit to generate the 3-phase PWM signals. A 16-bit counter is connected to 3 channel registers via comparators, that generate a signal when the counter contents match one of the channel register contents. A variety of control functions facilitate the adaptation of the T12 structure to different application needs. Besides the 3-phase PWM generation, the T12 block offers options for individual compare and capture functions, as well as dead-time control and hysteresis-like compare mode.

This section provides information about:

- T12 overview (see [Section 20.2.1](#))
- Counting scheme (see [Section 20.2.2](#))
- Compare modes (see [Section 20.2.3](#))
- Compare mode output path (see [Section 20.2.4](#))
- Capture modes (see [Section 20.2.5](#))
- Shadow transfer (see [Section 20.2.6](#))
- T12 operating mode selection (see [Section 20.2.7](#))
- T12 counter register description (see [Section 20.2.8](#))

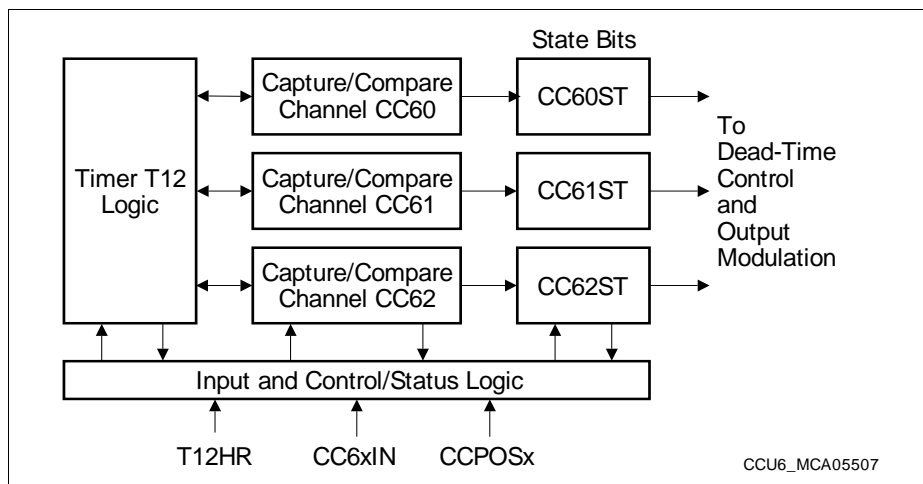


Figure 20-3 Overview Diagram of the Timer T12 Block

20.2.1 T12 Overview

Figure 20-4 shows a detailed block diagram of Timer T12. The functions of the timer T12 block are controlled by bits in registers **TCTR0**, **TCTR2**, **TCTR4**, and **PISELL**.

Timer T12 receives its input clock (f_{T12}) from the module clock f_{CC6} via a programmable prescaler and an optional 1/256 divider or from an input signal T12HR. These options are controlled via bit fields T12CLK and T12PRE (see **Table 20-2**). T12 can count up or down, depending on the selected operation mode. A direction flag, CDIR, indicates the current counting direction.

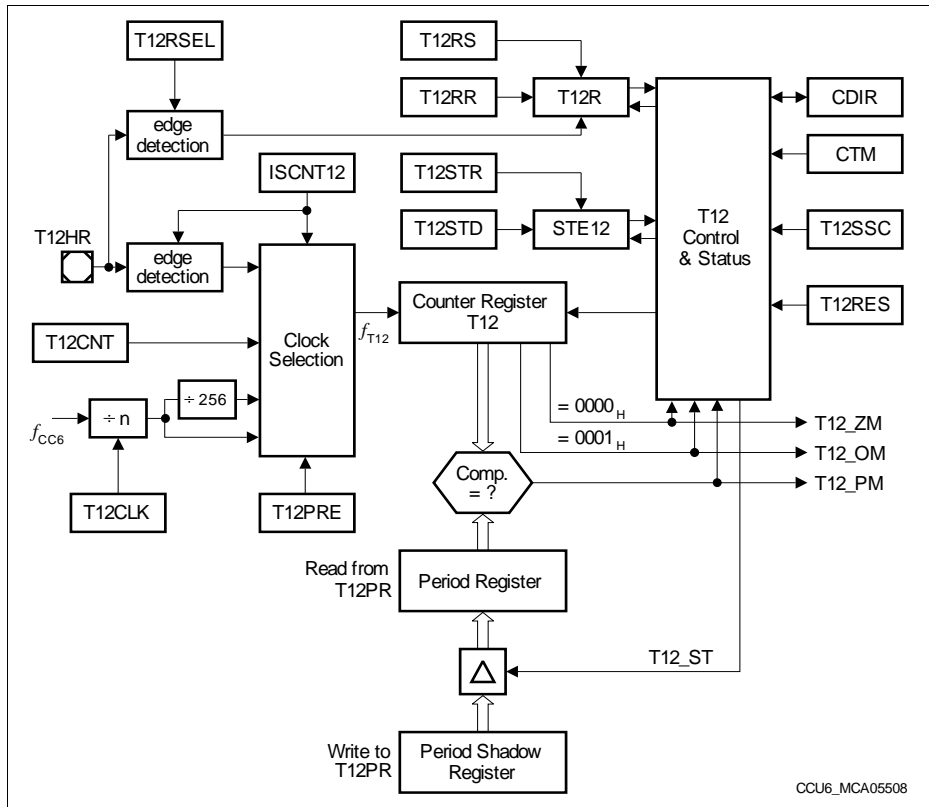


Figure 20-4 Timer T12 Logic and Period Comparators

Via a comparator, the T12 counter register **T12** is connected to a Period Register **T12PR**. This register determines the maximum count value for T12.

In Edge-Aligned mode, T12 is cleared to 0000_H after it has reached the period value defined by T12PR. In Center-Aligned mode, the count direction of T12 is set from 'up' to

'down' after it has reached the period value (please note that in this mode, T12 exceeds the period value by one before counting down). In both cases, signal T12_PM (T12 Period Match) is generated. The Period Register receives a new period value from its Shadow Period Register.

A read access to T12PR delivers the current period value at the comparator, whereas a write access targets the Shadow Period Register to prepare another period value. The transfer of a new period value from the Shadow Period Register into the Period Register (see [Section 20.2.6](#)) is controlled via the 'T12 Shadow Transfer' control signal, T12_ST. The generation of this signal depends on the operating mode and on the shadow transfer enable bit STE12. Providing a shadow register for the period value as well as for other values related to the generation of the PWM signal allows a concurrent update by software for all relevant parameters.

Two further signals indicate whether the counter contents are equal to 0000_H (T12_ZM = zero match) or 0001_H (T12_OM = one match). These signals control the counting and switching behavior of T12.

The basic operating mode of T12, either Edge-Aligned mode ([Figure 20-5](#)) or Center-Aligned mode ([Figure 20-6](#)), is selected via bit CTM. A Single-Shot control bit, T12SSC, enables an automatic stop of the timer when the current counting period is finished (see [Figure 20-7](#) and [Figure 20-8](#)).

The start or stop of T12 is controlled by the Run bit T12R that can be modified by bits in register [TCTR4](#). The run bit can be set/cleared by software via the associated set/clear bits T12RS or T12RR, it can be set by a selectable edge of the input signal T12HR ([TCTR2.T12RSEL](#)), or it is cleared by hardware according to preselected conditions.

The timer T12 run bit T12R must not be set while the applied T12 period value is zero. Timer T12 can be cleared via control bit T12RES. Setting this write-only bit does only clear the timer contents, but has no further effects, for example, it does not stop the timer.

The generation of the T12 shadow transfer control signal, T12_ST, is enabled via bit STE12. This bit can be set or reset by software indirectly through its associated set/clear control bits T12STR and T12STD.

While Timer T12 is running, write accesses to the count register T12 are not taken into account. If T12 is stopped and the Dead-Time counters are 0, write actions to register T12 are immediately taken into account.

20.2.2 T12 Counting Scheme

This section describes the clocking and counting capabilities of T12.

20.2.2.1 Clock Selection

In **Timer Mode** (**PISELH.ISCNT12** = 00_B), the input clock f_{T12} of Timer T12 is derived from the internal module clock f_{CC6} through a programmable prescaler and an optional 1/256 divider. The resulting prescaler factors are listed in **Table 20-2**. The prescaler of T12 is cleared while T12 is not running (**TCTR0.T12R** = 0) to ensure reproducible timings and delays.

Table 20-2 Timer T12 Input Frequency Options

T12CLK	Resulting Input Clock f_{T12} Prescaler Off (T12PRE = 0)	Resulting Input Clock f_{T12} Prescaler On (T12PRE = 1)
000 _B	f_{CC6}	$f_{CC6} / 256$
001 _B	$f_{CC6} / 2$	$f_{CC6} / 512$
010 _B	$f_{CC6} / 4$	$f_{CC6} / 1024$
011 _B	$f_{CC6} / 8$	$f_{CC6} / 2048$
100 _B	$f_{CC6} / 16$	$f_{CC6} / 4096$
101 _B	$f_{CC6} / 32$	$f_{CC6} / 8192$
110 _B	$f_{CC6} / 64$	$f_{CC6} / 16384$
111 _B	$f_{CC6} / 128$	$f_{CC6} / 32768$

In **Counter Mode**, timer T12 counts one step:

- If a 1 is written to **TCTR4.T12CNT** and **PISELH.ISCNT12** = 01_B
- If a rising edge of input signal T12HR is detected and **PISELH.ISCNT12** = 10_B
- If a falling edge of input signal T12HR is detected and **PISELH.ISCNT12** = 11_B

20.2.2.2 Edge-Aligned / Center-Aligned Mode

In **Edge-Aligned Mode** (CTM = 0), timer T12 is always counting upwards (CDIR = 0). When reaching the value given by the period register (period-match T12_PM), the value of T12 is cleared with the next counting step (saw tooth shape).

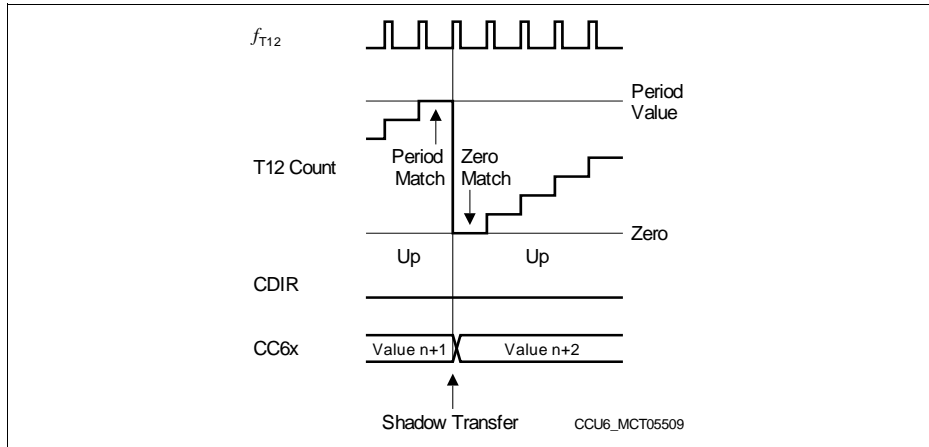


Figure 20-5 T12 Operation in Edge-Aligned Mode

As a result, in Edge-Aligned mode, the timer period is given by:

$$T12_{PER} = \langle \text{Period-Value} \rangle + 1; \text{ in } T12 \text{ clocks } (f_{T12}) \quad (20.1)$$

In **Center-Aligned Mode** (CTM = 1), timer T12 is counting upwards or downwards (triangular shape). When reaching the value given by the period register (period-match T12_PM) while counting upwards (CDIR = 0), the counting direction control bit CDIR is changed to downwards (CDIR = 1) with the next counting step.

When reaching the value 0001_H (one-match T12_OM) while counting downwards, the counting direction control bit CDIR is changed to upwards with the next counting step.

As a result, in Center-Aligned mode, the timer period is given by:

$$T12_{PER} = (\langle \text{Period-Value} \rangle + 1) \times 2; \text{ in } T12 \text{ clocks } (f_{T12}) \quad (20.2)$$

- With the next clock event of f_{T12} the count direction is set to counting up (CDIR = 0) when the counter reaches 0001_H while counting down.
- With the next clock event of f_{T12} the count direction is set to counting down (CDIR = 1) when the Period-Match is detected while counting up.
- With the next clock event of f_{T12} the counter counts up while CDIR = 0 and it counts down while CDIR = 1.

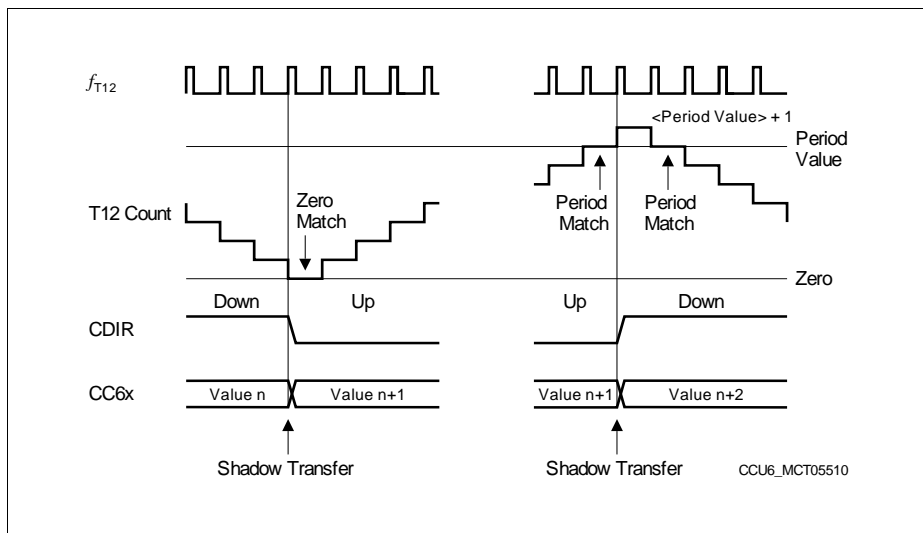


Figure 20-6 T12 Operation in Center-Aligned Mode

Note: Bit CDIR changes with the next timer clock event after the one-match or the period-match. Therefore, the timer continues counting in the previous direction for one cycle before actually changing its direction (see [Figure 20-6](#)).

20.2.2.3 Single-Shot Mode

In Single-Shot Mode, the timer run bit T12R is cleared by hardware. If bit T12SSC = 1, the timer T12 will stop when the current timer period is finished.

In Edge-Aligned mode, T12R is cleared when the timer becomes zero after having reached the period value (see [Figure 20-7](#)).

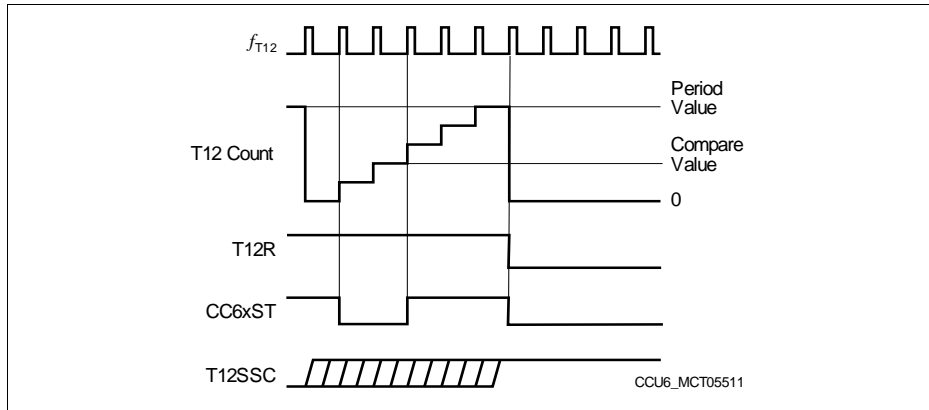


Figure 20-7 Single-Shot Operation in Edge-Aligned Mode

In Center-Aligned mode, the period is finished when the timer has counted down to zero (one clock cycle after the one-match while counting down, see [Figure 20-8](#)).

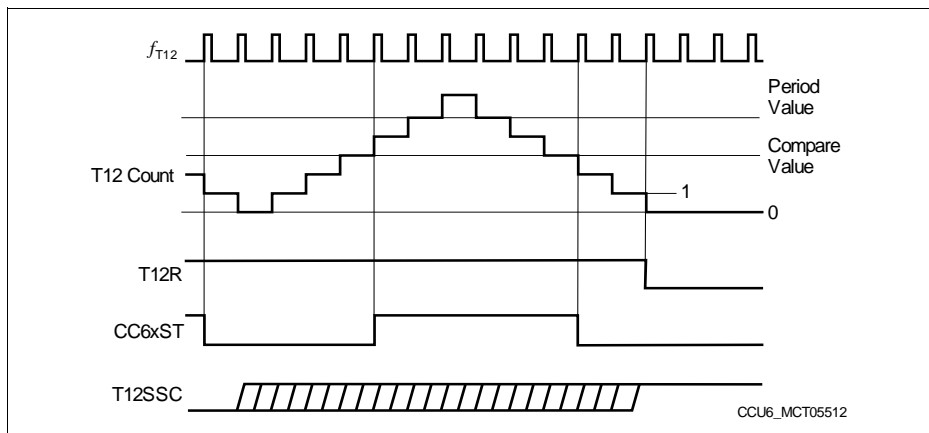


Figure 20-8 Single-Shot Operation in Center-Aligned Mode

20.2.3 T12 Compare Mode

Associated with Timer T12 are three individual capture/compare channels, that can perform compare or capture operations with regard to the contents of the T12 counter. The capture functions are explained in [Section 20.2.5](#).

20.2.3.1 Compare Channels

In Compare Mode (see [Figure 20-9](#)), the three individual compare channels CC60, CC61, and CC62 can generate a three-phase PWM pattern.

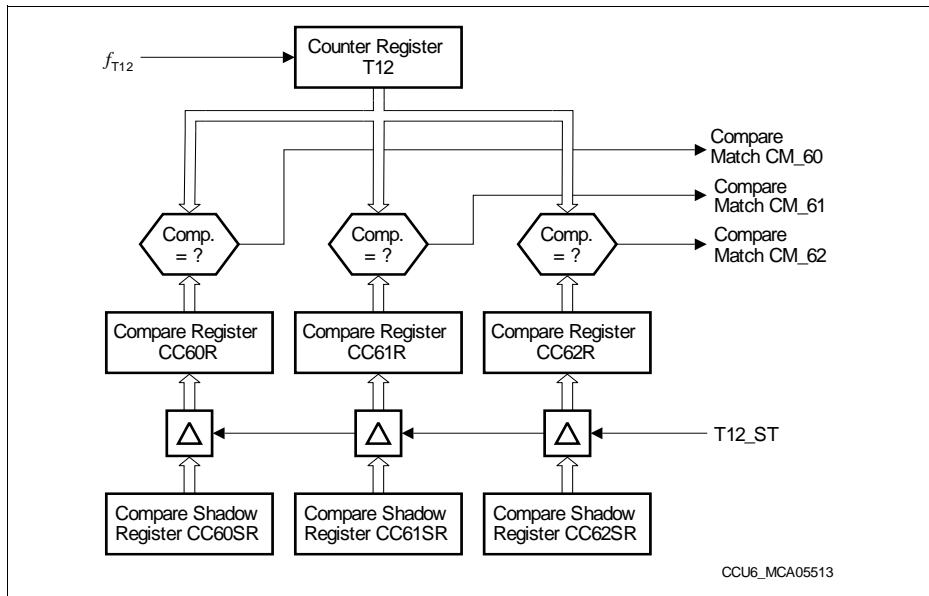


Figure 20-9 T12 Channel Comparators

Each compare channel is connected to the T12 counter register via its individual equal-to comparator, generating a match signal when the contents of the counter matches the contents of the associated compare register. Each channel consists of the comparator and a double register structure - the actual compare register CC6xR, feeding the comparator, and an associated shadow register CC6xSR, that is preloaded by software and transferred into the compare register when signal T12 shadow transfer, T12_ST, gets active. Providing a shadow register for the compare value as well as for other values related to the generation of the PWM signal facilitates a concurrent update by software for all relevant parameters of a three-phase PWM.

20.2.3.2 Channel State Bits

Associated with each (compare) channel is a State Bit, **CMPSTAT.CC6xST**, holding the status of the compare (or capture) operation (see **Figure 20-10**). In compare mode, the State Bits are modified according to a set of switching rules, depending on the current status of timer T12.

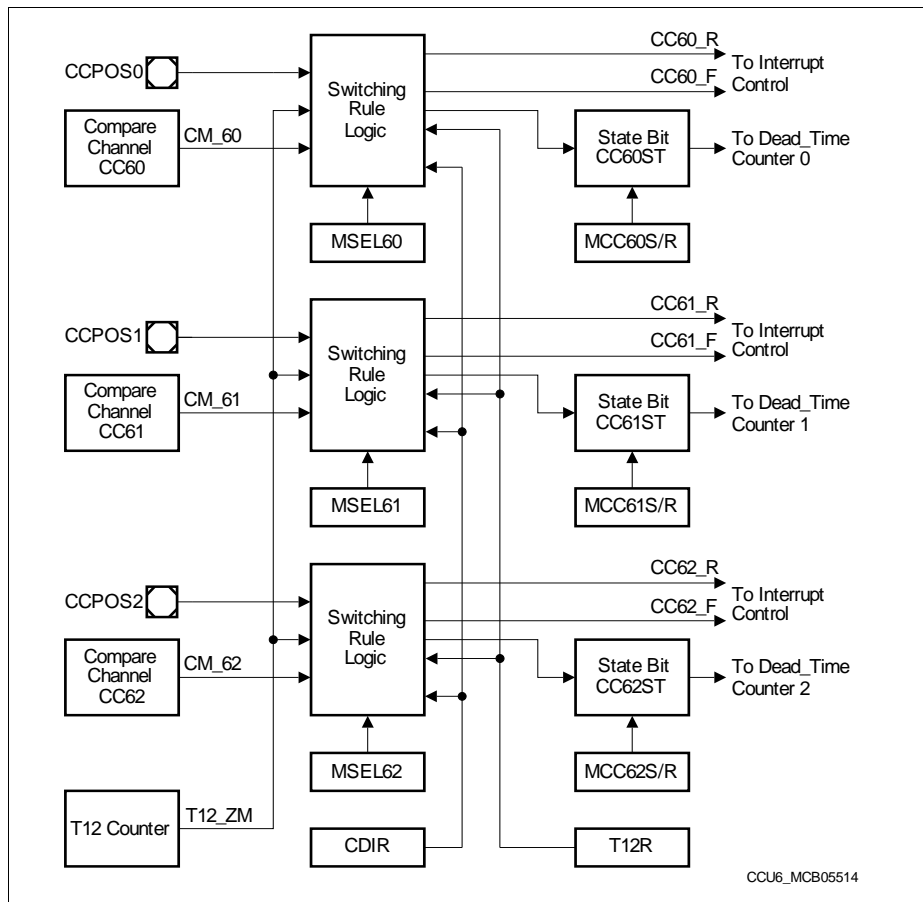


Figure 20-10 Compare State Bits for Compare Mode

The inputs to the switching rule logic for the CC6xST bits are the timer direction (CDIR), the timer run bit (T12R), the timer T12 zero-match signal (T12_ZM), and the actual individual compare-match signals CM_6x as well as the mode control bits, **T12MSEL.MSEL6x**.

Capture/Compare Unit 6 (CCU6)

In addition, each state bit can be set or cleared by software via the appropriate set and reset bits in register **CMPMODIF**, MCC6xS and MCC6xR. The input signals CCPOSx are used in hysteresis-like compare mode, whereas in normal compare mode, these inputs are ignored.

Note: In Hall Sensor, single shot or capture modes, additional/different rules are taken into account (see related sections).

A compare interrupt event CC6x_R is signaled when a compare match is detected while counting upwards, whereas the compare interrupt event CC6x_F is signaled when a compare match is detected while counting down. The actual setting of a State Bit has no influence on the interrupt generation in compare mode.

A modification of a State Bit CC6xST by the switching rule logic due to a compare action is only possible while Timer T12 is running ($T12R = 1$). If this is the case, the following switching rules apply for setting and clearing the State Bits in Compare Mode (illustrated in **Figure 20-11** and **Figure 20-12**):

A State Bit **CC6xST** is **set** to 1:

- with the next T12 clock (f_{T12}) after a compare-match when T12 is counting up (i.e., when the counter is incremented above the compare value);
- with the next T12 clock (f_{T12}) after a zero-match AND a parallel compare-match when T12 is counting up.

A State Bit **CC6xST** is **cleared** to 0:

- with the next T12 clock (f_{T12}) after a compare-match when T12 is counting down (i.e., when the counter is decremented below the compare value in center-aligned mode);
- with the next T12 clock (f_{T12}) after a zero-match AND NO parallel compare-match when T12 is counting up.

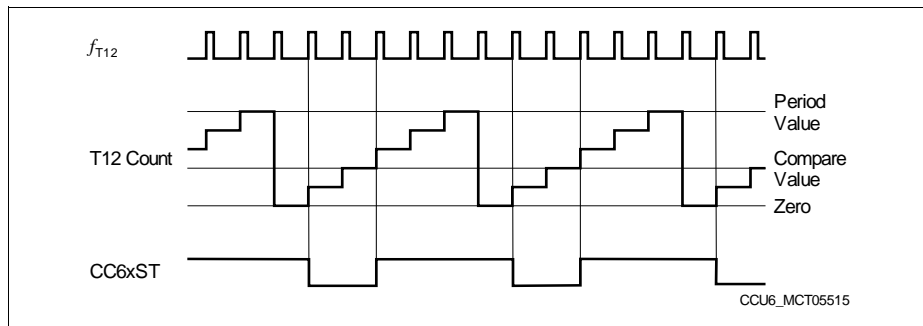


Figure 20-11 Compare Operation, Edge-Aligned Mode

Figure 20-13 illustrates some more examples for compare waveforms. It is important to note that in these examples, it is assumed that some of the compare values are changed

Capture/Compare Unit 6 (CCU6)

while the timer is running. This change is performed via a software preload of the Shadow Register, CC6xSR. The value is transferred to the actual Compare Register CC6xR with the T12 Shadow Transfer signal, T12_ST, that is assumed to be enabled.

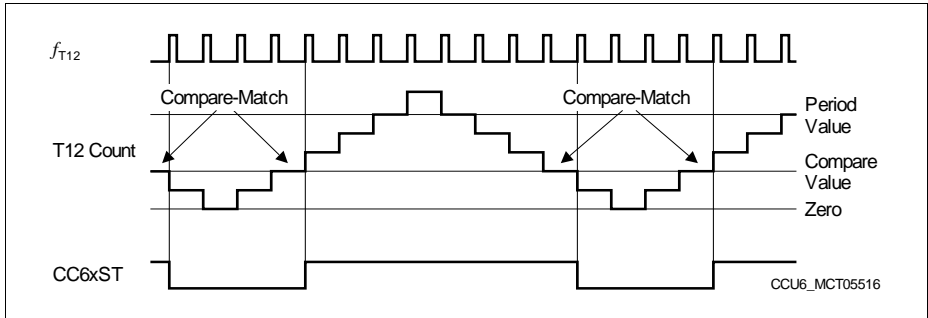


Figure 20-12 Compare Operation, Center-Aligned Mode

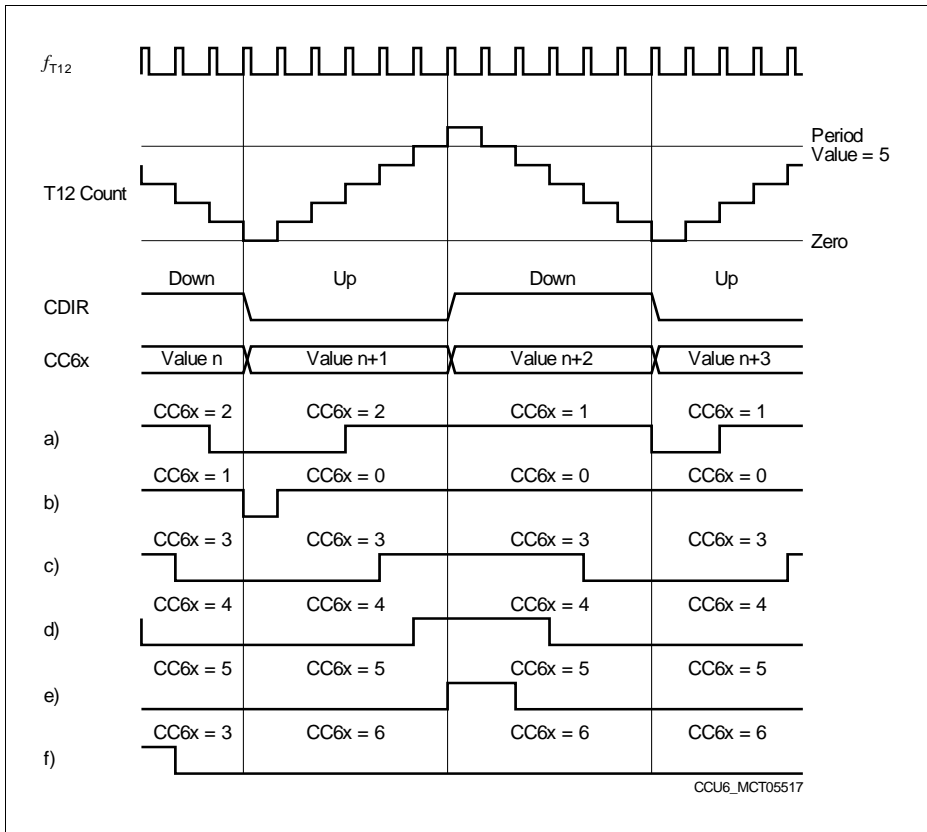


Figure 20-13 Compare Waveform Examples

Example b) illustrates the transition to a duty cycle of 100%. First, a compare value of 0001_H is used, then changed to 0000_H . Please note that a low pulse with the length of one T12 clock is still produced in the cycle where the new value 0000_H is in effect; this pulse originates from the previous value 0001_H . In the following timer cycles, the State Bit CC6xST remains at 1, producing a 100% duty cycle signal. In this case, the compare rule 'zero-match AND compare-match' is in effect.

Example f) shows the transition to a duty cycle of 0%. The new compare value is set to $\langle \text{Period-Value} \rangle + 1$, and the State Bit CC6ST remains cleared.

Figure 20-14 illustrates an example for the waveforms of all three channels. With the appropriate dead-time control and output modulation, a very efficient 3-phase PWM signal can be generated.

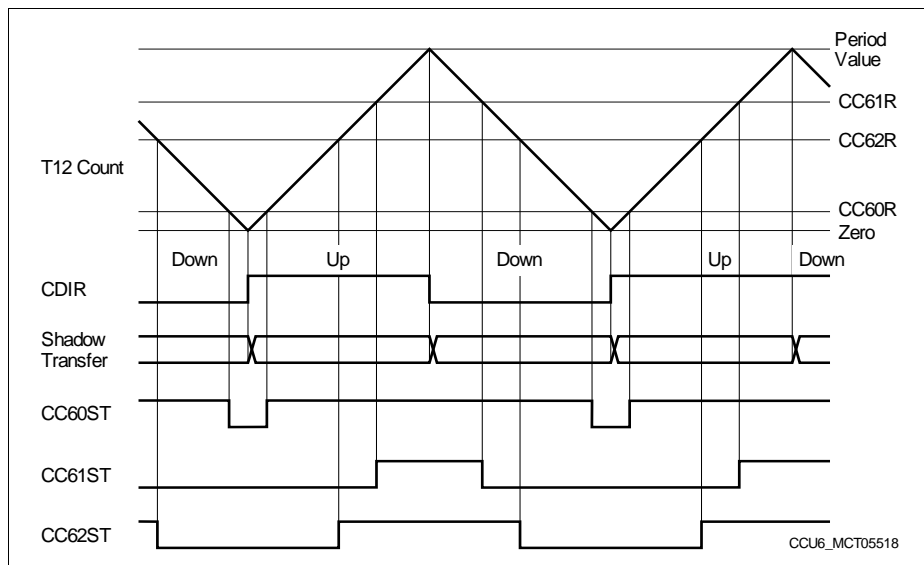


Figure 20-14 Three-Channel Compare Waveforms

20.2.3.3 Hysteresis-Like Control Mode

The hysteresis-like control mode (**T12MSEL**.MSEL6x = 1001_B) offers the possibility to switch off the PWM output if the input CCPOSx becomes 0 by clearing the State Bit CC6xST. This can be used as a simple motor control feature by using a comparator indicating, e.g., overcurrent. While CCPOSx = 0, the PWM outputs of the corresponding channel are driving their passive levels, because the setting of bit CC6xST is only possible while CCPOSx = 1.

As long as input CCPOSx is 0, the corresponding State Bit is held 0. When CCPOSx is at high level, the outputs can be in active state and are determined by bit CC6xST (see **Figure 20-10** for the state bit logic and **Figure 20-15** for the output paths).

The CCPOSx inputs are evaluated with f_{CC6} .

This mode can be used to introduce a timing-related behavior to a hysteresis controller. A standard hysteresis controller detects if a value exceeds a limit and switches its output according to the compare result. Depending on the operating conditions, the switching frequency and the duty cycle are not fixed, but change permanently.

If (outer) time-related control loops based on a hysteresis controller in an inner loop should be implemented, the outer loops show a better behavior if they are synchronized to the inner loops. Therefore, the hysteresis-like mode can be used, that combines timer-related switching with a hysteresis controller behavior. For example, in this mode, an output can be switched on according to a fixed time base, but it is switched off as soon as a falling edge is detected at input CCPOSx.

This mode can also be used for standard PWM with overcurrent protection. As long as there is no low level signal at pin CCPOSx, the output signals are generated in the normal manner as described in the previous sections. Only if input CCPOSx shows a low level, e.g. due to the detection of overcurrent, the outputs are shut off to avoid harmful stress to the system.

20.2.4 Compare Mode Output Path

Figure 20-15 gives an overview on the signal path from a channel State Bit to its output pin in its simplest form. As illustrated, a user has a variety of controls to determine the desired output signal switching behavior in relation to the current state of the State Bit, CC6xST. Please refer to [Section 20.2.4.3](#) for details on the output modulation.

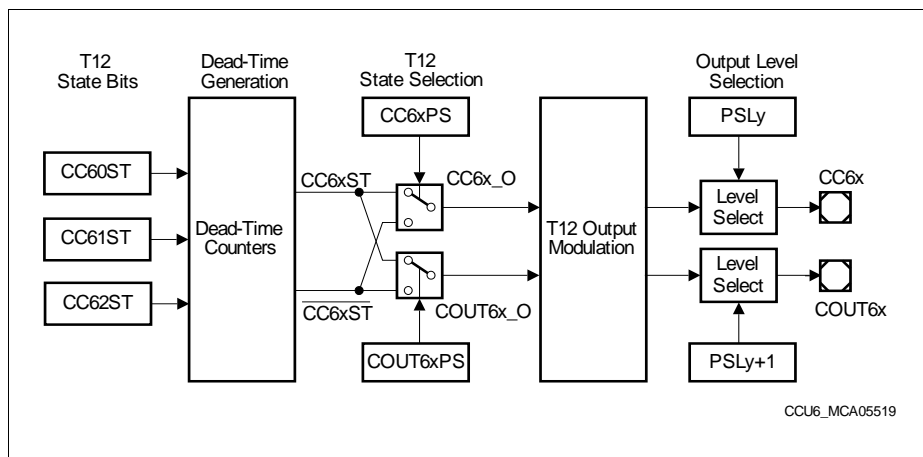


Figure 20-15 Compare Mode Simplified Output Path Diagram

The output path is based on signals that are defined as active or passive. The terms active and passive are not related to output levels, but to internal actions. This mainly applies for the modulation, where T12 and T13 signals are combined with the multi-channel signals and the trap function. The Output level Selection allows the user to define the output level at the output pin for the passive state (inverted level for the active state). It is recommended to configure this block in a way that an external power switch is switched off while the CCU6 delivers an output signal in the passive state.

20.2.4.1 Dead-Time Generation

The generation of (complementary) signals for the high-side and the low-side switches of one power inverter phase is based on the same compare channel. For example, if the high-side switch should be active while the T12 counter value is above the compare value (State Bit = 1), then the low-side switch should be active while the counter value is below the compare value (State Bit = 0).

In most cases, the switching behavior of the connected power switches is not symmetrical concerning the switch-on and switch-off times. A general problem arises if the time for switch-on is smaller than the time for switch-off of the power device. In this case, a short-circuit can occur in the inverter bridge leg, which may damage the complete system. In order to solve this problem by HW, this capture/compare unit

contains a programmable Dead-Time Generation Block, that delays the passive to active edge of the switching signals by a programmable time (the active to passive edge is not delayed).

The Dead-Time Generation Block, illustrated in **Figure 20-16**, is built in a similar way for all three channels of T12. It is controlled by bits in register **T12DTC**. Any change of a CC6xST State Bit activates the corresponding Dead-Time Counter, that is clocked with the same input clock as T12 (f_{T12}). The length of the dead-time can be programmed by bit field DTM. This value is identical for all three channels. Writing **TCTR4.DTRES = 1** sets all dead-times to passive.

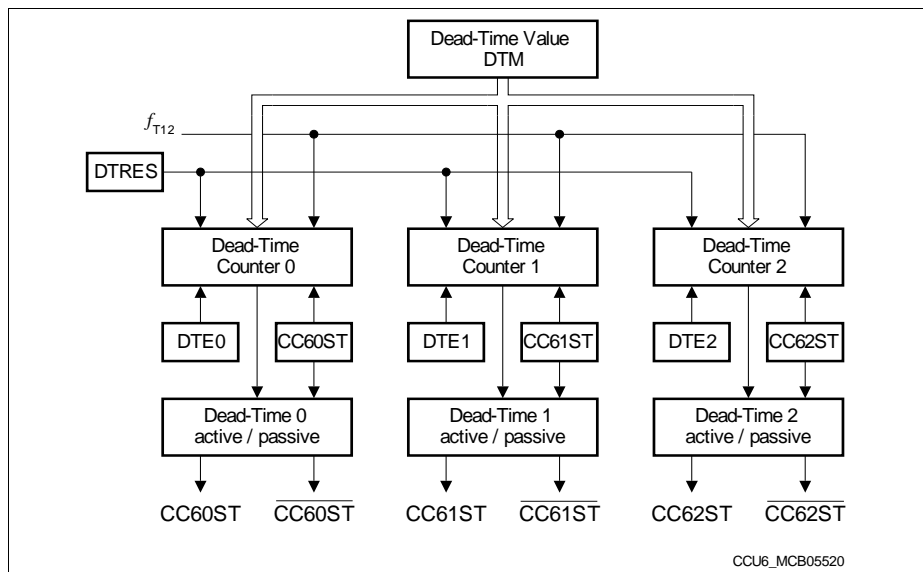


Figure 20-16 Dead-Time Generation Block Diagram

Each of the three dead-time counters has its individual dead-time enable bit, DTE_x. An enabled dead-time counter generates a dead-time delaying the passive-to-active edge of the channel output signal. The change in a State Bit CC6xST is not taken into account while the dead-time generation of this channel is currently in progress (active). This avoids an unintentional additional dead-time if a State Bit CC6xST changes too early. A disabled dead-time counter is always considered as passive and does not delay any edge of CC6xST.

Based on the State Bits CC6xST, the Dead-Time Generation Block outputs a direct signal CC6xST and an inverted signal $\overline{\text{CC6xST}}$ for each compare channel, each masked with the effect of the related Dead-Time Counters (waveforms illustrated in **Figure 20-17**).

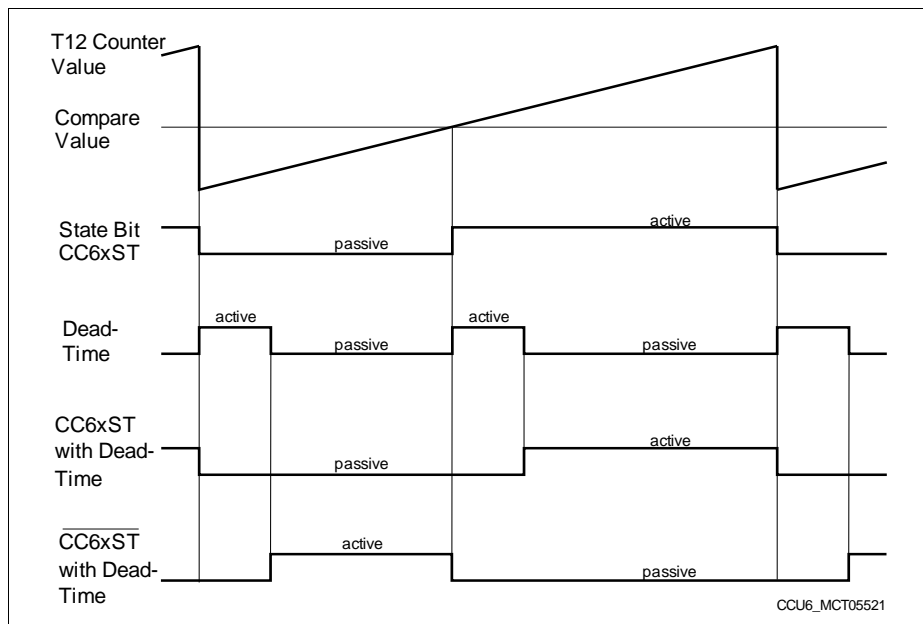


Figure 20-17 Dead-Time Generation Waveforms

20.2.4.2 State Selection

To support a wide range of power switches and drivers, the state selection offers the flexibility to define when a an output can be active and can be modulated, especially useful for **complementary or multi-phase PWM** signals.

The state selection is based on the signals CC6xST and $\overline{\text{CC6xST}}$ delivered by the dead-time generator (see [Figure 20-15](#)). Both signals are never active at the same time, but can be passive at the same time. This happens during the dead-time of each compare channel after a change of the corresponding State Bit CC6xST.

The user can select independently for each output signal CC6xO and COUT6xO if it should be active before or after the compare value has been reached (see register [CMPSTAT](#)). With this selection, the active (conducting) phases of complementary power switches in a power inverter bridge leg can be positioned with respect to the compare value (e.g. signal CC6xO can be active before, whereas COUT6xO can be active after the compare value is reached). Like this, the output modulation, the trap logic and the output level selection can be programmed independently for each output signal, although two output signals are referring to the same compare channel.

20.2.4.3 Output Modulation and Level Selection

The last block of the data path is the Output Modulation block. Here, all the modulation sources and the trap functionality are combined and control the actual level of the output pins (controlled by the modulation enable bits T1xMODENy and MCMEN in register **MODCTR**). The following signal sources can be combined here **for each T12 output signal** (see **Figure 20-18** for compare channel CC60):

- A **T12 related compare signal** CC6x_O (for outputs CC6x) or COUT6x_O (for outputs COUT6x) delivered by the T12 block (state selection with dead-time) with an individual enable bit T12MODENy per output signal (y = 0, 2, 4 for outputs CC6x and y = 1, 3, 5 for outputs COUT6x)
- The **T13 related compare signal** CC63_O delivered by the T13 state selection with an individual enable bit T13MODENy per output signal (y = 0, 2, 4 for outputs CC6x and y = 1, 3, 5 for outputs COUT6x)
- A **multi-channel output signal** MCMPy (y = 0, 2, 4 for outputs CC6x and y = 1, 3, 5 for outputs COUT6x) with a common enable bit MCMEN
- The **trap state** TRPS with an individual enable bit TRPENy per output signal (y = 0, 2, 4 for outputs CC6x and y = 1, 3, 5 for outputs COUT6x)

If one of the modulation input signals CC6x_O/COUT6x_O, CC63_O, or MCMPy of an output modulation block is enabled and is at passive state, the modulated is also in passive state, regardless of the state of the other signals that are enabled. Only if all enabled signals are in active state the modulated output shows an active state. If no modulation input is enabled, the output is in passive state.

If the Trap State is active (TRPS = 1), then the outputs that are enabled for the trap signal (by TRPENy = 1) are set to the passive state.

The output of each of the modulation control blocks is connected to a level select block that is configured by register **PSLR**. It offers the option to determine the actual output level of a pin, depending on the state of the output line (decoupling of active/passive state and output polarity) as specified by the Passive State Select bit PSLy. If the modulated output signal is in the passive state, the level specified directly by PSLy is output. If it is in the active state, the inverted level of PSLy is output. This allows the user to adapt the polarity of an active output signal to the connected circuitry.

The PSLy bits have shadow registers to allow for updates without undesired pulses on the output lines. The bits related to CC6x and COUT6x (x = 0, 1, 2) are updated with the T12 shadow transfer signal (T12_ST). A read action returns the actually used values, whereas a write action targets the shadow bits. Providing a shadow register for the PSL value as well as for other values related to the generation of the PWM signal facilitates a concurrent update by software for all relevant parameters.

Figure 20-18 shows the output modulation structure for compare channel CC60 (output signals CC60 and COUT60). A similar structure is implemented for the other two compare channels CC61 and CC62.

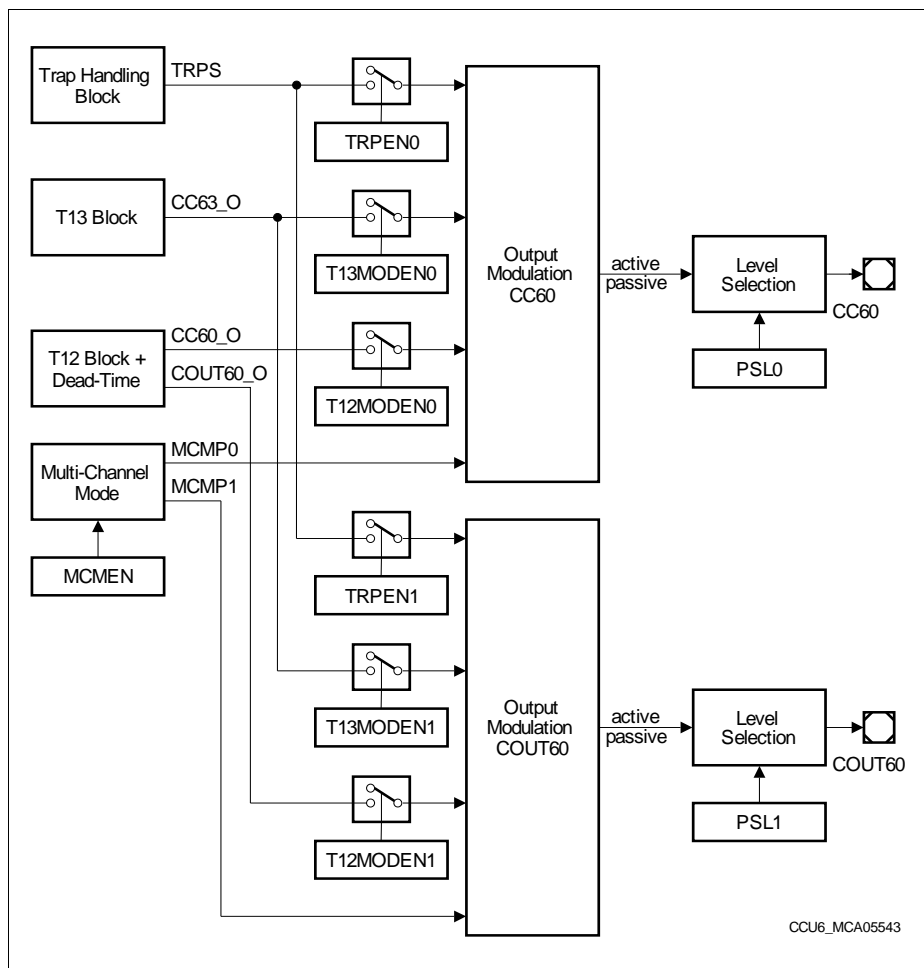


Figure 20-18 Output Modulation for Compare Channel CC60

20.2.5 T12 Capture Modes

Each of the three channels of the T12 Block can also be used to capture T12 time information in response to an external signal CC6xIN.

In capture mode, the interrupt event CC6x_R is detected when a rising edge is detected at the input CC6xIN, whereas the interrupt event CC6x_F is detected when a falling edge is detected.

There are a number of different modes for capture operation. In all modes, both of the registers of a channel are used. The selection of the capture modes is done via the **T12MSEL**. MSEL6x bit fields and can be selected individually for each of the channels.

Table 20-3 Capture Modes Overview

MSEL6x	Mode	Signal	Active Edge	CC6nSR Stored in	T12 Stored in
0100 _B	1	CC6xIN	Rising	–	CC6xR
		CC6xIN	Falling	–	CC6xSR
0101 _B	2	CC6xIN	Rising	CC6xR	CC6xSR
0110 _B	3	CC6xIN	Falling	CC6xR	CC6xSR
0111 _B	4	CC6xIN	Any	CC6xR	CC6xSR

Figure 20-19 illustrates **Capture Mode 1**. When a rising edge (0-to-1 transition) is detected at the corresponding input signal CC6xIN, the current contents of Timer T12 are captured into register CC6xR. When a falling edge (1-to-0 transition) is detected at the input signal CC6xIN, the contents of Timer T12 are captured into register CC6xSR.

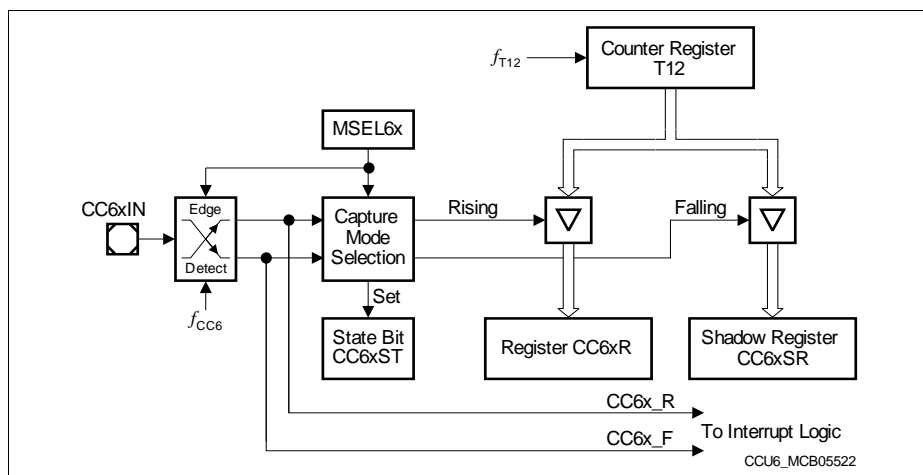


Figure 20-19 Capture Mode 1 Block Diagram

Capture/Compare Unit 6 (CCU6)

Capture Modes 2, 3 and 4 are shown in **Figure 20-20**. They differ only in the active edge causing the capture operation. In each of the three modes, when the selected edge is detected at the corresponding input signal CC6xIN, the current contents of the shadow register CC6xSR are transferred into register CC6xR, and the current Timer T12 contents are captured in register CC6xSR (simultaneous transfer). The active edge is a rising edge of CC6xIN for Capture Mode 2, a falling edge for Mode 3, and both, a rising or a falling edge for Capture Mode 4, as shown in **Table 20-3**. These capture modes are very useful in cases where there is little time between two consecutive edges of the input signal.

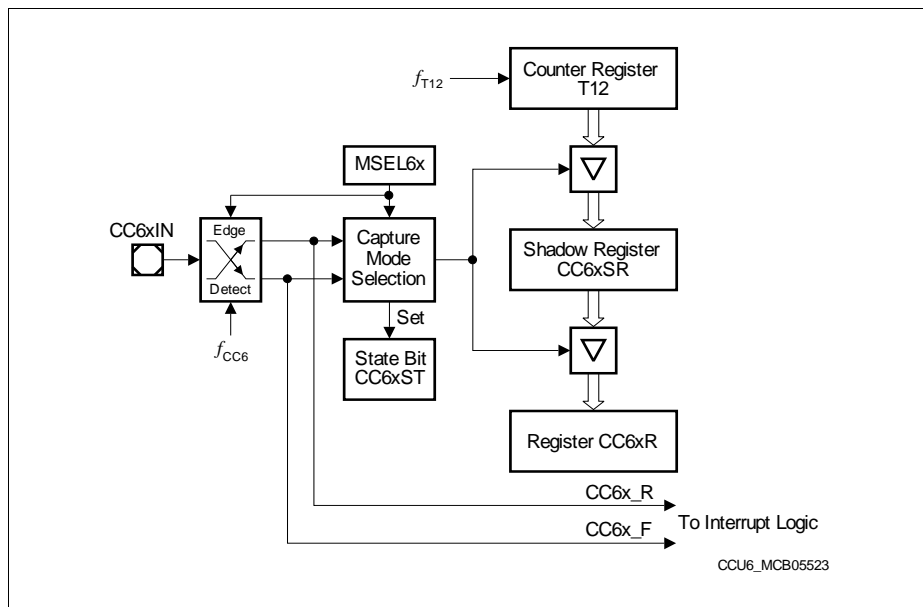


Figure 20-20 Capture Modes 2, 3 and 4 Block Diagram

Capture/Compare Unit 6 (CCU6)

Five further capture modes are called **Multi-Input Capture Modes**, as they use two different external inputs, signal CC6xIN and signal CCPOSx.

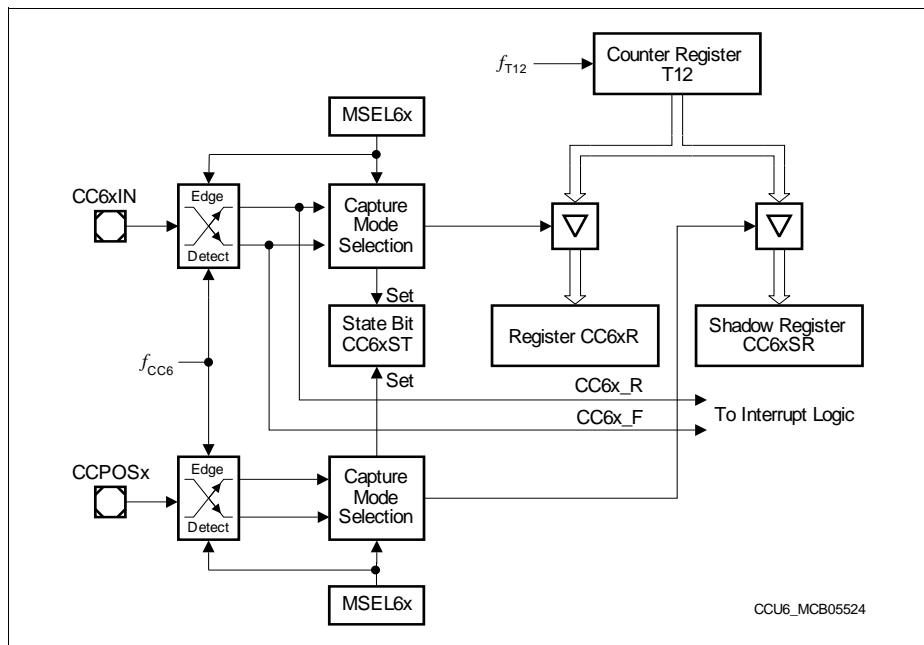


Figure 20-21 Multi-Input Capture Modes Block Diagram

In each of these modes, the current T12 contents are captured in register CC6xR in response to a selected event at signal CC6xIN, and in register CC6xSR in response to a selected event at signal CCPOSx. The possible events can be opposite input transitions, or the same transitions, or any transition at the two inputs. The different options are detailed in [Table 20-4](#).

In each of the various capture modes, the Channel State Bit, CC6xST, is set to 1 when the selected capture trigger event at signal CC6xIN or CCPOSx has occurred. The State Bit is not cleared by hardware, but can be cleared by software.

In addition, appropriate signal lines to the interrupt logic are activated, that can generate an interrupt request to the CPU. Regardless of the selected active edge, all edges detected at signal CC6xIN can lead to the activation of the appropriate interrupt request line (see also [Section 20.8](#)).

Table 20-4 Multi-Input Capture Modes Overview

MSEL6x	Mode	Signal	Active Edge	T12 Stored in
1010 _B	5	CC6xIN	Rising	CC6xR
		CCPOSx	Falling	CC6xSR
1011 _B	6	CC6xIN	Falling	CC6xR
		CCPOSx	Rising	CC6xSR
1100 _B	7	CC6xIN	Rising	CC6xR
		CCPOSx	Rising	CC6xSR
1101 _B	8	CC6xIN	Falling	CC6xR
		CCPOSx	Falling	CC6xSR
1110 _B	9	CC6xIN	Any	CC6xR
		CCPOSx	Any	CC6xSR
1111 _B	—	reserved (no capture or compare action)		

20.2.6 T12 Shadow Register Transfer

A special shadow transfer signal (T12_ST) can be generated to facilitate updating the period and compare values of the compare channels CC60, CC61, and CC62 synchronously to the operation of T12. Providing a shadow register for values defining one PWM period facilitates a concurrent update by software for all relevant parameters. The next PWM period can run with a new set of parameters. The generation of this signal is requested by software via bit **TCTR0.STE12** (set by writing 1 to the write-only bit **TCTR4.T12STR**, cleared by writing 1 to the write-only bit **TCTR4.T12STD**).

Figure 20-22 shows the shadow register structure and the shadow transfer signals, as well as on the read/write accessibility of the various registers.

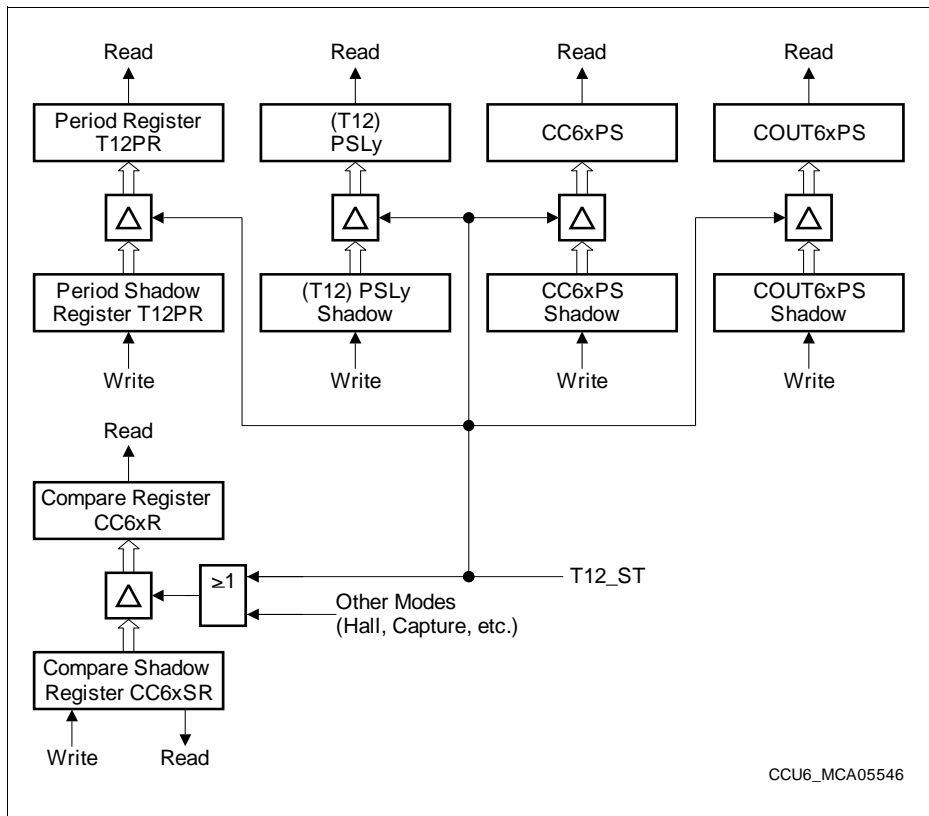


Figure 20-22 T12 Shadow Register Overview

A T12 shadow register transfer takes place (T12_ST active):

- while timer T12 is not running (T12R = 0), or
- STE12 = 1 and a Period-Match is detected while counting up, or
- STE12 = 1 and a One-Match is detected while counting down

When signal T12_ST is active, a shadow register transfer is triggered with the next cycle of the T12 clock. Bit STE12 is automatically cleared with the shadow register transfer.

20.2.7 Timer T12 Operating Mode Selection

The operating mode for the T12 channels are defined by the bit fields **T12MSEL.MSEL6x**.

Table 20-5 T12 Capture/Compare Modes Overview

MSEL6x	Selected Operating Mode
0000 _B , 1111 _B	Capture/Compare modes switched off
0001 _B , 0010 _B , 0011 _B	Compare mode, see Section 20.2.3 same behavior for all three codings
01XX _B	Double-Register Capture modes, see Section 20.2.5
1000 _B	Hall Sensor Mode, see Section 20.6 In order to properly enable this mode, all three MSEL6x fields have to be programmed to Hall Sensor mode.
1001 _B	Hysteresis-like compare mode, see Section 20.2.3.3
1010 _B , 1011 _B , 1100 _B , 1101 _B , 1110 _B	Multi-Input Capture modes, see Section 20.2.5

The clocking and counting scheme of the timers are controlled by the timer control registers **TCTR0** and **TCTR2**. Specific actions are triggered by write operations to register **TCTR4**.

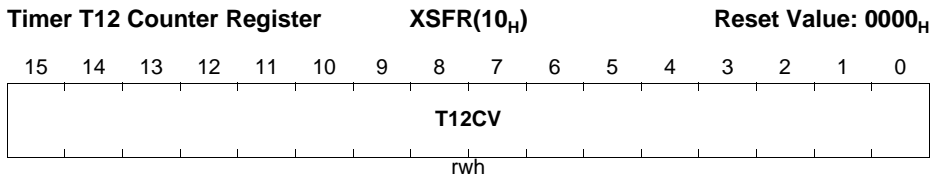
20.2.8 T12 related Registers

20.2.8.1 T12 Counter Register

Register T12 represents the counting value of timer T12. It can only be written while the timer T12 is stopped. Write actions while T12 is running are not taken into account. Register T12 can always be read by SW.

In edge-aligned mode, T12 only counts up, whereas in center-aligned mode, T12 can count up and down.

T12



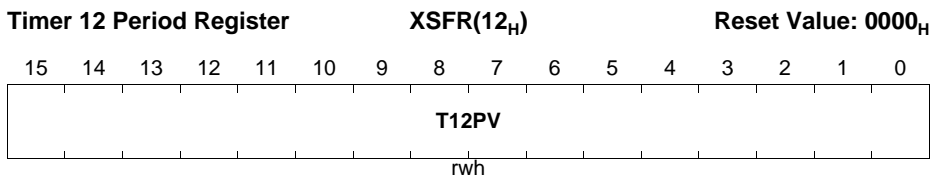
Field	Bits	Type	Description
T12CV	[15:0]	rwh	Timer 12 Counter Value This register represents the 16-bit counter value of Timer12.

Note: While timer T12 is stopped, the internal clock divider is reset in order to ensure reproducible timings and delays.

20.2.8.2 Period Register

Register T12PR contains the period value for timer T12. The period value is compared to the actual counter value of T12 and the resulting counter actions depend on the defined counting rules. This register has a shadow register and the shadow transfer is controlled by bit STE12. A read action by SW delivers the value that is currently used for the compare action, whereas the write action targets a shadow register. The shadow register structure allows a concurrent update of all T12-related values.

T12PR



Field	Bits	Type	Description
T12PV	[15:0]	rwh	T12 Period Value The value T12PV defines the counter value for T12 leading to a period-match. When reaching this value, the timer T12 is set to zero (edge-aligned mode) or changes its count direction to down counting (center-aligned mode).

20.2.8.3 Capture/Compare Registers

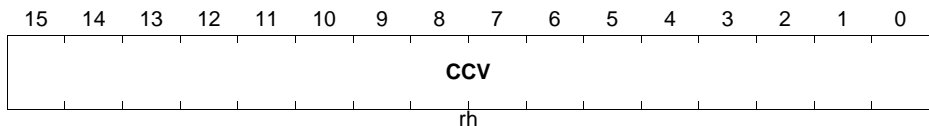
In compare mode, the registers CC6xR (x = 0 - 2) are the actual compare registers for T12. The values stored in CC6xR are compared (all three channels in parallel) to the counter value of T12. In capture mode, the current value of the T12 counter register is captured by registers CC6xR if the corresponding capture event is detected.

CC6xR (x = 0-2)

Capture/Compare Register for Channel CC6x

XSFR(18_H + 2*x)

Reset Value: 0000_H



Field	Bits	Type	Description
CCV	[15:0]	rh	Capture/Compare Value In compare mode, the bit fields CCV contain the values, that are compared to the T12 counter value. In capture mode, the captured value of T12 can be read from these registers.

20.2.8.4 Capture/Compare Shadow Registers

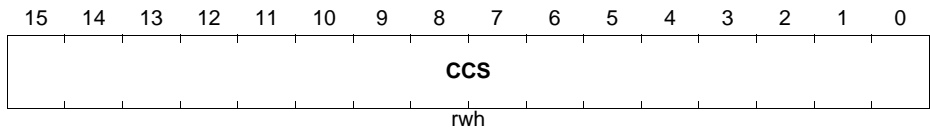
The registers CC6xR can only be read by SW, the modification of the value is done by a shadow register transfer from register CC6xSR. The corresponding shadow registers CC6xSR can be read and written by SW. In capture mode, the value of the T12 counter register can also be captured by registers CC6xSR if the selected capture event is detected (depending on the selected capture mode).

CC6xSR (x=0-2)

Capture/Compare Shadow Reg. for Channel CC6x

XSFR(20_H+2*x)

Reset Value: 0000_H



Field	Bits	Type	Description
CCS	[15:0]	rwh	Shadow Register for Channel x Capture/Compare Value In compare mode, the bit fields contents of CCS are transferred to the bit fields CCV for the corresponding channel during a shadow transfer. In capture mode, the captured value of T12 can be read from these registers.

Note: The shadow registers can also be written by SW in capture mode. In this case, the HW capture event wins over the SW write if both happen in the same cycle (the SW write is discarded).

20.2.8.5 Dead-time Control Register

Register T12DTC controls the dead-time generation for the timer T12 compare channels. Each channel can be independently enabled/disabled for dead-time generation. If enabled, the transition from passive state to active state is delayed by the value defined by bit field DTM.

The dead time counters are clocked with the same frequency as T12.

This structure allows symmetrical dead-time generation in center-aligned and in edge-aligned PWM mode. A duty cycle of 50% leads to CC6x, COUT6x switched on for: 0.5 * period - dead time.

Note: The dead-time counters are not reset by bit T12RES, but by bit DTRES.

T12DTC

Dead-Time Control Register for Timer12

XSFR(14 _H)										Reset Value: 0000 _H					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	DTR 2	DTR 1	DTR 0	0	DTE 2	DTE 1	DTE 0	DTM							
r	rh	rh	rh	r	rw	rw	rw	rw							

Field	Bits	Type	Description
DTM	[7:0]	rw	Dead-Time Bit field DTM determines the programmable delay between switching from the passive state to the active state of the selected outputs. The switching from the active state to the passive state is not delayed.
DTE2, DTE1, DTE0	10, 9, 8	rw	Dead Time Enable Bits Bits DTE0..DTE2 enable and disable the dead time generation for each compare channel (0, 1, 2) of timer T12. 0 _B Dead-Time Counter x is disabled. The corresponding outputs switch from the passive state to the active state (according to the actual compare status) without any delay. 1 _B Dead-Time Counter x is enabled. The corresponding outputs switch from the passive state to the active state (according to the compare status) with the delay programmed in bit field DTM.

Capture/Compare Unit 6 (CCU6)

Field	Bits	Type	Description
DTR2, DTR1, DTR0	14, 13, 12	rh	Dead Time Run Indication Bits Bits DTR0..DTR2 indicate the status of the dead time generation for each compare channel (0, 1, 2) of timer T12. 0 _B Dead-Time Counter x is currently in the passive state. 1 _B Dead-Time Counter x is currently in the active state.
0	15, 11	r	reserved; returns 0 if read; should be written with 0;

20.2.9 Capture/Compare Control Registers

20.2.9.1 Channel State Bits

The Compare State Register CMPSTAT contains status bits monitoring the current capture and compare state and control bits defining the active/passive state of the compare channels.

CMPSTAT

Compare State Register

XSFR(28_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T13 IM	C OUT 63PS	C OUT 62PS	CC 62PS	C OUT 61PS	CC 61PS	C OUT 60PS	CC 60PS	0	CC 63ST	CC POS 62	CC POS 61	CC POS 60	CC 62ST	CC 61ST	CC 60ST
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	r	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
CC60ST, CC61ST, CC62ST, CC63ST¹⁾	0, 1, 2, 6	rh	Capture/Compare State Bits Bits CC6xST monitor the state of the capture/compare channels. Bits CC6xST (x = 0, 1, 2) are related to T12, bit CC63ST is related to T13. 0 _B In compare mode, the timer count is less than the compare value. In capture mode, the selected edge has not yet been detected since the bit has been cleared by SW the last time. 1 _B In compare mode, the counter value is greater than or equal to the compare value. In capture mode, the selected edge has been detected.
CCPOS60, CCPOS61, CCPOS62	3, 4, 5	rh	Sampled Hall Pattern Bits Bits CCPOS6x (x = 0, 1, 2) are indicating the value of the input Hall pattern that has been compared to the current and expected value. The value is sampled when the event HCRDY (Hall Compare Ready) occurs. 0 _B The input CCPOS6x has been sampled as 0. 1 _B The input CCPOS6x has been sampled as 1.

Capture/Compare Unit 6 (CCU6)

Field	Bits	Type	Description
CC60PS, CC61PS, CC62PS, COUT60PS, COUT61PS, COUT62PS, COUT63PS 2)	8, 10, 12, 9, 11, 13, 14	rwh	Passive State Select for Compare Outputs Bits CC6xPS, COUT6xPS select the state of the corresponding compare channel, that is considered to be the passive state. During the passive state, the passive level (defined in register PSLR) is driven by the output pin. Bits CC6xPS, COUT6xPS (x = 0, 1, 2) are related to T12, bit CC63PS is related to T13. 0 _B The corresponding compare signal is in passive state while CC6xST is 0. 1 _B The corresponding compare signal is in passive state while CC6xST is 1. In capture mode, these bits are not used.
T13IM ³⁾	15	rwh	T13 Inverted Modulation Bit T13IM inverts the T13 signal for the modulation of the CC6x and COUT6x (x = 0, 1, 2) signals. 0 _B T13 output CC63_O is equal to CC63ST. 1 _B T13 output CC63_O is equal to $\overline{\text{CC63ST}}$.
0	7	r	reserved; returns 0 if read; should be written with 0;

1) These bits are set and cleared according to the T12, T13 switching rules

2) These bits have shadow bits and are updated in parallel to the capture/compare registers of T12, T13 respectively. A read action targets the actually used values, whereas a write action targets the shadow bits.

3) This bit has a shadow bit and is updated in parallel to the compare and period registers of T13. A read action targets the actually used values, whereas a write action targets the shadow bit.

Capture/Compare Unit 6 (CCU6)

The Compare Status Modification Register CMPMODIF provides software-control (independent set and clear conditions) for the channel state bits CC6xST. This feature enables the user to individually change the status of the output lines by software, for example when the corresponding compare timer is stopped.

CMPMODIF

Compare State Modification Register

XSFR(2A_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	MCC 63R		0		MCC 62R	MCC 61R	MCC 60R	0	MCC 63S		0		MCC 62S	MCC 61S	MCC 60S
r	w		r		w	w	w	r	w		r		w	w	w

Field	Bits	Type	Description
MCC60S, MCC61S, MCC62S, MCC63S, MCC60R, MCC61R, MCC62R, MCC63R	0, 1, 2, 6, 8, 9, 10, 14	w	Capture/Compare Status Modification Bits These bits are used to bits to set (MCC6xS) or to clear (MCC6xR) the corresponding bits CC6xST by SW. This feature allows the user to individually change the status of the output lines by SW, e.g. when the corresponding compare timer is stopped. This allows a bit manipulation of CC6xST-bits by a single data write action. The following functionality of a write access to bits concerning the same capture/compare state bit is provided: [MCC6xR, MCC6xS] = 00 _B Bit CC6xST is not changed. 01 _B Bit CC6xST is set. 10 _B Bit CC6xST is cleared. 11 _B reserved
0	[5:3], 7, [13:11], 15	r	reserved; returns 0 if read; should be written with 0;

20.2.9.2 T12 Mode Control Register

Register T12MSEL contains control bits to select the capture/compare functionality of the three channels of Timer T12.

T12MSEL

T12 Mode Select Register

XSFR (46_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D BYP	HSYNC			MSEL62			MSEL61			MSEL60					
rw	rw			rw			rw			rw			rw		

Field	Bits	Type	Description
MSEL60, MSEL61, MSEL62	[3:0], [7:4], [11:8]	rw	Capture/Compare Mode Selection These bit fields select the operating mode of the three T12 capture/compare channels. Each channel (x = 0, 1, 2) can be programmed individually for one of these modes (except for Hall Sensor Mode). Coding see Table 20-5 .
HSYNC	[14:12]	rw	Hall Synchronization Bit field HSYNC defines the source for the sampling of the Hall input pattern and the comparison to the current and the expected Hall pattern bit fields. Coding see Table 20-11 .
DBYP	15	rw	Delay Bypass DBYP controls whether the source signal for the sampling of the Hall input pattern (selected by HSYNC) is delayed by the Dead-Time Counter 0. <div style="margin-left: 20px;"> 0_B The bypass is not active. Dead-Time Counter 0 is generating a delay after the source signal becomes active. 1_B The bypass is active. Dead-Time Counter 0 is not used for a delay. </div>

20.2.9.3 Timer Control Registers

Register TCTR0 controls the basic functionality of both timers, T12 and T13.

Note: A write action to the bit fields T12CLK or T12PRE is only taken into account while the timer T12 is not running (T12R=0). A write action to the bit fields T13CLK or T13PRE is only taken into account while the timer T13 is not running (T13R=0).

TCTR0

Timer Control Register 0

XSFR(2C_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	STE 13	T13R	T13 PRE	T13CLK		CTM	CDIR	STE 12	T12R	T12 PRE	T12CLK				
r	rh	rh	rw	rw		rw	rh	rh	rh	rw	rw				

Field	Bits	Type	Description
T12CLK	[2:0]	rw	Timer T12 Input Clock Select Selects the input clock for timer T12 that is derived from the peripheral clock according to the equation $f_{T12} = f_{CC6} / 2^{<T12CLK>}$. 000 _B $f_{T12} = f_{CC6}$ 001 _B $f_{T12} = f_{CC6} / 2$ 010 _B $f_{T12} = f_{CC6} / 4$ 011 _B $f_{T12} = f_{CC6} / 8$ 100 _B $f_{T12} = f_{CC6} / 16$ 101 _B $f_{T12} = f_{CC6} / 32$ 110 _B $f_{T12} = f_{CC6} / 64$ 111 _B $f_{T12} = f_{CC6} / 128$
T12PRE	3	rw	Timer T12 Prescaler Bit In order to support higher clock frequencies, an additional prescaler factor of 1/256 can be enabled for the prescaler for T12. 0 _B The additional prescaler for T12 is disabled. 1 _B The additional prescaler for T12 is enabled.
T12R	4	rh	Timer T12 Run Bit¹⁾ T12R starts and stops timer T12. It is set/cleared by SW by setting bits T12RR or T12RS or it is cleared by HW according to the function defined by bit field T12SSC. 0 _B Timer T12 is stopped. 1 _B Timer T12 is running.

Field	Bits	Type	Description
STE12	5	rh	Timer T12 Shadow Transfer Enable Bit STE12 enables or disables the shadow transfer of the T12 period value, the compare values and passive state select bits and levels from their shadow registers to the actual registers if a T12 shadow transfer event is detected. Bit STE12 is cleared by hardware after the shadow transfer. A T12 shadow transfer event is a period-match while counting up or a one-match while counting down. 0 _B The shadow register transfer is disabled. 1 _B The shadow register transfer is enabled.
CDIR	6	rh	Count Direction of Timer T12 This bit is set/cleared according to the counting rules of T12. 0 _B T12 counts up. 1 _B T12 counts down.
CTM	7	rw	T12 Operating Mode 0 _B Edge-aligned Mode: T12 always counts up and continues counting from zero after reaching the period value. 1 _B Center-aligned Mode: T12 counts down after detecting a period-match and counts up after detecting a one-match.
T13CLK	[10:8]	rw	Timer T13 Input Clock Select Selects the input clock for timer T13 that is derived from the peripheral clock according to the equation $f_{T13} = f_{CC6} / 2^{<T13CLK>}$. 000 _B $f_{T13} = f_{CC6}$ 001 _B $f_{T13} = f_{CC6} / 2$ 010 _B $f_{T13} = f_{CC6} / 4$ 011 _B $f_{T13} = f_{CC6} / 8$ 100 _B $f_{T13} = f_{CC6} / 16$ 101 _B $f_{T13} = f_{CC6} / 32$ 110 _B $f_{T13} = f_{CC6} / 64$ 111 _B $f_{T13} = f_{CC6} / 128$

Field	Bits	Type	Description
T13PRE	11	rw	Timer T13 Prescaler Bit In order to support higher clock frequencies, an additional prescaler factor of 1/256 can be enabled for the prescaler for T13. 0 _B The additional prescaler for T13 is disabled. 1 _B The additional prescaler for T13 is enabled.
T13R	12	rh	Timer T13 Run Bit²⁾ T13R starts and stops timer T13. It is set/cleared by SW by setting bits T13RR or T13RS or it is set/cleared by HW according to the function defined by bit fields T13SSC, T13TEC and T13TED. 0 _B Timer T13 is stopped. 1 _B Timer T13 is running.
STE13	13	rh	Timer T13 Shadow Transfer Enable Bit STE13 enables or disables the shadow transfer of the T13 period value, the compare value and passive state select bit and level from their shadow registers to the actual registers if a T13 shadow transfer event is detected. Bit STE13 is cleared by hardware after the shadow transfer. A T13 shadow transfer event is a period-match. 0 _B The shadow register transfer is disabled. 1 _B The shadow register transfer is enabled.
0	[15: 14]	r	reserved; returns 0 if read; should be written with 0;

- 1) A concurrent set/clear action on T12R (from T12SSC, T12RR or T12RS) will have no effect. The bit T12R will remain unchanged.
- 2) A concurrent set/cleared action on T13R (from T13SSC, T13TEC, T13RR or T13RS) will have no effect. The bit T12R will remain unchanged.

Capture/Compare Unit 6 (CCU6)

Register TCTR2 controls the single-shot and the synchronization functionality of both timers T12 and T13. Both timers can run in single-shot mode. In this mode they stop their counting sequence automatically after one counting period with a count value of zero. The single-shot mode and the synchronization feature of T13 to T12 allow the generation of events with a programmable delay after well-defined PWM actions of T12.

TCTR2

Timer Control Register 2

XSFR(2E_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				T13 RSEL		T12 RSEL		0	T13 TED		T13 TEC		T13 SSC	T12 SSC	
r				rw		rw		r	rw		rw		rw	rw	

Field	Bits	Type	Description
T12SSC	0	rw	Timer T12 Single Shot Control This bit controls the single shot-mode of T12. 0 _B The single-shot mode is disabled, no HW action on T12R. 1 _B The single shot mode is enabled, the bit T12R is cleared by HW if - T12 reaches its period value in edge-aligned mode - T12 reaches the value 1 while down counting in center-aligned mode. In parallel to the clear action of bit T12R, the bits CC6xST (x=0, 1, 2) are cleared.
T13SSC	1	rw	Timer T13 Single Shot Control This bit controls the single shot-mode of T13. 0 _B No HW action on T13R 1 _B The single-shot mode is enabled, the bit T13R is cleared by HW if T13 reaches its period value. In parallel to the clear action of bit T13R, the bit CC63ST is cleared.

Field	Bits	Type	Description
T13TEC	[4:2]	rw	T13 Trigger Event Control bit field T13TEC selects the trigger event to start T13 (automatic set of T13R for synchronization to T12 compare signals) according to following combinations: 000 _B no action 001 _B set T13R on a T12 compare event on channel 0 010 _B set T13R on a T12 compare event on channel 1 011 _B set T13R on a T12 compare event on channel 2 100 _B set T13R on any T12 compare event (ch. 0, 1, 2) 101 _B set T13R upon a period-match of T12 110 _B set T13R upon a zero-match of T12 (while counting up) 111 _B set T13R on any edge of inputs CCPOSx
T13TED	[6:5]	rw	Timer T13 Trigger Event Direction¹⁾ Bit field T13TED delivers additional information to control the automatic set of bit T13R in the case that the trigger action defined by T13TEC is detected. 00 _B reserved, no action 01 _B while T12 is counting up 10 _B while T12 is counting down 11 _B independent on the count direction of T12
T12RSEL	[9:8]	rw	Timer T12 External Run Selection Bit field T12RSEL defines the event of signal T12HR that can set the run bit T12R by HW. 00 _B The external setting of T12R is disabled. 01 _B Bit T12R is set if a rising edge of signal T12HR is detected. 10 _B Bit T12R is set if a falling edge of signal T12HR is detected. 11 _B Bit T12R is set if an edge of signal T12HR is detected.

Field	Bits	Type	Description
T13RSEL	[11:10]	rw	Timer T13 External Run Selection Bit field T13RSEL defines the event of signal T13HR that can set the run bit T13R by HW. 00 _B The external setting of T13R is disabled. 01 _B Bit T13R is set if a rising edge of signal T13HR is detected. 10 _B Bit T13R is set if a falling edge of signal T13HR is detected. 11 _B Bit T13R is set if an edge of signal T13HR is detected.
0	7, [15: 12]	r	reserved; returns 0 if read; should be written with 0;

1) Example:

If the timer T13 is intended to start at any compare event on T12 (T13TEC=100) the trigger event direction can be programmed to

- counting up >> a T12 channel 0, 1, 2 compare match triggers T13R only while T12 is counting up
- counting down >> a T12 channel 0, 1, 2 compare match triggers T13R only while T12 is counting down
- independent from bit CDIR >> each T12 channel 0, 1, 2 compare match triggers T13R

The timer count direction is taken from the value of bit CDIR. As a result, if T12 is running in edge-aligned mode (counting up only), T13 can only be started automatically if bit field T13TED=01 or 11.

Capture/Compare Unit 6 (CCU6)

Register TCTR4 provides software-control (independent set and clear conditions) for the run bits T12R and T13R. Furthermore, the timers can be reset (while running) and bits STE12 and STE13 can be controlled by software. Reading these bits always returns 0.

TCTR4

Timer Control Register 4

XSFR(26_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T13 STD	T13 STR	T13 CNT	0		T13 RES	T13 RS	T13 RR	T12 STD	T12 STR	T12 CNT	0	DT RES	T12 RES	T12 RS	T12 RR
w	w	w	r		w	w	w	w	w	w	r	w	w	w	w

Field	Bits	Type	Description
T12RR	0	w	Timer T12 Run Reset Setting this bit clears the T12R bit. 0 _B T12R is not influenced. 1 _B T12R is cleared, T12 stops counting.
T12RS	1	w	Timer T12 Run Set Setting this bit sets the T12R bit. 0 _B T12R is not influenced. 1 _B T12R is set, T12 starts counting.
T12RES	2	w	Timer T12 Reset 0 _B No effect on T12. 1 _B The T12 counter register is cleared to zero. The switching of the output signals is according to the switching rules. Setting of T12RES has no impact on bit T12R.
DTRES	3	w	Dead-Time Counter Reset 0 _B No effect on the dead-time counters. 1 _B The three dead-time counter channels are cleared to zero.
T12CNT	5	w	Timer T12 Count Event 0 _B No action 1 _B If enabled (PISELH), timer T12 counts one step.
T12STR	6	w	Timer T12 Shadow Transfer Request 0 _B No action 1 _B STE12 is set, enabling the shadow transfer.

Field	Bits	Type	Description
T12STD	7	w	Timer T12 Shadow Transfer Disable 0 _B No action 1 _B STE12 is cleared without triggering the shadow transfer.
T13RR	8	w	Timer T13 Run Reset Setting this bit clears the T13R bit. 0 _B T13R is not influenced. 1 _B T13R is cleared, T13 stops counting.
T13RS	9	w	Timer T13 Run Set Setting this bit sets the T13R bit. 0 _B T13R is not influenced. 1 _B T13R is set, T13 starts counting.
T13RES	10	w	Timer T13 Reset 0 _B No effect on T13. 1 _B The T13 counter register is cleared to zero. The switching of the output signals is according to the switching rules. Setting of T13RES has no impact on bit T13R.
T13CNT	13	w	Timer T13 Count Event 0 _B No action 1 _B If enabled (PISELH), timer T13 counts one step.
T13STR	14	w	Timer T13 Shadow Transfer Request 0 _B No action 1 _B STE13 is set, enabling the shadow transfer.
T13STD	15	w	Timer T13 Shadow Transfer Disable 0 _B No action 1 _B STE13 is cleared without triggering the shadow transfer.
0	4, [12:11]	r	reserved; returns 0 if read; should be written with 0;

Note: A simultaneous write of a 1 to bits that set and clear the same bit will trigger no action. The corresponding bit will remain unchanged.

20.3 Operating Timer T13

Timer T13 is implemented similarly to Timer T12, but only with one channel in compare mode. A 16-bit up-counter is connected to a channel register via a comparator, that generates a signal when the counter contents match the contents of the channel register. A variety of control functions facilitate the adaptation of the T13 structure to different application needs. In addition, T13 can be started synchronously to timer T12 events.

This section provides information about:

- T13 overview (see [Section 20.3.1](#))
- Counting scheme (see [Section 20.3.2](#))
- Compare mode (see [Section 20.3.3](#))
- Compare output path (see [Section 20.3.4](#))
- Shadow register transfer (see [Section 20.3.5](#))
- T13 counter register description (see [Section 20.3.6](#))

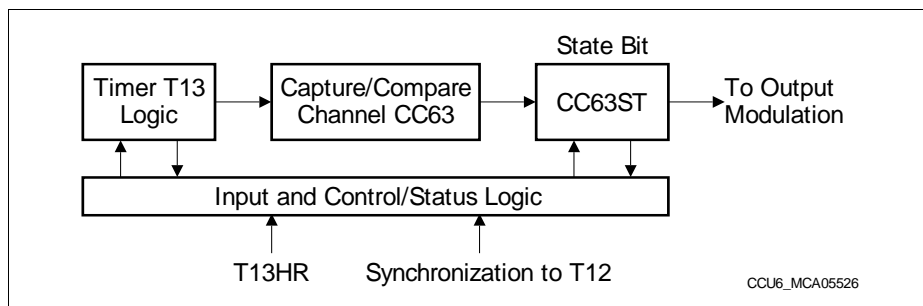


Figure 20-23 Overview Diagram of the Timer T13 Block

20.3.1 T13 Overview

Figure 20-24 shows a detailed block diagram of Timer T13. The functions of the timer T12 block are controlled by bits in registers **TCTR0**, **TCTR2**, **TCTR4**, and **PISELH**. Timer T13 receives its input clock, f_{T13} , from the module clock f_{CC6} via a programmable prescaler and an optional 1/256 divider or from an input signal T13HR. T13 can only count up (similar to the Edge-Aligned mode of T12).

Via a comparator, the timer T13 Counter Register **T13** is connected to the Period Register **T13PR**. This register determines the maximum count value for T13. When T13 reaches the period value, signal T13_PM (T13 Period Match) is generated and T13 is cleared to 0000_H with the next T13 clock edge. The Period Register receives a new period value from its Shadow Period Register, T13PS, that is loaded via software. The transfer of a new period value from the shadow register into T13PR is controlled via the 'T13 Shadow Transfer' control signal, T13_ST. The generation of this signal depends on the associated control bit STE13. Providing a shadow register for the period value as

Capture/Compare Unit 6 (CCU6)

well as for other values related to the generation of the PWM signal facilitates a concurrent update by software for all relevant parameters (refer to [Table 20.3.5](#)).

Another signal indicates whether the counter contents are equal to 0000_H (T13_ZM).

A Single-Shot control bit, T13SSC, enables an automatic stop of the timer when the current counting period is finished (see [Figure 20-26](#)).

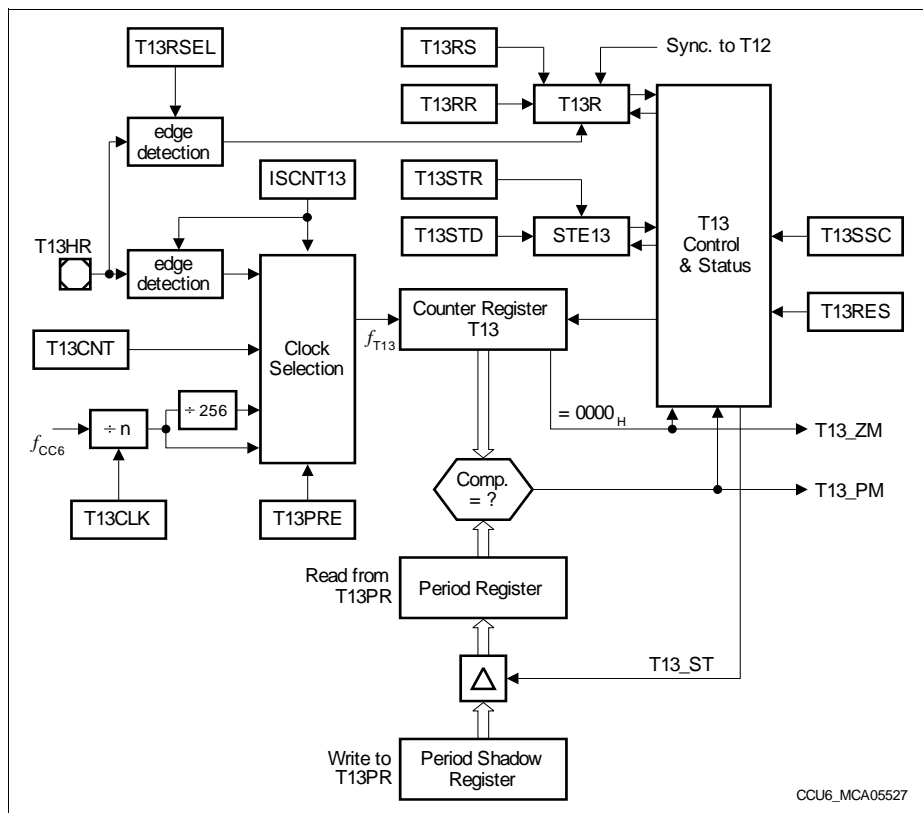


Figure 20-24 T13 Counter Logic and Period Comparators

The start or stop of T13 is controlled by the Run bit, T13R. This control bit can be set by software via the associated set/clear bits T13RS or T13RR in register [TCTR4](#), or it is cleared by hardware according to preselected conditions (single-shot mode).

The timer T13 run bit T13R must not be set while the applied T13 period value is zero. Bit T13R can be set automatically if an event of T12 is detected to synchronize T13 timings to T12 events, e.g. to generate a programmable delay via T13 after an edge of a T12 compare channel before triggering an AD conversion (T13 can trigger ADC

conversions).

Timer T13 can be cleared to 0000_H via control bit T13RES. Setting this write-only bit only clears the timer contents, but has no further effects, e.g., it does not stop the timer.

The generation of the T13 shadow transfer control signal, T13_ST, is enabled via bit STE13. This bit can be set or cleared by software indirectly through its associated set/reset control bits T13STR and T13STD.

Two bit fields, T13TEC and T13TED, control the synchronization of T13 to Timer T12 events. T13TEC selects the trigger event, while T13TED determines for which T12 count direction the trigger should be active.

While Timer T13 is running, write accesses to the count register T13 are not taken into account. If T13 is stopped, write actions to register T13 are immediately taken into account.

Note: The T13 Period Register and its associated shadow register are located at the same physical address. A write access to this address targets the Shadow Register, while a read access reads from the actual period register.

20.3.2 T13 Counting Scheme

This section describes the clocking and the counting capabilities of T13.

20.3.2.1 Clock Selection

In **Timer Mode** (**PISELH.ISCNT13** = 00_B), the input clock f_{T13} of Timer T13 is derived from the internal module clock f_{CC6} through a programmable prescaler and an optional 1/256 divider. The resulting prescaler factors are listed in **Table 20-6**. The prescaler of T13 is cleared while T13 is not running (**TCTR0.T13R** = 0) to ensure reproducible timings and delays.

Table 20-6 Timer T13 Input Clock Options

T13CLK	Resulting Input Clock f_{T13} Prescaler Off (T13PRE = 0)	Resulting Input Clock f_{T13} Prescaler On (T13PRE = 1)
000 _B	f_{CC6}	$f_{CC6} / 256$
001 _B	$f_{CC6} / 2$	$f_{CC6} / 512$
010 _B	$f_{CC6} / 4$	$f_{CC6} / 1024$
011 _B	$f_{CC6} / 8$	$f_{CC6} / 2048$
100 _B	$f_{CC6} / 16$	$f_{CC6} / 4096$
101 _B	$f_{CC6} / 32$	$f_{CC6} / 8192$
110 _B	$f_{CC6} / 64$	$f_{CC6} / 16384$
111 _B	$f_{CC6} / 128$	$f_{CC6} / 32768$

In **Counter Mode**, timer T13 counts one step:

- If a 1 is written to **TCTR4.T13CNT** and **PISELH.ISCNT13** = 01_B
- If a rising edge of input signal T13HR is detected and **PISELH.ISCNT13** = 10_B
- If a falling edge of input signal T13HR is detected and **PISELH.ISCNT13** = 11_B

20.3.2.2 T13 Counting

The period of the timer is determined by the value in the period Register T13PR according to the following formula:

$$T13_{PER} = \langle \text{Period-Value} \rangle + 1; \text{ in } T13 \text{ clocks } (f_{T13}) \quad (20.3)$$

Timer T13 can only count up, comparable to the Edge-Aligned mode of T12. This leads to very simple 'counting rule' for the T13 counter:

- The counter is cleared with the next T13 clock edge if a Period-Match is detected. The counting direction is always upwards.

The behavior of T13 is illustrated in **Figure 20-25**.

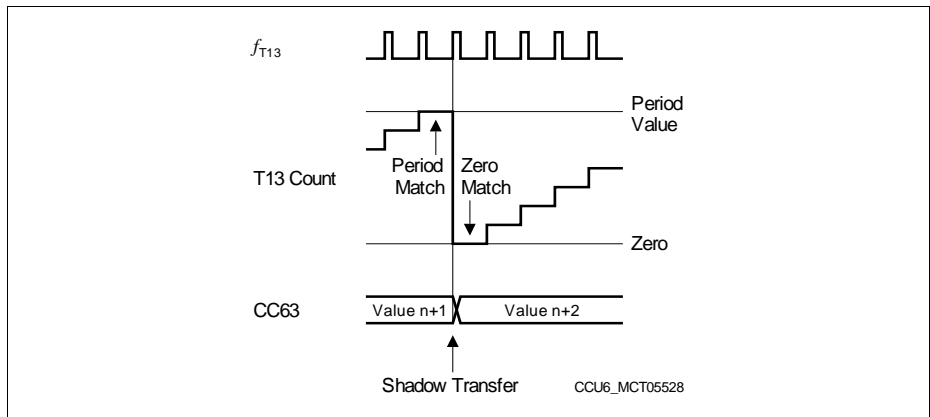


Figure 20-25 T13 Counting Sequence

20.3.2.3 Single-Shot Mode

In Single-Shot Mode, the timer run bit T13R is cleared by hardware. If bit T13SSC = 1, the timer T13 will stop when the current timer period is finished.

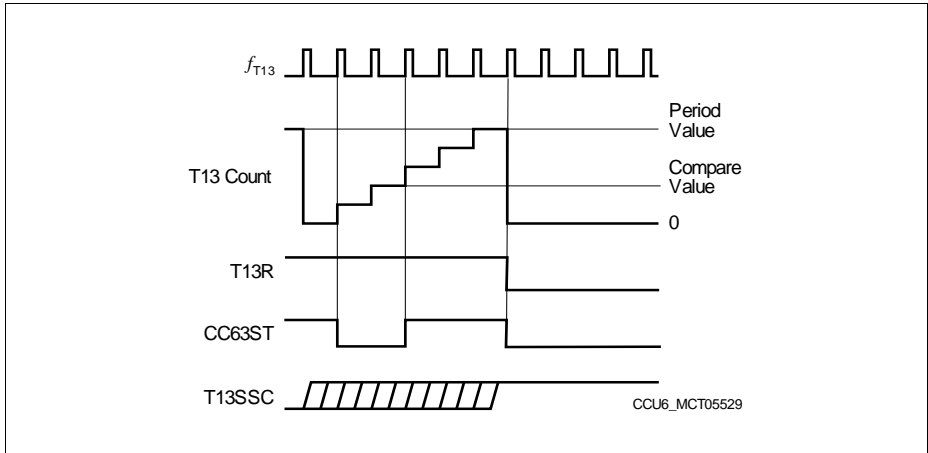


Figure 20-26 Single-Shot Operation of Timer T13

20.3.2.4 Synchronization to T12

Timer T13 can be synchronized to a T12 event. Bit fields T13TEC and T13TED select the event that is used to start Timer T13. The selected event sets bit T13R via HW, and T13 starts counting. Combined with the Single-Shot mode, this feature can be used to generate a programmable delay after a T12 event.

Figure 20-27 shows an example for the synchronization of T13 to a T12 event. Here, the selected event is a compare-match (compare value = 2) while counting up. The clocks of T12 and T13 can be different (other prescaler factor); the figure shows an example in which T13 is clocked with half the frequency of T12.

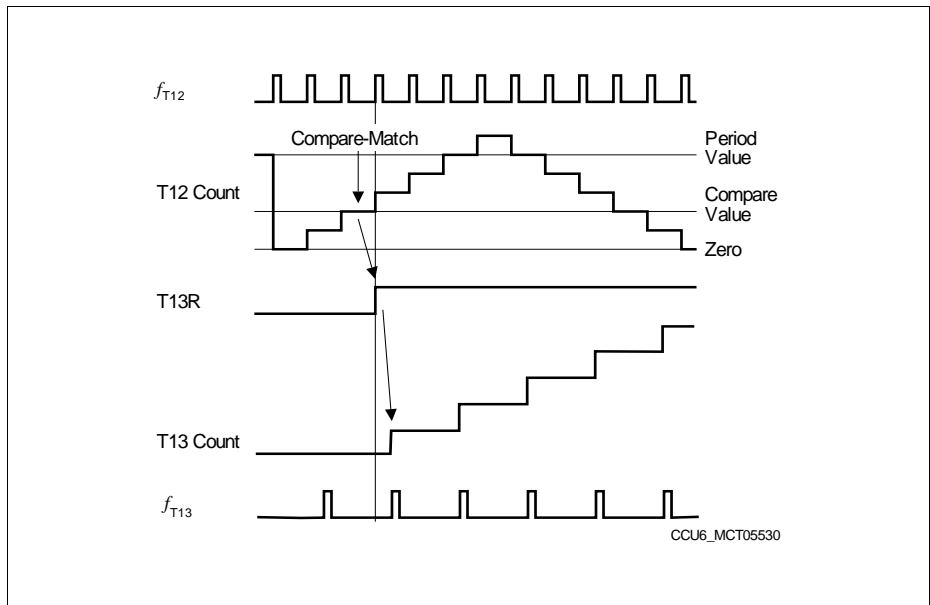


Figure 20-27 Synchronization of T13 to T12 Compare Match

Bit field T13TEC selects the trigger event to start T13 (automatic set of T13R for synchronization to T12 compare signals) according to the combinations shown in [Table 20-7](#). Bit field T13TED additionally specifies for which count direction of T12 the selected trigger event should be regarded (see [Table 20-8](#)).

Table 20-7 T12 Trigger Event Selection

T13TEC	Selected Event
000 _B	None
001 _B	T12 Compare Event on Channel 0 (CM_CC60)
010 _B	T12 Compare Event on Channel 1 (CM_CC61)
011 _B	T12 Compare Event on Channel 2 (CM_CC62)
100 _B	T12 Compare Event on any Channel (0, 1, 2)
101 _B	T12 Period-Match (T12_PM)
110 _B	T12 Zero-Match while counting up (T12_ZM and CDIR = 0)
111 _B	Any Hall State Change

Table 20-8 T12 Trigger Event Additional Specifier

T13TED	Selected Event Specifier
00 _B	Reserved, no action
01 _B	Selected event is active while T12 is counting up (CDIR = 0)
10 _B	Selected event is active while T12 is counting down (CDIR = 1)
11 _B	Selected event is active independently of the count direction of T12

20.3.3 T13 Compare Mode

Associated with Timer T13 is one compare channel, that can perform compare operations with regard to the contents of the T13 counter.

Figure 20-23 gives an overview on the T13 channel in Compare Mode. The channel is connected to the T13 counter register via an equal-to comparator, generating a compare match signal when the contents of the counter matches the contents of the compare register.

The channel consists of the comparator and a double register structure - the actual compare register, **CC63R**, feeding the comparator, and an associated shadow register, **CC63SR**, that is preloaded by software and transferred into the compare register when signal T13 shadow transfer, T13_ST, gets active. Providing a shadow register for the compare value as well as for other values related to the generation of the PWM signal facilitates a concurrent update by software for all relevant parameters.

Associated with the channel is a State Bit, **CMPSTAT.CC63ST**, holding the status of the compare operation. **Figure 20-28** gives an overview on the logic for the State Bit.

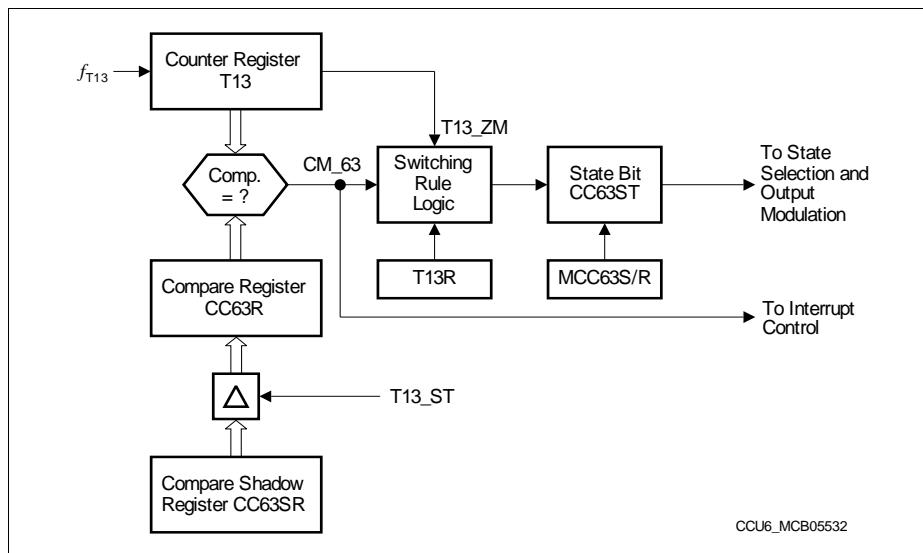


Figure 20-28 T13 State Bit Block Diagram

A compare interrupt event **CM_63** is signaled when a compare match is detected. The actual setting of a State Bit has no influence on the interrupt generation.

The inputs to the switching rule logic for the **CC63ST** bit are the timer run bit (**T13R**), the timer zero-match signal (**T13_ZM**), and the actual individual compare-match signal **CM_63**. In addition, the state bit can be set or cleared by software via bits **MCC63S** and

MCC63R in register **CMPMODIF**.

A modification of the State Bit CC63ST by hardware is only possible while Timer T13 is running ($T13R = 1$). If this is the case, the following switching rules apply for setting and resetting the State Bit in Compare Mode:

State Bit **CC63ST** is **set** to 1

- with the next T13 clock (f_{T13}) after a compare-match (T13 is always counting up) (i.e., when the counter is incremented above the compare value);
- with the next T13 clock (f_{T13}) after a zero-match AND a parallel compare-match.

State Bit **CC63ST** is **cleared** to 0

- with the next T13 clock (f_{T13}) after a zero-match AND NO parallel compare-match.

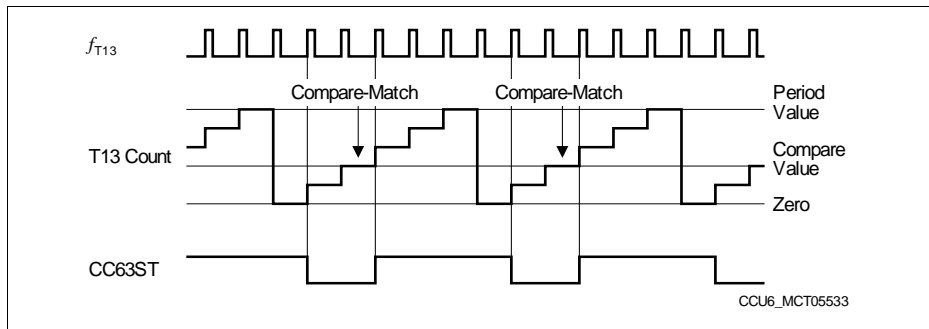


Figure 20-29 T13 Compare Operation

20.3.4 Compare Mode Output Path

Figure 20-30 gives an overview on the signal path from the channel State Bit CC63ST to its output pin COUT63. As illustrated, a user can determine the desired output behavior in relation to the current state of CC63ST. Please refer to [Section 20.2.4.3](#) for detailed information on the output modulation for T12 signals.

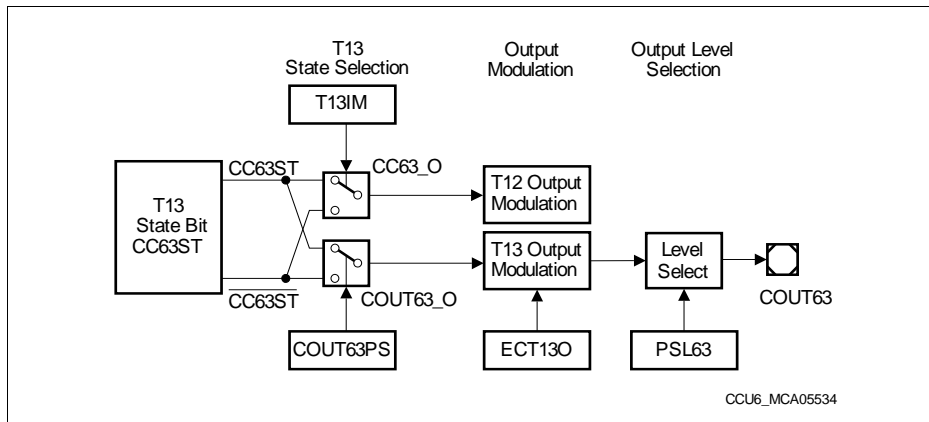


Figure 20-30 Channel 63 Output Path

The output line COUT63_O can generate a T13 PWM at the output pin COUT63. The signal CC63_O can be used to modulate the T12-related output signals with a T13 PWM. In order to decouple COUT63 from the internal modulation, the compare state leading to an active signal can be selected independently by bits T13IM and COUT63PS.

The last block of the data path is the Output Modulation block. Here, the modulation source T13 and the trap functionality are combined and control the actual level of the output pin COUT63 (see [Figure 20-31](#)):

- The **T13 related compare signal** COUT63_O delivered by the T13 state selection with the enable bit **MODCTR.ECT13O**
- The **trap state** TRPS with an individual enable bit **TRPCTR.TRPEN13**

If the modulation input signal COUT63_O is enabled (ECT13O = 1) and is at passive state, the modulated is also in passive state. If the modulation input is not enabled, the output is in passive state.

If the Trap State is active (TRPS = 1), then the output enabled for the trap signal (by TRPEN13 = 1) is set to the passive state.

The output of the modulation control block is connected to a level select block. It offers the option to determine the actual output level of a pin, depending on the state of the output line (decoupling of active/passive state and output polarity) as specified by the Passive State Select bit **PSLR.PSL63**. If the modulated output signal is in the passive

state, the level specified directly by PSL63 is output. If it is in the active state, the inverted level of PSL63 is output. This allows the user to adapt the polarity of an active output signal to the connected circuitry.

The PSL63 bit has a shadow register to allow for updates with the T13 shadow transfer signal (T13_ST) without undesired pulses on the output lines. A read action returns the actually used value, whereas a write action targets the shadow bit. Providing a shadow register for the PSL value as well as for other values related to the generation of the PWM signal facilitates a concurrent update by software for all relevant parameters.

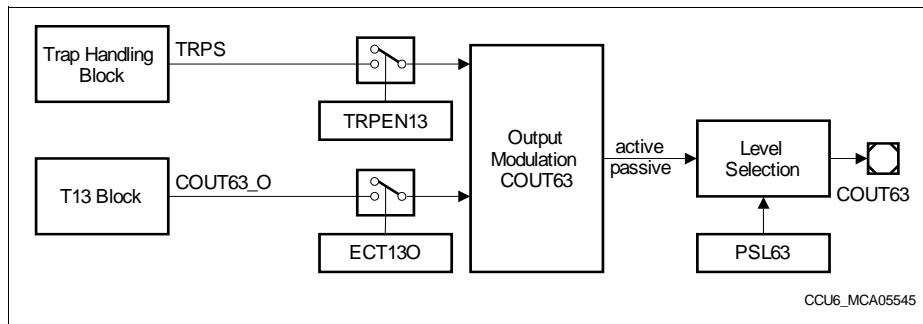


Figure 20-31 T13 Output Modulation

20.3.5 T13 Shadow Register Transfer

A special shadow transfer signal (T13_ST) can be generated to facilitate updating the period and compare values of the compare channel CC63 synchronously to the operation of T13. Providing a shadow register for values defining one PWM period facilitates a concurrent update by software for all relevant parameters. The next PWM period can run with a new set of parameters. The generation of this signal is requested by software via bit **TCTR0.STE13** (set by writing 1 to the write-only bit **TCTR4.T13STR**, cleared by writing 1 to the write-only bit **TCTR4.T13STD**).

When signal T13_ST is active, a shadow register transfer is triggered with the next cycle of the T13 clock. Bit STE13 is automatically cleared with the shadow register transfer.

A T13 shadow register transfer takes place (T13_ST active):

- while timer T13 is not running (T13R = 0), or
- STE13 = 1 and a Period-Match is detected while T13R = 1

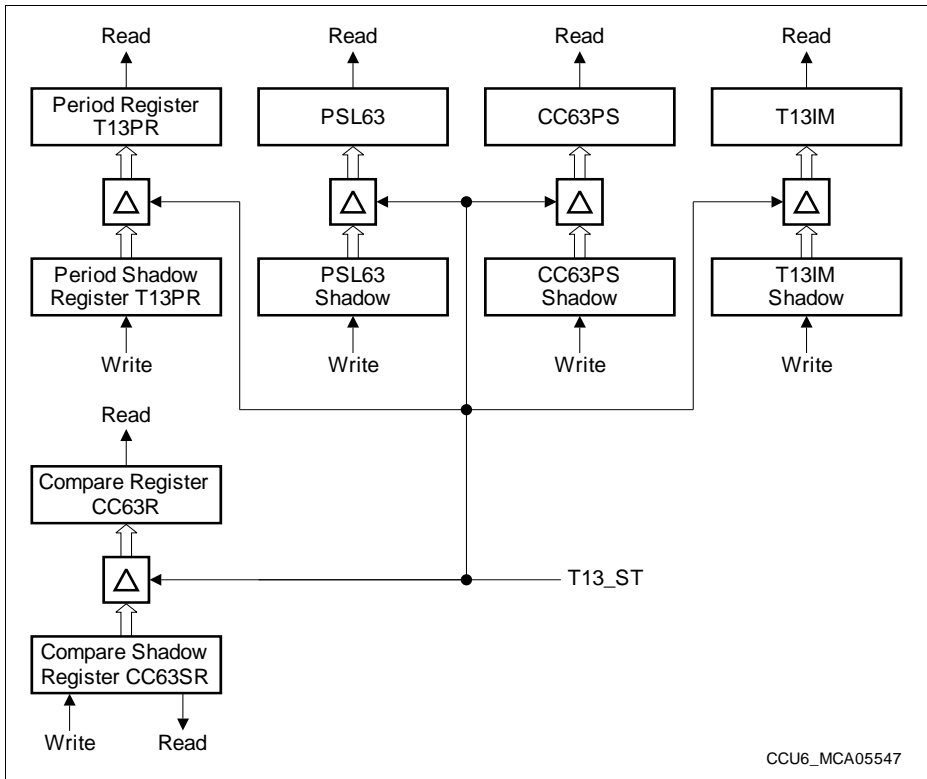


Figure 20-32 T13 Shadow Register Overview

20.3.6 T13 related Registers

20.3.6.1 T13 Counter Register

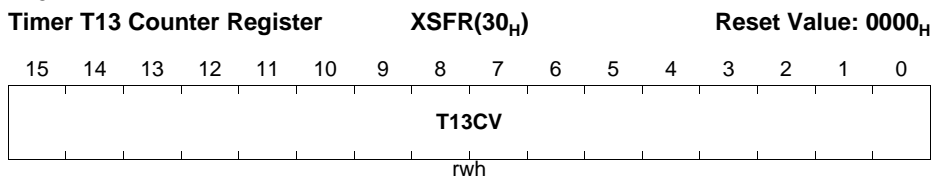
The generation of the patterns for a single channel pulse width modulation (PWM) is based on timer T13. The registers related to timer T13 can be concurrently updated (with well-defined conditions) in order to ensure consistency of the PWM signal. T13 can be synchronized to several timer T12 events.

Timer T13 only supports compare mode on its compare channel CC63.

Register T13 represents the counting value of timer T13. It can only be written while the timer T13 is stopped. Write actions while T13 is running are not taken into account. Register T13 can always be read by SW.

Timer T13 only supports edge-aligned mode (counting up).

T13



Field	Bits	Type	Description
T13CV	[15:0]	rwh	Timer 13 Counter Value This register represents the 16-bit counter value of Timer13.

Note: While timer T13 is stopped, the internal clock divider is reset in order to ensure reproducible timings and delays.

20.3.6.2 Period Register

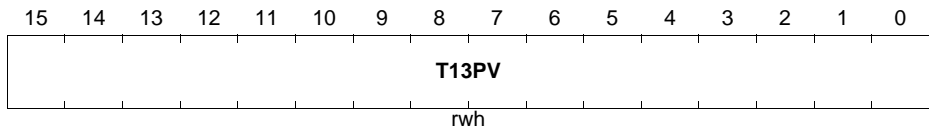
Register T13PR contains the period value for timer T13. The period value is compared to the actual counter value of T13 and the resulting counter actions depend on the defined counting rules. This register has a shadow register and the shadow transfer is controlled by bit STE13. A read action by SW delivers the value currently used for the compare action, whereas the write action targets a shadow register. The shadow register structure allows a concurrent update of all T13-related values.

T13PR

Timer 13 Period Register

XSFR(32_H)

Reset Value: 0000_H



Field	Bits	Type	Description
T13PV	[15:0]	rwh	T13 Period Value The value T13PV defines the counter value for T13 leading to a period-match. When reaching this value, the timer T13 is set to zero.

20.3.6.3 Compare Register

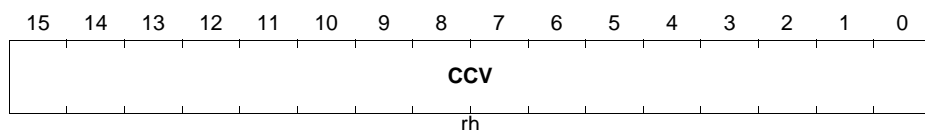
Registers CC63R is the actual compare register for T13. The values stored in CC63R is compared to the counter value of T13. The State Bit CC63ST is located in register **CMPSTAT**.

CC63R

Compare Register for T13

XSFR(34_H)

Reset Value: 0000_H



Field	Bits	Type	Description
CCV	[15:0]	rh	Channel CC63 Compare Value The bit field CCV contains the value, that is compared to the T13 counter value.

20.3.6.4 Compare Shadow Register

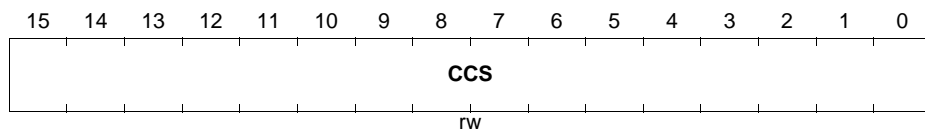
The register CC63R can only be read by SW, the modification of the value is done by a shadow register transfer from register CC63SR. The corresponding shadow register CC63SR can be read and written by SW.

CC63SR

Compare Shadow Register for T13

XSFR(36_H)

Reset Value: 0000_H



Field	Bits	Type	Description
CCS	[15:0]	rw	Shadow Register for Channel CC63 Compare Value The bit field contents of CCS is transferred to the bit field CCV during a shadow transfer.

20.4 Trap Handling

The trap functionality permits the PWM outputs to react on the state of the input signal $\overline{\text{CTRAP}}$. This functionality can be used to switch off the power devices if the trap input becomes active (e.g. to perform an emergency stop). The trap handling and the effect on the output modulation are controlled by the bits in the trap control register **TRPCTR**. The trap flags TRPF and TRPS are located in register **IS** and can be set/cleared by SW by writing to registers **ISS** and **ISR**.

Figure 20-33 gives an overview on the trap function.

The Trap Flag TRPF monitors the trap input and initiates the entry into the Trap State. The Trap State Bit TRPS determines the effect on the outputs and controls the exit of the Trap State.

When a trap condition is detected ($\overline{\text{CTRAP}} = 0$) and the input is enabled ($\text{TRPPEN} = 1$), both, the Trap Flag TRPF and the Trap State Bit TRPS, are set to 1 (trap state active). The output of the Trap State Bit TRPS leads to the Output Modulation Blocks (for T12 and for T13) and can there deactivate the outputs (set them to the passive state). Individual enable control bits for each of the six T12-related outputs and the T13-related output facilitate a flexible adaptation to the application needs.

There are a number of different ways to exit the Trap State. This offers SW the option to select the best operation for the application. Exiting the Trap State can be done either immediately when the trap condition is removed ($\text{CTRAP} = 1$ or $\text{TRPPEN} = 0$), or under software control, or synchronously to the PWM generated by either Timer T12 or Timer T13.

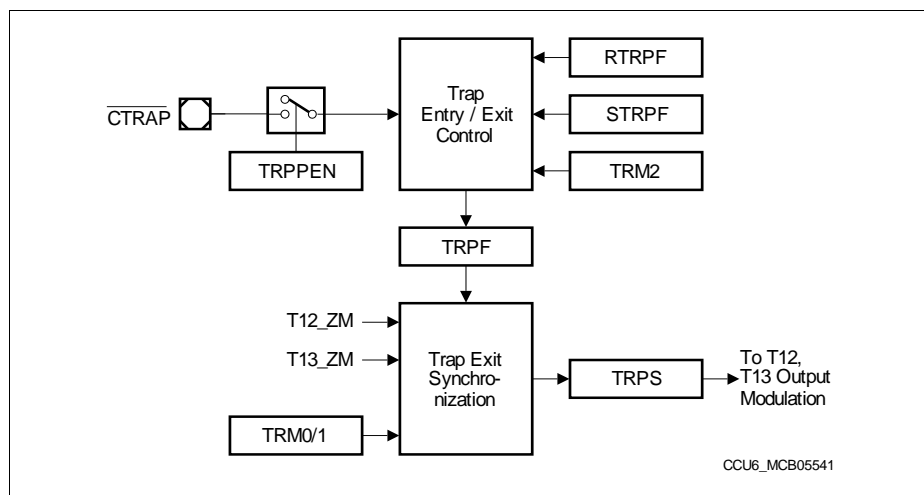


Figure 20-33 Trap Logic Block Diagram

Capture/Compare Unit 6 (CCU6)

Clearing of TRPF is controlled by the mode control bit TRPM2. If $\text{TRPM2} = 0$, TRPF is automatically cleared by HW when CTRAP returns to the inactive level ($\text{CTRAP} = 1$) or if the trap input is disabled ($\text{TRPPEN} = 0$). When $\text{TRPM2} = 1$, TRPF must be reset by SW after CTRAP has become inactive.

Clearing of TRPS is controlled by the mode control bits TRPM1 and TRPM0 (located in the Trap Control Register TRPCTR). A reset of TRPS terminates the Trap State and returns to normal operation. There are three options selected by TRPM1 and TRPM0. One is that the Trap State is left immediately when the Trap Flag TRPF is cleared, without any synchronization to timers T12 or T13. The other two options facilitate the synchronization of the termination of the Trap State to the count periods of either Timer T12 or Timer T13. **Figure 20-34** gives an overview on the associated operation.

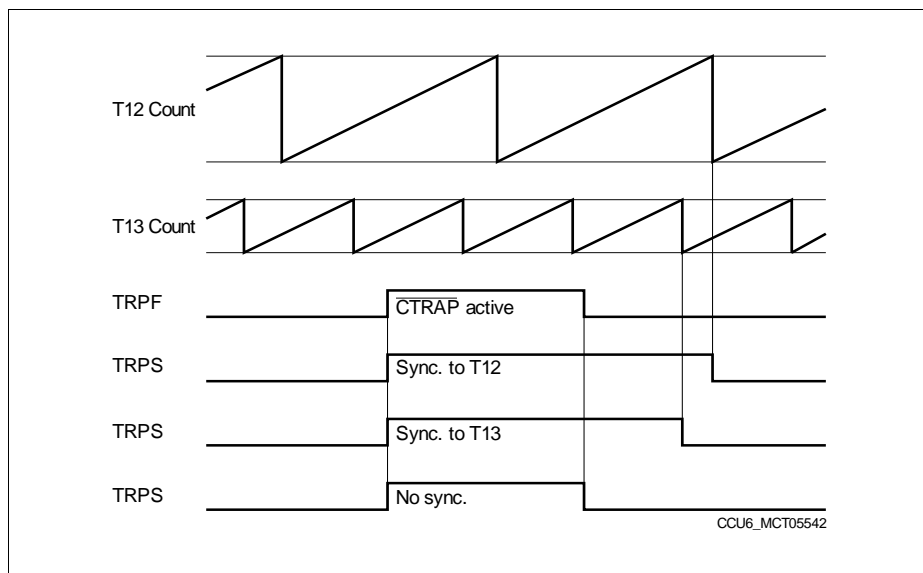


Figure 20-34 Trap State Synchronization (with TRM2 = 0)

20.5 Multi-Channel Mode

The Multi-Channel mode offers the possibility to modulate all six T12-related output signals with one instruction. The bits in bit field **MCMOUT.MCMP** are used to specify the outputs that may become active. If Multi-Channel mode is enabled (bit **MODCTR.MCMEN** = 1), only those outputs may become active, that have a 1 at the corresponding bit position in bit field **MCMP**.

This bit field has its own shadow bit field **MCMOUTS.MCMPS**, that can be written by software. The transfer of the new value in **MCMP** to the bit field **MCMP** can be triggered by, and synchronized to, T12 or T13 events. This structure permits the software to write the new value, that is then taken into account by the hardware at a well-defined moment and synchronized to a PWM signal. This avoids unintended pulses due to unsynchronized modulation sources.

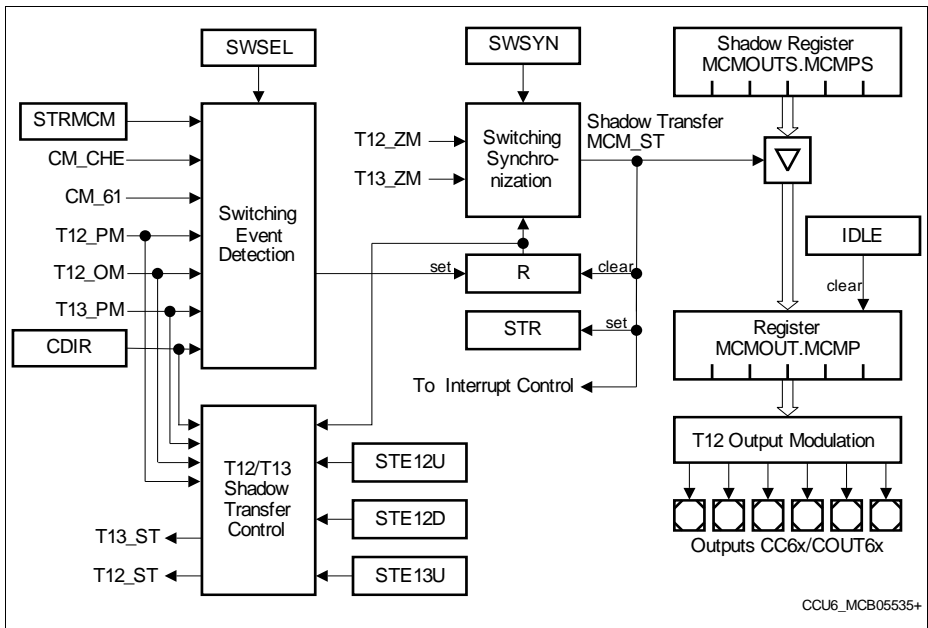


Figure 20-35 Multi-Channel Mode Block Diagram

Figure 20-35 shows the functional blocks for the Multi-Channel operation, controlled by bit fields in register **MCMCTR**. The event that triggers the update of bit field **MCMP** is chosen by **SWSEL**. In order to synchronize the update of **MCMP** to a PWM generated by T12 or T13, bit field **SWSYN** allows the selection of the synchronization event leading to the transfer from **MCMPS** to **MCMP**. Due to this structure, an update takes place with a new PWM period. A reminder flag **R** is set when the selected switching event occurs

Capture/Compare Unit 6 (CCU6)

(the event is not necessarily synchronous to the modulating PWM), and is cleared when the transfer takes place. This flag can be monitored by software to check for the status of this logic block. If the shadow transfer from MCMPS to MCMP takes place, bit **IS.STR** becomes set and an interrupt can be generated.

In addition to the Multi-Channel shadow transfer event MCM_ST, the shadow transfers for T12 (T12_ST) and T13 (T13_ST) can be generated to allow concurrent updates of applied duty cycles for T12 and/or T13 modulation and Multi-Channel patterns.

If it is explicitly desired, the update takes place immediately with the occurrence of the selected event when the direct synchronization mode is selected. The update can also be requested by software by writing to bit field MCMPS with the shadow transfer request bit STRMCM = 1. The option to trigger an update by SW is possible for all settings of SWSEL.

By using the direct mode and bit STRMCM = 1, the update takes place completely under software control.

The event selection and synchronization options are summarized in [Table 20-9](#) and [Table 20-10](#).

Table 20-9 Multi-Channel Mode Switching Event Selection

SWSEL	Selected Event (see register MCMCTR)
000 _B	No automatic event detection
001 _B	Correct Hall Event (CM_CHE) detected at input signals CCPOSx without additional delay
010 _B	T13 Period-Match (T13_PM)
011 _B	T12 One-Match while counting down (T12_OM and CDIR = 1)
100 _B	T12 Compare Channel 1 Event while counting up (CM_61 and CDIR = 0) to support the phase delay function by CC61 for block commutation mode.
101 _B	T12 Period-Match while counting up (T12_PM and CDIR = 0)
110 _B , 111 _B	Reserved, no action

Table 20-10 Multi-Channel Mode Switching Synchronization

SWSYN	Synchronization Event (see register MCMCTR)
00 _B	Direct Mode: the trigger event directly causes the shadow transfer
01 _B	T13 Zero-Match (T13_ZM), the MCM shadow transfer is synchronized to a T13 PWM

Table 20-10 Multi-Channel Mode Switching Synchronization (cont'd)

SWSYN	Synchronization Event (see register MCMCTR)
10 _B	T12 Zero-Match (T12_ZM), the MCM shadow transfer is synchronized to a T12 PWM
11 _B	Reserved, no action

20.6 Hall Sensor Mode

For Brushless DC-Motors in block commutation mode, the Multi-Channel Mode has been introduced to provide efficient means for switching pattern generation. These patterns need to be output in relation to the angular position of the motor. For this, usually Hall sensors or Back-EMF sensing are used to determine the angular rotor position. The CCU6 provides three inputs, CCPOS0, CCPOS1, and CCPOS2, that can be used as inputs for the Hall sensors or the Back-EMF detection signals.

There is a strong correlation between the motor position and the output modulation pattern. When a certain position of the motor has been reached, indicated by the sampled Hall sensor inputs (the Hall pattern), the next, pre-determined Multi-Channel Modulation pattern has to be output. Because of different machine types, the modulation pattern for driving the motor can vary. Therefore, it is wishful to have a wide flexibility in defining the correlation between the Hall pattern and the corresponding Modulation pattern. Furthermore, a hardware mechanism significantly reduces the CPU for block-commutation.

The CCU6 offers the flexibility by having a register containing the currently assumed Hall pattern (CURH), the next expected Hall pattern (EXPH) and the corresponding output pattern (MCMP). A new Modulation pattern is output when the sampled Hall inputs match the expected ones (EXPH). To detect the next rotation phase (segment for block commutation), the CCU6 monitors the Hall inputs for changes. When the next expected Hall pattern is detected, the next corresponding Modulation pattern is output.

To increase for noise immunity (to a certain extend), the CCU6 offers the possibility to introduce a sampling delay for the Hall inputs. Some changes of the Hall inputs are not leading to the expected Hall pattern, because they are only short spikes due to noise. The Hall pattern compare logic compares the Hall inputs to the next expected pattern and also to the currently assumed pattern to filter out spikes.

For the Hall and Modulation output patterns, a double-register structure is implemented. While register **MCMOUT** holds the actually used values, its shadow register **MCMOUTS** can be loaded by software from a pre-defined table, holding the appropriate Hall and Modulation patterns for the given motor control.

A transfer from the shadow register into register MCMOUT can take place when a correct Hall pattern change is detected. Software can then load the next values into register MCMOUTS. It is also possible by software to force a transfer from MCMOUTS into MCMOUT.

Note: The Hall input signals CCPOSx and the CURH and EXPH bit fields are arranged in the following order:

CCPOS0 corresponds to CURH.0 (LSB) and EXPH.0 (LSB)

CCPOS1 corresponds to CURH.1 and EXPH.1

CCPOS2 corresponds to CURH.2 (MSB) and EXPH.2 (MSB)

20.6.1 Hall Pattern Evaluation

The Hall sensor inputs CCPOSx can be permanently monitored via an edge detection block (with the module clock f_{CC6}). In order to suppress spikes on the Hall inputs due to noise in rugged inverter environment, two optional noise filtering methods are supported by the Hall logic (both methods can be combined).

- **Noise filtering with delay:**
 For this function, the mode control bit fields MSEL6x for all T12 compare channels must be programmed to 1000_B and DBYP = 0. The selected event triggers Dead-Time Counter 0 to generate a programmable delay (defined by bit field DTM). When the delay has elapsed, the evaluation signal HCRDY becomes activated.
 Output modulation with T12 PWM signals is not possible in this mode.
- **Noise filtering by synchronization to PWM:**
 The Hall inputs are not permanently monitored by the edge detection block, but samples are taken only at defined points in time during a PWM period. This can be used to sample the Hall inputs when the switching noise (due to PWM) does not disturb the Hall input signals.

If neither the delay function of Dead-Time Counter 0 is not used for the Hall pattern evaluation nor the Hall mode for Brushless DC-Drive control is enabled, the timer T12 block is available for PWM generation and output modulation.

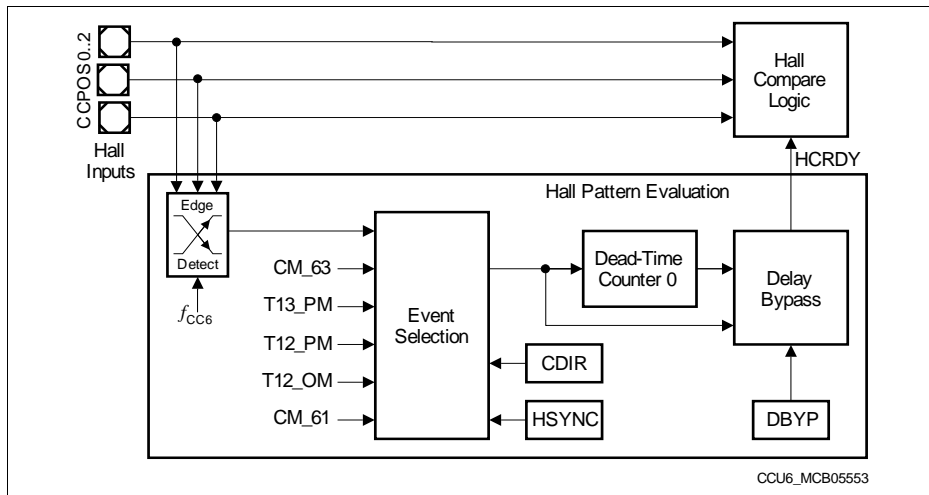


Figure 20-36 Hall Pattern Evaluation

If the evaluation signal HCRDY (Hall Compare Ready, see [Figure 20-37](#)) becomes activated, the Hall inputs are sampled and the Hall compare logic starts the evaluation of the Hall inputs.

Figure 20-36 illustrates the events for Hall pattern evaluation and the noise filter logic, **Table 20-11** summarizes the selectable trigger input signals.

Table 20-11 Hall Sensor Mode Trigger Event Selection

HSYNC	Selected Event (see register T12MSEL)
000 _B	Any edge at any of the inputs CCPOSx, independent from any PWM signal (permanent check).
001 _B	A T13 Compare-Match (CM_63).
010 _B	A T13 Period-Match (T13_PM).
011 _B	Hall sampling triggered by HW sources is switched off.
100 _B	A T12 Period-Match while counting up (T12_PM and CDIR = 0).
101 _B	A T12 One-Match while counting down (T12_OM and CDIR = 1).
110 _B	A T12 Compare-Match of compare channel CC61 while counting up (CM_61 and CDIR = 0).
111 _B	A T12 Compare-Match of compare channel CC61 while counting down (CM_61 and CDIR = 1).

20.6.2 Hall Pattern Compare Logic

Figure 20-37 gives an overview on the double-register structure and the pattern compare logic. Software writes the next modulation pattern (MCMPS) and the corresponding current (CURHS) and expected (EXPHS) Hall patterns into the shadow register MCMOUTS. Register MCMOUT holds the actually used values CURH and EXPH. The modulation pattern MCMP is provided to the T12 Output Modulation block. The current (CURH) and expected (EXPH) Hall patterns are compared to the sampled Hall sensor inputs (visible in register **CMPSTAT**). Sampling of the inputs and the evaluation of the comparator outputs is triggered by the evaluation signal HCRDY (Hall Compare Ready), that is detailed in the next section.

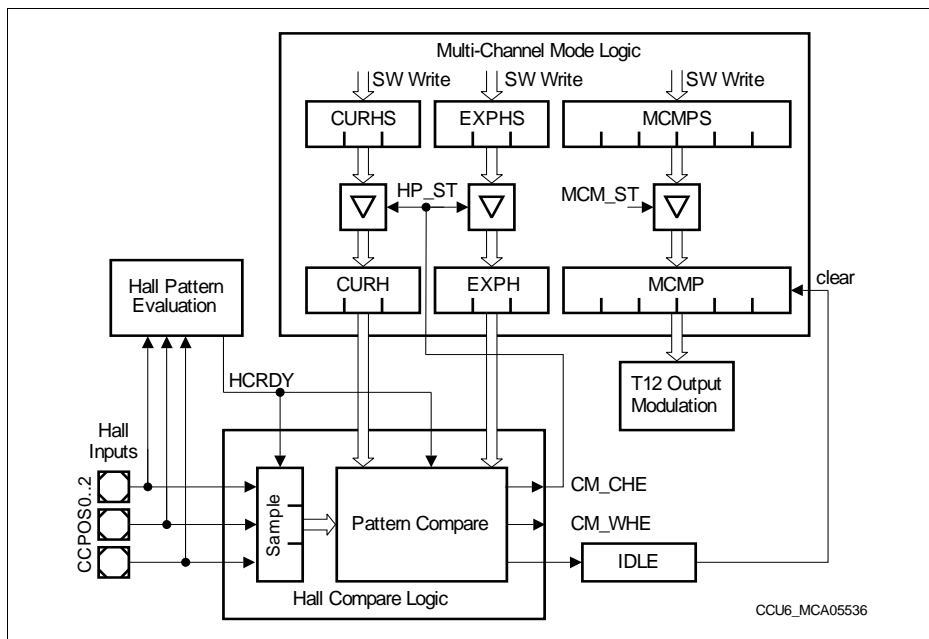


Figure 20-37 Hall Pattern Compare Logic

- If the sampled Hall pattern matches the value programmed in CURH, the detected transition was a spike (no Hall event) and no further actions are necessary.
- If the sampled Hall pattern matches the value programmed in EXPH, the detected transition was the expected event (correct Hall event CM_CHE) and the MCMP value has to change.
- If the sampled Hall pattern matches neither CURH nor EXPH, the transition was due to a major error (wrong Hall event CM_CWE) and can lead to an emergency shut down (IDLE).

At every correct Hall event (CM_CHE), the next Hall patterns are transferred from the shadow register MCMOUTS into MCMOUT (Hall pattern shadow transfer HP_ST), and a new Hall pattern with its corresponding output pattern can be loaded (e.g. from a predefined table in memory) by software into MCMOUTS. For the Modulation patterns, signal MCM_ST is used to trigger the transfer.

Loading this shadow register can also be done by writing MCMOUTS.STRHP = 1 (for EXPH and CURH) or MCMOUTS.STRMCMP = 1 (for MCMP).

20.6.3 Hall Mode Flags

Depending on the Hall pattern compare operation, a number of flags are set in order to indicate the status of the module and to trigger further actions and interrupt requests.

Flag **IS.CHE** (Correct Hall Event) is set by signal CM_CHE when the sampled Hall pattern matches the expected one (EXPH). This flag can also be set by SW by setting bit **ISS.SCHE** = 1. If enabled by bit **IEN.ENCHE** = 1, the set signal for CHE can also generate an interrupt request to the CPU. Bit field **INP.INPCHE** defines which service request output becomes activated in case of an interrupt request. To clear flag CHE, SW needs to write **ISR.RCHE** = 1.

Flag **IS.WHE** indicates a Wrong Hall Event. Its handling for flag setting and resetting as well as interrupt request generation are similar to the mechanism for flag CHE.

The implementation of flag STR is done in the same way as for CHE and WHE. This flag is set by HW by the shadow transfer signal MCM_ST (see also [Figure 20-35](#)).

Please note that for flags CHE, WHE, and STR, the interrupt request generation is triggered by the set signal for the flag. That means, a request can be generated even if the flag is already set. There is no need to clear the flag in order to enable further interrupt requests.

The implementation for the IDLE flag is different. It is set by HW through signal CM_WHE if enabled by bit ENIDLE. Software can also set the flag via bit SIDLE. As long as bit IDLE is set, the modulation pattern field MCMP is cleared to force the outputs to the passive state. Flag IDLE must be cleared by software by writing RIDLE = 1 in order to return to normal operation. To fully restart from IDLE mode, the transfer requests for the bit fields in register MCMOUTS to register MCMOUT have to be initiated by software via bits STRMCM and STRHP in register MCMOUTS. In this way, the release from IDLE mode is under software control, but can be performed synchronously to the PWM signal.

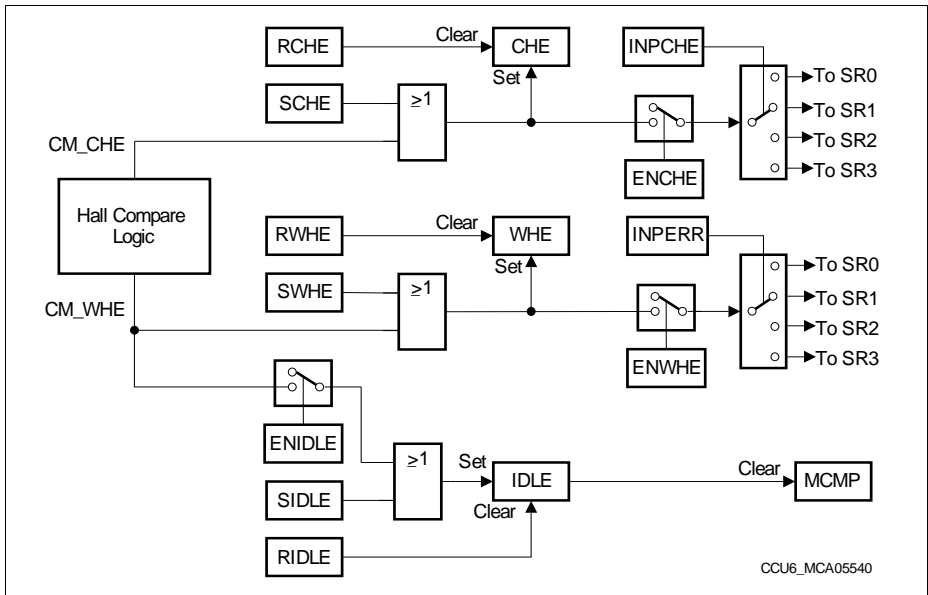


Figure 20-38 Hall Mode Flags

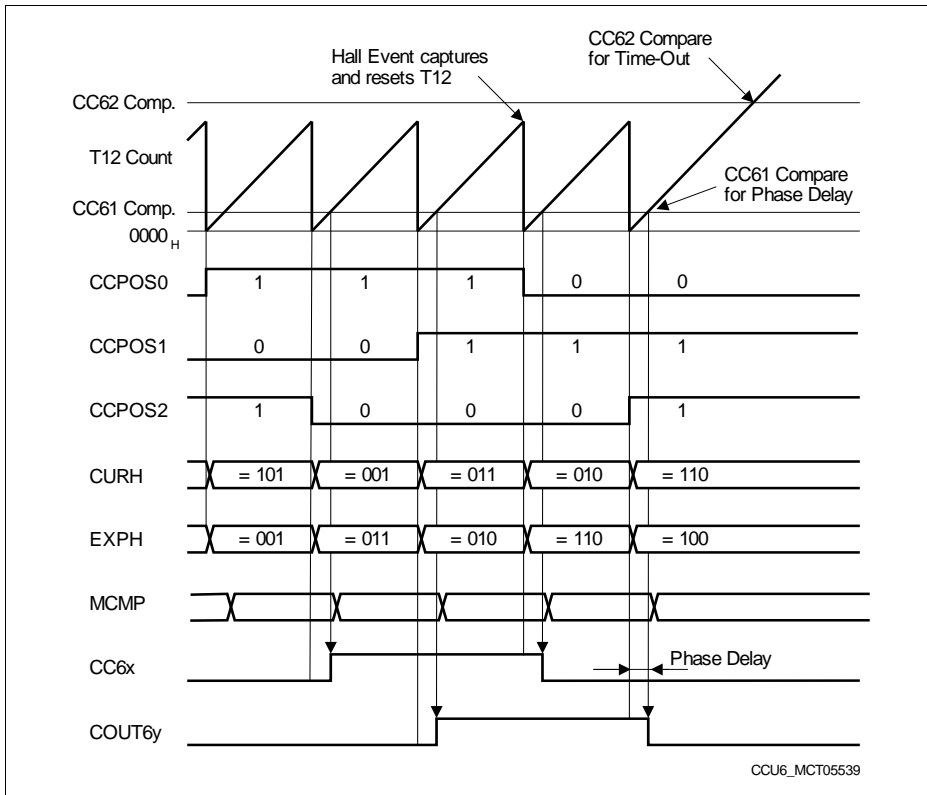


Figure 20-40 Brushless DC-Motor Control Example (all MSEL6x = 1000_B)

After the detection of an expected Hall pattern (CM_CHE active), the T12 count value is captured into channel CC60 (representing the actual rotor speed by measuring the elapsed time between the last two correct Hall events), and T12 is reset. When the timer reaches the compare value in channel CC61, the next multi-channel state is switched by triggering the shadow transfer of bit field MCMP (if enabled in bit field **SWEN**). This trigger event can be combined with the synchronization of the next multi-channel state to the PWM source (to avoid spikes on the output lines, see **Section 20.5**). This compare function of channel CC61 can be used as a phase delay from the position sensor input signals to the switching of the output signals, that is necessary if a sensorless back-EMF technique or Hall sensors are used. The compare value in channel CC62 can be used as a time-out trigger (interrupt), indicating that the actual motor speed is far below the desired destination value. An abnormal load change can be detected with this feature and PWM generation can be disabled.

20.7 Modulation Control Registers

20.7.1 Modulation Control

This register contains bits enabling the modulation of the corresponding output signal by PWM pattern generated by the timers T12 and T13. Furthermore, the multi-channel mode can be enabled as additional modulation source for the output signals.

MODCTR

Modulation Control Register

XSFR(40_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECT 130	0	T13MODEN					MCM EN	0	T12MODEN						
rw	r	rw					rw	r	rw						

Field	Bits	Type	Description
T12MODEN	[5:0]	rw	T12 Modulation Enable These bits enable the modulation of the corresponding output signal by a PWM pattern generated by timer T12. T12MODEN0 = MODCTR.0 for output CC60 T12MODEN1 = MODCTR.1 for output COUT60 T12MODEN2 = MODCTR.2 for output CC61 T12MODEN3 = MODCTR.3 for output COUT61 T12MODEN4 = MODCTR.4 for output CC62 T12MODEN5 = MODCTR.5 for output COUT62 0 _B The modulation of the corresponding output signal by a T12 PWM pattern is disabled. 1 _B The modulation of the corresponding output signal by a T12 PWM pattern is enabled.
MCMEN	7	rw	Multi-Channel Mode Enable 0 _B The modulation of the corresponding output signal by a multi-channel pattern according to bit field MCMOUT is disabled. 1 _B The modulation of the corresponding output signal by a multi-channel pattern according to bit field MCMOUT is enabled.

Field	Bits	Type	Description
T13MODEN	[13:8]	rw	T13 Modulation Enable These bits enable the modulation of the corresponding output signal by the PWM pattern CC63_O generated by timer T13. T13MODEN0 = MODCTR.8 for output CC60 T13MODEN1 = MODCTR.9 for output COUT60 T13MODEN2 = MODCTR.10 for output CC61 T13MODEN3 = MODCTR.11 for output COUT61 T13MODEN4 = MODCTR.12 for output CC62 T13MODEN5 = MODCTR.13 for output COUT62 0 _B The modulation of the corresponding output signal by a T13 PWM pattern is disabled. 1 _B The modulation of the corresponding output signal by a T13 PWM pattern is enabled.
ECT13O	15	rw	Enable Compare Timer T13 Output 0 _B The output COUT63 is in the passive state. 1 _B The output COUT63 is enabled for the PWM signal generated by T13.
0	6, 14	r	reserved; returns 0 if read; should be written with 0;

20.7.2 Trap Control Register

The register TRPCTR controls the trap functionality. It contains independent enable bits for each output signal and control bits to select the behavior in case of a trap condition. The trap condition is a low level on the $\overline{\text{CTR\!AP}}$ input pin, that is monitored (inverted level) by bit IS.TRPF. While TRPF=1 (trap input active), the trap state bit IS.TRPS is set to 1.

TRPCTR

Trap Control Register

XSFR(42_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRP PEN	TRP EN 13	TRPEN						0				TRP M2	TRP M1	TRP M0	
rw	rw	rw						r				rw	rw	rw	

Field	Bits	Type	Description
TRPM1, TRPM0	1, 0	rw	<p>Trap Mode Control Bits 1, 0</p> <p>These two bits define the behavior of the selected outputs when leaving the trap state after the trap condition has become inactive again.</p> <p>A synchronization to the timer driving the PWM pattern avoids unintended pulses when leaving the trap state.</p> <p>The combination [TRPM1, TRPM0] leads to:</p> <p>00_B The trap state is left (return to normal operation) after TRPF has become 0 again when a zero-match of T12 (while counting up) is detected (synchronization to T12).</p> <p>01_B The trap state is left (return to normal operation) after TRPF has become 0 again when a zero-match of T13 is detected (synchronization to T13).</p> <p>10_B reserved</p> <p>11_B The trap state is left (return to normal operation) immediately after TRPF has become 0 again without any synchronization to T12 or T13.</p>

Field	Bits	Type	Description
TRPM2	2	rw	Trap Mode Control Bit 2 This bit defines how the trap flag TRPF <u>can be</u> cleared after the trap input condition ($\overline{\text{CTRAP}} = 0$ and $\text{TRPPEN} = 1$) is no longer valid (either by $\overline{\text{CTRAP}} = 1$ or by $\text{TRPPEN} = 0$). 0_B Automatic Mode: Bit TRPF is cleared by HW if the trap input condition is no longer valid. 1_B Manual Mode: Bit TRPF stays 0 after the trap input condition is no longer valid. It has to be cleared by SW by writing $\text{ISR.RTRPF} = 1$.
TRPEN	[13:8]	rw	Trap Enable Control Setting a bit enables the trap functionality for the following corresponding output signals: $\text{TRPEN0} = \text{TRPCTR.8}$ for output CC60 $\text{TRPEN1} = \text{TRPCTR.9}$ for output COUT60 $\text{TRPEN2} = \text{TRPCTR.10}$ for output CC61 $\text{TRPEN3} = \text{TRPCTR.11}$ for output COUT61 $\text{TRPEN4} = \text{TRPCTR.12}$ for output CC62 $\text{TRPEN5} = \text{TRPCTR.13}$ for output COUT62 0_B The trap functionality of the corresponding output signal is disabled. The output state is independent from bit IS.TRPS. 1_B The trap functionality of the corresponding output signal is enabled. The output state is set to the passive while $\text{IS.TRPS}=1$.
TRPEN13	14	rw	Trap Enable Control for Timer T13 0_B The trap functionality for output COUT63 is disabled. The output state is independent from bit IS.TRPS. 1_B The trap functionality for output COUT63 is enabled. The output state is set to the passive while $\text{IS.TRPS}=1$.

Field	Bits	Type	Description
TRPPEN	15	rw	<p>Trap Pin Enable</p> <p>This bit enables the input (pin) function for the trap generation. An interrupt can <u>only be generated</u> if a falling edge is detected at pin CTRAP while TRPPEN = 1.</p> <p>0_B The CCU6 trap functionality based on the input CTRAP is disabled. A CCU6 trap can only be generated by SW by setting bit TRPF.</p> <p>1_B The CCU6 trap functionality based on the input CTRAP is enabled. A CCU6 trap can be <u>generated</u> by SW by setting bit TRPF or by CTRAP=0.</p>
0	[7:3]	r	<p>reserved; returns 0 if read; should be written with 0;</p>

20.7.3 Passive State Level Register

Register PSLR defines the passive state level of the PWM outputs of the module. The passive state level is the value that is driven during the passive state of the output. During the active state, the corresponding output pin drives the active state level, that is the inverted passive state level. The passive state level permits to adapt the driven output levels to the driver polarity (inverted, not inverted) of the connected power stage. The bits in this register have shadow bit fields to permit a concurrent update of all PWM-related parameters (bit field PSL is updated with T12_ST, whereas PSL63 is updated with T13_ST). The actually used values can be read (attribute "rh"), whereas the shadow bits can only be written (attribute "w").

PSLR

Passive State Level Register

XSFR(44_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								PSL 63	0	PSL					
r								rwh	r	rwh					

Field	Bits	Type	Description
PSL	[5:0]	rwh	Compare Outputs Passive State Level These bits define the passive level driven by the module outputs during the passive state. PSL0 = PSLR.0 for output CC60 PSL1 = PSLR.1 for output COUT60 PSL2 = PSLR.2 for output CC61 PSL3 = PSLR.3 for output COUT61 PSL4 = PSLR.4 for output CC62 PSL5 = PSLR.5 for output COUT62 0 _B The passive level is 0. 1 _B The passive level is 1.
PSL63	7	rwh	Passive State Level of Output COUT63 This bit defines the passive level driven by the module output COUT63 during the passive state. 0 _B The passive level is 0. 1 _B The passive level is 1.
0	6, [15:8]	r	reserved; returns 0 if read; should be written with 0;

20.7.4 Multi-Channel Mode Registers

Register MCMCTR contains control bits for the multi-channel functionality.

MCMCTR

Multi-Channel Mode Control Register

XSFR(4E_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0					STE 13U	STE 12D	STE 12U	0		SWSYN	0		SWSEL		
r					rw	rw	rw	r		rw		r		rw	

Field	Bits	Type	Description
SWSEL	[2:0]	rw	Switching Selection Bit field SWSEL selects one of the following trigger request sources (next multi-channel event) for the shadow transfer MCM_ST from MCMPS to MCMP. The trigger request is stored in the reminder flag R until the shadow transfer is done and flag R is cleared automatically with the shadow transfer. The shadow transfer takes place synchronously with an event selected in bit field SWSYN. 000 _B No trigger request will be generated 001 _B Correct Hall pattern detected (CM_CHE) 010 _B T13 period-match detected (while counting up) 011 _B T12 one-match (while counting down) 100 _B T12 channel 1 compare-match detected (phase delay function) 101 _B T12 period match detected (while counting up) 110 _B reserved, no trigger request will be generated 111 _B reserved, no trigger request will be generated

Field	Bits	Type	Description
SWSYN	[5:4]	rw	Switching Synchronization Bit field SWSYN defines the synchronization mechanism of the shadow transfer event MCM_ST if it has been requested before (flag R set by an event selected by SWSEL) and if MCMEN = 1. This feature permits the synchronization of the outputs to the PWM source, that is used for modulation (T12 or T13). 00 _B Direct; the trigger event immediately leads to the shadow transfer 01 _B A T13 zero-match triggers the shadow transfer 10 _B A T12 zero-match (while counting up) triggers the shadow transfer 11 _B reserved; no action
STE12U	8	rw	Shadow Transfer Enable for T12 Upcounting This bit enables the shadow transfer T12_ST if flag MCMOUT.R is set or becomes set while a T12 period match is detected while counting up. 0 _B No action 1 _B The T12_ST shadow transfer mechanism is enabled if MCMEN = 1.
STE12D	9	rw	Shadow Transfer Enable for T12 Downcounting This bit enables the shadow transfer T12_ST if flag MCMOUT.R is set or becomes set while a T12 one match is detected while counting down. 0 _B No action 1 _B The T12_ST shadow transfer mechanism is enabled if MCMEN = 1.
STE13U	10	rw	Shadow Transfer Enable for T13 Upcounting This bit enables the shadow transfer T13_ST if flag MCMOUT.R is set or becomes set while a T13 period match is detected. 0 _B No action 1 _B The T13_ST shadow transfer mechanism is enabled if MCMEN = 1.
0	3, [7:6], [15:11]	r	reserved; returns 0 if read; should be written with 0;

Capture/Compare Unit 6 (CCU6)

Register MCMOUTS contains bits used as pattern input for the multi-channel mode and the Hall mode. This register is a shadow register (that can be read and written) for register MCMOUT, indicating the currently active signals.

MCMOUTS

Multi-Channel Mode Output Shadow Register

XSFR(4A_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STR HP	0	CURHS			EXPHS			STR MCM	0		MCMPs				
w	r	rw			rw			w	r		rw				

Field	Bits	Type	Description
MCMPs	[5:0]	rw	Multi-Channel PWM Pattern Shadow Bit field MCMPs is the shadow bit field for bit field MCMP. The multi-channel shadow transfer is triggered by MCM_ST according to the transfer conditions defined by register MCMCTR.
STRMCM	7	w	Shadow Transfer Request for MCMPs Writing STRMCM = 1 leads to an immediate activation of MCM_ST to update bit field MCMP by the value of MCMPs. When read, this bit always delivers 0. 0 _B No action. 1 _B Bit field MCMP is updated.
EXPHS	[10:8]	rw	Expected Hall Pattern Shadow Bit field EXPHS is the shadow bit field for bit field EXPH. The shadow transfer takes place when a correct Hall event is detected (CM_CHE).
CURHS	[13:11]	rw	Current Hall Pattern Shadow Bit field CURHS is the shadow bit field for bit field CURH. The shadow transfer takes place when a correct Hall event is detected (CM_CHE).

Field	Bits	Type	Description
STRHP	15	w	Shadow Transfer Request for the Hall Pattern Writing STRHP = 1 leads to an immediate activation of HP_ST to update bit fields EXPH and CURH by EXPHS and CURHS. When read, this bit always delivers 0. 0 _B No action. 1 _B Bit fields EXPH and CURH are updated.
0	6, 14	r	reserved; returns 0 if read; should be written with 0;

MCMOUT

Multi-Channel Mode Output Register

XSFR(4C_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		CURH		EXPH		0		R	MCMP						
r		rh		rh		rh		r	rh			rh			

Field	Bits	Type	Description
MCMP	[5:0]	rh	Multi-Channel PWM Pattern Bit field MCMP defines the output pattern for the multi-channel mode. If this mode is enabled by MODCTR.MCMEN = 1, the output state of all T12 related PWM outputs can be modified. This bit field is 0 while IS.IDLE = 1. MCMP0 = MCMOUT.0 for output CC60 MCMP1 = MCMOUT.1 for output COUT60 MCMP2 = MCMOUT.2 for output CC61 MCMP3 = MCMOUT.3 for output COUT61 MCMP4 = MCMOUT.4 for output CC62 MCMP5 = MCMOUT.5 for output COUT62 0 _B The output is set to the passive state. A PWM generated by T12 or T13 are not taken into account. 1 _B The output can be in the active state, depending on the enabled PWM modulation signals generated by T12, T13 and the trap state.

Field	Bits	Type	Description
R	6	rh	Reminder Flag This flag indicates that the shadow transfer from MCMPS to MCMP has been requested by the selected trigger source. It is cleared when the shadow transfer takes place or while MCMEN=0. 0 _B A shadow transfer MCM_ST is not requested. 1 _B A shadow transfer MCM_ST is requested, but has not yet been executed, because the selected synchronization condition has not yet occurred.
EXPH	[10:8]	rh	Expected Hall Pattern Bit field EXPH is updated by a shadow transfer HP_ST from bit field EXPHS. If HCRDY = 1, EXPH is compared to the sampled CCPOSx inputs in order to detect the occurrence of the next desired (=expected) hall pattern or a wrong pattern. If the sampled hall pattern at the hall input pins is equal to bit field EXPH, a correct Hall event has been detected (CM_CHE).
CURH	[13:11]	rh	Current Hall Pattern Bit field CURH is updated by a shadow transfer HP_ST from bit field CURHS. If HCRDY = 1, CURH is compared to the sampled CCPOSx inputs in order to detect a spike. If the sampled Hall pattern at the Hall input pins is equal to bit field CURH, no Hall event has been detected. If the sampled Hall input pattern is neither equal to CURH nor equal to EXPH, the Hall event was not the desired one and may be due to a fatal error (e.g. blocked rotor, etc.). In this case, a wrong Hall event has been detected (CM_WHE).
0	7, [15:14]	r	reserved; returns 0 if read; should be written with 0;

20.8 Interrupt Handling

This section describes the interrupt handling of the CCU6 module.

20.8.1 Interrupt Structure

The HW interrupt event or the SW setting of the corresponding interrupt set bit (in register ISS) sets the event indication flags (in register IS) and can trigger the interrupt generation. The interrupt pulse is generated independently from the interrupt status flag in register IS (it is not necessary to clear the related status bit to be able to generate another interrupt). The interrupt flag can be cleared by SW by writing to the corresponding bit in register ISR.

If enabled by the related interrupt enable bit in register IEN, an interrupt pulse can be generated on one of the four service request outputs (SR0 to SR3) of the module. If more than one interrupt source is connected to the same interrupt node pointer (in register INP), the requests are logically OR-combined to one common service request output (see [Figure 20-41](#)).

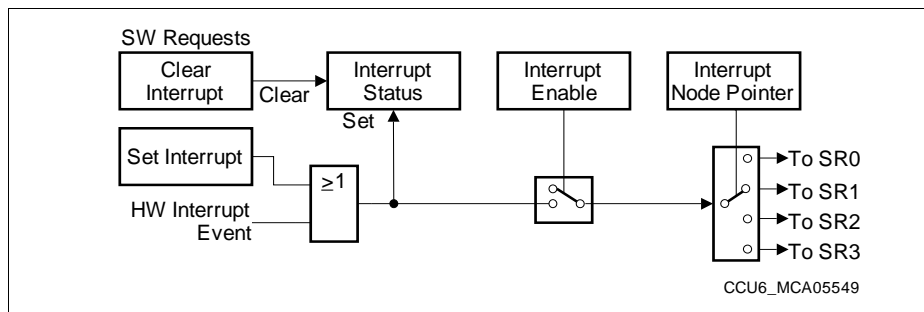


Figure 20-41 General Interrupt Structure

The available interrupt events in the CCU6 are shown in [Figure 20-42](#).

Capture/Compare Unit 6 (CCU6)

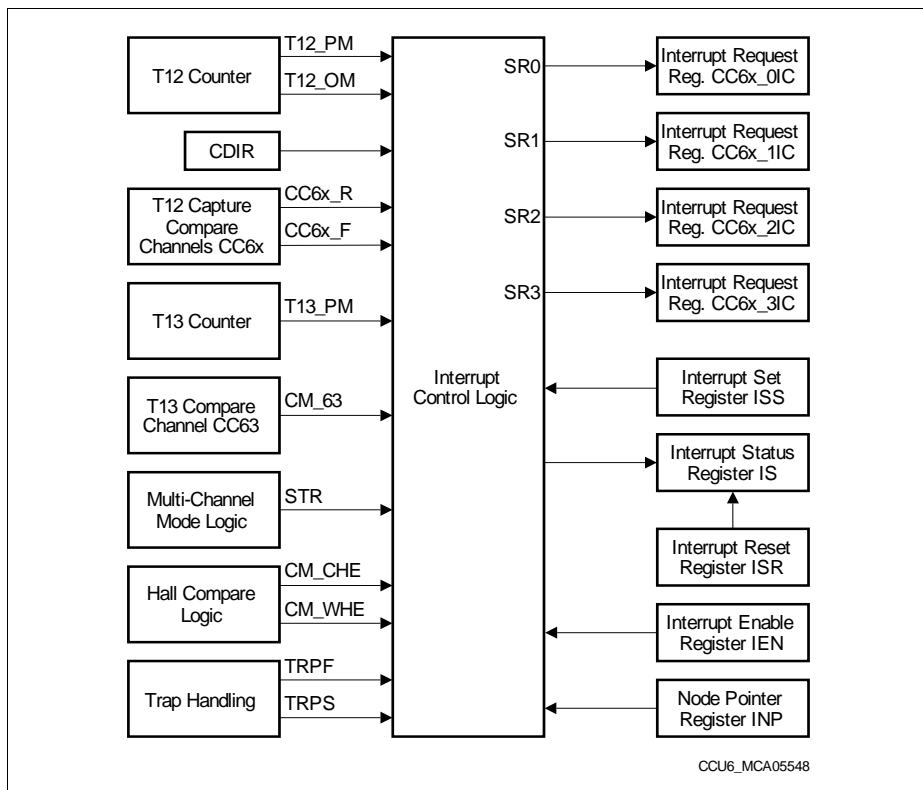


Figure 20-42 Interrupt Sources and Events

20.8.2 Interrupt Registers

20.8.2.1 Interrupt Status Register

Register IS contains the individual interrupt request bits. This register can only be read, write actions have no impact on the contents of this register. The SW can set or clear the bits individually by writing to the registers ISS (to set the bits) or to register ISR (to clear the bits).

The interrupt generation is independent from the value of the bits in register IS, e.g. the interrupt will be generated (if enabled) even if the corresponding bit is already set. The trigger for an interrupt generation is the detection of a set condition (by HW or SW) for the corresponding bit in register IS.

In compare mode (and hall mode), the timer-related interrupts are only generated while the timer is running ($T1xR=1$). In capture mode, the capture interrupts are also generated while the timer T12 is stopped.

Note: Not all bits in register IS can generate an interrupt. Other status bits have been added, that have a similar structure for their set and clear actions. It is recommended that SW checks the interrupt bits bit-wisely (instead of common OR over the bits).

IS

Interrupt Status Register

XSFR(50_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STR	IDLE	WHE	CHE	TRP S	TRP F	T13 PM	T13 CM	T12 PM	T12 OM	ICC 62F	ICC 62R	ICC 61F	ICC 61R	ICC 60F	ICC 60R
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
ICC60R, ICC61R, ICC62R	0, 2, 4	rh	Capture, Compare-Match Rising Edge Flag This bit indicates that event CC6x_R has been detected. This event occurs in compare mode when a compare-match is detected while T12 is counting up (CM_6x and $CDIR = 0$) and in capture mode when a rising edge is detected at the related input CC6xIN. 0 _B The event has not yet been detected. 1 _B The event has been detected.

Field	Bits	Type	Description
ICC60F, ICC61F, ICC62F	1, 3, 5	rh	Capture, Compare-Match Falling Edge Flag This bit indicates that event CC6x_F has been detected. This event occurs in compare mode when a compare-match is detected while T12 is counting down (CM_6x and CDIR = 1) and in capture mode when a falling edge is detected at the related input CC6xIN. 0 _B The event has not yet been detected. 1 _B The event has been detected.
T12OM	6	rh	Timer T12 One-Match Flag This bit indicates that a timer T12 one-match while counting down (T12_OM and CDIR = 1) has been detected. 0 _B The event has not yet been detected. 1 _B The event has been detected.
T12PM	7	rh	Timer T12 Period-Match Flag This bit indicates that a timer T12 period-match while counting up (T12_PM and CDIR = 0) has been detected. 0 _B The event has not yet been detected. 1 _B The event has been detected.
T13CM	8	rh	Timer T13 Compare-Match Flag This bit indicates that a timer T13 compare-match (CM_63) has been detected. 0 _B The event has not yet been detected. 1 _B The event has been detected.
T13PM	9	rh	Timer T13 Period-Match Flag This bit indicates that a timer T13 period-match (T13_PM) has been detected. 0 _B The event has not yet been detected. 1 _B The event has been detected.
TRPF	10	rh	Trap Flag This bit indicates if a trap condition (input $\overline{\text{CTRAP}}$ = 0 or by SW) is / has been detected. If TRM2= 0, it becomes cleared automatically if CTRAP = 1 or TRPPEN = 0, whereas if TRM2 = 1, it has to be cleared by writing RTRPF = 1. 0 _B The trap condition has not been detected. 1 _B The trap condition is / has been detected.

Field	Bits	Type	Description
TRPS	11	rh	Trap State¹⁾ This bit indicates the actual trap state. It is set if TRPF = 1 and becomes cleared according to the mode selected in register TRPCTR. 0 _B The trap state is not active. 1 _B The trap state is active.
CHE	12	rh	Correct Hall Event This bit indicates that a correct Hall event (CM_CHE) has been detected. 0 _B The event has not yet been detected. 1 _B The event has been detected.
WHE	13	rh	Wrong Hall Event This bit indicates that a wrong Hall event (CM_WHE) has been detected. 0 _B The event has not yet been detected. 1 _B The event has been detected.
IDLE	14	rh	IDLE State If enabled by ENIDLE = 1, this bit is set together with bit WHE and it has to be cleared by SW. 0 _B No action. 1 _B Bit field MCMP is cleared, the selected outputs are set to passive state.
STR	15	rh	Multi-Channel Mode Shadow Transfer Request This bit indicates that a shadow transfer from MCMPS to MCMP (MCM_ST) has taken place. 0 _B The event has not yet been detected. 1 _B The event has been detected.

- 1) During the trap state, the selected outputs are set to the passive state. The logic level driven during the passive state is defined by the corresponding bit in register PSLR. Bits TRPS=1 and TRPF=0 can occur if the trap condition is no longer active but the selected synchronization has not yet taken place.

20.8.2.2 Interrupt Status Set Register

Register ISS contains individual interrupt request set bits to generate a CCU6 interrupt request by software. Writing a 1 sets the bit(s) in register IS at the corresponding bit position(s) and can generate an interrupt event (if available and enabled).

All bit positions read as 0.

ISS

Interrupt Status Set Register

XSFR(52_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S
STR	IDLE	WHE	CHE	WHC	TRP	T13	T13	T12	T12	CC	CC	CC	CC	CC	CC
					F	PM	CM	PM	OM	62F	62R	61F	61R	60F	60R
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Field	Bits	Type	Description
SCC60R, SCC61R, SCC62R	0, 2, 4	w	Set Capture, Compare-Match Rising Edge Flag 0 _B No action 1 _B Bit CC6xR will be set.
SCC60F, SCC61F, SCC62F	1, 3, 5	w	Set Capture, Compare-Match Falling Edge Flag 0 _B No action 1 _B Bit CC6xF will be set.
ST12OM	6	w	Set Timer T12 One-Match Flag 0 _B No action 1 _B Bit T12OM will be set.
ST12PM	7	w	Set Timer T12 Period-Match Flag 0 _B No action 1 _B Bit T12PM will be set.
ST13CM	8	w	Set Timer T13 Compare-Match Flag 0 _B No action 1 _B Bit T13CM will be set.
ST13PM	9	w	Set Timer T13 Period-Match Flag 0 _B No action 1 _B Bit T13PM will be set.
STRPF	10	w	Set Trap Flag 0 _B No action 1 _B Bits TRPF and TRPS will be set.

Field	Bits	Type	Description
SWHC	11	w	Software Hall Compare 0 _B No action 1 _B The Hall compare action is triggered.
SCHE	12	w	Set Correct Hall Event Flag 0 _B No action 1 _B Bit CHE will be set.
SWHE	13	w	Set Wrong Hall Event Flag 0 _B No action 1 _B Bit WHE will be set.
SIDLE	14	w	Set IDLE Flag 0 _B No action 1 _B Bit IDLE will be set.
SSTR	15	w	Set STR Flag 0 _B No action 1 _B Bit STR will be set.

20.8.2.3 Status Reset Register

Register ISR contains bits to individually clear the interrupt event flags by software. Writing a 1 clears the bit(s) in register IS at the corresponding bit position(s). All bit positions read as 0.

ISR

Interrupt Status Reset Register

XSFR(54_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R STR	R IDLE	R WHE	R CHE	0	R TRPF	R T13 PM	R T13 CM	R T12 PM	R T12 OM	R CC 62F	R CC 62R	R CC 61F	R CC 61R	R CC 60F	R CC 60R
W	W	W	W	r	W	W	W	W	W	W	W	W	W	W	W

Field	Bits	Type	Description
RCC60R, RCC61R, RCC62R	0, 2, 4	w	Reset Capture, Compare-Match Rising Edge Flag 0 _B No action 1 _B Bit CC6xR will be cleared.
RCC60F, RCC61F, RCC62F	1, 3, 5	w	Reset Capture, Compare-Match Falling Edge Flag 0 _B No action 1 _B Bit CC6xF will be cleared.
RT12OM	6	w	Reset Timer T12 One-Match Flag 0 _B No action 1 _B Bit T12OM will be cleared.
RT12PM	7	w	Reset Timer T12 Period-Match Flag 0 _B No action 1 _B Bit T12PM IS will be cleared.
RT13CM	8	w	Reset Timer T13 Compare-Match Flag 0 _B No action 1 _B Bit T13CM will be cleared.
RT13PM	9	w	Reset Timer T13 Period-Match Flag 0 _B No action 1 _B Bit T13PM will be cleared.
RTRPF	10	w	Reset Trap Flag 0 _B No action 1 _B Bit TRPF will be cleared (not taken into account while input CTRAP=0 and TRPPEN=1.

Field	Bits	Type	Description
RCHE	12	w	Reset Correct Hall Event Flag 0 _B No action 1 _B Bit CHE will be cleared.
RWHE	13	w	Reset Wrong Hall Event Flag 1 _B No action 0 _B Bit WHE will be cleared.
RIDLE	14	w	Reset IDLE Flag 0 _B No action 1 _B Bit IDLE will be cleared.
RSTR	15	w	Reset STR Flag 0 _B No action 1 _B Bit STR will be cleared.
0	11	r	reserved; returns 0 if read; should be written with 0;

20.8.2.4 Interrupt Enable Register

Register IEN contains the interrupt enable bits and a control bit to enable the automatic idle function in the case of a wrong hall pattern.

IEN

Interrupt Enable Register

XSFR(58_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN STR	EN IDLE	EN WHE	EN CHE	0	EN TRP F	EN T13 PM	EN T13 CM	EN T12 PM	EN T12 OM	EN CC 62F	EN CC 62R	EN CC 61F	EN CC 61R	EN CC 60F	EN CC 60R
rw	rw	rw	rw	r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ENCC60R, ENCC61R, ENCC62R	0, 2, 4	rw	Capture, Compare-Match Rising Edge Interrupt Enable for Channel CC6x 0 _B No interrupt will be generated if the set condition for bit CC6xR in register IS occurs. 1 _B An interrupt will be generated if the set condition for bit CC6xR in register IS occurs. The service request output that will be activated is selected by bit field INPCC6x.
ENCC60F, ENCC61F, ENCC62F	1, 3, 5	rw	Capture, Compare-Match Falling Edge Interrupt Enable for Channel CC6x 0 _B No interrupt will be generated if the set condition for bit CC6xF in register IS occurs. 1 _B An interrupt will be generated if the set condition for bit CC6xF in register IS occurs. The service request output that will be activated is selected by bit field INPCC6x.
ENT12OM	6	rw	Enable Interrupt for T12 One-Match 0 _B No interrupt will be generated if the set condition for bit T12OM in register IS occurs. 1 _B An interrupt will be generated if the set condition for bit T12OM in register IS occurs. The service request output that will be activated is selected by bit field INPT12.

Field	Bits	Type	Description
ENT12PM	7	rw	Enable Interrupt for T12 Period-Match 0_B No interrupt will be generated if the set condition for bit T12PM in register IS occurs. 1_B An interrupt will be generated if the set condition for bit T12PM in register IS occurs. The service request output that will be activated is selected by bit field INPT12.
ENT13CM	8	rw	Enable Interrupt for T13 Compare-Match 0_B No interrupt will be generated if the set condition for bit T13CM in register IS occurs. 1_B An interrupt will be generated if the set condition for bit T13CM in register IS occurs. The service request output that will be activated is selected by bit field INPT13.
ENT13PM	9	rw	Enable Interrupt for T13 Period-Match 0_B No interrupt will be generated if the set condition for bit T13PM in register IS occurs. 1_B An interrupt will be generated if the set condition for bit T13PM in register IS occurs. The service request output that will be activated is selected by bit field INPT13.
ENTRPF	10	rw	Enable Interrupt for Trap Flag 0_B No interrupt will be generated if the set condition for bit TRPF in register IS occurs. 1_B An interrupt will be generated if the set condition for bit TRPF in register IS occurs. The service request output that will be activated is selected by bit field INPERR.
ENCHE	12	rw	Enable Interrupt for Correct Hall Event 0_B No interrupt will be generated if the set condition for bit CHE in register IS occurs. 1_B An interrupt will be generated if the set condition for bit CHE in register IS occurs. The service request output that will be activated is selected by bit field INPCHE.

Field	Bits	Type	Description
ENWHE	13	rw	Enable Interrupt for Wrong Hall Event 0 _B No interrupt will be generated if the set condition for bit WHE in register IS occurs. 1 _B An interrupt will be generated if the set condition for bit WHE in register IS occurs. The service request output that will be activated is selected by bit field INPERR.
ENIDLE	14	rw	Enable Idle This bit enables the automatic entering of the idle state (bit IDLE will be set) after a wrong hall event has been detected (bit WHE is set). During the idle state, the bit field MCMP is automatically cleared. 0 _B The bit IDLE is not automatically set when a wrong hall event is detected. 1 _B The bit IDLE is automatically set when a wrong hall event is detected.
ENSTR	15	rw	Enable Multi-Channel Mode Shadow Transfer Interrupt 0 _B No interrupt will be generated if the set condition for bit STR in register IS occurs. 1 _B An interrupt will be generated if the set condition for bit STR in register IS occurs. The service request output that will be activated is selected by bit field INPCHE.
0	11	r	reserved; returns 0 if read; should be written with 0;

20.8.2.5 Interrupt Node Pointer Register

Register INP contains the interrupt node pointers allowing a flexible interrupt handling. These bit fields define which service request output will be activated if the corresponding interrupt event occurs and the interrupt generation for this event is enabled.

INP

Interrupt Node Pointer Register XSFR(56_H) Reset Value: 3940_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		INP T13	INP T12	INP ERR	INP CHE	INP CC62	INP CC61	INP CC60							
r		rw	rw	rw	rw	rw	rw	rw	rw						

Field	Bits	Type	Description
INPCC60, INPCC61, INPCC62	[1:0], [3:2], [5:4]	rw	Interrupt Node Pointer for Channel CC6x Interrupts This bit field defines the service request output activated due to a set condition for bit CC6xR (if enabled by bit ENCC6xR) or for bit CC6xF (if enabled by bit ENCC6xF). 00 _B Service request output SR0 is selected. 01 _B Service request output SR1 is selected. 10 _B Service request output SR2 is selected. 11 _B Service request output SR3 is selected.
INPCHE	[7:6]	rw	Interrupt Node Pointer for the CHE Interrupt This bit field defines the service request output activated due to a set condition for bit CHE (if enabled by bit ENCHE) or for bit STR (if enabled by bit ENSTR). Coding see INPCC6x.
INPERR	[9:8]	rw	Interrupt Node Pointer for Error Interrupts This bit field defines the service request output activated due to a set condition for bit TRPF (if enabled by bit ENTRPF) or for bit WHE (if enabled by bit ENWHE). Coding see INPCC6x.

Field	Bits	Type	Description
INPT12	[11:10]	rw	Interrupt Node Pointer for Timer12 Interrupts This bit field defines the service request output activated due to a set condition for bit T12OM (if enabled by bit ENT12OM) or for bit T12PM (if enabled by bit ENT12PM). Coding see INPCC6x.
INPT13	[13:12]	rw	Interrupt Node Pointer for Timer13 Interrupt This bit field defines the service request output activated due to a set condition for bit T13CM (if enabled by bit ENT13CM) or for bit T13PM (if enabled by bit ENT13PM). Coding see INPCC6x.
0	[15:14]	r	reserved; returns 0 if read; should be written with 0;

20.9 General Module Operation

This section provides information about the:

- Configuration of the behavior of the different device operating modes (see mode control description in [Section 20.9.1](#))
- Input selection (see [Section 20.9.2](#))
- General register description (see [Section 20.9.3](#))

20.9.1 Mode Control

The mode control concept for system control tasks, such as power saving, or suspend request for debugging, allows to program the module behavior under different device operating conditions. The behavior of a CCU6 kernel can be programmed for each of the device operating modes, that are requested by the global state control part of the SCU. Therefore, a CCU6 module provides a kernel state configuration register **KSCFG** defining the behavior in the following device operating modes:

- **Normal operation:**

This operating mode is the default operating mode when neither a suspend request nor a clock-off request are pending. The module clock is not switched off and the CCU6 registers can be read or written. The kernel behavior is defined by KSCFG.NOMCFG.

- **Suspend mode:**

This operating mode is requested when a suspend request (issued by a debugger) is pending in the device. The module clock is not switched off and the CCU6 registers can be read or written. The kernel behavior is defined by KSCFG.SUMCFG.

- **Clock-off mode:**

This operating mode is requested for power saving purposes. The module clock is switched off automatically when all kernels of the CCU6 module reached their specified state in a stop mode. In this case, CCU6 registers can not be accessed. The kernel behavior is defined by KSCFG.COMCFG.

The kernel distinguishes four different blocks (T12, T13, Hall logic, and trap logic). These blocks can be individually enabled for the request of stop mode 0 and stop mode 1 by the sensitivity bits **KSCSR.SBx**. If the request sensitivity is disabled, the block continues normal operation. If the request sensitivity is enabled, the block operates as specified for the selected stop mode.

The complete CCU6 acknowledge is given to the GSC when all four blocks have reached their defined end condition.

Table 20-12 CCU6 Functional Blocks

Block	Function	Sensitivity Bit
0	Timer T12: A functional enable is delivered until the specified stop condition is reached. Then, T12 stops counting and the CC6xIN input stages are frozen.	KSCSR.SB0
1	Timer T13: A functional enable is delivered until the specified stop condition is reached. Then, T13 stops counting.	KSCSR.SB1
2	Hall Logic: The hall logic is stopped immediately and the CCPOSx input stages are frozen.	KSCSR.SB2
3	Trap Logic: The trap logic is stopped immediately and the CTRAP input stage is frozen.	KSCSR.SB3

The behavior of the CCU6 kernel can be programmed for each of the device operating modes (normal operation, suspend mode, clock-off mode). Therefore, it supports four kernel modes, as shown in [Table 20-13](#).

Table 20-13 CCU6 Kernel Behavior

Kernel Mode	Kernel Behavior	Code
run mode 0	kernel operation as specified, no impact on CCU6 operation (same behavior for run mode 0 and run mode 1)	00 _B
run mode 1		01 _B

Table 20-13 CCU6 Kernel Behavior (cont'd)

Kernel Mode	Kernel Behavior	Code
stop mode 0	<p>The sensitivity bits are taken into account for:</p> <p>T12 block: Timer T12 continues normal operation (if running) until they reach the end of the PWM period and then it stops (same stop condition as in single shot mode). When the timer stops, the CC6xIN inputs are frozen.</p> <p>T13 block: Timer T13 continues normal operation (if running) until they reach the end of the PWM period and then it stops (same stop condition as in single shot mode).</p> <p>Hall logic block: The CCPOSx input values are frozen.</p> <p>Trap logic block: The CTRAP input value is frozen.</p>	10 _B
stop mode 1	<p>The output lines enabled for the trap condition are set to their passive values (similar to a trap state). The sensitivity bits are taken into account for:</p> <p>T12 block: Timer T12 stops immediately and CC6xIN inputs are frozen.</p> <p>T13 block: Timer T13 stops.</p> <p>Hall logic block: The CCPOSx input values are frozen.</p> <p>Trap logic block: The CTRAP input value is frozen.</p>	11 _B

Generally, bit field KSCFG.NOMCFG should be configured for run mode 0 as default setting for standard operation. If a CCU6 kernel should not react to a suspend request (and to continue operation as in normal mode), bit field KSCFG.SUMCFG has to be configured with the same value as KSCFG.NOMCFG. If a CCU6 kernel should show a different behavior and stop operation when a specific stop condition is reached, the code for stop mode 0 or stop mode 1 has to be written to KSCFG.SUMCFG.

A similar mechanism applies for the clock-off mode with the possibility to program the desired behavior by bit field KSCFG.COMCFG.

Note: The stop mode selection strongly depends on the application needs and it is very unlikely that different stop modes are required in parallel in the same application. As a result, only one stop mode type (either 0 or 1) should be used in the bit fields in register KSCFG. Do not mix stop mode 0 and stop mode 1 and avoid transitions from stop mode 0 to stop mode 1 (or vice versa) for the CCU6 module.

If the module clock is disabled by KSCFG.MODEN = 0 or in clock-off mode when the stop condition is reached (in stop mode 0 or 1), the module can not be accessed by read or write operations (except register KSCFG that can always be accessed). As a consequence, it can not be configured.

Please note that bit KSCFG.MODEN should only be set by SW while all configuration fields are configured for run mode 0.

20.9.2 Input Selection

Each CCU6 input signal can be selected from a vector of four or eight possible inputs by programming the port input select registers **PISELL** and **PISELH**. This permits to adapt the pin functionality of the device to the application requirements.

The output pins for the module output signals are chosen in the ports.

Naming convention:

The input vector CC60IN[D:A] for input signal CC60IN is composed of the signals CC60INA to CC60IND.

Note: All functional inputs of the CCU6 are synchronized to f_{CC6} before they affect the module internal logic. The resulting delay of $2/f_{CC6}$ and for asynchronous signals an additional uncertainty of $1/f_{CC6}$ have to be taken into account for precise timing calculation. An edge of an input signal can only be correctly detected if the high phase and the low phase of the input signal are both longer than $1/f_{CC6}$.

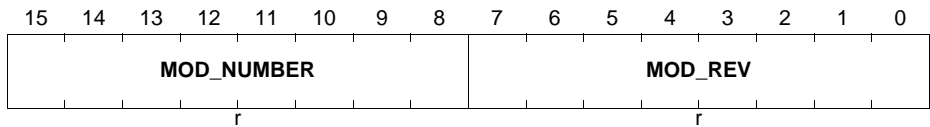
20.9.3 General Registers

20.9.3.1 ID Register

The ID register is a read-only register used for CCU6 module identification purposes. It provides 8 bits for module identification and 8 bits for revision numbering.

ID

Module Identification Register **XSFR(08_H)** **Reset Value: 54XX_H**



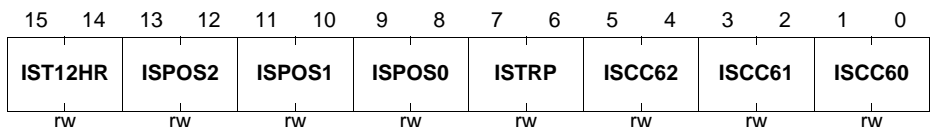
Field	Bits	Type	Description
MOD_REV	[7:0]	r	Module Revision Number Value Bits 7-0 bits are used for module revision numbering. The value of the module revision number starts with 01 _H (first revision), 02 _H , 03 _H , ... up to FF _H .
MOD_NUMBER	[15:8]	r	Module Identification Number Value Bits 15-8 are used for module identification. The CCU6 has the module number 54 _H .

20.9.3.2 Port Input Select Registers

Registers PISELL and PISELH contain bit fields selecting the actual input signal for the module inputs.

PISELL

Port Input Select Register Low **XSFR(04_H)** **Reset Value: 0000_H**



Field	Bits	Type	Description
ISCC60	[1:0]	rw	Input Select for CC60 This bit field defines the input signal used as CC60 capture input. 00 _B The signal CC60INA is selected. 01 _B The signal CC60INB is selected. 10 _B The signal CC60INC is selected. 11 _B The signal CC60IND is selected.
ISCC61	[3:2]	rw	Input Select for CC61 This bit field defines the input signal used as CC61 capture input. 00 _B The signal CC61INA is selected. 01 _B The signal CC61INB is selected. 10 _B The signal CC61INC is selected. 11 _B The signal CC61IND is selected.
ISCC62	[5:4]	rw	Input Select for CC62 This bit field defines the input signal used as CC62 capture input. 00 _B The signal CC62INA is selected. 01 _B The signal CC62INB is selected. 10 _B The signal CC62INC is selected. 11 _B The signal CC62IND is selected.
ISTRP	[7:6]	rw	Input Select for CTRAP This bit field defines the input signal used as CTRAP input. 00 _B The signal CTRAPA is selected. 01 _B The signal CTRAPB is selected. 10 _B The signal CTRAPC is selected. 11 _B The signal CTRAPD is selected.
ISPOS0	[9:8]	rw	Input Select for CCPOS0 This bit field defines the input signal used as CCPOS0 input. 00 _B The signal CCPOS0A is selected. 01 _B The signal CCPOS0B is selected. 10 _B The signal CCPOS0C is selected. 11 _B The signal CCPOS0D is selected.

Field	Bits	Type	Description
ISPOS1	[11:10]	rw	Input Select for CCPOS1 This bit field defines the input signal used as CCPOS1 input. 00 _B The signal CCPOS1A is selected. 01 _B The signal CCPOS1B is selected. 10 _B The signal CCPOS1C is selected. 11 _B The signal CCPOS1D is selected.
ISPOS2	[13:12]	rw	Input Select for CCPOS2 This bit field defines the input signal used as CCPOS2 input. 00 _B The signal CCPOS2A is selected. 01 _B The signal CCPOS2B is selected. 10 _B The signal CCPOS2C is selected. 11 _B The signal CCPOS2D is selected.
IST12HR	[15:14]	rw	Input Select for T12HR This bit field defines the input signal used as T12HR input. 00 _B Either signal T12HRA (if T12EXT = 0) or T12HRE (if T12EXT = 1) is selected. 01 _B Either signal T12HRB (if T12EXT = 0) or T12HRF (if T12EXT = 1) is selected. 10 _B Either signal T12HRC (if T12EXT = 0) or T12HRG (if T12EXT = 1) is selected. 11 _B Either signal T12HRD (if T12EXT = 0) or T12HRH (if T12EXT = 1) is selected.

PISELH

Port Input Select Register High

XSFR(06_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								T13 EXT	T12 EXT	ISCNT13		ISCNT12		IST13HR	
r								rw	rw	rw		rw		rw	

Field	Bits	Type	Description
IST13HR	[1:0]	rw	Input Select for T13HR This bit field defines the input signal used as T13HR input. 00 _B Either signal T13HRA (if T13EXT = 0) or T13HRE (if T13EXT = 1) is selected. 01 _B Either signal T13HRB (if T13EXT = 0) or T13HRF (if T13EXT = 1) is selected. 10 _B Either signal T13HRC (if T13EXT = 0) or T13HRG (if T13EXT = 1) is selected. 11 _B Either signal T13HRD (if T13EXT = 0) or T13HRH (if T13EXT = 1) is selected.
ISCNT12	[3:2]	rw	Input Select for T12 Counting Input This bit field defines the input event leading to a counting action of T12. 00 _B The T12 prescaler generates the counting events. Bit TCTR4.T12CNT is not taken into account. 01 _B Bit TCTR4.T12CNT written with 1 is a counting event. The T12 prescaler is not taken into account. 10 _B The timer T12 is counting each rising edge detected in the selected T12HR signal. 11 _B The timer T12 is counting each falling edge detected in the selected T12HR signal.
ISCNT13	[5:4]	rw	Input Select for T13 Counting Input This bit field defines the input event leading to a counting action of T13. 00 _B The T13 prescaler generates the counting events. Bit TCTR4.T13CNT is not taken into account. 01 _B Bit TCTR4.T13CNT written with 1 is a counting event. The T13 prescaler is not taken into account. 10 _B The timer T13 is counting each rising edge detected in the selected T13HR signal. 11 _B The timer T13 is counting each falling edge detected in the selected T13HR signal.

Field	Bits	Type	Description
T12EXT	6	rw	Extension for T12HR Inputs This bit extends the 2-bit field IST12HR. 0 _B One of the signals T12HR[D:A] is selected. 1 _B One of the signals T12HR[H:E] is selected.
T13EXT	7	rw	Extension for T13HR Inputs This bit extends the 2-bit field IST13HR. 0 _B One of the signals T13HR[D:A] is selected. 1 _B One of the signals T13HR[H:E] is selected.
0	[15:8]	r	reserved; returns 0 if read; should be written with 0;

20.9.3.3 Kernel State Configuration Register

The kernel state configuration register KSCFG allows the selection of the desired kernel modes for the different device operating modes.

Bit fields KSCFG.NOMCFG and KSCFG.COMCFG are reset by an application reset. Bit field KSCFG.SUMCFG is reset by a debug reset.

Note: The coding of the bit fields NOMCFG, SUMCFG and COMCFG is described in [Table 20-13](#).

KSCFG

Kernel State Configuration Register

XSFR(00 _H)											Reset Value: 0000 _H				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BP COM	0	COMCFG	BP SUM	0	SUMCFG	BP NOM	0	NOMCFG	0					BP MOD EN	MOD EN
w	r	rw	w	r	rw	w	r	rw	r	rw		r		w	rw

Field	Bits	Type	Description
MODEN	0	rw	Module Enable This bit enables the module kernel clock and the module functionality. 0 _B The module is switched off immediately (without respecting a stop condition). It does not react on mode control actions and the module clock is switched off. The module does not react on read accesses and ignores write accesses (except to KSCFG). 1 _B The module is switched on and can operate. After writing 1 to MODEN, it is recommended to read register KSCFG to avoid pipeline effects in the control block before accessing other CCU6 registers.
BPMODEN	1	w	Bit Protection for MODEN This bit enables the write access to the bit MODEN. It always reads 0. 0 _B MODEN is not changed. 1 _B MODEN is updated with the written value.

Field	Bits	Type	Description
NOMCFG	[5:4]	rw	Normal Operation Mode Configuration This bit field defines the kernel mode applied in normal operation mode. 00 _B Run mode 0 is selected. 01 _B Run mode 1 is selected. 10 _B Stop mode 0 is selected. 11 _B Stop mode 1 is selected.
BPNO	7	w	Bit Protection for NOMCFG This bit enables the write access to the bit field NOMCFG. It always reads 0. 0 _B NOMCFG is not changed. 1 _B NOMCFG is updated with the written value.
SUMCFG	[9:8]	rw	Suspend Mode Configuration This bit field defines the kernel mode applied in suspend mode. Coding like NOMCFG.
BPSUM	11	w	Bit Protection for SUMCFG This bit enables the write access to the bit field SUMCFG. It always reads 0. 0 _B SUMCFG is not changed. 1 _B SUMCFG is updated with the written value.
COMCFG	[13:12]	rw	Clock Off Mode Configuration This bit field defines the kernel mode applied in clock-off mode. Coding like NOMCFG.
BPCOM	15	w	Bit Protection for COMCFG This bit enables the write access to the bit field COMCFG. It always reads 0. 0 _B COMCFG is not changed. 1 _B COMCFG is updated with the written value.
0	[3:2], 6, 10, 14	r	Reserved returns 0 if read; should be written with 0;

Note: The bit protection bits BPxxx allow partly modification of the configuration bits with a single write operation (without the need of a read-modify-write mechanism handled by the CPU).

20.9.3.4 Kernel State Sensitivity Control Register

The kernel state control sensitivity register bits define which internal block is effected by stop modes 0 and 1.

KSCSR

Kernel State Control Sensitivity Register

XSFR(0E_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
												SB3	SB2	SB1	SB0
												r	rw	rw	rw

Field	Bits	Type	Description
SB0, SB1, SB2, SB3	0, 1, 2, 3	rw	Sensitivity Block x This bit defines if block x of the CCU6 kernel is sensitive to stop mode 0 or stop mode 1. The functional definition of the blocks is given in Table 20-12 . 0 _B Block x is not sensitive to stop mode 0 or stop mode 1 and behaves like in run mode 0. It continues normal operation without respecting the defined stop condition. 1 _B Block x is sensitive to stop mode 0 or stop mode 1. It is respecting the defined stop condition.
0	[15:4]	r	reserved; returns 0 if read; should be written with 0;

20.10 Implementation

This section describes the implementation of the CCU6 modules in the XC27x8X device.

- Address map (see [Section 20.10.1](#))
- Interrupt control registers (see [Section 20.10.2](#))
- Synchronous start (see [Section 20.10.3](#))
- Connections of CCU60 (see [Section 20.10.4.1](#))
- Connections of CCU61 (see [Section 20.10.4.2](#))
- Connections of CCU62 (see [Section 20.10.4.3](#))
- Connections of CCU63 (see [Section 20.10.4.4](#))

20.10.1 Address Map

The four CCU6 modules in the XC27x8X, named CCU60 to CCU63, can be accessed in the following address ranges.

The exact register address is given by the offset of the register (given in [Table 20-1](#)) plus the kernel base address (given in [Table 20-14](#)) of the module.

Table 20-14 Registers Address Space

Module	Base Address	End Address	Note
CCU60	EA00 _H	EA7E _H	
CCU61	EA80 _H	EAFE _H	
CCU62	EB00 _H	EB7E _H	
CCU63	EB80 _H	EBFE _H	

Table 20-15 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
please refer to register table in Section 20.1.3		H	

20.10.2 Interrupt Control Registers

The interrupt control registers are located in the SFR area. They are described in the general interrupt chapter.

Table 20-16 CCU6 Interrupt Control Registers

Short Name	Description
CCU60_0IC	Interrupt Control Register for SR0 of CCU60
CCU60_1IC	Interrupt Control Register for SR1 of CCU60
CCU60_2IC	Interrupt Control Register for SR2 of CCU60
CCU60_3IC	Interrupt Control Register for SR3 of CCU60
CCU61_0IC	Interrupt Control Register for SR0 of CCU61
CCU61_1IC	Interrupt Control Register for SR1 of CCU61
CCU61_2IC	Interrupt Control Register for SR2 of CCU61
CCU61_3IC	Interrupt Control Register for SR3 of CCU61
CCU62_0IC	Interrupt Control Register for SR0 of CCU62
CCU62_1IC	Interrupt Control Register for SR1 of CCU62
CCU62_2IC	Interrupt Control Register for SR2 of CCU62
CCU62_3IC	Interrupt Control Register for SR3 of CCU62
CCU63_0IC	Interrupt Control Register for SR0 of CCU63
CCU63_1IC	Interrupt Control Register for SR1 of CCU63
CCU63_2IC	Interrupt Control Register for SR2 of CCU63
CCU63_3IC	Interrupt Control Register for SR3 of CCU63

20.10.3 Synchronous Start Feature

Synchronous start is supported by bit `SYSCON1.GLCCST` (global capture/compare start) in the SCU module that is connected to the `T12HR` and `T13HR` inputs of all CCU6x modules.

The same signal can also be connected to other capture/compare units in order to allow a synchronous start of the capture/compare timers.

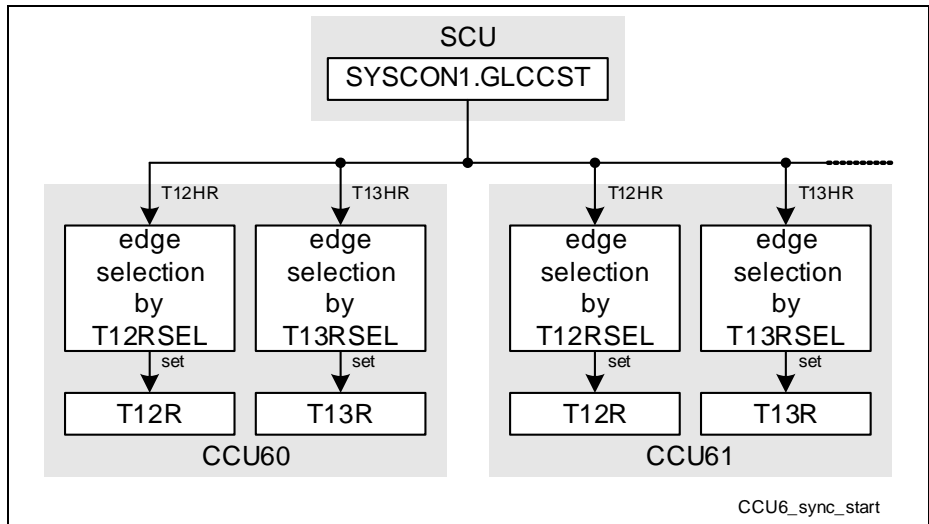


Figure 20-43 Synchronization Concept

20.10.4 Digital Connections

The following tables show the digital connections of the CCU6x modules with other modules or pins in the XC27x8X device.

Each input signal can be selected among 4 or 8 possible input lines, e.g. the input vector for input signal CC60IN is composed of CC60IN[D:A], whereas the input vectors for T12HR and T13HR are composed of T12HR[H:A] and T13HR[H:A].

The following sections refer to the interface signals, whereas the connections of the service request outputs SR[3:0] to the interrupt control registers of each CCU6x to the interrupt control registers is given in [Section 20.10.2](#).

The CCU6x modules are clocked with the XC27x8X system clock, so $f_{CC6} = f_{SYS}$.

Note: All functional inputs of the CCU6 are synchronized to f_{CC6} before they can affect the module internal logic. The resulting delay of $2/f_{CC6}$ and an uncertainty of $1/f_{CC6}$ have to be taken into account for precise timing calculation.

An edge of an input signal can only be correctly detected if both, the high phase and the low phase of the input signal are each longer than $1/f_{CC6}$.

20.10.4.1 Connections of CCU60

This table describes the module interconnections of CCU60.

Table 20-17 CCU60 Digital Connections in XC27x8X

Signal	from/to Module	I/O to CCU60	Can be used to/as
CC60INA	P10.0	I	input signals for capture event on channel CC60
CC60INB	0	I	
CC60INC	0	I	
CC60IND	RTC interrupt	I	
CC61INA	P10.1	I	input signals for capture event on channel CC61
CC61INB	P8.1	I	
CC61INC	0	I	
CC61IND	WUT trigger (SCU)	I	
CC62INA	P10.2	I	input signals for capture event on channel CC62
CC62INB	P8.2	I	
CC62INC	0	I	
CC62IND	0	I	

Table 20-17 CCU60 Digital Connections in XC27x8X (cont'd)

Signal	from/to Module	I/O to CCU60	Can be used to/as
CTRAPA	P10.6	I	input signals for CTRAP, the ESRx input refers to the synchronized input signal, which can be filtered (if enabled)
CTRAPB	P8.6	I	
CTRAPC	ESR2	I	
CTRAPD	ERU_PDOUT2	I	
CCPOS0A	P10.7	I	input signals for CCPOS0
CCPOS0B	P9.7	I	
CCPOS0C	CCU61_SR3	I	
CCPOS0D	0	I	
CCPOS1A	P10.8	I	input signals for CCPOS1
CCPOS1B	P9.6	I	
CCPOS1C	CCU63_SR3	I	
CCPOS1D	0	I	
CCPOS2A	P10.9	I	input signals for CCPOS2
CCPOS2B	P9.5	I	
CCPOS2C	ADC0_SR3	I	
CCPOS2D	0	I	
T12HRA	CCU63_MCM_ST	I	input signals for T12HR
T12HRB	P5.5	I	
T12HRC	P5.8	I	
T12HRD	SYSCON.GLCCST	I	
T12HRE	ADC0_ARBCNT	I	
T12HRF	0	I	
T12HRG	0	I	
T12HRH	0	I	

Table 20-17 CCU60 Digital Connections in XC27x8X (cont'd)

Signal	from/to Module	I/O to CCU60	Can be used to/as
T13HRA	EXTCLK (SCU)	I	input signals for T13HR
T13HRB	CCU60_T12_ZM	I	
T13HRC	P5.8	I	
T13HRD	SYSCON.GLCCST	I	
T13HRE	ADC0_ARBCNT	I	
T13HRF	0	I	
T13HRG	U0C0_SR3	I	
T13HRH	0	I	
CC60	P10.0	O	compare outputs of channel CC60
CC60	ADC0_REQGT0H	O	
COUT60	P10.3 P8.3	O	
CC61	P10.1 P8.1	O	compare outputs of channel CC61
CC61	ADC0_REQGT1H	O	
COUT61	P10.4 P8.4	O	
CC62	P10.2 P8.2	O	compare outputs of channel CC62
CC62	ADC0_REQGT2H	O	
COUT62	P10.5 P8.5	O	
COUT63	P10.7 P10.10 P8.6 U0C0_DX2F U0C1_DX2F	O	compare output of channel CC63
COUT63	ADCx_REQGTyA	O	ADC triggers
T12_ZM	CCU60_T13HRB	O	T12 zero match
T13_PM	ERU_OGU02	O	T13 period match

Table 20-17 CCU60 Digital Connections in XC27x8X (cont'd)

Signal	from/to Module	I/O to CCU60	Can be used to/as
MCM_ST	CCU61_T12HRA ERU_OGU01	O	MCM shadow transfer
SR3	CCU61_CCPOS0C	O	CCU61 trigger
SR3	CCU63_CCPOS1C	O	CCU63 trigger

20.10.4.2 Connections of CCU61

This table describes the module interconnections of CCU61.

Table 20-18 CCU61 Digital Connections in XC27x8X

Signal	from/to Module	I/O to CC61	Can be used to/as
CC60INA	P0.0	I	input signals for capture event on channel CC60
CC60INB	P11.5	I	
CC60INC	0	I	
CC60IND	0	I	
CC61INA	P0.1	I	input signals for capture event on channel CC61
CC61INB	P11.2	I	
CC61INC	0	I	
CC61IND	0	I	
CC62INA	P0.2	I	input signals for capture event on channel CC62
CC62INB	P11.4	I	
CC62INC	0	I	
CC62IND	0	I	
CTRAPA	P0.6	I	input signals for CTRAP, the ESRx input refers to the synchronized input signal, that can be filtered (if enabled)
CTRAPB	P0.7	I	
CTRAPC	ESR2	I	
CTRAPD	P11.1	I	
CCPOS0A	P4.5	I	input signals for CCPOS0
CCPOS0B	0	I	
CCPOS0C	CCU60_SR3	I	
CCPOS0D	0	I	
CCPOS1A	P4.6	I	input signals for CCPOS1
CCPOS1B	0	I	
CCPOS1C	CCU62_SR3	I	
CCPOS1D	0	I	

Table 20-18 CCU61 Digital Connections in XC27x8X (cont'd)

Signal	from/to Module	I/O to CC61	Can be used to/as
CCPOS2A	P4.7	I	input signals for CCPOS2
CCPOS2B	0	I	
CCPOS2C	ADC1_SR3	I	
CCPOS2D	0	I	
T12HRA	CCU60_MCM_ST	I	input signals for T12HR
T12HRB	P1.2	I	
T12HRC	P5.8	I	
T12HRD	SYSCON.GLCCST	I	
T12HRE	ADC0_ARBCNT	I	
T12HRF	0	I	
T12HRG	0	I	
T12HRH	0	I	
T13HRA	P5.10	I	input signals for T13HR
T13HRB	CCU61_T12_ZM	I	
T13HRC	P5.8	I	
T13HRD	SYSCON.GLCCST	I	
T13HRE	ADC0_ARBCNT	I	
T13HRF	P11.3	I	
T13HRG	U1C0_SR3	I	
T13HRH	0	I	
CC60	P0.0 P11.5	O	compare outputs of channel CC60
COU60	P0.3 P11.0	O	
CC61	P0.1 P11.2	O	compare outputs of channel CC61
COU61	P0.4 P11.1	O	

Table 20-18 CCU61 Digital Connections in XC27x8X (cont'd)

Signal	from/to Module	I/O to CC61	Can be used to/as
CC62	P0.2 P11.4	O	compare outputs of channel CC62
COUT62	P0.5 P11.3	O	
COUT63	P0.6 P11.3 P11.5 U1C0_DX2F U1C1_DX2F	O	compare output of channel CC63
COUT63	ADCx_REQGTyB	O	ADC triggers
T12_ZM	CCU61_T13HRB	O	T12 zero match
T13_PM	ERU_OGU12	O	T13 period match
MCM_ST	CCU62_T12HRA ERU_OGU11	O	MCM shadow transfer
SR3	CCU60_CCPOS0C	O	CCU60 trigger
SR3	CCU62_CCPOS1C	O	CCU62 trigger
SR3	ADC0_REQTRyC	O	ADC0 trigger

20.10.4.3 Connections of CCU62

This table describes the module interconnections of CCU62.

Table 20-19 CCU62 Digital Connections in XC27x8X

Signal	from/to Module	I/O to CCU62	Can be used to/as
CC60INA	P1.7	I	input signals for capture event on channel CC60
CC60INB	P8.3	I	
CC60INC	0	I	
CC60IND	0	I	
CC61INA	P1.6	I	input signals for capture event on channel CC61
CC61INB	P8.4	I	
CC61INC	0	I	
CC61IND	0	I	
CC62INA	P1.2	I	input signals for capture event on channel CC62
CC62INB	P8.5	I	
CC62INC	0	I	
CC62IND	0	I	
CTRAPA	P7.1	I	input signals for CTRAP, the ESRx input refers to the synchronized input signal, which can be filtered (if enabled)
CTRAPB	P1.0	I	
CTRAPC	ESR2	I	
CTRAPD	P8.6	I	
CCPOS0A	P7.2	I	input signals for CCPOS0
CCPOS0B	P4.1	I	
CCPOS0C	CCU63_SR3	I	
CCPOS0D	0	I	
CCPOS1A	P7.3	I	input signals for CCPOS1
CCPOS1B	P4.2	I	
CCPOS1C	CCU61_SR3	I	
CCPOS1D	0	I	

Table 20-19 CCU62 Digital Connections in XC27x8X (cont'd)

Signal	from/to Module	I/O to CCU62	Can be used to/as
CCPOS2A	P7.4	I	input signals for CCPOS2
CCPOS2B	P4.3	I	
CCPOS2C	ADC0_SR3	I	
CCPOS2D	0	I	
T12HRA	CCU61_MCM_ST	I	edge detection off input signals for T12HR
T12HRB	P1.3	I	
T12HRC	P5.8	I	
T12HRD	SYSCON.GLCCST	I	
T12HRE	ADC1_ARBCNT	I	
T12HRF	0	I	
T12HRG	0	I	
T12HRH	0	I	
T13HRA	CAN_INT_O15	I	input signals for T13HR
T13HRB	CCU62_T12_ZM	I	
T13HRC	P5.8	I	
T13HRD	SYSCON.GLCCST	I	
T13HRE	ADC1_ARBCNT	I	
T13HRF	0	I	
T13HRG	U2C0_SR3	I	
T13HRH	0	I	
CC60	P1.7 P8.3	O	compare outputs of channel CC60
COU60	P1.5 P9.7	O	
CC61	P1.6 P8.4	O	compare outputs of channel CC61
COU61	P1.4 p9.6	O	

Table 20-19 CCU62 Digital Connections in XC27x8X (cont'd)

Signal	from/to Module	I/O to CCU62	Can be used to/as
CC62	P1.2 P8.5	O	compare outputs of channel CC62
COUT62	P1.1 P9.5	O	
COUT63	P1.3 P9.4 P9.7 U2C0_DX2F U2C1_DX2F	O	compare output of channel CC63
COUT63	ADCx_REQGTyC	O	ADC triggers
T12_ZM	CCU62_T13HRB	O	T12 zero match
T13_PM	ERU_OGU22	O	T13 period match
MCM_ST	CCU63_T12HRA ERU_OGU21	O	MCM shadow transfer
SR3	CCU61_CCPOS1C	O	CCU61 trigger
SR3	CCU63_CCPOS0C	O	CCU63 trigger
SR3	ADC1_REQTRyC	O	ADC1 trigger

20.10.4.4 Connections of CCU63

This table describes the module interconnections of CCU63.

Table 20-20 CCU63 Digital Connections in XC27x8X

Signal	from/to Module	I/O to CCU63	Can be used to/as
CC60INA	P9.0	I	input signals for capture event on channel CC60
CC60INB	P2.0	I	
CC60INC	0	I	
CC60IND	0	I	
CC61INA	P9.1	I	input signals for capture event on channel CC61
CC61INB	P2.1	I	
CC61INC	0	I	
CC61IND	0	I	
CC62INA	P9.2	I	input signals for capture event on channel CC62
CC62INB	P2.2	I	
CC62INC	0	I	
CC62IND	0	I	
CTRAPA	P9.6	I	input signals for CTRAP, the ESRx input refers to the synchronized input signal, which can be filtered (if enabled)
CTRAPB	P9.7	I	
CTRAPC	ESR2	I	
CTRAPD	ERU_PDOUT3	I	
CCPOS0A	P11.0	I	input signals for CCPOS0
CCPOS0D	0	I	
CCPOS0C	CCU62_SR3	I	
CCPOS0D	0	I	
CCPOS1A	P11.1	I	input signals for CCPOS1
CCPOS1B	0	I	
CCPOS1C	CCU60_SR3	I	
CCPOS1D	0	I	

Table 20-20 CCU63 Digital Connections in XC27x8X (cont'd)

Signal	from/to Module	I/O to CCU63	Can be used to/as
CCPOS2A	P11.2	I	input signals for CCPOS2
CCPOS2B	0	I	
CCPOS2C	ADC1_SR3	I	
CCPOS2D	0	I	
T12HRA	CCU62_MCM_ST	I	input signals for T12HR
T12HRB	P5.4	I	
T12HRC	P5.8	I	
T12HRD	SYSCON.GLCCST	I	
T12HRE	ADC1_ARBCNT	I	
T12HRF	0	I	
T12HRG	0	I	
T12HRH	0	I	
T13HRA	CAN_INT_O15	I	input signals for T13HR
T13HRB	CCU63_T12_ZM	I	
T13HRC	P5.8	I	
T13HRD	SYSCON.GLCCST	I	
T13HRE	ADC1_ARBCNT	I	
T13HRF	P5.13	I	
T13HRG	U3C0_SR3	I	
T13HRH	0	I	
CC60	P9.0 P2.0	O	compare outputs of channel CC60
CC60	ADC1_REQGT0H	O	
COU60	P2.13 P9.3	O	
CC61	P9.1 P2.1	O	compare outputs of channel CC61
CC61	ADC1_REQGT1H	O	
COU61	P9.4 P10.7	O	

Table 20-20 CCU63 Digital Connections in XC27x8X (cont'd)

Signal	from/to Module	I/O to CCU63	Can be used to/as
CC62	P9.2 P2.2	O	compare outputs of channel CC62
CC62	ADC1_REQGT2H	O	
COUT62	P9.5 P9.6 P10.12	O	
COUT63	P9.6 P2.3 U3C0_DX2F U3C1_DX2F	O	compare output of channel CC63
COUT63	ADCx_REQGTyD	O	ADC triggers
T12_ZM	CCU63_T13HRB	O	T12 zero match
T13_PM	ERU_OGU32	O	T13 period match
MCM_ST	CCU60_T12HRA ERU_OGU31	O	MCM shadow transfer
SR3	CCU60_CCPOS1C	O	CCU60 trigger
SR3	CCU62_CCPOS0C	O	CCU62 trigger

21 Universal Serial Interface Channel

The **Universal Serial Interface Channel** module (USIC) is a flexible interface module covering several serial communication protocols. A USIC module contains two independent communication channels named UxC0 and UxC1, with x being the number of the USIC module (e.g. channel y of USIC module x is referenced as UxCy). The user can program during run-time which protocol will be handled by each communication channel and which pins are used.

This chapter is structured as follows:

- Introduction (see [Page 21-1](#))
- Operating the USIC (see [Page 21-13](#))
- ASC protocol for UART and LIN (see [Page 21-110](#))
- SSC protocol (see [Page 21-131](#))
- IIC protocol (see [Page 21-161](#))
- IIS protocol (see [Page 21-185](#))
- Module implementation in XC27x8X (see [Page 21-205](#))

21.1 Introduction

This section gives an overview about the feature set of the USIC and introduces the USIC structure. It describes the:

- Feature set overview (see [Page 21-2](#))
- Channel structure (see [Page 21-5](#))
- Input stages (see [Page 21-6](#))
- Output signals (see [Page 21-7](#))
- Baud rate generator (see [Page 21-8](#))
- Channel events and interrupts (see [Page 21-9](#))
- Data shifting and handling (see [Page 21-9](#))

21.1.1 Feature Set Overview

Each USIC channel can be individually configured to match the application needs, e.g. the protocol can be selected or changed during run time without the need for a reset. The following protocols are supported:

- **UART** (ASC, asynchronous serial channel)
 - Module capability: receiver/transmitter with max. baud rate $f_{\text{SYS}} / 4$
 - Wide baud rate range down to single-digit baud rates
 - Number of data bits per data frame: 1 to 63
 - MSB or LSB first
- **LIN** Support by hardware (Local Interconnect Network)
 - Data transfers based on ASC protocol
 - Baud rate detection possible by built-in capture event of baud rate generator
 - Checksum generation under software control for higher flexibility
- **SSC/SPI** (synchronous serial channel with or without slave select lines)
 - Module capability: maximum baud rate $f_{\text{SYS}} / 2$, limited by loop delay
 - Number of data bits per data frame 1 to 63, more with explicit stop condition
 - MSB or LSB first
- **IIC** (Inter-IC Bus)
 - Application baud rate 100 kbit/s to 400 kbit/s
 - 7-bit and 10-bit addressing supported
 - Full master and slave device capability
- **IIS** (infotainment audio bus)
 - Module capability: maximum baud rate $f_{\text{SYS}} / 2$

Note: The real baud rates that can be achieved in a real application depend on the operating frequency of the device, timing parameters as described in the Data Sheet, signal delays on the PCB and timings of the peer device.

In addition to the flexible choice of the communication protocol, the USIC structure has been designed to reduce the system load (CPU load) allowing efficient data handling. The following aspects have been considered:

- **Data buffer capability**
 The standard buffer capability includes a double word buffer for receive data and a single word buffer for transmit data. This allows longer CPU reaction times (e.g. interrupt latency).
- **Additional FIFO buffer capability**
 In addition to the standard buffer capability, the received data and the data to be transmitted can be buffered in a FIFO buffer structure. The size of the receive and the transmit FIFO buffer can be programmed independently. Depending on the application needs, a total buffer capability of 64 data words can be assigned to the receive and transmit FIFO buffers of a USIC module (the two channels of the USIC module share the 64 data word buffer).

In addition to the FIFO buffer, a bypass mechanism allows the introduction of high-priority data without flushing the FIFO buffer.

- **Transmit control information**

For each data word to be transmitted, a 5-bit transmit control information has been added to automatically control some transmission parameters, such as word length, frame length, or the slave select control for the SPI protocol. The transmit control information is generated automatically by analyzing the address where the user software has written the data word to be transmitted (32 input locations = $2^5 = 5$ bit transmit control information).

This feature allows individual handling of each data word, e.g. the transmit control information associated to the data words stored in a transmit FIFO can automatically modify the slave select outputs to select different communication targets (slave devices) without CPU load. Alternatively, it can be used to control the frame length.

- **Flexible frame length control**

The number of bits to be transferred within a data frame is independent of the data word length and can be handled in two different ways. The first option allows automatic generation of frames up to 63 bits with a known length. The second option supports longer frames (even unlimited length) or frames with a dynamically controlled length.

- **Interrupt capability**

The events of each USIC channel can be individually routed to one of 4 service request outputs SR[3:0], depending on the application needs. Furthermore, specific start and end of frame indications are supported in addition to protocol-specific events.

- **Flexible interface routing**

Each USIC channel offers the choice between several possible input and output pins connections for the communications signals. This allows a flexible assignment of USIC signals to pins that can be changed without resetting the device.

- **Input conditioning**

Each input signal is handled by a programmable input conditioning stage with programmable filtering and synchronization capability.

- **Baud rate generation**

Each USIC channel contains an own baud rate generator. The baud rate generation can be based either on the internal module clock or on an external frequency input. This structure allows data transfers with a frequency that can not be generated internally, e.g. to synchronize several communication partners.

- **Transfer trigger capability**

In master mode, data transfers can be triggered by events generated outside the USIC module, e.g. at an input pin or a timer unit (transmit data validation). This feature allows time base related data transmission.

- **Debugger support**

The USIC offers specific addresses to read out received data without interaction with

Universal Serial Interface Channel

the FIFO buffer mechanism. This feature allows debugger accesses without the risk of a corrupted receive data sequence.

To reach a desired baud rate, two criteria have to be respected, the module capability and the application environment. The module capability is defined with respect to the module's input clock frequency, being the base for the module operation. Although the module's capability being much higher (depending on the module clock and the number of module clock cycles needed to represent a data bit), the reachable baud rate is generally limited by the application environment. In most cases, the application environment limits the maximum reachable baud rate due to driver delays, signal propagation times, or due to EMI reasons.

Note: Depending on the selected additional functions (such as digital filters, input synchronization stages, sample point adjustment, data structure, etc.), the maximum reachable baud rate can be limited. Please also take care about additional delays, such as (internal or external) propagation delays and driver delays (e.g. for collision detection in ASC mode, for IIC, etc.).

21.1.2 Channel Structure

The USIC module contains two independent communication channels, with a structure as shown in [Figure 21-1](#).

The data shift unit and the data buffering of each channel support full-duplex data transfers. The protocol-specific actions are handled by the protocol pre-processors (PPP). In order to simplify data handling, an additional FIFO data buffer is optionally available for each USIC module to store transmit and receive data for each channel. This FIFO data buffer is not necessarily available in all devices (please refer to USIC implementation chapter for details).

Due to the independent channel control and baud rate generation, the communication protocol, baud rate and the data format can be independently programmed for each communication channel.

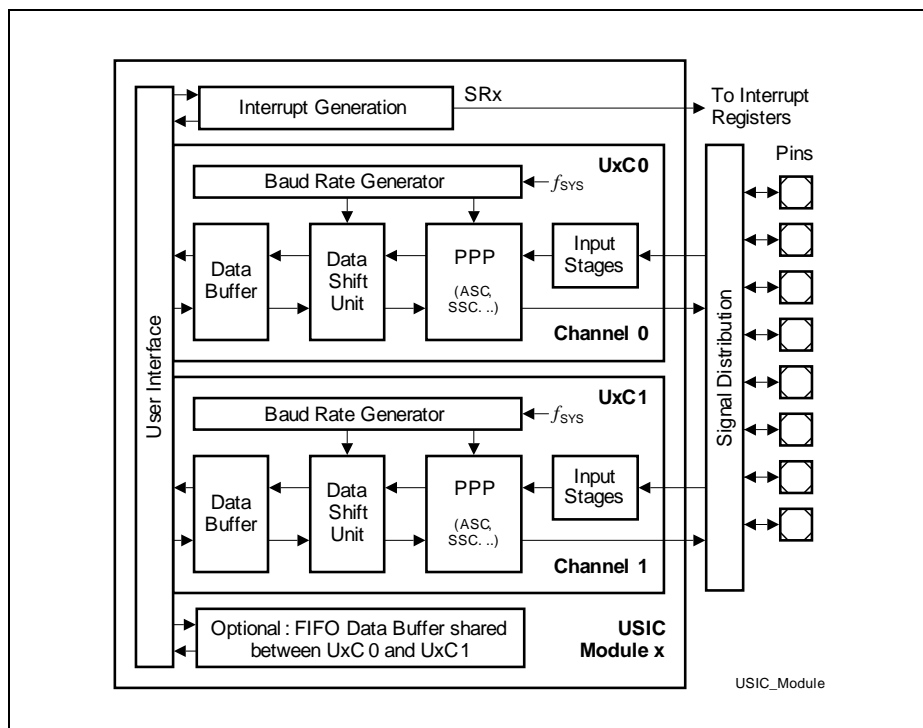


Figure 21-1 USIC Module/Channel Structure

21.1.3 Input Stages

For each protocol up to three input signals are available, the number of actually used inputs depends on the selected protocol. Each input signal is handled by an input stage (called DX0, DX1, DX2) for signal conditioning, such as input selection, polarity control, or a digital input filter. They can be classified according to their meaning for the protocols, see [Table 21-1](#).

The inputs marked as “optional” are not needed for the standard function of a protocol and may be used for enhancements. The descriptions of protocol-specific items are given in the related protocol chapters, for the external frequency input please refer to the baud rate generator, and for the transmit data validation to the data handling section.

Table 21-1 Input Signals for Different Protocols

Selected Protocol	Shift Data Input (handled by DX0)	Shift Clock Input (handled by DX1)	Shift Control Input (handled by DX2)
ASC, LIN	RXD	optional: external frequency input or TXD collision detection	optional: transmit data validation
SSC, SPI (Master)	DIN (MRST, MISO)	optional: external frequency input or delay compensation	optional: transmit data validation or delay compensation
SSC, SPI (Slave)	DIN (MTSR, MOSI)	SCLKIN	SELIN
IIC	SDA	SCL	optional: transmit data validation
IIS (Master)	DIN	optional: external frequency input or delay compensation	optional: transmit data validation or delay compensation
IIS (Slave)	DIN	SCLKIN	WAIN

Note: To allow a certain flexibility in assigning required USIC input functions to port pins of the device, each input stage can select the desired input location among several possibilities.

The available USIC signals and their port locations are listed in the implementation chapter, see [Page 21-212](#).

21.1.4 Output Signals

For each protocol up to eleven protocol-related output signals are available, the number of actually used outputs depends on the selected protocol. They can be classified according to their meaning for the protocols, see [Table 21-2](#).

The outputs marked as “optional” are not needed for the standard function of a protocol and may be used for enhancements. The descriptions of protocol-specific items are given in the related protocol chapters. The MCLKOUT output signal has a stable frequency relation to the shift clock output (the frequency of MCLKOUT can be higher than for SCLKOUT) for synchronization purposes of a slave device to a master device. If the baud rate generator is not needed for a specific protocol (e.g. in SSC slave mode), the SCLKOUT and MCLKOUT signals can be used as clock outputs with 50% duty cycle with a frequency that can be independent from the communication baud rate.

Table 21-2 Output Signals for Different Protocols

Selected Protocol	Shift Data Output DOUT	Shift Clock Output SCLKOUT	Shift Control Outputs SELO[7:0]	Master Clock Output MCLKOUT
ASC, LIN	TXD	not used	not used	optional: master time base
SSC, SPI (master)	DOUT (MTSR, MOSI)	master shift clock	slave select, chip select	optional: master time base
SSC, SPI (slave)	DOUT (MRST, MISO)	optional: independent clock output	not used	optional: independent clock output
IIC	SDA	SCL	not used	optional: master time base
IIS (master)	DOUT	master shift clock	WA	optional: master time base
IIS (slave)	DOUT	optional: independent clock output	not used	optional: independent clock output

Note: To allow a certain flexibility in assigning required USIC output functions to port pins of the device, most output signals are made available on several port pins. The port control itself defines pin-by-pin which signal is used as output signal for a port pin (see port chapter).

The available USIC signals and their port locations are listed in the implementation chapter, see [Page 21-212](#).

21.1.5 Baud Rate Generator

Each USIC Channel contains a baud rate generator structured as shown in **Figure 21-2**. It is based on coupled divider stages, providing the frequencies needed for the different protocols. It contains:

- A fractional divider to generate the input frequency $f_{PIN} = f_{FD}$ for baud rate generation based on the internal system frequency f_{SYS} .
- The DX1 input to generate the input frequency $f_{PIN} = f_{DX1}$ for baud rate generation based on an external signal.
- A protocol-related counter to provide the master clock signal MCLK, the shift clock signal SCLK, and other protocol-related signals. It can also be used for time interval measurement, e.g. baud rate detection.
- A time quanta counter associated to the protocol pre-processor defining protocol-specific timings, such shift control signals or bit timings, based on the input frequency f_{CTQIN} .
- The output signals MCLKOUT and SCLKOUT of the protocol-related divider that can be made available on pins. In order to adapt to different applications, some output characteristics of these signals can be configured.

For device-specific details about availability of USIC signals on pins please refer to the implementation section.

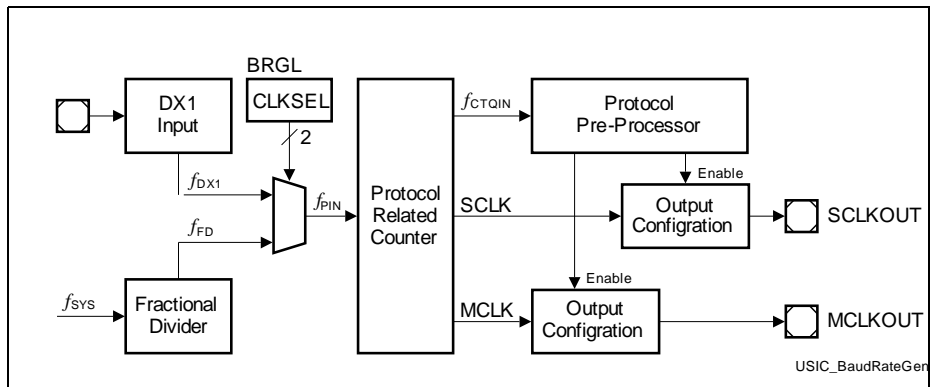


Figure 21-2 Baud Rate Generator

21.1.6 Channel Events and Interrupts

The notification of the user about events occurring during data traffic and data handling is based on:

- Data transfer events related to the transmission or reception of a data word, independent of the selected protocol.
- Protocol-specific events depending on the selected protocol.
- Data buffer events related to data handling by the optional FIFO data buffers.

21.1.7 Data Shifting and Handling

The data handling of the USIC module is based on an independent data shift unit (DSU) and a buffer structure that is similar for the supported protocols. The data shift and buffer registers are 16-bit wide (maximum data word length), but several data words can be concatenated to achieve longer data frames. The DSU inputs are the shift data (handled by input stage DX0), the shift clock (handled by the input stage DX1), and the shift control (handled by the input stage DX2). The signal DOUT represents the shift data output.

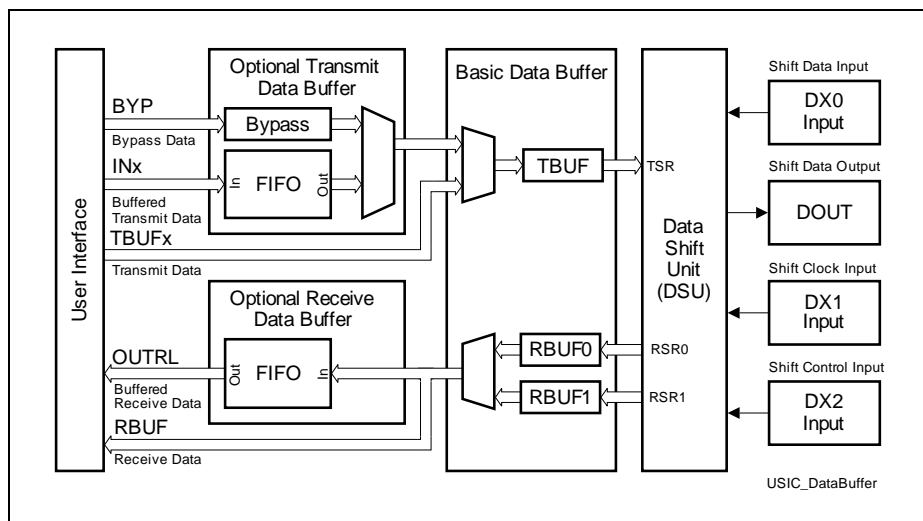


Figure 21-3 Principle of Data Buffering

The principle of data handling comprises:

- A transmitter with a transmit shift register (TSR) in the DSU and a transmit data buffer (TBUF). A data validation scheme allows triggering and gating of data transfers by external events under certain conditions.
- A receiver with two alternating receive shift registers (RSR0 and RSR1) in the DSU and a double receive buffer structure (RBUF0, RBUF1). The alternating receive shift

registers support the reception of data streams and data frames longer than one data word.

- Optional transmit and receive data buffers according to the first-in-first-out principle (FIFO), that are not necessarily available in all devices. For device-specific details about availability of the FIFO buffer please refer to the USIC implementation chapter.
- A user interface to handle data, interrupts, and status and control information.

21.1.7.1 Basic Data Buffer Structure

The read access to received data and the write access of data to be transmitted can be handled by a basic data buffer structure.

The received data stored in the receiver buffers RBUF0/RBUF1 can be read directly from these registers. In this case, the user has to take care about the reception sequence to read these registers in the correct order. To simplify the use of the receive buffer structure, register RBUF has been introduced. A read action from this register delivers the data word received first (oldest data) to respect the reception sequence. With a read access from at least the low byte of RBUF, the data is automatically declared to be no longer new and the next received data word becomes visible in RBUF and can be read out next.

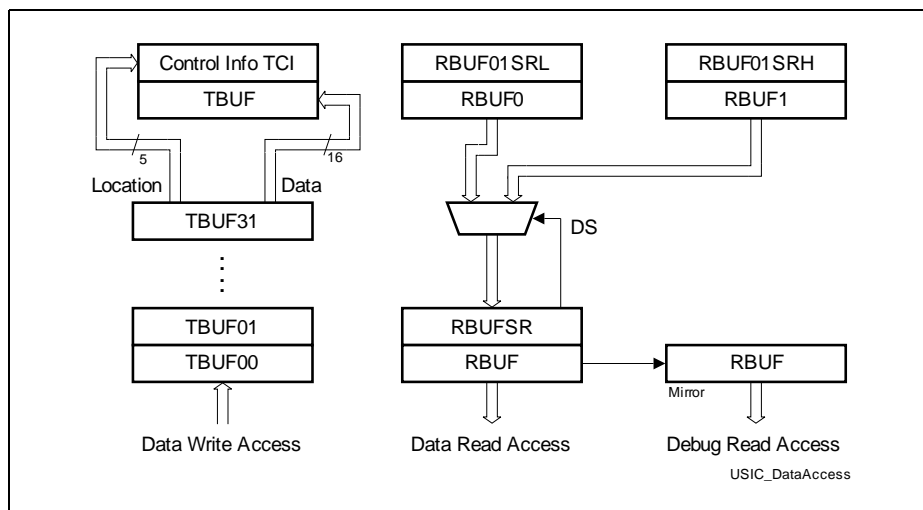


Figure 21-4 Data Access Structure without additional Data Buffer

It is recommended to read the received data words by accesses to RBUF and to avoid handling of RBUF0 and RBUF1. The USIC module also supports the use of debug accesses to receive data words. Debugger read accesses should not disturb the receive data sequence and, as a consequence, should not target RBUF. Therefore, register

RBUFD has been introduced. It contains the same value as RBUF, but a read access from RBUFD does not change the status of the data (same data can be read several times). In addition to the received data, some additional status information about each received data word is available in the receiver buffer status registers RBUF01SRL/H (related to data in RBUF0 and RBUF1) and RBUFSR (related to data in RBUF).

Transmit data can be loaded to TBUF by software by writing to the transmit buffer input locations TBUF_x (x = 00-31), consisting of 32 consecutive addresses. The data written to one of these input locations is stored in the transmit buffer TBUF. Additionally, the address of the written location is evaluated and can be used for additional control purposes. This 5-bit wide information (named **Transmit Control Information TCI**) can be used for different purposes in different protocols.

21.1.7.2 FIFO Buffer Structure

To allow easier data setup and handling, an additional data buffering mechanism can be optionally supported. The data buffer is based on the first-in-first-out principle (FIFO) that ensures that the sequence of transferred data words is respected.

If a FIFO buffer structure is used, the data handling scheme (data with associated control information) is similar to the one without FIFO. The additional FIFO buffer can be independently enabled/disabled for transmission and reception (e.g. if data FIFO buffers are available for a specific USIC channel, it is possible to configure the transmit data path without and the receive data path with FIFO buffering).

The transmit FIFO buffer is addressed by using 32 consecutive address locations for IN_x instead of TBUF_x (x=00-31) regardless of the FIFO depth. The 32 addresses are used to store the 5-bit TCI (together with the written data) associated with each FIFO entry.

The receive FIFO can be read out at two independent addresses, OUTR and OUTDRL instead of RBUF and RBUFD. A read from the OUTR location triggers the next data packet to be available for the next read (general FIFO mechanism). In order to allow non-intrusive debugging (without risk of data loss), a second address location (OUTDRL) has been introduced. A read at this location delivers the same value as OUTR, but without modifying the FIFO contents.

The transmit FIFO also has the capability to bypass the data stream and to load bypass data to TBUF. This can be used to generate high-priority messages or to send an emergency message if the transmit FIFO runs empty. The transmission control of the FIFO buffer can also use the transfer trigger and transfer gating scheme of the transmission logic for data validation (e.g. to trigger data transfers by events).

Note: The available size of a FIFO data buffer for a USIC channel depends on the specific device. Please refer to the implementation chapter for details about available FIFO buffer capability.

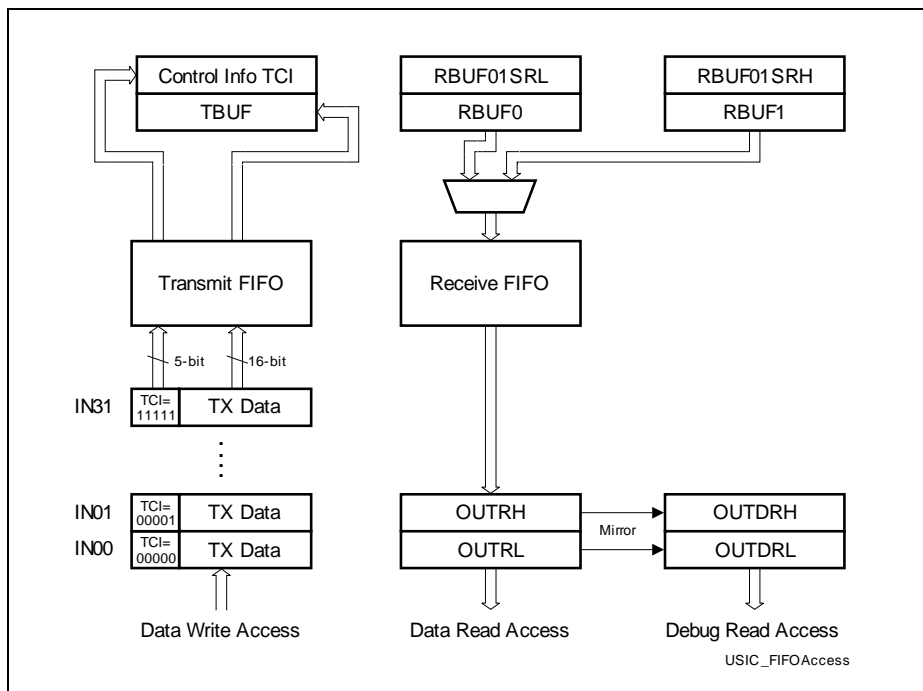


Figure 21-5 Data Access Structure with FIFO

21.2 Operating the USIC

This section describes how to operate the USIC communication channel.
It describes:

- Register Overview (see [Page 21-13](#))
- General channel operation (see [Page 21-18](#))
- Channel control and configuration registers (see [Page 21-25](#))
- Protocol related registers (see [Page 21-33](#))
- Input stages (see [Page 21-36](#))
- Input stage control registers (see [Page 21-38](#))
- Baud rate generation (see [Page 21-41](#))
- Baud rate and shift control registers (see [Page 21-46](#))
- Operating the transmit path (see on [Page 21-51](#))
- Operating the receive path (see [Page 21-55](#))
- Transfer control and status registers (see [Page 21-57](#))
- Data buffer registers (see [Page 21-69](#))
- Operating the FIFO data buffer (see [Page 21-79](#))
- FIFO buffer and bypass registers (see [Page 21-89](#))

21.2.1 Register Overview

The module itself being 32-bit wide, some registers have been split up in two parts for the 16-bit implementation. Both parts keep the same name as the former 32-bit register, with an additional index. The lower part ends with the index L, whereas the upper (higher) part ends with the index H. Former 32-bit registers consisting of only 16 used bits keep their name (without additional index), because only the used bits appear in the register map.

Table 21-3 shows all registers which are required for programming a USIC channel, as well as the FIFO buffer. It summarizes the USIC communication channel registers and defines the relative addresses and the reset values.

Please note that all registers can be accessed with any access width (8-bit, 16-bit), independent of the described width. Short addressing is not supported.

All USIC registers (except bit field KSCFG.SUMCFG) are always reset by a class 3 reset. Bit field KSCFG.SUMCFG is reset by a class 1 reset.

Note: The register bits marked “w” always deliver 0 when read. They are used to modify flip-flops in other registers or to trigger internal actions.

Universal Serial Interface Channel

Figure 21-6 shows the register types of the USIC module registers and channel registers. In a specific microcontroller, module registers of USIC module “x” are marked by the module prefix “USICx_”. Channel registers of USIC module “x” are marked by the channel prefix “UxC0_” and “UxC1_”.

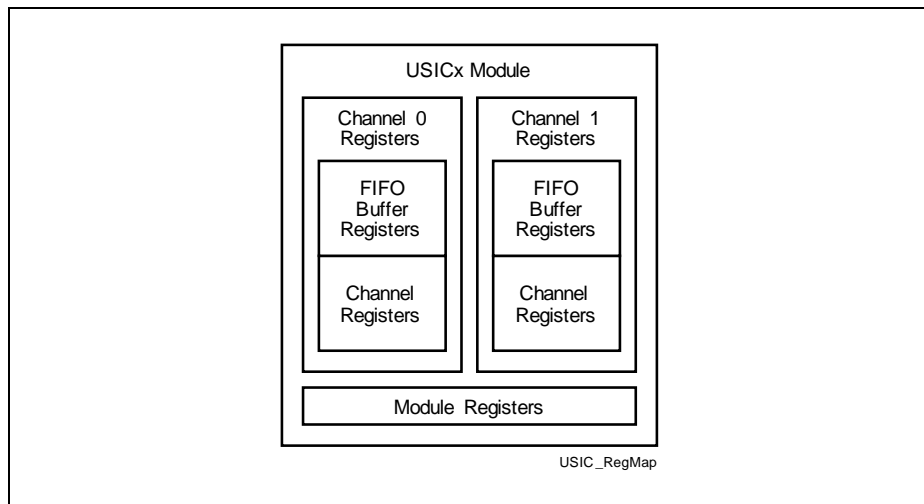


Figure 21-6 USIC Module and Channel Registers

Table 21-3 USIC Kernel-Related and Kernel Registers

Register Short Name	Register Long Name	Offset Addr.	Reset Value	Description see
Module Registers¹⁾				
IDL	Module Identification Register L	008 _H	C0XX _H	
IDH	Module Identification Register H	00A _H	003A _H	
Channel Registers				
FDRL	Fractional Divider Register L	004 _H	0000 _H	Page 21-46
FDRH	Fractional Divider Register H	006 _H	0000 _H	Page 21-47
KSCFG	Kernel State Configuration Register	00C _H	0000 _H	Page 21-29
CCR	Channel Control Register	010 _H	0000 _H	Page 21-25
INPRL	Interrupt Node Pointer Register L	014 _H	0000 _H	Page 21-31
INPRH	Interrupt Node Pointer Register H	016 _H	0000 _H	Page 21-32
CCFG	Channel Configuration Register	018 _H	00CF _H	Page 21-28
BRGL	Baud Rate Generator Register L	01C _H	0000 _H	Page 21-48

Table 21-3 USIC Kernel-Related and Kernel Registers (cont'd)

Register Short Name	Register Long Name	Offset Addr.	Reset Value	Description see
BRGH	Baud Rate Generator Register H	01E _H	0000 _H	Page 21-50
DX0CR	Input Control Register 0	020 _H	0000 _H	Page 21-38
DX1CR	Input Control Register 1	024 _H	0000 _H	
DX2CR	Input Control Register 2	028 _H	0000 _H	
SCTRL	Shift Control Register L	030 _H	0000 _H	Page 21-57
SCTRH	Shift Control Register H	032 _H	0000 _H	Page 21-59
FMRL	Flag Modification Register L	038 _H	0000 _H	Page 21-67
FMRH	Flag Modification Register H	03A _H	0000 _H	Page 21-68
TCSRL	Transmit Control/Status Register L	03C _H	0000 _H	Page 21-60
TCSRH	Transmit Control/Status Register H	03E _H	0000 _H	Page 21-65
PCRL	Protocol Control Register L	040 _H	0000 _H	Page 21-33 ²⁾
				Page 21-123 ³⁾
				Page 21-152 ⁴⁾
				Page 21-179 ⁵⁾
				Page 21-199 ⁶⁾
PCRH	Protocol Control Register H	042 _H	0000 _H	Page 21-33 ²⁾
				Page 21-126 ³⁾
				Page 21-154 ⁴⁾
				Page 21-179 ⁵⁾
				Page 21-201 ⁶⁾

Table 21-3 USIC Kernel-Related and Kernel Registers (cont'd)

Register Short Name	Register Long Name	Offset Addr.	Reset Value	Description see
PSR	Protocol Status Register	044 _H	0000 _H	Page 21-34 ²⁾
				Page 21-127 ³⁾
				Page 21-156 ⁴⁾
				Page 21-182 ⁵⁾
				Page 21-202 ⁶⁾
PSCR	Protocol Status Clear Register	048 _H	0000 _H	Page 21-35
RBUFD	Receiver Buffer Register for Debugger	04C _H	0000 _H	Page 21-77
RBUF0	Receiver Buffer Register 0	050 _H	0000 _H	Page 21-70
RBUF1	Receiver Buffer Register 1	054 _H	0000 _H	Page 21-73
RBUFSR	Receiver Buffer Status Register	058 _H	0000 _H	Page 21-78
RBUF	Receiver Buffer Register	05C _H	0000 _H	Page 21-76
RBUF01SRL	Receiver Buffer 01 Status Register L	060 _H	0000 _H	Page 21-70
RBUF01SRH	Receiver Buffer 01 Status Register H	062 _H	0000 _H	Page 21-73
–	Reserved; do not access this location.	06C _H	–	–
–	Reserved; do not access this location.	06E _H	–	–
TBUFx	Transmit Buffer Input Location x (x = 00-31)	080 _H + x*4	0000 _H	Page 21-69

FIFO Buffer Registers

BYP	Bypass Data Register	100 _H	0000 _H	Page 21-89
BYPCRL	Bypass Control Register L	104 _H	0000 _H	Page 21-89
BYP CRH	Bypass Control Register H	106 _H	0000 _H	Page 21-91
TRBPTRL	Transmit/Receive Buffer Pointer Register L	108 _H	0000 _H	Page 21-108
TRBPTRH	Transmit/Receive Buffer Pointer Register H	10A _H	0000 _H	Page 21-109

Table 21-3 USIC Kernel-Related and Kernel Registers (cont'd)

Register Short Name	Register Long Name	Offset Addr.	Reset Value	Description see
TBCTRL	Transmit Buffer Control Register L	110 _H	0000 _H	Page 21-98
TBCTRH	Transmit Buffer Control Register H	112 _H	0000 _H	Page 21-99
RBCTRL	Receive Buffer Control Register L	114 _H	0000 _H	Page 21-101
RBCTRH	Receive Buffer Control Register H	116 _H	0000 _H	Page 21-102
TRBSRL	Transmit/Receive Buffer Status Register L	118 _H	0808 _H	Page 21-92
TRBSRH	Transmit/Receive Buffer Status Register H	11A _H	0000 _H	Page 21-95
TRBSCR	Transmit/Receive Buffer Status Clear Register	11C _H	0000 _H	Page 21-96
OUTRL	Receive Buffer Output Register L	120 _H	0000 _H	Page 21-106
OUTRH	Receive Buffer Output Register H	122 _H	0000 _H	Page 21-106
OUTDRL	Receive Buffer Output Register L for Debugger	124 _H	0000 _H	Page 21-107
OUTDRH	Receive Buffer Output Register H for Debugger	126 _H	0000 _H	Page 21-107
INx	Transmit FIFO Buffer Input Location x (x = 00-31)	180 _H + x*4	0000 _H	Page 21-105

- 1) Details of the module identification registers are described in the implementation section (see [Page 21-208](#)).
- 2) This page shows the general register layout.
- 3) This page shows the register layout in ASC mode.
- 4) This page shows the register layout in SSC mode.
- 5) This page shows the register layout in IIC mode.
- 6) This page shows the register layout in IIS mode.

21.2.2 Operating the USIC Communication Channel

This section describes how to operate a USIC communication channel, including protocol control and status, mode control and interrupt handling. The following aspects have to be taken into account:

- Enable the USIC module for operation and configure the behavior for the different device operation modes (see [Page 21-19](#)).
- Configure the pinning (refer to description in the corresponding protocol section).
- Configure the data structure (shift direction, word length, frame length, polarity, etc.).
- Configure the data buffer structure of the optional FIFO buffer area. A FIFO buffer can only be enabled if the related bit in register CCFG is set.
- Select a protocol by CCR.MODE. A protocol can only be selected if the related bit in register CCFG is set.

21.2.2.1 Protocol Control and Status

The protocol-related control and status information are located in the protocol control registers PCRL and PCRH and in the protocol status register PSR. These registers are shared between the available protocols. As a consequence, the meaning of the bit positions in these registers is different within the protocols.

Use of PCRL/H Bits

The signification of the bits in registers PCRL/PCRH is indicated by the protocol-related alias names for the different protocols.

- PCRL/PRCH for the ASC protocol (see [Page 21-123](#))
- PCRL/PRCH for the SSC protocol (see [Page 21-152](#))
- PCRL/PRCH for the IIC protocol (see [Page 21-179](#))
- PCRL/PRCH for the IIS protocol (see [Page 21-199](#))

Use of PSR Flags

The signification of the flags in register PSR is indicated by the protocol-related alias names for the different protocols.

- PSR flags for the ASC protocol (see [Page 21-127](#))
- PSR flags for the SSC protocol (see [Page 21-156](#))
- PSR flags for the IIC protocol (see [Page 21-182](#))
- PSR flags for the IIS protocol (see [Page 21-202](#))

21.2.2.2 Mode Control

The mode control concept for system control tasks, such as power saving, or suspend request for debugging, allows to program the module behavior under different device operating conditions. The behavior of a communication channel can be programmed for each of the device operating modes, that are requested by the global state control part of the SCU. Therefore, each communication channel has an associated kernel state configuration register KSCFG defining its behavior in the following operating modes:

- Normal operation:
This operating mode is the default operating mode when neither a suspend request nor a clock-off request are pending. The module clock is not switched off and the USIC registers can be read or written. The channel behavior is defined by KSCFG.NOMCFG.
- Suspend mode:
This operating mode is requested when a suspend request is pending in the device. The module clock is not switched off and the USIC registers can be read or written. The channel behavior is defined by KSCFG.SUMCFG.
- Clock-off mode:
This operating mode is requested for power saving purposes. The module clock is switched off automatically when all channels of the USIC module reached their specified state in a stop mode. In this case, USIC registers can not be accessed. The channel behavior is defined by KSCFG.COMCFG.

The behavior of a USIC communication channel can be programmed for each of the device operating modes (normal operation, suspend mode, clock-off mode). Therefore, the USIC communication channel provides four kernel modes, as shown in [Table 21-4](#).

Table 21-4 USIC Communication Channel Behavior

Kernel Mode	Channel Behavior	KSCFG. NOMCFG
Run mode 0	Channel operation as specified, no impact on data transfer	00 _B
Run mode 1		01 _B
Stop mode 0	Explicit stop condition as described in the protocol chapters	10 _B
Stop mode 1		11 _B

Generally, bit field KSCFG.NOMCFG should be configured for run mode 0 as default setting for standard operation. If a communication channel should not react to a suspend request (and to continue its operation as in normal mode), bit field KSCFG.SUMCFG has to be configured with the same value as KSCFG.NOMCFG. If the communication channel should show a different behavior and stop operation when a specific stop condition is reached, the code for stop mode 0 or stop mode 1 have to be written to KSCFG.SUMCFG.

A similar mechanism applies for the clock-off mode with the possibility to program the desired behavior by bit field KSCFG.COMCFG.

The stop conditions are defined for the selected protocol (see mode control description in the protocol section).

Note: The stop mode selection strongly depends on the application needs and it is very unlikely that different stop modes are required in parallel in the same application. As a result, only one stop mode type (either 0 or 1) should be used in the bit fields in register KSCFG. Do not mix stop mode 0 and stop mode 1 and avoid transitions from stop mode 0 to stop mode 1 (or vice versa) for the same communication channel.

If the module clock is disabled by KSCFG.MODEN = 0 or in clock-off mode when the stop condition is reached (in stop mode 0 or 1), the module can not be accessed by read or write operations (except register KSCFG that can always be accessed).

21.2.2.3 General Channel Events and Interrupts

The general event and interrupt structure is shown in [Figure 21-7](#). If a defined condition is met, an event is detected and an event indication flag becomes automatically set. The flag stays set until it is cleared by software. If enabled, an interrupt can be generated if an event is detected. The actual status of the event indication flag has no influence on the interrupt generation. As a consequence, the event indication flag does not need to be cleared to generate further interrupts.

Additionally, the service request output SRx of the USIC channel that becomes activated in case of an event condition can be selected by an interrupt node pointer. This structure allows to assign events to interrupts, e.g. depending on the application, several events can share the same interrupt routine (several events activate the same SRx output) or can be handled individually (only one event activates one SRx output).

The SRx outputs are connected to interrupt control registers to handle the CPU reaction to the service requests. This assignment is described in the implementation section on [Page 21-210](#).

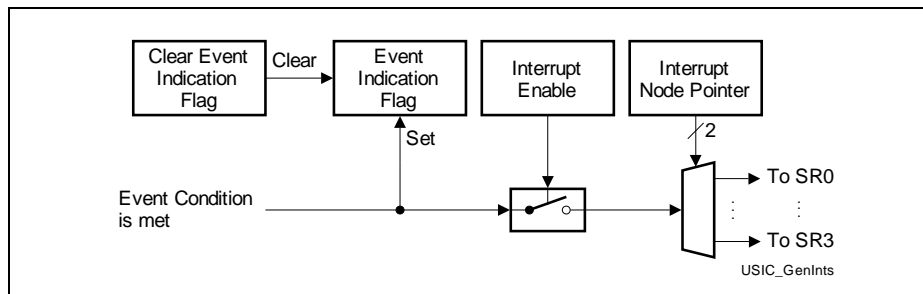


Figure 21-7 General Event and Interrupt Structure

21.2.2.4 Data Transfer Events and Interrupts

The data transfer events are based on the transmission or reception of a data word. The related indication flags are located in register PSR. All events can be individually enabled for interrupt generation.

- **Receive event to indicate that a data word has been received:**
 If a new received word becomes available in the receive buffer RBUF, either a receive event or an alternative receive event occurs.
 The receive event occurs if bit RBUFSR.PERR = 0. It is indicated by flag PSR.RIF and, if enabled, leads to receive interrupt.
- **Receiver start event to indicate that a data word reception has started:**
 When the receive clock edge that shifts in the first bit of a new data word is detected and reception is enabled, a receiver start event occurs. It is indicated by flag PSR.RSIF and, if enabled, leads to transmit buffer interrupt.
 In full duplex mode, this event follows half a shift clock cycle after the transmit buffer event and indicates when the shift control settings are internally “frozen” for the current data word reception and a new setting can be programmed.
 In SSC and IIS mode, the transmit data valid flag TCSRL.TDV is cleared in single shot mode with the receiver start event.
- **Alternative receive event to indicate that a specific data word has been received:**
 If a new received word becomes available in the receive buffer RBUF, either a receive event or an alternative receive event occurs.
 The alternative receive event occurs if bit RBUFSR.PERR = 1. It is indicated by flag PSR.AIF and, if enabled, leads to alternative receive interrupt.
 Depending on the selected protocol, bit RBUFSR.PERR is set to indicate a parity error in ASC mode, the reception of the first byte of a new frame in IIC mode, and the WA information about right/left channel in IIS mode. In SSC mode, it is used as indication if the received word is the first data word, and is set if first and reset if not.
- **Transmit shift event to indicate that a data word has been transmitted:**
 A transmit shift event occurs with the last shift clock edge of a data word. It is indicated by flag PSR.TSIF and, if enabled, leads to transmit shift interrupt.
- **Transmit buffer event to indicate that a data word transmission has been started:**
 When a data word from the transmit buffer TBUF has been loaded to the shift register and a new data word can be written to TBUF, a transmit buffer event occurs. This happens with the transmit clock edge that shifts out the first bit of a new data word and transmission is enabled. It is indicated by flag PSR.TBIF and, if enabled, leads to transmit buffer interrupt.
 This event also indicates when the shift control settings (word length, shift direction, etc.) are internally “frozen” for the current data word transmission.
 In ASC and IIC mode, the transmit data valid flag TCSRL.TDV is cleared in single shot mode with the transmit buffer event.
- **Data lost event to indicate a loss of the oldest received data word:**
 If the data word available in register RBUF (oldest data word from RBUF0 or RBUF1)

Universal Serial Interface Channel

has not been read out before it becomes overwritten with new incoming data, this event occurs. It is indicated by flag PSR.DLIF and, if enabled, leads to a protocol interrupt.

Table 21-5 shows the registers, bits and bit fields indicating the data transfer events and controlling the interrupts of a USIC channel.

Table 21-5 Data Transfer Events and Interrupt Handling

Event	Indication Flag	Indication cleared by	Interrupt enabled by	SRx Output selected by
Standard receive event	PSR.RIF	PSCR.CRIF	CCR.RIEN	INPRL.RINP
Receive start event	PSR.RSIF	PSCR.CRSIF	CCR.RSIEN	INPRL.TBINP
Alternative receive event	PSR.AIF	PSCR.CAIF	CCR.AIEN	INPRL.AINP
Transmit shift event	PSR.TSIF	PSCR.CTSIF	CCR.TSIEN	INPRL.TSINP
Transmit buffer event	PSR.TBIF	PSCR.CTBIF	CCR.TBIEN	INPRL.TBINP
Data lost event	PSR.DLIF	PSCR.CDLIF	CCR.DLIEN	INPRH.PINP

Figure 21-8 shows the two transmit events and interrupts.

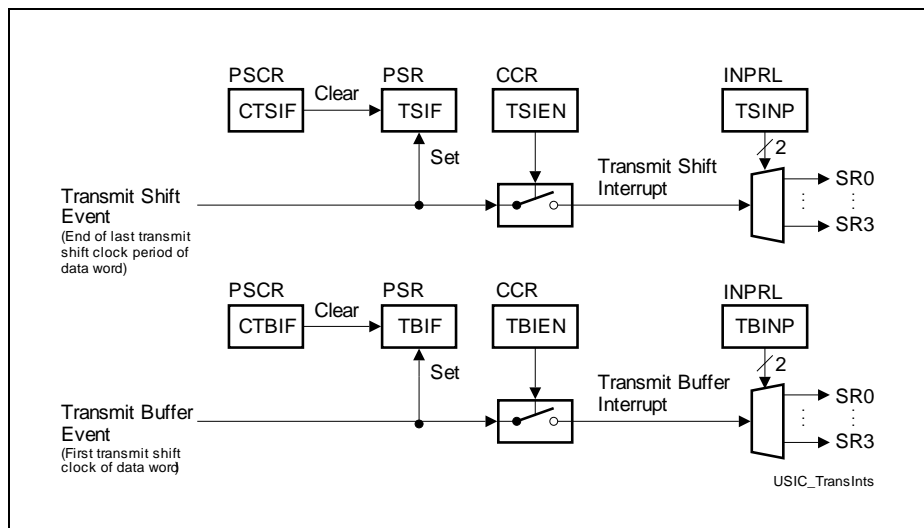


Figure 21-8 Transmit Events and Interrupts

21.2.2.5 Protocol-specific Events and Interrupts

These events are related to protocol-specific actions that are described in the corresponding protocol chapters. The related indication flags are located in register PSR. All events can be individually enabled for the generation of the common protocol interrupt.

- Protocol-specific events in ASC mode:
Synchronization break, data collision on the transmit line, receiver noise, format error in stop bits, receiver frame finished, transmitter frame finished
- Protocol-specific events in SSC mode:
MSLS event (start-end of frame in master mode), DX2T event (start/end of frame in slave mode), both based on slave select signals
- Protocol-specific events in IIC mode:
Wrong transmit code (error in frame sequence), start condition received, repeated start condition received, stop condition received, non-acknowledge received, arbitration lost, slave read request, other general errors
- Protocol-specific events in IIS mode:
DX2T event (change on WA line), WA falling edge or rising edge detected, WA generation finished

Table 21-6 Protocol-specific Events and Interrupt Handling

Event	Indication Flag	Indication cleared by	Interrupt enabled by	SRx Output selected by
Protocol-specific events in ASC mode	PSR.ST[8:2]	PSCR.CST[8:2]	PCRL.CTR[7:3]	INPRH.PINP
Protocol-specific events in SSC mode	PSR.ST[3:2]	PSCR.CST[3:2]	PCRL.CTR[15:14]	INPRH.PINP
Protocol-specific events in IIC mode	PSR.ST[8:1]	PSCR.CST[8:1]	PCRH.CTR[24:18]	INPRH.PINP
Protocol-specific events in IIS mode	PSR.ST[6:3]	PSCR.CST[6:3]	PCRL.CTR[6:4], PCRL.CTR[15]	INPRH.PINP

21.2.3 Channel Control and Configuration Registers

21.2.3.1 Channel Control Register

The channel control register contains the enable/disable bits for interrupt generation on channel events, the control of the parity generation and the protocol selection of a USIC channel.

CCR

Channel Control Register

(10_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AI EN	RI EN	TBI EN	TSI EN	DLI EN	RSI EN	PM		0			MODE				
rw	rw	rw	rw	rw	rw	rw		r			rw				

Field	Bits	Type	Description
MODE	[3:0]	rw	Operating Mode This bit field selects the protocol for this USIC channel. Selecting a protocol that is not available (see register CCFG) or a reserved combination disables the USIC channel. When switching between two protocols, the USIC channel has to be disabled before selecting a new protocol. In this case, registers PCRH, PCRL, and PSR have to be cleared or updated by software. 0 _H The USIC channel is disabled. All protocol-related state machines are set to an idle state. 1 _H The SSC (SPI) protocol is selected. 2 _H The ASC (SCI, UART) protocol is selected. 3 _H The IIS protocol is selected. 4 _H The IIC protocol is selected. Other bit combinations are reserved.

Universal Serial Interface Channel

Field	Bits	Type	Description
PM	[9:8]	rw	Parity Mode This bit field defines the parity generation of the sampled input values. 00 _B The parity generation is disabled. 01 _B Reserved 10 _B Even parity is selected (parity bit = 1 on odd number of 1s in data, parity bit = 0 on even number of 1s in data). 11 _B Odd parity is selected (parity bit = 0 on odd number of 1s in data, parity bit = 1 on even number of 1s in data).
RSIEN	10	rw	Receiver Start Interrupt Enable This bit enables the interrupt generation in case of a receiver start event. 0 _B The receiver start interrupt is disabled. 1 _B The receiver start interrupt is enabled. In case of a receiver start event, the service request output SRx indicated by INPRL.TBINP is activated.
DLIEN	11	rw	Data Lost Interrupt Enable This bit enables the interrupt generation in case of a data lost event (data received in RBUFx while RDVx = 1). 0 _B The data lost interrupt is disabled. 1 _B The data lost interrupt is enabled. In case of a data lost event, the service request output SRx indicated by INPRH.PINP is activated.
TSIEN	12	rw	Transmit Shift Interrupt Enable This bit enables the interrupt generation in case of a transmit shift event. 0 _B The transmit shift interrupt is disabled. 1 _B The transmit shift interrupt is enabled. In case of a transmit shift interrupt event, the service request output SRx indicated by INPRL.TSINP is activated.

Field	Bits	Type	Description
TBIEN	13	rw	Transmit Buffer Interrupt Enable This bit enables the interrupt generation in case of a transmit buffer event. 0 _B The transmit buffer interrupt is disabled. 1 _B The transmit buffer interrupt is enabled. In case of a transmit buffer event, the service request output SRx indicated by INPRL.TBINP is activated.
RIEN	14	rw	Receive Interrupt Enable This bit enables the interrupt generation in case of a receive event. 0 _B The receive interrupt is disabled. 1 _B The receive interrupt is enabled. In case of a receive event, the service request output SRx indicated by INPRL.RINP is activated.
AIEN	15	rw	Alternative Receive Interrupt Enable This bit enables the interrupt generation in case of a alternative receive event. 0 _B The alternative receive interrupt is disabled. 1 _B The alternative receive interrupt is enabled. In case of an alternative receive event, the service request output SRx indicated by INPRL.AINP is activated.
0	[7:4]	r	Reserved Read as 0; should be written with 0.

21.2.3.2 Channel Configuration Register

The channel configuration register contains indicates the functionality that is available in the USIC channel.

CCFG

Channel Configuration Register

(18_H)

Reset Value: 00CF_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			0					TB	RB		0	IIS	IIC	ASC	SSC
			r					r	r		r	r	r	r	r

Field	Bits	Type	Description
SSC	0	r	SSC Protocol Available This bit indicates if the SSC protocol is available. 0 _B The SSC protocol is not available. 1 _B The SSC protocol is available.
ASC	1	r	ASC Protocol Available This bit indicates if the ASC protocol is available. 0 _B The ASC protocol is not available. 1 _B The ASC protocol is available.
IIC	2	r	IIC Protocol Available This bit indicates if the IIC functionality is available. 0 _B The IIC protocol is not available. 1 _B The IIC protocol is available.
IIS	3	r	IIS Protocol Available This bit indicates if the IIS protocol is available. 0 _B The IIS protocol is not available. 1 _B The IIS protocol is available.
RB	6	r	Receive FIFO Buffer Available This bit indicates if an additional receive FIFO buffer is available. 0 _B A receive FIFO buffer is not available. 1 _B A receive FIFO buffer is available.
TB	7	r	Transmit FIFO Buffer Available This bit indicates if an additional transmit FIFO buffer is available. 0 _B A transmit FIFO buffer is not available. 1 _B A transmit FIFO buffer is available.

Field	Bits	Type	Description
0	[5:4], [15:8]	r	Reserved Read as 0; should be written with 0.

21.2.3.3 Kernel State Configuration Register

The kernel state configuration register KSCFG allows the selection of the desired kernel modes for the different device operating modes.

KSCFG

Kernel State Configuration Register (0C_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BP COM	0	COMCFG	BP SUM	0	SUMCFG	BP NOM	0	NOMCFG	0	0	BP MOD EN	MOD EN			
w	r	rw	w	r	rw	w	r	rw	r	r	w	rw			

Field	Bits	Type	Description
MODEN	0	rw	Module Enable This bit enables the module kernel clock and the module functionality. 0 _B The module is switched off immediately (without respecting a stop condition). It does not react on mode control actions and the module clock is switched off. The module does not react on read accesses and ignores write accesses (except to KSCFG). 1 _B The module is switched on and can operate. After writing 1 to MODEN, it is recommended to read register KSCFG to avoid pipeline effects in the control block before accessing other USIC registers.
BPMODEN	1	w	Bit Protection for MODEN This bit enables the write access to the bit MODEN. It always reads 0. 0 _B MODEN is not changed. 1 _B MODEN is updated with the written value.

Field	Bits	Type	Description
NOMCFG	[5:4]	rw	Normal Operation Mode Configuration This bit field defines the kernel mode applied in normal operation mode. 00 _B Run mode 0 is selected. 01 _B Run mode 1 is selected. 10 _B Stop mode 0 is selected. 11 _B Stop mode 1 is selected.
BPNOM	7	w	Bit Protection for NOMCFG This bit enables the write access to the bit field NOMCFG. It always reads 0. 0 _B NOMCFG is not changed. 1 _B NOMCFG is updated with the written value.
SUMCFG	[9:8]	rw	Suspend Mode Configuration This bit field defines the kernel mode applied in suspend mode. Coding like NOMCFG.
BPSUM	11	w	Bit Protection for SUMCFG This bit enables the write access to the bit field SUMCFG. It always reads 0. 0 _B SUMCFG is not changed. 1 _B SUMCFG is updated with the written value.
COMCFG	[13:12]	rw	Clock Off Mode Configuration This bit field defines the kernel mode applied in clock-off mode. Coding like NOMCFG.
BPCOM	15	w	Bit Protection for COMCFG This bit enables the write access to the bit field COMCFG. It always reads 0. 0 _B COMCFG is not changed. 1 _B COMCFG is updated with the written value.
0	[3:2], 6, 10, 14	r	Reserved Read as 0; should be written with 0. Bit 2 can read as 1 after BootROM exit (but can be ignored).

21.2.3.4 Interrupt Node Pointer Registers

The interrupt node pointer registers define the service request output SRx that is activated if the corresponding event occurs and interrupt generation is enabled.

INPRL

Interrupt Node Pointer Register L (14_H) **Reset Value: 0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	AINP	0	RINP	0	TBINP	0	TSINP								
r	rw	r	rw	r	rw	r	rw	r	rw	r	rw	r	rw	r	rw

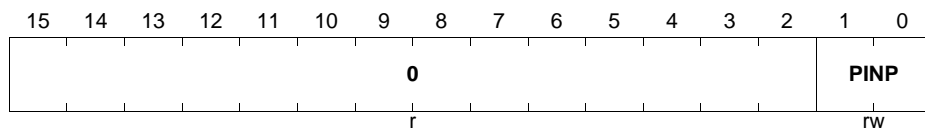
Field	Bits	Type	Description
TSINP	[1:0]	rw	Transmit Shift Interrupt Node Pointer This bit field defines which service request output SRx becomes activated in case of a transmit shift interrupt. 00 _B Output SR0 becomes activated. 01 _B Output SR1 becomes activated. 10 _B Output SR2 becomes activated. 11 _B Output SR3 becomes activated.
TBINP	[5:4]	rw	Transmit Buffer Interrupt Node Pointer This bit field defines which service request output SRx will be activated in case of a transmit buffer interrupt or a receive start interrupt. Coding like TSINP.
RINP	[9:8]	rw	Receive Interrupt Node Pointer This bit field defines which service request output SRx will be activated in case of a receive interrupt. Coding like TSINP.
AINP	[13:12]	rw	Alternative Receive Interrupt Node Pointer This bit field defines which service request output SRx will be activated in case of a alternative receive interrupt. Coding like TSINP.
0	[3:2], [7:6], [11:10], [15:14]	r	Reserved Read as 0; should be written with 0.

INPRH

Interrupt Node Pointer Register H

(16_H)

Reset Value: 0000_H



Field	Bits	Type	Description
PINP	[1:0]	rw	Protocol Interrupt Node Pointer This bit field defines which service request output SRx becomes activated in case of a protocol interrupt. 00 _B Output SR0 becomes activated. 01 _B Output SR1 becomes activated. 10 _B Output SR2 becomes activated. 11 _B Output SR3 becomes activated.
0	[15:2]	r	Reserved Read as 0; should be written with 0.

21.2.4 Protocol Related Registers

21.2.4.1 Protocol Control Registers

The bits in the protocol control registers define protocol-specific functions. They have to be configured by software before enabling a new protocol. Only the bits used for the selected protocol are taken into account, whereas the other bit positions always read as 0. The protocol-specific meaning is described in the related protocol section.

PCRL

Protocol Control Register L

(40_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTR 15	CTR 14	CTR 13	CTR 12	CTR 11	CTR 10	CTR 9	CTR 8	CTR 7	CTR 6	CTR 5	CTR 4	CTR 3	CTR 2	CTR 1	CTR 0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
CTR _x (x = 0-15)	x	rw	Protocol Control Bit x This bit is a protocol control bit.

PCRH

Protocol Control Register H

(42_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTR 31	CTR 30	CTR 29	CTR 28	CTR 27	CTR 26	CTR 25	CTR 24	CTR 23	CTR 22	CTR 21	CTR 20	CTR 19	CTR 18	CTR 17	CTR 16
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
CTR _x (x = 16-30)	x - 16	rwh	Protocol Control Bit x This bit is a protocol control bit that can be overwritten by protocol-specific information.
CTR31	15	rwh	Protocol Control Bit 31 In the various protocols, this bit controls the start and the stop of the MCLK signal. 0 _B Signal MCLK is not generated (MCLK = 0). 1 _B Signal MCLK generation is enabled.

21.2.4.2 Protocol Status Register

The flags in the protocol status register can be cleared by writing a 1 to the corresponding bit position in register PSCR. Writing a 1 to a bit position in PSR sets the corresponding flag, but doesn't lead to further actions (no interrupt generation). Writing a 0 has no effect. These flags should be cleared by software before enabling a new protocol. The protocol-specific meaning is described in the related protocol section.

PSR

Protocol Status Register

(44_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AIF	RIF	TBIF	TSIF	DLIF	RSIF	ST9	ST8	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
STx (x = 0-9)	x	rwh	Protocol Status Flag x See protocol specific description.
RSIF	10	rwh	Receiver Start Indication Flag 0 _B A receiver start event has not occurred. 1 _B A receiver start event has occurred.
DLIF	11	rwh	Data Lost Indication Flag 0 _B A data lost event has not occurred. 1 _B A data lost event has occurred.
TSIF	12	rwh	Transmit Shift Indication Flag 0 _B A transmit shift event has not occurred. 1 _B A transmit shift event has occurred.
TBIF	13	rwh	Transmit Buffer Indication Flag 0 _B A transmit buffer event has not occurred. 1 _B A transmit buffer event has occurred.
RIF	14	rwh	Receive Indication Flag 0 _B A receive event has not occurred. 1 _B A receive event has occurred.
AIF	15	rwh	Alternative Receive Indication Flag 0 _B An alternative receive event has not occurred. 1 _B An alternative receive event has occurred.

21.2.4.3 Protocol Status Clear Register

Read accesses to this register always deliver 0 at all bit positions.

PSCR

Protocol Status Clear Register

(48_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
AIF	RIF	TBIF	TSIF	DLIF	RSIF	ST9	ST8	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0
W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Field	Bits	Type	Description
CSTx (x = 0-9)	x	w	Clear Status Flag x in PSR 0 _B No action 1 _B Flag PSR.STx is cleared.
CRSIF	10	w	Clear Receiver Start Indication Flag 0 _B No action 1 _B Flag PSR.RSIF is cleared.
CDLIF	11	w	Clear Data Lost Indication Flag 0 _B No action 1 _B Flag PSR.DLIF is cleared.
CTSIF	12	w	Clear Transmit Shift Indication Flag 0 _B No action 1 _B Flag PSR.TSIF is cleared.
CTBIF	13	w	Clear Transmit Buffer Indication Flag 0 _B No action 1 _B Flag PSR.TBIF is cleared.
CRIF	14	w	Clear Receive Indication Flag 0 _B No action 1 _B Flag PSR.RIF is cleared.
CAIF	15	w	Clear Alternative Receive Indication Flag 0 _B No action 1 _B Flag PSR.AIF is cleared.

21.2.5 Operating the Input Stages

All three input stages offer the same feature set. They are used for all protocols, because the signal conditioning can be adapted in a very flexible way and the digital filters can be switched on and off separately.

21.2.5.1 General Input Structure

All input stages are built in a similar way as shown in **Figure 21-10**. All enable/disable functions and selections are controlled independently for each input stage by bits in the registers DX0CR, DX1CR, and DX2CR.

The desired input signal can be selected among the input lines DXnA to DXnG and a permanent 1-level by programming bit field DSEL. Please refer to the implementation chapter for the device-specific input signal assignment. Bit DPOL allows a polarity inversion of the selected input signal to adapt the input signal polarity to the internal polarity of the data shift unit and the protocol state machine. For some protocols, the input signals can be directly forwarded to the data shift unit for the data transfers (DSEN = 0, INSW = 1) without any further signal conditioning. In this case, the data path does not contain any delay due to synchronization or filtering.

In the case of noise on the input signals, there is the possibility to synchronize the input signal (signal DXnS is synchronized to f_{SYS}) and additionally to enable a digital noise filter in the signal path. The synchronized input signal (and optionally filtered if DFEN = 1) is taken into account by DSEN = 1. Please note that the synchronization leads to a delay in the signal path of 2-3 times the period of f_{SYS} .

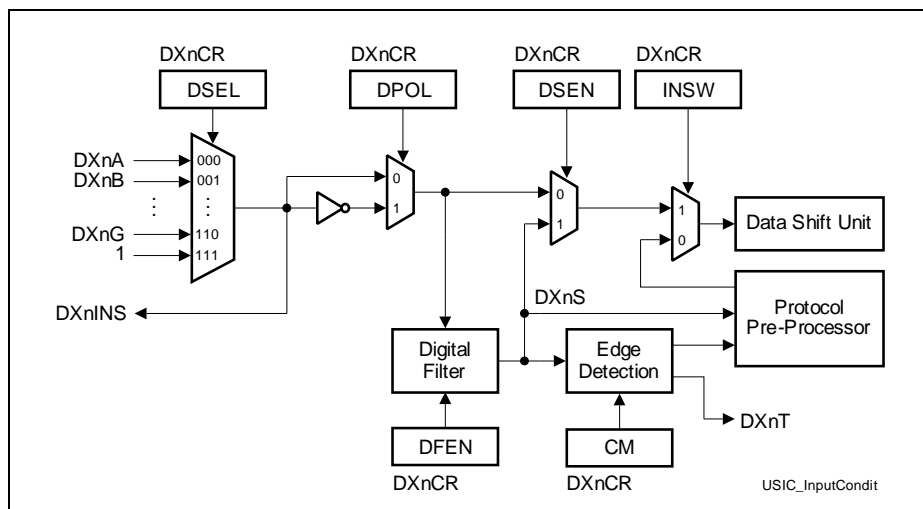


Figure 21-10 Input Conditioning

If the input signals are handled by a protocol pre-processor, the data shift unit is directly connected to the protocol pre-processor by $INSW = 0$. The protocol pre-processor is connected to the synchronized input signal $DXnS$ and, depending on the selected protocol, also evaluates the edges.

21.2.5.2 Digital Filter

The digital filter can be enabled to reduce noise on the input signals. Before being filtered, the input signal becomes synchronized to f_{SYS} . If the filter is disabled, signal $DXnS$ corresponds to the synchronized input signal. If the filter is enabled, pulses shorter than one filter sampling period are suppressed in signal $DXnS$. After an edge of the synchronized input signal, signal $DXnS$ changes to the new value if two consecutive samples of the new value have been detected.

In order to adapt the filter sampling period to different applications, it can be programmed. The first possibility is the system frequency f_{SYS} . Longer pulses can be suppressed if the fractional divider output frequency f_{FD} is selected. This frequency is programmable in a wide range and can also be used to determine the baud rate of the data transfers.

In addition to the synchronization delay of 2-3 periods of f_{SYS} , an enabled filter adds a delay of up to two filter sampling periods between the selected input and signal $DXnS$.

21.2.5.3 Edge Detection

The synchronized (and optionally filtered) signal $DXnS$ can be used as input to the data shift unit and is also an input to the selected protocol pre-processor. If the protocol pre-processor does not use the $DXnS$ signal for protocol-specific handling, $DXnS$ can be used for other tasks, e.g. to control data transmissions in master mode (a data word can be tagged valid for transmission, see chapter about data buffering).

A programmable edge detection indicates that the desired event has occurred by activating the trigger signal $DXnT$ (introducing a delay of one period of f_{SYS} before a reaction to this event can take place).

21.2.5.4 Selected Input Monitoring

The selected input signal of each input stage has been made available with the signals $DX0INS$, $DX1INS$, and $DX2INS$. These signals can be used in the system to trigger other actions, e.g. to generate interrupts.

21.2.5.5 Loop Back Mode

The USIC transmitter output signals can be connected to the corresponding receiver inputs of the same communication channel in loop back mode. Therefore, the input "G" of the input stages that are needed for the selected protocol have to be selected. In this

case, drivers for ASC, SSC, and IIS can be evaluated on-chip without the connections to port pins. Data transferred by the transmitter can be received by the receiver as if it would have been sent by another communication partner.

21.2.6 Input Stage Register

21.2.6.1 Input Control Registers

The input control registers contain the bits to define the characteristics of the input stages (input stage DX0 is controlled by register DX0CR, etc.).

DX0CR

Input Control Register 0 (20_H) **Reset Value: 0000_H**

DX1CR

Input Control Register 1 (24_H) **Reset Value: 0000_H**

DX2CR

Input Control Register 2 (28_H) **Reset Value: 0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DXS	0			CM		SF SEL	D POL	0	DS EN	DF EN	IN SW	0	DSEL		
rh	r			rw		rw	rw	r	rw	rw	rw	r	rw		

Field	Bits	Type	Description
DSEL	[2:0]	rw	Data Selection for Input Signal This bit field defines the input data signal for the corresponding input line for protocol pre-processor. The selection can be made from the input vector DXn[G:A]. 000 _B The data input DXnA is selected. 001 _B The data input DXnB is selected. 010 _B The data input DXnC is selected. 011 _B The data input DXnD is selected. 100 _B The data input DXnE is selected. 101 _B The data input DXnF is selected. 110 _B The data input DXnG is selected. 111 _B The data input is always 1.

Universal Serial Interface Channel

Field	Bits	Type	Description
INSW	4	rw	Input Switch This bit defines if the data shift unit input is derived from the input data path DXn or from the selected protocol pre-processors. 0_B The input of the data shift unit is controlled by the protocol pre-processor. 1_B The input of the data shift unit is connected to the selected data input line. This setting is used if the signals are directly derived from an input pin without treatment by the protocol pre-processor.
DFEN	5	rw	Digital Filter Enable This bit enables/disables the digital filter for signal DXnS. 0_B The input signal is not digitally filtered. 1_B The input signal is digitally filtered.
DSEN	6	rw	Data Synchronization Enable This bit selects if the asynchronous input signal or the synchronized (and optionally filtered) signal DXnS can be used as input for the data shift unit. 0_B The un-synchronized signal can be taken as input for the data shift unit. 1_B The synchronized signal can be taken as input for the data shift unit.
DPOL	8	rw	Data Polarity for DXn This bit defines the signal polarity of the input signal. 0_B The input signal is not inverted. 1_B The input signal is inverted.
SFSEL	9	rw	Sampling Frequency Selection This bit defines the sampling frequency of the digital filter for the synchronized signal DXnS. 0_B The sampling frequency is f_{SYS} . 1_B The sampling frequency is f_{FD} .

Field	Bits	Type	Description
CM	[11:10]	rw	Combination Mode This bit field selects which edge of the synchronized (and optionally filtered) signal DXnS activates the trigger output DXnT of the input stage. 00 _B The trigger activation is disabled. 01 _B A rising edge activates DXnT. 10 _B A falling edge activates DXnT. 11 _B Both edges activate DXnT.
DXS	15	rh	Synchronized Data Value This bit indicates the value of the synchronized (and optionally filtered) input signal. 0 _B The current value of DXnS is 0. 1 _B The current value of DXnS is 1.
0	3, 7, [14:12]	r	Reserved Read as 0; should be written with 0.

21.2.7 Operating the Baud Rate Generator

The following blocks can be configured to operate the baud rate generator, see also [Figure 21-2](#) on [Page 21-8](#).

21.2.7.1 Fractional Divider

The fractional divider generates its output frequency f_{FD} by dividing the input frequency f_{SYS} either by an integer factor n or by multiplication by $n/1024$. It has two operating modes:

- Normal divider mode (FDRL.DM = 01_B):
In this mode, the output frequency f_{FD} is derived from the input clock f_{SYS} by an integer division by a value between 1 and 1024. The division is based on a counter FDRH.RESULT that is incremented by 1 with f_{SYS} . After reaching the value 3FF_H, the counter is loaded with FDRL.STEP and then continues counting. In order to achieve $f_{FD} = f_{SYS}$, the value of STEP has to be programmed with 3FF_H.
The output frequency in normal divider mode is defined by the equation:

$$f_{FD} = f_{SYS} \times \frac{1}{n} \quad \text{with } n = 1024 - \text{STEP} \quad (21.1)$$

- Fractional divider mode (FDRL.DM = 10_B):
In this mode, the output frequency f_{FD} is derived from the input clock f_{SYS} by a fractional multiplication by $n/1024$ for a value of n between 0 and 1023. In general, the fractional divider mode allows to program the average output clock frequency with a finer granularity than in normal divider mode. Please note that in fractional divider mode f_{FD} can have a maximum period jitter of one f_{SYS} period. This jitter is not accumulated over several cycles.
The frequency f_{FD} is generated by an addition of FDRL.STEP to FDRH.RESULT with f_{SYS} . The frequency f_{FD} is based on the overflow of the addition result over 3FF_H.
The output frequency in fractional divider mode is defined by the equation:

$$f_{FD} = f_{SYS} \times \frac{n}{1024} \quad \text{with } n = \text{STEP} \quad (21.2)$$

The output frequency f_{FD} of the fractional divider is selected for baud rate generation by BRGL.CLKSEL = 00_B.

21.2.7.2 External Frequency Input

The baud rate can be generated referring to an external frequency input (instead of to f_{SYS}) if in the selected protocol the input stage DX1 is not needed (DX1CTR.INSW = 0). In this case, an external frequency input signal at the DX1 input stage can be synchronized and sampled with the system frequency f_{SYS} . It can be optionally filtered

by the digital filter in the input stage. This feature allows data transfers with frequencies that can not be generated by the device itself, e.g. for specific audio frequencies.

If $BRGL.CLKSEL = 10_B$, the trigger signal $DX1T$ determines f_{DX1} . In this mode, either the rising edge, the falling edge, or both edges of the input signal can be used for baud rate generation, depending on the configuration of the $DX1T$ trigger event by bit field $DX1CTR.CM$. The signal $MCLK$ toggles with each trigger event of $DX1T$.

If $BRGL.CLKSEL = 11_B$, the rising edges of the input signal can be used for baud rate generation. The signal $MCLK$ represents the synchronized input signal $DX1S$.

Both, the high time and the low time of external input signal must each have a length of minimum 2 periods of f_{SYS} to be used for baud rate generation.

21.2.7.3 Protocol-Related Counter in Divider Mode

In divider mode, the protocol-related counter is used for an integer division delivering the output frequency f_{PDIV} . Additionally, two divider stages with a fixed division by 2 provide the output signals $MCLK$ and $SCLK$ with 50% duty cycle. If the fractional divider mode is used, the maximum fractional jitter of 1 period of f_{SYS} can also appear in these signals. The outputs frequencies of this divider is controlled by registers $BRGL$ and $BRGH$.

In order to define a frequency ratio between the master clock $MCLK$ and the shift clock $SCLK$, the divider stage for $MCLK$ is located in front of the divider by $PDIV+1$, whereas the divider stage for $SCLK$ is located at the output of this divider.

$$f_{MCLK} = \frac{f_{PIN}}{2} \quad (21.3)$$

$$f_{SCLK} = \frac{f_{PDIV}}{2} \quad (21.4)$$

In the case that the master clock is used as reference for external devices (e.g. for IIS components) and a fixed phase relation to $SCLK$ and other timing signals is required, it is recommended to use the $MCLK$ signal as input for the $PDIV$ divider. If the $MCLK$ signal is not used or a fixed phase relation is not necessary, the faster frequency f_{PIN} can be selected as input frequency.

$$\begin{aligned} f_{PDIV} &= f_{PIN} \times \frac{1}{PDIV + 1} & \text{if } PPPEN = 0 \\ f_{PDIV} &= f_{MCLK} \times \frac{1}{PDIV + 1} & \text{if } PPPEN = 1 \end{aligned} \quad (21.5)$$

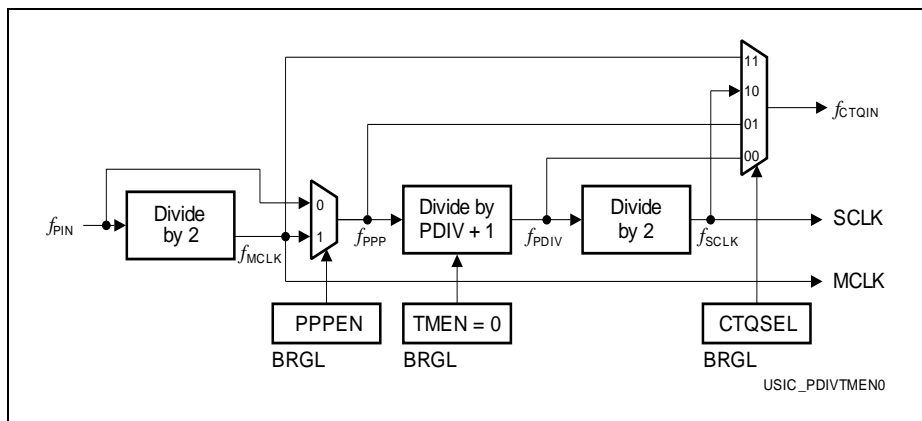


Figure 21-11 Protocol-Related Counter (Divider Mode)

21.2.7.4 Protocol-Related Counter in Capture Mode

In capture mode, the protocol-related counter stage can be used for time interval measurement (BRGL.TMEN = 1). In this case, the frequency division is disabled (reception and transmission are not possible) and the counter is working as capture timer by counting f_{PPP} periods. When reaching its maximum value, the counter stops counting. If an event is indicated by DX0T or DX1T, the actual counter value is captured into bit field BRGH.PDIV and the counter restarts from 0. Additionally, a transmit shift interrupt event is generated (bit PSRL.TSIF becomes set).

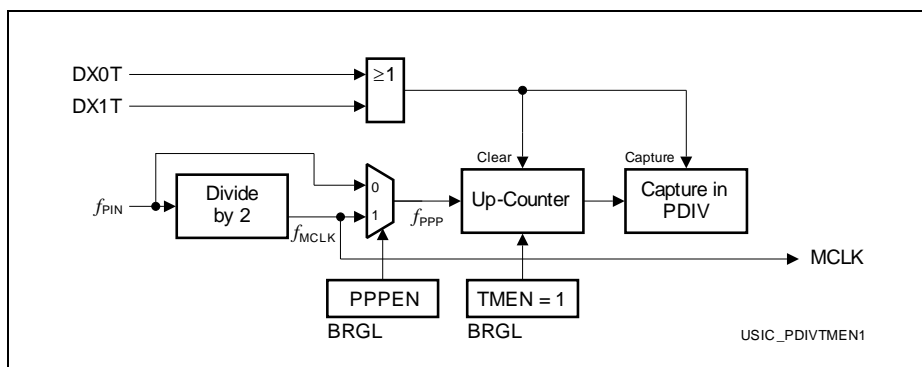


Figure 21-12 Protocol-Related Counter (Capture Mode)

The capture mode can be used to measure the baud rate in slave mode before starting data transfers, e.g. to measure the time between two edges of a data signal (by DX0T)

or of a shift clock signal (by DX1T). The conditions to activate the DXnT trigger signals can be configured in each input stage.

21.2.7.5 Time Quanta Counter

The time quanta counter CTQ associated to the protocol pre-processor allows to generate time intervals for protocol-specific purposes. The length of a time quantum t_q is given by the selected input frequency f_{CTQIN} and the programmed pre-divider value. The meaning of the time quanta depend on the selected protocol, please refer to the corresponding chapters for more protocol-specific information.

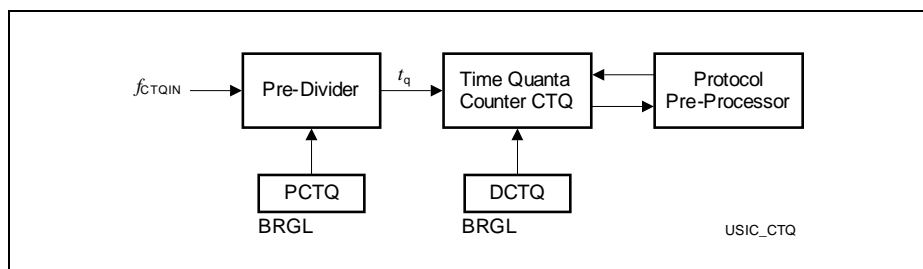


Figure 21-13 Time Quanta Counter

21.2.7.6 Shift Clock Output Configuration

The master clock output signal MCLKOUT available at the corresponding output pin can be configured in polarity. The MCLK signal can be generated for each protocol in order to provide a kind of higher frequency time base compared to the shift clock.

The configuration mechanism of the master clock output signal MCLKOUT ensures that no shortened pulses can occur. Each MCLK period consists of two phases, an active phase, followed by a passive phase. The polarity of the MCLKOUT signal during the active phase is defined by the inverted level of bit BRGH.MCLKCFG, evaluated at the start of the active phase. The polarity of the MCLKOUT signal during the passive phase is defined by bit BRGH.MCLKCFG, evaluated at the start of the passive phase. If bit BRGH.MCLKOUT is programmed with another value, the change is taken into account with the next change between the phases. This mechanism ensures that no shorter pulses than the length of a phase occur at the MCLKOUT output. In the example shown in [Figure 21-14](#), the value of BRGH.MCLKCFG is changed from 0 to 1 during the passive phase of MCLK period 2.

The generation of the MCLKOUT signal is enabled/disabled by the protocol pre-processor, based on bit PCRH.MCLK. After this bit has become set, signal MCLKOUT is generated with the next active phase of the MCLK period. If PCRH.MCLK = 0 (MCLKOUT generation disabled), the level for the passive phase is also applied for active phase.

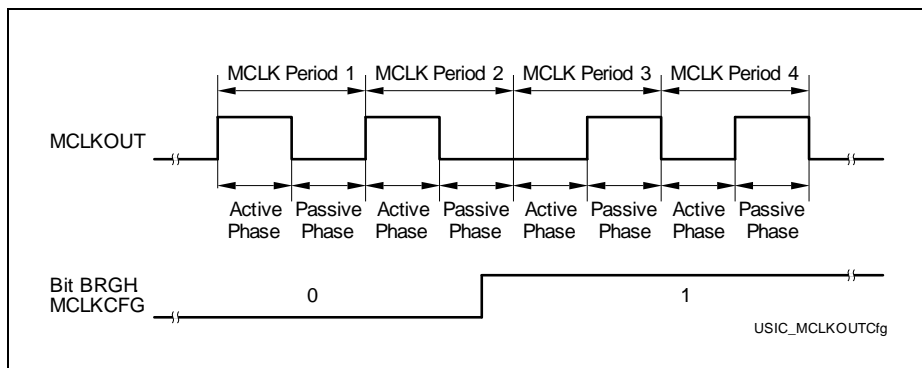


Figure 21-14 Master Clock Output Configuration

The shift clock output signal SCLKOUT available at the corresponding output pin can be configured in polarity and additionally, a delay of one period of f_{PDIV} (= half SCLK period) can be introduced. The delay allows to adapt the order of the shift clock edges to the application requirements. If the delay is used, it has to be taken into account for the calculation of the signal propagation times and loop delays.

The mechanism for the polarity control of the SCLKOUT signal is similar to the one for MCLKOUT, but based on bit field BRGH.SCLKCFG. The generation of the SCLKOUT signal is enabled/disabled by the protocol pre-processor. Depending on the selected protocol, the protocol pre-processor can control the generation of the SCLKOUT signal independently of the divider chain, e.g. for protocols without the need of a shift clock available at a pin, the SCLKOUT generation is disabled.

21.2.8 Baud Rate Generator Registers

21.2.8.1 Fractional Divider Registers

The fractional divider registers FDRL and FDRH allow the generation of the internal frequency f_{FD} , that is derived from the system clock f_{SYS} .

FDRL

Fractional Divider Register L

(04_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DM		0				STEP									
rw		r				rw									

Field	Bits	Type	Description
STEP	[9:0]	rw	Step Value In normal divider mode STEP contains the reload value for RESULT after RESULT has reached 3FF _H . In fractional divider mode STEP defines the value added to RESULT with each input clock cycle.
DM	[15:14]	rw	Divider Mode This bit fields defines the functionality of the fractional divider block. 00 _B The divider is switched off, $f_{FD} = 0$. 01 _B Normal divider mode selected. 10 _B Fractional divider mode selected. 11 _B The divider is switched off, $f_{FD} = 0$.
0	[13:10]	r	Reserved Read as 0; should be written with 0.

FDRH

Fractional Divider Register H

(06_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		0				RESULT									
rw		r				rh									

Field	Bits	Type	Description
RESULT	[9:0]	rh	Result Value In normal divider mode this bit field is updated with f_{SYS} according to: $RESULT = RESULT + 1$ In fractional divider mode this bit field is updated with f_{SYS} according to: $RESULT = RESULT + STEP$ If bit field DM is written with 01 _B or 10 _B , RESULT is loaded with a start value of 3FF _H .
0	[15:14]	rw	Reserved for Future Use Must be written with 0 to allow correct fractional divider operation.
0	[13:10]	r	Reserved Read as 0; should be written with 0.

21.2.8.2 Baud Rate Generator Registers

The protocol-related divider for baud rate generation is controlled by the registers BRGL and BRGH.

BRGL

Baud Rate Generator Register L

(1C_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	DCTQ					PCTQ	CTQSEL	0	PPP EN	TM EN	0	CLKSEL			
r	rw					rw	rw	r	rw	rw	r	rw	rw		

Field	Bits	Type	Description
CLKSEL	[1:0]	rw	Clock Selection This bit field defines the input frequency f_{PIN} 00 _B The fractional divider frequency f_{FD} is selected. 01 _B Reserved, no action 10 _B The trigger signal DX1T defines f_{PIN} . Signal MCLK toggles with f_{PIN} . 11 _B Signal MCLK corresponds to the DX1S signal and the frequency f_{PIN} is derived from the rising edges of DX1S.
TMEN	3	rw	Timing Measurement Enable This bit defines the functionality of the protocol-related divider. 0 _B Divider mode: $f_{PDIV} = f_{PPP} / (PDIV + 1)$ Data transfers are possible and the trigger signals DX0T and DX1T are ignored. 1 _B Capture mode: The 10-bit counter is incremented by 1 with f_{PPP} and stops counting when reaching its maximum value. If one of the trigger signals DX0T or DX1T become active, the counter value is captured into bit field PDIV, the counter is cleared and a transmit shift event is generated. Data transfers are not possible.

Field	Bits	Type	Description
PPPEN	4	rw	Enable 2:1 Divider for f_{PPP} This bit defines the input frequency f_{PPP} . 0_B The 2:1 divider for f_{PPP} is disabled. $f_{PPP} = f_{PIN}$ 1_B The 2:1 divider for f_{PPP} is enabled. $f_{PPP} = f_{MCLK} = f_{PIN} / 2$.
CTQSEL	[7:6]	rw	Input Selection for CTQ This bit defines the length of a time quantum for the protocol pre-processor. 00_B $f_{CTQIN} = f_{PDIV}$ 01_B $f_{CTQIN} = f_{PPP}$ 10_B $f_{CTQIN} = f_{SCLK}$ 11_B $f_{CTQIN} = f_{MCLK}$
PCTQ	[9:8]	rw	Pre-Divider for Time Quanta Counter This bit field defines length of a time quantum t_q for the time quanta counter in the protocol pre-processor. $t_Q = (PCTQ + 1) / f_{CTQIN}$
DCTQ	[14:10]	rw	Denominator for Time Quanta Counter This bit field defines the number of time quanta t_q taken into account by the time quanta counter in the protocol pre-processor.
0	2, 5, 15	r	Reserved Read as 0; should be written with 0.

BRGH

Baud Rate Generator Register H

(1E_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCLKCFG		M CLK CFG	0			PDIV									
rw		rw	r			rwh									

Field	Bits	Type	Description
PDIV	[9:0]	rwh	Divider Mode: Divider Factor to Generate f_{PDIV} This bit field defines the ratio between the input frequency f_{PP} and the divider frequency f_{PDIV} . Capture Mode: Captured Time Interval The value of the counter is captured into this bit field if one of the trigger signals DX0T or DX1T are activated by the corresponding input stage.
MCLKCFG	13	rw	Master Clock Configuration This bit field defines the level of the passive phase of the MCLKOUT signal. 0 _B The passive level is 0. 1 _B The passive level is 1.
SCLKCFG	[15:14]	rw	Shift Clock Output Configuration This bit field defines the level of the passive phase of the SCLKOUT signal and enables/disables a delay of half of a SCLK period. 00 _B The passive level is 0 and the delay is disabled. 01 _B The passive level is 1 and the delay is disabled. 10 _B The passive level is 0 and the delay is enabled. 11 _B The passive level is 1 and the delay is enabled.
0	[12:10]	r	Reserved Read as 0; should be written with 0.

21.2.9 Operating the Transmit Data Path

The transmit data path is based on a 16-bit wide transmit shift register TSR and a transmit buffer TBUF. The data transfer parameters like data word length, data frame length, or the shift direction are controlled commonly for transmission and reception by the shift control registers. Register TCSRL mainly controls the transmit data handling, whereas register TCSRH monitors the transmit status.

A change of the value of the data shift output signal DOUT only happens at the corresponding edge of the shift clock input signal. The level of the last data bit of a data word/frame is held constant at DOUT until the next data word begins with the next corresponding edge of the shift clock.

21.2.9.1 Transmit Buffering

The transmit shift register TSR can not be directly accessed by software, because it is automatically updated with the value stored in the transmit buffer TBUF if a currently transmitted data word is finished and new data is valid for transmission. Data words can be loaded directly into TBUF by writing to one of the transmit buffer input locations TBUFx (see [Page 21-52](#)) or, optionally, by a FIFO buffer stage (see [Page 21-79](#)).

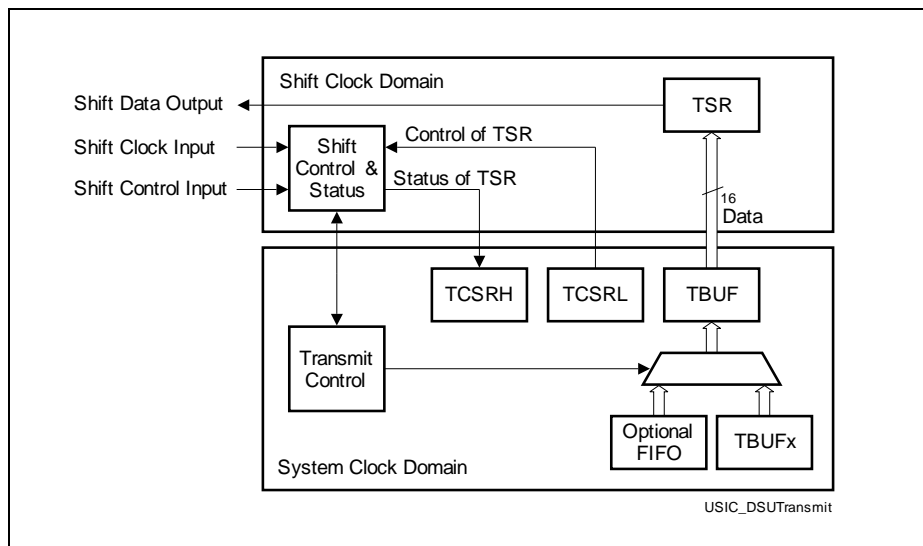


Figure 21-15 Transmit Data Path

21.2.9.2 Transmit Control Information

The transmit control information TCI can be used as additional control parameter for data transfers. The TCI is derived from the address x of the written TBUF x transmit buffer input location.

It can be used to dynamically change the data word length, the data frame length, or other protocol-specific functions (for more details about this topic, please refer to the corresponding protocol chapters). The way how the TCI is used in different applications can be programmed by bits WLEMD, FLEMD, SELMD, and WAMD in register TCSRL. Please note that not all possible settings lead to useful system behavior.

- **Word length control:**
If TCSRL.WLEMD = 1, bit field SCTRH.WLE is updated with TCI[3:0] if a transmit buffer input location TBUF x is written. This function can be used in all protocols to dynamically change the data word length between 1 and 16 data bits per data word. Additionally, bit TCSRL.EOF is updated with TCI[4]. This function can be used in SSC master mode to control the slave select generation to finish data frames. It is recommended to program TCSRL.FLEMD = TCSRL.SELMD = 0.
- **Frame length control:**
If TCSRL.FLEMD = 1, bit field SCTRH.FLE[4:0] is updated with TCI[4:0] and SCTRH.FLE[5] becomes 0 if a transmit buffer input location TBUF x is written. This function can be used in all protocols to dynamically change the data frame length between 1 and 32 data bits per data frame. It is recommended to program TCSRL.SELMD = TCSRL.WLEMD = TCSRL.WAMD = 0.
- **Select output control:**
If TCSRL.SELMD = 1, bit field PCR.CTR[20:16] is updated with TCI[4:0] and PCR.CTR[23:21] becomes 0 if a transmit buffer input location TBUF x is written. This function can be used in SSC master mode to define the targeted slave device(s). It is recommended to program TCSRL.WLEMD = TCSRL.FLEMD = TCSRL.WAMD = 0.
- **Word address control:**
If TCSRL.WAMD = 1, bit TCSRL.WA is updated with TCI[4] if a transmit buffer input location TBUF x is written. This function can be used in IIS mode to define if the data word is transmitted on the right or the left channel. It is recommended to program TCSRL.SELMD = TCSRL.FLEMD = 0.

21.2.9.3 Transmit Data Validation

The data word in the transmit buffer TBUF can be tagged valid or invalid for transmission by bit TCSR.L.TDV (transmit data valid). A combination of data flow related and event related criteria define whether the data word is considered valid for transmission. A data validation logic checks the start conditions for each data word. Depending on the result of the check, the transmit shift register is loaded with different values, according to the following rules:

- If a USIC channel is the communication master (it defines the start of each data word transfer), a data word transfer can only be started with valid data in the transmit buffer TBUF. In this case, the transmit shift register is loaded with the content of TBUF, that is not changed due to this action.
- If a USIC channel is a communication slave (it can not define the start itself, but has to react), a data word transfer requested by the communication master has to be started independently of the status of the data word in TBUF. If a data word transfer is requested and started by the master, the transmit shift register is loaded at the first corresponding shift clock edge either with the data word in TBUF (if it is valid for transmission) or with the level defined by bit SCTRL.PDL (if the content of TBUF has not been valid at the transmission start). In both cases, the content of TBUF is not changed.

The control and status bits for the data validation are located in registers TCSR.L or TCSR.H. The data validation is based on the logic blocks shown in **Figure 21-16**.

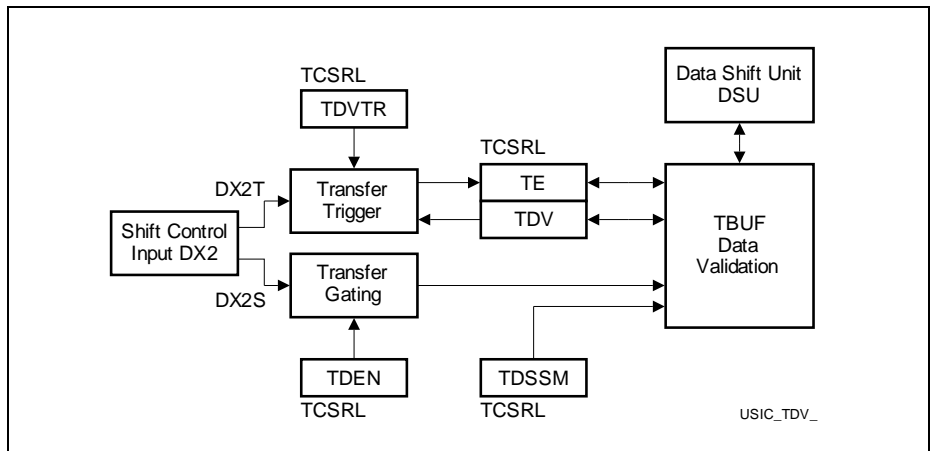


Figure 21-16 Transmit Data Validation

- A transfer gating logic enables or disables the data word transfer from TBUF under software or under hardware control. If the input stage DX2 is not needed for data

shifting, signal DX2S can be used for gating purposes. The transfer gating logic is controlled by bit field TCSRL.TDEN.

- A transfer trigger logic supports data word transfers related to events, e.g. timer based or related to an input pin. If the input stage DX2 is not needed for data shifting, signal DX2T can be used for trigger purposes. The transfer trigger logic is controlled by bit TCSRL.TDVTR and the occurrence of a trigger event is indicated by bit TCSRH.TE.
- A data validation logic combining the inputs from the gating logic, the triggering logic and DSU signals. A transmission of the data word located in TBUF can only be started if the gating enables the start, bit TCSRL.TDV = 1, and bit TCSRH.TE = 1. The content of the transmit buffer TBUF should not be overwritten with new data while it is valid for transmission and a new transmission can start. If the content of TBUF has to be changed, it is recommended to clear bit TCSRL.TDV by writing FMRL.MTDV = 10_B before updating the data. Bit TCSRL.TDV becomes automatically set when TBUF is updated with new data. Another possibility are the interrupts TBI (for ASC and IIC) or RSI (for SSC and IIS) indicating that a transmission has started. While a transmission is in progress, TBUF can be loaded with new data. In this case the user has to take care that an update of the TBUF content takes place before a new transmission starts.

With this structure, the following data transfer functionality can be achieved:

- If bit TCSRL.TDSSM = 0, the content of the transmit buffer TBUF is always considered as valid for transmission. The transfer trigger mechanism can be used to start the transfer of the same data word based on the selected event (e.g. on a timer base or an edge at a pin) to realize a kind of life-sign mechanism. Furthermore, in slave mode, it is ensured that always a correct data word is transmitted instead of the passive data level.
- Bit TCSRL.TDSSM = 1 has to be programmed to allow word-by-word data transmission with a kind of single-shot mechanism. After each transmission start, a new data word has to be loaded into the transmit buffer TBUF, either by software write actions to one of the transmit buffer input locations TBUFx or by an optional data buffer (e.g. FIFO buffer). To avoid that data words are sent out several times or to allow data handling with an additional data buffer (e.g. FIFO), bit TCSRL.TDSSM has to be 1.
- Bit TCSRL.TDV becoming automatically set when a new data word is loaded into the transmit buffer TBUF, a transmission start can be requested by a write action of the data to be transmitted to at least the low byte of one of the transmit buffer input locations TBUFx. The additional information TCI can be used to control the data word length or other parameters independently for each data word by a single write access.
- Bit field FMRL.MTDV allows software driven modification (set or clear) of bit TCSRL.TDV. Together with the gating control bit field TCSRL.TDEN, the user can set up the transmit data word without starting the transmission. A possible program

sequence could be: clear TCSRL.TDEN = 00_B, write data to TBUFx, clear TCSRL.TDV by writing FMRL.MTDV = 10_B, re-enable the gating with TCSRL.TDEN = 01_B and then set TCSRL.TDV under software control by writing FMRL.MTDV = 01_B.

21.2.10 Operating the Receive Data Path

The receive data path is based on two 16-bit wide receive shift registers RSR0 and RSR1 and a receive buffer for each of them (RBUF0 and RBUF1). The data transfer parameters like data word length, data frame length, or the shift direction are controlled commonly for transmission and reception by the shift control registers.

Register RBUF01SRL monitors the status of RBUF0 and register RBUF01SRH of RBUF1.

21.2.10.1 Receive Buffering

The receive shift registers cannot be directly accessed by software, but their contents are automatically loaded into the receive buffer registers RBUF0 (or RBUF1 respectively) if a complete data word has been received or the frame is finished. The received data words in RBUF0 or RBUF1 can be read out in the correct order directly from register RBUF or, optionally, from a FIFO buffer stage (see [Page 21-79](#)).

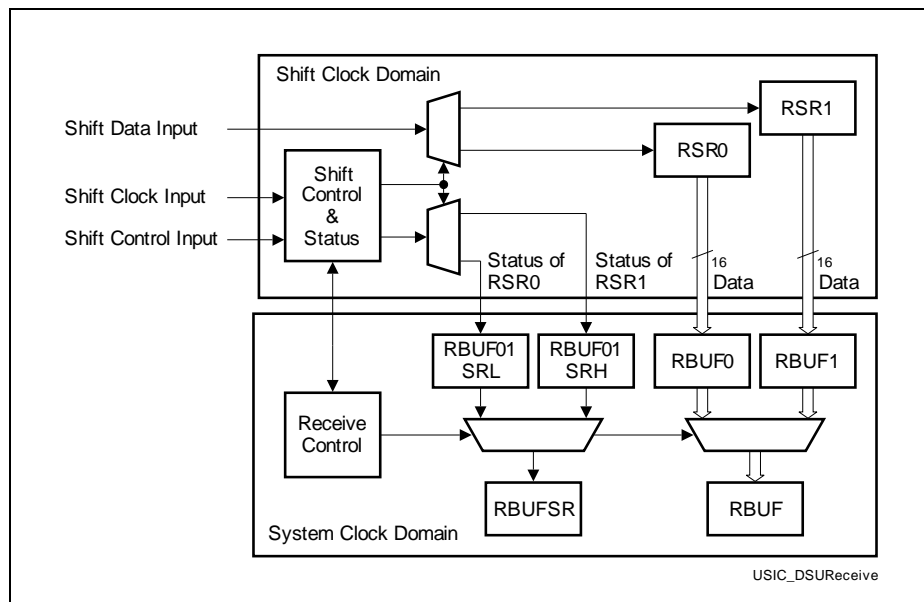


Figure 21-17 Receive Data Path

21.2.10.2 Baud Rate Constraints

The following baud rate constraints have to be respected to ensure correct data reception and buffering. The user has to take care about these restrictions when selecting the baud rate and the data word length with respect to the module clock frequency f_{SYS} .

- A received data word in a receiver shift register RSRx must be held constant for at least 4 periods of f_{SYS} in order to ensure correct loading of the related receiver buffer register RBUFx.
- The shift control signal has to be constant inactive for at least 5 periods of f_{SYS} between two consecutive frames in order to correctly detect the end of a frame.
- The shift control signal has to be constant active for at least 1 period of f_{SYS} in order to correctly detect a frame (shortest frame).
- A minimum setup and hold time of the shift control signal with respect to the shift clock signal has to be ensured.

21.2.11 Transfer Control and Status Registers

21.2.11.1 Shift Control Registers

The data shift unit is controlled by the registers defined in this section. The values in these registers are applied for data transmission and reception.

Please note that the shift control settings SDIR, WLE, and FLE are shared between transmitter and receiver. They are internally “frozen” for a each data word transfer in the transmitter with the first transmit shift clock edge and with the first receive shift clock edge in the receiver. The software has to take care that updates of these bit fields by software are done coherently (e.g. refer to the receiver start event indication PSR.RSIF).

SCTRL

Shift Control Register L

(30_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0						TRM		DOCFG		0			PDL		S DIR
r						rw		rw		r			rw		rw

Field	Bits	Type	Description
SDIR	0	rw	Shift Direction This bit defines the shift direction of the data words for transmission and reception. 0 _B Shift LSB first. The first data bit of a data word is located at bit position 0. 1 _B Shift MSB first. The first data bit of a data word is located at the bit position given by bit field SCTR.H.WLE.
PDL	1	rw	Passive Data Level This bit defines the output level at the shift data output signal when no data is available for transmission. The PDL level is output with the first relevant transmit shift clock edge of a data word. 0 _B The passive data level is 0. 1 _B The passive data level is 1.
DOCFG	[7:6]	rw	Data Output Configuration This bit defines the relation between the internal shift data value and the data output signal DOUT. X0 _B DOUT = shift data value X1 _B DOUT = inverted shift data value

Universal Serial Interface Channel

Field	Bits	Type	Description
TRM	[9:8]	rw	Transmission Mode This bit field describes how the shift control signal is interpreted by the DSU. Data transfers are only possible while the shift control signal is active. 00 _B The shift control signal is considered as inactive and data frame transfers are not possible. 01 _B The shift control signal is considered active if it is at 1-level. This is the setting to be programmed to allow data transfers. 10 _B The shift control signal is considered active if it is at 0-level. It is recommended to avoid this setting and to use the inversion in the DX2 stage in case of a low-active signal. 11 _B The shift control signal is considered active without referring to the actual signal level. Data frame transfer is possible after each edge of the signal.
0	[5:2], [15:10]	r	Reserved Read as 0; should be written with 0.

SCTRH

Shift Control Register H

(32_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				WLE				0		FLE					
r				rwh				r		rwh					

Field	Bits	Type	Description
FLE	[5:0]	rwh	Frame Length This bit field defines how many bits are transferred within a data frame. A data frame can consist of several concatenated data words. If TCSRL.FLEMD = 1, the value can be updated automatically by the data handler.
WLE	[11:8]	rwh	Word Length This bit field defines the data word length (amount of bits that are transferred in each data word) for reception and transmission. The data word is always right-aligned in the data buffer at the bit positions [WLE down to 0]. If TCSRL.WLEMD = 1, the value can be updated automatically by the data handler. 0 _H The data word contains 1 data bit located at bit position 0. 1 _H The data word contains 2 data bits located at bit positions [1:0]. ... E _H The data word contains 15 data bits located at bit positions [14:0]. F _H The data word contains 16 data bits located at bit positions [15:0].
0	[7:6], [15:12]	r	Reserved Read as 0; should be written with 0.

21.2.11.2 Transmission Control and Status Registers

The data transmission is controlled by register TCSRL.

TCSRL

Transmit Control/Status Register L (3C_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	WA	TD VTR	TDEN	0	TD SSM	TDV	EOF	SOF	0	WA MD	FLE MD	SEL MD	WLE MD		
r	rwh	rw	rw		r	rw	rh	rwh	rwh	r	rw	rw	rw	rw	

Field	Bits	Type	Description
WLEMD	0	rw	<p>WLE Mode</p> <p>This bit enables the data handler to automatically update the bit field SCTRH.WLE by the transmit control information TCI[3:0] and bit TCSR.EOF by TCI[4] (see Page 21-52). If enabled, an automatic update takes place when new data is loaded to register TBUF, either by writing to one of the transmit buffer input locations TBUFx or by an optional data buffer.</p> <p>0_B The automatic update of SCTRH.WLE and TCSR.EOF is disabled.</p> <p>1_B The automatic update of SCTRH.WLE and TCSR.EOF is enabled.</p>
SELMD	1	rw	<p>Select Mode</p> <p>This bit can be used mainly for the SSC protocol. It enables the data handler to automatically update bit field PCRH.CTR[20:16] by the transmit control information TCI[4:0] and clear bit field PCRH.CTR[23:21] (see Page 21-52). If enabled, an automatic update takes place when new data is loaded to register TBUF, either by writing to one of the transmit buffer input locations TBUFx or by an optional data buffer.</p> <p>0_B The automatic update of PCRH.CTR[23:16] is disabled.</p> <p>1_B The automatic update of PCRH.CTR[23:16] is enabled.</p>

Field	Bits	Type	Description
FLEMD	2	rw	FLE Mode This bit enables the data handler to automatically update bits SCTR.H.FLE[4:0] by the transmit control information TCI[4:0] and to clear bit SCTR.H.FLE[5] (see Page 21-52). If enabled, an automatic update takes place when new data is loaded to register TBUF, either by writing to one of the transmit buffer input locations TBUFx or by an optional data buffer. 0 _B The automatic update of FLE is disabled. 1 _B The automatic update of FLE is enabled.
WAMD	3	rw	WA Mode This bit can be used mainly for the IIS protocol. It enables the data handler to automatically update bit TCSRL.WA by the transmit control information TCI[4] (see Page 21-52). If enabled, an automatic update takes place when new data is loaded to register TBUF, either by writing to one of the transmit buffer input locations TBUFx or by an optional data buffer. 0 _B The automatic update of bit WA is disabled. 1 _B The automatic update of bit WA is enabled.
SOF	5	rw	Start Of Frame This bit is only taken into account for the SSC protocol, otherwise it is ignored. It indicates that the data word in TBUF is considered as the first word of a new SSC frame if it is valid for transmission (TCSRL.TDV = 1). This bit becomes cleared when the TBUF data word is transferred to the transmit shift register. 0 _B The data word in TBUF is not considered as first word of a frame. 1 _B The data word in TBUF is considered as first word of a frame. A currently running frame is finished and MSLS becomes deactivated (respecting the programmed delays).

Universal Serial Interface Channel

Field	Bits	Type	Description
EOF	6	rwh	<p>End Of Frame</p> <p>This bit is only taken into account for the SSC protocol, otherwise it is ignored. It can be modified automatically by the data handler if bit WLEMD = 1. It indicates that the data word in TBUF is considered as the last word of an SSC frame. If it is the last word, the MSLS signal becomes inactive after the transfer, respecting the programmed delays. This bit becomes cleared when the TBUF data word is transferred to the transmit shift register.</p> <p>0_B The data word in TBUF is not considered as last word of an SSC frame.</p> <p>1_B The data word in TBUF is considered as last word of an SSC frame.</p>
TDV	7	rh	<p>Transmit Data Valid</p> <p>This bit indicates that the data word in the transmit buffer TBUF can be considered as valid for transmission. The TBUF data word can only be sent out if TDV = 1. It is automatically set when data is moved to TBUF (by writing to one of the transmit buffer input locations TBUFx, or optionally, by the bypass or FIFO mechanism).</p> <p>0_B The data word in TBUF is not valid for transmission.</p> <p>1_B The data word in TBUF is valid for transmission and a transmission start is possible. New data should not be written to a TBUFx input location while TDV = 1.</p>

Universal Serial Interface Channel

Field	Bits	Type	Description
TDSSM	8	rw	<p>TBUF Data Single Shot Mode</p> <p>This bit defines if the data word TBUF data is considered as permanently valid or if the data should only be transferred once.</p> <p>0_B The data word in TBUF is not considered as invalid after it has been loaded into the transmit shift register. The loading of the TBUF data into the shift register does not clear TDV.</p> <p>1_B The data word in TBUF is considered as invalid after it has been loaded into the shift register. In ASC and IIC mode, TDV is cleared with the TBI event, whereas in SSC and IIS mode, it is cleared with the RSI event.</p> <p>TDSSM = 1 has to be programmed if an optional data buffer is used.</p>
TDEN	[11:10]	rw	<p>TBUF Data Enable</p> <p>This bit field controls the gating of the transmission start of the data word in the transmit buffer TBUF.</p> <p>00_B A transmission start of the data word in TBUF is disabled. If a transmission is started, the passive data level is sent out.</p> <p>01_B A transmission of the data word in TBUF can be started if TDV = 1.</p> <p>10_B A transmission of the data word in TBUF can be started if TDV = 1 while DX2S = 0.</p> <p>11_B A transmission of the data word in TBUF can be started if TDV = 1 while DX2S = 1.</p>
TDVTR	12	rw	<p>TBUF Data Valid Trigger</p> <p>This bit enables the transfer trigger unit to set bit TCSRH.TE if the trigger signal DX2T becomes active for event driven transfer starts, e.g. timer-based or depending on an event at an input pin. Bit TDVTR has to be 0 for protocols where the input stage DX2 is used for data shifting.</p> <p>0_B Bit TCSRH.TE is permanently set.</p> <p>1_B Bit TCSRH.TE is set if DX2T becomes active while TDV = 1.</p>

Universal Serial Interface Channel

Field	Bits	Type	Description
WA	13	rwh	Word Address This bit is only taken into account for the IIS protocol, otherwise it is ignored. It can be modified automatically by the data handler if bit WAMD = 1. Bit WA defines for which channel the data stored in TBUF will be transmitted. 0 _B The data word in TBUF will be transmitted after a falling edge of WA has been detected (referring to PSR.WA). 1 _B The data word in TBUF will be transmitted after a rising edge of WA has been detected (referring to PSR.WA).
0	4, 9, [15:14]	r	Reserved Read as 0; should be written with 0.

The data transmission status is monitored by register TCSRH.

TCSRH

Transmit Control/Status Register H (3E_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0			TE	TVC	TV	0	T SOF	0							
r			rh	rh	rh	r	rh	r							

Field	Bits	Type	Description
TSOF	8	rh	Transmitted Start Of Frame This bit indicates if the latest start of a data word transmission has taken place for the first data word of a new data frame. This bit is updated with the transmission start of each data word. 0 _B The latest data word transmission has not been started for the first word of a data frame. 1 _B The latest data word transmission has been started for the first word of a data frame.
TV	10	rh	Transmission Valid This bit represents the transmit buffer underflow and indicates if the latest start of a data word transmission has taken place with a valid data word from the transmit buffer TBUF. This bit is updated with the transmission start of each data word. 0 _B The latest start of a data word transmission has taken place while no valid data was available. As a result, the transmission of a data words with passive level (SCTRL.PDL) has been started. 1 _B The latest start of a data word transmission has taken place with valid data from TBUF.
TVC	11	rh	Transmission Valid Cumulated This bit cumulates the transmit buffer underflow indication TV. It is cleared automatically together with bit TV and has to be set by writing FMRL.ATVC = 1. 0 _B Since TVC has been set, at least one data buffer underflow condition has occurred. 1 _B Since TVC has been set, no data buffer underflow condition has occurred.

Field	Bits	Type	Description
TE	12	rh	<p>Trigger Event</p> <p>If the transfer trigger mechanism is enabled, this bit indicates that a trigger event has been detected ($DX2T = 1$) while $TCSRL.TDV = 1$. If the event trigger mechanism is disabled, the bit TE is permanently set. It is cleared by writing $FMRL.MTDV = 10_B$ or when the data word located in TBUF is loaded into the shift register.</p> <p>0_B The trigger event has not yet been detected. A transmission of the data word in TBUF can not be started.</p> <p>1_B The trigger event has been detected (or the trigger mechanism is switched off) and a transmission of the data word in TBUF can be started.</p>
0	[7:0], 9, [15:13]	r	<p>Reserved</p> <p>Read as 0; should be written with 0.</p>

21.2.11.3 Flag Modification Registers

The flag modification registers FMRL, FMRH allow the modification of control and status flags related to data handling by using only write accesses. Read accesses to FMRL, FMRH always deliver 0 at all bit positions.

Additionally, the service request outputs of this USIC channel can be activated by software (the activation is triggered by the write access and is deactivated automatically).

FMRL

Flag Modification Register L

(38_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C RDV 1	C RDV 0					0					A TVC	0		MTDV	
w	w					r					w	r		w	

Field	Bits	Type	Description
MTDV	[1:0]	w	Modify Transmit Data Valid Writing to this bit field can modify bits TCSR.L.TDV and TCSR.H.TE to control the start of a data word transmission by software. 00 _B No action. 01 _B Bit TDV is set, TE is unchanged. 10 _B Bits TDV and TE are cleared. 11 _B Reserved
ATVC	4	w	Activate Bit TVC Writing to this bit can set bit TCSR.H.TVC to start a new cumulation of the transmit buffer underflow condition. 0 _B No action. 1 _B Bit TCSR.H.TVC is set.
CRDV0	14	w	Clear Bits RDV for RBUF0 Writing 1 to this bit clears bits RBUF01SRL.RDV00 and RBUF01SRH.RDV10 to declare the received data in RBUF0 as no longer valid (to emulate a read action). 0 _B No action. 1 _B Bits RBUF01SRL.RDV00 and RBUF01SRH.RDV10 are cleared.

Universal Serial Interface Channel

Field	Bits	Type	Description
CRDV1	15	w	Clear Bit RDV for RBUF1 Writing 1 to this bit clears bits RBUF01SRL.RDV01 and RBUF01SRH.RDV11 to declare the received data in RBUF1 as no longer valid (to emulate a read action). 0 _B No action. 1 _B Bits RBUF01SRL.RDV01 and RBUF01SRH.RDV11 are cleared.
0	[3:2], [13:5]	r	Reserved Read as 0; should be written with 0.

FMRH

Flag Modification Register H

(3A_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0												SI O3	SI O2	SI O1	SI O0
r												w	w	w	w

Field	Bits	Type	Description
SIO0, SIO1, SIO2, SIO3	0, 1, 2, 3	w	Set Interrupt Output SRx Writing a 1 to this bit field activates the service request output SRx of this USIC channel. It has no impact on service request outputs of other USIC channels. 0 _B No action. 1 _B The service request output SRx is activated.
0	[15:4]	r	Reserved Read as 0; should be written with 0.

21.2.12 Data Buffer Registers

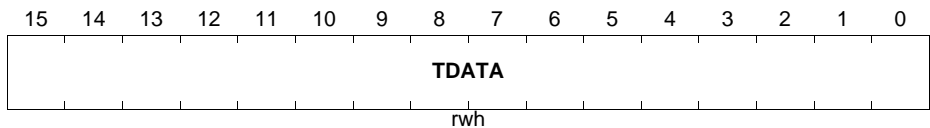
21.2.12.1 Transmit Buffer Locations

The 32 independent data input locations TBUF00 to TBUF31 are address locations that can be used as data entry locations for the transmit buffer. Data written to one of these locations will appear in a common register TBUF. Additionally, the 5 bit coding of the number [31:0] of the addressed data input location represents the transmit control information TCI (please refer to the protocol sections for more details).

The internal transmit buffer register TBUF contains the data that will be loaded to the transmit shift register for the next transmission of a data word. It can be read out at all TBUF00 to TBUF31 addresses.

TBUF_x (x = 00-31)

Transmit Buffer Input Location x **(80_H + x*4)** **Reset Value: 0000_H**



Field	Bits	Type	Description
TDATA	[15:0]	rwh	Transmit Data This bit field contains the data to be transmitted (read view). A data write action to at least the low byte of TDATA sets TCSRL.TDV.

21.2.12.2 Receive Buffer Registers RBUF0, RBUF1

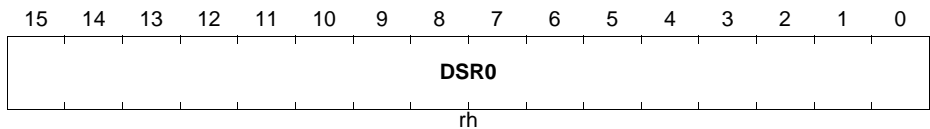
The receive buffer register RBUF0 contains the data received from RSR0. A read action does not change the status of the receive data from “not yet read = valid” to “already read = not valid”.

RBUF0

Receiver Buffer Register 0

(50_H)

Reset Value: 0000_H



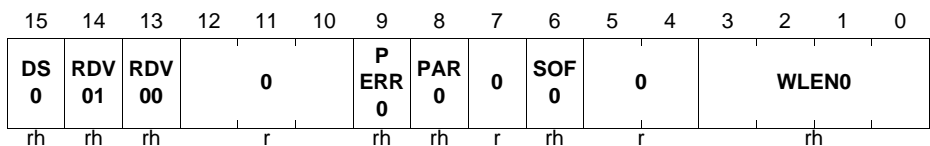
Field	Bits	Type	Description
DSR0	[15:0]	rh	Data of Shift Register 0

The receive buffer status register RBUF01SRL provides the status of the data in receive buffer RBUF0.

RBUF01SRL

Receiver Buffer 01 Status Register L (60_H)

Reset Value: 0000_H



Field	Bits	Type	Description
WLEN0	[3:0]	rh	Received Data Word Length in RBUF0 This bit field indicates how many bits have been received within the last data word stored in RBUF0. This number indicates how many data bits have to be considered as receive data, whereas the other bits in RBUF0 have been cleared automatically. The received bits are always right-aligned. 0 _H One bit has been received. ... F _H Sixteen bits have been received.

Universal Serial Interface Channel

Field	Bits	Type	Description
SOF0	6	rh	Start of Frame in RBUF0 This bit indicates whether the data word in RBUF0 has been the first data word of a data frame. 0 _B The data in RBUF0 has not been the first data word of a data frame. 1 _B The data in RBUF0 has been the first data word of a data frame.
PAR0	8	rh	Protocol-Related Argument in RBUF0 This bit indicates the value of the protocol-related argument. This value is elaborated depending on the selected protocol and adds additional information to the data word in RBUF0. The meaning of this bit is described in the corresponding protocol chapter.
PERR0	9	rh	Protocol-related Error in RBUF0 This bit indicates if the value of the protocol-related argument meets an expected value. This value is elaborated depending on the selected protocol and adds additional information to the data word in RBUF0. The meaning of this bit is described in the corresponding protocol chapter. 0 _B The received protocol-related argument PAR matches the expected value. The reception of the data word sets bit PSR.RIF and can generate a receive interrupt. 1 _B The received protocol-related argument PAR does not match the expected value. The reception of the data word sets bit PSR.AIF and can generate an alternative receive interrupt.

Universal Serial Interface Channel

Field	Bits	Type	Description
RDV00	13	rh	<p>Receive Data Valid in RBUF0</p> <p>This bit indicates the status of the data content of register RBUF0. This bit is identical to bit RBUF01SRH.RDV10 and allows consisting reading of information for the receive buffer registers. It is set when a new data word is stored in RBUF0 and automatically cleared if it is read out via RBUF.</p> <p>0_B Register RBUF0 does not contain data that has not yet been read out.</p> <p>1_B Register RBUF0 contains data that has not yet been read out.</p>
RDV01	14	rh	<p>Receive Data Valid in RBUF1</p> <p>This bit indicates the status of the data content of register RBUF1. This bit is identical to bit RBUF01SRH.RDV11 and allows consisting reading of information for the receive buffer registers. It is set when a new data word is stored in RBUF1 and automatically cleared if it is read out via RBUF.</p> <p>0_B Register RBUF1 does not contain data that has not yet been read out.</p> <p>1_B Register RBUF1 contains data that has not yet been read out.</p>
DS0	15	rh	<p>Data Source</p> <p>This bit indicates which receive buffer register (RBUF0 or RBUF1) is currently visible in registers RBUF(D) and in RBUFSR for the associated status information. It indicates which buffer contains the oldest data (the data that has been received first). This bit is identical to bit RBUF01SRH.DS1 and allows consisting reading of information for the receive buffer registers.</p> <p>0_B The register RBUF contains the data of RBUF0 (same for associated status information).</p> <p>1_B The register RBUF contains the data of RBUF1 (same for associated status information).</p>
0	[5:4], 7, [12:10]	r	<p>Reserved</p> <p>Read as 0; should be written with 0.</p>

Universal Serial Interface Channel

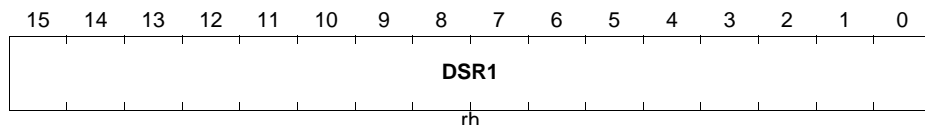
The receive buffer register RBUF1 contains the data received from RSR1. A read action does not change the status of the receive data from "not yet read = valid" to "already read = not valid".

RBUF1

Receiver Buffer Register 1

(54_H)

Reset Value: 0000_H



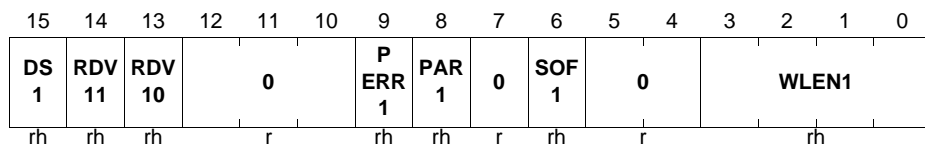
Field	Bits	Type	Description
DSR1	[15:0]	rh	Data of Shift Register 1

The receive buffer status register RBUF01SRH provides the status of the data in receive buffer RBUF1.

RBUF01SRH

Receiver Buffer 01 Status Register H (62_H)

Reset Value: 0000_H



Field	Bits	Type	Description
WLEN1	[3:0]	rh	Received Data Word Length in RBUF1 This bit field indicates how many bits have been received within the last data word stored in RBUF1. This number indicates how many data bits have to be considered as receive data, whereas the other bits in RBUF1 have been cleared automatically. The received bits are always right-aligned. 0 _H One bit has been received. ... F _H Sixteen bits have been received.

Field	Bits	Type	Description
SOF1	6	rh	Start of Frame in RBUF1 This bit indicates whether the data word in RBUF1 has been the first data word of a data frame. 0 _B The data in RBUF1 has not been the first data word of a data frame. 1 _B The data in RBUF1 has been the first data word of a data frame.
PAR1	8	rh	Protocol-Related Argument in RBUF1 This bit indicates the value of the protocol-related argument. This value is elaborated depending on the selected protocol and adds additional information to the data word in RBUF1. The meaning of this bit is described in the corresponding protocol chapter.
PERR1	9	rh	Protocol-related Error in RBUF1 This bit indicates if the value of the protocol-related argument meets an expected value. This value is elaborated depending on the selected protocol and adds additional information to the data word in RBUF1. The meaning of this bit is described in the corresponding protocol chapter. 0 _B The received protocol-related argument PAR matches the expected value. The reception of the data word sets bit PSR.RIF and can generate a receive interrupt. 1 _B The received protocol-related argument PAR does not match the expected value. The reception of the data word sets bit PSR.AIF and can generate an alternative receive interrupt.
RDV10	13	rh	Receive Data Valid in RBUF0 This bit indicates the status of the data content of register RBUF0. This bit is identical to bit RBUF01SRL.RDV00 and allows consisting reading of information for the receive buffer registers. 0 _B Register RBUF0 does not contain data that has not yet been read out. 1 _B Register RBUF0 contains data that has not yet been read out.

Field	Bits	Type	Description
RDV11	14	rh	Receive Data Valid in RBUF1 This bit indicates the status of the data content of register RBUF1. This bit is identical to bit RBUF01SRL.RDV01 and allows consisting reading of information for the receive buffer registers. 0 _B Register RBUF1 does not contain data that has not yet been read out. 1 _B Register RBUF1 contains data that has not yet been read out.
DS1	15	rh	Data Source This bit indicates which receive buffer register (RBUF0 or RBUF1) is currently visible in registers RBUF(D) and in RBUF SR for the associated status information. It indicates which buffer contains the oldest data (the data that has been received first). This bit is identical to bit RBUF01SRL.DS0 and allows consisting reading of information for the receive buffer registers. 0 _B The register RBUF contains the data of RBUF0 (same for associated status information). 1 _B The register RBUF contains the data of RBUF1 (same for associated status information).
0	[5:4], 7, [12:10]	r	Reserved Read as 0; should be written with 0.

21.2.12.3 Receive Buffer Registers RBUF, RBUFD, RBUFSR

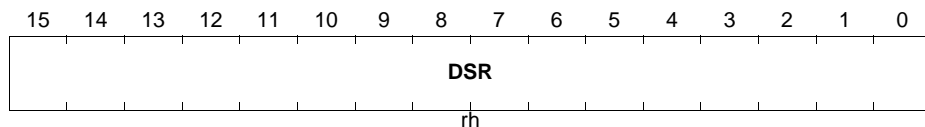
The receiver buffer register RBUF shows the content of the either RBUF0 or RBUF1, depending on the order of reception. Always the oldest data (the data word that has been received first) from both receive buffers can be read from RBUF. It is recommended to read out the received data from RBUF instead of RBUF0/1. With a read access of at least the low byte of RBUF, the status of the receive data is automatically changed from “not yet read = valid” to “already read = not valid”, the content of RBUF becomes updated, and the next received data word becomes visible in RBUF.

RBUF

Receiver Buffer Register

(5C_H)

Reset Value: 0000_H



Field	Bits	Type	Description
DSR	[15:0]	rh	Received Data This bit field monitors the content of either RBUF0 or RBUF1, depending on the reception sequence.

Universal Serial Interface Channel

If a debugger should be used to monitor the received data, the automatic update mechanism has to be de-activated to guaranty data consistency. Therefore, the receiver buffer register for debugging RBUFD is available. It is similar to RBUF, but without the automatic update mechanism by a read action. So a debugger (or other monitoring function) can read RBUFD without disturbing the receive sequence.

RBUFD

Receiver Buffer Register for Debugger (4C_H)

Reset Value: 0000_H



Field	Bits	Type	Description
DSR	[15:0]	rh	Data from Shift Register Same as RBUF.DSR, but without releasing the buffer after a read action.

Universal Serial Interface Channel

The receive buffer status register RBUFSR provides the status of the data in receive buffers RBUF and RBUFD. If bits RBUF01SRL.DS0 (or RBUF01SRH.DS1) are 0, the content of RBUF01SRL is monitored in RBUFSR, otherwise the content of RBUF01SRH is shown.

RBUFSR

Receiver Buffer Status Register

(58_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DS	RDV 1	RDV 0	0			P ERR	PAR	0	SOF	0	WLEN				
rh	rh	rh	r			rh	rh	r	rh	r	rh				

Field	Bits	Type	Description
WLEN	[3:0]	rh	Received Data Word Length in RBUF or RBUFD Description see RBUF01SRL.WLEN0 or RBUF01SRH.WLEN1.
SOF	6	rh	Start of Frame in RBUF or RBUFD Description see RBUF01SRL.SOF0 or RBUF01SRH.SOF1.
PAR	8	rh	Protocol-Related Argument in RBUF or RBUFD Description see RBUF01SRL.PAR0 or RBUF01SRH.PAR1.
PERR	9	rh	Protocol-related Error in RBUF or RBUFD Description see RBUF01SRL.PERR0 or RBUF01SRH.PERR1.
RDV0	13	rh	Receive Data Valid in RBUF or RBUFD Description see RBUF01SRL.RDV00 or RBUF01SRH.RDV10.
RDV1	14	rh	Receive Data Valid in RBUF or RBUFD Description see RBUF01SRL.RDV01 or RBUF01SRH.RDV11.
DS	15	rh	Data Source of RBUF or RBUFD Description see RBUF01SRL.DS0 or RBUF01SRH.DS1.
0	[5:4], 7, [12:10]	r	Reserved Read as 0; should be written with 0.

21.2.13 Operating the FIFO Data Buffer

The FIFO data buffers of a USIC module are built in a similar way, with transmit buffer and receive buffer capability for each channel. Depending on the device, the amount of available FIFO buffer area can vary. In the XC27x8X, totally 64 buffer entries can be distributed among the transmit or receive FIFO buffers of both channels of the USIC module.

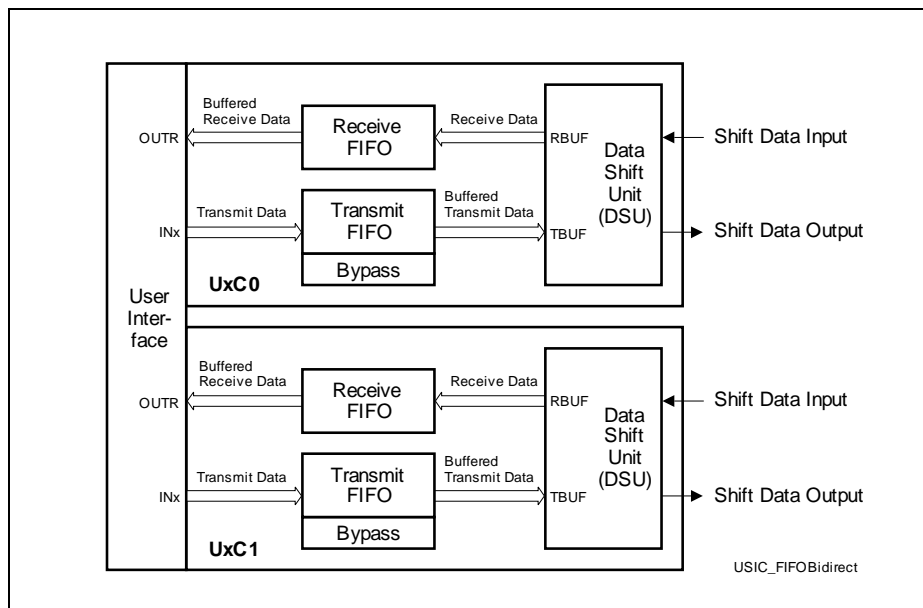


Figure 21-18 FIFO Buffer Overview

In order to operate the FIFO data buffers, the following issues have to be considered:

- **FIFO buffer available and selected:**
 The transmit FIFO buffer and the bypass structure are only available if CCFG.TB = 1, whereas the receive FIFO buffer is only available if CCFG.RB = 1.
 It is recommended to configure all buffer parameters while there is no data traffic for this USIC channel and the FIFO mechanism is disabled by TBCTRH.SIZE = 0 (for transmit buffer) or RBCTRH.SIZE = 0 (for receive buffer). The allocation of a buffer area by writing TBCTRL or RBCTRL has to be done while the corresponding FIFO buffer is disabled. The FIFO buffer interrupt control bits can be modified independently of data traffic.
- **FIFO buffer setup:**
 The total amount of available FIFO buffer entries limits the length of the transmit and receive buffers for each USIC channel.

- Bypass setup:
 In addition to the transmit FIFO buffer, a bypass can be configured as described on [Page 21-86](#).

21.2.13.1 FIFO Buffer Partitioning

If available, the FIFO buffer area consists of a defined number of FIFO buffer entries, each containing a data part and the associated control information (RCI for receive data, TCI for transmit data). One FIFO buffer entry represents the finest granularity that can be allocated to a receive FIFO buffer or a transmit FIFO buffer. All available FIFO buffer entries of a USIC module are located one after the other in the FIFO buffer area. The overall counting starts with FIFO entry 0, followed by 1, 2, etc.

For each USIC module, a certain number of FIFO entries is available, that can be allocated to the channels of the same USIC module. It is not possible to assign FIFO buffer area to USIC channels that are not located within the same USIC module.

For each USIC channel, the size of the transmit and the receive FIFO buffer can be chosen independently. For example, it is possible to allocate the full amount of available FIFO entries as transmit buffer for one USIC channel. Some possible scenarios of FIFO buffer partitioning are shown in [Figure 21-19](#).

Each FIFO buffer consists of a set of consecutive FIFO entries. The size of a FIFO data buffer can only be programmed as a power of 2, starting with 2 entries, then 4 entries, then 8 entries, etc. A FIFO data buffer can only start at a FIFO entry aligned to its size. For example, a FIFO buffer containing n entries can only start with FIFO entry 0, n , $2*n$, $3*n$, etc. and consists of the FIFO entries $[x*n, (x+1)*n-1]$, with x being an integer number (incl. 0). It is not possible to have "holes" with unused FIFO entries within a FIFO buffer, whereas there can be unused FIFO entries between two FIFO buffers.

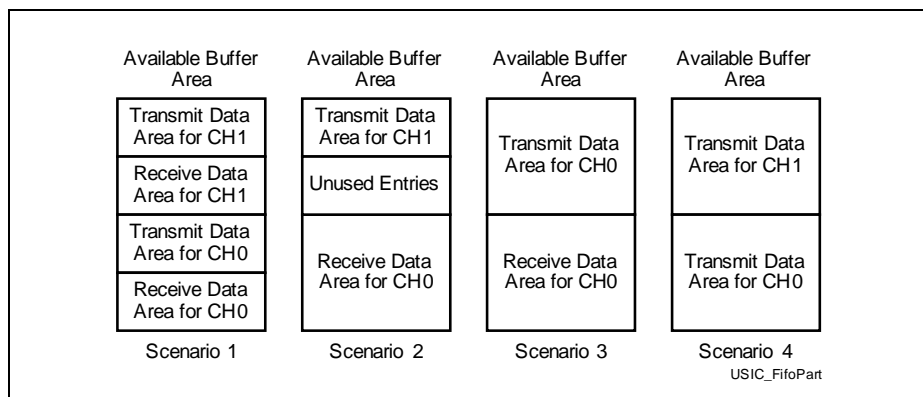


Figure 21-19 FIFO Buffer Partitioning

The data storage inside the FIFO buffers is based on pointers, that are internally updated whenever the data contents of the FIFO buffers have been modified. This happens automatically when new data is put into a FIFO buffer or the oldest data is taken from a FIFO buffer. As a consequence, the user program does not need to modify the pointers for data handling. Only during the initialization phase, the start entry of a FIFO buffer has to be defined by writing the number of the first FIFO buffer entry in the FIFO buffer to the corresponding bit field DPTR in register RBCTRL (for a receive FIFO buffer) or TBCTRL (for a transmit FIFO buffer) while the related bit field RBCTRH.SIZE=0 (or TBCTRH.SIZE = 0, respectively). The assignment of buffer entries to a FIFO buffer (regarding to size and pointers) must not be changed by software while the related USIC channel is taking part in data traffic.

21.2.13.2 Data Buffer Events and Interrupts

The transmit FIFO buffer mechanism detects the following events, that can lead to interrupts (if enabled).

- **Standard transmit buffer event:**
The filling level of the transmit buffer (given by TRBSRH.TBFLVL) exceeds (TBCTRH.LOF = 1) or falls below (TBCTRH.LOF = 0) a programmed limit (TBCTRL.LIMIT). The trigger of this event is the transition from equal to below or bigger, not the fact of being below or above.
If the standard transmit buffer event is used to indicate that new data has to be written to one of the INx locations, TBCTRH.LOF = 0 should be programmed.
- **Transmit buffer error event:**
The software has written to a full buffer. The written value is ignored.

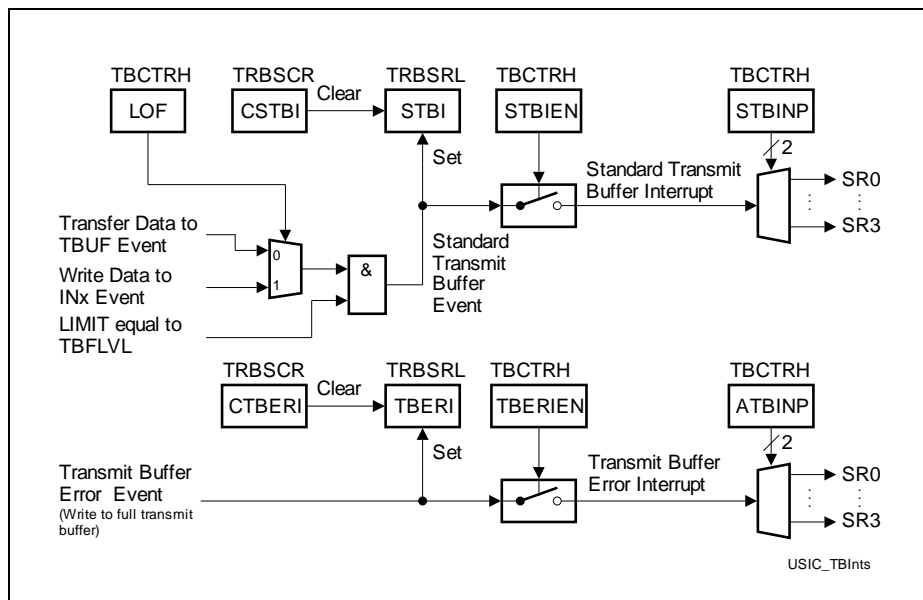


Figure 21-20 Transmit Buffer Events

The receive FIFO buffer mechanism detects the following events, that can lead to an interrupt (if enabled). The standard receive buffer event and the alternative receive buffer event can be programmed to two different modes, one referring to the filling level of the receive buffer, the other one related to a bit position in the receive control information RCI of the data word that becomes available in OUTRL.

If the interrupt generation refers to the filling level of the receive FIFO buffer, only the standard receive buffer event is used, whereas the alternative receive buffer event is not used. This mode can be selected to indicate that a certain amount of data has been received, without regarding the content of the associated RCI.

If the interrupt generation refers to RCI, the filling level is not taken into account. Each time a new data word becomes available in OUTRL, an event is detected. If bit RCI[4] = 0, a standard receive buffer event is signaled, otherwise an alternative receive buffer device (RCI[4] = 1). Depending on the selected protocol and the setting of RBCTR.H.RCIM, the value of RCI[4] can hold different information that can be used for protocol-specific interrupt handling (see protocol sections for more details).

- Standard receive buffer event in filling level mode (RBCTR.H.RNM = 0):
 The filling level of the receive buffer (given by TRBSR.H.RBFLVL) exceeds (RBCTR.H.LOF = 1) or falls below (RBCTR.H.LOF = 0) a programmed limit (RBCTR.H.LIMIT). The trigger of this event is the transition from equal to below or

greater, not the fact of being below or above.

If the standard receive buffer event is used to indicate that new data has to be read from OUTRL, RBCTRH.LOF = 1 should be programmed.

- Standard receive buffer event in RCI mode (RBCTRH.RNM = 1):
If the OUTR stage is updated with a new data value with RCI[4] = 0.
- Alternative receive buffer event in filling level mode (RBCTRH.RNM = 0): not used
- Alternative receive buffer event in RCI mode (RBCTRH.RNM = 1):
If the OUTR stage is updated with a new value with RCI[4] = 1.
- Receive buffer error event:
The software reads from an empty buffer. The read data is invalid.

Figure 21-21 shows the receiver buffer events and interrupts in filling level mode.

Note: A buffer event in filling level mode occurs only when the filling level transitions away from the threshold value. Transitions starting with a filling level other than the threshold level generate no trigger event.

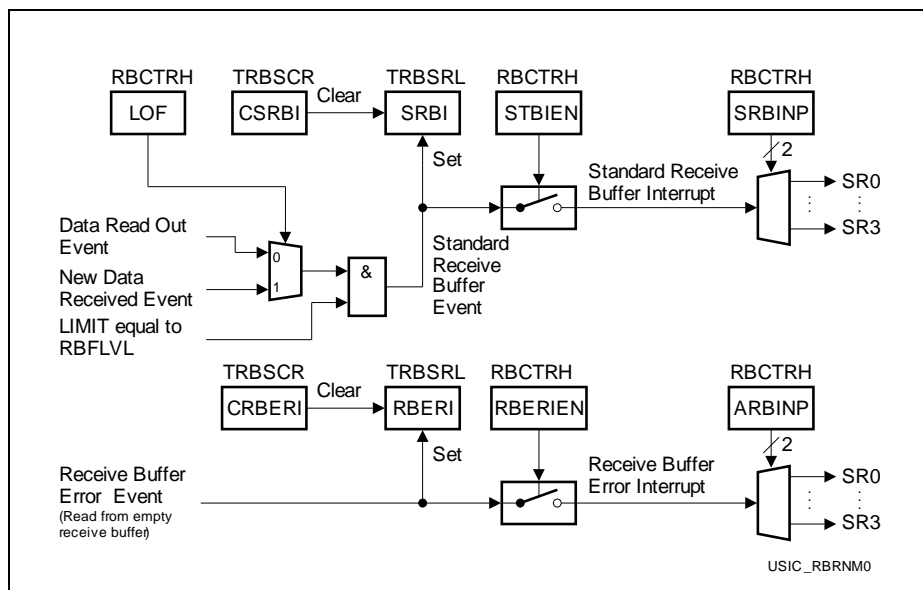


Figure 21-21 Receiver Buffer Events in Filling Level Mode

Figure 21-22 shows the receiver buffer events and interrupts in RCI mode.

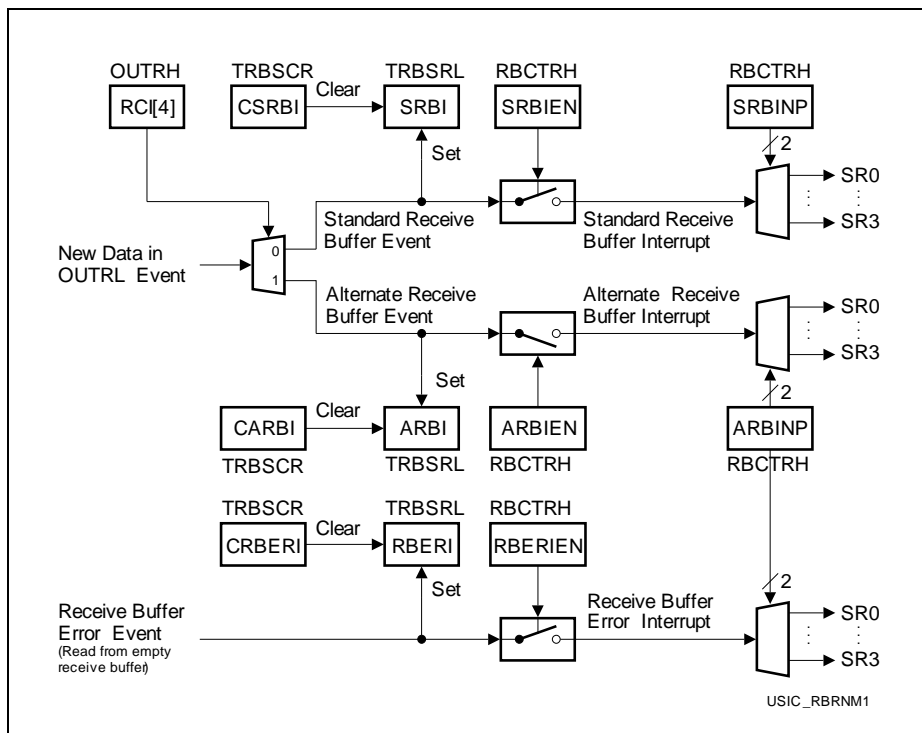


Figure 21-22 Receiver Buffer Events in RCI Mode

Table 21-7 shows the registers, bits and bit fields to indicate the buffer events and to control the interrupts related to the FIFO buffers (transmit and the receive) of a USIC channel.

Table 21-7 Buffer Events and Interrupt Handling

Event	Indication Flag	Indication cleared b	Interrupt enabled by	SRx Output selected by
Standard transmit buffer event	TRBSRL. STBI	TRBSCLR. CSTBI	TBCTRH. STBIEN	TBCTRH. STBINP
Transmit buffer error event	TRBSRL. TBERI	TRBSCLR. CTBERI	TBCTRH. TBERIEN	TBCTRH. ATBINP
Standard receive buffer event	TRBSRL. SRBI	TRBSCLR. CSRBI	RBCTRH. SRBIEN	RBCTRH. SRBINP

Table 21-7 Buffer Events and Interrupt Handling (cont'd)

Event	Indication Flag	Indication cleared b	Interrupt enabled by	SRx Output selected by
Alternative receive buffer event	TRBSRL. ARBI	TRBSCR. CARBI	RBCTRH. ARBIEN	RBCTRH. ARBINP
Receive buffer error event	TRBSRL. RBERI	TRBSCR. CRBERI	RBCTRH. RBERIEN	RBCTRH. ARBINTXDP

21.2.13.3 FIFO Buffer Bypass

The data bypass mechanism is part of the transmit FIFO control block. It allows to introduce a data word in the data stream without modifying the transmit FIFO buffer contents, e.g. to send a high-priority message. The bypass structure consists of a bypass data word of maximum 16 bits in register BYP and some associated control information in registers BYPCRL and BYPCRH. For example, these bits define the word length of the bypass data word and configure a transfer trigger and gating mechanism similar to the one for the transmit buffer TBUF.

The bypass data word can be tagged valid or invalid for transmission by bit BYRCRL.BDV (bypass data valid). A combination of data flow related and event related criteria define whether the bypass data word is considered valid for transmission. A data validation logic checks the start conditions for this data word. Depending on the result of the check, the transmit buffer register TBUF is loaded with different values, according to the following rules:

- Data from the transmit FIFO buffer or the bypass data can only be transferred to TBUF if TCSRL.TDV = 0 (TBUF is empty).
- Bypass data can only be transferred to TBUF if the bypass is enabled by BYPCRL.BDEN or the selecting gating condition is met.
- If the bypass data is valid for transmission and has either a higher transmit priority than the FIFO data or if the transmit FIFO is empty, the bypass data is transferred to TBUF.
- If the bypass data is valid for transmission and has a lower transmit priority than the FIFO buffer that contains valid data, the oldest transmit FIFO data is transferred to TBUF.
- If the bypass data is not valid for transmission and the FIFO buffer contains valid data, the oldest FIFO data is transferred to TBUF.
- If neither the bypass data is valid for transmission nor the transmit FIFO buffer contains valid data, TBUF is unchanged.

The bypass data validation is based on the logic blocks shown in [Figure 21-23](#).

- A transfer gating logic enables or disables the bypass data word transfer to TBUF under software or under hardware control. If the input stage DX2 is not needed for data shifting, signal DX2S can be used for gating purposes. The transfer gating logic is controlled by bit field BYPCRL.BDEN.
- A transfer trigger logic supports data word transfers related to events, e.g. timer based or related to an input pin. If the input stage DX2 is not needed for data shifting, signal DX2T can be used for trigger purposes. The transfer trigger logic is controlled by bit BYPCRL.BDVTR.
- A bypass data validation logic combining the inputs from the gating logic, the triggering logic and TCSRL.TDV.

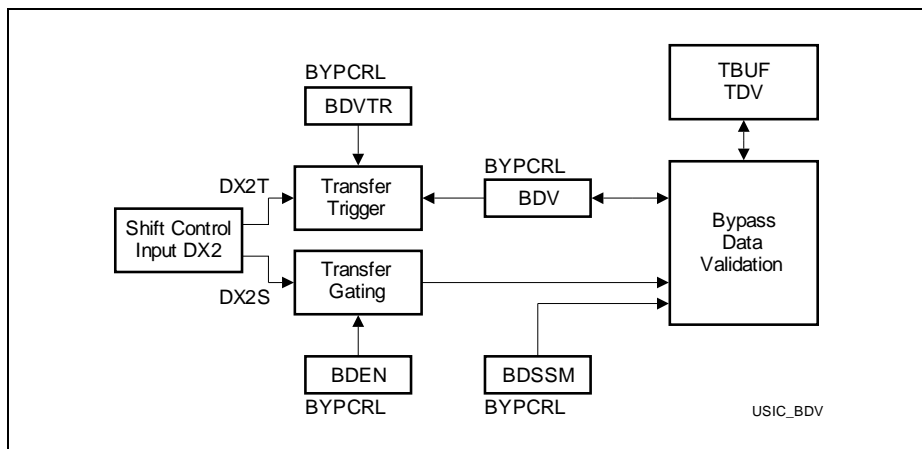


Figure 21-23 Bypass Data Validation

With this structure, the following bypass data transfer functionality can be achieved:

- Bit BYPCRL.BDSSM = 1 has to be programmed for a single-shot mechanism. After each transfer of the bypass data word to TBUF, the bypass data word has to be tagged valid again. This can be achieved either by writing a new bypass data word to BYP or by DX2T if BDVTR = 1 (e.g. trigger on a timer base or an edge at a pin).
- Bit BYPCRL.BDSSM = 0 has to be programmed if the bypass data is permanently valid for transmission (e.g. as alternative data if the data FIFO runs empty).

21.2.13.4 FIFO Access Constraints

The data in the shared FIFO buffer area is accessed by the hardware mechanisms for data transfer of each communication channel (for transmission and reception) and by software to read out received data or to write data to be transmitted. As a consequence, the data delivery rate can be limited by the FIFO mechanism. Each access by hardware to the FIFO buffer area has priority over a software access, that is delayed in case of an access collision.

In order to avoid data loss and stalling of the CPU due to delayed software accesses, the baud rate, the word length and the software access mechanism have to be taken into account. Each access to the FIFO data buffer area by software or by hardware takes one period of f_{SYS} . Especially a continuous flow of very short, consecutive data words can lead to an access limitation.

21.2.13.5 Handling of FIFO Transmit Control Information

In addition to the transmit data, the transmit control information TCI can be transferred from the transmit FIFO or bypass structure to the USIC channel. Depending on the selected protocol and the enabled update mechanism, some settings of the USIC channel parameters can be modified. The modifications are based on the TCI of the FIFO data word loaded to TBUF or by the bypass control information if the bypass data is loaded into TBUF.

- TCSRL.SELMD = 1: update of PCRH.CTR[20:16] by FIFO TCI or BYPCRH.BSELO with additional clear of PCRH.CTR[23:21]
- TCSRL.WLEMD = 1: update of SCTR.H.WLE and TCSRL.EOF by FIFO TCI or BYPCRL.BWLE (if the WLE information is overwritten by TCI or BWLE, the user has to take care that FLE is set accordingly)
- TCSRL.FLEMD = 1: update of SCTR.H.FLE[4:0] by FIFO TCI or BYPCRL.BWLE with additional clear of SCTR.H.FLE[5]
- TCSRL.WAMD = 1: update of TCSRL.WA by FIFO TCI[4]

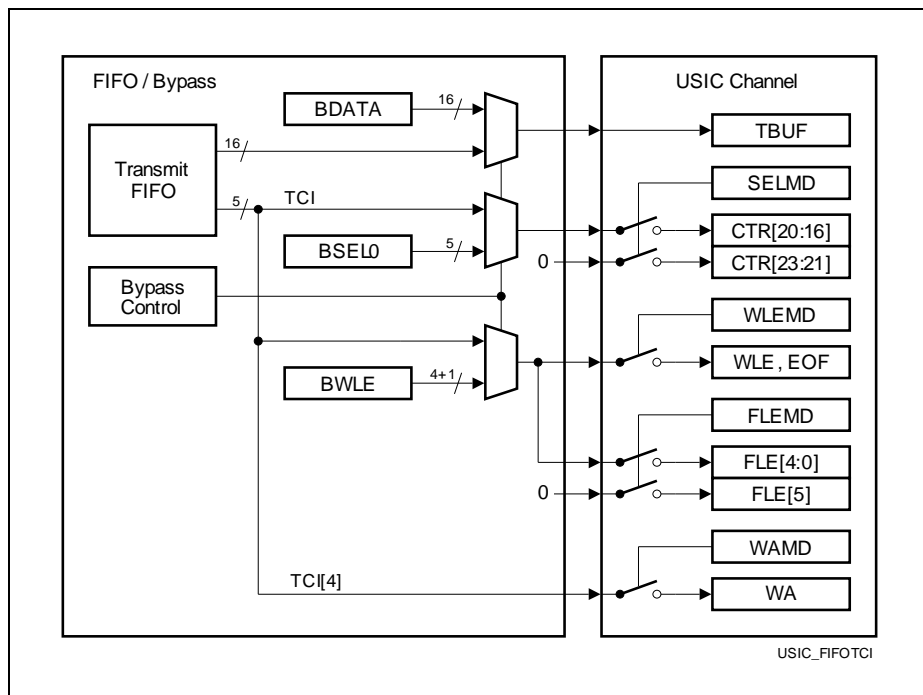


Figure 21-24 TCI Handling with FIFO / Bypass

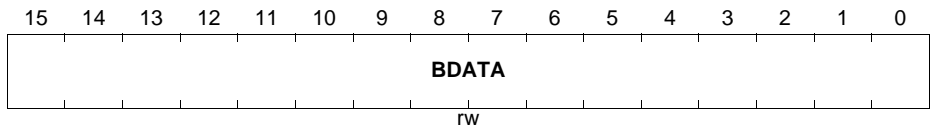
21.2.14 FIFO Buffer and Bypass Registers

21.2.14.1 Bypass Registers

A write action to at least the low byte of the bypass data register sets BYPCRL.BDV = 1 (bypass data tagged valid).

BYP

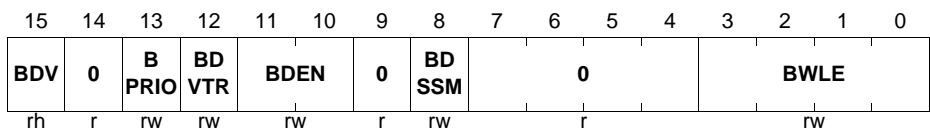
Bypass Data Register (100_H) **Reset Value: 0000_H**



Bit (Field)	Width	Type	Description
BDATA	[15:0]	rw	Bypass Data This bit field contains the bypass data.

BYPCRL

Bypass Control Register L (104_H) **Reset Value: 0000_H**



Field	Bits	Type	Description
BWLE	[3:0]	rw	Bypass Word Length This bit field defines the word length of the bypass data. The word length is given by BWLE + 1 with the data word being right-aligned in the data buffer at the bit positions [BWLE down to 0]. The bypass data word is always considered as an own frame with the length of BWLE. Same coding as SCTRH.WLE.

Field	Bits	Type	Description
BDSSM	8	rw	Bypass Data Single Shot Mode This bit defines if the bypass data is considered as permanently valid or if the bypass data is only transferred once (single shot mode). 0 _B The bypass data is still considered as valid after it has been loaded into TBUF. The loading of the data into TBUF does not clear BDV. 1 _B The bypass data is considered as invalid after it has been loaded into TBUF. The loading of the data into TBUF clears BDV.
BDEN	[11:10]	rw	Bypass Data Enable This bit field defines if and how the transfer of bypass data to TBUF is enabled. 00 _B The transfer of bypass data is disabled. 01 _B The transfer of bypass data to TBUF is possible. Bypass data will be transferred to TBUF according to its priority if BDV = 1. 10 _B Gated bypass data transfer is enabled. Bypass data will be transferred to TBUF according to its priority if BDV = 1 and while DX2S = 0. 11 _B Gated bypass data transfer is enabled. Bypass data will be transferred to TBUF according to its priority if BDV = 1 and while DX2S = 1.
BDVTR	12	rw	Bypass Data Valid Trigger This bit enables the bypass data for being tagged valid when DX2T is active (for time framing or time-out purposes). 0 _B Bit BDV is not influenced by DX2T. 1 _B Bit BDV is set if DX2T is active.
BPRIO	13	rw	Bypass Priority This bit defines the priority between the bypass data and the transmit FIFO data. 0 _B The transmit FIFO data has a higher priority than the bypass data. 1 _B The bypass data has a higher priority than the transmit FIFO data.

Universal Serial Interface Channel

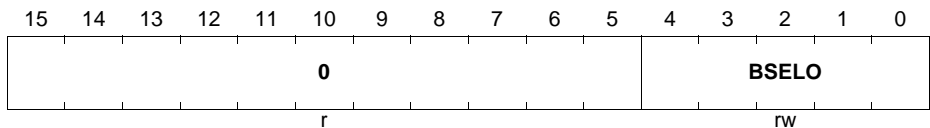
Field	Bits	Type	Description
BDV	15	rh	Bypass Data Valid This bit defines if the bypass data is valid for a transfer to TBUF. This bit is set automatically by a write access to at least the low-byte of register BYP. It can be cleared by software by writing TRBSCR.CBDV. 0 _B The bypass data is not valid. 1 _B The bypass data is valid.
0	[7:4], 9, 14	r	Reserved Read as 0; should be written with 0.

BYPCRH

Bypass Control Register H

(106_H)

Reset Value: 0000_H



Field	Bits	Type	Description
BSELO	[4:0]	rw	Bypass Select Outputs This bit field contains the value that is written to PCRH.CTR[20:16] if bypass data is transferred to TBUF. In the SSC protocol, this bit field can be used to define which SELOx output line will be activated when bypass data is transmitted.
0	[15:5]	r	Reserved Read as 0; should be written with 0.

21.2.14.2 General FIFO Buffer Control Registers

The transmit and receive FIFO status information of UxCy is given in registers UxCy_TRBSRL/H.

The bits related to the transmitter buffer in this register can only be written if the transmit buffer functionality is enabled by CCFG.TB = 1, otherwise write accesses are ignored. A similar behavior applies for the bits related to the receive buffer referring to CCFG.RB = 1.

The interrupt flags (event flags) in the transmit and receive FIFO status register TRBSRL can be cleared by writing a 1 to the corresponding bit position in register TRBSCR, whereas writing a 0 has no effect on these bits. Writing a 1 by software to SRBI, RBERI, ARBI, STBI, or TBERI sets the corresponding bit to simulate the detection of a transmit/receive buffer event, but without activating any service request output (therefore, see FMR.SIOx).

Bits TBUS and RBUS have been implemented for testing purposes. They can be ignored by data handling software. Please note that a read action can deliver either a 0 or a 1 for these bits. It is recommended to treat them as "don't care".

TRBSRL

Transmit/Receive Buffer Status Register L

(118_H)

Reset Value: 0808_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	T BUS	T FUL L	T EMP TY	0	TB ERI	ST BI	0	R BUS	R FUL L	R EMP TY	AR BI	RB ERI	SR BI		
r	rh	rh	rh	r	rwh	rwh	r	rh	rh	rh	rwh	rwh	rwh		

Field	Bits	Type	Description
SRBI	0	rwh	Standard Receive Buffer Event This bit indicates that a standard receive buffer event has been detected. It is cleared by writing TRBSCR.CSRBI = 1. If enabled by RBCTRH.SRBIEN, the service request output SRx selected by RBCTRH.SRBINP becomes activated if a standard receive buffer event is detected. 0 _B A standard receive buffer event has not been detected. 1 _B A standard receive buffer event has been detected.

Field	Bits	Type	Description
RBERI	1	rwh	<p>Receive Buffer Error Event</p> <p>This bit indicates that a receive buffer error event has been detected. It is cleared by writing <code>TRBSCR.CRBERI = 1</code>.</p> <p>If enabled by <code>RBCTRH.RBERIEN</code>, the service request output <code>SRx</code> selected by <code>RBCTRH.ARBINP</code> becomes activated if a receive buffer error event is detected.</p> <p>0_B A receive buffer error event has not been detected.</p> <p>1_B A receive buffer error event has been detected.</p>
ARBI	2	rwh	<p>Alternative Receive Buffer Event</p> <p>This bit indicates that an alternative receive buffer event has been detected. It is cleared by writing <code>TRBSCR.CARBI = 1</code>.</p> <p>If enabled by <code>RBCTRH.ARBIEN</code>, the service request output <code>SRx</code> selected by <code>RBCTRH.ARBINP</code> becomes activated if an alternative receive buffer event is detected.</p> <p>0_B An alternative receive buffer event has not been detected.</p> <p>1_B An alternative receive buffer event has been detected.</p>
REMPY	3	rh	<p>Receive Buffer Empty</p> <p>This bit indicates whether the receive buffer is empty.</p> <p>0_B The receive buffer is not empty.</p> <p>1_B The receive buffer is empty.</p>
RFULL	4	rh	<p>Receive Buffer Full</p> <p>This bit indicates whether the receive buffer is full.</p> <p>0_B The receive buffer is not full.</p> <p>1_B The receive buffer is full.</p>

Universal Serial Interface Channel

Field	Bits	Type	Description
RBUS	5	rh	Receive Buffer Busy This bit indicates whether the receive buffer is currently updated by the FIFO handler. 0 _B The receive buffer information has been completely updated. 1 _B The OUTRL/H update from the FIFO memory is ongoing. A read from OUTRL/H will be delayed. FIFO pointers from the previous read are not yet updated.
STBI	8	rwh	Standard Transmit Buffer Event This bit indicates that a standard transmit buffer event has been detected. It is cleared by writing TRBSCR.CSTBI = 1. If enabled by TBCTRH.STBIEN, the service request output SRx selected by TBCTRH.STBINP becomes activated if a standard transmit buffer event is detected. 0 _B A standard transmit buffer event has not been detected. 1 _B A standard transmit buffer event has been detected.
TBERI	9	rwh	Transmit Buffer Error Event This bit indicates that a transmit buffer error event has been detected. It is cleared by writing TRBSCR.CTBERI = 1. If enabled by TBCTRH.TBERIEN, the service request output SRx selected by TBCTRH.ATBINP becomes activated if a transmit buffer error event is detected. 0 _B A transmit buffer error event has not been detected. 1 _B A transmit buffer error event has been detected.
TEMPY	11	rh	Transmit Buffer Empty This bit indicates whether the transmit buffer is empty. 0 _B The transmit buffer is not empty. 1 _B The transmit buffer is empty.

Universal Serial Interface Channel

Field	Bits	Type	Description
TFULL	12	rh	Transmit Buffer Full This bit indicates whether the transmit buffer is full. 0 _B The transmit buffer is not full. 1 _B The transmit buffer is full.
TBUS	13	rh	Transmit Buffer Busy This bit indicates whether the transmit buffer is currently updated by the FIFO handler. 0 _B The transmit buffer information has been completely updated. 1 _B The FIFO memory update after write to INx is ongoing. A write to INx will be delayed. FIFO pointers from the previous INx write are not yet updated.
0	[7:6], 10, [15:14]	r	Reserved Read as 0; should be written with 0.

TRBSRH

Transmit/Receive Buffer Status Register H

(11A_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	TBFLVL						0	RBFLVL							
r	rh						r	rh							

Field	Bits	Type	Description
RBFLVL	[6:0]	rh	Receive Buffer Filling Level This bit field indicates the filling level of the receive buffer, starting with 0 for an empty buffer.
TBFLVL	[14:8]	rh	Transmit Buffer Filling Level This bit field indicates the filling level of the transmit buffer, starting with 0 for an empty buffer.
0	7, 15	r	Reserved Read as 0; should be written with 0.

Universal Serial Interface Channel

The bits in register TRBSCR are used to clear the notification bits in register TRBSRL or to clear the FIFO mechanism for the transmit or receive buffer. A read action always delivers 0.

TRBSCR

Transmit/Receive Buffer Status Clear Register

(11C_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLU SH TB	FLU SH RB	0			C BDV	C TB ERI	C ST BI	0				C AR BI	C RB ERI	C SR BI	
w	w	r			w	w	w	r				w	w	w	

Field	Bits	Type	Description
CSRBI	0	w	Clear Standard Receive Buffer Event 0 _B No effect. 1 _B Clear TRBSRL.SRBI.
CRBERI	1	w	Clear Receive Buffer Error Event 0 _B No effect. 1 _B Clear TRBSRL.RBERI.
CARBI	2	w	Clear Alternative Receive Buffer Event 0 _B No effect. 1 _B Clear TRBSRL.ARBI.
CSTBI	8	w	Clear Standard Transmit Buffer Event 0 _B No effect. 1 _B Clear TRBSRL.STBI.
CTBERI	9	w	Clear Transmit Buffer Error Event 0 _B No effect. 1 _B Clear TRBSRL.TBERI.
CBDV	10	w	Clear Bypass Data Valid 0 _B No effect. 1 _B Clear BYPCRL.BDV.
FLUSHRB	14	w	Flush Receive Buffer 0 _B No effect. 1 _B The receive FIFO buffer is cleared (filling level is cleared and output pointer is set to input pointer value). Should only be used while the FIFO buffer is not taking part in data traffic.

Field	Bits	Type	Description
FLUSHTB	15	w	Flush Transmit Buffer 0_B No effect. 1_B The transmit FIFO buffer is cleared (filling level is cleared and output pointer is set to input pointer value). Should only be used while the FIFO buffer is not taking part in data traffic.
0	[7:3], [13:11]	r	Reserved Read as 0; should be written with 0.

21.2.14.3 Transmit FIFO Buffer Control Registers

The transmit FIFO buffer is controlled by registers TBCTRL and TBCTRH. These registers can only be written if the transmit buffer functionality is enabled by CCFG.TB = 1, otherwise write accesses are ignored.

TBCTRL

Transmitter Buffer Control Register L (110_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		LIMIT						0		DPTR					
r		rw						r		w					

Field	Bits	Type	Description
DPTR	[5:0]	w	Data Pointer This bit field defines the start value for the transmit buffer pointers when assigning the FIFO entries to the transmit FIFO buffer. A read always delivers 0. When writing DPTR while SIZE = 0, both transmitter pointers TDIPTR and RTDOPTR in register TRBPTRL are updated with the written value and the buffer is considered as empty. A write access to DPTR while SIZE > 0 is ignored and does not modify the pointers.
LIMIT	[13:8]	rw	Limit For Interrupt Generation This bit field defines the target filling level of the transmit FIFO buffer that is used for the standard transmit buffer event detection.
0	[7:6], [15:14]	r	Reserved Read as 0; should be written with 0.

TBCTR_H

Transmitter Buffer Control Register H (112_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TB ERI EN	ST BI EN	0	LOF	0	SIZE			0			ATBINP		0	STBINP	
rw	rw	r	rw	r	rw			r			rw		r	rw	

Field	Bits	Type	Description
STBINP	[1:0]	rw	Standard Transmit Buffer Interrupt Node Pointer This bit field defines which service request output SR _x becomes activated in case of a standard transmit buffer event. 00 _B Output SR0 becomes activated. 01 _B Output SR1 becomes activated. 10 _B Output SR2 becomes activated. 11 _B Output SR3 becomes activated.
ATBINP	[4:3]	rw	Alternative Transmit Buffer Interrupt Node Pointer This bit field define which service request output SR _x will be activated in case of a transmit buffer error event. 00 _B Output SR0 becomes activated. 01 _B Output SR1 becomes activated. 10 _B Output SR2 becomes activated. 11 _B Output SR3 becomes activated.
SIZE	[10:8]	rw	Buffer Size This bit field defines the number of FIFO entries assigned to the transmit FIFO buffer. 000 _B The FIFO mechanism is disabled. The buffer does not accept any request for data. 001 _B The FIFO buffer contains 2 entries. 010 _B The FIFO buffer contains 4 entries. 011 _B The FIFO buffer contains 8 entries. 100 _B The FIFO buffer contains 16 entries. 101 _B The FIFO buffer contains 32 entries. 110 _B The FIFO buffer contains 64 entries. 111 _B Reserved

Universal Serial Interface Channel

Field	Bits	Type	Description
LOF	12	rw	Buffer Event on Limit Overflow This bit defines which relation between filling level and programmed limit leads to a standard transmit buffer event. 0_B A standard transmit buffer event occurs when the filling level equals the limit value and gets lower due to transmission of a data word. 1_B A standard transmit buffer interrupt event occurs when the filling level equals the limit value and gets bigger due to a write access to a data input location INx.
STBIEN	14	rw	Standard Transmit Buffer Interrupt Enable This bit enables/disables the generation of a standard transmit buffer interrupt in case of a standard transmit buffer event. 0_B The standard transmit buffer interrupt generation is disabled. 1_B The standard transmit buffer interrupt generation is enabled.
TBERIEN	15	rw	Transmit Buffer Error Interrupt Enable This bit enables/disables the generation of a transmit buffer error interrupt in case of a transmit buffer error event (software writes to a full transmit buffer). 0_B The transmit buffer error interrupt generation is disabled. 1_B The transmit buffer error interrupt generation is enabled.
0	2, [7:5], 11, 13	r	Reserved Read as 0; should be written with 0.

21.2.14.4 Receive FIFO Buffer Control Registers

The receive FIFO buffer is controlled by registers RBCTRL and RBCTRH. These registers can only be written if the receive buffer functionality is enabled by CCFG.RB = 1, otherwise write accesses are ignored.

RBCTRL

Receiver Buffer Control Register L (114_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		LIMIT						0		DPTR					
r		rw						r		w					

Field	Bits	Type	Description
DPTR	[5:0]	w	Data Pointer This bit field defines the start value for the receive buffer pointers when assigning the FIFO entries to the receive FIFO buffer. A read always delivers 0. When writing DPTR while SIZE = 0, both receiver pointers RDIPTR and RDOPTR in register TRBPTRH are updated with the written value and the buffer is considered as empty. A write access to DPTR while SIZE > 0 is ignored and does not modify the pointers.
LIMIT	[13:8]	rw	Limit For Interrupt Generation This bit field defines the target filling level of the receive FIFO buffer that is used for the standard receive buffer event detection.
0	[7:6], [15:14]	r	Reserved Read as 0; should be written with 0.

RBCTRH

Receiver Buffer Control Register H (116_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0							
RB ERI EN		SR BI EN		AR BI EN		LOF		RNM		SIZE			RCIM		0		ARBINP		0		SRBINP	
rw		rw		rw		rw		rw		rw			r		rw		r		rw			

Field	Bits	Type	Description
SRBINP	[1:0]	rw	Standard Receive Buffer Interrupt Node Pointer This bit field defines which service request output SRx becomes activated in case of a standard receive buffer event. 00 _B Output SR0 becomes activated. 01 _B Output SR1 becomes activated. 10 _B Output SR2 becomes activated. 11 _B Output SR3 becomes activated.
ARBINP	[4:3]	rw	Alternative Receive Buffer Interrupt Node Pointer This bit field defines which service request output SRx becomes activated in case of an alternative receive buffer event or a receive buffer error event. 00 _B The output SR0 becomes activated. 01 _B The output SR1 becomes activated. 10 _B The output SR2 becomes activated. 11 _B The output SR3 becomes activated.
RCIM	[7:6]	rw	Receiver Control Information Mode This bit field defines which information from the receiver status register RBUFSR is propagated as 5 bit receiver control information RCI[4:0] to the receive FIFO buffer and can be read out in registers OUT(D)RH. 00 _B RCI[4] = PERR, RCI[3:0] = WLEN 01 _B RCI[4] = SOF, RCI[3:0] = WLEN 10 _B RCI[4] = 0, RCI[3:0] = WLEN 11 _B RCI[4] = PERR, RCI[3] = PAR, RCI[2:1] = 00 _B , RCI[0] = SOF

Field	Bits	Type	Description
SIZE	[10:8]	rw	Buffer Size This bit field defines the number of FIFO entries assigned to the receive FIFO buffer. 000 _B The FIFO mechanism is disabled. The buffer does not accept any request for data. 001 _B The FIFO buffer contains 2 entries. 010 _B The FIFO buffer contains 4 entries. 011 _B The FIFO buffer contains 8 entries. 100 _B The FIFO buffer contains 16 entries. 101 _B The FIFO buffer contains 32 entries. 110 _B The FIFO buffer contains 64 entries. 111 _B Reserved
RNM	11	rw	Receiver Notification Mode This bit defines the receive buffer event mode. The receive buffer error event is not affected by RNM. 0 _B Filling level mode: A standard receive buffer event occurs when the filling level equals the limit value and changes, either due to a read access from OUTRL (LOF = 0) or due to a new received data word (LOF = 1). 1 _B RCI mode: A standard receive buffer event occurs when register OUTRL is updated with a new value if the corresponding value in OUTRH.RCI[4] = 0. If OUTRH.RCI[4] = 1, an alternative receive buffer event occurs instead of the standard receive buffer event.
LOF	12	rw	Buffer Event on Limit Overflow This bit defines which relation between filling level and programmed limit leads to a standard receive buffer event in filling level mode (RNM = 0). In RCI mode (RNM = 1), bit fields LIMIT and LOF are ignored. 0 _B A standard receive buffer event occurs when the filling level equals the limit value and gets lower due to a read access from OUTRL. 1 _B A standard receive buffer event occurs when the filling level equals the limit value and gets bigger due to the reception of a new data word.

Universal Serial Interface Channel

Field	Bits	Type	Description
ARBIEN	13	rw	Alternative Receive Buffer Interrupt Enable This bit enables/disables the generation of an alternative receive buffer interrupt in case of an alternative receive buffer event. 0_B The alternative receive buffer interrupt generation is disabled. 1_B The alternative receive buffer interrupt generation is enabled.
SRBIEN	14	rw	Standard Receive Buffer Interrupt Enable This bit enables/disables the generation of a standard receive buffer interrupt in case of a standard receive buffer event. 0_B The standard receive buffer interrupt generation is disabled. 1_B The standard receive buffer interrupt generation is enabled.
RBERIEN	15	rw	Receive Buffer Error Interrupt Enable This bit enables/disables the generation of a receive buffer error interrupt in case of a receive buffer error event (the software reads from an empty receive buffer). 0_B The receive buffer error interrupt generation is disabled. 1_B The receive buffer error interrupt generation is enabled.
0	2, 5	r	Reserved Read as 0; should be written with 0.

21.2.14.5 FIFO Buffer Data Registers

The 32 independent data input locations IN00 to IN31 are addresses that can be used as data entry locations for the transmit FIFO buffer. Data written to one of these locations will be stored in the transmit buffer FIFO. Additionally, the 5-bit coding of the number [31:0] of the addressed data input location represents the transmit control information TCI.

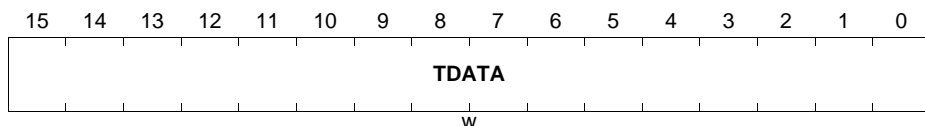
If the FIFO is already full and new data is written to it, the write access is ignored and a transmit buffer error event is signaled.

INx (x = 00-31)

Transmit FIFO Buffer Input Location x

$$(180_H + x * 4)$$

Reset Value: 0000_H



Field	Bits	Type	Description
TDATA	[15:0]	w	Transmit Data This bit field contains the data to be transmitted (write view), read actions deliver 0. A write action to at least the low byte of TDATA triggers the data storage in the FIFO.

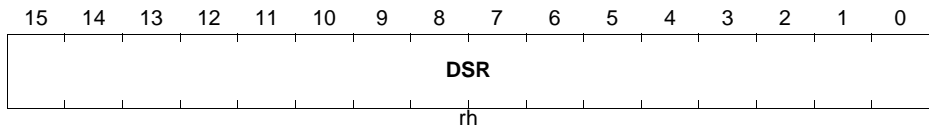
Universal Serial Interface Channel

The receiver FIFO buffer output register OUTRL shows the oldest received data word in the FIFO buffer. A read action from this address location delivers the received data. With a read access of at least the low byte, the data is declared to be read and the next entry becomes visible. Register OUTRH contains the receiver control information RCI containing the information selected by RBCTRH.RCIM. Write accesses to OUTRL/H are ignored.

OUTRL

Receiver Buffer Output Register L (120_H)

Reset Value: 0000_H

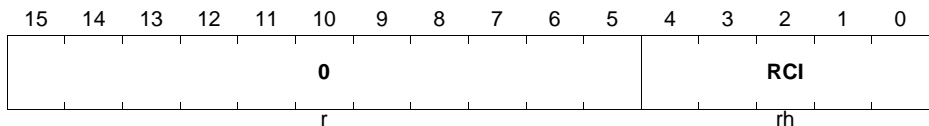


Field	Bits	Type	Description
DSR	[15:0]	rh	Received Data This bit field monitors the content of the oldest data word in the receive FIFO. Reading at least the low byte releases the buffer entry currently shown in DSR.

OUTRH

Receiver Buffer Output Register H (122_H)

Reset Value: 0000_H



Field	Bits	Type	Description
RCI	[4:0]	rh	Receiver Control Information This bit field monitors the receiver control information associated to DSR. The bit structure of RCI depends on bit field RBCTRH.RCIM.
0	[15:5]	r	Reserved Read as 0; should be written with 0.

Universal Serial Interface Channel

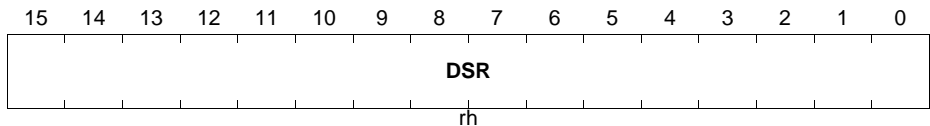
If a debugger should be used to monitor the received data in the FIFO buffer, the FIFO mechanism must not be activated in order to guaranty data consistency. Therefore, a second address set is available, named OUTDRL/H (D like debugger), having the same bit fields like the original buffer output register OUTRL/H, but without the FIFO mechanism. A debugger can read here (in order to monitor the receive data flow) without the risk of data corruption. Write accesses to OUTDRL/H are ignored.

OUTDRL

Receiver Buffer Output Register L for Debugger

(124_H)

Reset Value: 0000_H



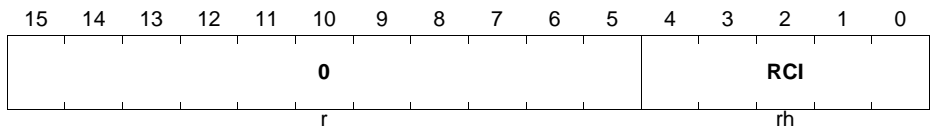
Field	Bits	Type	Description
DSR	[15:0]	rh	Data from Shift Register Same as OUTRL.DSR, but without releasing the buffer after a read action.

OUTDRH

Receiver Buffer Output Register H for Debugger

(126_H)

Reset Value: 0000_H



Field	Bits	Type	Description
RCI	[4:0]	rh	Receive Control Information from Shift Register Same as OUTRH.RCI.
0	[15:5]	r	Reserved Read as 0; should be written with 0.

21.2.14.6 FIFO Buffer Pointer Registers

The pointers for FIFO handling of the transmit and receive FIFO buffers are located in registers TRBPTRL (for the transmit buffer) and TRBPTRH (for the receive buffer). The pointers are automatically handled by the FIFO buffer mechanism and do not need to be modified by software. As a consequence, these registers can only be read by software (e.g. for verification purposes), whereas write accesses are ignored.

TRBPTRL

Transmit/Receive Buffer Pointer Register L

(108_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								0							
r					rh			r					rh		

Field	Bits	Type	Description
TDIPTR	[5:0]	rh	Transmitter Data Input Pointer This bit field indicates the buffer entry that will be used for the next transmit data coming from the INx addresses.
TDOPTR	[13:8]	rh	Transmitter Data Output Pointer This bit field indicates the buffer entry that will be used for the next transmit data to be output to TBUF.
0	[7:6], [15:14]	r	Reserved Read as 0; should be written with 0.

TRBPTRH

Transmit/Receive Buffer Pointer Register H
(10A_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								0							
r								r							

Field	Bits	Type	Description
RDIPTTR	[5:0]	rh	Receiver Data Input Pointer This bit field indicates the buffer entry that will be used for the next receive data coming from RBUF.
RDOPTTR	[13:8]	rh	Receiver Data Output Pointer This bit field indicates the buffer entry that will be used for the next receive data to be output at the OUT(D)RL addresses.
0	[7:6], [15:14]	r	Reserved Read as 0; should be written with 0.

21.3 Asynchronous Serial Channel (ASC = UART)

The asynchronous serial channel ASC covers the reception and the transmission of asynchronous data frames and provides a hardware LIN support. The receiver and transmitter being independent, frames can start at different points in time for transmission and reception. The ASC mode is selected by $CCR.MODE = 0010_B$ with $CCFG.ASC = 1$ (ASC mode available).

This chapter contains the following sections:

- Signal description (see [Page 21-110](#))
- Frame format (see [Page 21-111](#))
- Bit timing (see [Page 21-115](#))
- Operating the ASC (see [Page 21-114](#))
- Protocol registers (see [Page 21-123](#))
- Hardware LIN support (see [Page 21-129](#))

21.3.1 Signal Description

An ASC connection is characterized by the use of a single connection line between a transmitter and a receiver. The receiver input RXD signal is handled by the input stage DX0.

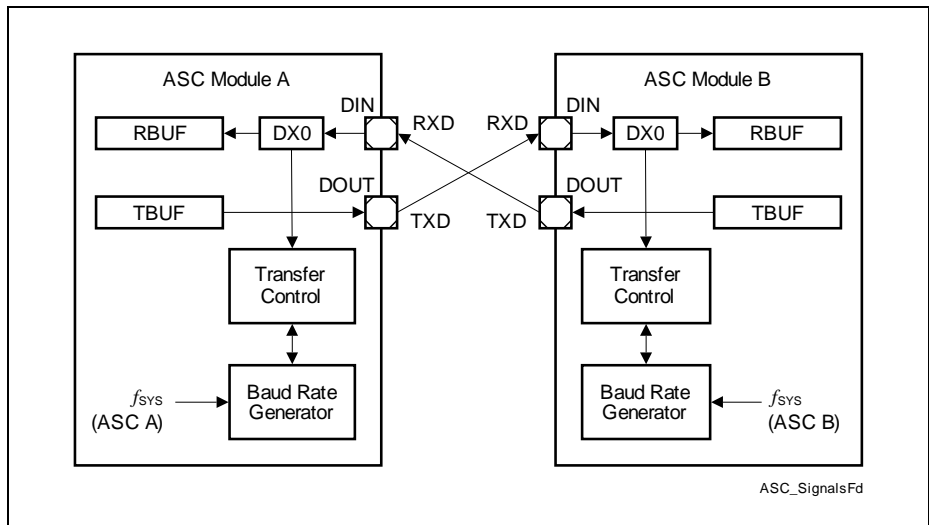


Figure 21-25 ASC Signal Connections for Full-Duplex Communication

For full-duplex communication, an independent communication line is needed for each transfer direction. [Figure 21-25](#) shows an example with a point-to-point full-duplex connection between two communication partners ASC A and ASC B.

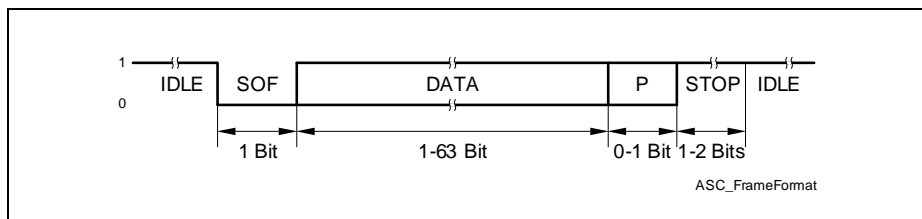


Figure 21-27 Standard ASC Frame Format

The protocol specific bits (SOF, P, STOP) are automatically handled by the ASC protocol state machine and do not appear in the data flow via the receive and transmit buffers.

21.3.2.1 Idle Time

The receiver and the transmitter independently check the respective data input lines (DX0, DX1) for being idle. The idle detection ensures that an SOF bit of a recently enabled ASC module does not collide with an already running frame of another ASC module.

In order to start the idle detection, the user software has to clear bits PSR.RXIDLE and/or PSR.TXIDLE, e.g. before selecting the ASC mode or during operation. If a bit is cleared by software while a data transfer is in progress, the currently running frame transfer is finished normally before starting the idle detection again. Frame reception is only possible if PSR.RXIDLE = 1 and frame transmission is only possible if PSR.TXIDLE = 1. The duration of the idle detection depends on the setting of bit PCRL.IDM. In the case that a collision is not possible, the duration can be shortened and the bus can be declared as being idle by setting PCRL.IDM = 0.

In the case that the complete idle detection is enabled by PCRL.IDM = 1, the data input of DX0 is considered as idle (PSR.RXIDLE becomes set) if a certain number of consecutive passive bit times has been detected. The same scheme applies for the transmitter's data input of DX1. Here, bit PSR.TXIDLE becomes set if the idle condition of this input signal has been detected.

The duration of the complete idle detection is given by the number of programmed data bits per frame plus 2 (in the case without parity) or plus 3 (in the case with parity). The counting of consecutive bit times with 1 level restarts from the beginning each time an edge is found, after leaving a stop mode or if ASC mode becomes enabled.

If the idle detection bits PSR.RXIDLE and/or TXIDLE are cleared by software, the counting scheme is not stopped (no re-start from the beginning). As a result, the cleared bit(s) can become set immediately again if the respective input line still meets the idle criterion.

Please note that the idle time check is based on bit times, so the maximum time can be up to 1 bit time more than programmed value (but not less).

21.3.2.2 Start Bit Detection

The receiver input signal DIN (selected signal of input stage DX0) is checked for a falling edge. An SOF bit is detected when a falling edge occurs while the receiver is idle or after the sampling point of the last stop bit. To increase noise immunity, the SOF bit timing starts with the first falling edge that is detected. If the sampled bit value of the SOF is 1, the previous falling edge is considered to be due to noise and the receiver is considered to be idle again.

21.3.2.3 Data Field

The length of the data field (number of data bits) can be programmed by bit field SCTR.H.FLE. It can vary between 1 and 63 data bits, corresponding to values of SCTR.H.FLE = 0 to 62 (the value of 63 is reserved and must not be programmed in ASC mode).

The data field can consist of several data words, e.g. a transfer of 12 data bits can be composed of two 8-bit words, with the 12 bits being split into 8-bits of the first word and 4 bits of the second word. The user software has to take care that the transmit data is available in-time, once a frame has been started. If the transmit buffer runs empty during a running data frame, the passive data level (SCTRL.PDL) is sent out.

The shift direction can be programmed by SCTRL.SDIR. The standard setting for ASC frames with LSB first is achieved with the default setting SDIR = 0.

21.3.2.4 Parity Bit

The ASC allows parity generation for transmission and parity check for reception on frame base. The type of parity can be selected by bit field CCR.PM, common for transmission and reception (no parity, even or odd parity). If the parity handling is disabled, the ASC frame does not contain any parity bit. For consistency reasons, all communication partners have to be programmed to the same parity mode.

After the last data bit of the data field, the transmitter automatically sends out its calculated parity bit if parity generation has been enabled. The receiver interprets this bit as received parity and compares it to its internally calculated one. The received parity bit value and the result of the parity check are monitored in the receiver buffer status registers as receiver buffer status information. These registers contain bits to monitor a protocol-related argument (PAR) and protocol-related error indication (PERR).

21.3.2.5 Stop Bit(s)

Each ASC frame is completed by 1 or 2 of stop bits with the signal level 1 (same level as the idle level). The number of stop bits is programmable by bit PSR.STPB. A new start bit can be transferred directly after the last stop bit.

21.3.3 Operating the ASC

In order to operate the ASC protocol, the following issues have to be considered:

- **Select ASC mode:**
It is recommended to configure all parameters of the ASC that do not change during run time while $CCR.MODE = 0000_B$. Bit field $SCTRL.TRM = 01_B$ has to be programmed. The configuration of the input stages has to be done while $CCR.MODE = 0000_B$ to avoid unintended edges of the input signals and the ASC mode can be enabled by $CCR.MODE = 0010_B$ afterwards.
- **Pin connections:**
Establish a connection of input stage DX0 with the selected receive data input pin (signal DIN) with $DX0CR.INSW = 0$ and configure a transmit data output pin (signal DOUT). For collision or idle detection of the transmitter, the input stage DX1 has to be connected to the selected transmit output pin, also with $DX1CR.INSW = 0$. Additionally, program $DX2CR.INSW = 0$.
Due to the handling of the input data stream by the synchronous protocol handler, the propagation delay of the synchronization in the input stage has to be considered.
- **Bit timing configuration:**
The desired baud rate setting has to be selected, comprising the fractional divider, the baud rate generator and the bit timing. Please note that not all feature combinations can be supported by the application at the same time, e.g. due to propagation delays. For example, the length of a frame is limited by the frequency difference of the transmitter and the receiver device. Furthermore, in order to use the average of samples ($SMD = 1$), the sampling point has to be chosen to respect the signal settling and data propagation times.
- **Data format configuration:**
The word length, the frame length, and the shift direction have to be set up according to the application requirements by programming the registers $SCTRL$ and $SCTRH$. If required by the application, the data input and output signals can be inverted. Additionally, the parity mode has to be configured ($CCR.PM$).

21.3.3.1 Bit Timing

In ASC mode, each bit (incl. protocol bits) is divided into time quanta in order to provide granularity in the sub-bit range to adjust the sample point to the application requirements. The number of time quanta per bit is defined by bit fields BRGL.DCTQ and the length of a time quantum is given by BRGL.PCTQ.

In the example given in [Figure 21-28](#), one bit time is composed of 16 time quanta (BRGL.DCTQ = 15). It is not recommended to program less than 4 time quanta per bit time.

Bit field PCRL.SP determines the position of the sampling point for the bit value. The value of PCRL.SP must not be set to a value greater than BRGL.DCTQ. It is possible to sample the bit value only once per bit time or to take the average of samples. Depending on bit PCRL.SMD, either the current input value is directly sampled as bit value, or a majority decision over the input values sampled at the latest three time quanta is taken into account. The standard ASC bit timing consists of 16 time quanta with sampling after 8 or 9 time quanta with majority decision.

The bit timing setup (number of time quanta and the sampling point definition) is common for the transmitter and the receiver. Due to independent bit timing blocks, the receiver and the transmitter can be in different time quanta or bit positions inside their frames. The transmission of a frame is aligned to the time quanta generation.

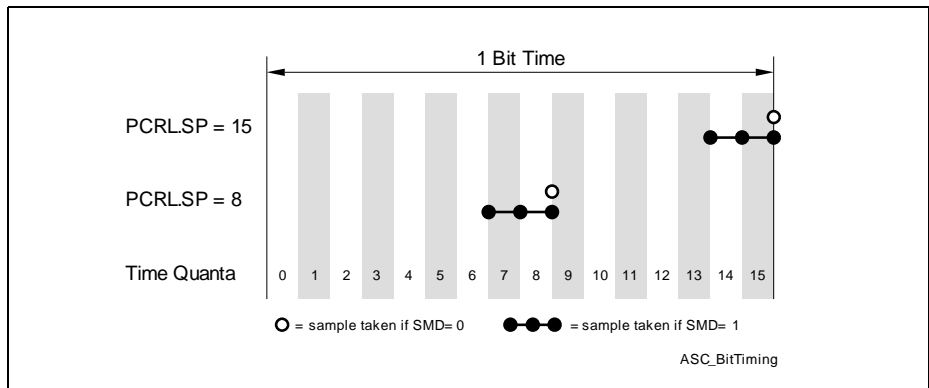


Figure 21-28 ASC Bit Timing

The sample point setting has to be adjusted carefully if collision or idle detection is enabled (via DX1 input signal), because the driver delay and some external delays have to be taken into account. The sample point for the transmit line has to be set to a value where the bit level is stable enough to be evaluated.

If the sample point is located late in the bit time, the signal itself has more time to become stable, but the robustness against differences in the clock frequency of transmitter and receiver decreases.

21.3.3.2 Baud Rate Generation

The baud rate f_{ASC} in ASC mode depends on the number of time quanta per bit time and their timing. The baud rate setting should only be changed while the transmitter and the receiver are idle. The bits in register BRGL define the baud rate setting:

- BRGL.CTQSEL
to define the input frequency f_{CTQIN} for the time quanta generation
- BRGL.PCTQ
to define the length of a time quantum (division of f_{CTQIN} by 1, 2, 3, or 4)
- BRGL.DCTQ
to define the number of time quanta per bit time

The standard setting is given by CTQSEL = 00_B ($f_{CTQIN} = f_{PDIV}$) and PPPEN = 0 ($f_{PPP} = f_{PIN}$). Under these conditions, the baud rate is given by:

$$f_{ASC} = f_{PIN} \times \frac{1}{PDIV + 1} \times \frac{1}{PCTQ + 1} \times \frac{1}{DCTQ + 1} \quad (21.6)$$

In order to generate slower frequencies, two additional divide-by-2 stages can be selected by CTQSEL = 10_B ($f_{CTQIN} = f_{SCLK}$) and PPPEN = 1 ($f_{PPP} = f_{MCLK}$), leading to:

$$f_{ASC} = \frac{f_{PIN}}{2 \times 2} \times \frac{1}{PDIV + 1} \times \frac{1}{PCTQ + 1} \times \frac{1}{DCTQ + 1} \quad (21.7)$$

21.3.3.3 Noise Detection

The ASC receiver permanently checks the data input line of the DX0 stage for noise (the check is independent from the setting of bit PCRL.SMD). Bit PSR.RNS (receiver noise) becomes set if the three input samples of the majority decision are not identical at the sample point for the bit value. The information about receiver noise gets accumulated over several bits in bit PSR.RNS (it has to be cleared by software) and can trigger a protocol interrupt each time noise is detected if enabled by PCRL.RNIEN.

21.3.3.4 Collision Detection

In some applications, such as data transfer over a single data line shared by several sending devices (see [Figure 21-26](#)), several transmitters have the possibility to send on the same data output line TXD. In order to avoid collisions of transmitters being active at the same time or to allow a kind of arbitration, a collision detection has been implemented.

The data value read at the TXD input at the DX1 stage and the transmitted data bit value are compared after the sampling of each bit value. If enabled by PCRL.CDEN = 1 and a bit sent is not equal to the bit read back, a collision is detected and bit PSR.COL is set. If enabled, bit PSR.COL = 1 disables the transmitter (the data output lines become 1)

and generates a protocol interrupt. The content of the transmit shift register is considered as invalid, so the transmit buffer has to be programmed again.

21.3.3.5 Pulse Shaping

For some applications, the 0 level of transmitted bits with the bit value 0 is not applied at the transmit output during the complete bit time. Instead of driving the original 0 level, only a 0 pulse is generated and the remaining time quanta of the bit time are driven with 1 level. The length of a bit time is not changed by the pulse shaping, only the signalling is changed.

In the standard ASC signalling scheme, the 0 level is signalled during the complete bit time with bit value 0 (ensured by programming $PCR.H.PL = 000_B$). In the case $PCR.H.PL > 000_B$, the transmit output signal becomes 0 for the number of time quanta defined by $PCR.H.PL$. In order to support correct reception with pulse shaping by the transmitter, the sample point has to be adjusted in the receiver according to the applied pulse length.

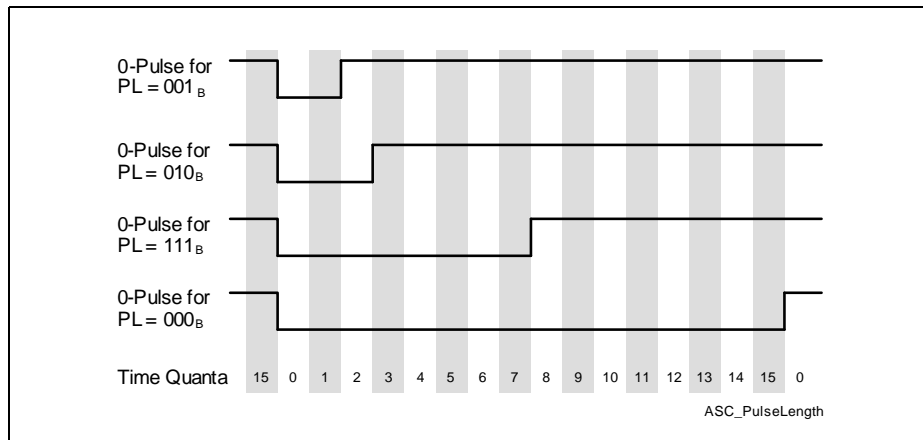


Figure 21-29 Transmitter Pulse Length Control

Figure 21-30 shows an example for the transmission of an 8-bit data word with LSB first and one stop bit (e.g. like for IrDA). The polarity of the transmit output signal has been inverted by $SCTRL.DOCFG = 01_B$.

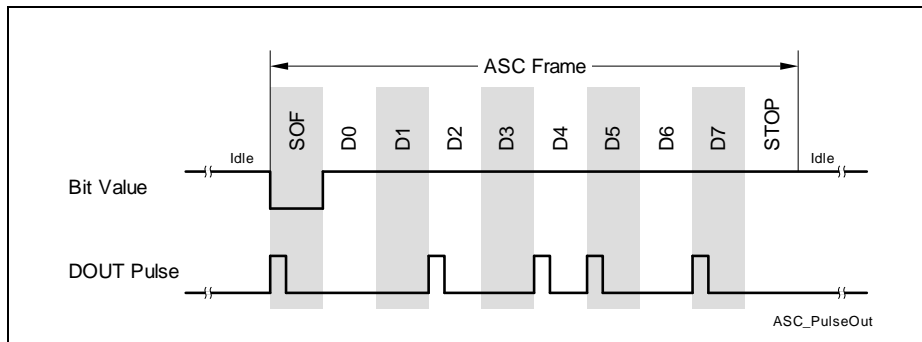


Figure 21-30 Pulse Output Example

21.3.3.6 Automatic Shadow Mechanism

The contents of the protocol control registers PCRL and PCRH, as well as bit field SCTR.H.FLE are internally kept constant while a data frame is transferred by an automatic shadow mechanism (shadowing takes place with each frame start). The registers can be programmed all the time with new settings that are taken into account for the next data frame. During a data frame, the applied (shadowed) setting is not changed, although new values have been written after the start of the data frame.

Bit fields SCTR.H.WLE and SCTR.L.SDIR are shadowed automatically with the start of each data word. As a result, a data frame can consist of data words with a different length. It is recommended to change SCTR.L.SDIR only when no data frame is running to avoid interference between hardware and software.

Please note that the starting point of a data word can be different for a transmitter and a receiver. In order to ensure correct handling, it is recommended to modify SCTR.H.WLE only while transmitter and receiver are both idle. If the transmitter and the receiver are referring to the same data signal (e.g. in a LIN bus system), SCTR.H.WLE can be modified while a data transfer is in progress after the RSI event has been detected.

21.3.3.7 End of Frame Control

The number of bits per ASC frame is defined by bit field SCTR.H.FLE. In order to support different frame length settings for consecutively transmitted frames, this bit field can be modified by hardware. The automatic update mechanism is enabled by TCSRL.FLEMD = 1 (in this case, bits TCSRL.WLEMD, SELMD, and WAMD have to be cleared).

If enabled, the transmit control information TCI automatically overwrites the bit field TCSRL.FLEMD when the ASC frame is started (leading to frames with 1 to 32 data bits). The TCI value represents the written address location of TBUFxx (without additional data

buffer) or INxx (with additional data buffer). With this mechanism, an ASC with 8 data bits is generated by writing a data word to TBUF07 (IN07, respectively).

21.3.3.8 Mode Control Behavior

In ASC mode, the following kernel modes are supported:

- Run Mode 0/1:
Behavior as programmed, no impact on data transfers.
- Stop Mode 0:
Bit PSR.TXIDLE is cleared. A new transmission is not started. A current transmission is finished normally. Bit PSR.RXIDLE is not modified. Reception is still possible. When leaving stop mode 0, bit TXIDLE is set according to PCR.IDM.
- Stop Mode 1:
Bit PSR.TXIDLE is cleared. A new transmission is not started. A current transmission is finished normally. Bit PSR.RXIDLE is cleared. A new reception is not possible. A current reception is finished normally. When leaving stop mode 1, bits TXIDLE and RXIDLE are set according to PCR.IDM.

21.3.3.9 Disabling ASC Mode

In order to switch off ASC mode without any data corruption, the receiver and the transmitter have to be both idle. This is ensured by requesting Stop Mode 1 in register KSCFG. After waiting for the end of the frame, the ASC mode can be disabled.

21.3.3.10 Protocol Interrupt Events

The following protocol-related events are generated in ASC mode and can lead to a protocol interrupt. The collision detection and the transmitter frame finished events are related to the transmitter, whereas the receiver events are given by the synchronization break detection, the receiver noise detection, the format error checks and the end of the received frame.

Please note that the bits in register PSR are not automatically cleared by hardware and have to be cleared by software in order to monitor new incoming events.

- Collision detection:
This interrupt indicates that the transmitted value (DOUT) does not match with the input value of the DX1 input stage at the sample point of a bit. For more details refer to [Page 21-116](#).
- Transmitter frame finished:
This interrupt indicates that the transmitter has completely finished a frame. Bit PSR.TFF becomes set at the end of the last stop bit. The DOUT signal assignment to port pins can be changed while no transmission is in progress.
- Receiver frame finished:
This interrupt indicates that the receiver has completely finished a frame. Bit

PSR.RFF becomes set at the end of the last stop bit. The DIN signal assignment to port pins can be changed while no reception is in progress.

- Synchronization break detection:
This interrupt can be used in LIN networks to indicate the reception of the synchronization break symbol (at the beginning of a LIN frame).
- Receiver noise detection:
This interrupt indicates that the input value at the sample point of a bit and at the two time quanta before are not identical.
- Format error:
The bit value of the stop bit(s) is defined as 1 level for the ASC protocol. A format error is signalled if the sampled bit value of a stop bit is 0.

21.3.3.11 Data Transfer Interrupt Handling

The data transfer interrupts indicate events related to ASC frame handling.

- Transmit buffer interrupt TBI:
Bit PSR.TBIF is set after the start of first data bit of a data word. This is the earliest point in time when a new data word can be written to TBUF.
With this event, bit TCSRL.TDV is cleared and new data can be loaded to the transmit buffer.
- Transmit shift interrupt TSI:
Bit PSR.TSIF is set after the start of the last data bit of a data word.
- Receiver start interrupt RSI:
Bit PSR.RSIF is set after the sample point of the first data bit of a data word.
- Receiver interrupt RI and alternative interrupt AI:
Bit PSR.RIF is set after the sampling point of the last data bit of a data word if this data word is not directly followed by a parity bit (parity generation disabled or not the last word of a data frame).
If the data word is directly followed by a parity bit (last data word of a data frame and parity generation enabled), bit PSR.RIF is set after the sampling point of the parity bit if no parity error has been detected. If a parity error has been detected, bit PSR.AIF is set instead of bit PSR.RIF.
The first data word of a data frame is indicated by RBUFSR.SOF = 1 for the received word.
Bit PSR.RIF is set for a receiver interrupt RI with WA = 0. Bit PSR.AIF is set for a alternative interrupt AI with WA = 1.

21.3.3.12 Protocol-Related Argument and Error

The protocol-related argument (RBUFSR.PAR) and the protocol-related error (RBUFSR.PERR) are two flags that are assigned to each received data word in the corresponding receiver buffer status registers.

In ASC mode, the received parity bit is monitored by the protocol-related argument and the result of the parity check by the protocol-related error indication (0 = received parity bit equal to calculated parity value). This information being elaborated only for the last received data word of each data frame, both bit positions are 0 for data words that are not the last data word of a data frame or if the parity generation is disabled.

21.3.3.13 Receive Buffer Handling

If a receive FIFO buffer is available (CCFG.RB = 1) and enabled for data handling (RBCTRH.SIZE > 0), it is recommended to set RBCTRH.RCIM = 11_B in ASC mode. This leads to an indication that the data word has been the first data word of a new data frame if bit OUTRH.RCI[0] = 1, a parity error is indicated by OUTRH.RCI[4] = 1, and the received parity bit value is given by OUTRH.RCI[3].

The standard receive buffer event and the alternative receive buffer event can be used for the following operations in RCI mode (RBCTRH.RNM = 1):

- A standard receive buffer event indicates that a data word can be read from OUTRL that has been received without parity error.
- An alternative receive buffer event indicates that a data word can be read from OUTRL that has been received with parity error.

21.3.3.14 Sync-Break Detection

The receiver permanently checks the DIN signal for a certain number of consecutive bit times with 0 level. The number is given by the number of programmed bits per frame (SCTRH.FLE) plus 2 (in the case without parity) or plus 3 (in the case with parity). If a 0 level is detected at a sample point of a bit after this event has been found, bit PSR.SBD is set and additionally, a protocol interrupt can be generated (if enabled by PCRL.SBD = 1). The counting restarts from 0 each time a falling edge is found at input DIN. This feature can be used for the detection of a synchronization break for slave devices in a LIN bus system (the master doesn't check for sync break).

For example, in a configuration for 8 data bits without parity generation, bit PCRL.SBD is set after at the next sample point at 0 level after 10 complete bit times have elapsed (representing the sample point of the 11th bit time since the first falling edge).

21.3.3.15 Transfer Status Indication

The receiver status can be monitored by flag PSR[9] = BUSY if bit PCRH.CTR[16] (receiver status enable RSTEN) is set. In this case, bit BUSY is set during a complete frame reception from the beginning of the start of frame bit to the end of the last stop bit.

Universal Serial Interface Channel

The transmitter status can be monitored by flag PSR[9] = BUSY if bit PCRH.CTR[17] (transmitter status enable TSTEN) is set. In this case, bit BUSY is set during a complete frame reception from the beginning of the start of frame bit to the end of the last stop bit. If both bits RSTEN and TSTEN are set, flag BUSY indicates the logical OR-combination of the receiver and the transmitter status. If both bits are cleared, flag BUSY is not modified depending on the transfer status (status changes are ignored).

21.3.4 ASC Protocol Registers

In ASC mode, the registers PCRH, PCRL and PSR handle ASC related information.

21.3.4.1 ASC Protocol Control Registers

In ASC mode, the PCRL/PCRH register bits or bit fields are defined as described in this section.

PCRL

Protocol Control Register L [ASC Mode]

(40_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PL			SP					FFI EN	FEI EN	RNI EN	CD EN	SBI EN	IDM	STP B	SMD
rw			rw					rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
SMD	0	rw	Sample Mode This bit field defines the sample mode of the ASC receiver. The selected data input signal can be sampled only once per bit time or three times (in consecutive time quanta). When sampling three times, the bit value shifted in the receiver shift register is given by a majority decision among the three sampled values. 0 _B Only one sample is taken per bit time. The current input value is sampled. 1 _B Three samples are taken per bit time and a majority decision is made.
STPB	1	rw	Stop Bits This bit defines the number of stop bits in an ASC frame. 0 _B The number of stop bits is 1. 1 _B The number of stop bits is 2.

Field	Bits	Type	Description
IDM	2	rw	Idle Detection Mode This bit defines if the idle detection is switched off or based on the frame length. 0 _B The bus idle detection is switched off and bits PSR.TXIDLE and PSR.RXIDLE are set automatically to enable data transfers without checking the inputs before. 1 _B The bus is considered as idle after a number of consecutive passive bit times defined by SCTRH.FLE plus 2 (in the case without parity bit) or plus 3 (in the case with parity bit).
SBIEN	3	rw	Synchronization Break Interrupt Enable This bit enables the generation of a protocol interrupt if a synchronization break is detected. The automatic detection is always active, so bit SBD can be set independently of SBIEN. 0 _B The interrupt generation is disabled. 1 _B The interrupt generation is enabled.
CDEN	4	rw	Collision Detection Enable This bit enables the reaction of a transmitter to the collision detection. 0 _B The collision detection is disabled. 1 _B If a collision is detected, the transmitter stops its data transmission, outputs a 1, sets bit PSR.COL and generates a protocol interrupt. In order to allow data transmission again, PSR.COL has to be cleared by software.
RNIEN	5	rw	Receiver Noise Detection Interrupt Enable This bit enables the generation of a protocol interrupt if receiver noise is detected. The automatic detection is always active, so bit PSR.RNS can be set independently of PCRL.RNIEN. 0 _B The interrupt generation is disabled. 1 _B The interrupt generation is enabled.

Field	Bits	Type	Description
FEIEN	6	rw	Format Error Interrupt Enable This bit enables the generation of a protocol interrupt if a format error is detected. The automatic detection is always active, so bits PSR.FER0/FER1 can be set independently of PCRL.FEIEN. 0 _B The interrupt generation is disabled. 1 _B The interrupt generation is enabled.
FFIEN	7	rw	Frame Finished Interrupt Enable This bit enables the generation of a protocol interrupt if the receiver or the transmitter reach the end of a frame. The automatic detection is always active, so bits PSR.RFF or PSR.TFF can be set independently of PCRL.FFIEN. 0 _B The interrupt generation is disabled. 1 _B The interrupt generation is enabled.
SP	[12:8]	rw	Sample Point This bit field defines the sample point of the bit value. The sample point must not be located outside the programmed bit timing ($PCRL.SP \leq BRGL.DCTQ$).
PL	[15:13]	rw	Pulse Length This bit field defines the length of a 0 data bit, counted in time quanta, starting with the time quantum 0 of each bit time. Each bit value that is a 0 can lead to a 0 pulse that is shorter than a bit time, e.g. for IrDA applications. The length of a bit time is not changed by PL, only the length of the 0 at the output signal. The pulse length must not be longer than the programmed bit timing ($PCRH.PL \leq BRGL.DCTQ$). This bit field is only taken into account by the transmitter and is ignored by the receiver. 000 _B The pulse length is equal to the bit length (no shortened 0). 001 _B The pulse length of a 0 bit is 2 time quanta. 010 _B The pulse length of a 0 bit is 3 time quanta. ... 111 _B The pulse length of a 0 bit is 8 time quanta.

PCRH

Protocol Control Register H [ASC Mode]

(42_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M							0							TST	RST
CLK														EN	EN
rw							r							rw	rw

Field	Bits	Type	Description
RSTEN	0	rw	Receiver Status Enable This bit enables the modification of flag PSR[9] = BUSY according to the receiver status. 0 _B Flag PSR[9] is not modified depending on the receiver status. 1 _B Flag PSR[9] is set during the complete reception of a frame.
TSTEN	1	rw	Transmitter Status Enable This bit enables the modification of flag PSR[9] = BUSY according to the transmitter status. 0 _B Flag PSR[9] is not modified depending on the transmitter status. 1 _B Flag PSR[9] is set during the complete transmission of a frame.
0	[14:2]	r	Reserved Returns 0 if read; not modified in ASC mode.
MCLK	15	rw	Master Clock Enable This bit enables the generation of the master clock MCLK. 0 _B The MCLK generation is disabled and the MCLK signal is 0. 1 _B The MCLK generation is enabled.

21.3.4.2 ASC Protocol Status Register

In ASC mode, the PSR register bits or bit fields are defined as described in this section. The bits and bit fields in register PSR are not cleared by hardware.

The flags in the PSR register can be cleared by writing a 1 to the corresponding bit position in register PSCR. Writing a 1 to a bit position in PSR sets the corresponding flag, but doesn't lead to further actions (no interrupt generation). Writing a 0 has no effect. The PSR flags should be cleared by software before enabling a new protocol.

PSR

Protocol Status Register [ASC Mode] (44_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AIF	RIF	TBIF	TSIF	DLIF	RSIF	BU SY	TFF	RFF	FER 1	FER 0	RNS	COL	SBD	RX IDLE	TX IDLE
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
TXIDLE	0	rwh	Transmission Idle This bit shows if the transmit line (DX1) has been idle. A frame transmission can only be started if TXIDLE is set. 0 _B The transmitter line has not yet been idle. 1 _B The transmitter line has been idle and frame transmission is possible.
RXIDLE	1	rwh	Reception Idle This bit shows if the receive line (DX0) has been idle. A frame reception can only be started if RXIDLE is set. 0 _B The receiver line has not yet been idle. 1 _B The receiver line has been idle and frame reception is possible.
SBD	2	rwh	Synchronization Break Detected¹⁾ This bit is set if a programmed number of consecutive bit values with level 0 has been detected (called synchronization break, e.g. in a LIN bus system). 0 _B A synchronization break has not yet been detected. 1 _B A synchronization break has been detected.

Field	Bits	Type	Description
COL	3	rwh	Collision Detected¹⁾ This bit is set if a collision has been detected (with PCRL.CDEN = 1). 0 _B A collision has not yet been detected and frame transmission is possible. 1 _B A collision has been detected and frame transmission is not possible.
RNS	4	rwh	Receiver Noise Detected¹⁾ This bit is set if receiver noise has been detected. 0 _B Receiver noise has not been detected. 1 _B Receiver noise has been detected.
FER0	5	rwh	Format Error in Stop Bit 0¹⁾ This bit is set if a 0 has been sampled in the stop bit 0 (called format error 0). 0 _B A format error 0 has not been detected. 1 _B A format error 0 has been detected.
FER1	6	rwh	Format Error in Stop Bit 1¹⁾ This bit is set if a 0 has been sampled in the stop bit 1 (called format error 1). 0 _B A format error 1 has not been detected. 1 _B A format error 1 has been detected.
RFF	7	rwh	Receive Frame Finished¹⁾ This bit is set if the receiver has finished the last stop bit. 0 _B The received frame is not yet finished. 1 _B The received frame is finished.
TFF	8	rwh	Transmitter Frame Finished¹⁾ This bit is set if the transmitter has finished the last stop bit. 0 _B The transmitter frame is not yet finished. 1 _B The transmitter frame is finished.
BUSY	9	r	Transfer Status BUSY This bit indicates the receiver status (if PCRH.RSTEN = 1) or the transmitter status (if PCRH.TSTEN = 1) or the logical OR combination of both (if PCRH.RSTEN = PCRH.TSTEN = 1). 0 _B A data transfer does not take place. 1 _B A data transfer currently takes place.
RSIF	10	rwh	Receiver Start Indication Flag 0 _B A receiver start event has not occurred. 1 _B A receiver start event has occurred.

Field	Bits	Type	Description
DLIF	11	rwh	Data Lost Indication Flag 0 _B A data lost event has not occurred. 1 _B A data lost event has occurred.
TSIF	12	rwh	Transmit Shift Indication Flag 0 _B A transmit shift event has not occurred. 1 _B A transmit shift event has occurred.
TBIF	13	rwh	Transmit Buffer Indication Flag 0 _B A transmit buffer event has not occurred. 1 _B A transmit buffer event has occurred.
RIF	14	rwh	Receive Indication Flag 0 _B A receive event has not occurred. 1 _B A receive event has occurred.
AIF	15	rwh	Alternative Receive Indication Flag 0 _B An alternative receive event has not occurred. 1 _B An alternative receive event has occurred.

1) This status bit can generate a protocol interrupt (see [Page 21-24](#)). The general interrupt status flags are described in the general interrupt chapter.

21.3.5 Hardware LIN Support

In order to support the LIN protocol, bit TCSRL.FLEMD = 1 should be set for the master. For slave devices, it can be cleared and the fixed number of 8 data bits has to be set (SCTRH.FLE = 7_H). For both, master and slave devices, the parity generation has to be switched off (CCR.PM = 00_B) and transfers take place with LSB first (SCTRL.SDIR = 0) and 1 stop bit (PCRL.STPB = 0).

The Local Interconnect Network (LIN) data exchange protocol contains several symbols that can all be handled in ASC mode. Each single LIN symbol represents a complete ASC frame. The LIN bus is a master-slave bus system with a single master and multiple slaves (for the exact definition please refer to the official LIN specification).

A complete LIN frame contains the following symbols:

- Synchronization break:

The master sends a synchronization break to signal the beginning of a new frame. It contains at least 13 consecutive bit times at 0 level, followed by at least one bit time at 1 level (corresponding to 1 stop bit). Therefore, TBUF11 (or IN11) has to be written with 0 (leading to a frame with SOF followed by 12 data bits at 0 level).

A slave device shall detect 11 consecutive bit times at 0 level, which done by the synchronization break detection. Bit PSR.SBD is set if such an event is detected and a protocol interrupt can be generated. Additionally, the received data value of 0 appears in the receive buffer and a format error is signaled.

Universal Serial Interface Channel

If the baud rate of the slave has to be adapted to the master, the baud rate measurement has to be enabled for falling edges by setting $BRGL.TMEN = 1$, $DX0CR.CM = 10_H$ and $DX1CR.CM = 00_H$ before the next symbol starts.

- Synchronization byte:

The master sends this symbol after writing the data value 55_H to TBUF07 (or IN07). A slave device can either receive this symbol without any further action (and can discard it) or it can use the falling edges for baud rate measurement. Bit $PSR.TSIF = 1$ (with optionally the corresponding interrupt) indicates the detection of a falling edge and the capturing of the elapsed time since the last falling edge in $BRGH.PDIV$. Valid captured values can be read out after the second, third, fourth and fifth activation of $TSIF$. After the fifth activation of $TSIF$ within this symbol, the baud rate detection has to be disabled ($BRGL.TMEN = 0$) and $BRGH.PDIV$ can be programmed with the formerly captured value divided by twice the number of time quanta per bit (assuming $BRGL.PCTQ = 00_B$).

In order to avoid a $PDIV$ overflow during baud rate measurement, the prescaler settings of the fractional divider must be set in a way that leads to a target value of $PDIV$ well below $1024 / (2 * \text{number of time quanta per bit time})$. As this procedure leads to low $PDIV$ target values, the baud rate measurement accuracy becomes limited. Therefore, the following procedure is recommended:

- Slowing down the fractional divider for baud rate measurement by $2 * \text{number of time quanta per bit time}$.
- Writing the current value of $FDRL.DM$ again to restart the fraction divider.
- Switching-on the baud rate measurement by writing $BRGL.TMEN = 1$ (note that the synchronization break detection is not possible when baud rate measurement is enabled).
- Restoring the fractional divider to its original settings.
- Switching-off the baud rate measurement by writing $BRGL.TMEN = 0$.
- The measurement result in $BRGH.PDIV$ can now be directly used as baud rate setting.

- Other symbols:

The other symbols of a LIN frame can be handled with ASC data frames without specific actions.

If LIN frames should be sent out on a frame base by the LIN master, the input $DX2$ can be connected to external timers to trigger the transmit actions (e.g. the synchronization break symbol has been prepared but is started if a trigger occurs). Please note that during the baud rate measurement of the ASC receiver, no transmission can take place by the ASC transmitter of the same USIC channel.

21.4 Synchronous Serial Channel (SSC)

The synchronous serial channel SSC covers the data transfer function of an SPI-like module. It can handle reception and transmission of synchronous data frames between a device operating in master mode and at least one device in slave mode. The SSC mode is selected by $CCR.MODE = 0001_B$ with $CCFG.SSC = 1$ (SSC mode is available).

This chapter contains the following sections:

- Signal description (see [Page 21-131](#))
- General SSC issues (see [Page 21-139](#))
- Master mode operation (see [Page 21-143](#))
- Slave mode operation (see [Page 21-150](#))
- Protocol registers (see [Page 21-152](#))
- Timing considerations (see [Page 21-158](#))

21.4.1 Signal Description

A synchronous SSC data transfer is characterized by a simultaneous transfer of a shift clock signal together with the transmit and/or receive data signal(s) to determine when the data is valid (definition of transmit and sample point).

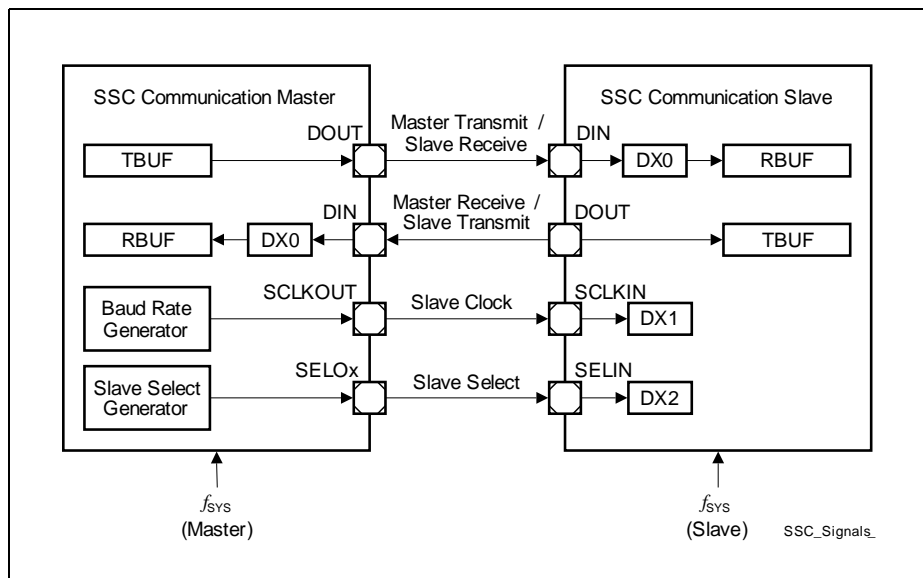


Figure 21-31 SSC Signals for Full-Duplex Communication

In order to explicitly indicate the start and the end of a data transfer and to address more than one slave devices individually, the SSC module supports the handling of slave

Universal Serial Interface Channel

select signals. They are optional and are not necessarily needed for SSC data transfers. The SSC module supports up to 8 different slave select output signals for master mode operation (named SELO_x, with x = 0-7) and 1 slave select input SELIN for slave mode. In most applications, the slave select signals are active low.

A device operating in master mode controls the start and end of a data frame, as well as the generation of the shift clock and slave select signals. This comprises the baud rate setting for the shift clock and the delays between the shift clock and the slave select output signals. If several SSC modules are connected together, there can be only one SSC master at a time, but several slaves. Slave devices receive the shift clock and optionally a slave select signal(s). For the programming of the input stages DX0, DX1, and DX2 please refer to [Page 21-36](#).

Table 21-8 SSC Communication Signals

SSC Mode	Receive Data	Transmit Data	Shift Clock	Slave Select(s)
Master	MRST ¹⁾ , input DIN, handled by DX0	MTSR ²⁾ , Output DOUT	Output SCLKOUT	Output(s) SELO _x
Slave	MTSR, input DIN, handled by DX0	MRST, Output DOUT	Input SCLKIN, handled by DX1	input SELIN, handled by DX2

1) MRST = master receive slave transmit, also known as MISO = master in slave out

2) MTSR = master transmit slave receive, also known as MOSI = master out slave in

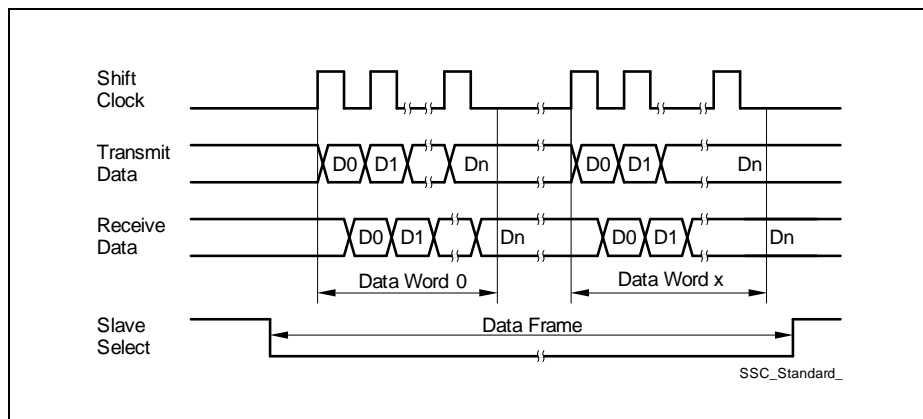


Figure 21-32 4-Wire SSC Standard Communication Signals

21.4.1.1 Transmit and Receive Data Signals

In half-duplex mode, a single data line is used, either for data transfer from the master to a slave or from a slave to the master. In this case, MRST and MTSR are connected together, one signal as input, the other one as output, depending on the data direction. The user software has to take care about the data direction to avoid data collision (e.g. by preparing dummy data of all 1s for transmission in case of a wired AND connection with open-drain drivers or by enabling/disabling push/pull output drivers). In full-duplex mode, data transfers take place in parallel between the master device and a slave device via two independent data signals MTSR and MRST, as shown in [Figure 21-31](#).

The receive data input signal DIN is handled by the input stage DX0. In master mode (referring to MRST) as well as in slave mode (referring to MTSR), the data input signal DIN is taken from an input pin. The signal polarity of DOUT (data output) with respect to the data bit value can be configured in block DOCFG (data output configuration) by bit field SCTRL.DOCFG.

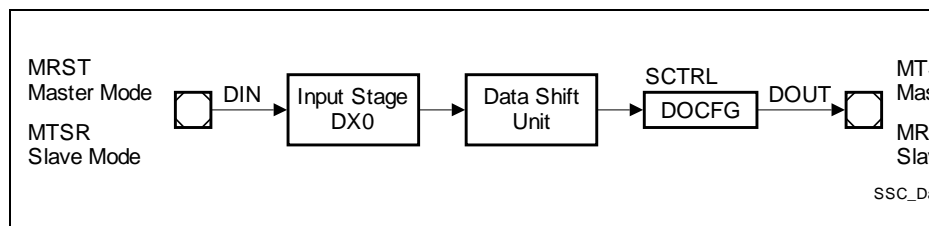


Figure 21-33 SSC Data Signals

21.4.1.2 Shift Clock Signals

The shift clock signal is handled by the input stage DX1. In slave mode, the signal SCLKIN is received from an external master, so the DX1 stage has to be connected to an input pin. The input stage can invert the received input signal to adapt to the polarity of SCLKIN to the function of the data shift unit (data transmission on rising edges, data reception on falling edges).

In master mode, the shift clock is generated by the internal baud rate generator. The output signal SCLK of the baud rate generator is taken as shift clock input for the data shift unit. The internal signal SCLK is made available for external slave devices by signal SCLKOUT.

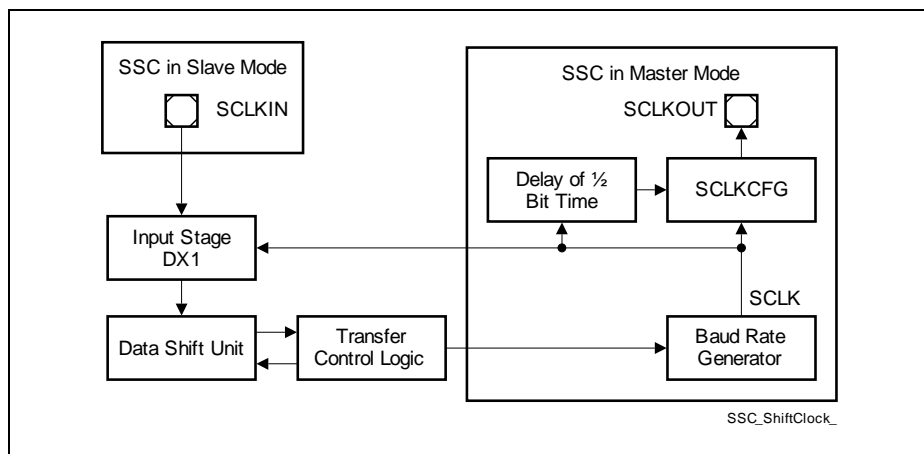


Figure 21-34 SSC Shift Clock Signals

Due to the multitude of different SSC applications, in master mode, there are different ways to configure the shift clock output signal SCLKOUT with respect to SCLK. This is done in the block SCLKCFG (shift clock configuration) by bit field BRGH.SCLKCFG, allowing 4 possible settings, as shown in [Figure 21-35](#).

- No delay, no polarity inversion (SCLKCFG = 00_B, SCLKOUT equals SCLK):
 The inactive level of SCLKOUT is 0, while no data frame is transferred. The first data bit of a new data frame is transmitted with the first rising edge of SCLKOUT and the first data bit is received in with the first falling edge of SCLKOUT. The last data bit of a data frame is transmitted with the last rising clock edge of SCLKOUT and the last data bit is received in with the last falling edge of SCLKOUT. This setting can be used in master and in slave mode. It corresponds to the behavior of the internal data shift unit.
- No delay, polarity inversion (SCLKCFG = 01_B):
 The inactive level of SCLKOUT is 1, while no data frame is transferred. The first data

Universal Serial Interface Channel

bit of a new data frame is transmitted with the first falling clock edge of SCLKOUT and the first data bit is received with the first rising edge of SCLKOUT. The last data bit of a data frame is transmitted with the last falling edge of SCLKOUT and the last data bit is received with the last rising edge of SCLKOUT. This setting can be used in master and in slave mode.

- SCLKOUT is delayed by 1/2 shift clock period, no polarity inversion (SCLKCFG = 10_B):

The inactive level of SCLKOUT is 0, while no data frame is transferred.

The first data bit of a new data frame is transmitted 1/2 shift clock period before the first rising clock edge of SCLKOUT. Due to the delay, the next data bits seem to be transmitted with the falling edges of SCLKOUT. The last data bit of a data frame is transmitted 1/2 period of SCLKOUT before the last rising clock edge of SCLKOUT. The first data bit is received 1/2 shift clock period before the first falling edge of SCLKOUT. Due to the delay, the next data bits seem to be received with the rising edges of SCLKOUT. The last data bit is received 1/2 period of SCLKOUT before the last falling clock edge of SCLKOUT.

This setting can be used only in master mode and not in slave mode (the connected slave has to provide the first data bit before the first SCLKOUT edge, e.g. as soon as it is addressed by its slave select).

- SCLKOUT is delayed by 1/2 shift clock period, polarity inversion (SCLKCFG = 11_B):

The inactive level of SCLKOUT is 1, while no data frame is transferred.

The first data bit of a new data frame is transmitted 1/2 shift clock period before the first falling clock edge of SCLKOUT. Due to the delay, the next data bits seem to be transmitted with the rising edges of SCLKOUT. The last data bit of a data frame is transmitted 1/2 period of SCLKOUT before the last falling clock edge of SCLKOUT. The first data bit is received 1/2 shift clock period before the first rising edge of SCLKOUT. Due to the delay, the next data bits seem to be received with the falling edges of SCLKOUT. The last data bit is received 1/2 period of SCLKOUT before the last rising clock edge of SCLKOUT.

This setting can be used only in master mode and not in slave mode (the connected slave has to provide the first data bit before the first SCLKOUT edge, e.g. as soon as it is addressed by its slave select).

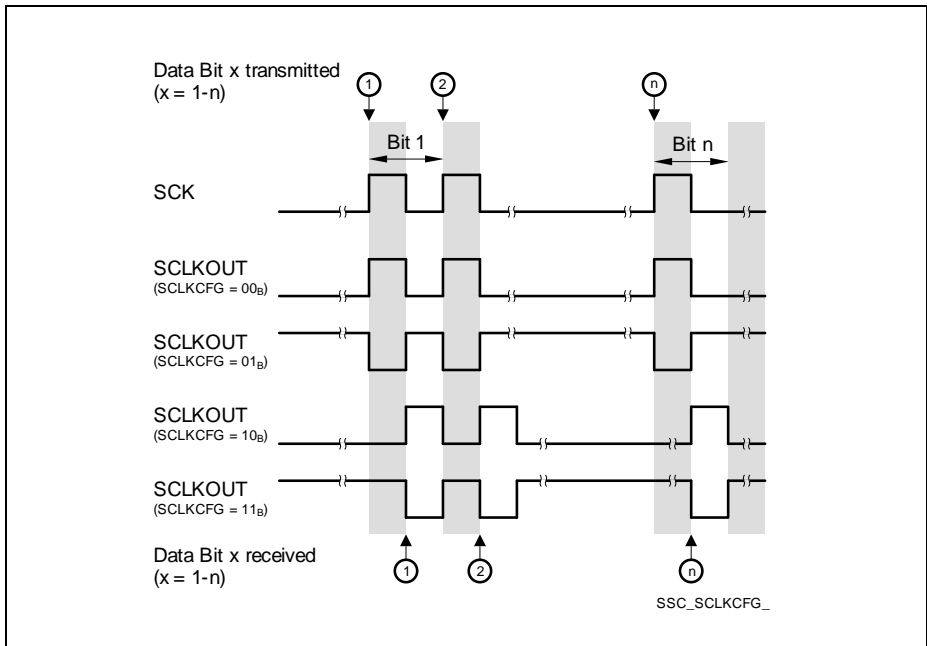


Figure 21-35 SCLKOUT Configuration in SSC Master Mode

Note: If a configuration with delay is selected and a slave select line is used, the slave select delays have to be set up accordingly.

21.4.1.3 Slave Select Signals

The slave select signal is handled by the input stage DX2. In slave mode, the input signal SELIN is received from an external master via an input pin. The input stage can invert the received input signal to adapt the polarity of signal SELIN to the function of the data shift unit (the module internal signals are considered as high active, so a data transfer is only possible while the slave select input of the data shift unit is at 1-level, otherwise, shift clock pulses are ignored and do not lead to data transfers). If an input signal SELIN is low active, it should be inverted in the DX2 input stage.

In master mode, a master slave select signal MSLS is generated by the internal slave select generator. In order to address different external slave devices independently, the internal MSLS signal is made available externally via up to 8 SELOx output signals that can be configured by the block SELCFG (select configuration).

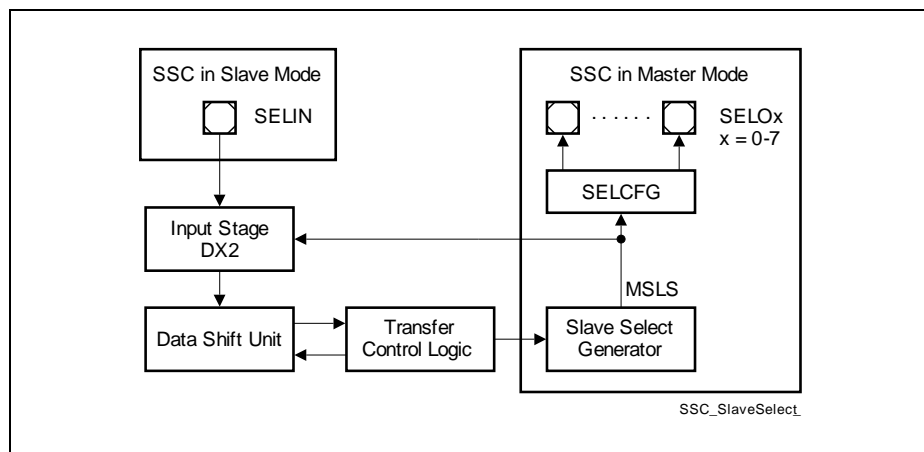


Figure 21-36 SSC Slave Select Signals

The control of the SELCFG block is based on protocol specific bits and bit fields in the protocol control register parts PCRL and PCRH. For the generation of the MSLS signal please refer to [Section 21.4.3.2](#).

- PCRL.SELCTR to choose between direct and coded select mode
- PCRL.SELINV to invert the SELOx outputs
- PCRH.SELO[7:0] as individual value for each SELOx line

The SELCFG block supports the following configurations of the SELOx output signals:

- Direct Select Mode (SELCTR = 1):
 Each SELOx line (with $x = 0-7$) can be directly connected to an external slave device. If bit x in bit field SELO is 0, the SELOx output is permanently inactive. A SELOx output becomes active while the internal signal MSLS is active (see

Section 21.4.3.2) and bit x in bit field SELO is 1. Several external slave devices can be addressed in parallel if more than one bit in bit field SELO are set during a data frame. The number of external slave devices that can be addressed individually is limited to the number of available SELOx outputs.

- Coded Select Mode (SELCTR = 0):
The SELOx lines (with x = 1-7) can be used as addresses for an external address decoder to increase the number of external slave devices. These lines only change with the start of a new data frame and have no other relation to MSLS. Signal SELO0 can be used as enable signal for the external address decoder. It is active while MSLS is active (during a data frame) and bit 0 in bit field SELO is 1. Furthermore, in coded select mode, this output line is delayed by one cycle of f_{SYS} compared to MSLS to allow the other SELOx lines to stabilize before enabling the address decoder.

21.4.2 Operating the SSC

This chapter contains SSC issues, that are of general interest and not directly linked to either master mode or slave mode.

21.4.2.1 Automatic Shadow Mechanism

The contents of the baud rate control registers BRGL and BRGH, bit field SCTR.H.FLE as well as the protocol control registers PCRL and PCRH are internally kept constant while a data frame is transferred (= while MSLS is active) by an automatic shadow mechanism. The registers can be programmed all the time with new settings that are taken into account for the next data frame. During a data frame, the applied (shadowed) setting is not changed, although new values have been written after the start of the data frame.

Bit fields SCTR.H.WLE and SCTRL.SDIR are shadowed automatically with the start of each data word. As a result, a data frame can consist of data words with a different length. It is recommended to change SCTRL.SDIR only when no data frame is running to avoid interference between hardware and software.

Please note that the starting point of a data word are different for a transmitter (first bit transmitted) and a receiver (first bit received). In order to ensure correct handling, it is recommended to refer to the receive start interrupt RSI before modifying SCTRL.WLE. If TCSRL.WLEMD = 1, it is recommended to update TCSRL and TBUFxx after the receiver start interrupt has been generated.

21.4.2.2 Mode Control Behavior

In SSC mode, the following kernel modes are supported:

- Run Mode 0/1:
Behavior as programmed, no impact on data transfers.
- Stop Mode 0/1:
The content of the transmit buffer is considered as not valid for transmission. Although being considered as 0, bit TCSRL.TDV it is not modified by the stop mode condition.
In master mode, a currently running word transfer is finished normally, but no new data word is started (the stop condition is not considered as end-of-frame condition). In slave mode, a currently running word transfer is finished normally. Passive data will be sent out instead of a valid data word if a data word transfer is started by the external master while the slave device is in stop mode. In order to avoid passive slave transmit data, it is recommended not to program stop mode for an SSC slave device if the master device does not respect the slave device's stop mode.

21.4.2.3 Disabling SSC Mode

In order to disable SSC mode without any data corruption, the receiver and the transmitter have to be both idle. This is ensured by requesting Stop Mode 1 in register KSCFG. After Stop Mode 1 has been acknowledged by KSCFG.2 = 1, the SSC mode can be disabled.

21.4.2.4 Data Frame Control

An SSC data frame can consist of several consecutive data words that may be separated by an inter-word delay. Without inter-word delay, the data words seem to form a longer data word, being equivalent to a data frame. The length of the data words are most commonly identical within a data frame, but may also differ from one word to another. The data word length information (defined by SCTRH.WLE) is evaluated for each new data word, whereas the frame length information (defined by SCTRH.FLE) is evaluated at the beginning at each start of a new frame.

The length of an SSC data frame can be defined in two different ways:

- By the number of bits per frame:
If the number of bits per data frame is defined (frame length FLE), a slave select signal is not necessarily required to indicate the start and the end of a data frame.
If the programmed number of bits per frame is reached within a data word, the frame is considered as finished and remaining data bits in the last data word are ignored and are not transferred.
This method can be applied for data frames with up to 63 data bits.
- By the slave select signal:
If the number of bits per data frame is not known, the start/end information of a data frame is given by a slave select signal. If a deactivation of the slave select signal is detected within a data word, the frame is considered as finished and remaining data bits in the last data word are ignored and are not transferred.
This method has to be applied for frames with more than 63 data bits (programming limit of FLE). The advantage of slave select signals is the clearly defined start and end condition of data frames in a data stream. Furthermore, slave select signals allow to address slave devices individually.

21.4.2.5 Parity Mode

Parity generation is not supported in SSC mode and bit field CCR.PM = 00_B has to be programmed.

21.4.2.6 Transfer Mode

In SSC mode, bit field SCTRL.TRM = 01_B has to be programmed to allow data transfers. Setting SCTRL.TRM = 00_B disables and stops the data transfer immediately.

21.4.2.7 Data Transfer Interrupt Handling

The data transfer interrupts indicate events related to SSC frame handling.

- **Transmit buffer interrupt TBI:**
Bit PSR.TBIF is set after the start of first data bit of a data word.
- **Transmit shift interrupt TSI:**
Bit PSR.TSIF is set after the start of the last data bit of a data word.
- **Receiver start interrupt RSI:**
Bit PSR.RSIF is set after the reception of the first data bit of a data word.
With this event, bit TCSRL.TDV is cleared and new data can be loaded to the transmit buffer.
- **Receiver interrupt RI:**
The reception of the second, third, and all subsequent words in a multi-word frame is always indicated by RBUFSSR.SOF = 0. Bit PSR.RIF is set after the reception of the last data bit of a data word if RBUFSSR.SOF = 0.
Bit RBUFSSR.SOF indicates whether the received data word has been the first data word of a multi-word frame or some subsequent word. In SSC mode, it decides if alternative interrupt or receive interrupt is generated.
- **Alternative interrupt AI:**
The reception of the first word in a frame is always indicated by RBUFSSR.SOF = 1. This is true both in case of reception of multi-word frames and single-word frames. In SSC mode, this results in setting PSR.AIF.

21.4.2.8 Protocol-Related Argument and Error

The protocol-related argument (RBUFSSR.PAR) and the protocol-related error (RBUFSSR.PERR) are two flags that are assigned to each received data word in the corresponding receiver buffer status registers.

In SSC mode, these flags are always 0 (parity handling must be disabled). The received start of frame indication is monitored by the protocol-related error indication (0 = received word is not the first word of a frame, 1 = received word is the first word of a new frame).

21.4.2.9 Receive Buffer Handling

If a receive FIFO buffer is available (CCFG.RB = 1) and enabled for data handling (RBCTRH.SIZE > 0), it is recommended to set RBCTRH.RCIM = 01_B in SSC mode. This leads to an indication that the data word has been the first data word of a new data frame if bit OUTRH.RCI[4] = 1, and the word length of the received data is given by OUTRH.RCI[3:0].

The standard receive buffer event and the alternative receive buffer event can be used for the following operation in RCI mode (RBCTRH.RNM = 1):

Universal Serial Interface Channel

- A standard receive buffer event indicates that a data word can be read from OUTRL that has not been the first word of a data frame.
- An alternative receive buffer event indicates that the first data word of a new data frame can be read from OUTRL.

21.4.3 Operating the SSC in Master Mode

In order to operate the SSC in master mode, the following issues have to be considered:

- **Select SSC mode:**
It is recommended to configure all parameters of the SSC that do not change during run time while $CCR.MODE = 0000_B$. Bit field $SCTRL.TRM = 01_B$ has to be programmed. The configuration of the input stages has to be done while $CCR.MODE = 0000_B$ to avoid unintended edges of the input signals and the SSC mode can be enabled by $CCR.MODE = 0001_B$ afterwards.
- **Pin connections:**
Establish a connection of input stage DX0 with the selected receive data input pin (DIN) with $DX0CR.INSW = 1$ and configure a transmit data output pin (DOUT).
- **Baud rate generation:**
The desired baud rate setting has to be selected, comprising the fractional divider and the baud rate generator. Bit $DX1CR.INSW = 0$ has to be programmed to use the baud rate generator output SCLK directly as input for the data shift unit. Configure a shift clock output pin (signal SCLKOUT).
- **Slave select generation:**
The slave select delay generation has to be enabled by setting $PCRL.MSLSEN = 1$ and the programming of the time quanta counter setting. Bit $DX2CR.INSW = 0$ has to be programmed to use the slave select generator output MSLS as input for the data shift unit. Configure slave select output pins (signals SELOx) if needed.
- **Data format configuration:**
The word length, the frame length, and the shift direction have to be set up according to the application requirements by programming the registers SCTRL and SCTR.H.

Note: The USIC can only receive in master mode if it is transmitting, because the master frame handling refers to bit TDV of the transmitter part.

21.4.3.1 Baud Rate Generation

The baud rate (determining the length of one data bit) of the SSC is defined by the frequency of the SCLK signal (one period of f_{SCLK} represents one data bit). The SSC baud rate generation does not imply any time quanta counter.

In a standard SSC application, the phase relation between the optional MCLK output signal and SCLK is not relevant and can be disabled ($BRGL.PPPEN = 0$). In this case, the SCLK signal directly derives from the protocol input frequency f_{PIN} . In the exceptional case that a fixed phase relation between the MCLK signal and SCLK is required (e.g. when using MCLK as clock reference for external devices), the additional divider by 2 stage has to be taken into account ($BRGL.PPPEN = 1$).

The adjustable divider factor is defined by bit field BRGH.PDIV.

$$f_{\text{SCLK}} = \frac{f_{\text{PIN}}}{2} \times \frac{1}{\text{PDIV} + 1} \quad \text{if } \text{PPPEN} = 0$$

$$f_{\text{SCLK}} = \frac{f_{\text{PIN}}}{2 \times 2} \times \frac{1}{\text{PDIV} + 1} \quad \text{if } \text{PPPEN} = 1$$
(21.8)

21.4.3.2 MSLS Generation

The slave select signals indicate the start and the end of a data frame and are also used by the communication master to individually select the desired slave device. A slave select output of the communication master becomes active a programmable time before a data part of the frame is started (leading delay T_{ld}), necessary to prepare the slave device for the following communication. After the transfer of a data part of the frame, it becomes inactive again a programmable time after the end of the last bit (trailing delay T_{td}) to respect the slave hold time requirements. If data frames are transferred back-to-back one after the other, the minimum time between the deactivation of the slave select and the next activation of a slave select is programmable (next-frame delay T_{nf}). If a data frame consists of more than one data word, an optional delay between the data words can also be programmed (inter-word delay T_{iw}).

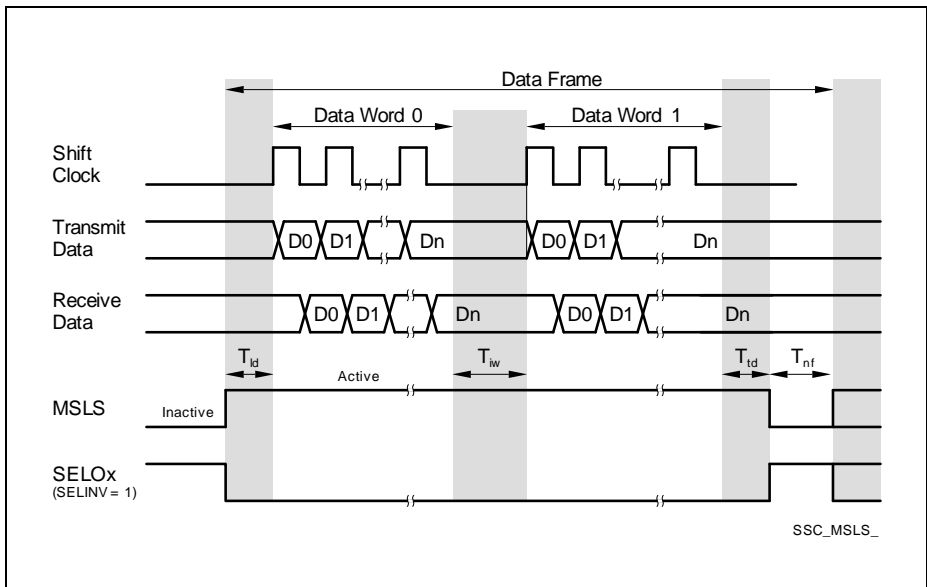


Figure 21-37 MSLS Generation in SSC Master Mode

In SSC master mode, the slave select delays are defined as follows:

- Leading delay T_{ld} :
The leading delay starts if valid data is available for transmission. The internal signal MSLS becomes active with the start of the leading delay. The first shift clock edge (rising edge) of SCLK is generated by the baud rate generator after the leading delay has elapsed.
- Trailing delay T_{td} :
The trailing delay starts at the end of the last SCLK cycle of a data frame. The internal signal MSLS becomes inactive with the end of the trailing delay.
- Inter-word delay T_{iw} :
This delay is optional and can be enabled/disabled by PCRH.TIWEN. If the inter-word delay is disabled (TIWEN = 0), the last data bit of a data word is directly followed by the first data bit of the next data word of the same data frame. If enabled (TIWEN = 1), the inter-word delay starts at the end of the last SCLK cycle of a data word. The first SCLK cycle of the following data word of the same data frame is started when the inter-word delay has elapsed. During this time, no shift clock pulses are generated and signal MSLS stays active. The communication partner has time to “digest” the previous data word or to prepare for the next one.
- Next-frame delay T_{nf} :
The next-frame delay starts at the end of the trailing delay. During this time, no shift clock pulses are generated and signal MSLS stays inactive. A frame is considered as finished after the next-frame delay has elapsed.

21.4.3.3 Automatic Slave Select Update

If the number of bits per SSC frame and the word length are defined by bit fields SCTRH.FLE and SCTRH.WLE, the transmit control information TCI can be used to update the slave select setting PCRH.CTR[23:16] to control the SELOx select outputs. The automatic update mechanism is enabled by TCSRL.SELMD = 1 (bits TCSRL.WLEMD, FLEMD, and WAMD have to be cleared). In this case, the TCI of the first data word of a frame defines the slave select setting of the complete frame due to the automatic shadow mechanism (see [Page 21-118](#)).

21.4.3.4 Slave Select Delay Generation

The slave select delay generation is based on time quanta. The length of a time quantum (defined by the period of the f_{CTQIN}) and the number of time quanta per delay can be programmed.

In standard SSC applications, the leading delay T_{ld} and the trailing delay T_{td} are mainly used to ensure stability on the input and output lines as well as to respect setup and hold times of the input stages. These two delays have the same length (in most cases shorter than a bit time) and can be programmed with the same set of bit fields.

- **BRGL.CTQSEL**
to define the input frequency f_{CTQIN} for the time quanta generation for T_{ld} and T_{td}
- **BRGL.PCTQ**
to define the length of a time quantum (division of f_{CTQIN} by 1, 2, 3, or 4) for T_{ld} and T_{td}
- **BRGL.DCTQ**
to define the number of time quanta for the delay generation for T_{ld} and T_{td}

The inter-word delay T_{iw} and the next-frame delay T_{nf} are used to handle received data or to prepare data for the next word or frame. These two delays have the same length (in most cases in the bit time range) and can be programmed with a second, independent set of bit fields.

- **PCRL.CTQSEL1**
to define the input frequency f_{CTQIN} for the time quanta generation for T_{nf} and T_{iw}
- **PCRL.PCTQ1**
to define the length of a time quantum (division of f_{CTQIN} by 1, 2, 3, or 4) for T_{nf} and T_{iw}
- **PCRL.DCTQ1**
to define the number of time quanta for the delay generation for T_{nf} and T_{iw}
- **PCRH.TIWEN**
to enable/disable the inter-word delay T_{iw}

Each delay depends on the length of a time quantum and the programmed number of time quanta given by the bit fields CTQSEL/CTQSEL1, PCTQ/DCTQ and PCTQ1/DCTQ1 (the coding of CTQSEL1 is similar to CTQSEL, etc.). To provide a high flexibility in programming the delay length, the input frequencies can be selected between several possibilities (e.g. based on bit times or on the faster inputs of the protocol-related divider). The delay times are defined as follows:

$$T_{ld} = T_{td} = \frac{(PCTQ + 1) \times (DCTQ + 1)}{f_{CTQIN}} \quad (21.9)$$

$$T_{iw} = T_{nf} = \frac{(PCTQ1 + 1) \times (DCTQ1 + 1)}{f_{CTQIN}}$$

21.4.3.5 Protocol Interrupt Events

The following protocol-related events generated in SSC mode and can lead to a protocol interrupt. They are related to the start and the end of a data frame. After the start of a data frame a new setting could be programmed for the next data frame and after the end of a data frame the SSC connections to pins can be changed.

Please note that the bits in register PSR are not all automatically cleared by hardware and have to be cleared by software in order to monitor new incoming events.

- **MSLS Interrupt:**
This interrupt indicates in master mode (MSLS generation enabled) that a data frame has started (activation of MSLS) and has been finished (deactivation of MSLS). Any change of the internal MSLS signal sets bit PSR.MSLSEV and additionally, a protocol interrupt can be generated if PCRL.MSLSIEN = 1. The actual state of the internal MSLS signal can be read out at PSR.MSLS to take appropriate actions when this interrupt has been detected.
- **DX2T Interrupt:**
This interrupt monitors edges of the input signal of the DX2 stage (although this signal is not used as slave select input for data transfers).
A programmable edge detection for the DX2 input signal sets bit PSR.DX2TEV and additionally, a protocol interrupt can be generated if PCRL.DX2TIEN = 1. The actual state of the selected input signal can be read out at PSR.DX2S to take appropriate actions when this interrupt has been detected.

21.4.3.6 End-of-Frame Control

The information about the frame length is required for the MSLS generator of the master device. In addition to the mechanism based on the number of bits per frame (selected with $SCTRH.FLE < 63$), the following alternative mechanisms for end of frame handling are supported. It is recommended to set $SCTRH.FLE = 63$ (if several end of frame mechanisms are activated in parallel, the first end condition being found finishes the frame).

- **Software-based start of frame indication TCSRL.SOF:**
 This mechanism can be used if software handles the TBUF data without data FIFO. If bit SOF is set, a valid content of TBUF is considered as first word of a new frame. Bit SOF has to be set before the content of TBUF is transferred to the transmit shift register, so it is recommended to write it before writing data to TBUF. A current data word transfer is finished completely and the slave select delays T_{td} and T_{nf} are applied before starting a new data frame with T_{td} and the content of TBUF. For software-handling of bit SOF, bit $TCSRL.WLEMD = 0$ has to be programmed. In this case, all $TBUF[31:0]$ address locations show an identical behavior (TCI not taken into account for data handling).
- **Software-based end of frame indication TCSRL.EOF:**
 This mechanism can be used if software handles the TBUF data without data FIFO. If bit EOF is set, a valid content of TBUF is considered as last word of a new frame. Bit EOF has to be set before the content of TBUF is transferred to the transmit shift register, so it is recommended to write it before writing data to TBUF. The data word in TBUF is sent out completely and the slave select delays T_{td} and T_{nf} are applied. A new data frame can start with T_{td} with the next valid TBUF value. For software-handling of bit EOF, bit $TCSRL.WLEMD = 0$ has to be programmed. In this case, all $TBUF[31:0]$ address locations show an identical behavior (TCI not taken into account for data handling).
- **Software-based address related end of frame handling:**
 This mechanism can be used if software handles the TBUF data without data FIFO. If bit $TCSRL.WLEMD = 1$, the address of the written $TBUF[31:0]$ is used as transmit control information $TCI[4:0]$ to update $SCTRH.WLE (= TCI[3:0])$ and $TCSRL.EOF (= TCI[4])$ for each data word. The written $TBUF[31:0]$ address location defines the word length and the end of a frame (locations $TBUF[31:16]$ lead to a frame end). For example, writing transmit data to $TBUF[07]$ results in a data word of 8-bit length without finishing the frame, whereas writing transmit data to $TBUF[31]$ leads to a data word length of 16 bits, followed by T_{td} , the deactivation of MSLS and T_{nf} . If $TCSRL.WLEMD = 1$, bits $TCSRL.EOF$ and SOF , as well as $SCTRH.WLE$ must not be written by software after writing data to a TBUF location. Furthermore, it is recommended to clear bits $TCSRL.SELMD$, $FLEMD$ and $WAMD$.
- **FIFO-based address related end of frame handling:**
 This mechanism can be used if a data FIFO is used to store the transmit data. The general behavior is similar to the software-based address related end of frame

Universal Serial Interface Channel

handling, except that transmit data is not written to the locations TBUF[31:0], but to the FIFO input locations IN[31:0] instead. In this case, software must not write to any of the TBUF locations.

- **TBUF related end of frame handling:**
If bit PCRL.FEM = 0, an end of frame is assumed if the transmit buffer TBUF does not contain valid transmit data at the end of a data word transmission (TCSRL.TDV = 0 or in Stop Mode). In this case, the software has to take care that TBUF does not run empty during a data frame in Run Mode. If bit PCRL.FEM = 1, signal MSLS stays active while the transmit buffer is waiting for new data (TCSRL.TDV = 1 again) or until Stop Mode is left.
- **Explicit end of frame by software:**
The software can explicitly stop a frame by clearing bit PSR.MSLS by writing a 1 to the related bit position in register PSCR. This write action immediately clears bit PSR.MSLS, whereas the internal MSLS signal becomes inactive after finishing a currently running word transfer and respecting the slave select delays T_{id} and T_{nf} .

21.4.4 Operating the SSC in Slave Mode

In order to operate the SSC in slave mode, the following issues have to be considered:

- **Select SSC mode:**
 It is recommended to configure all parameters of the SSC that do not change during run time while $CCR.MODE = 0000_B$. Bit field $SCTRL.TRM = 01_B$ has to be programmed. The configuration of the input stages has to be done while $CCR.MODE = 0000_B$ to avoid unintended edges of the input signals and the SSC mode can be enabled afterwards by $CCR.MODE = 0001_B$.
- **Pin connections:**
 Establish a connection of input stage DX0 with the selected receive data input pin (signal DIN) with $DX0CR.INSW = 1$ and configure a transmit data output pin (signal DOUT).
 Establish a connection of input stage DX1 with the selected shift clock input pin (signal SCLKIN) with $DX1CR.INSW = 1$.
 Establish a connection of input stage DX2 with the selected slave select input pin (signal SELIN) with $DX2CR.INSW = 1$. If no slave select input signal is used, the DX2 stage has to deliver a 1-level to the data shift unit to allow data reception and transmission. If a slave device is not selected (DX2 stage delivers a 0 to the data shift unit) and a shift clock pulse are received, the incoming data is not received and the DOUT signal outputs the passive data level defined by $SCTRL.PDL$.
- **Baud rate generation:**
 The baud rate generator is not needed and can be switched off by the fractional divider.
- **Slave select generation:**
 The slave select delay generation is not needed and can be switched off. The bits and bit fields $MSLSEN$, $SELCTR$, $SELINV$, $CTQSEL1$, $PCTQ1$, $DCTQ1$, $MSLSIEN$, $SELO[7:0]$, and $TIWEN$ in registers $PCRL/PCRH$ are not necessary and can be programmed to 0.

21.4.4.1 Protocol Interrupts

The following protocol-related events generated in SSC mode and can lead to a protocol interrupt. They are related to the start and the end of a data frame. After the start of a data frame a new setting could be programmed for the next data frame and after the end of a data frame the SSC connections to pins can be changed.

Please note that the bits in register PSR are not all automatically cleared by hardware and have to be cleared by software in order to monitor new incoming events.

- **MSLS event:**
 The MSLS generation being switched off, this event is not available.
- **DX2T event:**
 The slave select input signal $SELIN$ is handled by the DX2 stage and the edges of the selected signal can generate a protocol interrupt. This interrupt allows to indicate

that a data frame has started and/or that a data frame has been completely finished. A programmable edge detection for the DX2 input signal activates DX2T, sets bit PSR.DX2TEV and additionally, a protocol interrupt can be generated if PCRL.DX2TIEN = 1. The actual state of the selected input signal can be read out at PSR.DX2S to take appropriate actions when this interrupt has been detected.

21.4.4.2 End-of-Frame Control

In slave mode, the following possibilities exist to determine the frame length. The slave device either has to refer to an external slave select signal, or to the number of received data bits.

- **Frame length known in advance by the slave device, no slave select:**
In this case bit field SCTR.H.FLE can be programmed to the known value (if it does not exceed 63 bits). A currently running data word transfer is considered as finished if the programmed frame length is reached.
- **Frame length not known by the slave, no slave select:**
In this case, the slave device's software has to decide on data word base if a frame is finished. Bit field SCTR.H.FLE can be either programmed to the word length SCTR.H.WLE, or to its maximum value to disable the slave internal frame length evaluation by counting received bits.
- **Slave device addressed via slave select signal SELIN:**
If the slave device is addressed by a slave select signal delivered by the communication master, the frame start and end information are given by this signal. In this case, bit field SCTR.H.FLE should be programmed to its maximum value to disable the slave internal frame length evaluation.

21.4.5 SSC Protocol Registers

In SSC mode, the registers PCRL, PCRH and PSR handle SSC related information.

21.4.5.1 SSC Protocol Control Registers

In SSC mode, the PCRL/PCRH register bits or bit fields are defined as described in this section.

PCRL

Protocol Control Register L [SSC Mode]

(40_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DX2 TIEN	MSL SIEN	0	DCTQ1				PCTQ1		CTQSEL1		FEM	SE INV	SEL CTR	MSL SEN	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
MSLSEN	0	rw	MSLS Enable This bit enables/disables the generation of the master slave select signal MSLS. If the SSC is a transfer slave, the SLS information is read from a pin and the internal generation is not needed. If the SSC is a transfer master, it has to provide the MSLS signal. 0 _B The MSLS generation is disabled (MSLS = 0). This is the setting for SSC slave mode. 1 _B The MSLS generation is enabled. This is the setting for SSC master mode.
SELCTR	1	rw	Select Control This bit selects the operating mode for the SELO[7:0] outputs. 0 _B The coded select mode is enabled. 1 _B The direct select mode is enabled.
SELINV	2	rw	Select Inversion This bit defines if the polarity of the SELO[7:0] outputs in relation to the master slave select signal MSLS. 0 _B The SELO outputs have the same polarity as the MSLS signal (active high). 1 _B The SELO outputs have the inverted polarity to the MSLS signal (active low).

Field	Bits	Type	Description
FEM	3	rw	Frame End Mode This bit defines if a transmit buffer content that is not valid for transmission is considered as an end of frame condition for the slave select generation. 0_B The current data frame is considered as finished when the last bit of a data word has been sent out and the transmit buffer TBUF does not contain new data ($TDV = 0$). 1_B The MSLS signal is kept active also while no new data is available and no other end of frame condition is reached. In this case, the software can accept delays in delivering the data without automatic deactivation of MSLS in multi-word data frames.
CTQSEL1	[5:4]	rw	Input Frequency Selection This bit field defines the input frequency f_{CTQIN} for the generation of the slave select delays T_{iw} and T_{nf} . 00_B $f_{CTQIN} = f_{PDIV}$ 01_B $f_{CTQIN} = f_{PPP}$ 10_B $f_{CTQIN} = f_{SCLK}$ 11_B $f_{CTQIN} = f_{MCLK}$
PCTQ1	[7:6]	rw	Divider Factor PCTQ1 for T_{iw} and T_{nf} This bit field represents the divider factor PCTQ1 (range = 0 - 3) for the generation of the inter-word delay and the next-frame delay. $T_{iw} = T_{nf} = 1/f_{CTQIN} * (PCTQ1 + 1) * (DCTQ1 + 1)$
DCTQ1	[12:8]	rw	Divider Factor DCTQ1 for T_{iw} and T_{nf} This bit field represents the divider factor DCTQ1 (range = 0 - 31) for the generation of the inter-word delay and the next-frame delay. $T_{iw} = T_{nf} = 1/f_{CTQIN} * (PCTQ1 + 1) * (DCTQ1 + 1)$
MSLSIEN	14	rw	MSLS Interrupt Enable This bit enables/disables the generation of a protocol interrupt if the state of the MSLS signal changes (indicated by $PSR.MSLSEV = 1$). 0_B A protocol interrupt is not generated if a change of signal MSLS is detected. 1_B A protocol interrupt is generated if a change of signal MSLS is detected.

Universal Serial Interface Channel

Field	Bits	Type	Description
DX2TIEN	15	rw	DX2T Interrupt Enable This bit enables/disables the generation of a protocol interrupt if the DX2T signal becomes activated (indicated by PSR.DX2TEV = 1). 0_B A protocol interrupt is not generated if DX2T is activated. 1_B A protocol interrupt is generated if DX2T is activated.
0	13	rw	Reserved Returns 0 if read; should be written with 0.

PCRH

Protocol Control Register H [SSC Mode]

(42_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M				0			TIW				SELO				
CLK							EN								
rw				rw			rw				rw				

Field	Bits	Type	Description
SELO	[7:0]	rw	Select Output This bit field defines the setting of the SELO[7:0] output lines. 0_B The corresponding SELOx line cannot be activated. 1_B The corresponding SELOx line can be activated (according to the mode selected by SELCTR).
TIWEN	8	rw	Enable Inter-Word Delay T_{iw} This bit enables/disables the inter-word delay T_{iw} after the transmission of a data word. 0_B No delay between data words of the same frame. 1_B The inter-word delay T_{iw} is enabled and introduced between data words of the same frame.

Field	Bits	Type	Description
MCLK	15	rw	Master Clock Enable This bit enables/disables the generation of the master clock output signal MCLK, independent from master or slave mode. 0 _B The MCLK generation is disabled and output MCLK = 0. 1 _B The MCLK generation is enabled.
0	[14:9]	rw	Reserved Returns 0 if read; not modified in SSC mode.

21.4.5.2 SSC Protocol Status Register

In SSC mode, the PSR register bits or bit fields are defined as described in this section. The bits and bit fields in register PSR are not cleared by hardware.

The flags in the PSR register can be cleared by writing a 1 to the corresponding bit position in register PSCR. Writing a 1 to a bit position in PSR sets the corresponding flag, but doesn't lead to further actions (no interrupt generation). Writing a 0 has no effect. The PSR flags should be cleared by software before enabling a new protocol.

PSR

Protocol Status Register [SSC Mode] (44_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AIF	RIF	TBIF	TSIF	DLIF	RSIF				0			DX2 TEV	MSL SEV	DX2 S	MSL S
rwh	rwh	rwh	rwh	rwh	rwh				r			rwh	rwh	rwh	rwh

Field	Bits	Type	Description
MSLS	0	rwh	MSLS Status This bit indicates the current status of the MSLS signal. It must be cleared by software to stop a running frame. 0 _B The internal signal MSLS is inactive (0). 1 _B The internal signal MSLS is active (1).
DX2S	1	rwh	DX2S Status This bit indicates the current status of the DX2S signal that can be used as slave select input SELIN. 0 _B DX2S is 0. 1 _B DX2S is 1.
MSLSEV	2	rwh	MSLS Event Detected¹⁾ This bit indicates that the MSLS signal has changed its state since MSLSEV has been cleared. Together with the MSLS status bit, the activation/deactivation of the MSLS signal can be monitored. 0 _B The MSLS signal has not changed its state. 1 _B The MSLS signal has changed its state.
DX2TEV	3	rwh	DX2T Event Detected¹⁾ This bit indicates that the DX2T trigger signal has been activated since DX2TEV has been cleared. 0 _B The DX2T signal has not been activated. 1 _B The DX2T signal has been activated.

Universal Serial Interface Channel

Field	Bits	Type	Description
0	[9:4]	r	Reserved Returns 0 if read; not modified in SSC mode.
RSIF	10	rwh	Receiver Start Indication Flag 0 _B A receiver start event has not occurred. 1 _B A receiver start event has occurred.
DLIF	11	rwh	Data Lost Indication Flag 0 _B A data lost event has not occurred. 1 _B A data lost event has occurred.
TSIF	12	rwh	Transmit Shift Indication Flag 0 _B A transmit shift event has not occurred. 1 _B A transmit shift event has occurred.
TBIF	13	rwh	Transmit Buffer Indication Flag 0 _B A transmit buffer event has not occurred. 1 _B A transmit buffer event has occurred.
RIF	14	rwh	Receive Indication Flag 0 _B A receive event has not occurred. 1 _B A receive event has occurred.
AIF	15	rwh	Alternative Receive Indication Flag 0 _B An alternative receive event has not occurred. 1 _B An alternative receive event has occurred.

1) This status bit can generate a protocol interrupt in SSC mode (see [Page 21-24](#)). The general interrupt status flags are described in the general interrupt chapter.

21.4.6 SSC Timing Considerations

The input and output signals have to respect certain timings in order to ensure correct data reception and transmission. In addition to module internal timings (due to input filters, reaction times on events, etc.), also the timings from the input pin via the input stage (T_{in}) to the module and from the module via the output driver stage to the pin (T_{out}), as well as the signal propagation on the wires (T_{prop}) have to be taken into account.

Please note that there might be additional delays in the DXn input stages, because the digital filter and the synchronization stages lead to systematic delays, that have to be considered if these functions are used.

21.4.6.1 Closed-loop Delay

A system-inherent limiting factor for the baud rate of an SSC connection is the closed-loop delay. In a typical application setup, a communication master device is connected to a slave device in full-duplex mode with independent lines for transmit and receive data. In a general case, all transmitters refer to one shift clock edge for transmission and all receivers refer to the other shift clock edge for reception. The master device's SSC module sends out the transmit data, the shift clock and optionally the slave select signal. Therefore, the baud rate generation (BRG) and slave select generation (SSG) are part of the master device. The frame control is similar for SSC modules in master and slave mode, the main difference is the fact which module generates the shift clock and optionally, the slave select signals.

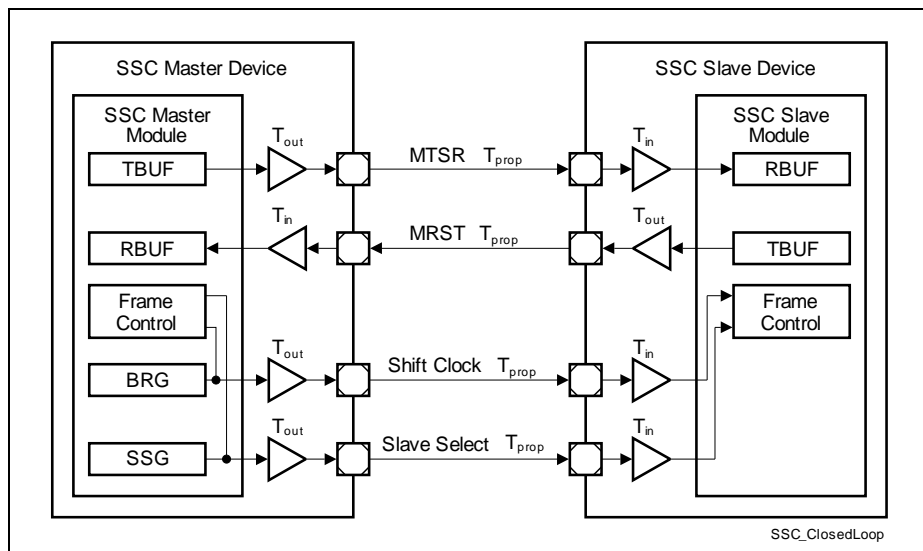


Figure 21-38 SSC Closed-loop Delay

The signal path between the SSC modules of the master and the slave device includes the master's output driver, the wiring to the slave device and the slave device's input stage. With the received shift clock edges, the slave device receives the master's transmit data and transmits its own data back to the master device, passing by a similar signal path in the other direction. The master module receives the slave's transmit data related to its internal shift clock edges. In order to ensure correct data reception in the master device, the slave's transmit data has to be stable (respecting setup and hold times) as master receive data with the next shift clock edge of the master (generally 1/2 shift clock period). To avoid data corruption, the accumulated delays of the input and output stages, the signal propagation on the wiring and the reaction times of the transmitter/receiver have to be carefully considered, especially at high baud rates.

In the given example, the time between the generation of the shift clock signal and the evaluation of the receive data by the master SSC module is given by the sum of $T_{out_master} + 2 * T_{prop} + T_{in_slave} + T_{out_slave} + T_{in_master}$ + module reaction times + input setup times. The input path is characterized by an input delay depending mainly on the input stage characteristics of the pads. The output path delay is determined by the output driver delay and its slew rate, the external load and current capability of the driver. The device specific values for the input/output driver are given in the Data Sheet.

21.4.6.2 Delay Compensation in Master Mode

A higher baud rate can be reached by delay compensation in master mode. This compensation is possible if (at least) the shift clock pin is bidirectional.

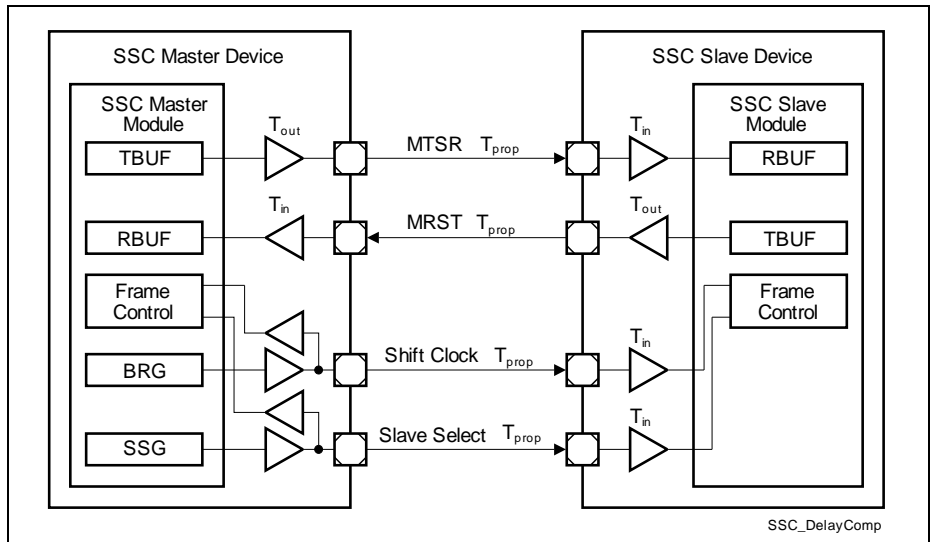


Figure 21-39 SSC Master Mode with Delay Compensation

Universal Serial Interface Channel

If the shift clock signal in master mode is directly taken from the input function in parallel to the output signal, the output delay of the master device's shift clock output is compensated and only the difference between the input delays of the master and the slave devices have to be taken into account instead of the complete master's output delay and the slave's input delay of the shift clock path.

In the given example, the time between the evaluation of the shift clock signal and the receive data by the master SSC module is reduced by $T_{in_master} + T_{out_master}$.

Although being a master mode, the shift clock input and optionally the slave select signal are not directly connected internally to the data shift unit, but are taken as external signals from input pins ($DXnCR.INSW = 1$). The delay compensation does not lead to additional pins for the SSC communication if the shift clock output pin (slave select output pin, respectively) is/are bidirectional. In this case, the input signal is decoupled from other internal signals, because it is related to the signal level at the pin itself.

21.5 Inter-IC Bus Protocol (IIC)

The IIC protocol of the USIC refers to the IIC bus specification version 2.1, January 2000 from Philips Semiconductors. Contrary to that specification, the USIC device assumes rise/fall times of the bus signals of max. 300 ns in all modes. Please refer to the pad characteristics in the AC/DC chapter for the driver capability. CBUS mode and HS mode are not supported.

The IIC mode is selected by `CCR.MODE = 0100B` with `CCFG.IIC = 1` (IIC mode available).

This chapter contains the following sections:

- Introduction (see [Page 21-161](#))
- Operating the IIC protocol (see [Page 21-165](#))
- Symbol timing and programming (see [Page 21-171](#))
- Data flow handling (see [Page 21-174](#))
- IIC protocol registers (see [Page 21-179](#))

21.5.1 Introduction

USIC IIC Features:

- Two-wire interface, with one line for shift clock transfer and synchronization (shift clock SCL), the other one for the data transfer (shift data SDA)
- Communication in standard mode (100 kBit/s) or in fast mode (up to 400 kBit/s)
- Support of 7-bit addressing, as well as 10-bit addressing
- Master mode operation,
where the IIC controls the bus transactions and provides the clock signal.
- Slave mode operation,
where an external master controls the bus transactions and provides the clock signal.
- Multi-master mode operation,
where several masters can be connected to the bus and bus arbitration can take place, i.e. the IIC module can be master or slave. The master/slave operation of an IIC bus participant can change from frame to frame.
- Efficient frame handling (low software effort), also allowing PEC transfers
- Powerful interrupt handling due to multitude of indication flags
- Compensation support for input delays

21.5.1.1 Signal Description

An IIC connection is characterized by two wires (SDA and SCL). The output drivers for these signals must have open-drain characteristics to allow the wired-AND connection of all SDA lines together and all SCL lines together to form the IIC bus system. Due to this structure, a high level driven by an output stage does not necessarily lead immediately to a high level at the corresponding input. Therefore, each SDA or SCL connection has to be input and output at the same time, because the input function always monitors the level of the signal, also while sending.

- Shift data SDA: input handled by DX0 stage, output signal DOUT
- Shift clock SCL: input handled by DX1 stage, output signal SCLKOUT

Figure 21-25 shows a connection of two IIC bus participants (modules IIC A and IIC B) using the USIC. In this example, the pin assignment of module IIC A shows separate pins for the input and output signals for SDA and SCL. This assignment can be used if the application does not provide pins having DOUT and a DX0 stage input for the same pin (similar for SCLKOUT and DX1). The pin assignment of module IIC B shows the connection of DOUT and a DX0 input at the same pin, also for SCLKOUT and a DX1 input.

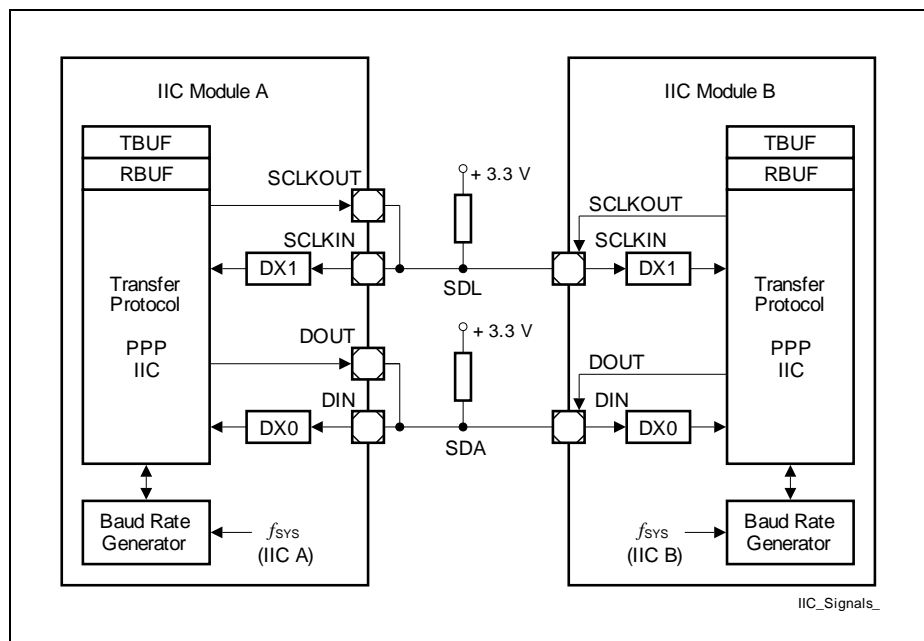


Figure 21-40 IIC Signal Connections

21.5.1.2 Symbols

A symbol is a sequence of edges on the lines SDA and SCL. Symbols contain 10 or 25 time quanta t_q , depending on the selected baud rate. The baud rate generator determines the length of the time quanta t_q , the sequence of edges in a symbol is handled by the IIC protocol pre-processor, and the sequence of symbols can be programmed by the user according to the application needs.

The following symbols are defined:

- Bus idle:
SDA and SCL are high. No data transfer takes place currently.
- Data bit symbol:
SDA stable during the high phase of SCL. SDA then represents the transferred bit value. There is one clock pulse on SCL for each transferred bit of data. During data transfers SDA may only change while SCL is low.
- Start symbol:
Signal SDA being high followed by a falling edge of SDA while SCL is high indicates a start condition. This start condition initiates a data transfer over the IIC bus after the bus has been idle.
- Repeated start symbol:
This start condition initiates a data transfer over the bus after a data symbol when the bus has not been idle. Therefore, SDA is set high and SCL low, followed by a start symbol.
- Stop symbol:
A rising edge on SDA while SCL is high indicates a stop condition. This stop condition terminates a data transfer to release the bus to idle state. Between a start condition and a stop condition an arbitrary number of bytes may be transferred.

21.5.2 Operating the IIC

In order to operate the IIC protocol, the following issues have to be considered:

- **Select IIC mode:**
 It is recommended to configure all parameters of the IIC that do not change during run time while $CCR.MODE = 0000_B$. Bit field $SCTRL.TRM = 11_B$ should to be programmed. The configuration of the input stages has to be done while $CCR.MODE = 0000_B$ to avoid unintended edges of the input signals and the IIC mode can be enabled by $CCR.MODE = 0100_B$ afterwards.
- **Pin connections:**
 Establish a connection of input stage DX0 (with $DX0CR.DPOL = 0$) to the selected shift data pin SDA (signal DIN) with $DX0CR.INSW = 0$ and configure the transmit data output signal DOUT (with $SCTRL.DOCFG = 00_B$) to the same pin. If available, this can be the same pin for input and output, or connect the selected input pin and the output pin to form the SDA line.
 The same mechanism applies for the shift clock line SCL. Here, signal $SCLKOUT$ (with $BRGH.SCLKCFG = 00_B$) and an input of the DX1 stage have to be connected (with $DX1CR.DPOL = 0$).
 The input stage DX2 is not used for the IIC protocol.
 If the digital input filters are enabled in the DX0/1 stages, their delays have to be taken into account for correct calculation of the signal timings.
 The pins used for SDA and SCL have to be set to open-drain mode to support the wired-AND structure of the IIC bus lines.
 Note that the basic I/O port configuration for the IIC I/O pins must also setup correctly before the IIC mode becomes enabled by $CCR.MODE = 0100_B$.
- **Bit timing configuration:**
 In standard mode (100 kBit/s) a minimum module frequency of 2 MHz is necessary, whereas in fast mode (400 kBit/s) a minimum of 10 MHz is required. Additionally, if the digital filter stage should be used to eliminate spikes up to 50 ns, a filter frequency of 20 MHz is necessary.
 There could be an uncertainty in the SCL high phase timing of maximum $1/f_{PP}$ if another IIC participant lengthens the SCL low phase on the bus.
 More details are given in [Section 21.5.3](#).
- **Data format configuration:**
 The data format has to be configured for 8 data bits ($SCTRH.WLE = 7$), unlimited data flow ($SCTRH.FLE = 3FF_H$), and MSB shifted first ($SCTRL.SDIR = 1$). The parity generation has to be disabled ($CCR.PM = 00_B$).
- **General hints:**
 The IIC slave module becomes active (for reception or transmission) if it is selected by the address sent by the master. In the case that the slave sends data to the master, it uses the transmit path. So a master must not request to read data from the slave address defined for its own channel in order to avoid collisions.
 The built-in error detection mechanisms are only activated while the IIC module is

taking part in IIC bus traffic.

If the slave can not deal with too high frequencies, it can lengthen the low phase of the SCL signal.

For data transfers according to the IIC specification, the shift data line SDA shall only change while SCL = 0 (defined by IIC bus specification).

21.5.2.1 Transmission Chain

The IIC bus protocol requiring a kind of in-bit-response during the arbitration phase and while a slave is transmitting, the resulting loop delay of the transmission chain can limit the reachable maximal baud rate, strongly depending on the bus characteristics (bus load, module frequency, etc.).

Figure 21-25 shows the general signal path and the delays in the case of a slave transmission. The shift clock SCL is generated by the master device, output on the wire, then it passes through the input stage and the input filter. Now, the edges can be detected and the SDA data signal can be generated accordingly. The SDA signal passes through the output stage and the wire to the master receiver part. There, it passes through the input stage and the input filter before it is sampled.

This complete loop has to be finished (including all settling times to obtain stable signal levels) before the SCL signal changes again. The delays in this path have to be taken into account for the calculation of the baud rate as a function of f_{SYS} and f_{PPP} .

21.5.2.2 Byte Stretching

If a device is selected as transceiver and should transmit a data byte but the transmit buffer TBUF does not contain valid data to be transmitted, the device ties down SCL = 0 at the end of the previous acknowledge bit. The waiting period is finished if new valid data has been detected in TBUF.

21.5.2.3 Baud Rate Update

The baud rate setting can be changed from frame to frame. The BRGL/H register setting and PCR.STIM are sampled (shadowed) while the IIC bus is idle. A new setting of these bits can be programmed while a frame is running. The new setting will be taken into account with the start of the next frame. In order to minimize the risk of inconsistencies when changing baud rate setting (several registers have to be updated), it is recommended to avoid baud rate changes while the IIC protocol is enabled, especially for slave devices.

21.5.2.4 Master Arbitration

During the address and data transmission, the master transmitter checks at the rising edge of SCL for each data bit if the value it is sending is equal to the value read on the SDA line. If yes, the next data bit values can be 0. If this is not the case (transmitted

value = 1, value read = 0), the master has lost the transmit arbitration. This is indicated by status flag PSR.ARL and can generate a protocol interrupt if enabled by PCRH.ARLIEN.

When the transmit arbitration has been lost, the software has to initialize the complete frame again, starting with the first address byte together with the start condition for a new master transmit attempt. Arbitration also takes place for the ACK bit.

21.5.2.5 Release of TBUF

In case of a non-acknowledge or an error, the content of TBUF becomes invalid. In both cases, the software has to flush the transmit buffer and to set it up again with appropriate values to react on the previous event.

21.5.2.6 Mode Control Behavior

In multi-master mode, only run mode 0 and stop mode 0 are supported, the other modes must not be programmed.

- **Run Mode 0:**
Behavior as programmed. If TCSRL.TDV = 0 (no new valid TBUF entry found) when a new TBUF entry needs to be processed, the IIC module waits for TDV becoming set to continue operation.
- **Run Mode 1:**
Behavior as programmed. If in master mode, TCSRL.TDV = 0 (no new valid TBUF entry found) when a new TBUF entry needs to be processed, the IIC module sends a stop condition to finish the frame. In slave mode, no difference to run mode 0.
- **Stop Mode 0:**
Bit TCSRL.TDV is internally considered as 0 (the bit itself is not modified by the stop mode). A currently running word is finished normally, but no new word is started in case of master mode (wait for TDV active).
Bit TDV being considered as 0 for master and slave, the slave will force a wait state on the bus if read by an external master, too.
Additionally, it is not possible to force the generation of a STOP condition out of the wait state. The reason is, that a master read transfer must be finished with a not-acknowledged followed by a STOP condition to allow the slave to release his SDA line. Otherwise the slave may force the SDA line to 0 (first data bit of next byte) making it impossible to generate the STOP condition (rising edge on SDA).
To continue operation, the mode must be switched to run mode 0
- **Stop Mode 1:**
Same as stop mode 0, but additionally, a master sends a STOP condition to finish the frame.
If stop mode 1 is requested for a master device after the first byte of a 10 bit address, a stop condition will be sent out. In this case, a slave device will issue an error interrupt.

21.5.2.7 IIC Protocol Interrupt Events

The following protocol-related events are generated in IIC mode and can lead to a protocol interrupt.

Please note that the bits in register PSR are not all automatically cleared by hardware and have to be cleared by software in order to monitor new incoming events.

- **Transmit buffer event:**
 The transmit buffer event indication flag PSR.TBIF is set when the content of the transmit buffer TBUF has been loaded to the transmit shift register, indicating that the action requested by the TBUF entry has started.
 With this event, bit TCSRL.TDV is cleared. This interrupt can be used to write the next TBUF entry while the last one is in progress (handled by the transmitter part).
- **Receive event:**
 This receive event indication flag PSR.RIF indicates that a new data byte has been written to the receive buffer RBUF0/1 (except for the first data byte of a new frame, that is indicated by an alternative receive interrupt). The flag becomes set when the data byte is received (after the falling edge of SCL). This interrupt can be used to read out the received data while a new data byte can be in progress (handled by the receiver part).
- **Alternate receive event:**
 The alternative receive event indication flag AIF is based on bit RBUFSR[9] (same as RBUF[9]), indicating that the received data word has been the first data word of a new data frame.
- **Protocol interrupt events:**
 The IIC protocol related interrupt events are either indicating the reception of symbols or the detection of frame errors (common indication PSR.ERR) or unexpected/wrong TDF codes (common indication PSR.WTDF).
 - start condition received at a correct position in a frame (PSR.SCR)
 - repeated start condition received at a correct position in a frame (PSR.RSCR)
 - stop condition transferred at a correct position in a frame (PSR.PCR)
 - master arbitration lost (PSR.ARL)
 - slave read requested (PSR.SRR)
 - acknowledge not received (PSR.NACK)
 - start condition not at the expected position in a frame (PSR.ERR)
 - stop condition not at the expected position in a frame (PSR.ERR)
 - as slave, 10-bit address interrupted by a stop condition after the first address byte (PSR.ERR)
 - TDF slave code in master mode (PSR.WTDF)
 - TDF master code in slave mode (PSR.WTDF)
 - Reserved TDF code found (PSR.WTDF)
 - Start condition code during a running frame in master mode (PSR.WTDF)
 - Data byte transmission code after transfer direction has been changed to reception (master read) in master mode (PSR.WTDF)

If a wrong TDF code is found in TBUF, the error event is active until the TDF value is either corrected or invalidated. If the related interrupt is enabled, the interrupt handler should check PSR.WDTF first and correct or invalidate TBUF, before dealing with the other possible interrupt events.

21.5.2.8 Receiver Address Acknowledge

After a (repeated) start condition, the master sends a slave address to identify the target device of the communication. The start address can comprise one or two address bytes (for 7 bit or for 10 bit addressing schemes). After an address byte, a slave sensitive to the transmitted address has to acknowledge the reception.

Therefore, the slave's address can be programmed in the device, where it is compared to the received address. In case of a match, the slave answers with an acknowledge (SDA = 0). Slaves that are not targeted answer with a non-acknowledge (SDA = 1).

In addition to the match of the programmed address, an other address byte value has to be answered with an acknowledge if the slave is capable to handle the corresponding requests. The address byte 00_H indicates a general call address, that can be acknowledged. The value 01_H stands for a start byte generation, that is not acknowledged

In order to allow selective acknowledges for the different values of the address byte(s), the following control mechanism is implemented:

- The address byte 00_H is acknowledged if bit PCRH.ACK00 is set.
- The address byte 01_H is not acknowledged.
- The first 7 bits of a received first address byte are compared to the programmed slave address (PCR.SLAD[15:9]). If these bits match, the slave sends an acknowledge. In addition to this, if the slave address is programmed to 1111 0XX_B, the slave device waits for a second address byte and compares it also to PCR.SLAD[7:0] and sends an acknowledge accordingly to cover the 10 bit addressing mode. The user has to take care about reserved addresses (refer to IIC specification for more detailed description). Only the address 1111 0XX_B is supported.

Under each of these conditions, bit PSR.SLSEL will be set when the addressing delivered a match. This bit is cleared automatically by a (repeated) start condition.

21.5.2.9 Receiver Handling

A selected slave receiver always acknowledges a received data byte. If the receive buffers RBUF0/1 are already full and can not accept more data, the respective register is overwritten (PSR.DLI becomes set in this case and a protocol interrupt can be generated).

An address reception also uses the registers RBUF0/1 to store the address before checking if the device is selected. The received addresses do not set RDV0/1, so the addresses are not handled like received data.

21.5.2.10 Receiver Status Information

In addition to the received data byte, some IIC protocol related information is stored in the 16-bit data word of the receive buffer. The received data byte is available at the bit positions RBUF[7:0], whereas the additional information is monitored at the bit positions RBUF[12:8]. This structure allows to identify the meaning of each received data byte without reading additional registers, also when using a FIFO data buffer.

- **RBUF[8]:**
Value of the received acknowledge bit. This information is also available in RBUFISR[8] as protocol argument.
- **RBUF[9]:**
A 1 at this bit position indicates that after a (repeated) start condition followed by the address reception the first data byte of a new frame has been received. A 0 at this bit position indicates further data bytes. This information is also available in RBUFISR[9], allowing different interrupt routines for the address and data handling.
- **RBUF[10]:**
A 0 at this bit position indicates that the data byte has been received when the device has been in slave mode, whereas a 1 indicates a reception in master mode.
- **RBUF[11]:**
A 1 at this bit position indicates an incomplete/erroneous data byte in the receive buffer caused by a wrong position of a START or STOP condition in the frame. The bit is not identical to the frame error status bit in PSR, because the bit in the PSR has to be cleared by software ("sticky" bit), whereas RBUF[11] is evaluated data byte by data byte. If RBUF[11] = 0, the received data byte has been correct, independent of former errors.
- **RBUF[12]:**
A 0 at this bit position indicates that the programmed address has been received. A 1 indicates a general call address.

21.5.3 Symbol Timing

The symbol timing of the IIC is determined by the master stimulating the shift clock line SCL. It is different for standard and fast IIC mode.

- 100 kBaud standard mode (PCR.H.STIM = 0):
The symbol timing is based on 10 time quanta t_q per symbol. A minimum module clock frequency $f_{SYS} = 2$ MHz is required.
- 400 kBaud standard mode (PCR.H.STIM = 1):
The symbol timing is based on 25 time quanta t_q per symbol. A minimum module clock frequency $f_{SYS} = 10$ MHz is required.

The baud rate setting should only be changed while the transmitter and the receiver are idle or CCR.MODE = 0. The bits in register BRGL define the length of a time quantum t_q that is given by one period of f_{PCTQ} .

- BRGL.CTQSEL
to define the input frequency f_{CTQIN} for the time quanta generation
- BRGL.PCTQ
to define the length of a time quantum (division of f_{CTQIN} by 1, 2, 3, or 4)
- BRGL.DCTQ
to define the number of time quanta per symbol (number of $t_q = DCTQ + 1$)

The standard setting is given by CTQSEL = 00_B ($f_{CTQIN} = f_{PDIV}$) and PPPEN = 0 ($f_{PPP} = f_{IN}$). Under these conditions, the frequency f_{PCTQ} is given by:

$$f_{PCTQ} = f_{PIN} \times \frac{1}{PDIV + 1} \times \frac{1}{PCTQ + 1} \quad (21.10)$$

To respect the specified SDA hold time of 300 ns after a falling edge of signal SCL, a hold delay t_{HDEL} has been introduced. It also prevents an erroneous detection of a start or a stop condition. The length of this delay can be programmed by bit field PCR.H.HDEL. Taking into account the input sampling and output update, bit field HDEL can be programmed according to:

$$\begin{aligned} HDEL &\geq 300 \text{ ns} \times f_{PPP} - \left(3 \times \frac{f_{PPP}}{f_{SYS}} \right) + 1 && \text{with digital filter and } HDEL_{min} = 2 \\ & && (21.11) \\ HDEL &\geq 300 \text{ ns} \times f_{PPP} - \left(3 \times \frac{f_{PPP}}{f_{SYS}} \right) + 2 && \text{without digital filter and } HDEL_{min} = 1 \end{aligned}$$

If the digital input filter is used, HDEL compensates the filter delay of 2 filter periods (f_{PPP} should be used) in case of a spike on the input signal. This ensures that a data bit on the SDA line changing just before the rising edge or behind the falling edge of SCL won't be treated as a start or stop condition.

21.5.3.1 Start Symbol

Figure 21-42 shows the general start symbol timing.

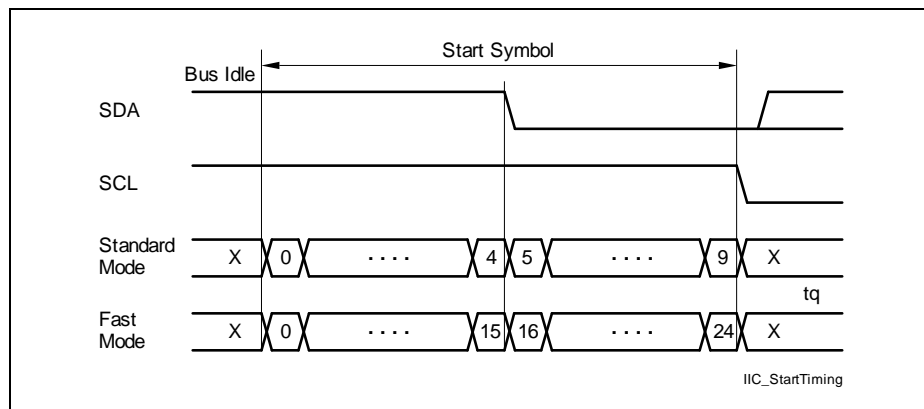


Figure 21-42 Start Symbol Timing

21.5.3.2 Repeated Start Symbol

During the first part of a repeated start symbol, an SCL low value is driven for the specified number of time quanta. Then a high value is output. After the detection of a rising edge at the SCL input, a normal start symbol is generated, as shown in Figure 21-43.

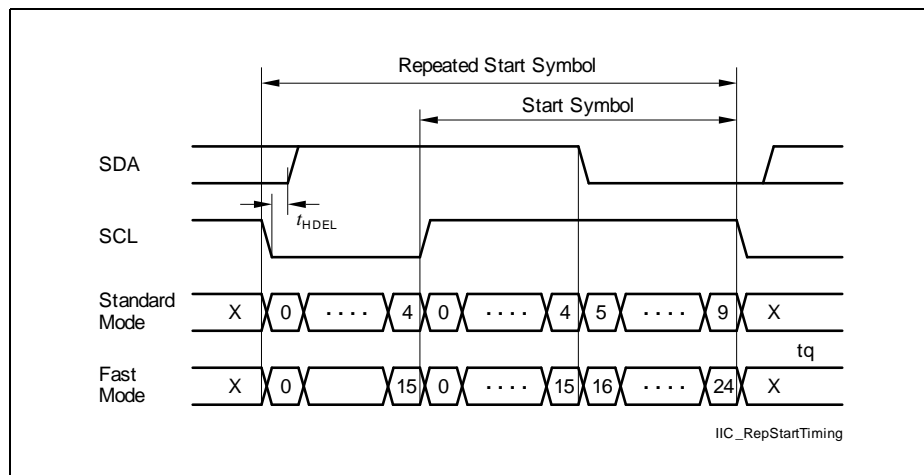


Figure 21-43 Repeated Start Symbol Timing

PCR.HDEL allows compensation of the delay of the SCL input path (sampling, filtering).

In the case of an acknowledge transmission, the USIC IIC waits for the receiver indicating that a complete byte has been received. This adds an additional delay of 3 periods of f_{SYS} to the path. The minimum module input frequency has to be selected properly to ensure the SDA setup time to SCL rising edge.

21.5.4 Data Flow Handling

The handling of the data flow and the sequence of the symbols in an IIC frame is controlled by the IIC transmitter part of the USIC communication channel. The IIC bus protocol is byte-oriented, whereas a USIC data buffer word can contain up to 16 data bits. In addition to the data byte to be transmitted (located at TBUF[7:0]), bit field TDF (transmit data format) to control the IIC sequence is located at the bit positions TBUF[10:8]. The TDF code defines for each data byte how it should be transmitted (IIC master or IIC slave), and controls the transmission of (repeated) start and stop symbols. This structure allows the definition of a complete IIC frame for an IIC master device only by writing to TBUFx or by using a FIFO data buffer mechanism, because no other control registers have to be accessed.

If a wrong or unexpected TDF code is encountered (e.g. due to a software error during setup of the transmit buffer), a stop condition will be sent out by the master. This leads to an abort of the currently running frame. A slave module waits for a valid TDF code and sets SCL = 0. The software then has to invalidate the unexpected TDF code and write a valid one.

Please note that during an arbitration phase in multi-master bus systems an unpredictable bus behavior may occur due to an unexpected stop condition.

21.5.4.1 Transmit Data Formats

The following transmit data formats are available in master mode:

- Send data byte as master (TDF = 000_B):
This format is used to transmit a data byte from the master to a slave. The transmitter sends its data byte (TBUF[7:0]), receives and checks the acknowledge bit sent by the slave.
- Receive data byte and send acknowledge 0 (TDF = 010_B):
This format is used by the master to read a data byte from a slave. The master acknowledges the transfer with a 0-level to continue the transfer. The content of TBUF[7:0] is ignored.
- Receive data byte and send acknowledge 1 (TDF = 011_B):
This format is used by the master to read a data byte from a slave. The master does not acknowledge the transfer with a 1-level to finish the transfer. The content of TBUF[7:0] is ignored.

Universal Serial Interface Channel

- Send start condition (TDF = 100_B):
If TBUF contains this entry while the bus is idle, a start condition will be generated. The content of TBUF[7:0] is taken as first address byte for the transmission (bits TBUF[7:1] are the address, the LSB is the read/write control).
- Send repeated start condition (TDF = 101_B):
If TBUF contains this entry and SCL = 0 and a byte transfer is not in progress, a repeated start condition will be sent out if the device is the current master. The current master is defined as the device that has set the start condition (and also won the master arbitration) for the current message. The content of TBUF[7:0] is taken as first address byte for the transmission (bits TBUF[7:1] are the address, the LSB is the read/write control).
- Send stop condition (TDF = 110_B):
If the current master has finished its last byte transfer (including acknowledge), it sends a stop condition if this format is in TBUF. The content of TBUF[7:0] is ignored.
- TDF = 111_B:
Reserved and must not be programmed. No additional action except releasing the TBUF entry and setting the error bit in PSR (that can lead to a protocol interrupt).

The following transmit data format is available in slave mode (the symbols in a frame are controlled by the master and the slave only has to send data if it has been “asked” by the master):

- Send data byte as slave (TDF = 001_B):
This format is used to transmit a data byte from a slave to the master. The transmitter sends its data byte (TBUF[7:0]) plus the acknowledge bit as a 1.

21.5.4.2 Valid Master Transmit Data Formats

Due to the IIC frame format definitions, only some specific sequences of TDF codes are possible and valid. If the USIC IIC module detects a wrong TDF code in a running frame, the transfer is aborted and flag PCR.WTDF is set. Additionally, an interrupt can be generated if enabled by the user. In case of a wrong TDF code, the frame will be aborted immediately with a STOP condition if the USIC IIC master still owns the SDA line. But if the accessed slave owns the SDA line (read transfer), the master must perform a dummy read with a non-acknowledge so that the slave releases the SDA line before a STOP condition can be sent. The received data byte of the dummy read will be stored in RBUF0/1, but RDV0/1 won't be set. Therefore the dummy read won't generate a receive interrupt and the data byte won't be stored into the receive FIFO.

If the transfer direction has changed in the current frame (master read access), the transmit data request (TDF = 000_B) is not possible and won't be accepted (leading to a wrong TDF Code indication).

Table 21-9 Valid TDF Codes Overview

Frame Position	Valid TDF Codes
First TDF code (master idle)	Start (100 _B)
Read transfer: second TDF code (after start or repeated start)	Receive with acknowledge (010 _B) or receive with not-acknowledge (011 _B)
Write transfer: second TDF code (after start or repeated start)	Transmit (000 _B), repeated start (101 _B), or stop (110 _B)
Read transfer: third and subsequent TDF code after acknowledge	Receive with acknowledge (010 _B) or receive with not-acknowledge (011 _B)
Read transfer: third and subsequent TDF code after not-acknowledge	Repeated start (101 _B) or stop (110 _B)
Write transfer: third and subsequent TDF code	Transmit (000 _B), repeated start (101 _B), or stop (110 _B)

- First TDF code:
A master transfer starts with the TDF start code (100_B). All other codes are ignored, but no WTDF error will be indicated.
- TDF code after a start (100_B) or repeated start code (101_B) in case of a read access:
If a master-read transfer is started (determined by the LSB of the address byte = 1), the transfer direction of SDA changes and the slave will actively drive the data line. In this case, only the codes 010_B and 011_B are valid. To abort the transfer in case of a wrong code, a dummy read must be performed by the master before the STOP condition can be generated.

Universal Serial Interface Channel

- TDF code after a start (100_B) or repeated start code (101_B) in case of a write access:
If a master-write transfer is started (determined by the LSB of the address byte = 0), the master still owns the SDA line. In this case, the transmit (000_B), repeated start (101_B) and stop (110_B) codes are valid. The other codes are considered as wrong. To abort the transfer in case of a wrong code, the STOP condition is generated immediately.
- TDF code of the third and subsequent command in case of a read access with acknowledged previous data byte:
If a master-read transfer is started (determined by the LSB of the address byte), the transfer direction of SDA changes and the slave will actively drive the data line. To force the slave to release the SDA line, the master has to not-acknowledge a byte transfer. In this case, only the receive codes 010_B and 011_B are valid. To abort the transfer in case of a wrong code, a dummy read must be performed by the master before the STOP condition can be generated.
- TDF code of the third and subsequent command in case of a read access with a not-acknowledged previous data byte:
If a master-read transfer is started (determined by the LSB of the address byte), the transfer direction of SDA changes and the slave will actively drive the data line. To force the slave to release the SDA line, the master has to not-acknowledge a byte transfer. In this case, only the restart (101_B) and stop code (110_B) are valid. To abort the transfer in case of a wrong code, the STOP condition is generated immediately.
- TDF code of the third and subsequent command in case of a write access:
If a master-write transfer is started (determined by the LSB of the address byte), the master still owns the SDA line. In this case, the transmit (000_B), repeated start (101_B) and stop (110_B) codes are valid. The other codes are considered as wrong. To abort the transfer in case of a wrong code, the STOP condition is generated immediately.
- After a master device has received a non-acknowledge from a slave device, a stop condition will be sent out automatically, except if the following TDF code requests a repeated start condition. In this case, the TDF code is taken into account, whereas all other TDF codes are ignored.

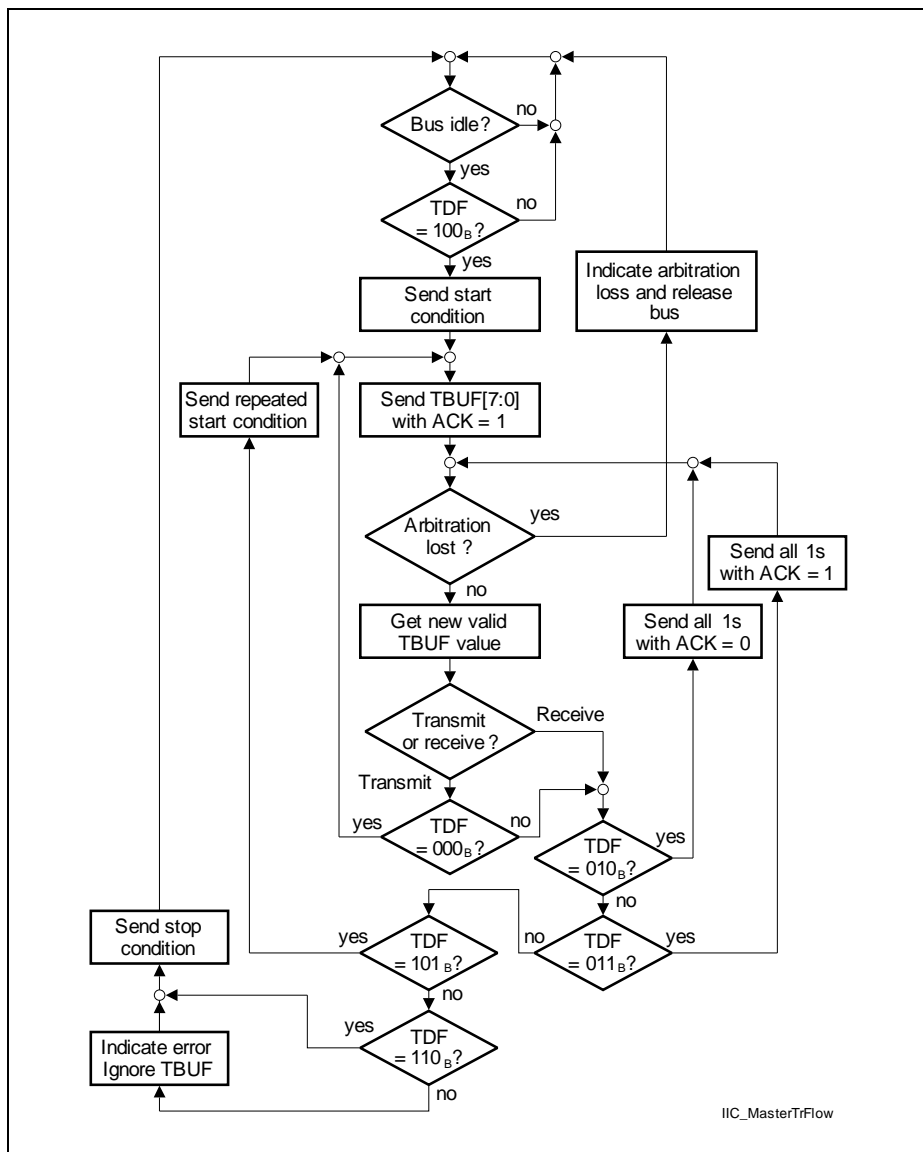


Figure 21-46 IIC Master Transmission

21.5.5 IIC Protocol Registers

In IIC mode, the registers PCRH, PCRL and PSR handle IIC related information.

21.5.5.1 IIC Protocol Control Registers

In IIC mode, the PCRL/PCRH register bits or bit fields are defined as described in this section.

PCRL

Protocol Control Register L [IIC Mode] (40_H)

Reset Value: 0000_H

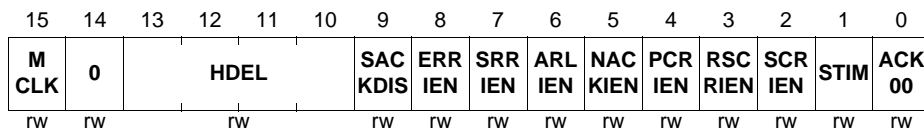


Field	Bits	Type	Description
SLAD	[15:0]	rw	Slave Address This bit field contains the programmed slave address. The corresponding bits in the first received address byte are compared to the bits SLAD[15:9] to check for address match. If SLAD[15:11] = 11110 _B , then the second address byte is also compared to SLAD[7:0].

PCRH

Protocol Control Register H [IIC Mode] (42_H)

Reset Value: 0000_H



Field	Bits	Type	Description
ACK00	0	rw	Acknowledge 00_H This bit defines if a slave device should be sensitive to the slave address 00 _H . 0 _B The slave device is not sensitive to this address. 1 _B The slave device is sensitive to this address.

Field	Bits	Type	Description
STIM	1	rw	Symbol Timing This bit defines how many time quanta are used in a symbol. 0 _B A symbol contains 10 time quanta. The timing is adapted for standard mode (100 kBaud). 1 _B A symbol contains 25 time quanta. The timing is adapted for fast mode (400 kBaud).
SCRIEN	2	rw	Start Condition Received Interrupt Enable This bit enables the generation of a protocol interrupt if a start condition is detected. 0 _B The start condition interrupt is disabled. 1 _B The start condition interrupt is enabled.
RSCRIEN	3	rw	Repeated Start Condition Received Interrupt Enable This bit enables the generation of a protocol interrupt if a repeated start condition is detected. 0 _B The repeated start condition interrupt is disabled. 1 _B The repeated start condition interrupt is enabled.
PCRIEN	4	rw	Stop Condition Received Interrupt Enable This bit enables the generation of a protocol interrupt if a stop condition is detected. 0 _B The stop condition interrupt is disabled. 1 _B The stop condition interrupt is enabled.
NACKIEN	5	rw	Acknowledge Not Received Interrupt Enable This bit enables the generation of a protocol interrupt if a missing acknowledge is detected by a master. 0 _B The acknowledge missing interrupt is disabled. 1 _B The acknowledge missing interrupt is enabled.
ARLIEN	6	rw	Arbitration Lost Interrupt Enable This bit enables the generation of a protocol interrupt if an arbitration lost event is detected. 0 _B The arbitration lost interrupt is disabled. 1 _B The arbitration lost interrupt is enabled.
SRRIEN	7	rw	Slave Read Request Interrupt Enable This bit enables the generation of a protocol interrupt if a slave read request is detected. 0 _B The slave read request interrupt is disabled. 1 _B The slave read request interrupt is enabled.

Field	Bits	Type	Description
ERRIEN	8	rw	Error Interrupt Enable This bit enables the generation of a protocol interrupt if an IIC error condition is detected (indicated by PSR.ERR or PSR.WTDF). 0 _B The error interrupt is disabled. 1 _B The error interrupt is enabled.
SACKDIS	9	rw	Slave Acknowledge Disable This bit disables the generation of an active acknowledge signal for a slave device (active acknowledge = 0 level). Once set by software, it is automatically cleared with each (repeated) start condition. If this bit is set after a byte has been received (indicated by an interrupt) but before the next acknowledge bit has started, the next acknowledge bit will be sent with passive level. This would indicate that the receiver does not accept more bytes. As a result, a minimum of 2 bytes will be received if the first receive interrupt is used to set this bit. 0 _B The generation of an active slave acknowledge is enabled (slave acknowledge with 0 level = more bytes can be received). 1 _B The generation of an active slave acknowledge is disabled (slave acknowledge with 1 level = reception stopped).
HDEL	[13:10]	rw	Hardware Delay This bit field defines the delay used to compensate the internal treatment of the SCL signal (see Page 21-171) in order to respect the SDA hold time specified for the IIC protocol.
0	14	rw	Reserved Returns 0 if read; should be written with 0.
MCLK	15	rw	Master Clock Enable This bit enables generation of the master clock MCLK (not directly used for IIC protocol, can be used as general frequency output). 0 _B The MCLK generation is disabled and MCLK is 0. 1 _B The MCLK generation is enabled.

21.5.5.2 IIC Protocol Status Register

The following PSR status bits or bit fields are available in IIC mode. Please note that the bits in register PSR are not cleared by hardware.

The flags in the PSR register can be cleared by writing a 1 to the corresponding bit position in register PSCR. Writing a 1 to a bit position in PSR sets the corresponding flag, but doesn't lead to further actions (no interrupt generation). Writing a 0 has no effect. These flags should be cleared by software before enabling a new protocol.

PSR

Protocol Status Register [IIC Mode] (44_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AIF	RIF	TBIF	TSIF	DLIF	RSIF	0	ERR	SRR	ARL	N ACK	PCR	R SCR	SCR	W TDF	SL SEL
rwh	rwh	rwh	rwh	rwh	rwh	r	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
SLSEL	0	rwh	Slave Select This bit indicates that this device has been selected as slave. 0 _B The device is not selected as slave. 1 _B The device is selected as slave.
WTDF	1	rwh	Wrong TDF Code Found¹⁾ This bit indicates that an unexpected/wrong TDF code has been found. A protocol interrupt can be generated if PCRH.ERRIEN = 1. 0 _B A wrong TDF code has not been found. 1 _B A wrong TDF code has been found.
SCR	2	rwh	Start Condition Received¹⁾ This bit indicates that a start condition has been detected on the IIC bus lines. A protocol interrupt can be generated if PCRH.SCRIEN = 1. 0 _B A start condition has not yet been detected. 1 _B A start condition has been detected.

Field	Bits	Type	Description
RSCR	3	rwh	Repeated Start Condition Received¹⁾ This bit indicates that a repeated start condition has been detected on the IIC bus lines. A protocol interrupt can be generated if PCRH.RSCRIEN = 1. 0 _B A repeated start condition has not yet been detected. 1 _B A repeated start condition has been detected.
PCR	4	rwh	Stop Condition Received¹⁾ This bit indicates that a stop condition has been detected on the IIC bus lines. A protocol interrupt can be generated if PCRH.PCRIEN = 1. 0 _B A stop condition has not yet been detected. 1 _B A stop condition has been detected.
NACK	5	rwh	Acknowledge Not Received¹⁾ This bit indicates that an acknowledge has not been received in master mode. This bit is not set in slave mode. A protocol interrupt can be generated if PCRH.NACKIEN = 1. 0 _B An acknowledge has been received. 1 _B An acknowledge has not been received.
ARL	6	rwh	Arbitration Lost¹⁾ This bit indicates that an arbitration has been lost. A protocol interrupt can be generated if PCRH.ARLIEN = 1. 0 _B An arbitration has not been lost. 1 _B An arbitration has been lost.
SRR	7	rwh	Slave Read Request¹⁾ This bit indicates that a slave read request has been detected. It becomes active to request the first data byte to be made available in the transmit buffer. For further consecutive data bytes, the transmit buffer issues more interrupts. For the end of the transfer, the master transmitter sends a stop condition. A protocol interrupt can be generated if PCRH.SRRIEN = 1. 0 _B A slave read request has not been detected. 1 _B A slave read request has been detected.

Universal Serial Interface Channel

Field	Bits	Type	Description
ERR	8	rwh	Error¹⁾ This bit indicates that an IIC error (frame format or TDF code) has been detected. A protocol interrupt can be generated if PCRH.ERRIEN = 1. 0 _B An IIC error has not been detected. 1 _B An IIC error has been detected.
0	9	r	Reserved Returns 0 if read; not modified in IIC mode.
RSIF	10	rwh	Receiver Start Indication Flag 0 _B A receiver start event has not occurred. 1 _B A receiver start event has occurred.
DLIF	11	rwh	Data Lost Indication Flag 0 _B A data lost event has not occurred. 1 _B A data lost event has occurred.
TSIF	12	rwh	Transmit Shift Indication Flag 0 _B A transmit shift event has not occurred. 1 _B A transmit shift event has occurred.
TBIF	13	rwh	Transmit Buffer Indication Flag 0 _B A transmit buffer event has not occurred. 1 _B A transmit buffer event has occurred.
RIF	14	rwh	Receive Indication Flag 0 _B A receive event has not occurred. 1 _B A receive event has occurred.
AIF	15	rwh	Alternative Receive Indication Flag 0 _B An alternative receive event has not occurred. 1 _B An alternative receive event has occurred.

1) This status bit can generate a protocol interrupt (see [Page 21-24](#)). The general interrupt status flags are described in the general interrupt chapter.

21.6 IIS Protocol

This chapter describes how the USIC module handles the IIS protocol. This serial protocol can handle reception and transmission of synchronous data frames between a device operating in master mode and a device in slave mode. An IIS connection based on a USIC communication channel supports half-duplex and full-duplex data transfers. The IIS mode is selected by $CCR.MODE = 0011_B$ with $CCFG.IIS = 1$ (IIS mode is available).

This chapter contains the following sections:

- Introduction (see [Page 21-185](#))
- General IIS issues (see [Page 21-189](#))
- Master mode operation (see [Page 21-194](#))
- Slave mode operation (see [Page 21-198](#))
- Protocol registers (see [Page 21-199](#))

21.6.1 Introduction

The IIS protocol is a synchronous serial communication protocol mainly for audio and infotainment applications and refers to the Philips specification, 1986, revised June 5, 1996.

21.6.1.1 Signal Description

A connection between an IIS master and an IIS slave is based on the following signals:

- A shift clock signal SCK, generated by the transfer master. It is permanently generated while an IIS connection is established, also while no valid data bits are transferred.
- A word address signal WA (also named WS), generated by the transfer master. It indicates the beginning of a new data word and the targeted audio channel (e.g. left/right). The word address output signal WA is available on all SELOx outputs if the WA generation is enabled (by $PCR.WAGEN = 1$ for the transfer master). The WA signal changes synchronously to the falling edges of the shift clock.
- If the transmitter is the IIS master device, it generates a master transmit slave receive data signal. The data changes synchronously to the falling edges of the shift clock.
- If the transmitter is the IIS slave device, it generates a master receive slave transmit data signal. The data changes synchronously to the falling edges of the shift clock.

The transmitter part and the receiver part of the USIC communication channel can be used together to establish a full-duplex data connection between an IIS master and a slave device.

Table 21-10 IIS IO Signals

IIS Mode	Receive Data	Transmit Data	Shift Clock	Word Address
Master	Input DIN, handled by DX0	Output DOUT	Output SCLKOUT	Output(s) SELOx
Slave	Input DIN, handled by DX0	Output DOUT	Input SCLKIN, handled by DX1	Input SELIN, handled by DX2

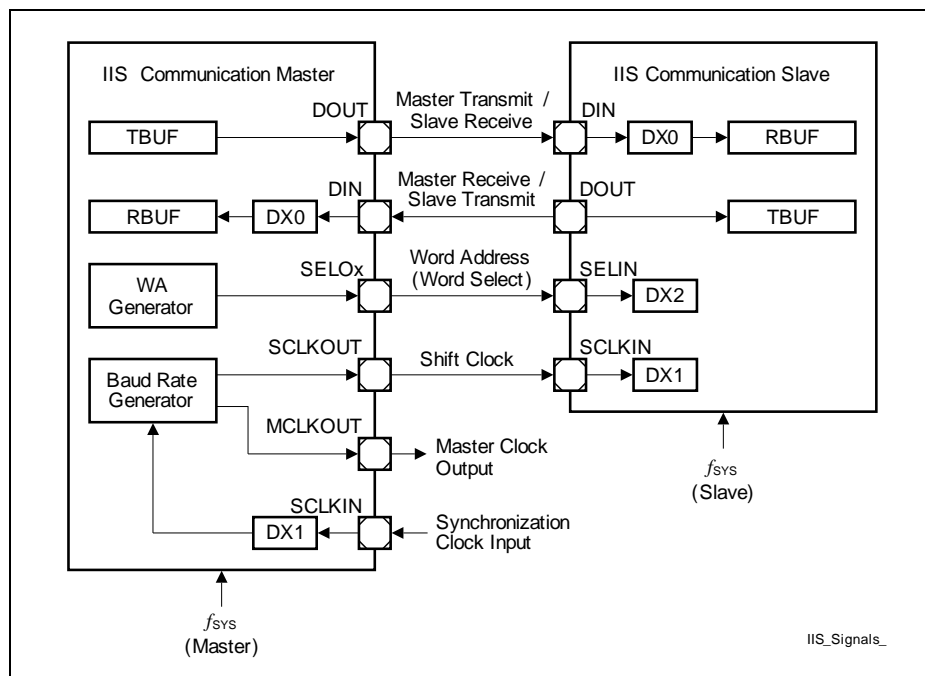


Figure 21-47 IIS Signals

Two additional signals are available for the USIC IIS communication master:

- A master clock output signal **MCLKOUT** with a fixed phase relation to the shift clock to support oversampling for audio components. It can also be used as master clock output of a communication network with synchronized IIS connections.
- A synchronization clock input **SCLKIN** for synchronization of the shift clock generation to an external frequency to support audio frequencies that can not be directly derived from the system clock f_{sys} of the communication master. It can be used as master clock input of a communication network with synchronized IIS connections.

21.6.1.2 Protocol Overview

An IIS connection supports transfers for two different data frames via the same data line, e.g. a data frames for the left audio channel and a data frame for the right audio channel. The word address signal WA is used to distinguish between the different data frames. Each data frame can consist of several data words.

In a USIC communication channel, data words are tagged for being transmitted for the left or for the right channel. Also the received data words contain a tag identifying the WA state when the data has been received.

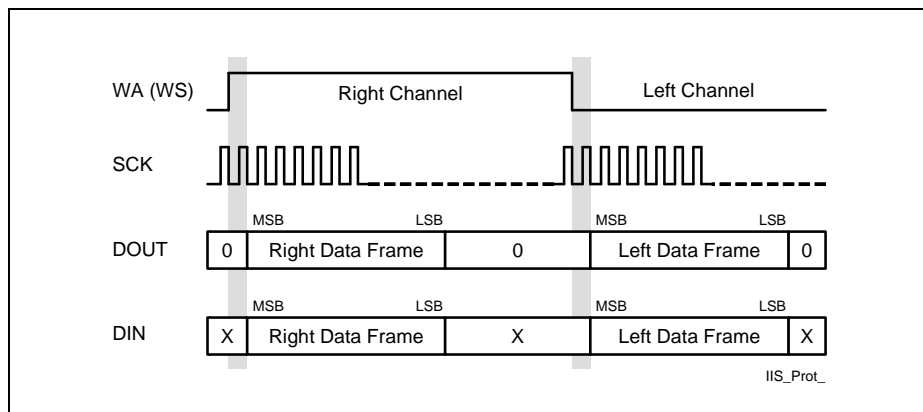


Figure 21-48 Protocol Overview

21.6.1.3 Transfer Delay

The transfer delay feature allows the transfer of data (transmission and reception) with a programmable delay (counted in shift clock periods).

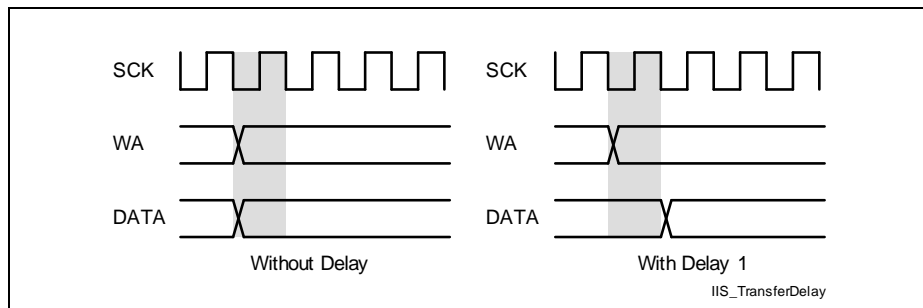


Figure 21-49 Transfer Delay for IIS

21.6.1.4 Connection of External Audio Components

The IIS signals can be used to communicate with external audio devices (such as Codecs) or other audio data sources/destinations.

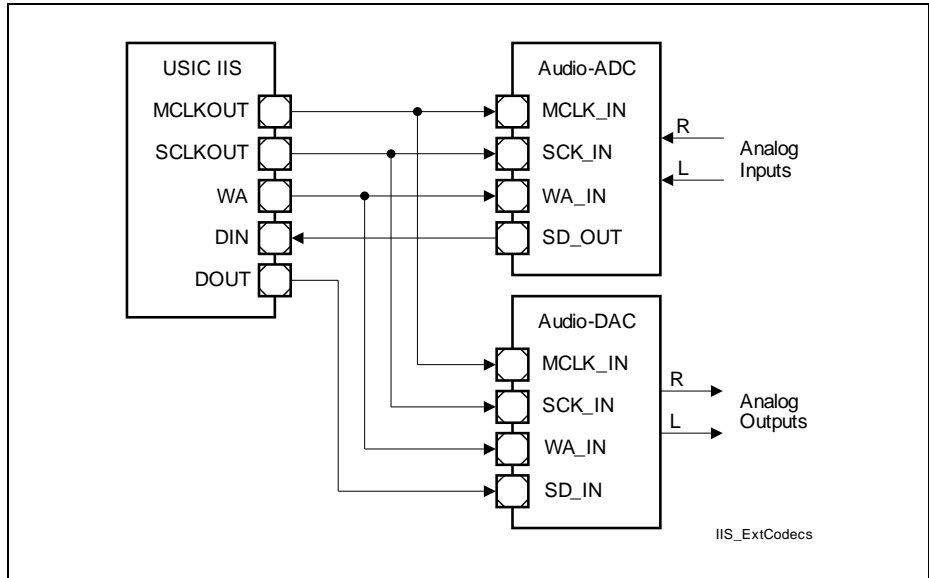


Figure 21-50 Connection of External Audio Devices

In some applications, especially for Audio-ADCs or Audio-DACs, a master clock signal is required with a fixed phase relation to the shift clock signal. The frequency of MCLKOUT is a multiple of the shift frequency SCLKOUT. This factor defines the oversampling factor of the external device (commonly used values: 256 or 384).

21.6.2 Operating the IIS

This chapter contains IIS issues, that are of general interest and not directly linked to master mode or slave mode.

21.6.2.1 Frame Length and Word Length Configuration

After each change of the WA signal, a complete data frame is intended to be transferred (frame length \leq system word length). The number of data bits transferred after a change of signal WA is defined by SCTR.H.FLE. A data frame can consist of several data words with a data word length defined by SCTR.H.WLE. The changes of signal WA define the system word length as the number of SCLK cycles between two changes of WA (number of bits available for the right channel and same number available for the left channel).

If the system word length is longer than the frame length defined by SCTR.H.FLE, the additional bits are transmitted with passive data level (SCTR.L.PDL). If the system word length is smaller than the device frame length, not all LSBs of the transmit data can be transferred.

It is recommended to program bits WLEMD, FLEMD and SELMD in register TCSRL to 0.

21.6.2.2 Automatic Shadow Mechanism

The baud rate and shift control setting are internally kept constant while a data frame is transferred by an automatic shadow mechanism. The registers can be programmed all the time with new settings that are taken into account for the next data frame. During a data frame, the applied (shadowed) setting is not changed, although new values have been written after the start of the data frame. The setting is internally "frozen" with the start of each data frame.

Although this shadow mechanism being implemented, it is recommended to change the baud rate and shift control setting only while the IIS protocol is switched off.

21.6.2.3 Mode Control Behavior

In IIS mode, the following kernel modes are supported:

- Run Mode 0/1:
Behavior as programmed, no impact on data transfers.
- Stop Mode 0/1:
Bit PCRL.WAGEN is internally considered as 0 (the bit itself is not changed). If WAGEN = 1, then the current system word cycle is finished and then the WA generation is stopped, but PSR.END is not set. The complete data frame is finished before entering stop mode, including a possible delay due to PCR.H.TDEL.
When leaving a stop mode with WAGEN = 1, the WA generation starts from the beginning.

21.6.2.4 Transfer Delay

The transfer delay can be used to synchronize a data transfer to an event (e.g. a change of the WA signal). This event has to be synchronously generated to the falling edge of the shift clock SCK (like the change of the transmit data), because the input signal for the event is directly sampled in the receiver (as a result, the transmitter can use the detection information with its next edge).

Event signals that are asynchronous to the shift clock while the shift clock is running must not be used. In the example in [Figure 21-49](#), the event (change of signal WA) is generated by the transfer master and as a result, is synchronous to the shift clock SCK. With the rising edge of SCK, signal WA is sampled and checked for a change. If a change is detected, a transfer delay counter TDC is automatically loaded with its programmable reload value (PCR.H.TDEL), otherwise it is decremented with each rising edge of SCK until it reaches 0, where it stops. The transfer itself is started if the value of TDC has become 0. This can happen under two conditions:

- TDC is reloaded with a PCR.H.TDEL = 0 when the event is detected
- TDC has reached 0 while counting down

The transfer delay counter is internal to the IIS protocol pre-processor and can not be observed by software. The transfer delay in SCK cycles is given by PCR.H.TDEL+1.

In the example in [Figure 21-51](#), the reload value PCR.H.TDEL for TDC is 0. When the samples taken on receiver side show the change of the WA signal, the counter TDC is reloaded. If the reload value is 0, the data transfer starts with 1 shift clock cycle delay compared to the change of WA.

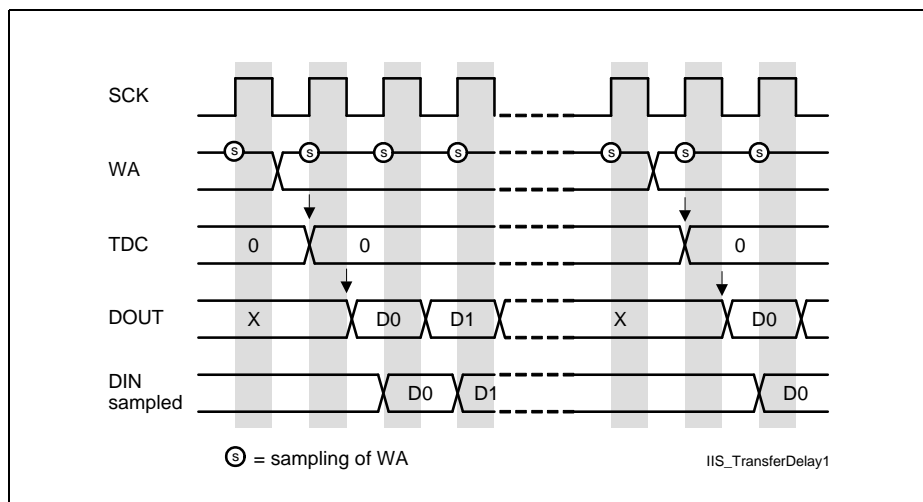


Figure 21-51 Transfer Delay with Delay 1

Universal Serial Interface Channel

The ideal case without any transfer delay is shown in **Figure 21-52**. The WA signal changes and the data output value become valid at the same time. This implies that the transmitter “knows” in advance that the event signal will change with the next rising edge of TCLK. This is achieved by delaying the data transmission after the previously detected WA change the system word length minus 1.

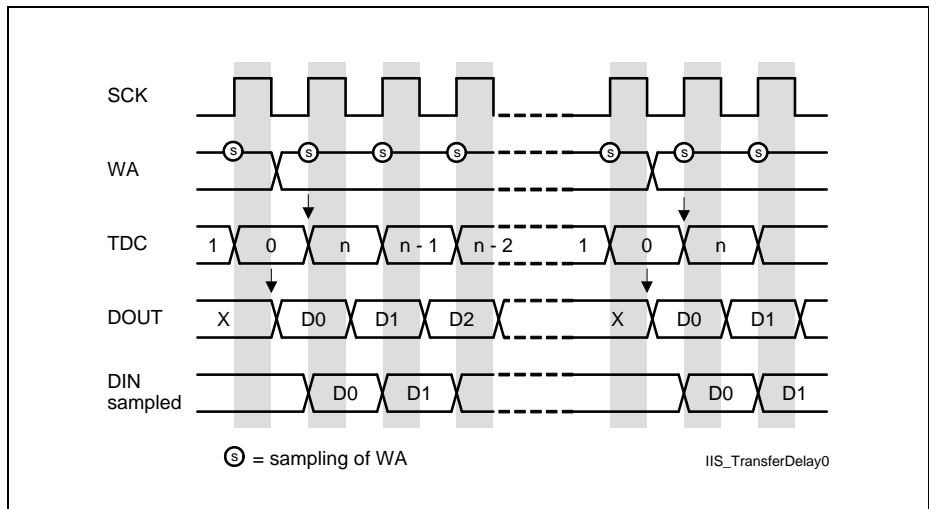


Figure 21-52 Transfer Delay with 0 Delay

If the end of the transfer delay is detected simultaneously to change of WA, the transfer is started and the delay counter is reloaded with PCRH.TDEL. This allows to run the USIC as IIS device without any delay. In this case, internally the delay from the previous event elapses just at the moment when a new event occurs. If PCRH.TDEL is set to a value bigger than the system word length, no transfer takes place.

21.6.2.5 Parity Mode

Parity generation is not supported in IIS mode and bit field CCR.PM = 00_B has to be programmed.

21.6.2.6 Transfer Mode

In IIS mode, bit field SCTRL.TRM = 11_B has to be programmed to allow data transfers. Setting SCTRL.TRM = 00_B disables and stops the data transfer immediately.

21.6.2.7 Data Transfer Interrupt Handling

The data transfer interrupts indicate events related to IIS frame handling.

- **Transmit buffer interrupt TBI:**
 Bit PSR.TBIF is set after the start of first data bit of a data word.
- **Transmit shift interrupt TSI:**
 Bit PSR.TSIF is set after the start of the last data bit of a data word.
- **Receiver start interrupt RSI:**
 Bit PSR.RSIF is set after the reception of the first data bit of a data word.
 With this event, bit TCSRL.TDV is cleared and new data can be loaded to the transmit buffer.
- **Receiver interrupt RI and alternative interrupt AI:**
 Bit PSR.RIF is set at after the reception of the last data bit of a data word with WA = 0.
 Bit RBUFSR.SOF indicates whether the received data word has been the first data word of a new data frame.
 Bit PSR.AIF is set at after the reception of the last data bit of a data word with WA = 1.
 Bit RBUFSR.SOF indicates whether the received data word has been the first data word of a new data frame.

21.6.2.8 Protocol-Related Argument and Error

In order to distinguish between data words received for the left or the right channel, the IIS protocol pre-processor samples the level of the WA input (just after the WA transition) and propagates it as protocol-related error (although it is not an error, but an indication) to the receive buffer status register at the bit position RBUFSR[9]. This bit position defines if either a standard receive interrupt (if RBUFSR[9] = 0) or an alternative receive interrupt (if RBUFSR[9] = 1) becomes activated when a new data word has been received. Incoming data can be handled by different interrupts or DMA mechanisms for the left and the right channel if the corresponding events are directed to different interrupt nodes. Flag PAR is always 0.

21.6.2.9 Transmit Data Handling

The IIS protocol pre-processor allows to distinguish between the left and the right channel for data transmission. Therefore, bit TCSRL.WA indicates on which channel the data in the buffer will be transmitted. If TCSRL.WA = 0, the data will be transmitted after a falling edge of WA. If TCSRL.WA = 1, the data will be transmitted after a rising edge of WA. The WA value sampled after the WA transition is considered to distinguish between both channels (referring to PSR.WA).

Bit TCSRL.WA can be automatically updated by the transmit control information TCI[4] for each data word if TCSRL.WAMD = 1. In this case, data written to TBUF[15:0] (or IN[15:0] if a FIFO data buffer is used) is considered as left channel data, whereas data

written to TBUF[31:16] (or IN[31:16] if a FIFO data buffer is used) is considered as right channel data.

21.6.2.10 Receive Buffer Handling

If a receive FIFO buffer is available (CCFG.RB = 1) and enabled for data handling (RBCTRH.SIZE > 0), it is recommended to set RBCTRH.RCIM = 11_B in IIS mode. This leads to an indication that the data word has been the first data word of a new data frame if bit OUTRH.RCI[0] = 1, and the channel indication by the sampled WA value is given by OUTRH.RCI[4].

The standard receive buffer event and the alternative receive buffer event can be used for the following operation in RCI mode (RBCTRH.RNM = 1):

- A standard receive buffer event indicates that a data word can be read from OUTRL that belongs to a data frame started when WA = 0.
- An alternative receive buffer event indicates that a data word can be read from OUTRL that belongs to a data frame started when WA = 1.

21.6.2.11 Loop-Delay Compensation

The synchronous signaling mechanism of the IIS protocol being similar to the one of the SSC protocol, the closed-loop delay has to be taken into account for the application setup. In IIS mode, loop-delay compensation in master mode is also possible to achieve higher baud rates.

Please refer to the more detailed description in the SSC chapter.

21.6.3 Operating the IIS in Master Mode

In order to operate the IIS in master mode, the following issues have to be considered:

- **Select IIS mode:**
 It is recommended to configure all parameters of the IIS that do not change during run time while $CCR.MODE = 0000_B$. Bit field $SCTRL.TRM = 11_B$ has to be programmed. The configuration of the input stages has to be done while $CCR.MODE = 0000_B$ to avoid unintended edges of the input signals and the IIS mode can be enabled by $CCR.MODE = 0011_B$ afterwards.
- **Pin connection for data transfer:**
 Establish a connection of input stage DX0 with the selected receive data input pin (DIN) with $DX0CR.INSW = 1$. Configure a transmit data output pin (DOUT) for a transmitter.
 The data shift unit allowing full-duplex data transfers based on the same WA signal, the values delivered by the DX0 stage are considered as data bits (receive function can not be disabled independently from the transmitter). To receive IIS data, the transmitter does not necessarily need to be configured (no assignment of DOUT signal to a pin).
- **Baud rate generation:**
 The desired baud rate setting has to be selected, comprising the fractional divider and the baud rate generator. Bit $DX1CR.INSW = 0$ has to be programmed to use the baud rate generator output SCLK directly as input for the data shift unit. Configure a shift clock output pin with the inverted signal SCLKOUT without additional delay ($BRGH.SCLKCFG = 01_B$).
- **Word address WA generation:**
 The WA generation has to be enabled by setting $PCRL.WAGEN = 1$ and the programming of the number of shift clock cycles between the changes of WA. Bit $DX2CR.INSW = 0$ has to be programmed to use the WA generator as input for the data shift unit. Configure WA output pin for signal SELOx if needed.
- **Data format configuration:**
 The word length, the frame length, and the shift direction have to be set up according to the application requirements by programming the registers SCTRL and SCTR. Generally, the MSB is shifted first ($SCTRL.SDIR = 1$).
 Bit $TCSRL.WAMD$ can be set to use the transmit control information $TCI[4]$ to distinguish the data words for transmission while $WA = 0$ or while $WA = 1$.

21.6.3.1 Baud Rate Generation

The baud rate is defined by the frequency of the SCLK signal (one period of f_{SCLK} represents one data bit).

If the fractional divider mode is used to generate f_{PIN} , there can be an uncertainty of one period of f_{SYS} for f_{PIN} . This uncertainty does not accumulate over several SCLK cycles.

As a consequence, the average frequency is reached, whereas the duty cycle of 50% of the SCLK and MCLK signals can vary by one period of f_{SYS} .

In IIS applications, where the phase relation between the optional MCLK output signal and SCLK is not relevant, SCLK can be based on the frequency f_{PIN} (BRGL.PPPEN = 0). In the case that a fixed phase relation between the MCLK signal and SCLK is required (e.g. when using MCLK as clock reference for external devices), the additional divider by 2 stage has to be taken into account (BRGL.PPPEN = 1). This division is due to the fact that signal MCLK toggles with each cycle of f_{PIN} . Signal SCLK is then based on signal MCLK, see **Figure 21-53**.

The adjustable integer divider factor is defined by bit field BRGH.PDIV.

$$\begin{aligned} f_{\text{SCLK}} &= \frac{f_{\text{PIN}}}{2} \times \frac{1}{\text{PDIV} + 1} && \text{if PPPEN} = 0 \\ f_{\text{SCLK}} &= \frac{f_{\text{PIN}}}{2 \times 2} \times \frac{1}{\text{PDIV} + 1} && \text{if PPPEN} = 1 \end{aligned} \quad (21.12)$$

Note: In the IIS protocol, the master (unit generating the shift clock and the WA signal) changes the status of its data and WA output line with the falling edge of SCK. The slave transmitter also has to transmit on falling edges. The sampling of the received data is done with the rising edges of SCLK. The input stage DX1 and the SCLKOUT have to be programmed to invert the shift clock signal to fit to the internal signals.

21.6.3.2 WA Generation

The word address (or word select) line WA regularly toggles after N cycles of signal SCLK. The time between the changes of WA is called system word length and can be programmed by using the following bit fields.

In IIS master mode, the system word length is defined by:

- BRGL.CTQSEL = 10_B
to base the WA toggling on SCLK
- BRGL.PCTQ
to define the number N of SCLK cycles per system word length
- BRGL.DCTQ
to define the number N of SCLK cycles per system word length

$$N = (\text{PCTQ} + 1) \times (\text{DCTQ} + 1) \quad (21.13)$$

21.6.3.3 Master Clock Output

The master clock signal MCLK can be generated by the master of the IIS transfer (BRGL.PPPEN = 1). It is used especially to connect external Codec devices. It can be configured by bit BRGH.MCLKCFG in its polarity to become the output signal MCLKOUT.

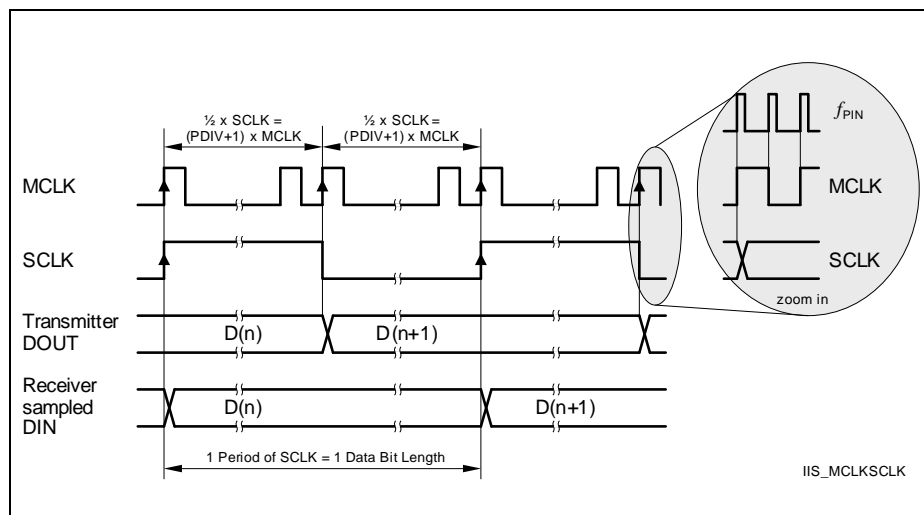


Figure 21-53 MCLK and SCLK for IIS

21.6.3.4 Protocol Interrupt Events

The following protocol-related events are generated in IIS mode and can lead to a protocol interrupt.

Please note that the bits in register PSR are not all automatically cleared by hardware and have to be cleared by software in order to monitor new incoming events.

- **WA rising/falling edge events:**
The WA generation block indicates two events that are monitored in register PSR. Flag PSR.WAFE is set with the falling edge, flag PSR.WARE with the rising edge of the WA signal. A protocol interrupt can be generated if PCRL.WAFEIEN = 1 for the falling edge, similar for PCRL.WAREIEN = 1 for a rising edge.
- **WA end event:**
The WA generation block also indicates when it has stopped the WA generation after it has been disabled by writing PCRL.WAGEN = 0. A protocol interrupt can be generated if PCRL.ENDIEN = 1.
- **DX2T event:**
An activation of the trigger signal DX2T is indicated by PSR.DX2TEV = 1 and can generate a protocol interrupt if PCRL.DX2TIEN = 1. This event can be evaluated instead of the WA rising/falling events if a delay compensation like in SSC mode (for details, refer to corresponding SSC section) is used.

21.6.4 Operating the IIS in Slave Mode

In order to operate the IIS in slave mode, the following issues have to be considered:

- **Select IIS mode:**
 It is recommended to configure all parameters of the IIS that do not change during run time while $CCR.MODE = 0000_B$. Bit field $SCTRL.TRM = 11_B$ has to be programmed. The configuration of the input stages has to be done while $CCR.MODE = 0000_B$ to avoid unintended edges of the input signals and the IIS mode can be enabled by $CCR.MODE = 0011_B$ afterwards.
- **Pin connection for data transfer:**
 Establish a connection of input stage DX0 with the selected receive data input pin (DIN) with $DX0CR.INSW = 1$. Configure a transmit data output pin (DOUT) for a transmitter.
 The data shift unit allowing full-duplex data transfers based on the same WA signal, the values delivered by the DX0 stage are considered as data bits (receive function can not be disabled independently from the transmitter). To receive IIS data, the transmitter does not necessarily need to be configured (no assignment of DOUT signal to a pin).
- **Pin connection for shift clock:**
 Establish a connection of input stage DX1 with the selected shift clock input pin (SCLKIN) with $DX1CR.INSW = 1$ and with inverted polarity ($DX1CR.DPOL = 1$).
- **Pin connection for WA input:**
 Establish a connection of input stage DX2 with the WA input pin (SELIN) with $DX2CR.INSW = 1$.
- **Baud rate generation:**
 The baud rate generator is not needed and can be switched off by the fractional divider.
- **WA generation:**
 The WA generation is not needed and can be switched off ($PCRL.WAGEN = 0$).

21.6.4.1 Protocol Events and Interrupts

The following protocol-related event is generated in IIS mode and can lead to a protocol interrupt.

Please note that the bits in register PSR are not all automatically cleared by hardware and have to be cleared by software in order to monitor new incoming events.

- **WA rising/falling/end events:**
 The WA generation being switched off, these events are not available.
- **DX2T event:**
 An activation of the trigger signal DX2T is indicated by $PSR.DX2TEV = 1$ and can generate a protocol interrupt if $PCRL.DX2TIEN = 1$.

21.6.5 IIS Protocol Registers

In IIS mode, the registers PCRL, PCRH and PSR handle IIS related information.

21.6.5.1 IIS Protocol Control Registers

In IIS mode, the PCRL/PCRH register bits or bit fields are defined as described in this section.

PCRL

Protocol Control Register L [IIS Mode]

(40_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DX2 TIEN					0				END IEN	WAR EIEN	WAF EIEN	0	SEL NV	DT EN	WAG EN
rw					rw				rw	rw	rw	r	rw	rw	rw

Field	Bits	Type	Description
WAGEN	0	rw	WA Generation Enable This bit enables/disables the generation of word address control output signal WA. 0 _B The IIS can be used as slave. The generation of the word address signal is disabled. The output signal WA is 0. The MCLKO signal generation depends on PCRH.MCLK. 1 _B The IIS can be used as master. The generation of the word address signal is enabled. The signal starts with a 0 after being enabled. The generation of MCLK is enabled, independent of PCRH.MCLK. After clearing WAGEN, the USIC module stops the generation of the WA signal within the next 4 WA periods.
DTEN	1	rw	Data Transfers Enable This bit enables/disables the transfer of IIS frames as a reaction to changes of the input word address control line WA. 0 _B The changes of the WA input signal are ignored and no transfers take place. 1 _B Transfers are enabled.

Field	Bits	Type	Description
SELINV	2	rw	Select Inversion This bit defines if the polarity of the SELOx outputs in relation to the internally generated word address signal WA. 0 _B The SELOx outputs have the same polarity as the WA signal. 1 _B The SELOx outputs have the inverted polarity to the WA signal.
WAFEIEN	4	rw	WA Falling Edge Interrupt Enable This bit enables/disables the activation of a protocol interrupt when a falling edge of WA has been generated. 0 _B A protocol interrupt is not activated if a falling edge of WA is generated. 1 _B A protocol interrupt is activated if a falling edge of WA is generated.
WAREIEN	5	rw	WA Rising Edge Interrupt Enable This bit enables/disables the activation of a protocol interrupt when a rising edge of WA has been generated. 0 _B A protocol interrupt is not activated if a rising edge of WA is generated. 1 _B A protocol interrupt is activated if a rising edge of WA is generated.
ENDIEN	6	rw	END Interrupt Enable This bit enables/disables the activation of a protocol interrupt when the WA generation stops after clearing PCR.WAGEN (complete system word length is processed before stopping). 0 _B A protocol interrupt is not activated. 1 _B A protocol interrupt is activated.
DX2TIEN	15	rw	DX2T Interrupt Enable This bit enables/disables the generation of a protocol interrupt if the DX2T signal becomes activated (indicated by PSR.DX2TEV = 1). 0 _B A protocol interrupt is not generated if DX2T is active. 1 _B A protocol interrupt is generated if DX2T is active.
0	3, [14:7]	rw	Reserved Returns 0 if read; should be written with 0;

PCRH

Protocol Control Register H [IIS Mode]

(42_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M					0							TDEL			
CLK															
rw					rw							rw			

Field	Bits	Type	Description
TDEL	[5:0]	rw	Transfer Delay This bit field defines the transfer delay when an event is detected. If bit field TDEL = 0, the additional delay functionality is switched off and a delay of one shift clock cycle is introduced.
0	[14:6]	rw	Reserved Returns 0 if read; should be written with 0.
MCLK	15	rw	Master Clock Enable This bit enables generation of the master clock MCLK (not directly used for IIC protocol, can be used as general frequency output). 0 _B The MCLK generation is disabled and MCLK is 0. 1 _B The MCLK generation is enabled.

21.6.5.2 IIS Protocol Status Register

The following PSR status bits or bit fields are available in IIS mode. Please note that the bits in register PSR are not cleared by hardware.

The flags in the PSR register can be cleared by writing a 1 to the corresponding bit position in register PSCR. Writing a 1 to a bit position in PSR sets the corresponding flag, but doesn't lead to further actions (no interrupt generation). Writing a 0 has no effect. These flags should be cleared by software before enabling a new protocol.

PSR

Protocol Status Register [IIS Mode] (44_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AIF	RIF	TBIF	TSIF	DLIF	RSIF		0		END	WA RE	WA FE	DX2 TEV	0	DX2 S	WA
rwh	rwh	rwh	rwh	rwh	rwh		r		rwh	rwh	rwh	rwh	r	rwh	rwh

Field	Bits	Type	Description
WA	0	rwh	Word Address This bit indicates the status of the WA input signal, sampled after a transition of WA has been detected. This information is forwarded to the corresponding bit position RBUF SR[9] to distinguish between data received for the right and the left channel. 0 _B WA has been sampled 0. 1 _B WA has been sampled 1.
DX2S	1	rwh	DX2S Status This bit indicates the current status of the DX2S signal, which is used as word address signal WA. 0 _B DX2S is 0. 1 _B DX2S is 1.
DX2TEV	3	rwh	DX2T Event Detected¹⁾ This bit indicates that the DX2T signal has been activated. In IIS slave mode, an activation of DX2T generates a protocol interrupt if PCRL.DX2TIEN = 1. 0 _B The DX2T signal has not been activated. 1 _B The DX2T signal has been activated.

Universal Serial Interface Channel

Field	Bits	Type	Description
WAFE	4	rwh	WA Falling Edge Event¹⁾ This bit indicates that a falling edge of the WA output signal has been generated. This event generates a protocol interrupt if PCRL.WAFEIEN = 1. 0 _B A WA falling edge has not been generated. 1 _B A WA falling edge has been generated.
WARE	5	rwh	WA Rising Edge Event¹⁾ This bit indicates that a rising edge of the WA output signal has been generated. This event generates a protocol interrupt if PCRL.WAREIEN = 1. 0 _B A WA rising edge has not been generated. 1 _B A WA rising edge has been generated.
END	6	rwh	WA Generation End¹⁾ This bit indicates that the WA generation has ended after clearing PCRL.WAGEN. This bit should be cleared by software before clearing WAGEN. 0 _B The WA generation has not yet ended (if it is running and WAGEN has been cleared). 1 _B The WA generation has ended (if it has been running).
RSIF	10	rwh	Receiver Start Indication Flag 0 _B A receiver start event has not occurred. 1 _B A receiver start event has occurred.
DLIF	11	rwh	Data Lost Indication Flag 0 _B A data lost event has not occurred. 1 _B A data lost event has occurred.
TSIF	12	rwh	Transmit Shift Indication Flag 0 _B A transmit shift event has not occurred. 1 _B A transmit shift event has occurred.
TBIF	13	rwh	Transmit Buffer Indication Flag 0 _B A transmit buffer event has not occurred. 1 _B A transmit buffer event has occurred.
RIF	14	rwh	Receive Indication Flag 0 _B A receive event has not occurred. 1 _B A receive event has occurred.
AIF	15	rwh	Alternative Receive Indication Flag 0 _B An alternative receive event has not occurred. 1 _B An alternative receive event has occurred.

Field	Bits	Type	Description
0	2, [9:7]	r	Reserved Returns 0 if read; not modified in IIS mode.

1) This status bit can generate a protocol interrupt (see [Page 21-24](#)). The general interrupt status flags are described in the general interrupt chapter.

21.7 USIC Implementation in XC27x8X

This section describes the implementation specific details of the USIC modules in the XC27x8X. It contains details about:

- Implementation Overview (see [Page 21-205](#))
- Channel Features (see [Page 21-206](#))
- Address Map (see [Page 21-207](#))
- Module Identification Registers (see [Page 21-208](#))
- Interrupt Control Registers (see [Page 21-210](#))
- Input/Output Connections (see [Page 21-212](#))
- USIC Module 0 I/O Lines (see [Page 21-213](#))
- USIC Module 1 I/O Lines (see [Page 21-216](#))
- USIC Module 2 I/O Lines (see [Page 21-219](#))
- USIC Module 3 I/O Lines (see [Page 21-222](#))
- USIC Module 4 I/O Lines (see [Page 21-224](#))

21.7.1 Implementation Overview

The XC27x8X device contains five identical USIC modules (USIC0, USIC1, USIC2, USIC3, and USIC4) with 2 communication channels each.

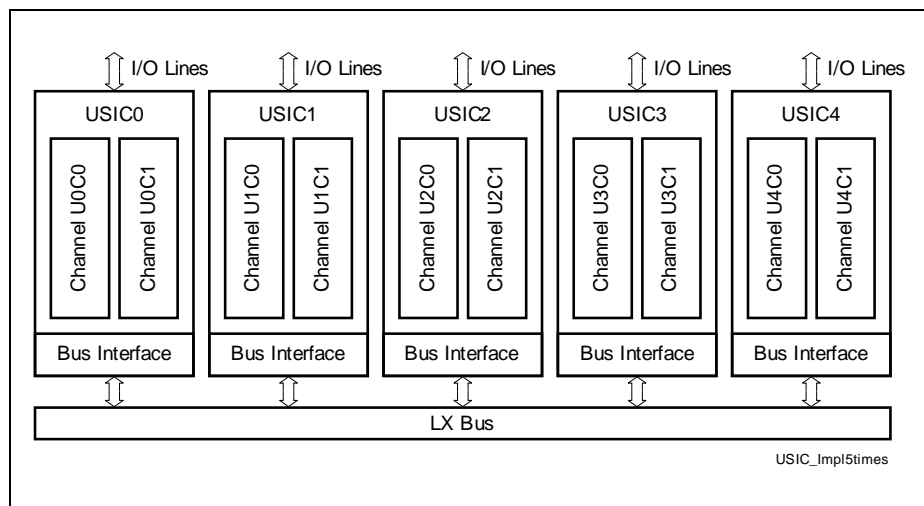


Figure 21-54 USIC Module Structure in XC27x8X

21.7.2 Channel Features

The USIC channels in the XC27x8X support the following functionality:

Table 21-11 USIC Module Feature Set

Channel	Protocol					FIFO Buffer Entries	SELOx ¹⁾		
	ASC	LIN support	SSC	IIC	IIS		100- Pins	144- Pins	176- Pins
U0C0	yes	yes	yes	yes	yes	64	5	8	8
U0C1	yes	yes	yes	yes	yes	shared	4	4	4
U1C0	yes	yes	yes	yes	yes	64	8	8	8
U1C1	yes	yes	yes	yes	yes	shared	5	5	5
U2C0	yes	yes	yes	yes	no ²⁾	64	2	6	6
U2C1	yes	yes	yes	yes	no ²⁾	shared	1	3	3
U3C0	yes	yes	yes	yes	yes	64	3	4	4
U3C1	yes	yes	yes	yes	yes	shared	0	2	2
U4C0	yes	yes	yes	yes	yes	64	0	2	2
U4C1	yes	yes	yes	yes	yes	shared	0	1	1

1) These are the maximum number of signals available in the 144-pin and 176-pin package.

2) The MCLKOUT signal is not available.

21.7.3 Address Map

The registers of the USIC communication channels are available at the following base addresses. The exact register address is given by the relative address of the register plus the channel base address (given in [Table 21-12](#)).

Note: No alternate address locations are available for the USIC module 4 (channels U4C0 and U4C1).

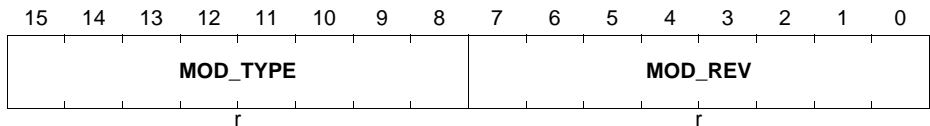
Table 21-12 Registers Address Space

Module	Base Address	End Address	Note
U0C0	204000 _H	2041FF _H	Standard locations
U0C1	204200 _H	2043FF _H	Standard locations
U1C0	204800 _H	2049FF _H	Standard locations
U1C1	204A00 _H	204BFF _H	Standard locations
U2C0	205000 _H	2051FF _H	Standard locations
U2C1	205200 _H	2053FF _H	Standard locations
U3C0	205800 _H	2059FF _H	Standard locations
U3C1	205A00 _H	205BFF _H	Standard locations
U4C0	206000 _H	2061FF _H	Standard locations
U4C1	206200 _H	2063FF _H	Standard locations
U0C0A	20B000 _H	20B1FF _H	Alternate locations
U0C1A	20B200 _H	20B3FF _H	Alternate locations
U1C0A	20B400 _H	20B5FF _H	Alternate locations
U1C1A	20B600 _H	20B7FF _H	Alternate locations
U2C0A	20B800 _H	20B9FF _H	Alternate locations
U2C1A	20BA00 _H	20BBFF _H	Alternate locations
U3C0A	20BC00 _H	20BDFF _H	Alternate locations
U3C1A	20BE00 _H	20BFFF _H	Alternate locations

21.7.4 Module Identification Registers

The module identification registers indicate the function and the design step of the USIC modules.

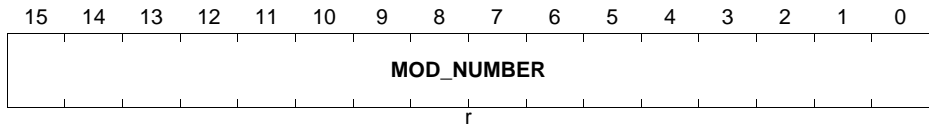
USIC0_IDL		
Module Identification Register L	(204008 _H)	Reset Value: C0XX _H
USIC1_IDL		
Module Identification Register L	(204808 _H)	Reset Value: C0XX _H
USIC2_IDL		
Module Identification Register L	(205008 _H)	Reset Value: C0XX _H
USIC3_IDL		
Module Identification Register L	(205808 _H)	Reset Value: C0XX _H
USIC4_IDL		
Module Identification Register L	(206008 _H)	Reset Value: C0XX _H
USIC0A_IDL		
Module Identification Register L	(20B008 _H)	Reset Value: C0XX _H
USIC1A_IDL		
Module Identification Register L	(20B408 _H)	Reset Value: C0XX _H
USIC2A_IDL		
Module Identification Register L	(20B808 _H)	Reset Value: C0XX _H
USIC3A_IDL		
Module Identification Register L	(20BC08 _H)	Reset Value: C0XX _H



Field	Bits	Type	Description
MOD_REV	[7:0]	r	Module Revision Number MOD_REV defines the revision number. The value of a module revision starts with 01 _H (first revision).
MOD_TYPE	[15:8]	r	Module Type This bit field is C0 _H . It defines the module as a 32-bit module.

Universal Serial Interface Channel

USIC0_IDH		
Module Identification Register H	(20400A_H)	Reset Value: 003A_H
USIC1_IDH		
Module Identification Register H	(20480A_H)	Reset Value: 003A_H
USIC2_IDH		
Module Identification Register H	(20500A_H)	Reset Value: 003A_H
USIC3_IDH		
Module Identification Register H	(20580A_H)	Reset Value: 003A_H
USIC4_IDH		
Module Identification Register H	(20600A_H)	Reset Value: 003A_H
USIC0A_IDH		
Module Identification Register H	(20B00A_H)	Reset Value: 003A_H
USIC1A_IDH		
Module Identification Register H	(20B40A_H)	Reset Value: 003A_H
USIC2A_IDH		
Module Identification Register H	(20B80A_H)	Reset Value: 003A_H
USIC3A_IDH		
Module Identification Register H	(20BC0A_H)	Reset Value: 003A_H



Field	Bits	Type	Description
MOD_NUMBER	[15:0]	r	Module Number Value This bit field defines the USIC module identification number (003A _H = USIC).

21.7.5 Interrupt Control Registers

Each USIC channel provides 4 service request outputs SR[3:0] (not all of them are necessarily connected to independent interrupt registers UxCy_nIC). [Table 21-13](#) shows the assignment of the service request outputs to the interrupt control registers.

Each USIC communication channel is connected to 3 dedicated interrupt control registers (connected to UxCy_SR[2:0], e.g. one for transmission, one for reception, the third one for protocol or error handling, or for the alternative receive events). A fourth interrupt control register per communication channel (connected to UxCy_SR3) is shared with module CC2.

The interrupt control registers are located in the SFR area. They are described in the general interrupt chapter.

Table 21-13 USIC Interrupt Control Registers

Service Request Output Line	Interrupt Control Register/Bit
SR0 of USIC0 channel 0	U0C0_0IC
SR1 of USIC0 channel 0	U0C0_1IC
SR2 of USIC0 channel 0	U0C0_2IC
SR3 of USIC0 channel 0	CC2_CC20IC, selected by ISSR.ISS4 CCU60_T13HRG
SR0 of USIC0 channel 1	U0C1_0IC
SR1 of USIC0 channel 1	U0C1_1IC
SR2 of USIC0 channel 1	U0C1_2IC
SR3 of USIC0 channel 1	CC2_CC21IC, selected by ISSR.ISS5
SR0 of USIC1 channel 0	U1C0_0IC
SR1 of USIC1 channel 0	U1C0_1IC
SR2 of USIC1 channel 0	U1C0_2IC
SR3 of USIC1 channel 0	CC2_CC22IC, selected by ISSR.ISS6 CCU61_T13HRG
SR0 of USIC1 channel 1	U1C1_0IC
SR1 of USIC1 channel 1	U1C1_1IC
SR2 of USIC1 channel 1	U1C1_2IC
SR3 of USIC1 channel 1	CC2_CC23IC, selected by ISSR.ISS7
SR0 of USIC2 channel 0	U2C0_0IC, selected by ISSR2.ISS6
SR1 of USIC2 channel 0	U2C0_1IC, selected by ISSR2.ISS7

Table 21-13 USIC Interrupt Control Registers (cont'd)

Service Request Output Line	Interrupt Control Register/Bit
SR2 of USIC2 channel 0	U2C0_2IC, selected by ISSR2.ISS8
SR3 of USIC2 channel 0	CC2_CC28IC, selected by ISSR.ISS12
	CCU62_T13HRG
SR0 of USIC2 channel 1	U2C1_0IC, selected by ISSR2.ISS9
SR1 of USIC2 channel 1	U2C1_1IC, selected by ISSR2.ISS10
SR2 of USIC2 channel 1	U2C1_2IC, selected by ISSR2.ISS11
SR3 of USIC2 channel 1	CC2_CC29IC, selected by ISSR.ISS13
SR0 of USIC3 channel 0	U3C0_0IC, selected by ISSR2.ISS12
SR1 of USIC3 channel 0	U3C0_1IC, selected by ISSR2.ISS13
SR2 of USIC3 channel 0	U3C0_2IC, selected by ISSR2.ISS14
SR3 of USIC3 channel 0	CC2_CC18IC, selected by ISSR.ISS2
	CCU63_T13HRG
SR0 of USIC3 channel 1	U3C1_0IC, selected by ISSR2.ISS15
SR1 of USIC3 channel 1	U3C1_1IC, selected by ISSR2.ISS1
SR2 of USIC3 channel 1	U3C1_2IC, selected by ISSR2.ISS1
SR3 of USIC3 channel 1	CC2_CC19IC, selected by ISSR.ISS3
SR0 of USIC4 channel 0	U4C0_0IC, selected by ISSR2.ISS1
SR1 of USIC4 channel 0	U4C0_1IC, selected by ISSR2.ISS2
SR2 of USIC4 channel 0	U4C0_2IC, selected by ISSR2.ISS3
SR3 of USIC4 channel 0	CC2_CC16IC, selected by ISSR.ISS0
	CCU62_T13HRH
SR0 of USIC4 channel 1	U4C1_0IC, selected by ISSR2.ISS4
SR1 of USIC4 channel 1	U4C1_1IC, selected by ISSR2.ISS5
SR2 of USIC4 channel 1	U4C1_2IC, selected by ISSR2.ISS5
SR3 of USIC4 channel 1	CC2_CC17IC, selected by ISSR.ISS1

21.7.6 Input/Output Connections

Figure 21-1 shows the I/O lines of one USIC channel. The tables in this section define the pin assignments and internal connections of the USIC channels I/O lines in the XC27x8X device. Naming convention: UxCy refers to USIC module x channel y.

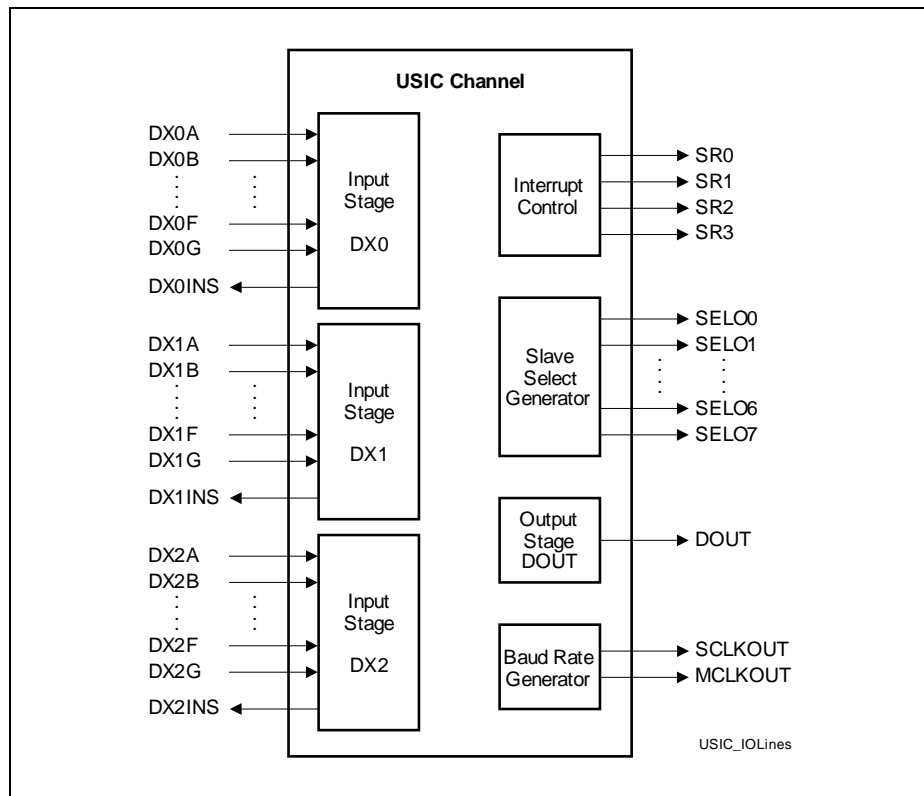


Figure 21-55 USIC Channel I/O Lines

The connections of the service request outputs SR[3:0] to the interrupt control registers are defined in [Table 21-13](#) on [Page 21-210](#).

21.7.6.1 USIC Module 0 I/O Lines

The signals of USIC module 0 have the prefix "U0C0_" for channel 0 and "U0C1_" for channel 1.

Table 21-14 I/O Connections of USIC0

Signal	Used as	From/To	
		Channel 0 – U0C0	Channel 1 – U0C1
Data Inputs			
DX0A	Shift data input	P10.0	P10.0
DX0B	Shift data input	P10.1	P10.7
DX0C	Shift data input	P10.6	P10.14
DX0D	Shift data input	P7.4	P2.3
DX0E	Shift data input	P2.3	P2.10
DX0F	Shift data input	P2.4	P7.3
DX0G	Loop back data shift input	U0C0_DOUT	U0C1_DOUT
Clock Inputs			
DX1A	Shift clock input	P10.1	P10.10
DX1B	Shift clock input	P10.2	P10.5
DX1C	Shift clock input	P10.8	P10.15
DX1D	Shift clock input	P2.5	P2.8
DX1E	Shift clock input	0	P7.4
DX1F	Input for single wire ASC collision detection	U0C0_DX0INS	U0C1_DX0INS
DX1G	Loop back shift clock input	U0C0_SCLKOUT	U0C1_SCLKOUT
Control Inputs			
DX2A	Shift control input	P10.3	P10.3
DX2B	Shift control input	P10.4	P10.4
DX2C	Shift control input	P10.10	P2.7
DX2D	Shift control input	P2.6	0
DX2E	Input for transmit data validation	CC24IO	RTC_T14INT
DX2F	Input for transmit data validation	CCU60_COUT63	CCU60_COUT63
DX2G	Loop back shift control input	U0C0_SELO0	U0C1_SELO0

Table 21-14 I/O Connections of USIC0 (cont'd)

Signal	Used as	From/To	
		Channel 0 – U0C0	Channel 1 – U0C1
Data Outputs			
DOUT	Shift data output	P2.3	P2.9
		P7.3	P2.10
		P10.1	P7.3
		P10.6	P7.4
		–	P10.0
		–	P10.7
		–	P10.14
		–	P10.15
		–	P4.3
		–	P2.4
Clock Outputs			
MCLKOUT	Master clock output, e.g. for IIS	P10.8	P10.9
SCLKOUT	Shift clock output	P2.5	P2.8
		P10.2	P7.4
		–	P10.5
Control Outputs			
SELO0	Shift control output 0	P2.6	P2.7
		P10.10	P10.8
SELO1	Shift control output 1	P2.7	P2.6
SELO2	Shift control output 2	P2.11	P2.11
SELO3	Shift control output 3	P2.10	P2.12
		P10.4	–
SELO4	Shift control output 5	P2.12	–
		P3.4	–
		P10.9	–
SELO5	Shift control output 5	P3.5	–
SELO6	Shift control output 6	P3.6	–
SELO7	Shift control output 7	P3.7	–

Table 21-14 I/O Connections of USIC0 (cont'd)

Signal	Used as	From/To	
		Channel 0 – U0C0	Channel 1 – U0C1
System Related Outputs			
DX0INS	External interrupt input for ERU	ERU_0A2	ERU_0B2
	Single wire ASC collision detection	U0C0_DX1F	U0C1_DX1F
DX1INS	–	–	–
DX2INS	External interrupt input for ERU	ERU_0A3	ERU_0B3
Loop Back Connections			
DOUT	Loop back shift data output	U0C0_DX0G	U0C1_DX0G
SCLKOUT	Loop back shift clock output	U0C0_DX1G	U0C1_DX1G
SELO0	Loop back shift control output	U0C0_DX2G	U0C1_DX2G

21.7.6.2 USIC Module 1 I/O Lines

The signals of USIC module 1 have the prefix "U1C0_" for channel 0 and "U1C1_" for channel 1.

Table 21-15 I/O Connections of USIC1

Signal	Used as	From/To	
		Channel 0 – U1C0	Channel 1 – U1C1
Data Inputs			
DX0A	Shift data input	P0.0	P0.6
DX0B	Shift data input	P0.1	P0.7
DX0C	Shift data input	P10.12	ESR1
DX0D	Shift data input	P10.13	ESR2
DX0E	Shift data input	ESR0	P6.0
DX0F	Shift data input	ESR1	CAN1INS
DX0G	Loop back data shift input	U1C0_DOUT	U1C1_DOUT
Clock Inputs			
DX1A	Shift clock input	P0.1	P0.5
DX1B	Shift clock input	P0.2	P0.6
DX1C	Shift clock input	P0.5	P6.2
DX1D	Shift clock input	P10.11	0
DX1E	Shift clock input	P10.12	0
DX1F	Input for single wire ASC collision detection	U1C0_DX0INS	U1C1_DX0INS
DX1G	Loop back shift clock input	U1C0_SCLKOUT	U1C1_SCLKOUT
Control Inputs			
DX2A	Shift control input	P0.3	P0.4
DX2B	Shift control input	ESR0	ESR1
DX2C	Shift control input	ESR1	ESR2
DX2D	Shift control input	P10.6	P6.3
DX2E	Input for transmit data validation	CC25IO	RTC_T14INT
DX2F	Input for transmit data validation	CCU61_COUT63	CCU61_COUT63
DX2G	Loop back shift control input	U1C0_SELO0	U1C1_SELO0

Table 21-15 I/O Connections of USIC1 (cont'd)

Signal	Used as	From/To	
		Channel 0 – U1C0	Channel 1 – U1C1
Data Outputs			
DOUT	Shift data output	P0.0	P0.6
		P0.1	P0.7
		P10.12	P6.1
		P10.13	P8.2
		P10.15	–
Clock Outputs			
MCLKOUT	Master clock output, e.g. for IIS	P1.0	P1.7
SCLKOUT	Shift clock output	P0.2	P0.5
		P10.11	P6.2
Control Outputs			
SELO0	Shift control output 0	P0.3	P0.4
		P10.6	P6.3
SELO1	Shift control output 1	P0.4	P0.3
		P10.14	–
SELO2	Shift control output 2	P0.5	P1.6
		P10.15	–
SELO3	Shift control output 3	P0.7	P1.5
		P10.13	–
SELO4	Shift control output 5	P1.0	P1.4
SELO5	Shift control output 5	P1.1	–
SELO6	Shift control output 6	P1.2	–
SELO7	Shift control output 7	P1.3	–
System Related Outputs			
DX0INS	External interrupt input for ERU	ERU_1A2	ERU_1B2
	Single wire ASC collision detection	U1C0_DX1F	U1C1_DX1F
DX1INS	External interrupt input for ERU	ERU_3B0	–
DX2INS	External interrupt input for ERU	ERU_1A3	ERU_1B3

Table 21-15 I/O Connections of USIC1 (cont'd)

Signal	Used as	From/To	
		Channel 0 – U1C0	Channel 1 – U1C1
Loop Back Connections			
DOUT	Loop back shift data output	U1C0_DX0G	U1C1_DX0G
SCLKOUT	Loop back shift clock output	U1C0_DX1G	U1C1_DX1G
SELO0	Loop back shift control output	U1C0_DX2G	U1C1_DX2G

21.7.6.3 USIC Module 2 I/O Lines

The signals of USIC module 2 have the prefix "U2C0_" for channel 0 and "U2C1_" for channel 1.

Table 21-16 I/O Connections of USIC2

Signal	Used as	From/To	
		Channel 0 – U2C0	Channel 1 – U2C1
Data Inputs			
DX0A	Shift data input	P3.0	P3.6
DX0B	Shift data input	P3.1	P3.7
DX0C	Shift data input	P1.5	P1.1
DX0D	Shift data input	P1.6	P1.2
DX0E	Shift data input	P9.5	ESR2
DX0F	Shift data input	P5.8	P5.10
DX0G	Loop back data shift input	U2C0_DOUT	U2C1_DOUT
Clock Inputs			
DX1A	Shift clock input	P3.0	P3.5
DX1B	Shift clock input	P3.2	P3.6
DX1C	Shift clock input	P1.7	P1.2
DX1D	Shift clock input	P9.7	0
DX1E	Shift clock input	0	0
DX1F	Input for single wire ASC collision detection	U2C0_DX0INS	U2C1_DX0INS
DX1G	Loop back shift clock input	U2C0_SCLKOUT	U2C1_SCLKOUT
Control Inputs			
DX2A	Shift control input	P3.3	P3.4
DX2B	Shift control input	P1.4	ESR2
DX2C	Shift control input	0	ESR1
DX2D	Shift control input	0	0
DX2E	Input for transmit data validation	CC26IO	RTC_T14INT
DX2F	Input for transmit data validation	CCU62_COUT63	CCU62_COUT63
DX2G	Loop back shift control input	U2C0_SELO0	U2C1_SELO0

Table 21-16 I/O Connections of USIC2 (cont'd)

Signal	Used as	From/To	
		Channel 0 – U2C0	Channel 1 – U2C1
Data Outputs			
DOUT	Shift data output	P3.0	P3.6
		P3.1	P3.7
		P1.6	P1.1
		P9.4	P10.8
		P9.5	–
		P10.5	–
Clock Outputs			
MCLKOUT	Master clock output, e.g. for IIS	–	–
SCLKOUT	Shift clock output	P3.2	P3.5
		P1.7	P1.2
Control Outputs			
SELO0	Shift control output 0	P3.3	P3.4
SELO1	Shift control output 1	P3.4	P3.3
SELO2	Shift control output 2	P3.5	P2.13
SELO3	Shift control output 3	P3.7	–
SELO4	Shift control output 4	P1.3	–
SELO5	Shift control output 5	P1.4	–
SELO6	Shift control output 6	–	–
SELO7	Shift control output 7	–	–
System Related Outputs			
DX0INS	External interrupt input for ERU	ERU_2A2	ERU_2B2
	Single wire ASC collision detection	U2C0_DX1F	U2C1_DX1F
DX1INS	External interrupt input for ERU	ERU_2B0	–
DX2INS	External interrupt input for ERU	ERU_2A3	ERU_2B3

Table 21-16 I/O Connections of USIC2 (cont'd)

Signal	Used as	From/To	
		Channel 0 – U2C0	Channel 1 – U2C1
Loop Back Connections			
DOUT	Loop back shift data output	U2C0_DX0G	U2C1_DX0G
SCLKOUT	Loop back shift clock output	U2C0_DX1G	U2C1_DX1G
SELO0	Loop back shift control output	U2C0_DX2G	U2C1_DX2G

21.7.6.4 USIC Module 3 I/O Lines

The signals of USIC module 3 have the prefix "U3C0_" for channel 0 and "U3C1_" for channel 1.

Table 21-17 I/O Connections of USIC3

Signal	Used as	From/To	
		Channel 0 – U3C0	Channel 1 – U3C1
Data Inputs			
DX0A	Shift data input	P10.3	P2.10
DX0B	Shift data input	P4.5	P11.4
DX0C	Shift data input	0	0
DX0D	Shift data input	0	P2.5
DX0E	Shift data input	0	0
DX0F	Shift data input	0	0
DX0G	Loop back data shift input	U3C0_DOUT	U3C1_DOUT
Clock Inputs			
DX1A	Shift clock input	P10.14	P11.0
DX1B	Shift clock input	P4.2	0
DX1C	Shift clock input	0	0
DX1D	Shift clock input	0	0
DX1E	Shift clock input	0	0
DX1F	Input for single wire ASC collision detection	U3C0_DX0INS	U3C1_DX0INS
DX1G	Loop back shift clock input	U3C0_SCLKOUT	U3C1_SCLKOUT
Control Inputs			
DX2A	Shift control input	P10.11	P11.1
DX2B	Shift control input	P10.2	P11.5
DX2C	Shift control input	P4.4	0
DX2D	Shift control input	0	0
DX2E	Input for transmit data validation	CC27IO	RTC_T14INT
DX2F	Input for transmit data validation	CCU63_COUT63	CCU63_COUT63
DX2G	Loop back shift control input	U3C0_SELO0	U3C1_SELO0

Table 21-17 I/O Connections of USIC3 (cont'd)

Signal	Used as	From/To	
		Channel 0 – U3C0	Channel 1 – U3C1
Data Outputs			
DOUT	Shift data output	P10.4	P2.11
		P4.5	P11.2
		P4.6	P11.4
Clock Outputs			
MCLKOUT	Master clock output, e.g. for IIS	–	–
SCLKOUT	Shift clock output	P10.14	P11.0
		P4.2	–
Control Outputs			
SELO0	Shift control output 0	P10.11	P11.1
SELO1	Shift control output 1	P10.2	P11.5
SELO2	Shift control output 2	P4.4	–
SELO3	Shift control output 3	P4.1	–
SELO4	Shift control output 4	–	–
SELO5	Shift control output 5	–	–
SELO6	Shift control output 6	–	–
SELO7	Shift control output 7	–	–
System Related Outputs			
DX0INS	External interrupt input for ERU	–	–
	Single wire ASC collision detection	U3C0_DX1F	U3C1_DX1F
DX1INS	External interrupt input for ERU	–	–
DX2INS	External interrupt input for ERU	–	–
Loop Back Connections			
DOUT	Loop back shift data output	U3C0_DX0G	U3C1_DX0G
SCLKOUT	Loop back shift clock output	U3C0_DX1G	U3C1_DX1G
SELO0	Loop back shift control output	U3C0_DX2G	U3C1_DX2G

21.7.6.5 USIC Module 4 I/O Lines

The signals of USIC module 4 have the prefix "U4C0_" for channel 0 and "U4C1_" for channel 1.

Table 21-18 I/O Connections of USIC4

Signal	Used as	From/To	
		Channel 0 – U4C0	Channel 1 – U4C1
Data Inputs			
DX0A	Shift data input	P2.12	P1.6
DX0B	Shift data input	0	0
DX0C	Shift data input	0	P7.0
DX0D	Shift data input	P2.7	P7.1
DX0E	Shift data input	P2.13	0
DX0F	Shift data input	0	0
DX0G	Loop back data shift input	U4C0_DOUT	U4C1_DOUT
Clock Inputs			
DX1A	Shift clock input	P11.3	P8.4
DX1B	Shift clock input	0	0
DX1C	Shift clock input	0	P8.5
DX1D	Shift clock input	P11.0	0
DX1E	Shift clock input	0	0
DX1F	Input for single wire ASC collision detection	U4C0_DX0INS	U4C1_DX0INS
DX1G	Loop back shift clock input	U4C0_SCLKOUT	U4C1_SCLKOUT
Control Inputs			
DX2A	Shift control input	P11.5	P8.6
DX2B	Shift control input	0	0
DX2C	Shift control input	0	0
DX2D	Shift control input	0	0
DX2E	Input for transmit data validation	CC28IO	RTC_T14INT
DX2F	Input for transmit data validation	CCU62_COUT63	CCU62_COUT63
DX2G	Loop back shift control input	U4C0_SELO0	U4C1_SELO0

Table 21-18 I/O Connections of USIC4 (cont'd)

Signal	Used as	From/To	
		Channel 0 – U4C0	Channel 1 – U4C1
Data Outputs			
DOUT	Shift data output	P2.13	P7.1
		0	0
		–	0
Clock Outputs			
MCLKOUT	Master clock output, e.g. for IIS	0	P8.1
SCLKOUT	Shift clock output	P11.0	P8.5
		0	0
Control Outputs			
SELO0	Shift control output 0	P3.3	P8.3
SELO1	Shift control output 1	P11.2	–
SELO2	Shift control output 2	–	–
SELO3	Shift control output 3	–	–
SELO4	Shift control output 4	–	–
SELO5	Shift control output 5	–	–
SELO6	Shift control output 6	–	–
SELO7	Shift control output 7	–	–
System Related Outputs			
DX0INS	External interrupt input for ERU	–	–
	Single wire ASC collision detection	U4C0_DX1F	U4C1_DX1F
DX1INS	External interrupt input for ERU (SCU)	–	–
DX2INS	External interrupt input for ERU (SCU)	–	–
Loop Back Connections			
DOUT	Loop back shift data output	U4C0_DX0G	U4C1_DX0G
SCLKOUT	Loop back shift clock output	U4C0_DX1G	U4C1_DX1G
SELO0	Loop back shift control output	U4C0_DX2G	U4C1_DX2G

22 Controller Area Network (MultiCAN) Controller

This chapter describes the MultiCAN controller of the XC27x8X. It contains the following sections:

- Overview of the MultiCAN Kernel (see [Section 22.1](#))
- Functional description of the MultiCAN Kernel (see [Section 22.2](#))
- XC27x8X implementation specific details and registers of the MultiCAN controller (port connections and control, interrupt control, address decoding, clock control, see [Section 22.4](#)).

Note: The MultiCAN kernel register names described in this chapter will be referenced in the XC27x8X User's Manual by the module name prefix "CAN_".

22.1 MultiCAN Short Description

This section describes the serial communication interfaces CAN (Controller Area Network) of the communication module MultiCAN of the XC27x8X Derivatives.

22.1.1 Overview

The MultiCAN module contains 3 independent CAN nodes and 64 objects, representing the communication interfaces.

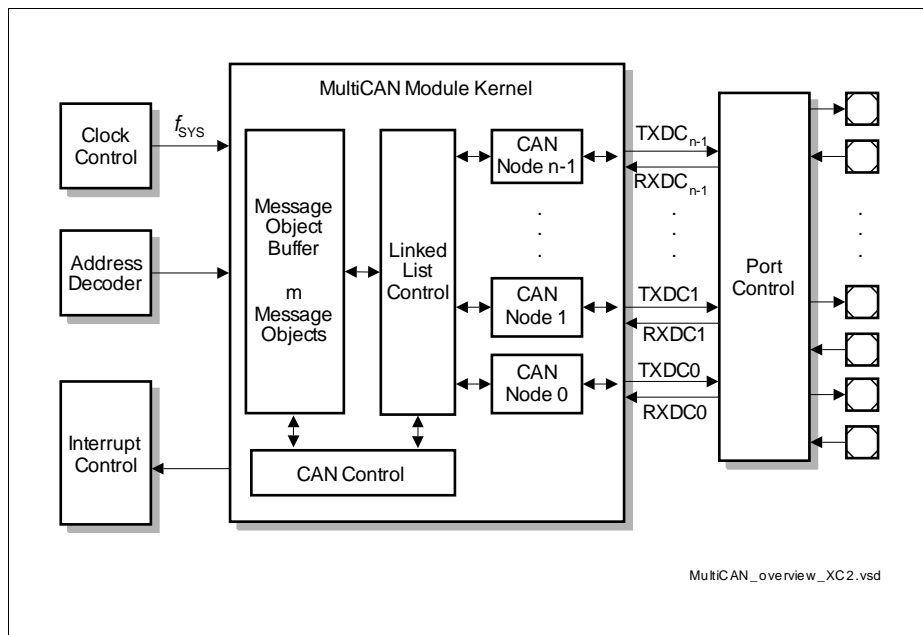


Figure 22-1 Overview of the MultiCAN

22.1.2 MultiCAN Features

Several key features contribute to the high performance of the MultiCAN module:

- 6 independent CAN nodes and 256 message objects available
- Compliant with ISO 11898
- CAN functionality according to CAN specification V2.0 B active
- Dedicated control registers for each CAN node
- Data transfer rates up to 1 Mbit/s
- Flexible and powerful message transfer control and error handling capabilities
- Advanced CAN bus bit timing analysis and baud rate detection for each CAN node via a frame counter
- Full-CAN functionality: A set of message objects can be individually
 - Allocated (assigned) to any CAN node
 - Configured as transmit or receive object
 - Set up to handle frames with 11-bit or 29-bit identifier
 - Identified by a timestamp via a frame counter
 - Configured to remote monitoring mode

Controller Area Network (MultiCAN) Controller

- Advanced acceptance filtering
 - Each message object provides an individual acceptance mask to filter incoming frames
 - A message object can be configured to accept standard or extended frames or to accept both standard and extended frames
 - Message objects can be grouped into four priority classes for transmission and reception
 - The selection of the message to be transmitted first can be based on frame identifier, IDE bit and RTR bit according to CAN arbitration rules, or according to its order in the list
- Advanced message object functionality
 - Message objects can be combined to build FIFO message buffers of arbitrary size, limited only by the total number of message objects
 - Message objects can be linked to form a gateway that automatically transfers frames between two different CAN buses. A single gateway can link any two CAN nodes. An arbitrary number of gateways can be defined.
- Advanced data management
 - The message objects are organized in double-chained lists
 - List reorganizations can be performed at any time, even during full operation of the CAN nodes
 - A powerful, command-driven list controller manages the organization of the list structure and ensures consistency of the list
 - Message FIFOs are based on the list structure and can easily be scaled in size during CAN operation
 - Static allocation commands offer compatibility with TwinCAN applications that are not list-based
- Advanced interrupt handling
 - Up to 16 interrupt output lines are available. Interrupt requests can be routed individually to one of the 16 interrupt output lines
 - Message post-processing notifications can be mapped flexibly using dedicated registers consisting of notification bits

22.2 CAN Functional Description

This section describes the core features of the CAN module.

22.2.1 Conventions and Definitions

Table 22-1 defines constants that are used throughout the MultiCAN specification. These are fixed values for a given MultiCAN implementation.

Table 22-1 Fixed Module Constants

Constant	Value	Description
n_objects	256	Number of Message Objects n_objects denotes the total amount of message objects available.
n_interrupts	16	Number of Interrupt Output Lines n_interrupts denotes the total number of interrupt outputs available.
n_pendings	256	Number of Message Pending Bits n_pendings denotes the number of message pending bits available. The number of message pending registers is given by $n_pendings/32$.
n_lists	8	Number of Lists n_lists denotes the total number of lists available for allocation of message number.
n_nodes	6	Number of CAN Nodes Available n_nodes denotes the total number of CAN nodes available. As each CAN node has its own list in addition to the list of un-allocated elements, the relation $n_nodes < n_lists$ is true.

22.2.2 Introduction

The MultiCAN module contains 6 Full-CAN nodes operating independently or exchanging data and remote frames via a gateway function. Transmission and reception of CAN frames is handled in accordance to CAN specification V2.0part B (active). Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

22.2.2.1 Feature Overview

All CAN nodes share a common set of message objects, where each message object may be individually allocated to one of the CAN nodes. Besides serving as a storage

Controller Area Network (MultiCAN) Controller

container for incoming and outgoing frames, message objects may be combined to build gateways between the CAN nodes or to setup a FIFO buffer.

The message objects are organized in double chained lists, where each CAN node has its own list of message objects. A CAN node stores frames only into message objects that are allocated to the list of the CAN node. It only transmits messages from objects of this list.

A powerful, command driven list controller performs all list operations.

The bit timings for the CAN nodes are derived from the peripheral clock (f_{CAN}) and are programmable up to a data rate of 1 Mbaud. A pair of receive and transmit pins connects each CAN node to a bus transceiver.

Features

- Compliant to ISO 11898.
- CAN functionality according to CAN specification V2.0 B active.
- Dedicated control registers are provided for each CAN node.
- A data transfer rate up to 1 Mbaud is supported.
- Flexible and powerful message transfer control and error handling capabilities are implemented.
- Advanced CAN bus bit timing analysis and baud rate detection can be performed for each CAN node via the frame counter.
- Full-CAN functionality: A set of 256 message objects can be individually
 - allocated (assigned) to any CAN node
 - configured as transmit or receive object
 - setup to handle frames with 11-bit or 29-bit identifier
 - counted or assigned a timestamp via a frame counter
 - configured to remote monitoring mode
- Advanced Acceptance Filtering:
 - Each message object provides an individual acceptance mask to filter incoming frames.
 - A message object can be configured to accept only standard or only extended frames or to accept both standard and extended frames.
 - Message objects can be grouped into 4 priority classes.
 - The selection of the message to be transmitted first can be performed on the basis of frame identifier, IDE bit and RTR bit according to CAN arbitration rules.
- Advanced Message Object Functionality:
 - Message Objects can be combined to build FIFO message buffers of arbitrary size, which is only limited by the total number of message objects.
 - Message objects can be linked to form a gateway to automatically transfer frames between 2 different CAN buses. A single gateway can link any two CAN nodes. An arbitrary number of gateways may be defined.
- Advanced Data Management:

Controller Area Network (MultiCAN) Controller

- The Message objects are organized in double chained lists.
- List reorganizations may be performed any time, even during full operation of the CAN nodes.
- A powerful, command driven list controller manages the organization of the list structure and ensures consistency of the list.
- Message FIFOs are based on the list structure and can easily be scaled in size during CAN operation.
- Static Allocation Commands offer compatibility with TwinCAN applications, which are not list based.
- **Advanced Interrupt Handling:**
 - Up to 16 interrupt output lines are available. Most interrupt requests can be individually routed to one of the 16 interrupt output lines.
 - Message postprocessing notifications can be flexibly aggregated into a dedicated register field of 256 notification bits.

Controller Area Network (MultiCAN) Controller

22.2.2.2 Module Structure

Figure 22-2 shows the general structure of the MultiCAN module with n CAN nodes ($n=6$ in XC27x8X).

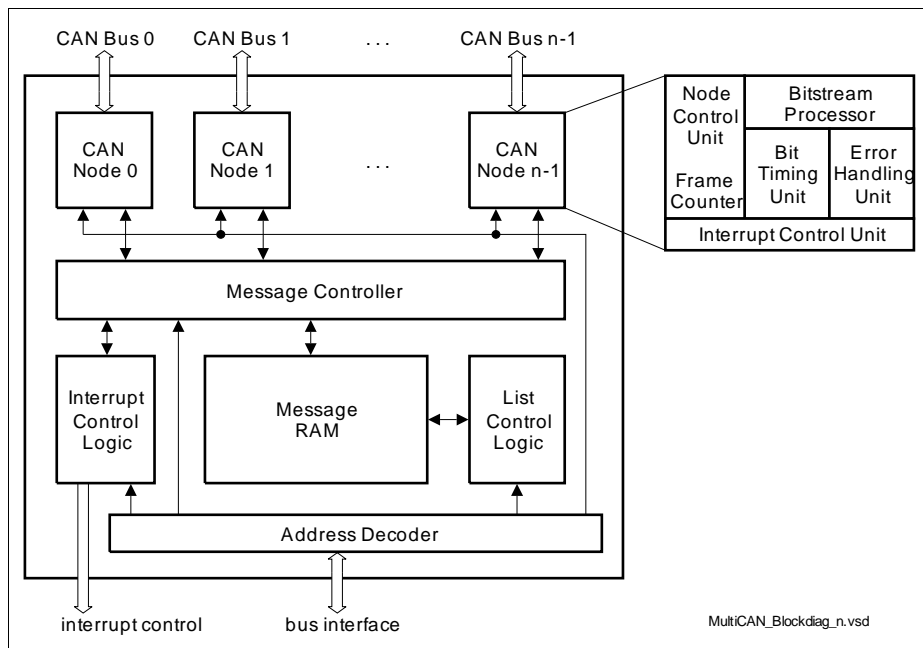


Figure 22-2 MultiCAN Block Diagram with several CAN Nodes

Controller Area Network (MultiCAN) Controller

CAN Nodes

Each CAN node consists of several sub-units as described in [Table 22-2](#):

Table 22-2 Subunits of CAN Nodes

Subunit	Description
Bit Stream Processor	The Bit Stream Processor performs data, remote, error and overload frame processing according to the ISO 11898 standard. This includes conversion between the serial data stream and the input/output shift registers.
Bit Timing Unit	The Bit Timing Unit defines the length of a bit time and the location of the sample point according to the user settings, taking into account propagation delays and phase shift errors. The Bit Timing Unit also performs resynchronization.
Error Handling Unit	The Error Handling Unit manages the receive and transmit error counter. According to the contents of both counters the CAN node is set into an "Error Active", "Error Passive" or "Bus-Off" state.
Node Control Unit	The Node Control Unit coordinates the operation of the CAN node: <ul style="list-style-type: none"> • Enables/disable CAN transfer of the node • Enable/Disable and generate node specific events that lead to an interrupt request (CAN bus errors, successful frame transfers etc.) • Administration of the Frame Counter

Message Controller

The message controller handles the exchange of CAN frames between the CAN nodes and the message objects which are stored in the Message RAM. It performs:

- Receive Acceptance filtering to determine the correct message object for storing of a received CAN frame.
- Transmit Acceptance Filtering to determine the message object to be transmitted first, individually for each CAN node.
- Content transfer between message objects and the CAN nodes, taking into account the status/control bits of the message objects.
- Handling of the FIFO buffering and Gateway functionality.
- Aggregation of message pending notification bits.

List Controller

The list controller performs all operations that lead to a modification of the double chained message object lists. Only the list controller is allowed to modify the list structure. The allocation/deallocation or reallocation of a message object can be requested via a user command interface (command panel). The list controller state machine then performs the requested command autonomously.

22.2.3 CAN Node Control

Each CAN node may be configured and run independently from the other CAN nodes. To this end each CAN node is equipped with an individual set of SFR registers to control and to monitor the CAN node.

22.2.3.1 Bit Timing

According to ISO 11898 standard, a CAN bit time is subdivided into different segments (**Figure 22-3**). Each segment consists of multiples of a time quantum t_q . The magnitude of t_q is adjusted by the bit field BRP and by bit DIV8, both controlling the baud rate prescaler (see bit timing register NBTR). The baud rate prescaler is driven by the MultiCAN module clock f_{CAN} .

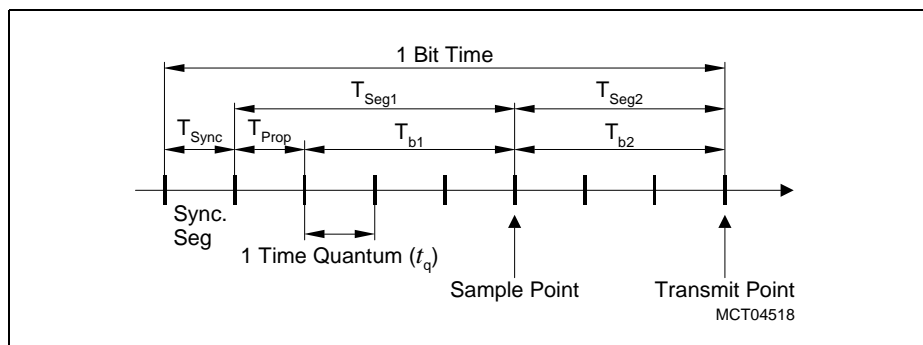


Figure 22-3 CAN Bus Bit Timing Standard

The Synchronization Segment (T_{Sync}) allows a phase synchronization between transmitter and receiver time base. The Synchronization Segment length is always 1 t_q . The Propagation Time Segment (T_{Prop}) takes into account the physical propagation delay in the transmitter output driver, on the CAN bus line and in the transceiver circuit. For a working collision detect mechanism, T_{Prop} has to be two times the sum of all propagation delay quantities rounded up to a multiple of t_q . The Phase Buffer Segments 1 and 2 (T_{b1} , T_{b2}) before and after the signal sample point are used to compensate a mismatch between transmitter and receiver clock phase detected in the synchronization segment.

The maximum number of time quanta allowed for resynchronization is defined by bit field SJW in the CAN Node Bit Timing register NBTR. The Propagation Time Segment and the Phase Buffer Segment 1 are combined to parameter TSeg1, which is defined by the value TSEG1 in the respective CAN Node Bit Timing register NBTR. A minimum of 3 time quanta is requested by the ISO standard. Parameter TSeg2, which is defined by the value of TSEG2 in the CAN Node Bit Timing Register NBTR, covers the Phase Buffer Segment 2. A minimum of 2 time quanta is requested by the ISO standard. According

Controller Area Network (MultiCAN) Controller

ISO standard, a CAN bit time, calculated as the sum of T_{Sync} , T_{Seg1} and T_{Seg2} , must not fall below 8 time quanta.

Calculation of the bit time:

$$\begin{aligned}
 t_q &= (\text{BRP}+1) / f_{\text{CAN}} && \text{if DIV8} = 0 \\
 &= 8 \times (\text{BRP}+1) / f_{\text{CAN}} && \text{if DIV8} = 1 \\
 T_{\text{Sync}} &= 1 t_q \\
 T_{\text{Seg1}} &= (\text{TSEG1} + 1) \times t_q && (\text{min. } 3 t_q) \\
 T_{\text{Seg2}} &= (\text{TSEG2} + 1) \times t_q && (\text{min. } 2 t_q) \\
 \text{bit time} &= T_{\text{Sync}} + T_{\text{Seg1}} + T_{\text{Seg2}} && (\text{min. } 8 t_q)
 \end{aligned}$$

To compensate phase shifts between clocks of different CAN controllers, the CAN controller has to synchronize on any edge from the recessive to the dominant bus level. If the hard synchronization is enabled (at the start of frame), the bit time is restarted at the synchronization segment. Otherwise, the resynchronization jump width T_{SJW} defines the maximum number of time quanta a bit time may be shortened or lengthened by one resynchronization. The value of SJW is programmed in the CAN Node Bit Timing Register.

$$\begin{aligned}
 T_{\text{SJW}} &= (\text{SJW} + 1) \times t_q \\
 T_{\text{Seg1}} &\geq T_{\text{SJW}} + T_{\text{prop}} \\
 T_{\text{Seg2}} &\geq T_{\text{SJW}}
 \end{aligned}$$

The maximum relative tolerance for f_{CAN} depends on the Phase Buffer Segments and the resynchronization jump width.

$$\begin{aligned}
 df_{\text{CAN}} &\leq \min(Tb1, Tb2) / 2 \times (13 \times \text{bit time} - Tb2) \quad \text{AND} \\
 df_{\text{CAN}} &\leq T_{\text{SJW}} / 20 \times \text{bit time}
 \end{aligned}$$

A valid CAN bit timing must be written to the CAN Node Bit Timing Register NBTR before resetting the INIT bit in the Node Control Register, i.e. before enabling the operation of the CAN node.

The Node Bit Timing Register may be written only if bit CCE (Configuration Change Enable) is set in the corresponding Node Control Register.

22.2.3.2 CAN Error Handling

The Error Handling Unit of the CAN node is responsible for the fault confinement of the CAN device. Its two counters, the Receive Error Counter and the Transmit Error Counter (control register NECNT), are incremented and decremented by commands from the Bit Stream Processor. If the Bit Stream Processor itself detects an error while a transmit operation is running, the Transmit Error Counter is incremented by 8. An increment of 1 is used, when the error condition was reported by an external CAN node via an error frame generation. For error analysis, the transfer direction of the disturbed message and the node, recognizing the transfer error, are indicated in the control register NECNT of the respective CAN node. According to the values of the error counters, the CAN node is set into the states "error active", "error passive" and "bus-off".

The CAN node is in error active state, if both error counters are below the error passive limit of 128. It is in error passive state, if at least one of the error counters equals or exceeds 128.

The bus-off state is activated if the Transmit Error Counter equals or exceeds the bus-off limit of 256. This state is reported by flag BOFF in the NSR status register of the CAN node. The device remains in this state, until the bus-off recovery sequence is finished. Additionally, there is the bit EWRN in the NSR status register, which is set, if at least one of the error counters equals or exceeds the error warning limit defined by bit field EWRNLVL in the control registers NECNT of the CAN node. Bit EWRN is reset if both error counters fall below the error warning limit again (see [Page 22-63](#)).

22.2.3.3 CAN Frame Counter

Each CAN node is equipped with a frame counter which allows to count transmitted/received CAN frames or to obtain information about the time instant when a frame has been started to transmit or being received by the CAN node. CAN frame counting/bit time counting is performed by a 16 bit counter which is controlled by register NFCR of the respective CAN node. Bit field CFSEL of register NFCR defines the operation mode of the frame counter:

- **Frame Count Mode:** The frame counter is incremented after the successful transmission and/or reception of a CAN frame. The incremented value is copied to the CFC field of the Interrupt Pointer Register of the message object involved in the transfer.
- **Time Stamp Mode:** The frame counter is incremented with the beginning of a new bit time. When the transmission/reception of a frame starts, the value of the frame counter is captured and stored to the CFC field of register NFCR. After the successful transfer of the frame the captured value is copied to the CFC field of the Interrupt Pointer Register of the message object involved in the transfer.
- **Bit Timing Mode:** Used for baud rate detection and analysis of the bit timing ([Chapter 22.2.5.3](#)).

22.2.3.4 CAN Node Interrupts

Each CAN node is equipped with four interrupt sources.

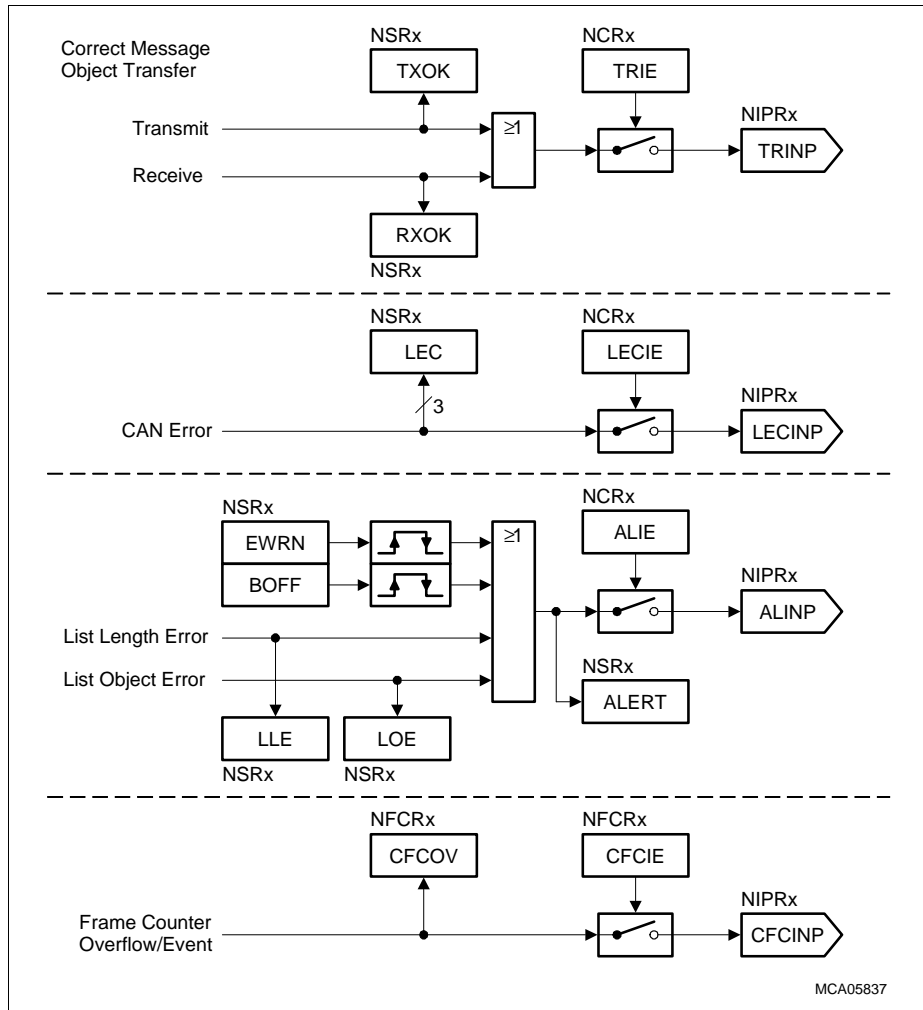


Figure 22-4 CAN Node Interrupts

Controller Area Network (MultiCAN) Controller

An interrupt request is generated upon:

- The successful transmission/reception of a frame,
- An overflow of the frame counter (frame count mode/time stamp mode) or a bit timing measurement event (bit timing mode),
- An error related to the CAN node.

22.2.4 Message Object List Structure

The message objects of the MultiCAN module are organized in double chained lists, where each message object has a pointer to the previous message object in the list as well as a pointer to the next message object in the list.

22.2.4.1 Basics

The MultiCAN module provides 16 different lists, where each object is allocated to one of these lists. A 4 bit LIST bit field in the Message Object Control Register indicates the list to which the respective message object is currently allocated. In the example of [Figure 22-5](#) three message objects are allocated to the list with list index 2.

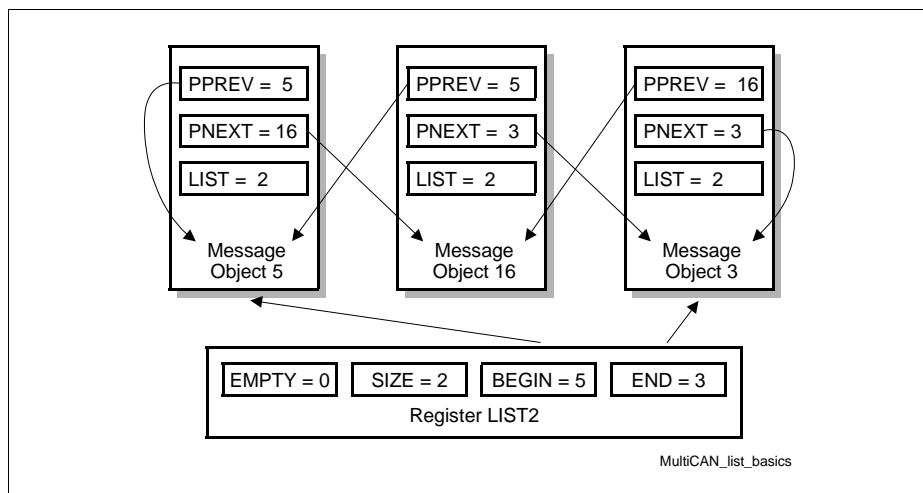


Figure 22-5 Example Allocation of Message Objects to a List

The BEGIN field of the List Register points to the first element in the list (object 5 in the example) whereas the END field points to the last element in the list (object 3 in the example). The number of elements in the list is indicated in the SIZE field of the List Register (#elements = SIZE + 1, thus SIZE = 2 for the 3 elements of the example). The

Controller Area Network (MultiCAN) Controller

EMPTY bit indicates a list with no elements (EMPTY = 0 in the example, as the list is not empty).

Each message object has a pointer PNEXT (located in the Message Object Control Register) that points to the next message object in the list and a pointer PREV that points to the previous message object in the list. PPREV of the first message object points to the object itself because the first object has no predecessor (in the example object 5 is the first object, indicated by PPREV = 5). PNEXT of the last message object also points to the object itself because the last element has no successor (in the example object 3 is the last object, indicated by PNEXT = 3).

Each message object also has a 4 bit LIST field (located in the Message Object Control Register) which shows list index of the list to which the object is currently allocated (the objects of the example are allocated to list 2, thus LIST = 2).

22.2.4.2 List of Unallocated Elements

The list with list index 0 has a special meaning: It is the list of all unallocated elements. An element is called unallocated if and only if it belongs to list zero. It is called allocated if and only if it belongs to one of the other lists.

After reset all message objects are unallocated, i.e. belong to the list of unallocated elements. The initial allocation of the message objects within the list of unallocated objects is ordered by message number, i.e. the predecessor of message object n is object n-1 and the successor of object n is object n+1.

22.2.4.3 Connection to the CAN Nodes

One CAN node is linked to exactly one unique list of message objects..

Table 22-3 List Indices

List Index	Description
0	List of unallocated elements
1 to n_nodes	Lists associated to a CAN node. List index i belongs to CAN node i -1.
n_nodes+1 to n_lists-1	Free user lists, which are not associated to a CAN node.

Controller Area Network (MultiCAN) Controller

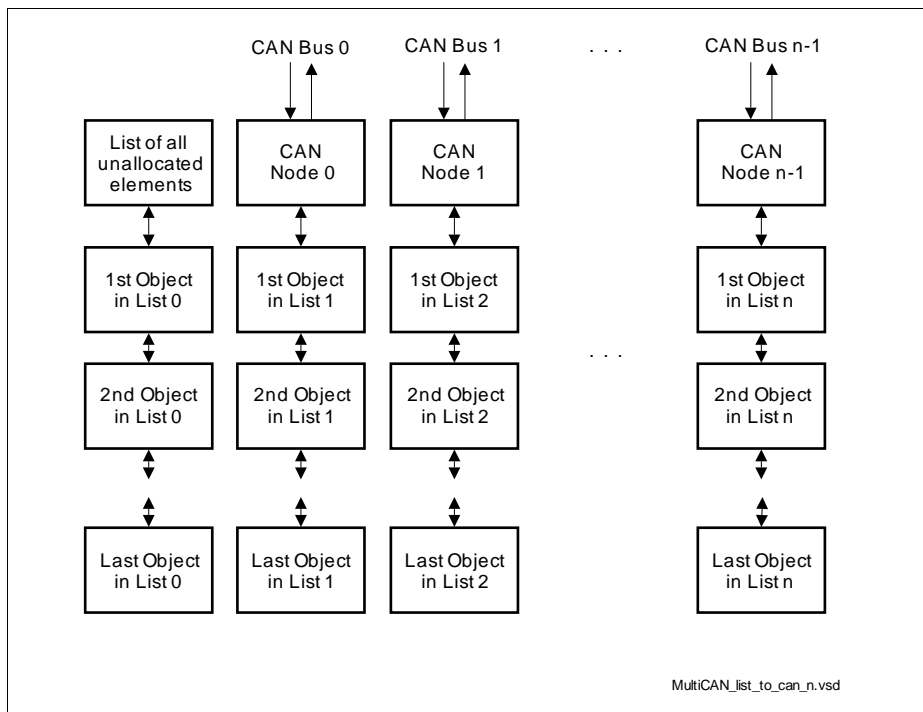


Figure 22-6 Message Objects Linked to several CAN Nodes

22.2.4.4 List Command Panel

The list structure may not be modified directly by means of write accesses to the LIST registers and the PPREV, PNEXT and LIST fields in the message objects as they are read only. The management of the list structure is performed by and limited to the list controller unit inside the MultiCAN module. The list controller is controlled via a command panel which allows the user to issue list allocation commands to the list controller. The list controller basically serves two purposes:

1. Ensure that all operations that modify the list structure result in a consistent list structure.
2. Present maximum comfort and flexibility to the user.

The list controller and the associated command panel allows the programmer to concentrate on the final properties of the list, which are characterized by the allocation of message objects to a CAN node and the ordering relation between objects which are allocated to the same list. The process of list (re-)building is left to the list controller.

A panel command is started by writing the respective command code (see [Table 22-9 “Panel Commands” on Page 22-53](#)) into the PANCMD field of the panel control register. The corresponding command arguments must be written to PANAR1 and PANAR2 before writing the command code or latest together with the command code in a single 32 bit write access to the panel control register (only possible within 32 bit system environments).

With the write of a valid command code the BUSY flag in the Panel Control Register becomes active (BUSY = 1) and the control panel registers are locked, which means that write accesses to the Panel Control Register are ignored. The BUSY flag remains active and the control panel remains locked until the execution of the requested command is completed.

When the issued command is a dynamic allocation which takes an element from the list of unallocated objects, then also the RBUSY bit becomes active together with the BUSY bit (RBUSY = BUSY = 1) to indicate that PANAR1 and PANAR2 are going to be updated by the list controller:

1. The message number of the message object taken from the list of unallocated elements is written to PANAR1.
2. An error status is posted to bit 7 of PANAR2 (Bit 7 = ERR). If ERR = 1 then the list of unallocated elements was empty and the command is aborted. If ERR = 0 then the list was not empty and the command will be performed successfully.

The results are written before the list controller starts the actual allocation process. As soon as the results are available, RBUSY becomes inactive (RBUSY = 0) again, while BUSY still remains active until completion of the command. This allows the user to setup the new message object while it is still in the process of list allocation. The access to message objects is not limited during ongoing list operations. However, any access to a

Controller Area Network (MultiCAN) Controller

register resource located inside the RAM delays the ongoing allocation process by one access cycle.

As soon as the command is done the BUSY flag becomes inactive (BUSY = 0) and write accesses to the Panel Control Register are enabled again. Also the NOP command code is automatically written to the CMD field of the Panel Control Register. A new command may be started any time during BUSY inactive.

All fields of the Panel Control Register except BUSY and RBUSY may be written by the user. This allows to save and restore the Panel Control Register if the Command Panel shall be used within independent (mutually interruptible) interrupt routines. If this is the case then any task that uses the Command Panel and that may interrupt another task also using the Command Panel should poll the BUSY flag until it becomes inactive and save the whole PANCTR register to a save memory location before issuing a command. At the end it should restore PANCTR from the said memory location.

Before a message object which is allocated to the list of an active CAN node shall be moved to another list or to another position within the same list, bit MSGVAL ("Message Valid") should be cleared in the Message Object Control Register of the message object.

22.2.5 CAN Node Analysis Features

CAN Analyze Mode allows to monitor the CAN traffic without affecting the logical state of the CAN bus.

22.2.5.1 Analyze Mode

CAN Analyze Mode is selected by setting bit CALM in the Node Control Register. CAN Analyze Mode may be selected for each CAN node individually.

In CAN Analyze Mode the transmit pin of the CAN node is held on recessive level. The CAN node may receive frames (data-, remote-, and error frames) but is not allowed to transmit. Active error frames are sent recessive. Received data/remote frames are not acknowledged (i.e. acknowledge slot is sent recessive), but will be received and stored in matching message objects as long as there is any other node that acknowledges the frame.

All message object functionality is available, but no transmit request will be executed.

22.2.5.2 Loop-back Mode

The MultiCAN module provides a loop-back mode to enable an in-system test of the MultiCAN module as well as the development of CAN driver software without access to an external CAN bus.

The loop-back feature consists of an internal CAN bus (inside the MultiCAN module) and a bus select switch for each CAN node ([Figure 22-7](#)). With the switch each CAN node can be wired either to the internal CAN bus (loop-back mode activated) or the external CAN bus, i.e. the transmit- and receive pins (normal operation). The CAN bus which is currently not selected is driven recessive, i.e. the transmit pin is held at 1 and the receive pin is ignored by the CAN nodes which are in loop-back mode.

Loop-back Mode is selected individually for each CAN node by setting bit LBM in the respective Node Port Control Register. All CAN nodes that are in loop-back mode may communicate on the internal CAN bus without affecting the normal operation of the other CAN nodes which are not in loop-back mode.

Controller Area Network (MultiCAN) Controller

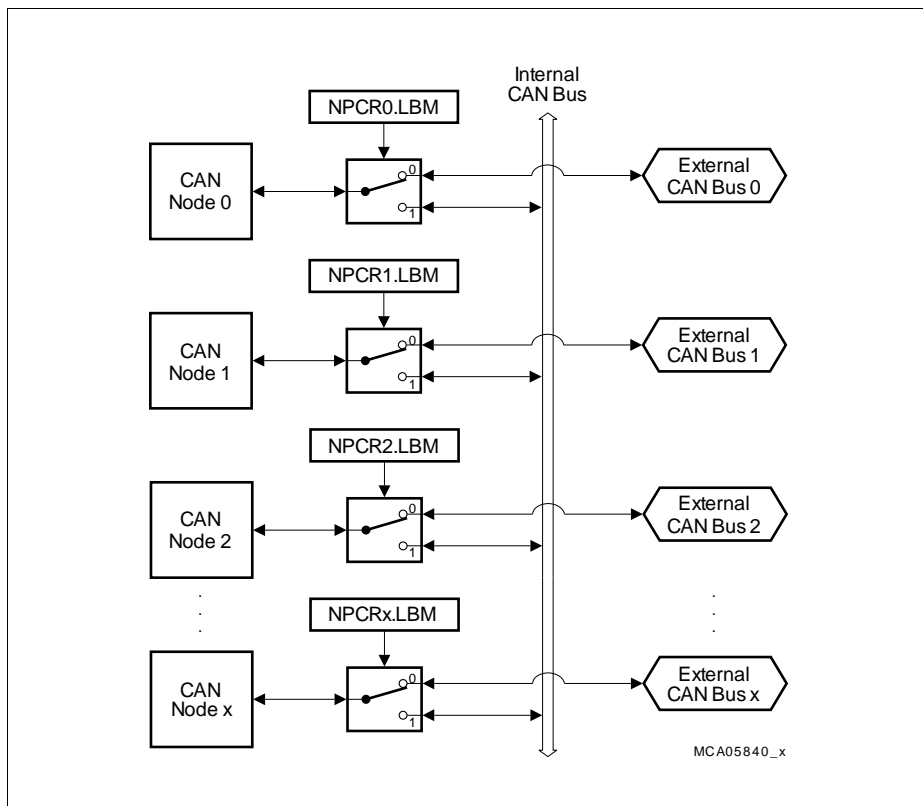


Figure 22-7 Loop-back Mode for several CAN Nodes

22.2.5.3 Bit Timing Analysis

For each CAN node detailed analysis of the bit timing can be performed by means of using dedicated analysis modes of the CAN frame counter. The bit timing analysis functionality of the frame counter may be used for automatic detection of the CAN baud rate as well as for the analysis of the timing of the CAN network.

Bit timing analysis for a CAN node is selected by $CFMOD = 10_B$ (Bit Timing Mode) in the CAN Node Frame Counter Register.

Bit timing analysis does not affect the operation of the CAN node.

The measurement results are written to the CFC field. Whenever CFC is updated in Bit Timing Mode, then also the CFCOV bit is set in order to indicate the update event. If CFCIE is set then also an interrupt request is generated, where for the CAN node $i = 0$ to 5 the interrupt request is generated on the interrupt output line i .

Automatic Baud Rate Detection

Automatic baud rate detection requires to measure the time between the observation of subsequent dominant edges on the CAN bus. This measurement is automatically performed if $CFSE = 000_B$ in the CAN Node Frame Counter Register. With each dominant edge monitored on the CAN receive input the time (measured in clock cycles) between this edge and the most recent dominant edge is stored in the CFC field.

Synchronization Analysis

The bit time synchronization is monitored if $CFSEL = 010_B$. The time between the first dominant edge and the sample point is measured and stored in CFC. The bit timing synchronization offset may be derived from this time as the first edge after the sample point triggers synchronization and there is only one synchronization between consecutive sample points.

Synchronization Analysis may be used to fine tune the baud rate during reception of the first CAN frame with the measured baud rate.

Driver Delay Measurement

The delay between a transmitted edge and the corresponding received edge is measured with $CFSEL = 011_B$ (dominant to dominant) and $CFSEL = 001_B$ (recessive to recessive). These delays indicate the time needed to represent a new bit value on the physical implementation of the CAN bus.

22.2.6 Message Acceptance Filtering

The message acceptance filtering includes receive and transmit filtering.

22.2.6.1 Receive Acceptance Filtering

When a message object is received on a CAN node, then a unique message object is determined in which the received frame will be stored upon successful frame reception. A message object qualifies for the reception of a frame if and only if the following conditions are fulfilled:

1. The message object is allocated to the list of the CAN node on which the frame is received.
2. MSGVAL is set in the Message Control Register
3. RXEN is set in the Message Control Register
4. The DIR bit in the Message Control Register equals the RTR bit of the received frame. If DIR = 1 (transmit object) then the message object only accepts remote frames. If DIR = 0 (receive object) then the message object only accepts data frames.
5. If MIDE = 1 in the Acceptance Mask Register (MOAMR) then the IDE bit of the received frame equals the IDE bit in the Arbitration Register (MOAR). IF MOAR.IDE = 1 then the message object only accepts frames with extended identifier. If MOAR.IDE = 0 then the message object only accepts standard frames. If MOAMR.MIDE = 0 then the IDE bit of the received frame is don't care, i.e. the message object accepts both standard and extended frames.
6. The identifier of the received frame matches the identifier stored in the Arbitration Register of the message object with respect to the acceptance mask in the MOAMR register. This means that each bit of the received identifier is equal to the corresponding identifier bit in the Acceptance Register, except those bits for which the corresponding mask bits in MOAMR are cleared. These identifier bits are don't care. **Figure 22-8** illustrates this identifier check.

A priority ordering relation is defined for the message objects:

A message object A has higher receive priority than a message object B if and only if the following conditions are fulfilled:

1. A belongs to a higher priority class than B, i.e. MOAR.PRI of A must be less than or equal to MOAR.PRI of B.
2. If both objects belong to the same priority class (PRI of A = PRI of B) then message object B is a list successor of A, i.e. B can be reached by means of successively stepping forward in the list, starting from A.

Among all messages that fulfill all 6 qualifying criteria the unique message object with highest receive priority wins acceptance filtering, i.e. is selected for storage of the received frame. All other message objects loose receive acceptance filtering.

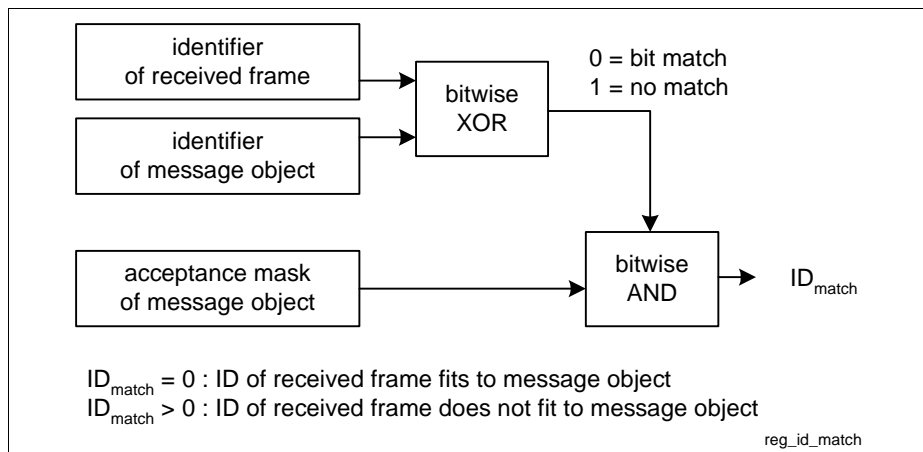


Figure 22-8 Received Message Identifier Acceptance Check

22.2.6.2 Transmit Acceptance Filtering

A message is requested for transmission by means of setting a transmit request in the message object which holds the message. If more than one message object has a valid transmit request for the same CAN node, then a single message object is chosen for actual transmission from the candidates, because only a single message object may be transmitted at the same time on a single CAN bus.

A message object qualifies for transmission on a given CAN node if and only if it meets the following criteria (**Figure 22-9**):

1. The message object is allocated to the list of the CAN node considered.
2. MSGVAL is set in the Message Object Control Register.
3. TXRQ is set in the Message Object Control Register.
4. TXEN0 and TXEN1 are set in the Message Object Control Register.

A priority order relation is defined for all qualifying objects to determine the message to be transmitted first: Let A and B be two message objects qualifying for transmission, where without loss of generality object B is assumed to be a list successor of A, i.e. B can be reached by means of successively stepping forward in the list, starting from A. For both message objects associated CAN messages CAN_A and CAN_B are defined, where identifier, IDE and RTR bit are taken from MOAR.ID, MOAR.IDE and MOCTR.DIR.

If both message objects belong to a different priority class (different value of bit field PRI in the Message Object Arbitration Register MOAR) then the message object with lower PRI value has higher transmit priority and will be transmitted first.

Controller Area Network (MultiCAN) Controller

If both message objects belong to the same priority class (equal value of bit field MOAR.PRI), then message object A has higher transmit priority than object B if and only if one of the following conditions is fulfilled:

1. PRI = 10 and CAN message CAN_A has higher or equal priority than CAN message CAN_B with respect to CAN arbitration rules (see [Table 22-13](#)).
2. PRI = 01 or PRI = 11 (priority by list order).

The unique message object that qualifies for transmission and has highest transmit priority wins transmit acceptance filtering, i.e. will be transmitted first. All other message objects lose the current transmit acceptance filtering round. They get a new chance in subsequent filtering rounds.

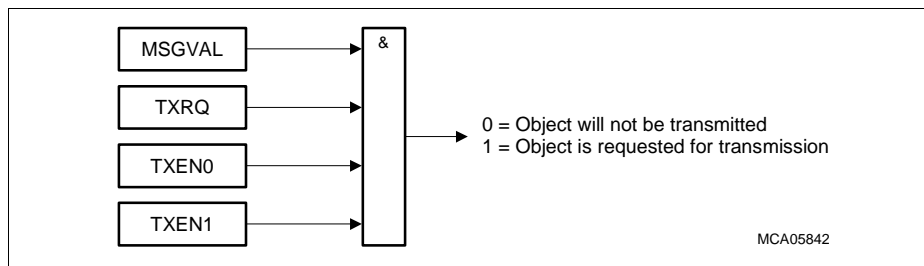


Figure 22-9 Effective Transmit Request of Message Object

22.2.7 Message Postprocessing Interface

When a message object has received or transmitted a frame successfully then the CPU may be notified to perform message postprocessing on the message object. The postprocessing interface of the MultiCAN module consists of two elements:

1. Message Interrupts to trigger postprocessing.
2. Message Pending Registers to aggregate the pending message interrupts into a common structure for postprocessing.

22.2.7.1 Message Interrupts

When the storage of a received frame into a message object or the successful transmission of a frame is completed then a message interrupt may be requested. For each message object both transmit and receive interrupts may be routed individually to one of the available interrupt output lines, as illustrated in [Table 22-10](#). A receive interrupt is not restricted to the direct storage of a received frame from the CAN node the message object belongs to. It also occurs upon frame storage induced by FIFO or gateway action. The TXPND and RXPND bits are set whenever a successful transmission/reception takes place, no matter if the respective interrupt is enabled or not.

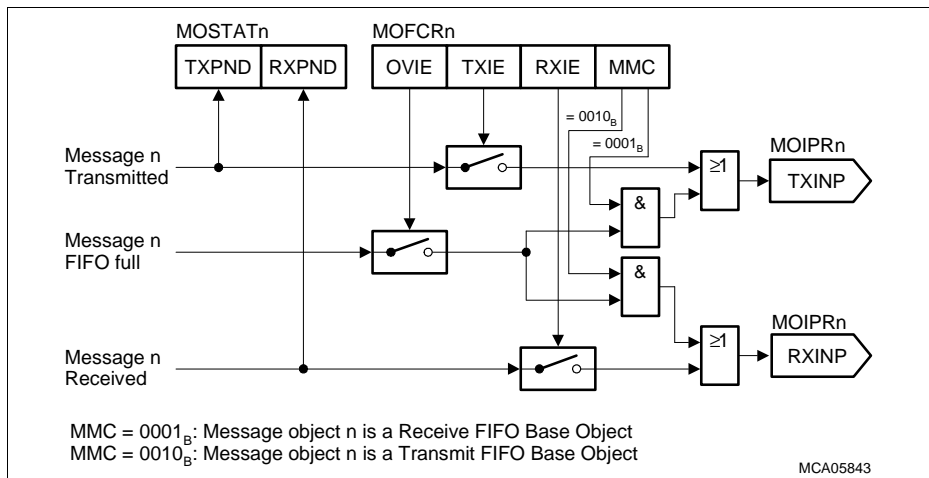


Figure 22-10 Message Interrupt Request Routing

22.2.7.2 Message Pending

When a message interrupt request is generated then also a message pending bit is set in one of the Message Pending Register. To this end the pending bit selection field MPN is defined in the Message Object Interrupt Pointer Register. The value of MPN is combined with TXINP and RXINP to yield the effective bit position of the Pending bit, as illustrated in [Figure 22-11](#). The bit position consists of 2 parts:

1. The high part (bits [7:5]) of the calculated position selects the Message Pending Register in which the pending bit will be set.
2. The low part (bits [4:0]) of the calculated position selects the position (0-31) of the pending bit within the 32 bit Message Pending Register.

The MPSEL bit field in the MultiCAN Control Register allows to include the interrupt request node pointer (RXINP for reception, TXINP for transmission) so as to implement different target location of the pending bit for receive and transmit.

The Message Pending Registers may be written by the CPU, but those bits that are written 1 are left unchanged and only those bits which are written 0 are cleared. This allows to clear individual bits with a single write access instead of a read/modify/write-back access. Thus there is no access conflict when the MultiCAN module sets another pending bit in the same register at the same time.

Each Message Pending Register is linked to an individual Message Index Register which displays the lowest bit position of all set (1) bits in the Message Pending Register. The Message Index Register is read only and is updated immediately when the value of the corresponding Message Pending Register changes.

There is no direct link between the Message Pending Registers and the interrupt request nodes. Such a link may, however, be established by the application. For example, each interrupt request node could be linked to a unique Message Pending Register. The example shown in [Figure 22-12](#) links message Pending Register n to interrupt output line n (n = 0-7).

Controller Area Network (MultiCAN) Controller

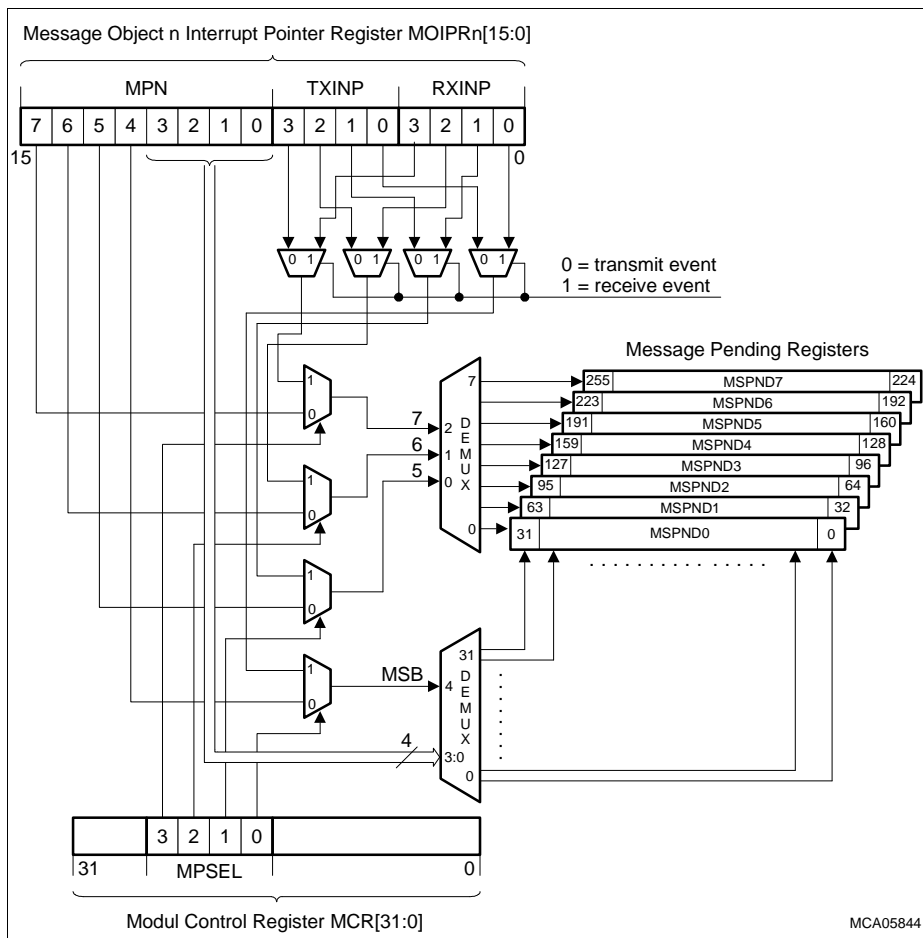


Figure 22-11 Target Location of the Message Pending Bit (Transmit/Receive)

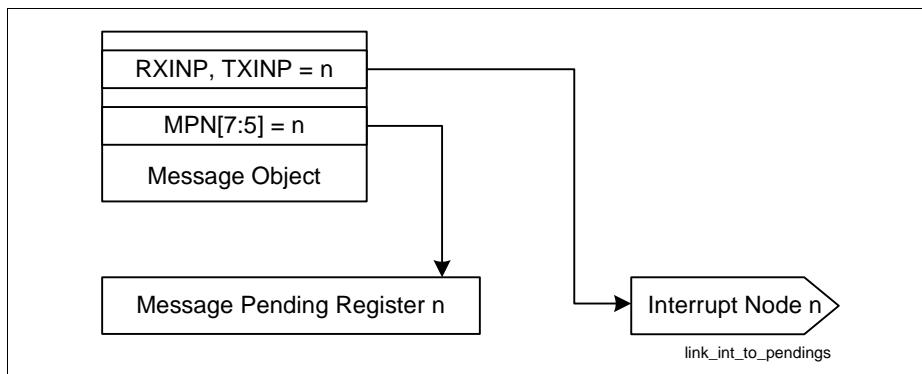


Figure 22-12 Example Link of Message Pending Registers to Interrupt Output Lines

22.2.8 Message Object Data Handling

The following section describes the actions taken during a frame reception and during a frame transmission.

22.2.8.1 Frame Reception

When a message is received on the CAN bus then the storage of the message into a message object is prepared and performed according to the scheme shown in [Figure 22-13](#). The MultiCAN module not just copies the received data into the message object, but it provides advanced features to enable consistent data exchange between MultiCAN and CPU.

MSGVAL

The MSGVAL ("Message Valid") bit in the Message Object Control Register is the main switch of the message object. The MultiCAN module only stores information in the message object during the frame reception process when MSGVAL is set (MSGVAL = 1).

Whenever MSGVAL is reset (MSGVAL = 0) by the CPU then the MultiCAN module stops all ongoing write accesses to the message object so that the message object may be reconfigured by the CPU in subsequent write accesses to the message object without being disturbed by the MultiCAN.

RTSEL

When the CPU re-configures a message object (i.e. clears MSGVAL, modifies the message object and sets MSGVAL again) during CAN operation then the following scenario can occur:

1. The message object wins receive acceptance filtering.
2. The CPU clears MSGVAL to reconfigure the message object.
3. The CPU sets MSGVAL again after reconfiguration.
4. The end of the received frame is reached. As MSGVAL is set, the received data are stored in the message object, a message interrupt request is generated, gateway and fifo actions are processed etc.

The storage of the received data may be undesirable if the context of the message object has changed, because the old message object configuration has been used for acceptance filtering of the message.

Bit MOCTR.RTSEL ("Receive/Transmit Selected") allows to disconnect a message object from an ongoing frame reception:

When a message object wins receive acceptance filtering then bit RTSEL is set (RTSEL = 1) by the MultiCAN in order to indicate an upcoming frame delivery. The MultiCAN checks RTSEL for value 1 upon successful frame reception in order to verify

Controller Area Network (MultiCAN) Controller

that the object is still ready for receiving the frame. The received frame is stored in the message object (along with all subsequent actions such as message interrupts, FIFO & gateway actions, flag updates) only if RTSEL = 1.

When the user invalidates a message object during CAN operation (MSGVAL → 0) then the user should clear RTSEL before setting MSGVAL again (latest with the same write access that sets MSGVAL) in order to prevent the storage of a frame that belongs to the old context of the message object. Thus message object reconfiguration should consist of the following sequence of steps:

1. Clear MSGVAL.
2. Reconfigure message object while MSGVAL = 0.
3. Clear RTSEL and set MSGVAL.

RXEN

Bit MOCTR.RXEN enables a message object for frame reception. A message object can receive CAN messages from the CAN bus only if RXEN = 1. The MultiCAN evaluates RXEN only during receive acceptance filtering. After receive acceptance filtering RXEN is ignored, i.e. the value of RXEN has no influence on the actual storage of a received message in a message object.

Bit RXEN enables a “soft phase out” of a message object: When the user clears RXEN then a currently received CAN message for which the message object has won acceptance filtering is still stored in the message object, but for subsequent messages the message object no longer wins receive acceptance filtering.

RXUPD, NEWDAT and MSGLST

An ongoing frame storage process is indicated with the RXUPD (“Receive Updating”) bit in the Message Object Control Register. The MultiCAN module sets RXUPD with the start and clears RXUPD with the end of a message object update (which consists of frame storage as well as flag updates).

After storing the received frame (identifier, IDE bit, DLC and for data frames also the data field) in the message object NEWDAT (“New Data”) is set by the MultiCAN. If NEWDAT was already set then also MSGLST (“Message Lost”) is set in order to indicate data loss.

The RXUPD and NEWDAT flags may be used by the CPU to read consistent frame data from the message object during ongoing CAN operation. The following steps are recommended:

1. Clear NEWDAT
2. Read message content (identifier, data etc.) from message object
3. Read Message Object Control Register and check that both NEWDAT and RXUPD are cleared. If this is not the case then goto back to step 1.
4. As step 3 was successful, the read message content is consistent, i.e. has not been updated by the MultiCAN while reading.

Controller Area Network (MultiCAN) Controller

The bits RXUPD, NEWDAT and MSGLST work in the same fashion for the reception of data as well as remote frames.

22.2.8.2 Frame Transmission

The process of message object transmission is illustrated in [Figure 22-14](#). In addition to copying the message content (identifier, IDE bit, RTR = DIR bit, DLC and for data frames also the data field) to the internal transmit buffer of the CAN node that the message object belongs to, also several status flags are served and monitored in order to enable consistent data handling.

The transmission process (after transmit acceptance filtering) of a given message object makes no difference between remote and data frames.

MSGVAL, TXRQ, TXEN0, TXEN1

For the MSGVAL bit the section **“MSGVAL” on Page 22-29** for frame reception is also valid for transmission.

A message may only be transmitted if all four bits MSGVAL (“Message Valid”), TXRQ (“Transmit Request”), TXEN0 (“Transmit Enable 0”), TXEN1 (“Transmit Enable 1”) of the Message Object Control Register are set (1) (see also [Figure 22-9](#)). Although these bits are equivalent with respect to the transmission process, they have different semantics:

Table 22-4 Bits to set (1) in MOCTR for message transmission

Bit	Description
MSGVAL	Message Valid Main Switch of the Message Object
TXRQ	Transmit Request Standard Transmit Request bit. The CPU should set this bit whenever a message object shall be transmitted. TXRQ is cleared automatically at the end of the successful transmission, except when there are new data (indicated by NEWDAT = 1) to be transmitted. When the single transmit trial bit is set (STT = 1) in the Message Object Function Register then TXRQ is already cleared by the MultiCAN when the content of the message object is copied to the transmit frame buffer of the CAN node. A received remote request (i.e. remote frame received on CAN bus) sets bit TXRQ to request the transmission of the corresponding data frame.

Controller Area Network (MultiCAN) Controller

Table 22-4 Bits to set (1) in MOCTR for message transmission (cont'd)

Bit	Description
TXEN0	Transmit Enable 0 This bit may be temporarily cleared by the CPU to suppress the transmission of this object when it writes new content to the data field. This avoids transmission of inconsistent frames which consist of a mixture of old and new data. Remote requests are still accepted during TXEN0 = 0, but transmission of the data frame is suspended until the CPU re-enables transmission (TXEN0 = 1).
TXEN1	Transmit Enable 1 This bit is used in transmit FIFOs to select the message object which is transmit active within the FIFO structure. For message objects which are not transmit FIFO elements TXEN1 may either be set to 1 permanently or be used as a second, independent transmission enable bit.

RTSEL

When a message object has been identified to be transmitted next (by acceptance filtering) then the MultiCAN set bit MOCTR.RTSEL ("Receive/Transmit Selected").

When the MultiCAN copies the message object to the transmit buffer it checks bit RTSEL and the message is transmitted only if RTSEL = 1.

After the successful transmission of the message bit RTSEL is checked again and message postprocessing is only performed if RTSEL = 1.

A complete reconfiguration of an operating message object should be done by means of the following steps:

1. Clear MSGVAL ("Message Valid").
2. Reconfigure message object while MSGVAL = 0.
3. Clear RTSEL and set MSGVAL.

Here clearing RTSEL ensures that the message object is disconnected from an ongoing/scheduled transmission and no message object processing (copying message to transmit buffer incl. clearing NEWDAT, clearing TXRQ, time stamp update, message interrupt etc.) within the old context of the object may occur after the message object becomes valid again, but within a new context.

NEWDAT

When the content of a message object has been transferred to the transmit buffer of the CAN node then bit NEWDAT ("New Data") is cleared to indicate that the transmit data of the message object are no longer new.

Controller Area Network (MultiCAN) Controller

When the CAN transmission of the frame is successful and NEWDAT is still cleared (i.e. no new data have been copied to the message object in the meantime) then TXRQ ("Transmit Request") is cleared automatically.

If, however, the NEWDAT bit has been set again by the CPU (because a new frame shall be transmitted) then TXRQ is not cleared in order to enable the transmission of the new data.

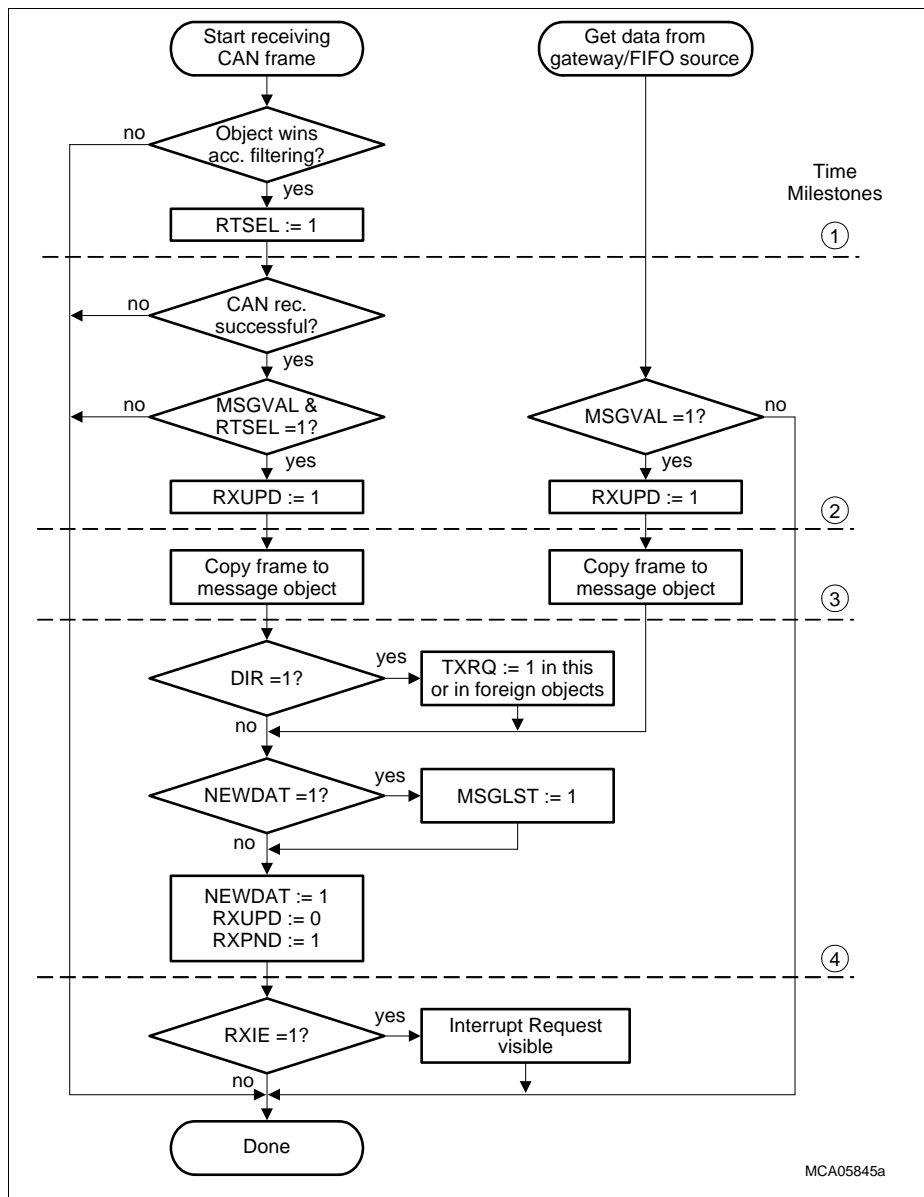


Figure 22-13 Data Delivery to Message Object by MultiCAN Module

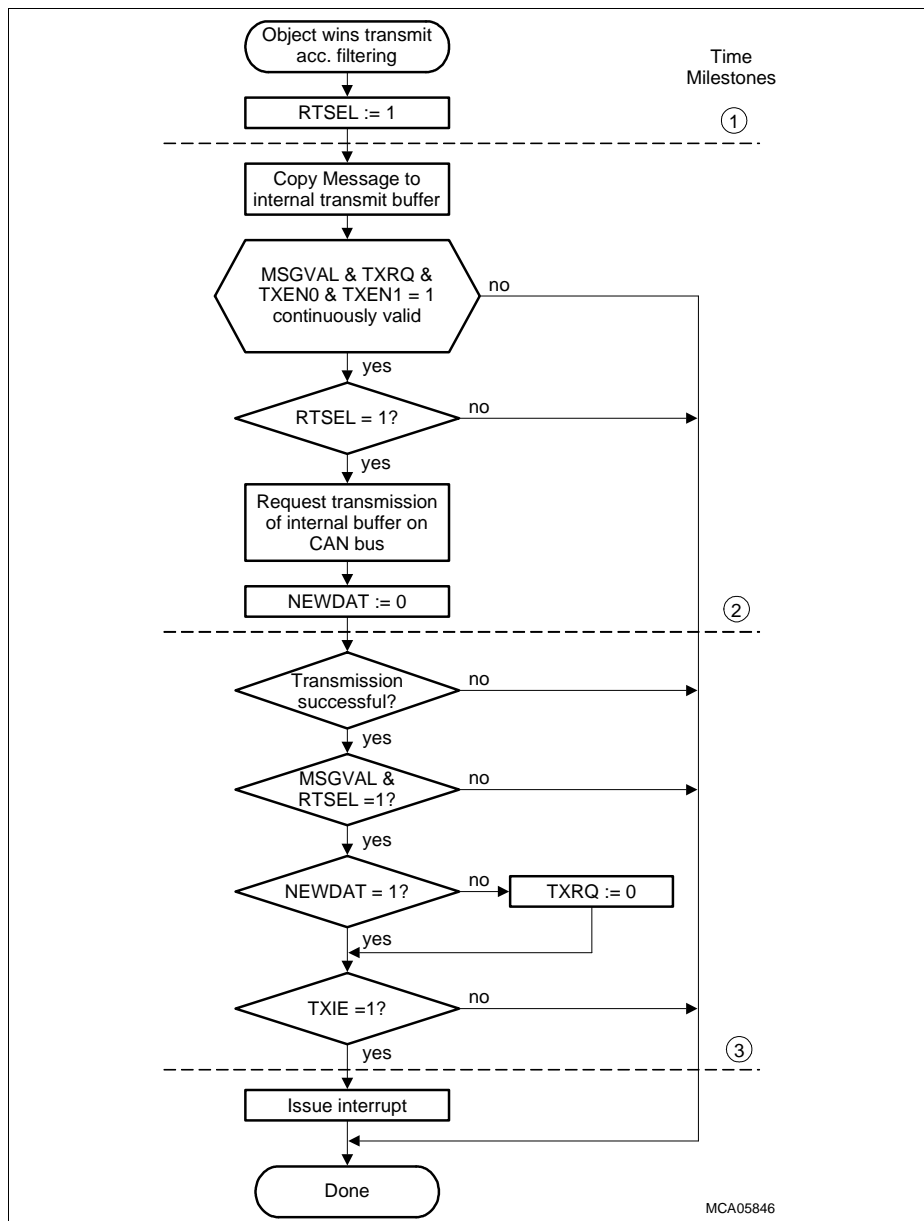


Figure 22-14 Transmission of a Message Object

22.2.9 Message Object Functionality

This section describes the functionality that is related to each individual Message Object.

22.2.9.1 Standard Message Object Mode

Standard message mode is selected via $MMC = 0000_B$ in the Message Object Function Control Register of the message object. In this mode a message object may transmit and receive CAN frames according to the basic rules as described in the previous sections. Additional services such as Single Data Transfer Mode or Single Transmit Trial (see sections below) are available and may be selected individually by the user.

22.2.9.2 Single Data Transfer Mode

Single Data Transfer Mode is a useful feature in order to broadcast data over the CAN bus without unintended doubling of information. Single Data Transfer Mode is selected via bit SDT in the Message Object Function Register of the message object.

Message Reception

When a received message is stored in a message object and further messages are stored in the same message object before the CPU reads the first message object, then the content of the first message gets lost and is replaced with the content of the subsequent messages (indicated by $MSGLST = 1$).

If $SDT = 1$ (Single Data Transfer Mode activated) then the MultiCAN controller automatically clears the MSGVAL bit of the message object after the storage of a received data frame to prevent the reception of further messages.

The reception of a remote frame does not lead to the clearance of MSGVAL.

Message Transmission

When a message object receives a series of multiple remote requests then it transmit several data frames in response to the requests. If the data within the message object has not been updated in the time between the transmissions, the same data may be represented more than once on the CAN bus.

In Single Data Transfer Mode ($SDT = 1$) this is avoided because the MultiCAN controller automatically clears MSGVAL after the successful transmission of a data frame.

The transmission of a remote frame does not clear MSGVAL.

22.2.9.3 Single Transmit Trial

If the bit STT in the message object function register is set ($STT = 1$) then the transmission request is cleared ($TXRQ := 0$) when the frame content of the message

Controller Area Network (MultiCAN) Controller

object has been copied to the internal transmit buffer of the CAN node. Thus the transmission of the message object is not tried again when it fails due to CAN bus errors.

22.2.9.4 Message Object FIFO Structure

In case of high CPU load it may be difficult to process a series of CAN frames in time. This may happen for the short term reception of multiple messages as well as the transmission of a series with tight due date.

Therefore a FIFO buffer structure has been implemented in order to avoid loss of incoming messages and to minimize the setup time for outgoing messages. The FIFO structure may also be used to automate the reception or transmission of a series of CAN messages and to generate a single message interrupt when the whole series is done.

There may be as many FIFOs in parallel as are required by the application. The number of FIFOs and their size are only limited by the number of message objects available. A FIFO may be installed, resized and deinstalled any time, even during CAN operation.

The basic structure of a FIFO is shown in [Figure 22-15](#). A FIFO consists of a single base object (shown on the left side) and several slave objects (shown on the right side). The slave objects are chained together in the same list structure. The base object may be allocated to any list. Although [Figure 22-15](#) shows the base object as a separate item apart from the slave objects, it is also possible to integrate the base object at any place into the chain of slave objects, so that the base object is slave object, too (not possible for gateways). The FIFO structure fully relies on the list structure. The absolute object numbers of the message objects have no impact on the operation of the FIFO.

The base object needs not be allocated to the same list as the slave objects. Only the slave object must be allocated to a common list (as they are chained together). The BOT, CUR and TOP pointer link the base object to the slave objects, no matter whether the base object is allocated to the same or to another list than the slave objects.

The absolute minimum FIFO would consist of a single message object which is both FIFO base and FIFO slave (not very useful). The biggest possible FIFO would use all message objects of the MultiCAN module. Any sizes between these extremes are possible.

In the FIFO base object the boundaries of the FIFO are defined. The BOT field in the FIFO/Gateway Pointer Register of the base object points to the first (bottom) slave element in the FIFO. The TOP field in the FIFO/Gateway Pointer Register of the base object points to the last (top) slave element.

The CUR field in the FIFO/Gateway Pointer Register of the FIFO base object points to the actual slave object selected by the MultiCAN for message transfer. When a message transfer takes place with this object then CUR is moved to the next position. If CUR has already reached the top of the FIFO (CUR = TOP) then it is wrapped around to the bottom of the FIFO (CUR := BOT). Otherwise CUR is moved to the next message object in the list structure of the slave objects (CUR := PNEXT of current object). This scheme

Controller Area Network (MultiCAN) Controller

yields a circular FIFO structure where the fields BOT and TOP just establish the link from the last to the first element, which is missing in the linear structure.

The SEL field in the FIFO/Gateway Pointer register of the base object may be used for monitoring purposes. It allows to select any slave object and to generate a message interrupt if the CUR pointer reaches the value of SEL. Thus SEL offers a convenient way to determine the end of a predefined series of message transfers, or it may be used to issue a warning to the CPU when the FIFO gets full.

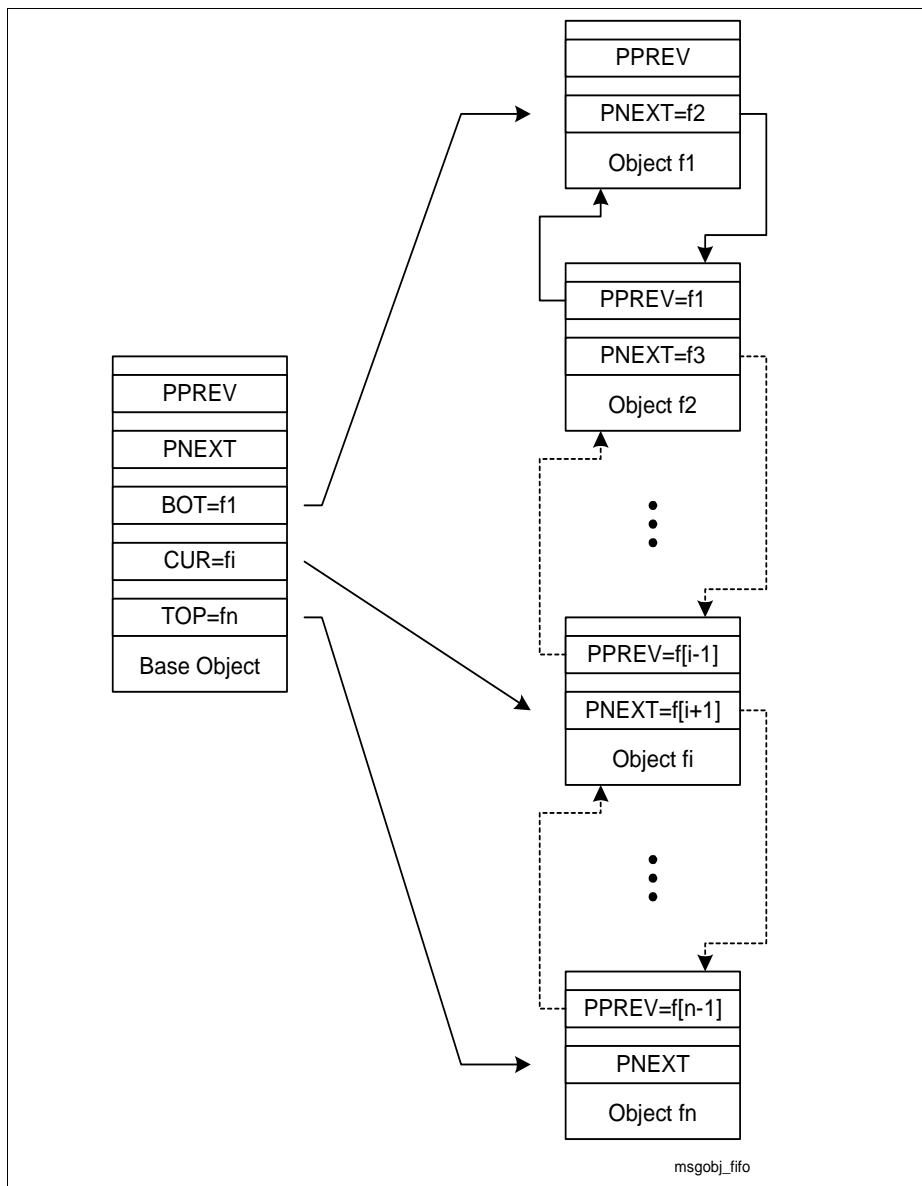


Figure 22-15 FIFO Structure with FIFO Base and n FIFO Destinations (Slaves)

22.2.9.5 Receive FIFO

The Receive FIFO structure is used to buffer incoming (received) remote or data frames. A Receive FIFO is selected via $MMC = 0001_B$ in the Message Object Function Control Register of the FIFO base object. This MMC code automatically designates the message object as FIFO base object. The message mode of the FIFO slave objects are not relevant for the operation of the Receive FIFO.

When the FIFO base object receives a frame from the CAN node it belongs to, then the frame is not stored in the base object. Instead the message is stored in the message object that is selected by the CUR pointer in the FIFO/Gateway Pointer Register of the FIFO base object.

The message object selected by CUR receives the CAN message as if it were the direct receiver of the message. However, $MMC = 0000_B$ is implicitly assumed for the FIFO slave, i.e. a standard message delivery is performed. The actual message mode (MMC) of the FIFO slave is ignored. There is also no extra acceptance filtering to match the received frame against the identifier, IDE bit and DIR bit of the slave object.

When the FIFO base object receives a CAN frame then the MultiCAN moves the current pointer CUR to the next message object in the FIFO structure, which will then be used to store the next incoming message. The old value of CUR is used for the current transfer.

If bit OVIE is set in the Message Object Function Register of the FIFO base object and the pointer CUR reaches the value stored in SEL then a FIFO overflow interrupt request is generated. The interrupt request is generated on interrupt output line TXINP (TXINP of the base object) immediately after the storage of the received frame into the slave object. Transmit interrupts are still generated if TXIE is set.

A CAN message is stored in a FIFO slave only if $MSGVAL = 1$ in both FIFO base and slave object.

In case that the Slave Objects of a Receive FIFO are members of a list of an active CAN node, then all of them should have the bit RXEN set to 0, receiving only the messages already filtered by the Base Object. Otherwise, any Slave Object with the RXEN bit set to 1 would operate additionally as an independent receive object according to its own acceptance filter setting.

In case that the Receive FIFO Slave Objects are members of a free list, not assigned to any CAN Node, then the setting of the bit RXEN is "don't care".

22.2.9.6 Transmit FIFO

The Transmit FIFO structure is used to buffer a series of data or remote frames to be transmitted.

A Transmit FIFO base object is selected via $MMC = 0010_B$ in the Message Object Function Control Register of the FIFO base object. Unlike the Receive FIFO the Transmit FIFO requires the explicit declaration of the FIFO slave objects via $MMC = 0011_B$. The CUR pointer of all slave objects must point back to the Transmit FIFO Base Object (to be initialized by user).

The TXEN1 bits of all message objects except the one which is selected by the CUR pointer of the base object must be cleared (to be initialized by user). TXEN1 of the message object selected by CUR must be set. CUR may be initialized to any FIFO slave object.

When tagging the message objects of the FIFO valid to start the operation of the FIFO then the base object must be tagged valid ($MSGVAL := 1$) first.

When a Transmit FIFO shall be deinstalled during operation, then the slave objects must be tagged invalid ($MSGVAL := 0$) first.

The Transmit FIFO uses the TXEN1 bit in the Message Object Control Register of all FIFO elements to select the actual message for transmission. Transmit acceptance filtering evaluates TXEN1 for each message object and a message object may win transit acceptance filtering only if TXEN1 is set. When a FIFO element has transmitted a message then in addition to standard transmit postprocessing (clear TXRQ, transmit interrupt etc.) the MultiCAN clears TXEN1 in that message object and moves the CUR pointer in the corresponding FIFO base object to the next message object to be transmitted. TXEN1 is set automatically in the next message object. Thus TXEN1 moves along the FIFO structure like a token to select the active element.

IF bit OVIE is set in the Message Object Function Register of the FIFO base object and the pointer CUR reaches the value stored in SEL then a FIFO overflow interrupt request is generated. The interrupt request is generated on interrupt output line as defined by RXINP (RXINP of the base object) when postprocessing of the received frame is done. Receive interrupts are still generated for the Transmit FIFO base object if bit RXIE is set.

22.2.9.7 Gateway Mode

The Gateway Mode allows to establish an automatic information transfer between two independent CAN bus systems without CPU interaction.

The Gateway Mode operates on message object level. In Gateway mode, information is transferred between two message objects, resulting in an information transfer between the two CAN nodes to which the message objects are allocated. A gateway may be established between any pair of CAN nodes and there may be as many gateways as there are message objects available to build the gateway structure.

Gateway Mode is selected via MMC = 0100_B in the Message Object Function Control Register of the gateway source object. The gateway destination object is selected by the CUR pointer in the FIFO/Gateway Pointer Register of the source object. The gateway destination object just needs to be valid (MSGVAL = 1), all other settings are not relevant for the information transfer from the source object to the destination object.

A gateway source object behaves like a standard message objects, but when a CAN frame has been received and stored in the source object, some additional actions are performed by the MultiCAN (**Figure 22-16**):

1. If bit DLCC is set in the Message Object Function Register of the source object, then the DLC code is copied from the source object to the destination object.
2. If bit IDC is set in the Message Object Function Register of the source object, then the identifier and the IDE bit are copied from the source object to the destination object.
3. If bit DATC is set in the Message Object Function Register of the source object, then the data field is copied from the source object to the destination object.
4. If bit GDFS is set in the Message Object Function Register of the source object, then TXRQ is set in the Message Object Control Register of the destination object.
5. RXPND and NEWDAT are set in the Message Object Control Register of the destination object.
6. A message interrupt request is generated for the destination object if RXIE is set in the Message Object Control Register of the destination object.
7. The current pointer CUR in the FIFO/Gateway Pointer Register of the source object is moved to the next destination object according to the FIFO rules as described in **Chapter 22.2.9.4**. A gateway with a single (static) destination object is obtained by means of setting TOP = BOT = CUR = destination object.

The link from the source to the destination object works in the same way as the link from a FIFO source to a FIFO slave. This means that a gateway with an integrated destination FIFO may be created (**Figure 22-15**), where the object on the left in **Figure 22-15** is the gateway source object and the message objects on the right side are the gateway destination objects.

The gateway works in the same way for the reception of data frames (source object is receive object, i.e. DIR = 0) as well as for the reception of remote frames (source object is transmit object).

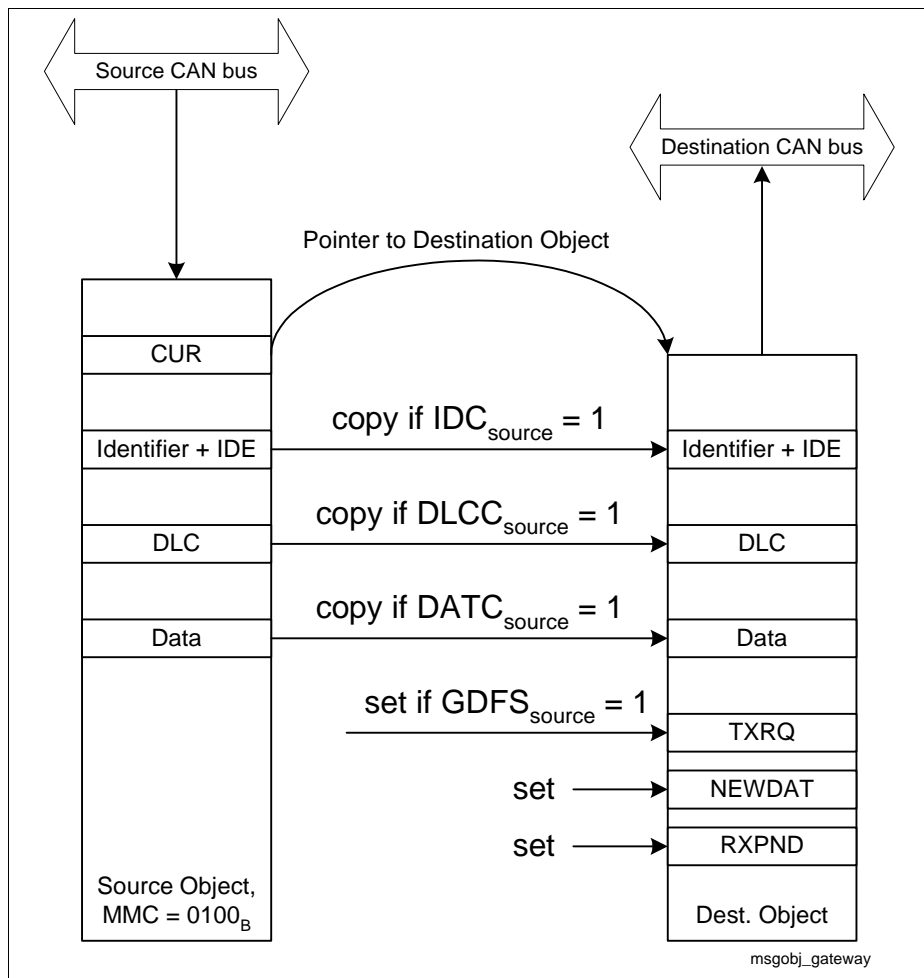


Figure 22-16 Gateway Transfer from Source to Destination

22.2.9.8 Foreign Remote Requests

When a remote frame received on a CAN node is stored in a message object, then a transmit request is set in order to trigger the answer (data frame transmission) to the request or to automatically issue a secondary request. If bit FRREN is cleared (FRREN = 0) in the Function Control register of the message object where the remote request is stored, then TXRQ is set in the Control Register of the same message object.

If bit FRREN is set (FRREN = 1: foreign remote request enabled) then TXRQ is set in the message object that is referenced by pointer CUR in the FIFO/Gateway Pointer Register. The value of CUR is, however, not changed by this feature.

Although the foreign remote request feature works independently from the selected message mode, it is especially useful for gateways to issue a remote request on the source of a gateway upon the reception of a remote request on the gateway destination. According to the setting of FRREN in the gateway destination object there are two ways to handle remote requests that appear on the destination side (assuming that the source object is a receive object and the destination is a transmit object, i.e. $DIR_{source} = 0$ and $DIR_{destination} = 1$):

FRREN = 0 in the Gateway Destination Object

1. A remote frame is received by gateway destination.
2. TXRQ is set automatically in the gateway destination object.
3. A data frame with the current data stored in the destination object is transmitted on the destination bus.

FRREN = 1 in the Gateway Destination Object

1. A remote frame is received by gateway destination.
2. TXRQ is set automatically in the gateway source object (must be referenced by CUR pointer of the destination object).
3. A remote request is transmitted by the source object (which is a receive object) on the source CAN bus.
4. The receiver of the remote request responds with a data frame on the source bus.
5. The data frame is stored in the source object.
6. The data frame is copied to the destination object (gateway action).
7. TXRQ is set in the destination object (assuming $GDFS_{source} = 1$).
8. The new data stored in the destination object is transmitted on the destination bus, as response to the initial remote request on the destination bus.

22.2.10 MultiCAN Kernel Registers

The register set of the MultiCAN module consists of three distinct subsets:

1. The **Global Module Registers** apply to the whole MultiCAN module and exist only once.
2. The **CAN Node Registers** apply to a single CAN node and thus exist once for each CAN node.
3. The collection of **Message Object Registers** defines a single message object and thus exists once for each message object.

22.2.10.1 Register Address Map

Table 22-5 shows the address map of the MultiCAN module with respect to the base address of the MultiCAN module.

Table 22-5 MultiCAN Address Map (Relative to MultiCAN Base Address)

Register Group	Start address	Total Range
Global Module Registers	+100 _H	+100 _H to + 1FF _H
CAN Node Registers for CANx, x = 0 - 5	+200 _H	+200 _H to + 7FF _H
Message Objects n = 0 - 255	+1000 _H	+1000 _H to + 2FFF _H

Global Module Registers

The global module registers exist only once. They are listed in [Table 22-6](#) with their relative address with respect to the start address of the Global Module Registers.

Table 22-6 Relative Addresses of Global Module Registers

Register	Rel. Address	Full Name of Register
LIST0L	100 _H	List Registers 0 Low
LIST0H	102 _H	List Registers 0 High
LIST1L	104 _H	List Registers 1 Low
LIST1H	106 _H	List Registers 1 High
LIST2L	108 _H	List Registers 2 Low
LIST2H	10A _H	List Registers 2 High
LIST3L	10C _H	List Registers 3 Low
LIST3H	10E _H	List Registers 3High
LIST4L	110 _H	List Registers 4 Low
LIST4H	112 _H	List Registers 4 High
LIST5L	114 _H	List Registers 5 Low
LIST5H	116 _H	List Registers 5 High
LIST6L	118 _H	List Registers 6 Low
LIST6H	11A _H	List Registers 6 High
LIST7L	11C _H	List Registers 7 Low
LIST7H	11E _H	List Registers 7 High
MSPND0L	140 _H	Message Pending Registers 0 Low
MSPND0H	142 _H	Message Pending Registers 0 High
MSPND1L	144 _H	Message Pending Registers 1 Low
MSPND1H	146 _H	Message Pending Registers 1 High
MSPND2L	148 _H	Message Pending Registers 2 Low
MSPND2H	14A _H	Message Pending Registers 2 High
MSPND3L	14C _H	Message Pending Registers 3 Low
MSPND3H	14E _H	Message Pending Registers 3 High
MSPND4L	150 _H	Message Pending Registers 4 Low
MSPND4H	152 _H	Message Pending Registers 4 High
MSPND5L	154 _H	Message Pending Registers 5 Low

Controller Area Network (MultiCAN) Controller

Table 22-6 Relative Addresses of Global Module Registers

Register	Rel. Address	Full Name of Register
MSPND5H	156 _H	Message Pending Registers 5 High
MSPND6L	158 _H	Message Pending Registers 6 Low
MSPND6H	15A _H	Message Pending Registers 6 High
MSPND7L	15C _H	Message Pending Registers 7 Low
MSPND7H	15E _H	Message Pending Registers 7 High
MSID0	180 _H	Message Index Registers 0
MSID1	184 _H	Message Index Registers 1
MSID2	188 _H	Message Index Registers 2
MSID3	18C _H	Message Index Registers 3
MSID4	190 _H	Message Index Registers 4
MSID5	194 _H	Message Index Registers 5
MSID6	198 _H	Message Index Registers 6
MSID7	19C _H	Message Index Registers 7
MSIMASKL	1C0 _H	Message Index Mask Register Low
MSIMASKH	1C2 _H	Message Index Mask Register High
PANCTRL	1C4 _H	Panel Control Register Low
PANCTRH	1C6 _H	Panel Control Register High
MCR	1C8 _H	Module Control Register
MITR	1CC _H	Module Interrupt Trigger Register
-	+120 _H ... +13E _H +148 _H ... +17E _H +188 _H ... +1BE _H +1CE _H ... +1FE _H	Reserved

CAN Node Registers

The registers of a CAN node are located at consecutive 32 bit addresses according to [Table 22-7](#) which shows the relative address of the 32 bit CAN Node Registers with respect to the base address of CAN node register block. The CAN Node Register block exists once for each CAN node.

Table 22-7 Relative Addresses of CAN Node Registers

Register	Rel. Address	Full Name of Register
NCR	+00 _H	CAN Node Control Register
NSR	+04 _H	CAN Node Status Register
NIPR	+08 _H	CAN Node Interrupt Pointer Register
NPCR	+0C _H	CAN Node Port Control Register
NBTRL	+10 _H	CAN Node Bit Timing Register Low
NBTRH	+12 _H	CAN Node Bit Timing Register High
NECNTL	+14 _H	CAN Node Error Counter Register Low
NECNTH	+16 _H	CAN Node Error Counter Register High
NFCRL	+18 _H	CAN Node Frame Counter Register Low
NFCRH	+1A _H	CAN Node Frame Counter Register High
-	+1C _H to +FE _H	Reserved

Message Object Registers

The registers of a message object are located at consecutive 32 bit addresses according to [Table 22-8](#) which shows the relative address of the 32 bit Message Object Registers with respect to the base address of the Message Object.

Table 22-8 Relative Addresses of Message Object Registers

Register	Rel. Address	Full Name of Register
MOFCRL	+00 _H	Message Object Function Control Register Low
MOFCRH	+02 _H	Message Object Function Control Register High
MOFGPRL	+04 _H	Message Object FIFO/Gateway Pointer Reg. Low
MOFGPRH	+06 _H	Message Object FIFO/Gateway Pointer Reg. High
MOIPRL	+08 _H	Message Object Interrupt Pointer Register Low
MOIPRH	+0A _H	Message Object Interrupt Pointer Register High
MOAMRL	+0C _H	Message Object Acceptance Mask Register Low
MOAMRH	+0E _H	Message Object Acceptance Mask Register High
MODATALL	+10 _H	Message Object Data Register Low Low
MODATALH	+12 _H	Message Object Data Register Low High
MODATAHL	+14 _H	Message Object Data Register High Low

Controller Area Network (MultiCAN) Controller

Table 22-8 Relative Addresses of Message Object Registers

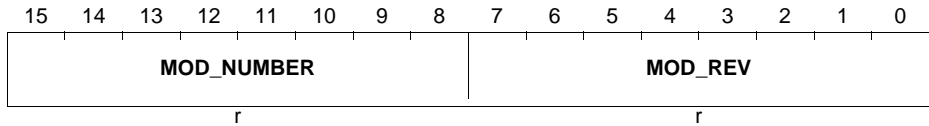
Register	Rel. Address	Full Name of Register
MODATAHH	+16 _H	Message Object Data Register High High
MOARL	+18 _H	Message Object Arbitration Register Low
MOARH	+1A _H	Message Object Arbitration Register High
MOCTRL	+1C _H	Message Object Control Register Low
MOCTRH	+1E _H	Message Object Control Register High
MOSTATL	+1C _H	Message Object Control Register Low
MOSTATH	+1E _H	Message Object Status Register High

Registers Description

22.2.10.2 Module Identification Register

ID

Module Identification Register (08_H) **Reset Value: 40XX_H**



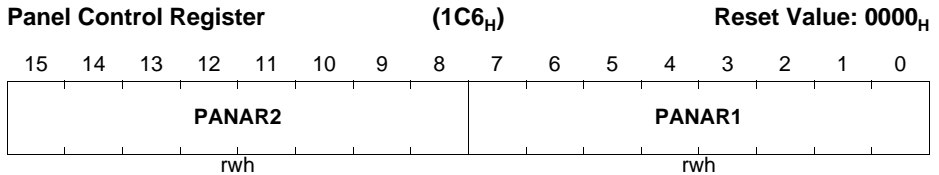
Field	Bits	Type	Description
MOD_REV	[7:0]	r	Module Revision Number Value Bits 7-0 bits are used for module revision numbering. The value of the module revision number starts with 01 _H (first revision), 02 _H , 03 _H , ... up to FF _H .
MOD_NUMBER	[15:8]	r	Module Identification Number Value Bits 15-8 are used for module identification. The MultiCAN has the module number 40 _H .

22.2.10.3 Command Panel

All list operations such as allocation, deallocation and relocation of message objects within the list structure are performed via the Command Panel. It is not possible to modify the list structure directly by means of writing to the message objects and the LIST registers.

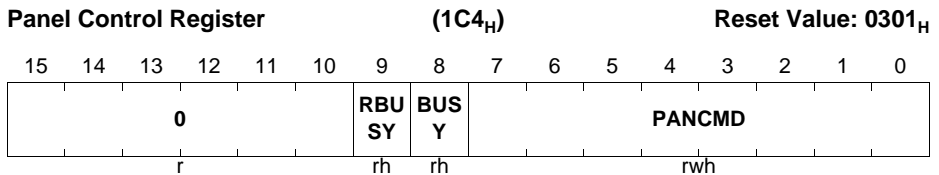
A new command is started by means of writing the command arguments and the command code to the Panel Control Register.

PANCTR



Field	Bits	Type	Description
PANAR1	[7:0]	rwh	Panel Argument 1
PANAR2	[15:8]	rwh	Panel Argument 2

PANCTRL



Field	Bits	Type	Description
PANCMD	[7:0]	rwh	Panel Command A new command is started by means of writing the command number to PANCMD. At the end of a panel command the NOP (no operation) command code is automatically written to PANCMD.
BUSY	8	rh	Panel Busy 0 _B Panel has finished command and is ready to accept a new command. 1 _B Panel operation is in progress.

Controller Area Network (MultiCAN) Controller

Field	Bits	Type	Description
RBUSY	9	rh	Result Busy 0_B No update of PANAR1 and PANAR2 is scheduled by the list controller. 1_B A list command is running (BUSY = 1) that will write results to PANAR1 and PANAR2, but the results are not yet available.
0	[15:10]	r	reserved; returns '0' if read; should be written with '0';

Controller Area Network (MultiCAN) Controller

Panel Commands

A panel operation consists of a command code to be written to PANCMD and up to 2 panel arguments (PANAR1, PANAR2). Commands that have a return value deliver it to the PANAR1 field. Commands that deliver an error flag post it to bit 7 of PANAR2.

Table 22-9 Panel Commands

Code	PANAR2	PANAR1	Command Description
0			No Operation Writing value 0 to PANCMD has no effect. No new command is started.
1	Result: Bit 7 : ERR Bit 6-0 : undefined		Initialize Lists Run the initialization sequence to reset the CTRL and LIST field of all message objects and the list registers LIST[7:0] to their reset values. This results in the deallocation of all message objects. The initialization command requires that bits INIT and CCE are set in the Node Control Register of all CAN nodes 0-5. An ERR bit (bit 7 of PANAR2) reports the success of the operation: 0Success 1Not all INIT and CCE bits are set. Thus no initialization is performed. The initialization command is automatically performed with each reset of the MultiCAN module, but with the exception that all message object registers are reset.
2	Argument: List Index	Argument: Message Object Number	Static Allocate Allocate a given message object to a list. The message object is removed from the list that it currently belongs to and appended to the end of the list, given by PANAR2. This command is also used to deallocate a message object. In this case the target list is the list of unallocated elements. (PANAR2 = 0).

Controller Area Network (MultiCAN) Controller

Table 22-9 Panel Commands

Code	PANAR2	PANAR1	Command Description
3	Argument: List Index Result: Bit 7 : ERR Bit 6-0 : undefined	Result: Message Object Number	Dynamic Allocate Allocate the first message object of the list of unallocated objects to the selected list. The message object is appended to the end of the list. The message number of the message object is returned in PANAR1. An ERR bit (bit 7 of PANAR2) reports the success of the operation: 0Success. 1The operation has not been performed because the list of unallocated elements was empty.
4	Argument: Destination Object Number	Argument: Source Object Number	Static Insert Before Remove a message object (source object) from the list that it currently belongs to and insert it before a given destination object into the list structure of the destination object. The source object thus becomes the predecessor of the destination object.
5	Argument: Destination Object Number Result: Bit 7 : ERR Bit 6-0 : undefined	Result: Object Number of inserted object	Dynamic Insert Before Insert a new message object before a given destination object. The new object is taken from the list of unallocated elements (the first element is chosen). The number of the new object is delivered as result to PANAR1. An ERR bit (bit 7 of PANAR2) reports the success of the operation: 0Success. 1The operation has not been performed because the list of unallocated elements was empty.
6	Argument: Destination Object Number	Argument: Source Object Number	Static Insert Behind Remove a message object (source object) from the list that it currently belongs to and insert it behind a given destination object into the list structure of the destination object. The source object thus becomes the successor of the destination object.

Controller Area Network (MultiCAN) Controller

Table 22-9 Panel Commands

Code	PANAR2	PANAR1	Command Description
7	Argument: Destination Object Number Result: Bit 7 : ERR Bit 6-0 : undefined	Result: Object Number of inserted object	Dynamic Insert Behind Insert a new message object behind a given destination object. The new object is taken from the list of unallocated elements (the first element is chosen). The number of the new object is delivered as result to PANAR1. An ERR bit (bit 7 of PANAR2) reports the success of the operation: 0Success. 1The operation has not been performed because the list of unallocated elements was empty.
8 - 255	-	-	Reserved

Controller Area Network (MultiCAN) Controller

22.2.10.4 Module Setup

The Module Control Register contains basic settings to define the operation of the module.

MCR

Module Control Register

(1C8_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPSEL										0					
rw										r					

Field	Bits	Type	Description
MPSEL	[15:12]	rw	<p>Message Pending Selector</p> <p>MPSEL allows to calculate the bit position of the message pending bit to be set after a message reception/transmission interrupt from a mixture of RXINP, TXINP and MPN (Message Pending Number). With the definitions</p> <p>INP ... RXINP upon message reception, TXINP upon message transmission</p> <p>MPN ... 8 bit message pending number</p> <p>the effective position of the message pending bit is calculated according to the formula</p> $POS = ((INP \& MPSEL) \ll 4) \mid (MPN \& (\sim MPSEL \ll 4)) \mid (MPN \& = 0x0F_H)$ <p>If MPSEL = 0 then the position is simply given by the message pending number MPN.</p> <p>If MPSEL = 1111_B then the upper 4 bits of the position is given by the interrupt output line pointer INP and the lower 4 bits are taken from MPN.</p>
0	[11:0]	r	<p>reserved;</p> <p>returns '0' if read; should be written with '0';</p>

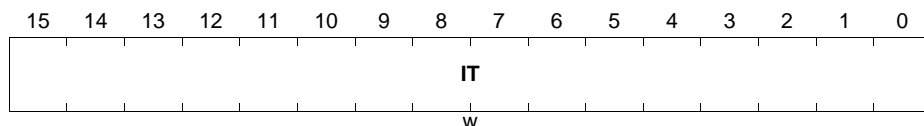
Controller Area Network (MultiCAN) Controller

22.2.10.5 Interrupt Trigger Register ITR

The Interrupt Trigger Register ITR allows to trigger interrupt requests on each interrupt output line by software.

MITR

Module Interrupt Trigger Register (1CC_H) **Reset Value: 0000_H**



Field	Bits	Type	Description
IT	[15:0]	w	Interrupt Trigger Writing value 1 to bit n (n = 15-0) generates an interrupt request on interrupt output line n. Writing value 0 has no effect. Reading delivers always 0. More than one interrupt request may be generated at the same time by means of writing 1 to several bit positions of IT with a single write access.

22.2.10.6 List Pointer

Each CAN node has an own list which defines the message objects that are allocated to the respective node. In addition to that there is the list of all unallocated objects and finally a general purpose user list which is not associated to a CAN node. Each list is assigned a list index according to [Table 22-3 “List Indices” on Page 22-15](#).

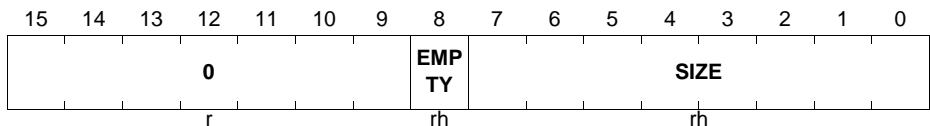
Each list is terminated with a List Register which defines the first and the last element in the list.

LIST0H

List Register 0 High (102_H) Reset Value: 00FF_H

LISTyH (y = 1-7)

List Register y High (102_H+y*4) Reset Value: 0100_H



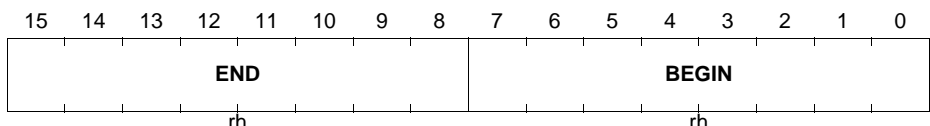
Field	Bits	Type	Description
SIZE	[7:0]	rh	Size of List The number of elements in the list l is given by $\#elements = SIZE + 1$, provided the list is not empty. If the list l is empty, the value of SIZE is zero.
EMPTY	8	rh	List Empty Indication 0_B At least one message object is allocated to list l. 1_B No message object is allocated to the list l.
0	[15:9]	r	Reserved; read as 0; should be written with 0.

LIST0L

List Register 0 Low (100_H) Reset Value: FF00_H

LISTxL (x = 1-7)

List Register x Low (100_H+x*4) Reset Value: 0000_H



Controller Area Network (MultiCAN) Controller

Field	Bits	Type	Description
BEGIN	[7:0]	rh	List Begin Pointer to the first message object in the list l.
END	[15:8]	rh	END Pointer Pointer to the last message object in the list l.

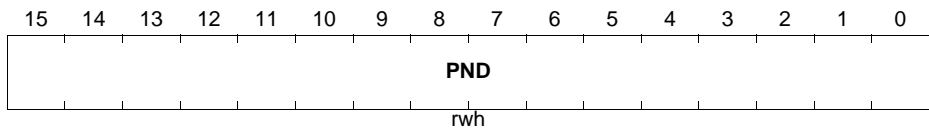
22.2.10.7 Message Notifications

When a message object generates an interrupt request upon the transmission or reception of a message, then the request is routed to the interrupt output line selected by TXINP or RXINP of the message object. As there are more message objects than interrupt output lines, an interrupt routine typically processes requests from more than one message object. Therefore a priority selection mechanism is implemented in the MultiCAN module to select the highest priority object within a collection of message objects. The Message Pending Register contains the interrupt pending.

MSPNDkH (k = 0-7)

Message Pending Register k High ($142_H + k \cdot 4$)

Reset Value: 0000_H

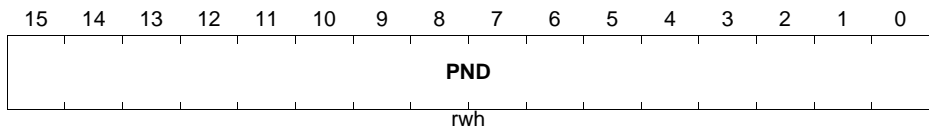


Field	Bits	Type	Description
PND[31:16]	[15:0]	rwh	Message Pending When a message interrupt occurs then the message object sets a bit in one of the MSPND register, where the bit position is given by the MPN[4:0] field of the IPR register of the message object. The register selection n is given by the higher bits of MPN. The register bits may be cleared by SW (write 0), but writing 1 has no effect.

MSPNDkL (k = 0-7)

Message Pending Register k Low ($140_H + k \cdot 4$)

Reset Value: 0000_H



Field	Bits	Type	Description
PND[15:0]	[15:0]	rwh	Message Pending The same as PND[31:16]

Controller Area Network (MultiCAN) Controller

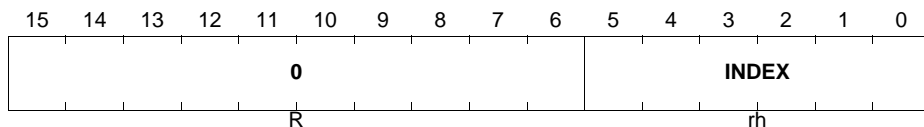
Each Message Pending Register has a Message Index Register associated to it. The Message Index Register shows the active (set) pending bit with lowest bit position within groups of pending bits.

MSIDk (k = 0-7)

Message Index Register k

(180_H+k*4)

Reset Value: 0020_H



Field	Bits	Type	Description
INDEX	[5:0]	rh	Message Pending Index The value of INDEX is given by the bit position i of the pending bit of MSPNDk with the following properties: 1. MSPNDk[i] & IM[i] = 1 2. i = 0 or MSPNDk[i-1:0] & IM[i-1:0] = 0 If no bit of MSPNDk satisfies these conditions then INDEX reads 100000 _B . Thus INDEX shows the position of the first pending bit of MSPNDk, where only those bits of MSPNDk which are selected in the Message Index Mask Register are taken into account.
0	[15:6]	r	Reserved: read as 0; should be written with 0.

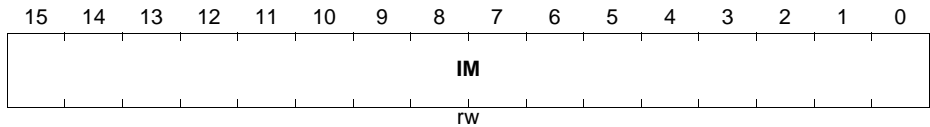
Controller Area Network (MultiCAN) Controller

The Message Index Mask Register selects individual bits for the calculation of the Message Pending Index. The Message Index Mask Register is used commonly for all Message Pending registers and their associated Message Index registers.

MSIMASKH

Message Index Mask Register High (1C2_H)

Reset Value: 0000_H

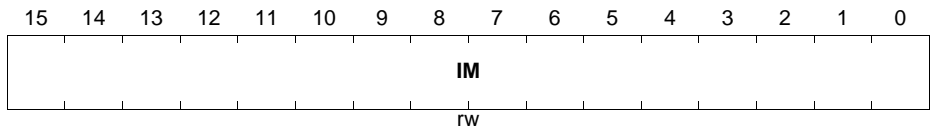


Field	Bits	Type	Description
IM[31:16]	[15:0]	rw	Message Index Mask Only those bits in MSPNDk for which the corresponding Index Mask bits are set contribute to the calculation of the Message Index.

MSIMASKL

Message Index Mask Register Low (1C0_H)

Reset Value: 0000_H



Field	Bits	Type	Description
IM[15:0]	[15:0]	rw	Message Index Mask Only those bits in MSPNDk for which the corresponding Index Mask bits are set contribute to the calculation of the Message Index.

22.2.11 CAN Node Specific Registers

The CAN node specific registers exist once for each CAN node of the MultiCAN module. They contain information that is directly related to the operation of the CAN nodes and which may not be shared among the nodes.

The Node Control Register contains basic settings that define the operation of the CAN node and the interaction of the CAN node with the message objects.

Controller Area Network (MultiCAN) Controller

NCRx (x = 0-5)

Node x Control Register

(200_H+x*100_H)

Reset Value: 0001_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							SUS EN	CAL M	CCE	0	CAN DIS	ALIE	LECI E	TRIE	INIT
r							rw	rw	rw	r	rw	rw	rw	rw	rwh

Field	Bits	Type	Description
INIT	0	rwh	<p>Node Initialization</p> <p>0_B Resetting bit INIT enables the participation of the node in the CAN traffic. If the CAN node is in the bus off state then the ongoing bus off recovery (which does not depend on the INIT bit) is continued. With the end of the bus off recovery sequence the CAN node is allowed to take part in the CAN traffic. If the CAN node is not in the bus off state a sequence of 11 consecutive recessive bits must be detected before the node is allowed to take part in the CAN traffic.</p> <p>1_B Setting this bit terminates the participation of this node in the CAN traffic. Any ongoing frame transfer is cancelled and the transmit line goes recessive. If the CAN node is in the bus off state then the running bus off recovery sequence is continued. If the INIT bit is still set after the successful completion of the bus off recovery sequence, i.e. after detecting 128 sequences of 11 consecutive recessive bits (11 *1) then the CAN node leaves the bus off state but remains inactive as long as INIT remains set.</p> <p>Bit INIT is automatically set when the CAN node becomes 'bus off' (see Page 22-12).</p>
TRIE	1	rw	<p>Transfer Interrupt Enable</p> <p>If this bit is set, then an interrupt request is generated upon the successful reception or transmission of a CAN frame. The interrupt output line is selected by TRINP in the CAN Node Interrupt Pointer Register.</p>

Controller Area Network (MultiCAN) Controller

Field	Bits	Type	Description
LECIE	2	rw	LEC indicated Error Interrupt Enable If this bit is set, then an interrupt request is generated upon each update of the LEC field in the Node Status Register leading to LEC > 0 (CAN protocol error). The interrupt output line is selected by LECINP in the CAN Node Interrupt Pointer Register.
ALIE	3	rw	Alert Interrupt Enable If this bit is set then an alert interrupt is generated on one of the following events: <ol style="list-style-type: none"> 1) A change of bit BOFF in the CAN Node Status Register. 2) A change of bit EWRN in the CAN Node Status Register. 3) A List Length Error, which also sets bit LLE in the CAN Node Status Register. 4) A List Object Error, which also sets bit LOE in the CAN Node Status Register. 5) Bit INIT has been set by the MultiCAN. The interrupt is requested on the interrupt output line selected by ALINP in the CAN Node Interrupt Pointer Register.
CANDIS	4	rw	CAN Disable Setting this bit disables the CAN node. The CAN node first waits until it is BUS IDLE or BUS OFF. Then bit INIT is automatically set and an alert interrupt is generated if bit ALIE is set.
CCE	6	rw	Configuration Change Enable 0 _B The Bit Timing Register, the Port Control Register and the Error Counter Register may only be read. All attempts to modify them are ignored. 1 _B The Bit Timing Register, the Port Control Register and the Error Counter Register may be read and written.

Controller Area Network (MultiCAN) Controller

Field	Bits	Type	Description
CALM	7	rw	Can Analyze Mode If this bit is set then the CAN node operates in analyze mode. This means that messages may be received, but not transmitted. No acknowledge is sent on the CAN bus upon frame reception. Active error flags are sent recessive instead of dominant. The transmit line is continuously held at recessive (1) level. Bit CALM can be written only while bit INIT is set.
SUSEN	8	rw	Suspend Enable This bit allows to set the CAN node into suspend mode via OCDS (on chip debug support): 0 _B An OCDS suspend trigger is ignored by the CAN node. 1 _B An OCDS suspend trigger disables the CAN node: As soon as the CAN node becomes BUS IDLE or BUS OFF bit INIT is internally forced to '1' to disable the CAN node. The actual value of bit INIT remains unchanged. Bit SUSEN is reset via OCDS Reset.
0	5, [15:9]	r	Reserved; read as 0; should be written with 0.

Controller Area Network (MultiCAN) Controller

The Node Status Register reports errors as well as successfully transferred CAN frames.

NSRx (x = 0-5)

Node x Status Register

(204_H+x*100_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0					SUS ACK	LOE	LLE	BOF F	EWR N	ALE RT	RXO K	TXO K	LEC		
r					rh	rwh	rwh	rh	rh	rwh	rwh	rwh	rwh		

Field	Bits	Type	Description
LEC	[2:0]	rwh	Last Error Code The encoding of this bit field is detailed in Table 22-10 .
TXOK	3	rwh	Message Transmitted Successfully 0 _B No successful transmission since last flag reset. 1 _B A message has been transmitted successfully (error free and acknowledged by at least another node). TXOK must be reset by software (write 0). Writing 1 has no effect.
RXOK	4	rwh	Message Received Successfully 0 _B No successful reception since last flag reset. 1 _B A message has been received successfully. RXOK must be reset by software (write 0). Writing 1 has no effect.
ALERT	5	rwh	Alert Warning The ALERT bit is set upon the occurrence of one of the following events (the same events which also trigger an alert interrupt if ALIE is set): <ol style="list-style-type: none"> 1) A change of bit BOFF in the CAN Node Status Register. 2) A change of bit EWRN in the CAN Node Status Register. 3) A List Length Error, which also sets bit LLE in the CAN Node Status Register. 4) A List Object Error, which also sets bit LOE in the CAN Node Status Register. 5) Bit INIT has been set by the MultiCAN. ALERT must be reset by software (write 0). Writing 1 has no effect.

Controller Area Network (MultiCAN) Controller

Field	Bits	Type	Description
EWRN	6	rh	Error Warning Status 0_B No warning limit exceeded. 1_B One of the error counters REC or TEC reached the warning limit EWRNLVL.
BOFF	7	rh	Bus-off Status 0_B CAN controller is not in the bus-off state. 1_B CAN controller is in the bus-off state.
LLE	8	rwh	List Length Error 0_B No list length error since last flag reset. 1_B A list length error has been detected during message acceptance filtering. The number of elements in the list that belongs to this CAN node differs from the list SIZE given in the list termination pointer. LLE must be reset by software (write 0). Writing 1 has no effect.
LOE	9	rwh	List Object Error 0_B No list object error since last flag reset. 1_B A list object error has been detected during message acceptance filtering. A message object with wrong LIST index entry in the Message Object Control Register has been detected. LOE must be reset by software (write 0). Writing 1 has no effect.
SUSACK	10	rh	Suspend Acknowledge 0_B The CAN node is not in suspend mode or a suspend request is pending, but the CAN node has not yet reached BUS IDLE or BUS OFF. 1_B The CAN node is in suspend mode: The CAN node is inactive (bit NCR.INIT internally forced to '1') due to an OCDS suspend request.
0	[15:11]	r	Reserved; read as 0; should be written with 0.

Encoding of the LEC Bitfield

Table 22-10 Encoding of the LEC Bit Field

LEC Value	Signification
000 _B	<u>No Error:</u> No error was detected for the last message on the CAN bus.
001 _B	<u>Stuff Error:</u> More than 5 equal bits in a sequence have occurred in a part of a received message where this is not allowed.
010 _B	<u>Form Error:</u> A 'fixed format part' of a received frame has the wrong format.
011 _B	<u>Ack Error:</u> The transmitted message was not acknowledged by another node.
100 _B	<u>Bit1 Error:</u> During a message transmission the CAN node tried to send a recessive level (1) outside the arbitration field and the acknowledge slot, but the monitored bus value was dominant.
101 _B	<u>Bit0 Error:</u> Two different conditions are signalled by this code: a) During transmission of a message (or acknowledge bit, active error flag, overload flag) the CAN node tried to send a dominant level (0), but the monitored bus value was recessive. b) During bus-off recovery this code is set each time a sequence of 11 recessive bits has been monitored. The CPU may use this code as indication that the bus is not continuously disturbed.
110 _B	<u>CRC Error:</u> The CRC checksum of the received message was incorrect.
111 _B	<u>CPU write to LEC:</u> Whenever the the CPU writes the value 111 to LEC, it takes the value 111. Whenever the CPU writes another value to LEC, the written LEC value is ignored.

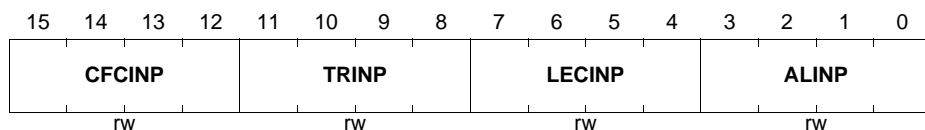
Controller Area Network (MultiCAN) Controller

The Node Interrupt Pointer Register connects each interrupt request source of the CAN node to one of the up to 16 available interrupt output lines.

NIPRx (x = 0-5)

Node x Interrupt Pointer Register (208_H+x*100_H)

Reset Value: 0000_H



Field	Bits	Type	Description
ALINP	[3:0]	rw	Alert Interrupt Node Pointer Number of interrupt output line INT_Om (m=0-15) reporting the “Alert Interrupt Request”, if enabled by ALIE = 1.
LECINP	[7:4]	rw	Last Error Code Interrupt Node Pointer Number of interrupt output line INT_Om (m=0-15) reporting the “Last Error Interrupt Request”, if enabled by LECIE = 1.
TRINP	[11:8]	rw	Transfer OK Interrupt Node Pointer Number of interrupt output line INT_Om (m=0-15) reporting the “Transfer Interrupt Request”, if enabled by TRIE.
CFCINP	[15:12]	rw	Frame Counter Interrupt Node Pointer Number of interrupt output line INT_Om (m=0-15) reporting the “Frame Counter Overflow Interrupt Request”, if enabled by CFCIE = 1.

Controller Area Network (MultiCAN) Controller

The Node Port Control Register configures the CAN bus transmit/receive ports. NPCRx may be written only if bit NCRx.CCE is set.

NPCRx (x = 0-5)

Node x Port Control Register

(20C_H+x*100_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							LBM	0					RXSEL		
r							rw	r					rw		

Field	Bits	Type	Description
RXSEL	[2:0]	rw	Receive Select RXSEL selects one out of 8 possible receive inputs. CAN traffic is performed through the selected input. The other inputs are ignored. See also Chapter 22.4.4
LBM	8	rw	Loop Back Mode 0 _B Loop back mode is disabled. 1 _B Loop back mode is enabled. This node is connected to an internal (virtual) loop back CAN bus. All CAN nodes which are in loop back mode are connected to this virtual CAN bus so that they can communicate with each other internally. The external transmit line is forced recessive in loop back mode.
0	[7:3], [15:9]	r	Reserved; read as 0; should be written with 0.

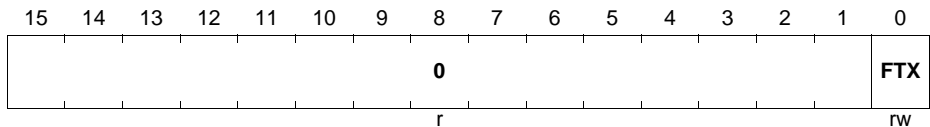
Controller Area Network (MultiCAN) Controller

The Node Bit Timing Register contains all parameters to setup the bit timing for the CAN transfer. NBTRx may be written only if bit NCRx.CCE is set.

NBTRxH (x = 0-5)

Node x Bit Timing Register High (212_H+x*100_H)

Reset Value: 0000_H



Field	Bits	Type	Description
FTX	0	rw	Fast Transmit (TTC only) When a message is requested for transmission on the CAN bus, then the start of frame (SOF) symbol is sent with the beginning of a new bit time. If the CAN bus is in the idle state and bit FTX is set (FTX = 1) then a new bit time is started immediately with the transmit trigger of a new message. This eliminates the variable delay between the transmit trigger of a message and the actual SOF signal on the transmit output. Such a variable delay occurs when transmit triggers occur at different positions within a CAN bit time.
0	[15:1]	r	reserved; returns '0' if read; should be written with '0';

Controller Area Network (MultiCAN) Controller

NBTRxL (x = 0-5)

Node x Bit Timing Register Low ($210_H + x \cdot 100_H$)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIV8		TSEG2		TSEG1			SJW		BRP						
rw		rw		rw			rw		rw						

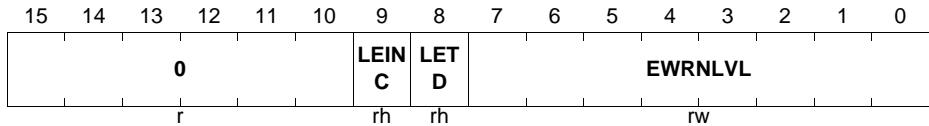
Field	Bits	Type	Description
BRP	[5:0]	rw	Baud Rate Prescaler The duration of one time quantum is given by (BRP + 1) clock cycles if DIV8 = 0. The duration of one time quantum is given by $8 \times (\text{BRP} + 1)$ clock cycles if DIV8 = 1.
SJW	[7:6]	rw	(Re)Synchronization Jump Width (SJW + 1) time quanta are allowed for resynchronization.
TSEG1	[11:8]	rw	Time Segment Before Sample Point (TSEG1 + 1) time quanta is the user defined nominal time between the end of the synchronization segment and the sample point. It includes the propagation segment, which takes into account signal propagation delays. The time segment may be lengthened due to resynchronization. Valid values for TSEG1 are 2 to 15.
TSEG2	[14:12]	rw	Time Segment After Sample Point (TSEG2 + 1) time quanta is the user defined nominal time between the sample point and the start of the next synchronization segment. It may be shortened due to resynchronization. Valid values for TSEG2 are 1 to 7.
DIV8	15	rw	Divide Prescaler Clock by 8 0 _B A time quantum lasts (BRP+1) clock cycles. 1 _B A time quantum lasts $8 \times (\text{BRP}+1)$ clock cycles.

Controller Area Network (MultiCAN) Controller

NECNTxH (x = 0-5)

Node x Error Counter Register High(216_H+x*100_H)

Reset Value: 0060_H

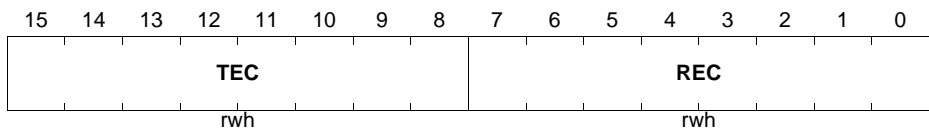


Field	Bits	Type	Description
EWRNLVL	[7:0]	rw	Error Warning Level Bit field EWRNLVL defines the threshold value (warning level, default 96) to be reached in order to set the corresponding error warning bit EWRN.
LETD	8	rh	Last Error Transfer Direction 0 _B The last error occurred while the CAN node was receiver (REC has been incremented). 1 _B The last error occurred while the CAN node was transmitter (TEC has been incremented).
LEINC	9	rh	Last Error Increment 0 _B The last error led to an error counter increment of 1. 1 _B The last error led to an error counter increment of 8.
0	[15:10]	r	Reserved; read as 0; should be written with 0.

NECNTxL (x = 0-5)

Node x Error Counter Register Low(214_H+x*100_H)

Reset Value: 0000_H



Controller Area Network (MultiCAN) Controller

Field	Bits	Type	Description
REC	[7:0]	rwh	Receive Error Counter Bit field REC contains the value of the receive error counter of the CAN node.
TEC	[15:8]	rwh	Transmit Error Counter Bit field TEC contains the value of the transmit error counter of the CAN node.

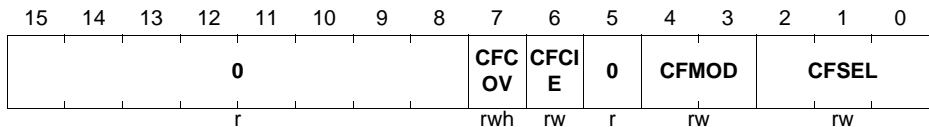
Controller Area Network (MultiCAN) Controller

The Node Frame Counter Register contains the actual value of the frame counter as well as control and status bits of the frame counter.

NFCRxH (x = 0-5)

Node x Frame Counter Register High(21A_H+x*100_H)

Reset Value: 0000_H



Field	Bits	Type	Description
CFSEL	[2:0]	rw	CAN Frame Count Selection This bit field selects the function of the frame counter for the chosen frame count mode. Frame Count Mode Bit 0: If Bit 0 of CFSEL is set then CFC is incremented each time a foreign frame (i.e. a frame not matching to a message object) has been received on the CAN bus. Bit 1: If Bit 1 of CFSEL is set then CFC is incremented each time a frame matching to a message object has been received on the CAN bus. Bit 2: If Bit 2 of CFSEL is set then CFC is incremented each time a frame has been transmitted successfully by the node. Time Stamp Mode The frame counter is incremented (internally) with the beginning of a new bit time. Its value is permanently sampled in the CFC field while the bus is idle. The value sampled just before the SOF bit of a new frame is detected is written to the corresponding message object. When the treatment of a message object is finished, the sampling continues. Bit Timing Mode The available bit timing measurement modes are shown in Table 22-11 . If CFCIE is set then an interrupt on request node x (where x is the CAN node index) is generated with a CFC update.

Controller Area Network (MultiCAN) Controller

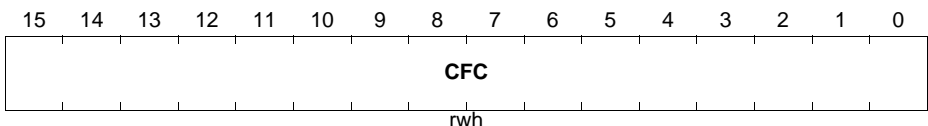
Field	Bits	Type	Description
CFMOD	[4:3]	rw	CAN Frame Counter Mode This bit field defines the operation mode of the frame counter. 00 _B Frame Count Mode: The frame counter is incremented upon the reception and transmission of frames. 01 _B Time Stamp Mode: The frame counter is used to count CAN bit times. 10 _B Bit Timing Mode: The frame counter is used for analysis of the bit timing. ¹⁾ 11 _B reserved
CFCIE	6	rw	CAN Frame Count Interrupt Enable 0 _B CAN Frame Counter Overflow interrupt request is disabled. 1 _B CAN Frame Counter Overflow interrupt request is enabled.
CFCOV	7	rwh	CAN Frame Counter Overflow Flag Flag CFCOV is set upon a frame counter overflow (transition from FFFF _H to 0000 _H). In bit timing analysis mode CFCOV is set upon an update of CFC. An interrupt request is generated if CFCIE = 1. 0 _B No overflow has occurred since last flag reset. 1 _B An overflow has occurred since last flag reset. CFCOV must be cleared by software.
0	5, [15:8]	r	reserved; returns '0' if read; should be written with '0';

- 1) For all bit timing analysis modes, the count value of NFCRx.CFC always displays the measured value minus 1.
 Example: A CFC value of 34 in mode CFSEL = 000 indicates that 35 have been elapsed between the most recent 2 dominant edges on the receive input.

NFCRxL (x = 0-5)

Node x Frame Counter Register Low(218_H+x*100_H)

Reset Value: 0000_H



Field	Bits	Type	Description
CFC	[15:0]	rwh	CAN Frame Counter In Frame Count Mode this bit field contains the frame count value. In TimeStamp Mode this bit field contains the captured bit time count value, captured with the start of a new frame.

Bit Timings Analysis Modes and States

Table 22-11 Bit Timing Analysis Modes (CFMOD = 10)

CFSEL	Measurement
000	Whenever a dominant edge (transition from 1 to 0) is monitored on the receive input the time (measured in clock cycles) between this edge and the most recent dominant edge is stored in CFC.
001	Whenever a recessive edge (transition from 0 to 1) is monitored on the receive input the time (measured in clock cycles) between this edge and the most recent dominant edge is stored in CFC.
010	Whenever a dominant edge is received as a result of a transmitted dominant edge the time (clock cycles) between both edges is stored in CFC.
011	Whenever a recessive edge is received as a result of a transmitted recessive edge the time (clock cycles) between both edges is stored in CFC.
100	Whenever a dominant edge that qualifies for synchronization is monitored on the receive input the time (measured in clock cycles) between this edge and the most recent sample point is stored in CFC.
101	With each sample point, the time (measured in clock cycles) between the start of the new bit time and the start of the previous bit time is stored in CFC[11:0]. Additional information is written to CFC[15:12] at each sample point: CFC[15] : Transmit value of actual bit time CFC[14] : Receive sample value of actual bit time CFC[13:12] : CAN bus information (see Table 22-12)
110	reserved
111	reserved

Table 22-12 CAN Bus State Information

CFC[13:12]	CAN bus state
00	NoBit The CAN bus is idle, performs bit (de-) stuffing or is in one of the following frame segments: SOF, SRR, CRC, delimiters, first 6 EOF bits, IFS
01	NewBit This code represents the first bit of a new frame segment. The current bit is the first bit in one of the following frame segments: bit 10 (MSB) of standard ID (transmit only), RTR, reserved bits, IDE, DLC(MSB), bit 7 (MSB) in each data byte and the first bit of the ID extension
10	Bit This code represents a bit inside a frame segment with a length of more than one bit (not the first bit of those frame segments which is indicated by NewBit). The current bit is processed within one of the following frame segments: ID bits (except first bit of standard ID for transmission and first bit of ID extension), DLC (3 LSB) and bits 6-0 in each data byte
11	Done The current bit is in one of the following frame segments: Acknowledge slot, last bit of EOF, active/passive error frame, overload frame. Two or more directly consecutive Done codes signal an error frame.

22.2.12 Message Object Registers

The Message Object Control Register contains control bits for the CAN transfer and the message object link pointer. Each control bit has a corresponding bit in the CTRL field. A control bit is set by writing 1 to the corresponding bit in CTRL. It is cleared by writing 1 to the control bit directly. Any other combination leaves the control bit unchanged. After reset initialization the pointer PNEXT (read value of MOCTRnH[15:8]) points to message object n+1 (PNEXT = n+1), except for PNEXT of message object 255, which terminates the initial list (PNEXT = 255). Pointer PREV (read value of MOCTRnH[7:0]) initially points to message object n-1 (PPREV = n-1), except for PPREV of message object 0 which indicates the start of the initial list (PPREV = 0). This reset initialization means that all message objects initially belong to the list of unallocated elements.

Controller Area Network (MultiCAN) Controller

MOCTR0H

Message Object 0 Control Register High (101E_H)

Reset Value: 0100_H

MOCTR255H

Message Object 255 Control Register High (2FFE_H)

Reset Value: FFFE_H

MOCTRnH (n = 1-254)

Message Object n Control Register High (101E_H+n*20_H)

Reset Value:

((n+1)*0100_H)+((n-1)*0001_H)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				SET DIR	SET TXE N1	SET TXE N0	SET TXR Q	SET RXE N	SET RTS EL	SET MSG VAL	SET MSG LST	SET NEW DAT	SET RXU PD	SET TXP ND	SET RXP ND
W				W	W	W	W	W	W	W	W	W	W	W	W

Field	Bits	Type	Description
SETRXPND	0	w	Set Receive Pending This bit sets the RXPND
SETTXPND	1	w	Set Transmit Pending This bit sets the TXPND
SETRXUPD	2	w	Set Receive Updating This bit sets the RXUPD
SETNEWDAT	3	w	Set New Data This bit sets the NEWDAT
SETMSGGLST	4	w	Set Message Lost This bit sets the MSGGLST
SETMSGVAL	5	w	Set Message Valid This bit sets the MSGVAL
SETRTSEL	6	w	Set Receive/Transmit Selected This bit sets the RTSEL
SETRXEN	7	w	Set Receive Enable This bit sets the RXEN
SETTXRQ	8	w	Set Transmit Request This bit sets the TXRQ
SETTXEN0	9	w	Set Transmit Enable 0 This bit sets the TXEN0
SETTXEN1	10	w	Set Transmit Enable 1 This bit sets the TXEN1

Controller Area Network (MultiCAN) Controller

Field	Bits	Type	Description
SETDIR	11	w	Set Message Direction This bit sets the DIR
0	[15:12]	w	Reserved Should be written with 0.

MOCTRnL (n = 0-255)

Message Object n Control Register Low(101C_H+n*20_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				RES DIR	RES TXE N1	RES TXE N0	RES TXR Q	RES RXE N	RES RTS EL	RES MSG VAL	RES MSG LST	RES NEW DAT	RES RXU PD	RES TXP ND	RES RXP ND
w				w	w	w	w	w	w	w	w	w	w	w	w

Field	Bits	Type	Description
RESRXPND	0	w	Reset Receive Pending This bit resets the RXPND
RESTXPND	1	w	Reset Transmit Pending This bit resets the TXPND
RESRXUPD	2	w	Reset Receive Updating This bit resets the RXUPD
RESNEWDAT	3	w	Reset New Data This bit resets the NEWDAT
RESMSGSLST	4	w	Reset Message Lost This bit resets the MSGSLST
RESMSGVAL	5	w	Reset Message Valid This bit resets the MSGVAL
RESRTSEL	6	w	Reset Receive/Transmit Selected This bit resets the RTSEL
RESRXEN	7	w	Reset Receive Enable This bit resets the RXEN
RESTXRQ	8	w	Reset Transmit Request This bit resets the TXRQ
RESTXEN0	9	w	Reset Transmit Enable 0 This bit resets the TXEN0

Controller Area Network (MultiCAN) Controller

Field	Bits	Type	Description
RESTXEN1	10	w	Reset Transmit Enable 1 This bit resets the TXEN1
RESDIR	11	w	Reset Message Direction This bit resets the DIR
0	[15:12]	w	Reserved Should be written with 0.

MOSTAT0H

Message Object 0 Status Register High (101E_H)

Reset Value: 0100_H

MOSTAT255H

Message Object 255 Status Register High (2FFE_H)

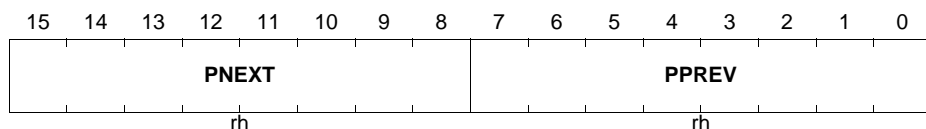
Reset Value: FFFE_H

MOSTATnH (n = 1-254)

Message Object n Status Register High (101E_H+n*20_H)

Reset Value:

((n+1)*0100_H)+((n-1)*0001_H)

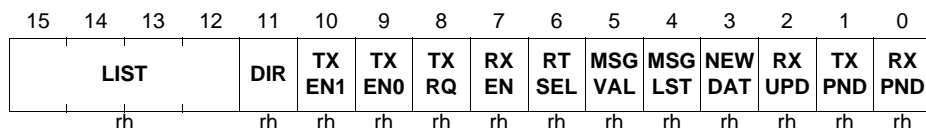


Field	Bits	Type	Description
PNEXT	[15:8]	rh	Pointer to Previous Message Object PPREV holds the message object number of the previous message object in a message list structure.
PPREV	[7:0]	rh	Pointer to Next Message Object PNEXT holds the message object number of the next message object in a message list structure.

MOSTATnL (n = 0-255)

Message Object n Status Register Low(101C_H+n*20_H)

Reset Value: 0000_H



Controller Area Network (MultiCAN) Controller

Field	Bits	Type	Description
RXPND	0	rh	Receive Pending 0_B No CAN message has been received. 1_B A CAN message has been received by the message object n, either directly or via gateway copy action. RXPND is not reset by hardware but must be reset by software.
TXPND	1	rh	Transmit Pending 0_B No CAN message has been transmitted. 1_B A CAN message from message object n has been transmitted successfully over the CAN bus. TXPND is not reset by hardware but must be reset by software.
RXUPD	2	rh	Receive Updating 0_B No receive update ongoing. 1_B Message identifier, DLC, and data of the message object are currently updated.
NEWDAT	3	rh	New Data 0_B No update of the message object n since last flag reset. 1_B Message object n has been updated. NEWDAT is set by hardware after a received CAN frame has been stored in message object n. NEWDAT is cleared by hardware when a CAN transmission of message object n has been started. NEWDAT should be set by software after the new transmit data has been stored in message object n to prevent the automatic reset of TXRQ at the end of an ongoing transmission.
MSGLST	4	rh	Message Lost 0_B No CAN message is lost. 1_B A CAN message is lost because NEWDAT has become set again when it has already been set.

Controller Area Network (MultiCAN) Controller

Field	Bits	Type	Description
MSGVAL	5	rh	Message Valid 0_B Message object n is not valid. 1_B Message object n is valid. Only a valid message object takes part in CAN transfers.
RTSEL	6	rh	Receive/Transmit Selected 0_B Message object n is not selected for receive or transmit operation. 1_B Message object n is selected for receive or transmit operation. Frame Reception: RTSEL is set by hardware when message object n has been identified for storage of a CAN frame that is currently received. Before a received frame becomes finally stored in message object n, a check is performed to determine if RTSEL is set. Thus the CPU can suppress a scheduled frame delivery to this message object n by clearing RTSEL by software. Frame Transmission: RTSEL is set by hardware when message object n has been identified to be transmitted next. A check is performed to determine if RTSEL is still set before message object n is actually set up for transmission and bit NEWDAT is cleared. It is also checked that RTSEL is still set before its message object n is verified due to the successful transmission of a frame. RTSEL needs to be checked only when the context of message object n changes, and a conflict with an ongoing frame transfer shall be avoided. In all other cases, RTSEL can be ignored. RTSEL has no impact on message acceptance filtering. RTSEL is not cleared by hardware.
RXEN	7	rh	Receive Enable 0_B Message object n is not enabled for frame reception. 1_B Message object n is enabled for frame reception. RXEN is evaluated for receive acceptance filtering only.

Controller Area Network (MultiCAN) Controller

Field	Bits	Type	Description
TXRQ	8	rh	Transmit Request 0 _B No transmission of message object n is requested. 1 _B Transmission of message object n on the CAN bus is requested. The transmit request becomes valid only if TXRQ, TXEN0, TXEN1 and MSGVAL are set. TXRQ is set by hardware if a matching Remote Frame has been received correctly. TXRQ is reset by hardware if message object n has been transmitted successfully and NEWDAT is not set again by software.
TXEN0	9	rh	Transmit Enable 0 0 _B Message object n is not enabled for frame transmission. 1 _B Message object n is enabled for frame transmission. Message object n can be transmitted only if both bits, TXEN0 and TXEN1, are set. The user may clear TXEN0 in order to inhibit the transmission of a message that is currently updated, or to disable automatic response of Remote Frames.
TXEN1	10	rh	Transmit Enable 1 0 _B Message object n is not enabled for frame transmission. 1 _B Message object n is enabled for frame transmission. Message object n can be transmitted only if both bits, TXEN0 and TXEN1, are set. TXEN1 is used by the MultiCAN module for selecting the active message object in the Transmit FIFOs.

Controller Area Network (MultiCAN) Controller

Field	Bits	Type	Description
DIR	11	rh	Message Direction 0_B Receive Object selected: With TXRQ = 1, a Remote Frame with the identifier of message object n is scheduled for transmission. On reception of a Data Frame with matching identifier, the message is stored in message object n. 1_B Transmit Object selected: If TXRQ = 1, message object n is scheduled for transmission of a Data Frame. On reception of a Remote Frame with matching identifier, bit TXRQ is set.
LIST	[15:12]	rh	List Allocation LIST indicates the number of the message list to which message object n is allocated. LIST is updated by hardware when the list allocation of the object is modified by a panel command.

Controller Area Network (MultiCAN) Controller

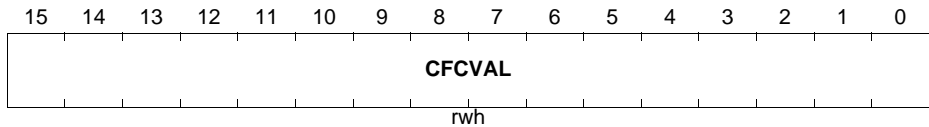
The Message Object Interrupt Pointer Registers MOIPR H/L hold various pointers related to message interrupts as well as the frame counter value.

MOIPRnH (n = 0-255)

Message Object n Interrupt Pointer Register High

(100A_H+n*20_H)

Reset Value: 0000_H



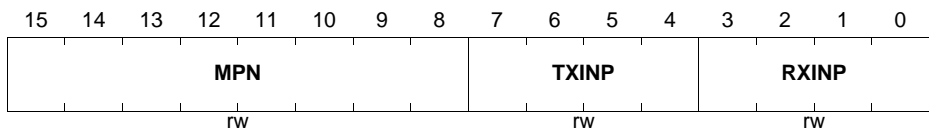
Field	Bits	Type	Description
CFCVAL	[15:0]	rwh	CAN Frame Counter Value When a message is stored in this message object or this message object has been successfully transmitted then the CAN frame counter value CFC of the CAN Node Frame Counter Register (NFCR) is copied to CFCVAL.

MOIPRnL (n = 0-255)

Message Object n Interrupt Pointer Register Low

(1008_H+n*20_H)

Reset Value: 0000_H



Field	Bits	Type	Description
RXINP	[3:0]	rw	Receive Interrupt Node Pointer Select the interrupt output line INT_Om (m=0-15) for receive interrupts.
TXINP	[7:4]	rw	Transmit Interrupt Node Pointer Select the interrupt output line INT_Om (m=0-15) for transmit interrupts.

Controller Area Network (MultiCAN) Controller

Field	Bits	Type	Description
MPN	[15:8]	rw	Message Pending Number This field selects the bit position of the bit in the message pending register to be set upon a receive/transmit interrupt.

Controller Area Network (MultiCAN) Controller

The Message Object Function Control Registers High / Low contain bits to select and to configure the function of the message object. It also holds the CAN data length code.

MOFCRnH (n = 0-255)

Message Object n Function Control Register High

(1002_H + n * 20_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				DLC				STT	SDT	RMM	FRR EN	0	OVIE	TXIE	RXIE
r				rwh				rw	rw	rw	rw	r	rw	rw	rw

Field	Bits	Type	Description
RXIE	0	rw	Receive Interrupt Enable If RXIE is set then a message interrupt request is generated with the reception of a CAN message, no matter whether the CAN message is received directly or indirectly via a gateway action. The interrupt is requested on interrupt output line as defined by RXINP.
TXIE	1	rw	Transmit Interrupt Enable If TXIE is set then a message interrupt request is generated when this message object successfully transmitted a message over the CAN bus. The interrupt is requested on interrupt output line as defined by TXINP.
OVIE	2	rw	Overflow Interrupt Enable IF OVIE = 1 then a FIFO full interrupt is generated when the pointer to the current object CUR reaches the value of SEL in the FIFO/Gateway Pointer Register. If this object is a receive FIFO base object then the FIFO full interrupt is requested on interrupt output line as defined by TXINP. If this object is a transmit FIFO base object then the FIFO full interrupt is requested on interrupt output line as defined by RXINP. For all other message object modes OVIE has no effect.

Controller Area Network (MultiCAN) Controller

Field	Bits	Type	Description
FRREN	4	rw	Foreign Remote Request Enable Specifies if the TXRQ bit is set in this message object or in a foreign object referenced by the pointer CUR. 0 _B TXRQ of this message object is set upon the reception of a matching remote frame. 1 _B TXRQ of the message object referenced by the pointer CUR is set upon the reception of a matching remote frame.
RMM	5	rw	Transmit Object Remote Monitoring 0 _B Remote monitoring disabled: The identifier, IDE bit and DLC of the message object remain unchanged upon the reception of a matching remote frame. 1 _B Remote monitoring enabled: The identifier, DLC and IDE bit of a matching remote frame are copied to this transmit object in order to monitor incoming remote frames. Bit RMM only applies to transmit objects and has no impact on receive objects.
SDT	6	rw	Single Data Transfer If SDT = 1 and this object is not a FIFO base object then MSGVAL is reset when this object has taken part in a successful data transfer (receive or transmit). If SDT = 1 and this object is a FIFO base object then MSGVAL is reset when the pointer to the current object CUR reaches the value of SEL in the FIFO/Gateway Pointer Register. With SDT = 0, bit MSGVAL is not affected.
STT	7	rw	Single Transmit Trial If this bit is set then TXRQ is cleared upon transmission start of this message object. Thus no transmission retry is performed in case of transmission failure.
DLC	[11:8]	rwh	Data Length Code Valid values for the data length are 0 to 8. DLC>8 leads to 8 data bytes, but the DLC code is not truncated upon reception or transmission of CAN frames.

Controller Area Network (MultiCAN) Controller

Field	Bits	Type	Description
0	3, [15:12]	r	Reserved; read as 0; should be written with 0.

MOFCRnL (n = 0-255)

Message Object n Function Control Register Low

(1000_H+n*20_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				DAT C	DLC C	IDC	GDFS	0				MMC			
r				rw	rw	rw	rw	r				rw			

Field	Bits	Type	Description
MMC	[3:0]	rw	Message Mode Control Bit field MMC controls the functionality of the message object. 0000 _B Standard Message Object 0001 _B Receive FIFO Base Object 0010 _B Transmit FIFO Base Object 0011 _B Transmit FIFO Slave Object 0100 _B Gateway Source Object XXXX _B Reserved
GDFS	8	rw	Gateway Data Frame Send 1 _B TXRQ is set in the gateway destination object after the transfer of a data frame from the gateway source to the gateway destination. 0 _B TXRQ is not set in the destination object. Applicable only to Gateway Source Object.
IDC	9	rw	Identifier Copy IF IDC = 1 then the identifier of the gateway source object (after storing the received frame in the source) is copied to the gateway destination. Applicable only to Gateway Source Object.
DLCC	10	rw	Data Length Code Copy If DLCC = 1 then the data length code of the gateway source object (after storing the received frame in the source) is copied to the gateway destination. Applicable only to Gateway Source Object.

Controller Area Network (MultiCAN) Controller

Field	Bits	Type	Description
DATC	11	rw	Data Copy If DATC = 1 then the data field (registers MODATA0 and MODATA4) of the gateway source object (after storing the received frame in the source) is copied to the gateway destination. Applicable only to Gateway Source Object.
0	[7:4], [15:12]	r	reserved; returns '0' if read; should be written with '0';

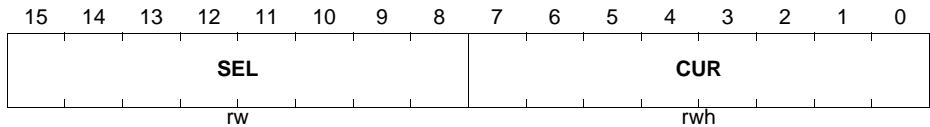
Controller Area Network (MultiCAN) Controller

The Message Object FIFO/Gateway Pointer Registers H/L contain a set of message object link pointer used for FIFO and gateway functionality

MOFGPRnH (n = 0-255)

Message Object n FIFO/Gateway Pointer Register High
(1006_H+n*20_H)

Reset Value: 0000_H

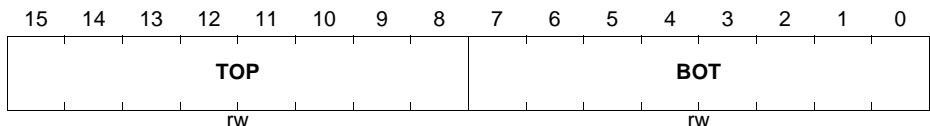


Field	Bits	Type	Description
CUR	[7:0]	rwh	Current Object Pointer The Current Object Pointer links to the actual target object within a FIFO/Gateway structure. After a FIFO/gateway operation CUR is updated with the message number of the next message object in the list structure (given by PNEXT of the message control register) until it reaches the FIFO top element (given by TOP) when it is reset to the bottom element (given by BOT).
SEL	[15:8]	rw	Object Select Pointer The Object Select Pointer is the second (software) pointer to complement the hardware pointer CUR in the FIFO structure. SEL is used for monitoring purposes only.

MOFGPRnL (n = 0-255)

Message Object n FIFO/Gateway Pointer Register Low
(1004_H+n*20_H)

Reset Value: 0000_H



Controller Area Network (MultiCAN) Controller

Field	Bits	Type	Description
BOT	[7:0]	rw	Bottom Pointer The Bottom Pointer points to the first element in a FIFO structure.
TOP	[15:8]	rw	Top Pointer The TOP pointer points to the last element in a FIFO structure.

Note: The pointers in this register must be set to objects assigned to the same CAN node. It is forbidden to refer to objects that are not in the linked list for the same CAN node.

Controller Area Network (MultiCAN) Controller

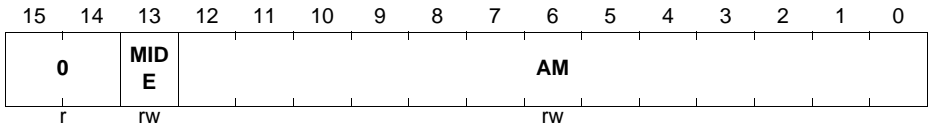
Registers MOAMR H/L contain the mask bits for the acceptance filtering of the message object.

MOAMRnH (n = 0-255)

Message Object n Acceptance Mask Register High

(100E_H+n*20_H)

Reset Value: 3FFF_H



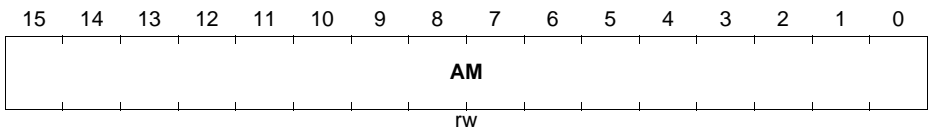
Field	Bits	Type	Description
AM[28:16]	[12:0]	rw	Acceptance Mask for Message Identifier High see description of MOAMRnL.AM[15:0]
MIDE	13	rw	Acceptance Mask bit for Message IDE bit 0 _B This message objects accepts the reception of both standard and extended frames. 1 _B This message object only receives frames with matching IDE bit.
0	[15:14]	r	Reserved; read as 0; should be written with 0.

MOAMRnL (n = 0-255)

Message Object n Acceptance Mask Register Low

(100C_H+n*20_H)

Reset Value: FFFF_H



Field	Bits	Type	Description
AM[15:0]	[15:0]	rw	Acceptance Mask for Message Identifier Mask to filter incoming messages with standard identifiers (AM[28:18]) or extended identifiers (AM[28:0]). For standard identifiers bits AM[17:0] are "don't care".

Controller Area Network (MultiCAN) Controller

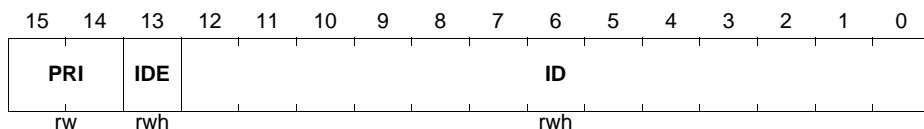
Registers MOAR H/L contain the CAN identifier of the message object.

MOARnH (n = 0-255)

Message Object n Arbitration Register High

(101A_H+n*20_H)

Reset Value: 0000_H



Field	Bits	Type	Description
ID[28:16]	[12:0]	rwh	CAN Identifier of Message Object Identifier of a standard message (ID[28:18]) or an extended message (ID[28:0]). For standard identifiers bits ID[17:0] are "don't care".
IDE	13	rwh	CAN IDE bit of Message Object 0 _B Standard frame with 11-bit identifier 1 _B Extended frame with 29-bit identifier

Controller Area Network (MultiCAN) Controller

Field	Bits	Type	Description
PRI	[15:14]	rw	Priority Class PRI assigns one of the four priority classes 0, 1, 2, 3 to the message object, with lower PRI number meaning higher priority. Message objects with lower PRI value always win acceptance filtering for frame reception and transmission over message objects with higher PRI value. Acceptance filtering based on identifier/mask and list position is only performed between message objects of the same priority class. PRI also defines the acceptance filtering method for transmission: 00 _B Time Triggered CAN (TTCAN only) ¹⁾ 01 _B Transmit acceptance filtering is based on the list order, i.e. this message object is considered for transmission only if there is no other message object with valid transmit request (MSGVAL & TXRQ & TXEN0 & TXEN1 = 1) somewhere before this object in the list. 10 _B Transmit acceptance filtering is based on the CAN identifier, i.e. this message object is considered for transmission only if there is no other message object with higher priority identifier+IDE+DIR (with respect to CAN arbitration rules) somewhere in the list (see Table 22-13). 11 _B Transmit acceptance filtering is based on the list order (like PRI = 01).

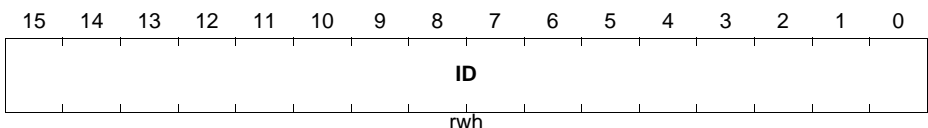
1) If a TTCAN extension is not available or switched off for a CAN node, the message objects with PRI=00 are not taken into account for transmission.

MOARnL (n = 0-255)

Message Object n Arbitration Register Low

(1018_H+n*20_H)

Reset Value: 0000_H



Controller Area Network (MultiCAN) Controller

Field	Bits	Type	Description
ID[15:0]	[15:0]	rwh	CAN Identifier of Message Object Low Identifier of a standard message (ID[28:18]) or an extended message (ID[28:0]). For standard identifiers bits ID[17:0] are "don't care".

Transmit Priority

Table 22-13 Transmit Priority based on CAN Arbitration Rules

Settings of arbitrarily chosen message objects A and B, where A has higher transmit priority than B	Comment
A.MOAR[28:18] < B.MOAR[28:18] (11 bit standard identifier of A less than 11 bit standard identifier of B)	Messages with lower standard identifier have higher priority than messages with higher standard identifier. MOAR[28] is the most significant bit (MSB) of the standard identifier. MOAR[18] is the least significant bit of the standard identifier.
A.MOAR[28:18] = B.MOAR[28:18] A.MOAR.IDE = 0 (send standard frame) B.MOAR.IDE = 1 (send extended frame)	Standard frames have higher transmit priority than extended frames with equal standard identifier.
A.MOAR[28:18] = B.MOAR[28:18] A.MOAR.IDE = B.MOAR.IDE = 0 A.MOCTR.DIR = 1 (send data frame) B.MOCTR.DIR = 0 (send remote frame)	Standard data frames have higher transmit priority than standard remote frames with equal identifier.
A.MOAR[28:0] = B.MOAR[28:0] A.MOAR.IDE = B.MOAR.IDE = 1 A.MOCTR.DIR = 1 (send data frame) B.MOCTR.DIR = 0 (send remote frame)	Extended data frames have higher transmit priority than extended remote frames with equal identifier.
A.MOAR[28:0] < B.MOAR[28:0] A.MOAR.IDE = B.MOAR.IDE = 1 (29 bit identifier)	Extended frames with lower identifier have higher transmit priority than extended frames with higher identifier. MOAR[28] is the most significant bit (MSB) of the overall identifier (standard identifier MOAR[28:18] and identifier extension MOAR[17:0]). MOAR[0] is the least significant bit (LSB) of the overall identifier.

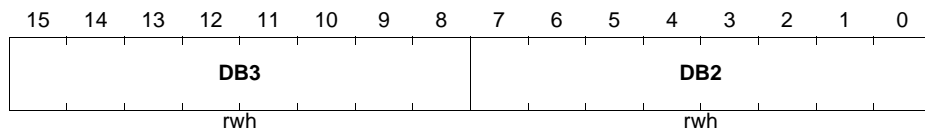
Controller Area Network (MultiCAN) Controller

MODATAnLH (n = 0-255)

Message Object n Data Register Low High

(1012_H+n*20_H)

Reset Value: 0000_H



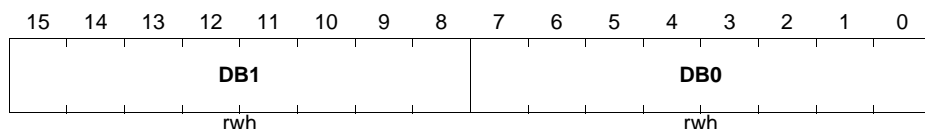
Field	Bits	Type	Description
DB2	[7:0]	rwh	CAN Data Byte 2
DB3	[15:8]	rwh	CAN Data Byte 3

MODATAnLL (n = 0-255)

Message Object n Data Register Low Low

(1010_H+n*20_H)

Reset Value: 0000_H



Field	Bits	Type	Description
DB0	[7:0]	rwh	CAN Data Byte 0
DB1	[15:8]	rwh	CAN Data Byte 1

Controller Area Network (MultiCAN) Controller

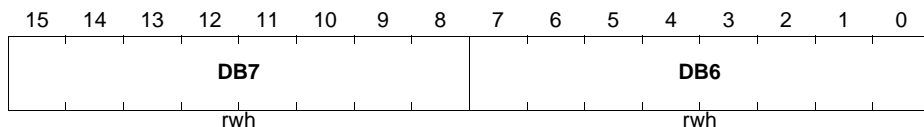
Registers MODATAH H/L contain the highest four CAN data bytes. Unused data bytes are padded zero upon reception and ignored for transmission .

MODATANHH (n = 0-255)

Message Object n Data Register High High

(1016_H+n*20_H)

Reset Value: 0000_H



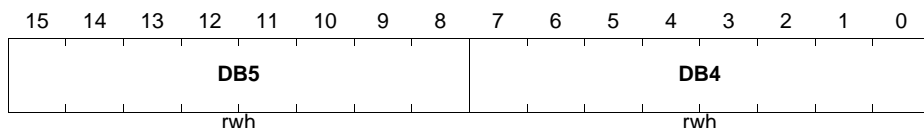
Field	Bits	Type	Description
DB6	[7:0]	rwh	CAN Data Byte 6
DB7	[15:8]	rwh	CAN Data Byte 7

MODATANHL (n = 0-255)

Message Object n Data Register High Low

(1014_H+n*20_H)

Reset Value: 0000_H



Field	Bits	Type	Description
DB4	[7:0]	rwh	CAN Data Byte 4
DB5	[15:8]	rwh	CAN Data Byte 5

22.3 General Control and Status

The following section describes the general clock, debug and interrupt topics.

22.3.1 Clock Control

The CAN clock frequency f_{CAN} of the functional blocks of the MultiCAN module is derived from the system clock f_{SYS} (= clock on the system bus). The fractional divider FDIV in the module is used to generate the CAN clock frequency for the bit timing calculation. This frequency is identical for all CAN nodes. The scheduler itself is in the f_{SYS} domain. The clock generation can be enabled/disabled by the fractional divider control bit field FDR.DM.

The fractional divider FDIV output f_{CAN} is based on the system clock f_{SYS} , but only every n-th clock pulse is taken. The register file is in the system frequency domain. The suspend signal (coming as acknowledge from the module as answer to the OCDS suspend request) freezes or resets the fractional divider.

Note: The receive input line contains a synchronization stage to ensure stable input data. Together with the internal CAN state machine, this leads to a minimum reaction time of at least 3 clock cycles of f_{SYS} between CAN input and output. The switching delay of the input stages can be generally neglected, whereas the rise/fall times of the port output drivers (programmable values) should be taken into account, especially for higher baud rates.

The table below indicates the minimum operating frequencies in MHz for f_{SYS} , that are required for a baud rate of 1 MBaud for the active CAN nodes (the highest CAN baud rate of the activated CAN nodes has to be taken into account). If less baud rate is desired, the values can be scaled linearly (e.g. for a maximum of 500 kBaud, 50% of the indicated value are required).

The values imply that the CPU (or PCP, or DMA) executes a maximum of accesses to the MultiCAN module. The values may contain rounding effects.

Table 22-14 Minimum Operating Frequencies [MHz]

Number of allocated message objects MO^{1) 2)}	1 CAN node active	2 CAN nodes active	3 CAN nodes active	4 CAN nodes active	5 CAN nodes active	6 CAN nodes active
16 MO	12	19	26	33	40	47
32 MO	15	23	30	37	44	52
64 MO	21	28	37	46	53	61
128 MO	40	45	50	55	61	70
144 MO	42	47	52	57	62	70
160 MO	46	51	56	61	66	72

Controller Area Network (MultiCAN) Controller

Table 22-14 Minimum Operating Frequencies [MHz] (cont'd)

Number of allocated message objects MO^{1) 2)}	1 CAN node active	2 CAN nodes active	3 CAN nodes active	4 CAN nodes active	5 CAN nodes active	6 CAN nodes active
176 MO	50	55	60	66	71	76
192 MO	54	59	65	70	75	80
208 MO	58	64	69	74	79	84
224 MO	63	68	73	78	83	89
240 MO	67	72	77	82	88	93
256 MO	71	76	81	87	92	97

- 1) Only those message objects have to be taken into account that are allocated to a CAN node. The unallocated message objects have no influence on the minimum operating frequency.
- 2) In case of using CAN bootstrap loader, with one active node and two active message objects, the MultiCAN module needs minimum frequency of 10 MHz.

The baud rate generation of the MultiCAN being based on f_{SYS} , this frequency has to be chosen carefully to allow correct CAN bit timing. The required value of f_{SYS} is given by an integer multiple (n) of the CAN baud rate multiplied by the number of time quanta per CAN bit time. For example, to reach 1 Mbit/s with 20 tq per bit time, possible values of f_{SYS} are given by formula $[n \times 20]$ MHz, with n being an integer value, starting at 1. In order to minimize jitter, it is not recommended to use the fractional divider mode for high baud rates.

22.3.2 Port Input Control

There is the possibility to select the input lines for the RXDCANx inputs for the CAN nodes. The selected input is connected to the CAN node and is also available to wake up the system.

22.3.3 Suspend Mode

The suspend mode can be triggered by the OCDS in order to freeze the state of the module and to have access to the registers (at least for read actions). There are several aspects related to the suspend mode:

- All actions are immediately stopped ("hard suspend"):
The module clock is switched off as soon as the suspend line becomes active. This mode is supported by the fast switch off feature of the BPI. Write actions to the module are not supported and only combinatorial read actions deliver the desired data (the CAN RAM and the CAN registers can not be accessed).
In this mode, all further module actions are disabled and there is a very high probability that the communication with other devices is made impossible and that the CAN bus is blocked by the device in hard suspend mode (e.g. if the suspended CAN just sends a dominant level). A normal continuation when the suspend mode is left is not always possible and reset must be activated.
- The current action is finished ("soft suspend"):
The module functions are stopped (clock is still running!) automatically after internal actions have been finished, for example after a CAN frame has been sent out. Due to this behavior, the communication network is not blocked due to the suspend mode of one communication partner. Furthermore, all registers are accessible for read and write actions. As a result, the debugger can stop the module actions and modify registers. These modifications are taken into account after the suspend mode is left. This mode is designed to be able to modify registers or to read them by the OCDS while the rest of the systems is still running and not corrupted by the suspend mode.

In the MultiCAN module a suspend mechanism is implemented allowing the individual freeze of CAN nodes. The fast switch off feature (hard suspend) of the BPI must not be activated by the user in order to support the soft suspend mode. In order to allow the required flexibility for the system, each CAN node can be individually enabled for the soft suspend mode.

The hard suspend feature can be enabled/disabled for the complete MultiCAN module, whereas the soft suspend feature can be enabled/disabled independently for each CAN node. The fractional divider disables the CAN clock only if all CAN nodes signal that they can be suspended. A CAN node that is not active can always be suspended.

22.3.4 Interrupt Structure

The general interrupt structure is shown in the figure below. The interrupt event can trigger the interrupt generation. The interrupt pulse is generated independently from the interrupt flag in the interrupt status register. The interrupt flag can be reset by SW by writing a 0 to it.

If enabled by the related interrupt enable bit in the interrupt enable register, an interrupt pulse can be generated at one of the 16 interrupt output lines INT_Ox of the module. If more than one interrupt source is connected to the same interrupt node pointer (in the interrupt node pointer register), the requests are combined to one common line.

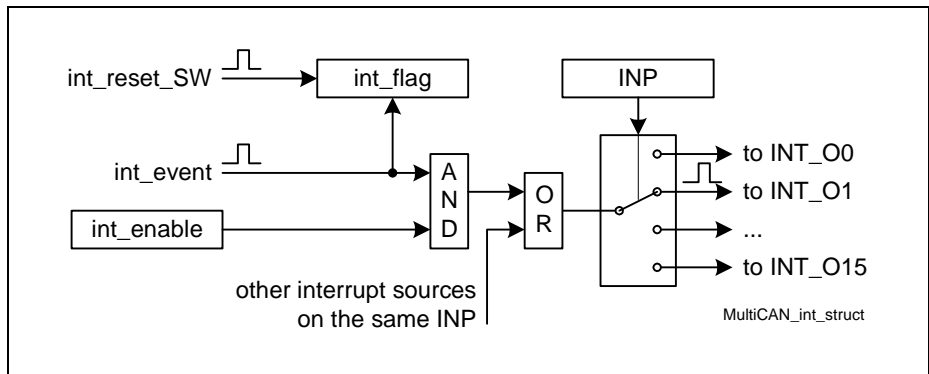


Figure 22-17 General Interrupt Structure

22.4 MultiCAN Module Implementation

This section describes CAN module interfaces with the clock control, port connections, interrupt control, and address decoding.

22.4.1 Interfaces of the CAN Module

Figure 22-18 shows the XC27x8X specific implementation details and interconnections of the CAN module. The I/O lines of the CAN module kernel (two I/O lines of each CAN node) are connected to the ports as described in **Table 22-18**. The CAN module is further supplied by clock control, interrupt control, and address decoding logic.

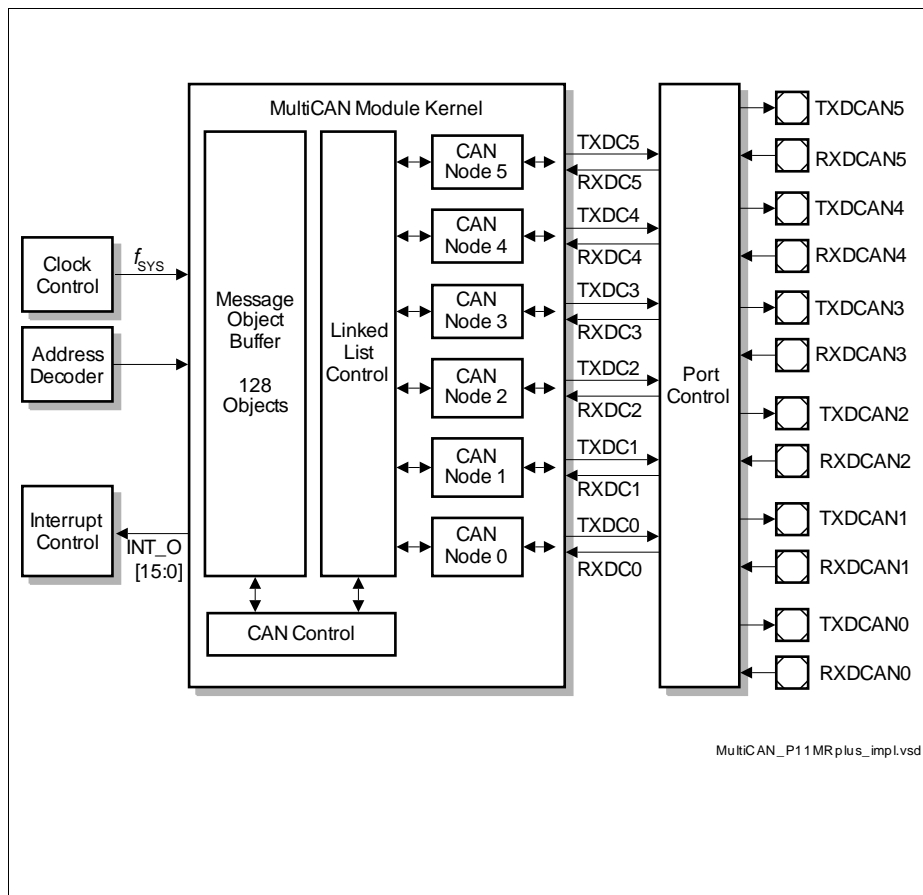


Figure 22-18 CAN Module Implementation and Interconnections

Controller Area Network (MultiCAN) Controller

The MultiCAN interrupt control register x is connected to the CAN interrupt output line INT_Ox, with x = 15 - 0.

22.4.2 Module Clock Generation

As shown in [Figure 22-19](#), the clock signals for the MultiCAN module are generated and controlled by a clock generation unit. This clock generation unit is responsible for the enable/disable control, the clock frequency adjustment, and the debug clock control.

The frequency control of the module timer clock f_{CAN} is performed via the CAN_FDR register.

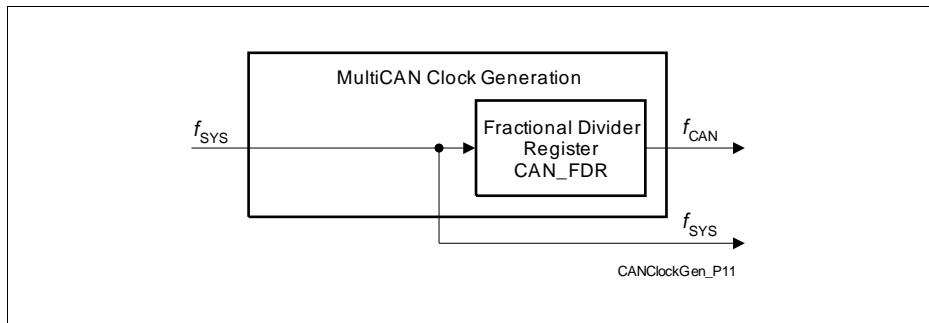


Figure 22-19 MultiCAN Module Clock Generation

The module control clock f_{SYS} is used inside the MultiCAN module kernel for control purposes such as e.g. for clocking of control logic and register operations. The frequency of f_{SYS} is identical to the system clock frequency f_{SYS} .

The module timer clock f_{CAN} is used inside the MultiCAN module kernels as input clock for all timing relevant operations.

The frequency of f_{CAN} is defined by:

$$f_{CAN} = f_{SYS} \times \frac{1}{n} \quad \text{with } n = 1024 - \text{CAN_FDR.STEP}$$

$$\text{or } f_{CAN} = f_{SYS} \times \frac{n}{1024} \quad \text{with } n = 0-1023$$

Note: The upper formula applies to normal divider mode of the fractional divider (CAN_FDR.DM = 01_B). The lower formula applies to fractional divider mode (CAN_FDR.DM = 10_B).

Note: Input signal ECEN of the MultiCAN fractional divider is wired to 0.

22.4.2.1 Fractional Divider Overview

The fractional divider allows to generate output clocks from an input clock using a programmable divider. The fractional divider divides an input clock f_{IN} either by the factor $1/n$ or by a fraction of $n/1024$ for any value of n from 0 to 1023 and outputs the clock signals, f_{OUT} . The clock generation can be enabled/disabled by the fractional divider register control bit field FDR.DM.

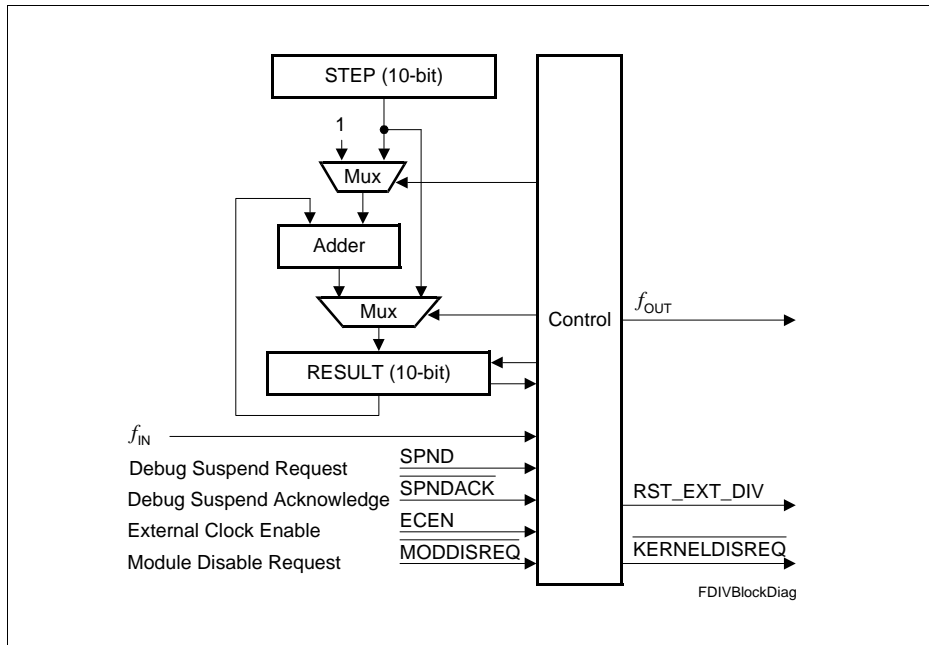


Figure 22-20 Fractional Divider Block Diagram

The clock generation in the fractional divider is further controlled by four input signals.

Table 22-15 Fractional Divider I/O Lines

Signal	I/O	Description
SPND	Input	Suspend Request Input is controlled by the debug system suspend request signal. It becomes active when a general suspend request is issued from the debug system to the on-chip modules.
SPNDACK		Suspend Acknowledge Input is driven with the disable acknowledge signal from the module kernel. This signal is activated by the module kernel as a response to a suspend request that has been issued by the fractional divider via $\overline{\text{KERNELDISREQ}} = 0$.
MODDISREQ		Module Disable Request Input is connected to the disable request output from the clock logic. An active signal at this input results in the activation of output signal $\overline{\text{KERNELDISREQ}}$.
ECEN		External Clock Enable Signal ECEN can be used to synchronize the fractional divider clock generation to external events.
$\overline{\text{KERNELDISREQ}}$	Output	Kernel Disable Request This output signal becomes active when either $\overline{\text{MODDISREQ}}$ is activated or when SPND becomes active.
RST_EXT_DIV		Reset External Divider This output signal allows to control (stop/reset) external divider stages for f_{OUT} .
f_{OUT}		Module Clock Enable Signal f_{OUT} is the enable signal for the module clock. The module clock itself is built by and-ing the f_{OUT} enable signal with f_{IN} . Module clock frequency references mostly refer to the AND combination of f_{OUT} with f_{IN} .

The fractional divider has two operating modes:

- Normal divider mode
- Fractional divider mode

Normal Divider Mode

In normal divider mode ($FDR.DM = 01_B$) the fractional divider behaves like a reload counter (addition of +1) that generates an output clock pulse at f_{OUT} on the transition from $3FF_H$ to 000_H . $FDR.RESULT$ represents the counter value and $FDR.STEP$ defines the reload value.

The output frequencies in normal divider mode are defined according the following formulas:

$$f_{OUT} = f_{IN} \times \frac{1}{n} \quad \text{with } n = 1024 - STEP$$

In order to get $f_{OUT} = f_{IN}$ STEP must be programmed with $3FF_H$. **Figure 22-21** shows the operation of the normal divider mode with a reload value of $FDR.STEP = 3FD_H$. The clock frequency of f_{OUT} is represented by and-ing the f_{OUT} enable signal with f_{IN} .

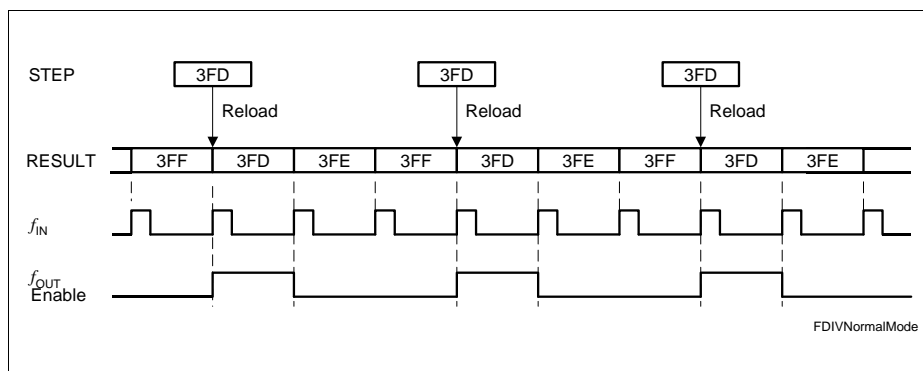


Figure 22-21 Normal Mode Timing

Fractional Divider Mode

When the fractional divider mode is selected ($FDR.DM = 10_B$), the output clock f_{OUT} is derived from the input clock f_{IN} by division of a fraction of $n/1024$ for any value of n from 0 to 1023. In general, the fractional divider mode allows to program the average output clock frequency with a higher accuracy than in normal divider mode.

In fractional divider mode an output clock pulse at f_{OUT} is generated dependent on the result of the addition $FDR.RESULT + FDR.STEP$. If the addition leads to an overflow over $3FF_H$ a pulse is generated at f_{OUT} . Note that in fractional divider mode the clock f_{OUT} can have a maximum period jitter of one f_{IN} clock period.

The output frequencies in fractional divider mode are defined according the following formulas:

$$f_{OUT} = f_{IN} \times \frac{n}{1024} \quad \text{with } n = 0-1023$$

Figure 22-22 shows the operation of the fractional divider mode with a reload value of $FDR.STEP = 234_H$ (= factor $564/1024 = 0.55$). The clock frequency of f_{OUT} is represented by and-ing the f_{OUT} enable signal with f_{IN} .

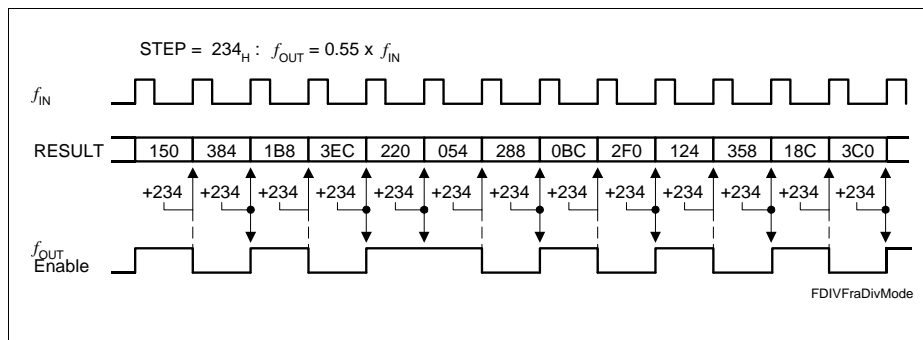


Figure 22-22 Fractional Divider Mode Timing

Suspend Mode Control

The fractional divider allows to control its operation according to the input Suspend Request (SPND). This input is activated in suspend mode by the on-chip debug control logic. In suspend mode, the module registers are accessible for read and write actions, but the other module internal functions are frozen. Suspend mode is requested by $SPND = 1$. Suspend mode is entered one f_{IN} clock cycle after the suspend mode request has been acknowledged by setting $SPNDACK$ to 0 (granted suspend mode) and

Controller Area Network (MultiCAN) Controller

FDR.SC is not equal 00_B (clock output signal disabled). Suspend mode is immediately entered when bit SM is set to 1 and FDR.SC is not equal 00_B (immediate suspend mode). The state of signals SPND and SPNDACK is latched in two status flags of register FDR, SUSREQ and SUSACK. SPND and (SPNDACK or bit SM) must remain set both to maintain the suspend mode.

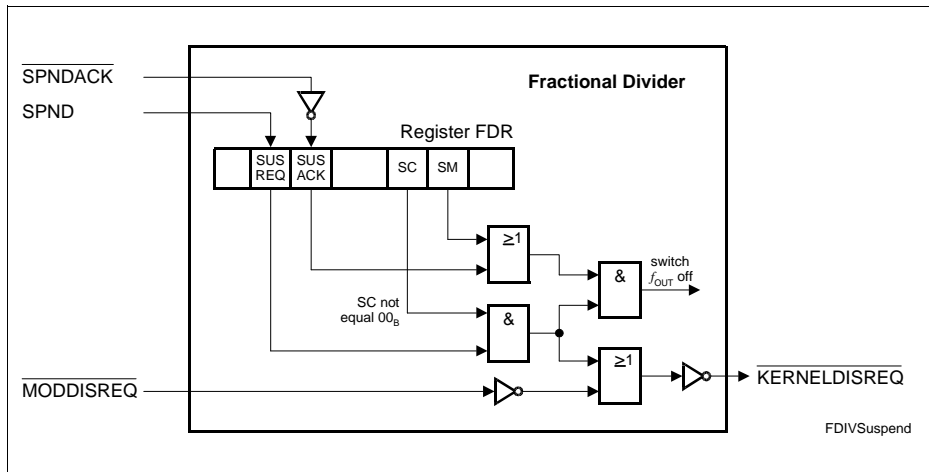


Figure 22-23 Suspend Mode Configuration

The Kernel Disable Request signal KERNELDISREQ becomes always active when MODDISREQ is activated, independently of the suspend mode settings in the fractional divider logic.

External Clock Enable

When the module clock generation has been disabled by software (setting FDR.DISCLK = 1), the disable state can be left via input ECEN = 1 (hardware controlled). This feature is enabled when FDR.ENHW = 1. In the MultiCAN module, signal ECEN is tied to 0.

Registers Overview

Fractional Divider Registers

The fractional divider contains two registers, FDRL (lower 16 bits) and FDRH (higher 16 bits).

Controller Area Network (MultiCAN) Controller

FDRL

Fractional Divider Register L

(0C_H)

Reset Value: 0000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DM		SC		SM	0	STEP									
rw		rw		rw	r	rw									

Field	Bits	Type	Description
STEP	[9:0]	rw	Step Value In normal divider mode STEP contains the reload value for RESULT. In fractional divider mode this bit field defines the 10-bit value that is added to the RESULT with each input clock cycle.
SM	11	rw	Suspend Mode SM selects between granted or immediate suspend mode. 0 _B Granted suspend mode selected 1 _B Immediate suspend mode selected
SC	[13:12]	rw	Suspend Control This bit field defines the behavior of the fractional divider in suspend mode (bit SUSREQ and SUSACK set). 00 _B Clock generation continues. 01 _B Clock generation is stopped and the clock output signals are not generated. RESULT is not changed except when writing bit field DM with 01B or 10B. 10 _B Clock generation is stopped and the clock output signals are not generated. RESULT is loaded with 3FF _H . 11 _B Same as SC = 10B but RST_EXT_DIV is 1 (independently of bit field DM).

Controller Area Network (MultiCAN) Controller

Field	Bits	Type	Description
DM	[15:14]	rw	Divider Mode This bit fields defines the functionality of the fractional divider block. 00 _B Fractional divider is switched off; no output clock is generated. RST_EXT_DIV is 1. RESULT is not updated (default after reset). 01 _B Normal divider mode selected. 10 _B Fractional divider mode selected. 11 _B Fractional divider is switched off; no output clock is generated. RESULT is not updated.
0	10	r	Reserved read as 0; should be written with 0.

FDRH

Fractional Divider Register H

(0E_H)

Reset Value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIS CLK	EN HW	SUS REQ	SUS ACK	0	RESULT										
rwh	rw	rh	rh	r	rh										

Field	Bits	Type	Description
RESULT	[9:0]	rh	Result Value In normal divider mode RESULT acts as reload counter (addition +1). In fractional divider mode this bit field contains the result of the addition RESULT+STEP. If DM is written with 01 _B or 10 _B , RESULT is loaded with 3FF _H .
SUSACK	12	rh	Suspend Mode Acknowledge 0 _B Suspend mode is not acknowledged. 1 _B Suspend mode is acknowledged. Suspend mode is entered when SUSACK and SUSREQ are set.

Controller Area Network (MultiCAN) Controller

Field	Bits	Type	Description
SUSREQ	13	rh	Suspend Mode Request 0_B Suspend mode is not requested. 1_B Suspend mode is requested. Suspend mode is entered when SUSREQ and SUSACK are set.
ENHW	14	rw	Enable Hardware Clock Control 0_B Bit DISCLK cannot be reset by HW by a high level at input signal ECEN. 1_B Bit DISCLK is reset by hardware while input signal ECEN is at high level.
DISCLK	15	rwh	Disable Clock 0_B Clock generation of f_{OUT} is enabled according to the setting of bit field DM. 1_B Fractional divider is stopped. The enable signal f_{OUT} becomes inactive. No change except when writing bit field DM.
0	[11:10]	r	Reserved read as 0; should be written with 0.

Fractional Divider Operation Modes

Table 22-16 Fractional Divider Function Table

Mode	SC	DM	RES_EXT_DIV	RESULT	f_{OUT}	Operation of Fractional Divider
Normal Mode	–	00	1	unchanged	inactive	switched off
		01	0	continuously updated ¹⁾	active	normal divider mode
		10				fractional divider mode
		11		unchanged	inactive	switched off

Controller Area Network (MultiCAN) Controller

Table 22-16 Fractional Divider Function Table

Mode	SC	DM	RES_EXT_DIV	RESULT	f_{OUT}	Operation of Fractional Divider
Suspend Mode	00	00	1	unchanged	inactive	switched off
		01	0	continuously updated ¹⁾	active	normal divider mode
		10				fractional divider mode
		11				unchanged
	01	00	1	unchanged	inactive	switched off
		01	0	unchanged ¹⁾		halted
		10				switched off
		11				
	10	00	1	loaded with 3FF _H	inactive	switched off
		01	0			halted
		10				switched off
		11				
	11	—	1	loaded with 3FF _H	inactive	switched off

1) Each write operation to FDR with DM = 01_B or 10_B sets RESULT to 3FF_H.

22.4.3 Mode Control

The mode control concept for system control tasks, such as power saving, or suspend request for debugging, allows to program the module behavior under different device operating conditions. The behavior of the MultiCAN kernel can be programmed for each of the device operating modes, that are requested by the global state control part of the SCU. MultiCAN has an associated register MCAN_KSCCFG defining the behavior of the kernel of the module in the following device operating modes:

- **Normal operation:**

This operating mode is the default operating mode when neither a suspend request nor a clock-off request are pending. The module clock is not switched off and the MultiCAN registers can be read or written. The kernel behavior is defined by KSCCFG.NOMCFG.

- **Suspend mode:**

This operating mode is requested when a suspend request (issued by a debugger) is pending in the device. The module clock is not switched off and the MultiCAN

Controller Area Network (MultiCAN) Controller

registers can be read or written. The kernel behavior is defined by KSCCFG.SUMCFG.

- **Clock-off mode:**

This operating mode is requested for power saving purposes. The module clock is switched off automatically when all kernels of the MultiCAN module reached their specified state in a stop mode. In this case, MultiCAN registers can not be accessed. The kernel behavior is defined by KSCCFG.COMCFG.

For the MultiCAN module, the following internal actions can be influenced by mode control:

- A current transmission of a CAN message:

If there is a pending request, it can be started. This start has to be enabled by the mode control. If the current kernel mode allows the start (run modes 0 and 1), it will be executed. If the kernel mode does not allow a start (stop modes 0 and 1), the request is not started. The start request is not cancelled, but frozen. A “frozen” request is started as programmed if the kernel mode is changed to a run mode again.

The behavior of the MultiCAN kernel can be programmed for each of the device operating modes (normal operation, suspend mode, clock-off mode). Therefore, the MultiCAN kernel supports four kernel modes, as shown in [Table 22-17](#).

Controller Area Network (MultiCAN) Controller

Table 22-17 MultiCAN Kernel Behavior

Kernel Mode	Kernel Behavior	Code
run mode 0	kernel operation as specified, no impact on data transfer (same behavior for run mode 0 and run mode 1)	00 _B
run mode 1		01 _B
stop mode 0	A currently running transfer is completely finished and the result is treated. Pending requests are not taken into account (but not deleted). They restart after entering a run mode as programmed. The arbiter continues as programmed.	10 _B
stop mode 1	Like stop mode 0, but the arbiter is stopped after it has finished its arbitration round.	11 _B

Generally, bit field KSCCFG.NOMCFG should be configured for run mode 0 as default setting for standard operation. If the MultiCAN kernel should not react to a suspend request (and to continue operation as in normal mode), bit field KSCCFG.SUMCFG has to be configured with the same value as KSCCFG.NOMCFG. If the MultiCAN kernel should show a different behavior and stop operation when a specific stop condition is reached, the code for stop mode 0 or stop mode 1 has to be written to KSCCFG.SUMCFG.

A similar mechanism applies for the clock-off mode with the possibility to program the desired behavior by bit field KSCCFG.COMCFG.

Note: The stop mode selection strongly depends on the application needs and it is very unlikely that different stop modes are required in parallel in the same application. As a result, only one stop mode type (either 0 or 1) should be used in the bit fields in register KSCCFG. Do not mix stop mode 0 and stop mode 1 and avoid transitions from stop mode 0 to stop mode 1 (or vice versa) for the MultiCAN module.

Please note that bit KSCCFG.MODEN should only be set by SW while all configuration fields are configured for run mode 0.

Controller Area Network (MultiCAN) Controller

22.4.4 Connection of External Signals

The following table shows the digital connections of the MultiCAN signals with other modules or pins in the XC27x8X device.

The selected input signal (selected by bit field RXSEL) for each CAN node is made available by signal CANxINS (CAN node x input signal, with x = 4 - 0). These signals can be used in the SCU for wake-up purposes and to allow two CAN nodes receive the same signal (analysis and safety feature).

Table 22-18 MultiCAN Connections in XC27x8X

Signal	from/to Module	I/O to CAN	Can be used to/as
MultiCAN Node 0 Signals			
RXDC0A	P2.3	I	receive input A (NPCR0.RXSEL = 000 _B)
RXDC0B	P0.3		receive input B (NPCR0.RXSEL = 001 _B)
RXDC0C	P2.0		receive input C (NPCR0.RXSEL = 010 _B)
RXDC0D	P2.6		receive input D (NPCR0.RXSEL = 011 _B)
RXDC0E	ESR1		receive input E (NPCR0.RXSEL = 100 _B)
RXDC0F	P11.0		receive input F (NPCR0.RXSEL = 101 _B)
RXDC0G	1		receive input G (NPCR0.RXSEL = 110 _B)
RXDC0H	0		receive input H (NPCR0.RXSEL = 111 _B)
TXDC0	P0.1	O	transmit output
	P0.2		
	P2.1		
	P2.4		
	P2.5		
	P11.1		

Controller Area Network (MultiCAN) Controller

Table 22-18 MultiCAN Connections in XC27x8X (cont'd)

Signal	from/to Module	I/O to CAN	Can be used to/as
MultiCAN Node 1 Signals			
RXDC1A	P2.4	I	receive input A (NPCR1.RXSEL = 000 _B)
RXDC1B	P0.4		receive input B (NPCR1.RXSEL = 001 _B)
RXDC1C	P2.7		receive input C (NPCR1.RXSEL = 010 _B)
RXDC1D	CAN0INS		receive input D (NPCR1.RXSEL = 011 _B)
RXDC1E	ESR2		receive input E (NPCR1.RXSEL = 100 _B)
RXDC1F	P8.1		receive input F (NPCR1.RXSEL = 101 _B)
RXDC1G	1		receive input G (NPCR1.RXSEL = 110 _B)
RXDC1H	0		receive input H (NPCR1.RXSEL = 111 _B)
CAN1INS	U1C1_DX0F	O	
TXDC1	P0.6	O	transmit output
	P2.2		
	P2.9		
	P8.2		
MultiCAN Node 2 Signals			
RXDC2A	P4.3	I	receive input A (NPCR2.RXSEL = 000 _B)
RXDC2B	P10.11		receive input B (NPCR2.RXSEL = 001 _B)
RXDC2C	CAN1INS		receive input C (NPCR2.RXSEL = 010 _B)
RXDC2D	P2.13		receive input D (NPCR2.RXSEL = 011 _B)
RXDC2E	P6.1		receive input E (NPCR2.RXSEL = 100 _B)
RXDC2F	P5.15		receive input F (NPCR2.RXSEL = 101 _B)
RXDC2G	1		receive input F (NPCR2.RXSEL = 110 _B)
RXDC2H	0		receive input H (NPCR2.RXSEL = 111 _B)
TXDC2	P4.1	O	transmit output
	P4.2		
	P10.12		
	P6.0		
	P2.12		

Controller Area Network (MultiCAN) Controller

Table 22-18 MultiCAN Connections in XC27x8X (cont'd)

Signal	from/to Module	I/O to CAN	Can be used to/as
MultiCAN Node 3 Signals			
RXDC3A	P3.3	I	receive input A (NPCR3.RXSEL = 000 _B)
RXDC3B	P3.0		receive input B (NPCR3.RXSEL = 001 _B)
RXDC3C	P10.14		receive input C (NPCR3.RXSEL = 010 _B)
RXDC3D	CAN2INS		receive input D (NPCR3.RXSEL = 011 _B)
RXDC3E	P0.5		receive input E (NPCR3.RXSEL = 100 _B)
RXDC3F	1		receive input F (NPCR3.RXSEL = 101 _B)
RXDC3G	1		receive input G (NPCR3.RXSEL = 110 _B)
RXDC3H	0		receive input H (NPCR3.RXSEL = 111 _B)
TXDC3	P3.1 P3.2 P10.13 P0.7	O	transmit output
MultiCAN Node 4 Signals			
RXDC4A	P3.4	I	receive input A (NPCR4.RXSEL = 000 _B)
RXDC4B	P7.0		receive input B (NPCR4.RXSEL = 001 _B)
RXDC4C	P10.7		receive input C (NPCR4.RXSEL = 010 _B)
RXDC4D	CAN3INS		receive input D (NPCR4.RXSEL = 011 _B)
RXDC4E	P1.7		receive input E (NPCR4.RXSEL = 100 _B)
RXDC4F	1		receive input F (NPCR4.RXSEL = 101 _B)
RXDC4G	1		receive input G (NPCR4.RXSEL = 110 _B)
RXDC4H	0		receive input H (NPCR4.RXSEL = 111 _B)
TXDC4	P3.6 P7.1 P7.2 P10.6	O	transmit output

MultiCAN Node 5 Signals

Controller Area Network (MultiCAN) Controller

Table 22-18 MultiCAN Connections in XC27x8X (cont'd)

Signal	from/to Module	I/O to CAN	Can be used to/as
RXDC5A	P1.4	I	receive input A (NPCR4.RXSEL = 000 _B)
RXDC5B	P11.4		receive input B (NPCR4.RXSEL = 001 _B)
RXDC5C	P2.1		receive input C (NPCR4.RXSEL = 010 _B)
RXDC5D	CAN4INS		receive input D (NPCR4.RXSEL = 011 _B)
RXDC5E	1		receive input E (NPCR4.RXSEL = 100 _B)
RXDC5 [G:F]	1		receive inputs [G:F] (NPCR4.RXSEL = 101 _B to 110 _B)
RXDC5H	0		receive input H (NPCR4.RXSEL = 111 _B)
TXDC5	P2.0 P7.2 P11.3	O	transmit output

General MultiCAN Signals

INT_O[15:0]	interrupt controller	O	interrupt output lines (service requests) ¹⁾
	INT_O15 to CCU62 and CCU63		notification for timer start on .

1) CAN interrupts are shared with interrupts of other modules. See the ISSRx register description.

22.4.5 MultiCAN Module Register Address Map

In addition to the standard address location of the MultiCAN module in the address segment 20 0000_H, an alternative address location has been introduced. This location allow accessing the USIC channels and the MultiCAN module with the same data page pointer in the address segment 20 8000_H, with the USIC addresses from 20 B000_H to 20 BBFF_H. Like this, each MultiCAN register can be accessed at two addresses, one standard location, starting at 20 0000_H and one alternative location, starting at 20 8000_H.

Note: The complete and detailed address map of the MultiCAN modules is described in the chapter "Register Overview" of the XC27x8X System Units.

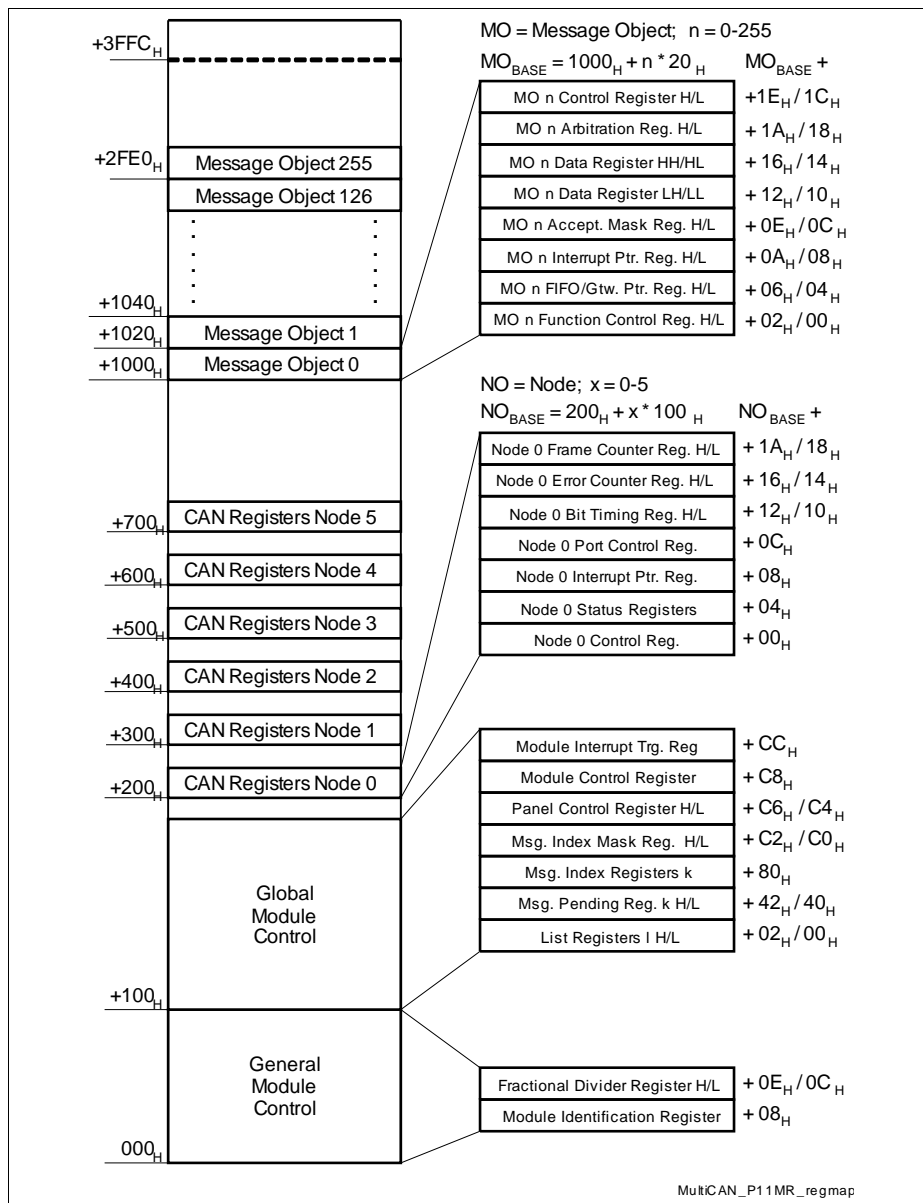
In the MultiCAN module address range, the following register blocks are located at the offset start addresses, see [Figure 22-24](#):

- 0000_H General registers for clock control, fractional divider, ID
- 0100_H Global Module Control registers
- 0200_H CAN node 0 registers
- 1000_H Message object memory (32 bytes for each object)

The CAN RAM is automatically initialized after reset by the list controller in order to ensure correct list pointers in each message object. The end of this CAN RAM initialization is indicated by bit PANCTR.BUSY becoming inactive. Before the end of the initialization sequence, the CAN module must not be accessed with other instructions than polling for bit PANCTR.BUSY.

The CAN RAM can be optionally enabled for parity detection. The feature is controlled in the SCU.

Controller Area Network (MultiCAN) Controller



MultiCAN_P11MR_regmap

Figure 22-24 MultiCAN Module Register Map

22.4.6 Module Base Address Table

In the XC27x8X, the registers of the MultiCAN module are located in the following address ranges:

Table 22-19 Registers Address Space

Module	Base Address	End Address	Note
CAN	20 0000 _H	20 3FFF _H	16 KB
CANa	20 8000 _H	20 AFFF _H	12 KB

Keyword Index

A

Acronyms 1-3
 ADC
 Equidistant Sampling **17-94**
 Address Windows (External Bus) 12-9
 Addressing Modes
 Code Addressing 5-33
 CoREG Addressing Mode 5-47
 DSP Addressing Modes 5-43
 Indirect Addressing Modes 5-41
 Long Addressing Modes 5-38
 Short Addressing Modes 5-36
 ALU 5-54
 Atomic Instruction 5-8

B

Baudrate
 Bootstrap Loader 14-25
 Bit
 Manipulation 5-58
 Manipulation Instructions 15-2
 Protected 3-16
 Protection 5-58
 reserved 2-15
 Block Diagram ITC / PEC 7-4
 Bootstrap Loader 14-18
 Branch Prediction 5-7
 Bus Phases (External Bus) 12-3
 Byte Write Configuration (EBC) 12-15

C

C166S-V2 5-1
 CAN
 Block diagram 22-2
 Clock control 22-100
 Features 22-2
 Functional description 22-4
 Interrupt structure 22-103
 Module implementation 22-104
 MultiCAN

Analysis mode 22-19
 Bit timing 22-10
 Block diagram 22-7
 Error handling 22-12
 Gateway mode 22-42
 Interrupts 22-13
 Message acceptance filtering
 22-22
 Message object FIFO 22-37
 Message object lists 22-14
 Node control 22-10

Overview 22-4

Registers

LISTiH **22-58**
 LISTiL **22-58**
 MCR **22-56**
 MITR **22-57**
 MOAMRnH **22-94**
 MOAMRnL **22-94**
 MOARnH **22-95**
 MOARnL **22-96**
 MOCTRnH **22-79, 22-81**
 MOCTRnL **22-80, 22-81**
 MODATAnHH **22-99**
 MODATAnHL **22-99**
 MODATAnLH **22-98**
 MODATAnLL **22-98**
 MOFCRnH **22-88**
 MOFCRnL **22-90**
 MOFGPRnH **22-92**
 MOFGPRnL **22-92**
 MOIPRnH **22-86**
 MOIPRnL **22-86**
 MSIDk **22-61**
 MSIMASKH **22-62**
 MSIMASKL **22-62**
 MSPNDkH **22-60**
 MSPNDkL **22-60**
 NBTRxH **22-71**
 NBTRxL **22-72**
 NCRx **22-63**

NECNTxH **22-73**
 NECNTxL **22-73**
 NFCRxH **22-75**
 NFCRxL **22-76**
 NIPRx **22-69**
 NPCRx **22-70**
 NSRx **22-66**
 PANCTRH **22-51**
 PANCTRL **22-51**
 CAPCOM12
 Capture Mode 19-9
 Counter Mode 19-6
 CAPCOM2 2-15
 Capture Mode
 GPT1 16-19
 GPT2 (CAPREL) 16-53
 CCU6 2-17
 Clock
 generation 2-30
 output signal 9-23
 Clock System
 Main oscillator 9-5
 Oscillator run detection 9-16
 Clock system
 Clock source 9-8
 Gain control 9-6
 PLL, see "PLL"
 Concatenation of Timers 16-18, 16-51
 Context Switch 5-28
 Count direction 16-5, 16-43
 Counter 16-17, 16-51
 Counter Mode (GPT1) 16-9, 16-47
 CPU 2-6, 5-1
 CPU Stack Pointer 5-49

D

Data Page 5-39
 Demultiplexed External Bus 12-5
 Development Support 1-1
 Direction
 count 16-5, 16-43
 Division 5-60
 Double-Register Compare 19-18

DPP 5-39
 DSP Processing 5-62

E

EBC
 Address Windows 12-9
 Bus Phases 12-3
 Byte Write Configuration 12-15
 Idle State 12-13
 Interface 12-1
 Ready Control 12-11
 Register Description 12-14
 Shutdown Control 12-21
 Timing 12-2
 ESR 9-74
 ESRx 7-1
 EXTBUS 12-1
 Extend Instruction 5-8
 External
 Bus 2-11
 Interrupts 7-46
 External Bus **12-1**

F

FADC
 Data reduction filter 17-78
 Registers
 CRRn **17-85**
 FCRn **17-82, 17-84**
 Flags 5-53–5-56
 Flash
 Command Sequences 3-26
 Change Read Margin 3-29
 Change Read Timing 3-29
 Clear Status 3-28
 Disable Read Protection 3-36
 Disable Write Protection 3-37
 Enter Page Mode 3-30
 Enter Security Page Mode 3-31
 Erase Page 3-34
 Erase Sector 3-33
 Erase Security Page 3-35
 Load Page Word 3-31

Program Page 3-32
 Re-Enable Read/Write Protection 3-37
 Reset to Read 3-28
 Concurrent Program/Erase 3-39
 Definitions 3-20
 Array 3-21
 Block 3-21
 Drain Disturb 3-21
 Endurance 3-20
 Erasing 3-20
 Memory 3-21
 Page 3-21
 Programming 3-20
 Retention 3-20
 Sector 3-21
 ECC 3-41
 EEPROM Emulation 3-54
 Interrupt Generation 3-56
 Linear Code Pre-Fetch 3-24
 Logical Sectors 3-43
 Margin Reads 3-42
 Operating Modes 3-22
 Command Mode 3-23
 Page Mode 3-23
 Read Mode 3-22
 Protection
 Details 3-45
 Determining RPA and WPA 3-48
 Effective Read Security 3-49
 Effective Write Security 3-49
 Examples 3-52
 Lower Layer "Physical State" 3-46
 Middle Layer "Flash State" 3-47
 Overview 3-42
 Security Pages 3-51
 Upper Layer "Protection State" 3-48
 Recommendations
 EEPROM Emulation 3-57
 Programming Code and Constant Data 3-56
 Recommendations 3-56

Sequence Errors 3-38
 Wait States 3-24, 3-61
 Fractional divider
 Block diagram 22-106
 Operating modes 22-108
 Suspend mode 22-109
 Frequency
 output signal 9-23

G

Gated timer mode (GPT1) 16-8
 Gated timer mode (GPT2) 16-46
 GPRs
 General Purpose Registers 5-24
 GPT 2-18
 GPT1 16-3
 GPT12E
 Register Table 16-78
 GPT2 16-41

I

ICACHE **6-1**
 Address Space 6-2
 Coherency 6-3
 Data Access 6-5
 Data Integrity 6-4
 ECC 6-4
 Enable 6-3
 Replacement 6-3
 Statistic 6-6
 Idle State (External Bus) 12-13
 IMB 3-58
 Block Diagram 3-58
 Error Reporting Summary 3-81
 Overview 3-58
 Registers
 Overview 3-60
 Startup, Shutdown 3-80
 Incremental Interface Mode (GPT1) 16-10
 Instruction 15-1
 Bit Manipulation 15-2
 Pipeline 5-9
 Pointer 5-34

protected 15-6
Interface
 External Bus 12-1
Interrupt
 External 7-46
 Latency 7-49
 Priority 7-9
 RTC 18-13
 System 2-8, 7-3
IO Area
 CPU Pipeline behaviour **5-10**

L

Latency
 Interrupt, PEC 7-49
Long Transfer Mode **7-39**
LXBUS 12-1
LXBus 2-12

M

MAC Unit 5-62
Mask Protection 5-58
Memory 2-10, 3-1
 Address Space Overview 3-1
 CPU behavior when accessing IO Area **5-10**
 Data Retention Memories 3-83
 Data SRAM (DSRAM) 3-10
 Dual-Port RAM (DPRAM) 3-10
 External Memory Space 3-18
 Flash 3-14, **3-20**
 Flash Emulation 3-13
 IMB 3-58
 IO Areas 3-17
 Little Endian 3-2
 Marker Memory (MKMEM) 3-11
 Memory Map 3-3
 On-Chip Program Memory Map 3-12
 Program/Data SRAM (PSRAM) 3-13
 Protected Bits 3-16
 Register Areas 3-5
 Standby RAM (SBRAM) 3-11
 Accesses 3-83

System Stack 3-15
Memory checker
 Functionality 4-2, 4-3
 Interfaces 4-22
 Polynomials 4-8
 Preferable usage 4-11
 Principal of LFSR 4-5
 Principle of MISR 4-7
Register
 COUNT **4-20**
 ID **4-16**
 IR **4-17**
 Overview 4-15
 RRH **4-18**
 RRL **4-17**
 TPRH **4-21**
 TPRL **4-21**

MPU
 Registers Overview 8-3
Multiplexed External Bus 12-6
Multiplication 5-60

N

Non-Segmented Mode 5-33

O

OCDS
 Requests 7-48

P

P11_HE Block Diagram 2-1
PD+ Bus
 Bit Protection 5-58
PEC
 Latency 7-49
 Long Transfer Mode **7-39**
 Short Transfer Mode **7-38**

Peripheral
 Summary 2-13
Pins 11-1
Pipeline 5-9
PLL **9-7**
 Functionality 9-7

Switching parameters 9-17
 Port 2-29
 Temperature compensation 9-181
 Ports
 Configuring a Pin 10-15
 Output register Pn_OUT 10-10
 Pad driver control 10-7
 Structure
 Analog 10-5
 Digital I/O and Analog Input 10-4
 Hardware Override 10-3
 Prefetch 5-5
 Protected
 instruction 15-6
 Protected Bits 3-16, 5-58

R

Ready Control (External Bus) 12-11
 Real Time Clock (->RTC) 2-20, 18-1
 Registers
 EBC 12-14
 Reserved bits 2-15
 Reset 9-54
 Module behavior 9-62
 RTC 2-20, 18-1
 interrupt 18-13

S

Segmented Mode 5-33
 Short Transfer Mode **7-38**
 Shutdown Control (EBC) 12-21
 System Stack 5-49

T

Temperature compensation 9-181
 Timer 16-3, 16-41
 Auxiliary Timer 16-14, 16-48
 Concatenation 16-18, 16-51
 Core Timer 16-5, 16-43
 Counter Mode (GPT1) 16-9, 16-47
 Gated Mode (GPT1) 16-8
 Gated Mode (GPT2) 16-46
 Incremental Interface Mode (GPT1)

16-10
 Mode (GPT1) 16-7
 Mode (GPT2) 16-45
 Timing (External Bus) 12-2
 Tools 1-1

U

USIC

ASC mode 21-110
 Automatic shaping 21-118
 Baud rate 21-116
 Bit timing 21-115
 Collision detection 21-116
 Data transfer interrupts 21-120
 EOF control 21-118
 Frame format 21-111
 Noise detection 21-116
 Protocol interrupts 21-119
 Protocol registers 21-123
 Pulse shaping 21-117
 Receive buffer 21-121
 Signals 21-110
 Sync-break detection 21-121
 Transfer status 21-121
 Baud rate 21-8
 Channel structure 21-5
 Data buffer 21-10
 Data shifting and handling 21-9
 Data transfer interrupts 21-21
 External frequency 21-41
 Feature set 21-2
 FIFO buffer 21-11
 FIFO data buffer 21-79
 Fractional divider 21-41
 General interrupts 21-20
 IIC mode 21-161
 Baud rate 21-166
 Byte stretching 21-166
 Data bit symbol 21-173
 Data flow handling 21-174
 Frame format 21-164
 Master arbitration 21-166
 Master transmission 21-178

- Mode control 21-167
- Protocol interrupts 21-168
- Protocol registers 21-179
- Receiver address acknowledge 21-169
- Receiver handling 21-169
- Receiver status 21-170
- Signals 21-162
- Start symbol 21-172
- Stop symbol 21-173
- Symbol timing 21-171
- Transmission chain 21-166
- Transmit data 21-174
- IIS mode 21-185
 - Baud rate 21-194
 - Connection of Audio devices 21-188
 - Data interrupts 21-192
 - Frame and word length 21-189
 - Mode control 21-189
 - Protocol interrupts 21-197, 21-198
 - Protocol overview 21-187
 - Protocol registers 21-199
 - Receive data 21-193
 - Signals 21-185
 - Slave mode operation 21-198
 - Transfer delay 21-187, 21-190
 - Transmit data 21-192
 - WA generation 21-195, 21-196
- Implementation
 - Address map 21-207
 - Channels 21-206
 - I/O lines of USIC0 21-213
 - I/O lines of USIC1 21-216
 - I/O lines of USIC2 21-219
 - I/O lines of USIC3 21-222
 - I/O lines of USIC4 21-224
 - Interrupt registers 21-210
 - Overview 21-205
- Input stages 21-6, 21-36
- Kernel registers
 - Baud rate registers 21-46
 - BRGH 21-50
 - BRGL 21-48
 - BYP 21-89
 - BYP CRH 21-91
 - BYP CRL 21-89
 - CCFG 21-28
 - CCR 21-25
 - Channel control and configuration registers 21-25
 - Data buffer registers 21-69
 - DX0CR 21-38
 - DX1CR 21-38
 - DX2CR 21-38
 - FDRH 21-47
 - FDRL 21-46
 - FIFO buffer and bypass registers 21-89
 - FMRH 21-68
 - FMRL 21-67
 - INPRH 21-32
 - INPRL 21-31
 - Input stage register 21-38
 - INx 21-105
 - KSCFG 21-29
 - OUTDRH 21-107
 - OUTDRL 21-107
 - OUTRH 21-106
 - OUTRL 21-106
 - Overview 21-14
 - PCRH 21-33, 21-126, 21-154, 21-179, 21-201
 - PCRL 21-33, 21-123, 21-152, 21-179, 21-199
 - Protocol registers 21-33
 - PSCR 21-35
 - PSR 21-34, 21-127, 21-156, 21-182, 21-202
 - RBCTRH 21-102
 - RBCTRL 21-101
 - RBUF 21-76
 - RBUF0 21-70
 - RBUF01SRH 21-73
 - RBUF01SRL 21-70
 - RBUF1 21-73

RBUFDF 21-77
 RBUFSR 21-78
 SCTRHF 21-59
 SCTRL 21-57
 TBCTRHF 21-99
 TBCTRL 21-98
 TBUFx 21-69
 TCSRHF 21-65
 TCSRL 21-60
 Transfer control/status registers
 21-57
 TRBPTRHF 21-109
 TRBPTRL 21-108
 TRBSCH 21-96
 TRBSRH 21-95
 TRBSRL 21-92
 Mode control 21-19
 Module registers
 USIC0_IDH 21-209
 USIC0_IDL 21-208
 USIC1_IDH 21-209
 USIC1_IDL 21-208
 USIC2_IDH 21-209
 USIC2_IDL 21-208
 USIC3_IDH 21-209
 USIC3_IDL 21-208
 USIC4_IDH 21-209
 USIC4_IDL 21-208
 Output signals 21-7
 Protocol control and status 21-18
 Protocol interrupts 21-24
 Protocol related counter 21-42
 Receive buffering 21-55
 Registers overview 21-14
 SSC mode 21-131
 Automatic Shadow mechanism
 21-139
 Baud rate 21-143
 Data frame control 21-140
 EOF control 21-148, 21-151
 Master mode 21-143
 Protocol interrupts 21-147, 21-150
 Protocol registers 21-152

Receive buffer 21-141
 Signals 21-131
 Slave mode 21-150
 Slave select delay 21-146
 Slave select generation 21-144
 Time quanta counter 21-44
 Transmit buffering 21-51

W

Watchdog 2-28
 Watchdog Timer 9-185
 Kernel Registers 9-191
 Modes of operation
 Disable Mode 9-188
 Normal Mode 9-187
 Prewarning Mode 9-188
 Period calculation 9-186

Z

Zero-Cycle Jump 5-7

Register Index

A

ADC0_KSCFG 17-13
 ADCx_ALR0 17-61
 ADCx_ASENr 17-49
 ADCx_BWDCFG 17-98
 ADCx_BWDENr 17-98
 ADCx_CHCTRr 17-54
 ADCx_CHINCR 17-110
 ADCx_CHINFR 17-109
 ADCx_CHINPRr 17-114
 ADCx_CRCRr 17-31
 ADCx_CRMRRr 17-29
 ADCx_CRPRr 17-32
 ADCx_EMCTR 17-104
 ADCx_EMENr 17-103
 ADCx_EVINCR 17-108
 ADCx_EVINFR 17-107
 ADCx_EVINPRr 17-111
 ADCx_GLOBCFG 17-18
 ADCx_GLOBCTR 17-17
 ADCx_GLOBSTR 17-20
 ADCx_ID 17-15
 ADCx_INPRr 17-56
 ADCx_LCBRRr 17-59
 ADCx_Q0Rr 17-43
 ADCx_QBURr 17-44
 ADCx_QINRr 17-42
 ADCx_QMRr 17-38, 17-84
 ADCx_QSRr 17-40
 ADCx_RCRr 17-69
 ADCx_RESRAVr 17-67
 ADCx_RESRAr 17-67
 ADCx_RESRVr 17-66
 ADCx_RESRRr 17-66
 ADCx_RSIRr 17-45
 ADCx_RSPRRr 17-50
 ADCx_RSSR 17-68
 ADCx_SYNCTR 17-93
 ADCx_VFR 17-71
 ADDRSEL7 12-24

ADDRSELx 12-19

C

CAN_LISTiH 22-58
 CAN_LISTiL 22-58
 CAN_MCR 22-56
 CAN_MITR 22-57
 CAN_MOAMRnH 22-94
 CAN_MOAMRnL 22-94
 CAN_MOARnH 22-95
 CAN_MOARnL 22-96
 CAN_MOCTRnH 22-79, 22-81
 CAN_MOCTRnL 22-80, 22-81
 CAN_MODATAnHH 22-99
 CAN_MODATAnHL 22-99
 CAN_MODATAnLH 22-98
 CAN_MODATAnLL 22-98
 CAN_MOFRCrH 22-88
 CAN_MOFRCrL 22-90
 CAN_MOFGRPrH 22-92
 CAN_MOFGRPrL 22-92
 CAN_MOIPRnH 22-86
 CAN_MOIPRnL 22-86
 CAN_MSIDk 22-61
 CAN_MSIMASKH 22-62
 CAN_MSIMASKL 22-62
 CAN_MSPNDkH 22-60
 CAN_MSPNDkL 22-60
 CAN_NBTRxH 22-71
 CAN_NBTRxL 22-72
 CAN_NCRr 22-63
 CAN_NECNTxH 22-73
 CAN_NECNTxL 22-73
 CAN_NFCRrH 22-75
 CAN_NFCRrL 22-76
 CAN_NIPRRr 22-69
 CAN_NPCRRr 22-70
 CAN_NSRr 22-66
 CAN_PANCTRrH 22-51
 CAN_PANCTRrL 22-51
 CAPREL 16-64

CC2_DRM 19-40
 CC2_KSCCFG 19-43
 CC2_M4/5/6/7 19-37
 CC2_OUT 19-39
 CC2_SEE 19-42
 CC2_SEM 19-42
 CCU6x_CC63R 20-64
 CCU6x_CC63SR 20-64
 CCU6x_CC6xR 20-33
 CCU6x_CC6xSR 20-34
 CCU6x_CMPMODIF 20-39
 CCU6x_CMPSTAT 20-37
 CCU6x_IEN 20-98
 CCU6x_INP 20-101
 CCU6x_IS 20-91
 CCU6x_ISR 20-96
 CCU6x_ISS 20-94
 CCU6x_KSCFG 20-112
 CCU6x_KSCSR 20-114
 CCU6x_MCMOUT 20-87
 CCU6x_MCMOUTS 20-86
 CCU6x_MODCTR 20-78
 CCU6x_PISELH 20-109
 CCU6x_PISELL 20-107
 CCU6x_PSLR 20-83
 CCU6x_T12 20-32
 CCU6x_T12DTC 20-35
 CCU6x_T12MSEL 20-40
 CCU6x_T12PR 20-32
 CCU6x_T13 20-62
 CCU6x_T13PR 20-63
 CCU6x_TCTR0 20-41
 CCU6x_TCTR2 20-44
 CCU6x_TCTR4 20-47
 CCU6x_TRPCTR 20-80
 CP 5-31
 CPUCON1 5-21
 CPUCON2 5-22
 CSP 5-34

D

DPP0/1/2/3 5-39

E

EBCMOD0 12-14
 EBCMOD1 12-16

F

FADC_CRR0 17-85
 FADC_FCR0 17-82, 17-84
 FADC_FCR1 17-82, 17-84
 FADC_FCRn 17-82
 FCONCS7 12-23
 FCONCSx 12-18
 FL_KSCCFG 3-77

G

GPT12E_CAPREL 16-64
 GPT12E_KSCCFG 16-75
 GPT12E_T2,-T3,-T4 16-28
 GPT12E_T2CON 16-32, 16-34
 GPT12E_T3CON 16-30
 GPT12E_T5,-T6 16-63
 GPT12E_T5CON 16-67
 GPT12E_T6CON 16-65

I

ICACHE_CTRL 6-8
 ICACHE_DACON 6-11
 ICACHE_DATAx 6-14
 ICACHE_ECCLH 6-15
 ICACHE_EDCON 6-9
 ICACHE_HIT 6-18
 ICACHE_HMCON 6-17
 ICACHE_MISS 6-18
 ICACHE_RADD 6-12
 ICACHE_TAG 6-16
 ICACHE_WADD 6-13
 IDX0/1 5-43
 IMB module registers 3-60
 IMB_ECC_STAT 3-74
 IMB_ECC_TRAP 3-72
 IMB_FSR_BUSY 3-66
 IMB_FSR_OP 3-67
 IMB_FSR_PROT 3-68

IMB_IMBCTRH 3-63
 IMB_IMBCTRL 3-61
 IMB_INTCTR 3-64
 IMB_MAR0 3-70
 IMB_PROCONx 3-72
 IP 5-34

M

MAH 5-67
 MAL 5-66
 MCHK_COUNT 4-20
 MCHK_ID 4-16
 MCHK_IR 4-17
 MCHK_RRH 4-18
 MCHK_RRL 4-17
 MCHK_TPRH 4-21
 MCHK_TPRL 4-21
 MCW 5-63
 MDC 5-61
 MDH 5-60
 MDL 5-61
 MEM_KSCCFG 3-76
 MPU_PM0 8-5
 MPU_PMx 8-7
 MPU_PRA 8-9
 MPU_PRD 8-7
 MPU_PRLx 8-4
 MPU_PRUx 8-4
 MRW 5-70
 MSW 5-68

O

ONES 5-72

P

Pn_DIDIS
 P15 10-17
 P5 10-17
 P6 10-17
 Pn_IN 10-13
 Pn_IOCRx 10-14
 Pn_OMRH
 P10 10-11

P2 10-11
 Pn_OMRL 10-11
 Pn_OUT 10-10
 Pn_POCON 10-8
 Ports
 Pn_DIDIS 10-17
 Pn_IN 10-13
 Pn_IOCRx 10-14
 Pn_OMR 10-11
 PSW 5-53

Q

QR0/1 5-42
 QX0/1 5-44

R

RTC_CON 18-6
 RTC_IC 18-15
 RTC_ISNC 18-14
 RTC_KSCCFG 18-16
 RTC_RELH/L 18-10
 RTC_RTCH/L 18-9
 RTC_T14 18-8
 RTC_T14REL 18-8

S

SBRAM module registers 3-85
 SBRAM_DATA0 3-88
 SBRAM_DATA1 3-89
 SBRAM_RADD 3-85
 SBRAM_WADD 3-86
 SP 5-50
 SPSEG 5-50
 STKOV 5-52
 STKUN 5-52

T

T2, T3, T4 16-28
 T5, T6 16-63
 T5CON 16-67
 T6CON 16-65
 TCONCS7 12-22
 TCONCSx 12-17

U

USIC0_IDH 21-209
 USIC0_IDL 21-208
 USIC1_IDH 21-209
 USIC1_IDL 21-208
 USIC2_IDH 21-209
 USIC2_IDL 21-208
 USIC3_IDH 21-209
 USIC3_IDL 21-208
 USIC4_IDH 21-209
 USIC4_IDL 21-208
 UxCy_BRGH 21-50
 UxCy_BRGL 21-48
 UxCy_BYP 21-89
 UxCy_BYPCRH 21-91
 UxCy_BYPCRL 21-89
 UxCy_CCFG 21-28
 UxCy_CCR 21-25
 UxCy_DX0CR 21-38
 UxCy_DX1CR 21-38
 UxCy_DX2CR 21-38
 UxCy_FDRH 21-47
 UxCy_FDRL 21-46
 UxCy_FMRH 21-68
 UxCy_FMRL 21-67
 UxCy_INPRH 21-32
 UxCy_INPRL 21-31
 UxCy_INx 21-105
 UxCy_KSCFG 21-29
 UxCy_OUTDRH 21-107
 UxCy_OUTDRL 21-107
 UxCy_OUTRH 21-106
 UxCy_OUTRL 21-106
 UxCy_PCRH 21-33, 21-126, 21-154,
 21-179, 21-201
 UxCy_PCRL 21-33, 21-123, 21-152,
 21-179, 21-199
 UxCy_PSCR 21-35
 UxCy_PSR 21-34, 21-127, 21-156,
 21-182, 21-202
 UxCy_RBCTRH 21-102
 UxCy_RBCTRL 21-101

UxCy_RBUF 21-76
 UxCy_RBUF0 21-70
 UxCy_RBUF01SRH 21-73
 UxCy_RBUF01SRL 21-70
 UxCy_RBUF1 21-73
 UxCy_RBUFD 21-77
 UxCy_RBUFSR 21-78
 UxCy_SCTRH 21-59
 UxCy_SCTRL 21-57
 UxCy_TBCTRH 21-99
 UxCy_TBCTRL 21-98
 UxCy_TBUFx 21-69
 UxCy_TCSRH 21-65
 UxCy_TCSRL 21-60
 UxCy_TRBPTRH 21-109
 UxCy_TRBPTRL 21-108
 UxCy_TRBSCR 21-96
 UxCy_TRBSRH 21-95
 UxCy_TRBSRL 21-92

Z

ZEROS 5-72

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