International
IR Rectifier

Space Grade DC-DC Converter Revolutionizes Low Power RF Designs with Proprietary Design Topology

By

Tiva Bussarakons, Marketing Director

International Rectifier, Aerospace and Defense

Abstract

A space grade multiple output DC-DC converter design platform offers world class performance and cost benefits with established assembly outlines for most custom requirements. IR's Mx series targets low power RF (radio frequency) equipment onboard a spacecraft where the converter's key performance include very low input/output noise and its capability to orderly sequence the outputs during power up and power down. The design platform incorporates proprietary design topology that can accommodate most major satellite power buses and a wide range of output voltage and output current combinations while maintaining the same assembly outlines for most design applications. With its extensive design heritage, design qualification and established design analysis templates, the Mx series offers the space industry the truly cost effective design solutions that minimize program risk and a very short time to market.

Introduction

Standards for power requirements and form factors for equipment designs do not exist for space applications. Major satellite manufactures establish their own power bus standards, the main power line that regulates the power from the solar panels and delivers regulated voltage to all the payload and system equipment. Most have a unique input/output voltage range, voltage level and dynamic behavior, tele-command (TC) and telemetry (TLM) interfaces among the subsystems are also very distinctive. The converters' output voltages and powers while dictated by the types of load are often very unique even from one payload design or program to the next. The distinction or lack of standards is believed to be due to the competitive nature of the industry. Each manufacture attempts to gain a competitive edge on functional performances and overall power conversion efficiency resulting in uniqueness in designs and the lack of similarity in power converters. No two DC-DC converters are alike.

IR's Mx design platform is created with these diverse input, output and functional requirements in mind. In addition to insistence for high efficiency and functional performances, the space industry when making any make/buy decisions for a DC-DC converter for new equipment designs, demands design documentation/analyses and flight heritage to mitigate program risks that may cause slippage in delivery schedule and added costs.

Target Applications

Mx design platform targets low RF power design applications requiring power up to 15W. The platform is developed specifically for sensitive RF equipment onboard a spacecraft, i.e., receivers, transmitters, beacons, low noise amplifiers (LNAs), and up/down converters. Mx design platform is designed for continuous operations in radiation environments that are presented to commercial, military and scientific missions operating in long term geosynchronous (GEO), medium earth (MEO) and low earth (LEO) orbits.

Platform Description

Mx series is a radiation hardened multiple outputs DC-DC converter design platform that can be adapted to most satellite input and output power requirements. The design topology allows simple component changes in the primary section to accommodate different bus voltages. While most design applications require power up to 15W, the platform has adequate design margin to accommodate slightly higher combined output power than 15W. The platform includes TC/TLM design that can be readily adapted to most major satellite interface requirements. The Mx series also includes a hold-up capacitor bank and electrical circuitry to insure proper turn-on and turn-off timing among the outputs, a critical biasing sequence for GaAs FET devices commonly used for RF power amplifiers.

Two standard assembly outlines exist. MA platform is for output power up to 5W. MB platform with a slightly larger outline is for output power of up to 15W. Open board PCB style construction is chosen to facilitate design adaptation and design changes as needed. Proprietary design simulation tools and design analysis templates are created to quickly and accurately provide performance projection and design tradeoffs where decision in design changes can be made with a high level of confidence. The platform offers RF equipment designers the ability to react and incorporate last minute design adjustments with very little or no impact to program schedule.

Platform Design Benefits

In addition to deliverable hardware, i.e., engineering model (EM), engineering qualification model (EQM), preflight model (PFM), and flight model (FM), almost all space programs require extensive design, qualification and program documentations. These items typically include preliminary/critical design review meetings, thermal analysis, stress analysis, reliability analysis, worst case analysis, failure mode effect analysis, radiation susceptibility analysis, acceptance and qualification test procedures/reports, monthly program reports, updated program schedule, weekly status update, and dedicated program management function.

These deliverable items, program review and design review meetings usually incur substantial costs and impact program schedule and often time become the pacing items when design changes occur. The Mx design configuration and the proprietary simulation and design tools are primed to lessen the schedule and cost impacts. The following generic design tools and templates allow a new design or a design change to be processed and completed in an expeditious manner.

- Established printed circuit board designs for diverse design requirements
- Standardized I/O interfaces and interface control drawings (ICDs)

- Analysis baselines
- Generic component types and declared components list
- Manufacturing travelers, assembly processes, test setup and test procedure templates
- Design analysis templates
- Environmental qualification test procedure templates or previous qualification of similar designs

Key Performances and Features

Key performances and functional features of Mx series can be summarized as follow

- Accommodates most major power buses, 28V, 50V, 70V, and 100V
- Integrated input filter to insure EMC/EMI compatibility to most satellite power buses
- No limitation on number of outputs though most requirements are triple output configuration
- Each output can be configured to meet output voltage levels up to 15V and any current level up to 1A
- Guaranteed voltage accuracy and regulation to within 1% begin-of-life (BOL) and 2% end-of-life (EOL) accounting for temperature, radiation and aging effects
- No cross regulation and cross talk as each output is independently regulated
- Two design patents are deployed to maximize efficiency performance
- Efficiency is in the range of 65 to 75% depending on output voltage, current and power.
- Each output uses linear regulator enabling output noise to be less than 1 mVRMS
- Conducted susceptibility (CS) rejection is as high as 100 dB as a result of a two stage regulation design
- Outputs are orderly sequenced during power-up and power-down to insure proper biasing for RF amplifier devices
- Isolated ON/OFF tele-command and ON/OFF status telemetry with a latching relay
- Two established assembly outlines for differing output powers
- All components are space flight qualified class S

Samples of Actual Performances

Waveforms below taken from products delivered to customers are samples of the actual performances.

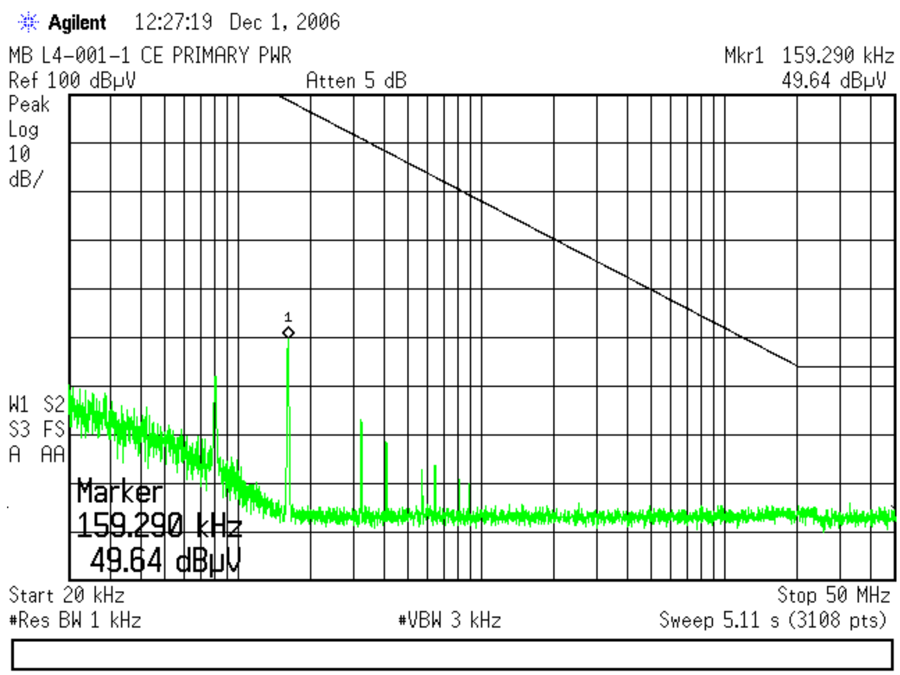

Figure 1 – EMC Performance

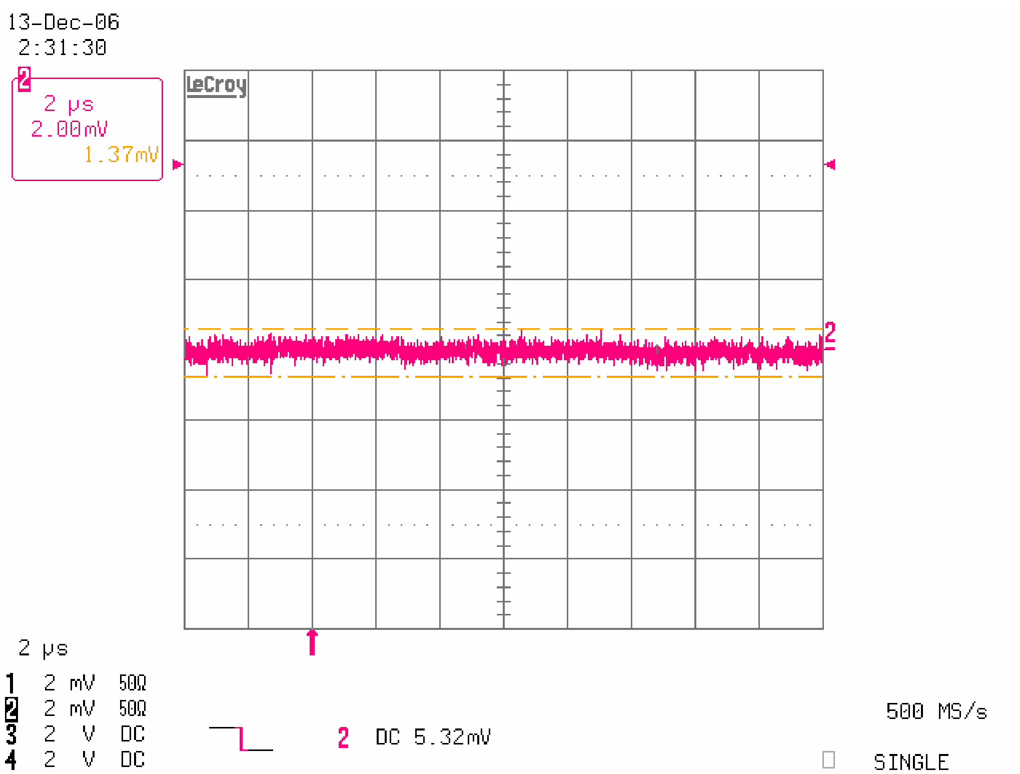

Figure 2– Output Ripple/Noise

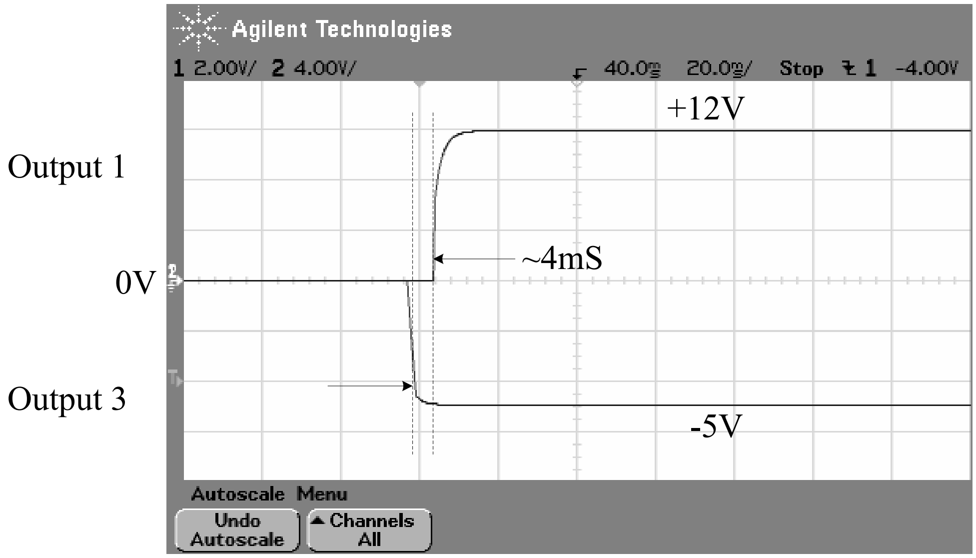

Figure 3 – Outputs Timing During Turn-on, Output 1 (+12V) vs. Output 3 (-5V)

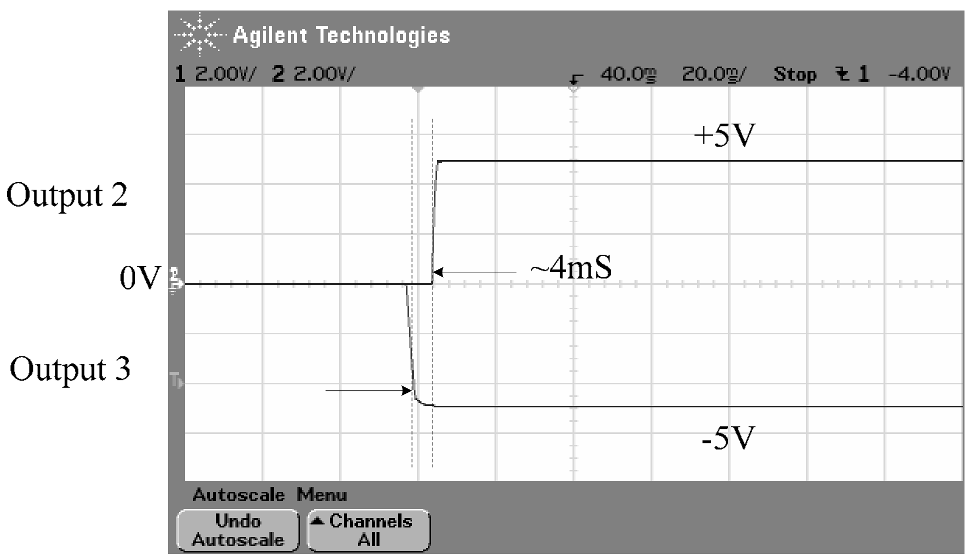

Figure 4 - Outputs Timing During Turn-on, Output 2 (+5V) vs. Output 3 (-5V)

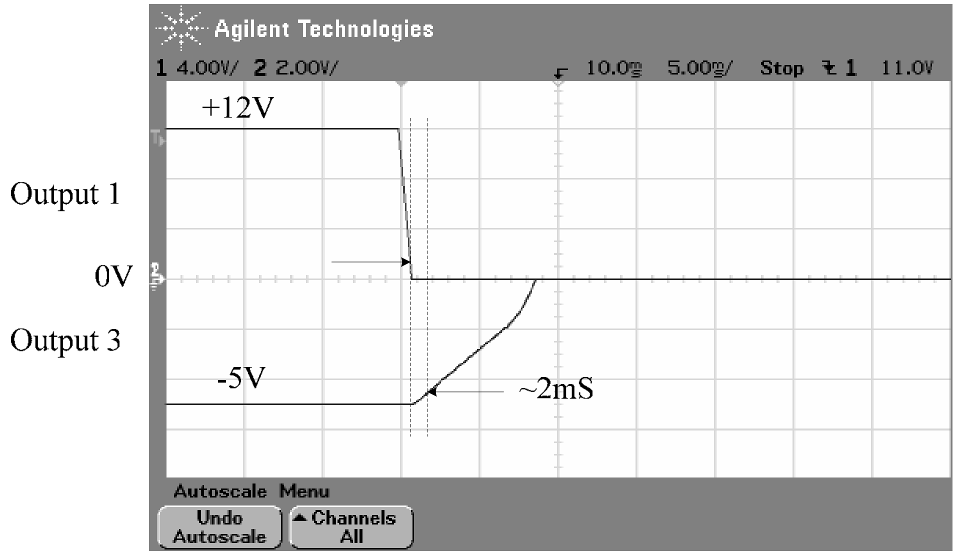

Figure 5 – Outputs Timing During Turn-off, Output 1 (+12V) vs. Output 3 (-5V)

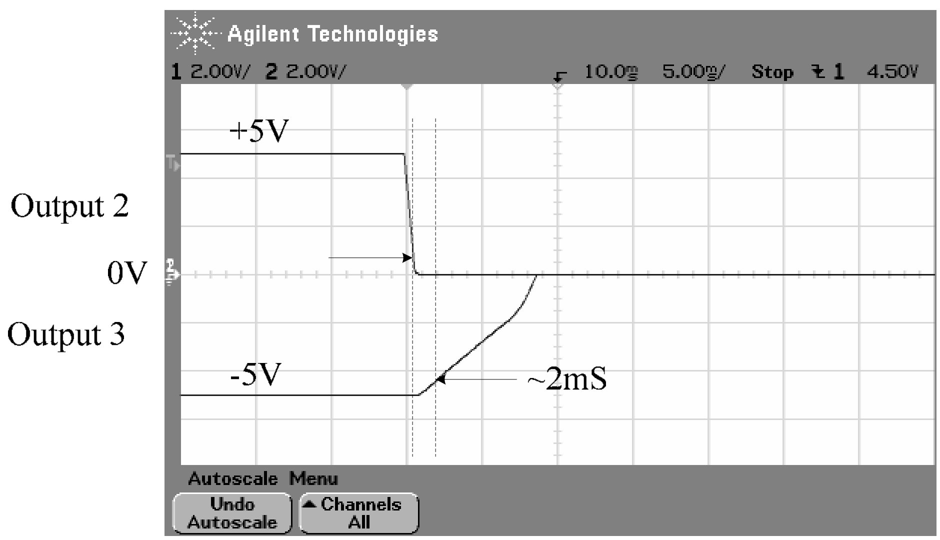

Figure 6 – Outputs Timing During Turn-off, Output 2 (+5V) vs. Output 3 (-5V)

Design Description

Functional block diagram shown in Figure 7 represents the design topology for both the MA and MB platforms. The differences are highlighted by the shaded blocks. They include the primary power stage, power transformer and output rectification scheme. While triple output designs are common for most applications, the platform can easily be configured to accommodate any number of outputs i.e., 2, 4 or more, with the limitation being the total combined output power requirements. Refer to Figure 8 for an example of an MB platform assembly.

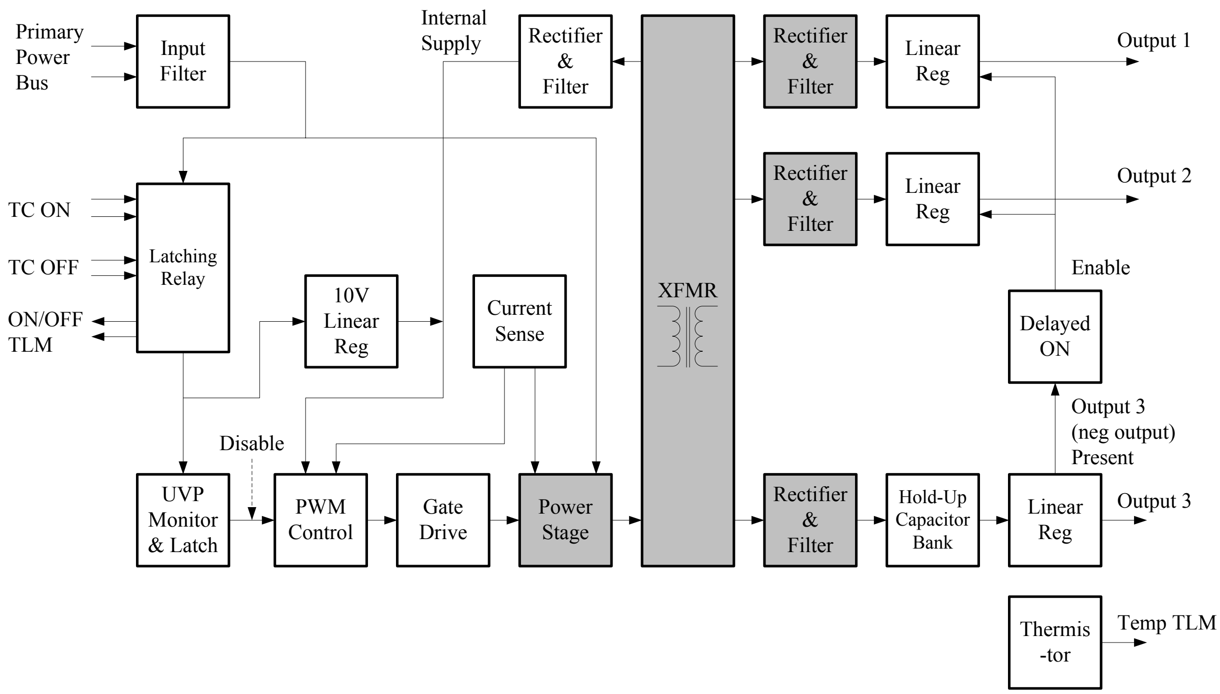

Figure 7 – Mx Series Functional Block diagram

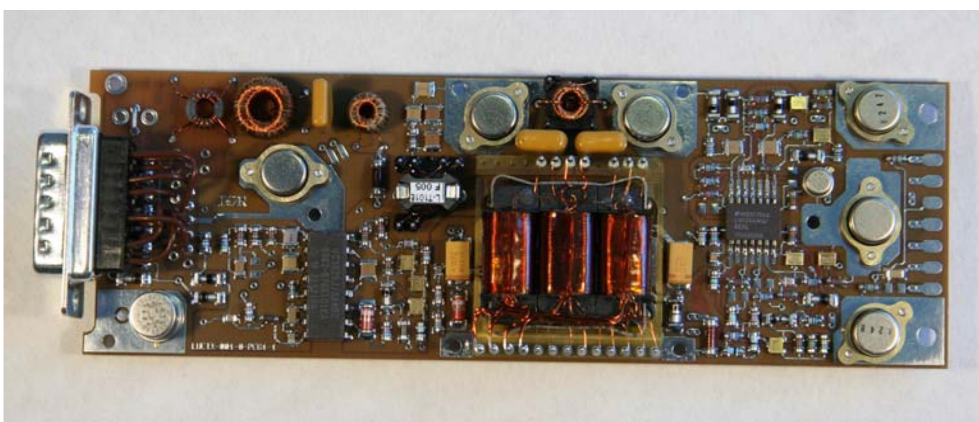

Figure 8 – MB Platform Assembly

Design Topology

Both the MA and MB designs deploy dual voltage regulation stages, one in the primary and one in the secondary. Regulation in the primary uses current mode control topology to maximize efficiency. The topology also offers inherent current regulation and primary over-current protection. Regulation in the primary is built around a standard PWM controller with known performance characteristics in the targeted radiation environments. Voltage regulation is performed on the internal 10V supply via a bootstrap winding of the power transformer (XFMR). All primary circuitries including PWM controller and gate drive circuitry are powered by an internal 10V linear regulator upon power up. The internal 10V supply takes over all biasing responsibility upon achieving regulation.

All primary input circuitries are galvanically isolated from the secondary output via a power transformer. Secondary voltages of the transformer are stepped down, rectified and filtered feeding downstream output regulators. All outputs are independently regulated by linear voltage regulators which offer inherent excellent noise and regulation performances. The regulators use discrete components with a bipolar transistor as a pass element to minimize voltage headroom and maximize efficiency. The regulator circuit is a proprietary design that has been used successfully for many design applications. Extremely low output noise and high CS rejection are possible with the dual stage regulation scheme. Guaranteed end of life (EOL) performances for voltage accuracy and regulation can be demonstrated through worst case and aging design analysis. Please refer to Table 1 for specific performance limits.

MA vs. MB

While both the MA and MB platforms deploy the same basic design topology, there are some differences in the power train designs. MA platform uses a single switch flyback power stage with traditional flyback transformer and simple output rectification/filter design configuration. This simplifies the converter design which minimizes components count and size. The MB platform accommodates higher output power requirements that are greater than 5W. A patented Hy-bridge rectifier (Ref. 1) topology and integrated magnetic (Ref. 2) in conjunction with two-switch half bridge power stage is chosen to maximize converter's efficiency. Unlike the traditional method of rectification, the proprietary Hy-bridge rectifier arrangement yields only one voltage drop which reduces output rectification losses and increases efficiency.

Outputs Timing

Outputs 1 and 2 are typically designated as positive outputs. Each output commences to turn on only after Output 3 (negative output) reaches regulation band by way of an 'Enable' signal generated by internal circuitries. A capacitor bank with sufficient energy storage capacity is added preceding Output 3 to insure adequate hold-up time for Output 3 to maintain regulation until Outputs 1 and 2 decay to safe level nearing zero volt during a power-down sequence. Samples of turn-on and turn-off waveforms are shown in Figure 3 through 6 above.

Output Voltage/Current Range

All three output regulators can accommodate wide output voltage/current range with the limitation on the combined output power. Please refer to Table 1 for more detail voltage and current limitations for each of the outputs. The regulators use a common design with slight design variations for different voltage and current requirements.

Input/Output Power Train

Both the single-switch flyback and two-switch half bridge can easily accommodate a wide range of input voltages. The switch elements are selected based on the operating input bus voltage and dynamic transient conditions. Transformer design and turn-ratios are adjusted accordingly. The output rectifiers may require different voltage and current ratings. MA and MB assembly outline designs have taken into account all the changes in component foot prints due to the deviations in input and output requirements. The established PCB layouts and dimensions can normally be maintained for most design applications.

Input Filter

The Mx platform also includes an input filter design that yields very low reflected line noise and is expected to satisfy EMI/EMC requirements of most major satellite power buses. While the design will change to accommodate different input bus voltages, the change in the filter components have very little or no impact on the assembly layouts. Figure 1 above presents an actual performance.

TC/TLM/Temperature Telemetry

The TC/TLM interface is designed to accommodate a standard high level pulse command using latching relay providing the necessary isolation. The telemetry ON/OFF status is bi-level. The TC/TLM interfaces are isolated from one another and from any other functional and input/output terminals within the converter. Temperature telemetry is available and can be included as required.

Mechanical Design, Assembly Outlines and Cooling

Assemblies of the MA and MB designs are open board PCB style construction populated with a combination of the traditional thru-hole and surface mount components. MA outline dimensions are 3.346”L x 2.402”W x 0.768”H (85.0 mm L x 61.0 mm W x 19.5 mm H) and 6.0”L x 2.0”W x 0.709”H (152.4 mm L x 50.8 mm W x 18.0 mm H) for MB. The electrical interface is achieved via solderable terminals for the MA series and combination of sub-D connector and solderable terminals for the MB series. Assembly can be fastened to host equipment as part of an overall RF equipment or a higher level assembly with on-board mounting holes. Cooling is required. The mounting holes used for mechanical or assembly support are also used to conduct heat from the assembly. The assembly package designs lend themselves to output and input customization without deviation to the assembly outlines. Refer to Figures 9 below for an MB assembly outline dimensions.

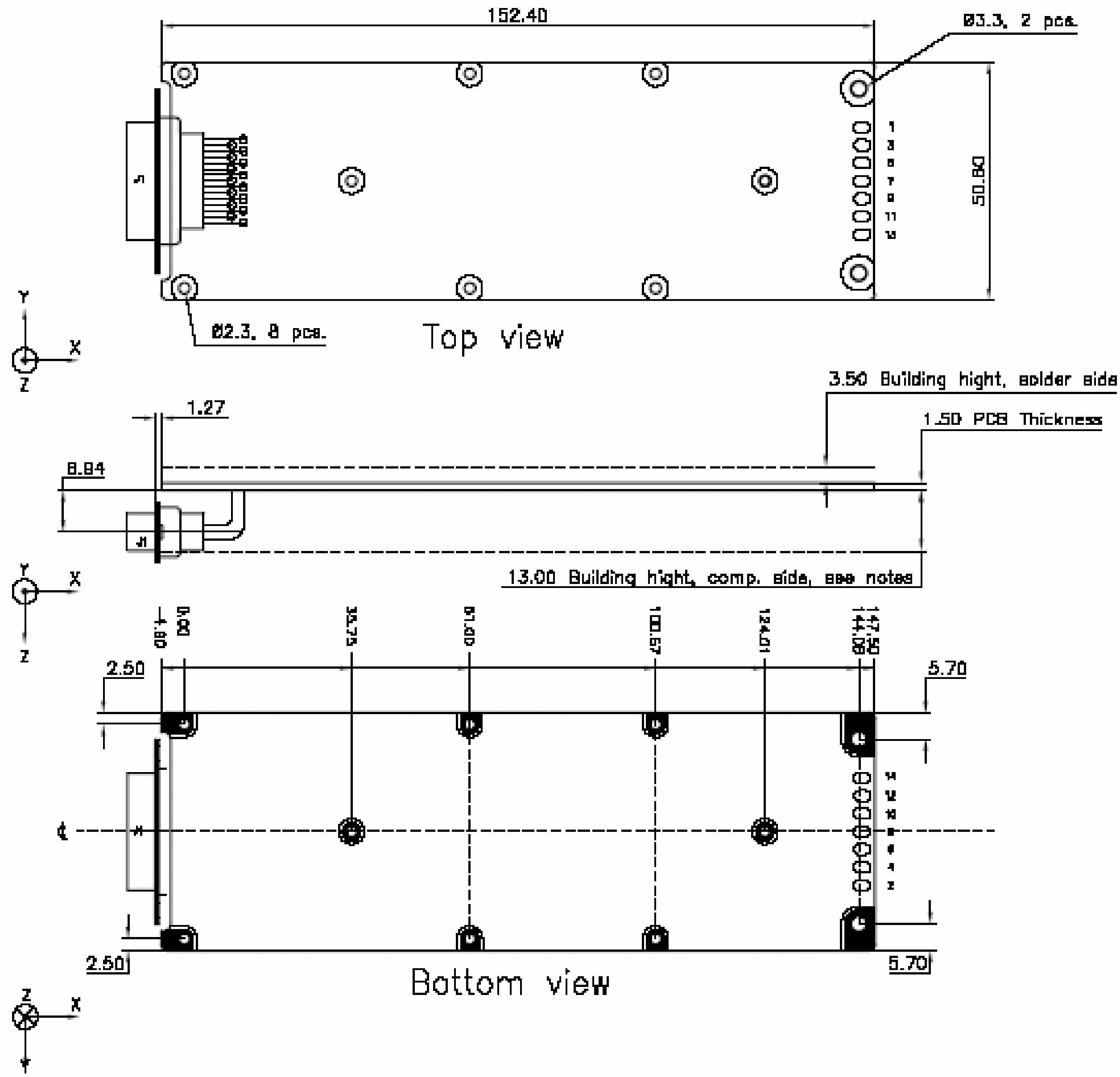

Figure 9 – MB Assembly Outline

Key Performance Summary:

Following is a summary of key generic performances for both the MA and MB platforms.

Parameter	Performance
Electrical	
Input DC-Bus Voltage	28V unregulated; 50V, 70V, 100V regulated
Input Under Voltage Protection	Automatic shutdown if input drops below a threshold. Auto restart or UVP latch is possible. ±1V hysteresis

Parameter	Performance
Output 1	Vout: 3 to 15V fixed ±1% initial setting & temperature BOL, ±2% EOL radiation and aging Iout: 0 to 1000 mA, 6W max
Output 2	Vout: 6 to 15V fixed, ±1% initial setting & temperature BOL, ±2% EOL radiation and aging Iout: 0 to 1000 mA, 6W max
Output 3	Vout: -2 to -15V fixed, ±1% initial setting & temperature BOL, ±2% EOL radiation and aging Iout: 0 to 1000 mA, 4W max
Output Power	MA: 5W max MB: 15W max (slightly higher power is possible)
Overload and Short Circuit Protection	All outputs can withstand a continuous short circuit and overload conditions.
No-Load Operation	No-load operation will not cause excessive over voltage or damage
Output Over Voltage Protection	Single point failure free regarding over voltage at the output
Output Sequencing	Output 3 (designated negative output) will reach regulation first at turn on before Output 1 & 2 begin to rise. It will remain in regulation until Outputs 1 & 2 decays to near zero volt before it begins to fall when powered down.
Efficiency	65 to 75% depending on input DC bus and output voltage
Isolation	Input, output and tele-command port are isolated from one another, >1Mohms and <50 nF
Tele-command	High level pulse command (latching relay)
Telemetry – ON/OFF Status	Bi-level derived from +5V line
Temperature Telemtery	Thermistor type TBD depending on application
EMC - Conducted Emission on Output	<1 mVrms, frequency domain of 100Hz – 50 MHz
EMC – Conducted Emission on Input	0 - 100 KHz: 80 dbμArms 100 KHz – 10 MHz: -20 db/dec 10 MHz – 50 MHz: 40 dbμArms
EMC – Conducted Susceptibility	>90 dB for Iout >500 mA >100 dB for Iout ≤ 500 mA. Primary power sine wave injection of 2 Vp-p, 100 Hz – 50 MHz.
Inrush current	200% max. of maximum steady state input current upon TC command upon TC <10A – hot plug-in (4V/μS)
Life Time	15 years minimum in orbit 18 years design life time for aging
Reliability	<180 FIT at 60ºC per MIL-HDBK-217F, Notice F2, based on 0.035FIT for soldering and crimp and dissipated power is

Parameter	Performance
	used instead of rated power for MOSFETs
Mechanical & Environmental Properties	
Temperature	Acceptance: -20ºC to +75ºC Qualification: -25ºC to +85ºC Cold Start: -40ºC Non-Operating: -40ºC to +85ºC
Size	MA: 85mm x 61mm x 19.5mm or 3.346"x2.402"x0.77" (LxWxH) MB: 152.4mm x 50.8mm x 18mm or 6"x 2"x 0.71" (LxWxH)
Mass	MA: 75 grams max. MB: 130 grams max.
Vibration	Meets typical launch requirements
Shock	Meets typical launch requirements

Table 1 – Key Performance Summary

Design Heritage

At the time of this writing, IR is under contracts to complete eleven different configurations of the Mx platforms, several of which have been delivered to customers. The platform can be customized to accommodate most major power buses. The power buses the IR design team has experience with are as follows:

Alcatel SPACEBUS 3000, 50V
Alcatel SPACEBUS 4000, 100V
Astrium EUROSTAR 2000, 26-43V
Astrium EUROSTAR 3000, 50V
Space Systems Loral FS1300, 97-100V
Lockheed Martin A2100, 54.5-70V
NPOPM Express A, 22-31V
NPOPM Express, 22-33V
Orbital STAR-1, 24-36V
Orbital STAR-2, 23-36V
ISRO (Indian Space Research Organization), 26-43V
BSS (Boeing Satellite Systems), HS601 HP
ESA (European Space Agency), 28V

Program Milestone Development Schedule

Power converters for space design applications are known to require a lengthy development cycle. Typical delivery lead time for flight models (FM) may range from 12 to 18 months or longer in some instances depending on complexity and last minute changes in requirements. IR's Mx design platform offers much shorter lead time. Delivery of FM hardware with complete SDRL items can be expected in about 8 months. Following is a typical program milestone schedule for an Mx converter.

International Rectifier

Milestone Event	**Timeline***
1. Kick-Off Meeting	1 week
2. Initial design (ICD, I/F, etc.)	1 month
3. Detailed Design	2 months
4. Preliminary Design Review (PDR)	2½ months
5. Internal Elegant Breadboard (EBB)	3 months
6. EM/EQM Delivery	5½ months
7. Critical Design Review (CDR)	6 months
8. Manufacturing and Test Readiness Review	7 months
9. FM delivery, 1st Unit (10-15 FMs/week)	8 months

* After receipt of order

Please note that design analyses and other deliverable documents are normally submitted at a preliminary format at PDR. The final versions are part of a CDR data package.

Summary

Mx design platform is created to meet market demand for high performance low power multiple output DC-DC converters specifically for lower RF equipment on board a satellite. The platform is designed to accommodate requirements that could only be met by a customized design that normally requires long development and engineering cycle time. Mx platform offers two standard assembly outlines. Last minute design changes can normally be accommodated without altering the standard package assemblies. A EBB can be designed, developed and be available for engineering evaluations in 3 months. FMs with complete deliverable design analyses and qualification documentations can be delivered in about 8 months. With proprietary design simulation, design analysis templates and extensive design heritage, the platform is truly the design solution to mitigate program risks with very short time to market.

Acknowledgement

I would like to thanks the following colleagues for their valuable input and technical supports:

Dung Nguyen
Kare Lund
Lass Pedersen

References

1. U.S. Patent No. 4 899 271

2. U.S. Patent No. 5 335 163

3. “MB70150T Generic DC/DC Converter”, Kare Lund, International Rectifier, Aerospace & Defense, Denmark, March 2006.

4. “Military Satellites Pose Engineering Challenges in DC-DC Converter Development”, Tiva Bussarakons, Defense Electronics, A Primedia Publication, May 2004.

5. “Thick Film Hybrid DC-DC Converters are Standard ‘Brick’ for Satellite Power Systems’, Tiva Bussarakons, Defense Electronics, RF Design, June 2006.