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A novel high efficient approach to input bridges

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Abstract: Almost all equipments used in our daily life are supplied from the power line. They are all around us, we use several of them every day: TV sets, DVDs, chargers, computers, refrigerators, washing machines, dishwashers etc... All these equipments have one or more input diode-bridges to convert the 50-60Hz (400Hz in aircrafts) sinusoidal waveform, at different AC voltage depending on the country, to a rectified DC bus that is then stepped down to a lower voltage to feed the electronics or directly used to supply the inverter for motors.
This paper presents an innovative approach to implement the input bridge, using a self-driven synchronous rectification technique that allows the realization of a simple device with only four pins, as a direct high-efficient replacement of exiting standard input rectification devices.

1. Introduction

With the advent of electronic controls there are everyday fewer devices connected to our power lines that directly use the supplied AC voltage. Normal process is to convert the AC into a DC line and then use the latter to supply the electronics or the inverterised motors that are today's replacing old fashioned Induction AC motors. Also power factor correction moved from passive (capacitor's bank) to active solution, where this is possible.
This means that an input diode-bridge is always there, no matter if the system is using a PFC stage or not, and the well know implementation is shown in **Fig.** 1. This structure has a big drawback in efficiency since, no matter the current flow, two corresponding diodes are always in conduction inserting a fixed dropout and consequent power loss depending on current flow.

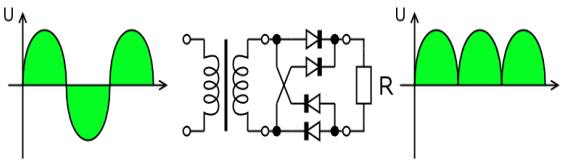

Fig. 1: AC line input and rectified DC output

In many applications where the power delivered to the output is not very high and the power dissipated into the four diodes is low, this configuration may remain a good cost-effective solution.

2. The synchronous rectification

It's well known, that a MOSFET structure has a parasitic diode in parallel with the FET, it is then possible to obtain a full bridge using 4 FETs, as shown in **Fig. 2**
The voltage across a standard diode is about 0.6V-1.0V, depending on the current flowing into it and the technology the diode is made of, and it's the major cause of the power loss in the bridge. Ever worse may appear the case of using only the body-diode of a Fet but if the Fet is driven using a synchronous rectification technique, then the body-diode conducts only for a very short part of the waveform, corresponding to the dead-times of the controlled Fets, and the Fets are forced in conduction for the major portion of the sinusoidal current input. Let's now make a simple test: consider a double wave (full) rectifier bridge and assume that the voltage across the diode in conduction mode is 0.6V only, we compare this against an active-bridge, having 4 Fets with a R_{DSON} @100°C equal to 10mOhm. The system output average current is 5A.
Table 1 shows the total efficiency comparison between the two solutions.

	Calculation	Expected Power Loss [W]	Comment
Diode	$2 \times V_F \times I_{AVG\text{-}RECT}$	6	Fairly large
MOSFET	$2 \times R_{DSon} \times I^2$in-rms	0.6	Reduced by ~90%

Table 1: Power losses comparison between standard and active input bridge

3. Practical implementation and circuit description

We easily understand at this point that using power Fets, in an active-bridge configuration with synchronous rectification control, is the way to improve efficiency and reduce or avoid an expensive and bulky heat-sink.
Using International Rectifier synchronous rectification ICs, IRF1166 and IRF1167 [1], the implementation becomes quite easy and the complete schematic of the active bridge is shown in

Fig 3. The ON-OFF transition of each Fet is controlled by the respective ICs, sensing each Drain to Source voltage. When this is negative the body-diode is on and the Fet is turned on, when the Vds voltage reaches back the 0V level, the IC turns off the Fet.

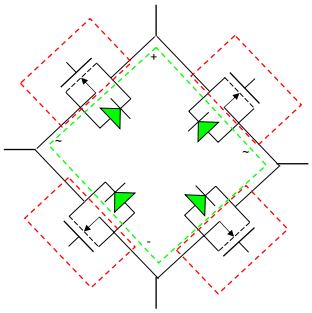

Fig. 2: A Mosfets Bridge

The turn-off threshold must be negative and as close as possible to 0V, in order to prevent a short circuit condition through high side and low side FET on the same leg. A drawback is that, at the end the current will force again the conduction of the body diode, but for a very short time. An internal high precision circuit measures constantly the Vds voltages, to accomplish this task; it has to be noted than the IC should also be able to withstand a very high voltage across the same sensing pins when the Fet is off since the other Fet in the same leg is on. The technical challenge is to have a comparator capable to detect few millivolts in a semi-period and then accepting several hundreds of volts across the same sensing pins in the next sinusoid semi-period. This is achieved thanks to IR Gen 5 HVIC technology integrating low voltage precise and fast components with high voltage devices and isolation barriers [2].

3.1 Working principle

At the beginning of the sinusoidal cycle, the current starts flowing into the body diode, generating a negative Vd-s voltage across the Fet, at that point the FET is turned on by the IC and the drop-out voltage across the component falls to a much lower voltage, increasing the system efficiency and reducing power losses.

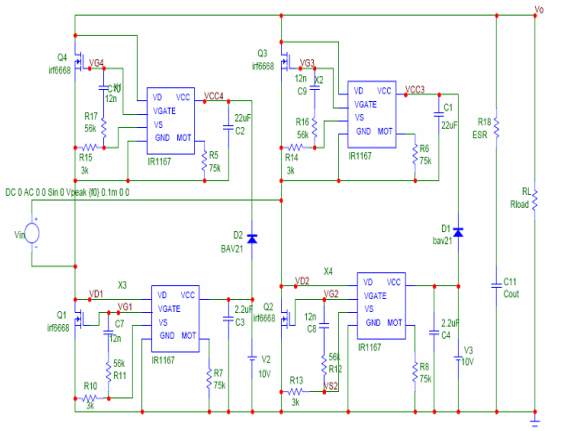

Fig. 3: Active Bridge practical implementation using 4 discrete IR1167 ICs

Once the FET is on, it must remain in this state until the rectified current will decrease to almost zero, the closer the better, so a zero crossing comparator can be used to understand when the drain-source voltage reaches the 0V condition. For this purpose the IC's turn-off threshold must be negative and close to zero, to avoid respectively cross conduction and reduce the body-diode conduction interval at the tail of the semi-sinusoid.

The IR1167 has been developed as a synchronous rectification IC, then its internal blanking times are in the order of ns to μS, however working at line frequency, quite long blanking times (or leading edge blanking intervals) must be implemented to avoid false triggering of the IC sensing circuit.

In fact, due to the low frequency operation and slow (sinusoidal) current ramp-up, it is often likely that after the first turn-on the FET's drop-out falls almost immediately below the turn-off threshold and the IC starts turning it on and off. This shows up as a square-wave ringing in the gate voltage of the Fets on that phase until the current reaches a decent level sufficient to generate enough drop-out across the FET in on-state**.** A similar ringing can be observed at the end of the semi-sinusoid when the Fet first is turned off, again for the same slow current slope. This behavior appears especially with resistive loads and sinusoidal current waveforms, while in the case of a capacitive load the situation is different since the current at FETs turn-on and off is steeper and a shorter blanking is needed. In normal operation each semi-cycle of the current takes in conduction 2 FETs, for half the line frequency (8.3ms or 10ms) and no ringing at turn-on or turn-off appears. To increase the internal IR1167 blanking times we added a RC network in the sensing loop, as it will be described in the next section.

3.2 The bootstrap supply and blanking time networks

As well known, in every line semi-period, only two FETs work, while the others remain off and their respective bulk diodes are reverse biased. It's evident that when Q2 and Q4 are on, Q1 and Q3 are instead off and the bootstrap diode D1 permits to recharge the bootstrap capacitors C1, which supply the high side devices IC3; in the other hand, when Q1 and Q3 are on it is the diode D2 that charges the bootstrap capacitor C2 supplying IC4. The RC network added between the Vgate and Vs pins of each IC generates the longer blanking times needed in this application. It is simply a derivative network that, using the same gate transition voltage applied to the FET, adds a temporary current pulse through the series resistor placed between the FET's source and the IC's Vs pins. The result is an artificial increase or decrease of the thresholds for a certain time, adding thus a longer blanking time that can be trimmed just changing the three RC network component values. Let's observe one of the four sections, X3, shown in **Fig.3**. At turn on, the gate voltage ramps up and the rising edge, partitioned, appears across the resistance R10, with the positive sign versus the Vs pin. This masks the real Fets drop-out and prevents the internal comparator of the IC, top left of **Fig 4,** from turning off the Fet. On the other hand, when the IC turns off the gate, the falling edge appears with the negative sign towards the Vs pin, effectively shifting the sensed voltage and inhibiting the turn on section, for as long as decided thru the RC network values.

4. System simulation

The system has been implemented in Microcap Simulator and a dedicated sub-circuit for the IR1167 has been prepared, see **Fig. 4**. Particular attention has been done in allowing the IR1167 model to work with a floating ground since the two upper devices in the schematic need to follow the AC input line and cannot be referenced to ground.
The simulation parameters are the following:

- Vin = 60Vpeak
- F = 50Hz
- Rload = 5Ω to 40Ω
- Cout = 0 to 1000 μF - ESR = 300mΩ

Several simulations have been run to test the system functionality and verify the effectiveness of the idea before proceeding with a hardware implementation.

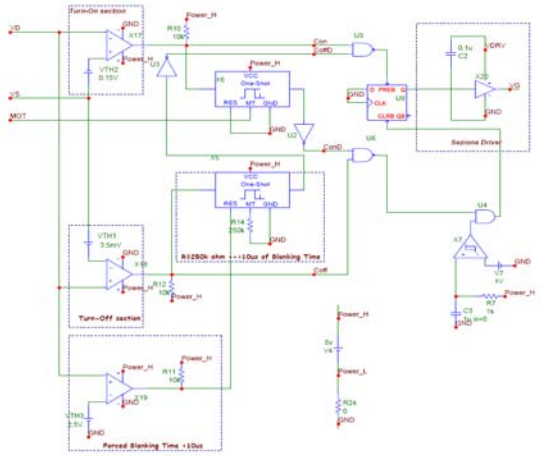

Fig.4: IR1167 sub circuit

4.1 Resistive load

The first series of simulations have been done comparing the Active Bridge Behaviour with the behaviour of a standard schottky diodes bridge, the following figures will show the obtained results. The schottky bridge was using 4x MBR10100 in TO220AB package while the 100V FET used in the Active Bridge was our DirectFet IRF6644. **Fig.5** shows the case of maximum load (5Ω), with a maximum peak output current of 12A and an average output power of about 360W.
In this case we could see perfectly the sinusoidal output voltage (green curve) and the currents (light-blue curve), while in the center appear the rectangular gate voltages of the low side Fets. It's also worth pointing out the sinusoidal shape of the floating Mos gate voltage in the central waveform, since they have to follow the sinusoidal input with a positive offset of 10.7V (Vgate).

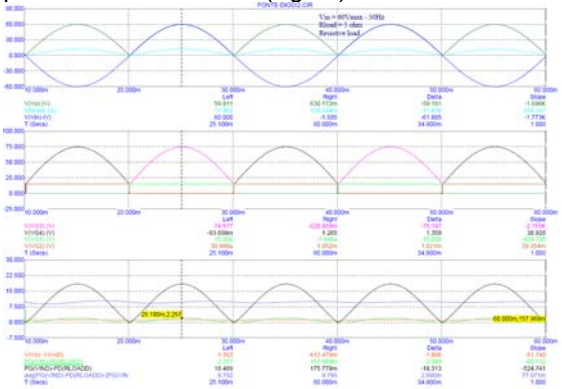

Fig. 5: Rload = 5ohm, Cout = 0
Top: Vin, Vout and Vo,
Center: Vg1, Vg2, Vg3 and Vg4
Bottom: Vo-Vo(schottky), Pdiss(active bridge), Pdiss (schottky), Pdiss(active bridge)-Pdiss(schottky)

The third plot, in the bottom, shows the power improvement of this solution, the sinusoidal black

trend of the power dissipated in the four diodes reaches the peak of 18W while the same peak for the active bridge barely gets close to 2.25W, this means a difference in average, plotted in the blue curve, of about 10W. At light load the situation may be different and the more complex circuit may not get enough benefit to justify its realization against a simple four diodes bridge; however the interesting results are plotted in Fig.6.

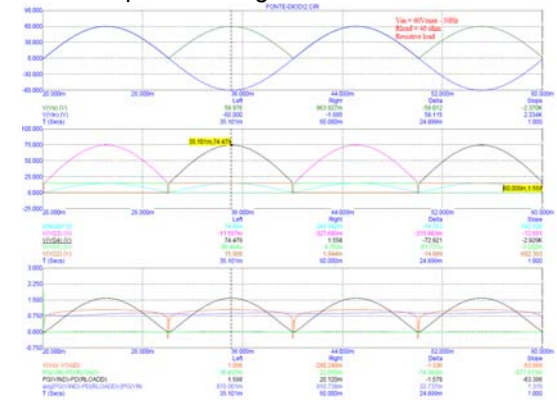

Fig. 6: Rload = 40ohm, Cout = 0
Top: Vin, Vout and Vo,
Center: Vg1, Vg2, Vg3 and Vg4
Bottom: Vo-Vo(schottky), Pdiss(active bridge), Pdiss (schottky), Pdiss(active bridge)-Pdiss(schottky)

In this last case the output power is only 45W, we still have a large difference in term of peak power dissipated, that is 0.036W against 1.6W and an average power loss gain of about 1W.

4.2 Capacitive load

A capacitive load certainly represents a more realistic application for a power line AC-DC converter. **Figs 7-8** show the results of the simulations respectively with 5Ω-40Ω and a total output capacitance of 1000µF.

The average gain on power loss changes from 20% at heavy load (5Ω) to about 5% at light load (40Ω). Also, it's worth pointing out that the package size of 4 diodes MBR10H100 occupy a footprint area of about 580mm^2 against only 120mm^2 if using 4 IRF6644 direcfets, achieving a pcb space saving of about 80%.

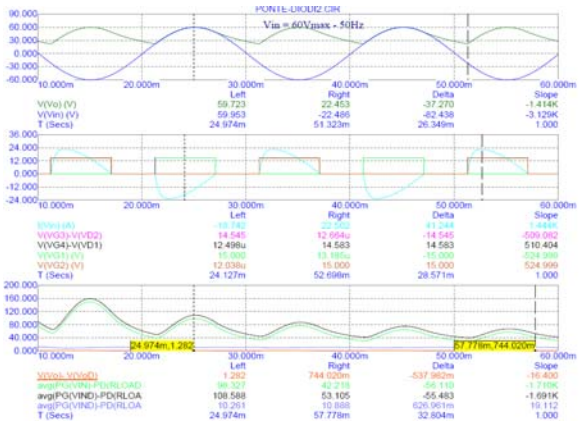

Fig. 7: Rload = 5ohm, Cout= 1000µF
Top: Vin, Vout and Vo
Center: Vg1, Vg2, Vg3 and Vg4
Bottom: Vo-Vo(schottky), Pdiss(active bridge), Pdiss (schottky), Pdiss(active bridge)-Pdiss(schottky)

4.3 IC implementation

In the proposed active-bridge controller of **Fig. 9**, thanks to IR GEN5 technology, the internal stages driving the two high side mosfets Q3 and Q4 can be realized in two separated floating epi-pocket all inside the same IC. The two boostrap diodes can also be integrated to save two external components. The added RC network, that avoids spurious transitions, can be replaced with dedicated blanking time blocks for each driver section, to better optimize the dead time with different FETs at different load requirements. In a further idea, the best IR Fets, bootstrap capacitors and Active Bridge controller IC, can be integrated into one single package, achieving a higher design density and allowing the realization of a simple device. This can then become a direct high-efficient replacement of exiting standard input rectification diode bridges.

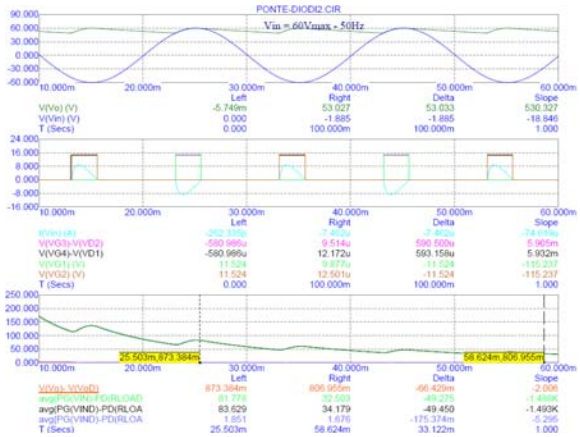

Fig. 8: Rload = 40 ohm, Cout= 1000µF
Top: Vin, Vout and Vo,
Center: Vg1, Vg2, Vg3 and Vg4

Bottom: Vo-Vo(schottky), Pdiss(active bridge), Pdiss (schottky), Pdiss(active bridge)-Pdiss(schottky)

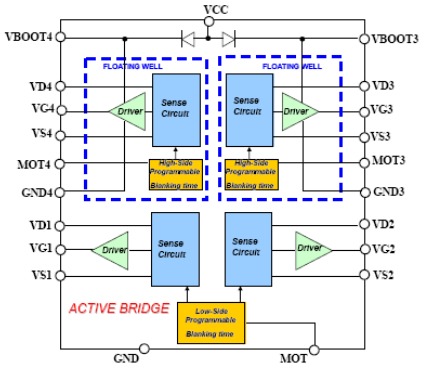

Fig. 9 New Active Bridge controller proposal

5.0 Hardware implementation

The circuit has been realized and tested in our lab. **Fig. 10** shows our first prototype made using four IRAC-D2 daughter cards. In the following some pictures show the actual waveforms both with pure resistive load (such as with a PFC stage) and capacitive load conditions. At the end of the chapter we will show the efficiency and power loss improvements compared with standard schottky-diode bridge solutions.

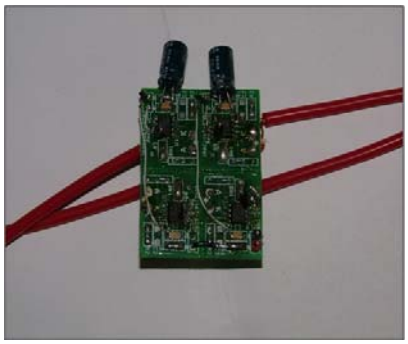

Fig. 10: prototype of Active Bridge

Fig.11-12 show the behavior of the Active Bridge in the case of pure resistive load, and it's interesting to note the effect of spurious transition on both low side (red curve) and high side gate signal (blue curve) without adding any external RC masking network.
These situations are better visible in the **Fig.13-14,** respectively at turn off and turn on transitions of the low side Fet gate.

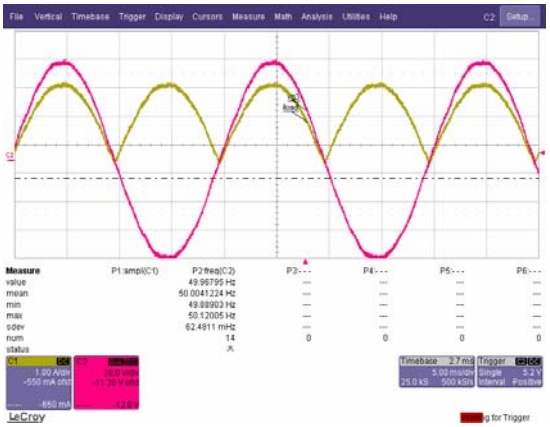

Fig 11: Input voltage and rectified output current with pure resistive load

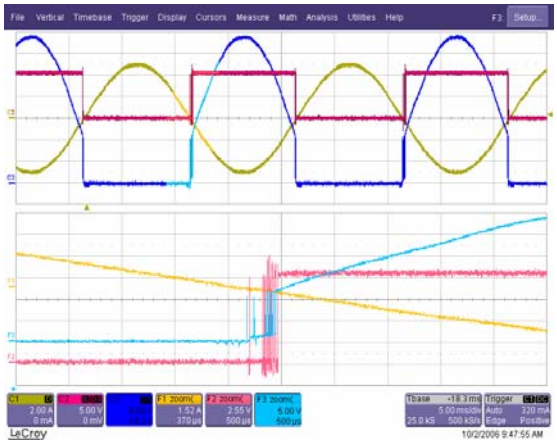

Fig 12: Top: Input current, Low side gate signal(red), High side gate signal(blue) Bottom: Spurious transitions on gate signals

After the IC turns the Fet off, the spurious transitions occur within 90us and it's easy to see that the first glitch happens just after 15us, when the internal IR1167's blanking time expires. All the other glitches appear separated by the same delay. At turn on, instead, the FET can't remain on for more than 3us and only after 280us the current level is high enough to avoid oscillations. Thus the minimum on time (MOT) of 3us at turn on and the minimum blanking time of 15us (typ) at turn off, implemented into the IR1167, are not enough to avoid spurious transitions, due to the slow sinusoidal current variation and a longer blanking time circuitry has been added.

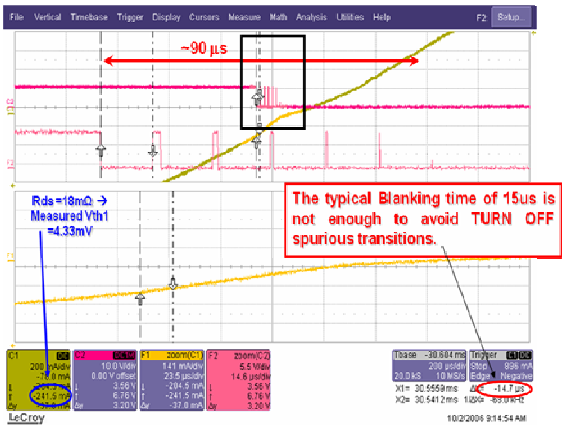

Fig 13: Spurious transitions on low side gate (red) at turn off

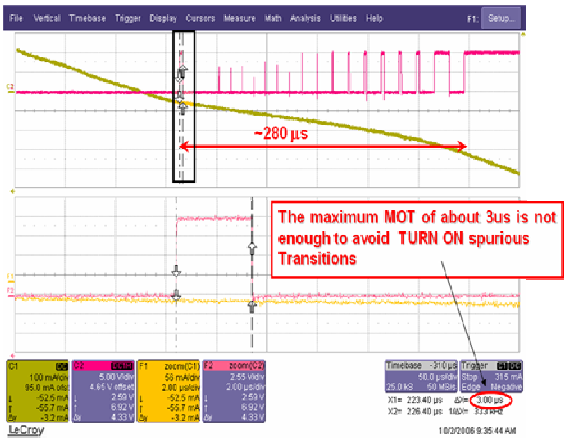

Fig 14: Spurious transition on low side gate (red) at turn on.

The same problem is instead less evident with a standard RC load, since the current variation is steeper. The following **Fig 15-16** show all the gate signals for each FET and the line current, with blanking time network implemented.

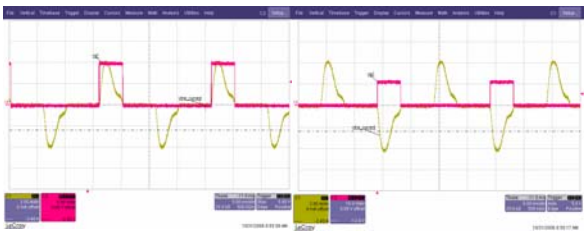

Fig 15: Vg1, Vg2: Gate signal Q1 and Q2 and line current under RC load R=22 ohm C=470uF.

5.1 Efficiency results

To verify the effectiveness of the idea we compared two active bridge designs, at different input voltages of 100V and 40V and different output power, against standard schottky-diode bridge solutions.

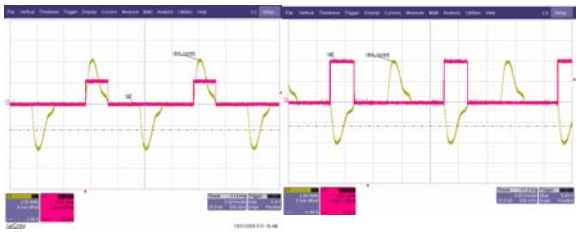

Fig 16: Vg3, Vg4: Gate signal Q3and Q4 and line current under RC load R=22 ohm C=470uF

Fig 17 and **Fig 18** show the results obtained: for the 40V system we used 4x IRF6613 (DirectFet medium Can) compared with 4 x SS34 in SMC package; for the 100V instead we used 4x IRF6644 (DirectFet medium Can) against 4x MBR10H100 in TO263 package.

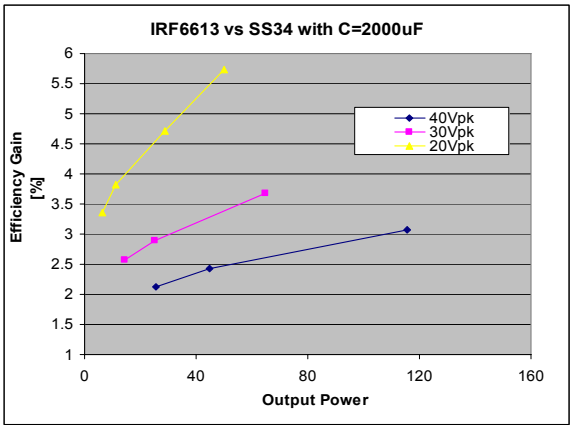

Fig. 17: Efficiency results at low voltage input

In the case of **Fig. 17** the amazing result is the 5.5% gain in efficiency at 20V input and about 50W output, the reason is the higher current flowing into the Fets showing much lower dropout than a diode.

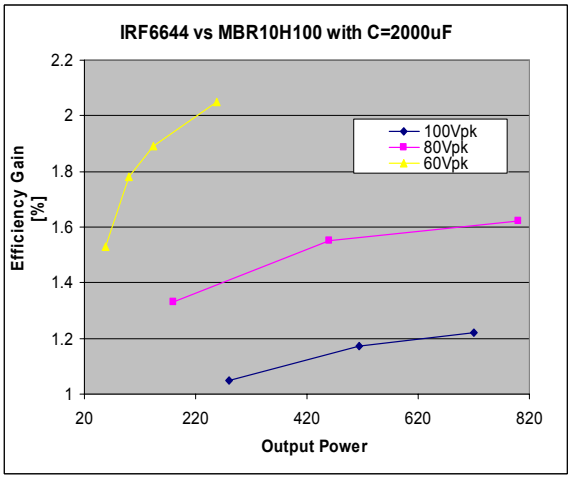

Fig. 18: Efficiency results at medium voltage input

At increasing input voltage and decreasing output current, the efficiency advantage drops to a still good 2% to 3%. The three curves are limited in power to limit the peak current into the devices to an acceptable operating level compared to their rated Id and If. In **Fig. 18** the efficiency gain shows the same trend: at 60V and 250W output the current is much higher and the gain is exciding the 2%; at 100V this efficiency gain drops to about 1.1% - 1.3% depending on the load.

This last case seems to be less appealing in the balance of benefits and cost, we have to remember however that the four IRF6644 are much smaller than the comparing diodes in TO263: each DirectFet is about 80% smaller in area and 95% in volumes than the diodes.

This allows a much smaller solution and higher power density, often eliminating the need of a bulky heat sink.

6 Conclusions

Using SO8 FETs or better DirectFETs in an Input active-bridge configuration (with synchronous rectification control), is the way to increase efficiency and power density whilst reducing or eliminating the need of an heat-sink.

The schematic proposed in **Fig. 3** shows how to make a simple full wave, active bridge input rectifier using available devices in the market and **Fig.9** represents instead the proposed new Active Bridge controller IC.

As shown from graphs, efficiency improvement is quite noticeable and the benefits may be different according to the output power:

a) If the output voltage is high the efficiency increase may not be very important, especially if delivering kW, but then the much lower power dissipation across the bridge allows for smaller and cooler solutions;

b) If the output voltage is low, efficiency becomes the predominant difference, also for low current outputs.

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