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An offset compensation technique for bandgap voltage reference in CMOS technology

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Abstract— **A precision integrated bandgap voltage reference in 0.35µm CMOS technology is here presented. The circuit uses natural npn bipolar transistors as reference diodes. A particular attention was paid to the compensation of the several offsets that could strongly influence the performances of the reference. A very simple sample and hold technique for offset compensation is here presented. The proposed technique is straight forward for all bandgap topologies which use diodes with a terminal connected to the ground node or to the supply node.**

The temperature coefficient (TC) of the generated output voltage is 12.7ppm/°C versus about 245ppm/°C of the same circuit without offset compensation.

A full description and an analytical expression for the proposed compensation technique are given. The results of the most relevant simulations are also reported. The circuit has been inserted in a test chip whose layout is shown.

I. INTRODUCTION

High performance electronic systems require stable and temperature independent voltage and current references for their proper operations. In particular, for mixed-signal interfaces, the possibility to generate these reference voltages on the silicon chip is essential. The most common CMOS voltage reference is a derivation of bipolar bandgap architectures exploiting a parasitic lateral BJT [1, 2]. This topology is called bandgap reference [3, 4] and it is used to provide a voltage output which has minimum dependence on temperature variation. However, common process and supply variations can introduce an error on the generated reference [5]. In particular, some internal offset and the mismatch between BJTs bias currents are recognized as the biggest influence on the precision of output voltage, thus changing both the absolute output value and its curvature versus temperature.

Different types of compensation techniques have been presented up to now [6, 7]. In this paper a topology of bandgap reference which uses a simple technique to cancel the aforementioned effects, based on a sample and hold stage, is presented. The proposed technique was tested on a bandgap circuit designed to realize a voltage reference for an integrated floating power supply [8], exploiting the low voltage signal devices (0.35µm CMOS) available in the used high voltage technology [9]. Anyway, this compensation technique does not depend on the properties of this technology and it can be used in a plain CMOS bandgap reference as well. No external trimming of the residual bandgap curvature has been implemented.

The circuit topology and the equations which describe the basic bandgap behaviour are discussed in Section II, whilst Section III explains all the circuit modifications and the proposed compensation technique. Simulation results obtained in Spectre® environment are shown in section IV.

II. CIRCUIT REALIZATION

In the high voltage technology used to realize the bandgap circuit, a n-epi layer is epitaxialy grown on a p-type substrate and has to be biased at the maximum available voltage in the system (generally the supply voltage). The p-sub must be directly connected to the global ground of the system. Therefore, the only npn bipolar transistor available in this environment has its collector connected to the supply voltage (see Fig. 1, 2). Consequently, the basic topology usable for the bandgap circuit is the one reported in Fig. 2.
In general, it is known that, if two BJTs operate at unequal current densities, the difference between their base-emitter voltages is directly proportional to the absolute temperature. It is also recognized that the base-emitter voltage of BJTs (forward voltage of a pn junction) exhibits a negative temperature coefficient (TC) [10]. In Fig. 2, the area of transistor Q2 is a multiple of the area of Q1 and they are biased by the same current which is regulated by choosing the value of resistors indicated as R. Resistor Rb is used to trim

the curvature of the output voltage (V_{BG}) versus temperature. In fact, V_{BG} can be written as:

$$V_{BG} = V_{BE2} + \Delta V_{BE} \cdot (1 + R/Rb) \quad (1)$$

Therefore, in (1) it is possible to compensate the behaviour of the V_{BE2} versus temperature by a trimming of the coefficient of ΔV_{BE}. The Op-amp in Fig. 2 can be implemented as a simple two stages scheme.

A very relevant problem that usually affects this topology of bandgap reference are the offset between the input terminals of this Op-amp and the offset due to the mismatch between resistors R (see Fig. 2) which causes a mismatch between the bias currents of the reference diodes [11].

It is important to exploit a technique which compensates these offsets, indicated as V_{OFF1} and V_{OFF2} respectively in Fig. 2. Hence, the introduction of additional elements to the circuit appears necessary.

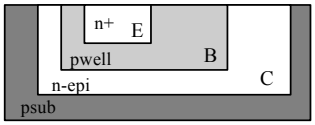

Fig. 1 - Silicon profile of npn bipolar transistor

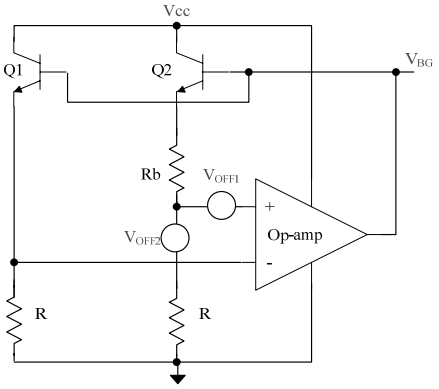

Fig. 2 – Basic structure of bandgap reference available in the used technology

III. Implemented circuit and offset compensation technique

The circuit and the modified Op-amp realized to avoid the problems described in the previous section are reported in Fig. 3a and Fig. 3b respectively. Fig. 4 shows the layout of the test chip. Sample and hold (S&H) block and few switches were introduced in the circuit shown in Fig. 1. The switches are used to change the configuration of the circuit during the phase when offsets are read and stored (indicated as compensation phase in the following) and the phase of normal operation. A clock with three non overlapping phases is needed to drive the switches (see Fig. 5). In the test chip, these signals were generated exploiting standard library blocks and the duration of T was few tens of μs. The value of T is not a critical parameter and it can be chosen in a wide range. Since bandgap references are commonly used in applications such as switched capacitors circuits or ADCs, in which clock signals are already present, these signals can be used and there is no need for any additional block. Signal N is used to select normal operation; signal O is used to select the compensation phase and was split in two parts, O_a and O_b. The critical switches (which both have one of their terminals connected to the capacitors used to store the offset components) were designed trying to minimize charge injection during the turn off: two dummy MOS (with source and drain terminals shorted together) were added to the drain and the source terminals of the n-channel and the p-channel which constitute the transmission-gate, to compensate the injected charge (clock feedthrough compensation).

The S&H, includes a switch followed by a capacitor (C_{HOLD}) and a buffer stage (Opamp2). This block stores the value of V_{BG} evaluated during the normal operation phase and holds it during the compensation phase.

The amplifier Op-amp was modified by introducing an auxiliary input stage, implemented by MOSFETs M1, M2 and M3, and two capacitors with same value, indicated as C1 and C2 (see Opamp1 in Fig. 3.b); all resistors are made of polysilicon. Capacitors C1 and C2 were introduced to store and eliminate the different offset components. Opamp2, used in buffer configuration in S&H block, is a simple two stages scheme. Devices Q1 and Q2 were chosen as a square array of equal elements, providing a matched block during layout phase.

During the compensation phase, the various offset voltages are charged on the capacitor C1 and C2: to understand the necessity to split this phase in two parts, consider the equivalent circuit in Fig. 6a. During this phase, two equal BJTs are used to bias the resistor R with equal currents keeping nodes x_1 and x_2 at the same voltage and to read the offsets V_{OFF1} and V_{OFF2}. Their base terminals are biased by the bandgap value stored by the S&H (V_{BG2}) during the normal operation. The auxiliary input stage and the second gain stage of Opamp1 are in a buffer configuration to store the offset components on C1 and C2. The non inverting input of A_{AUX} is biased by V_{BG2}. Since the used BJTs could be affected by a process mismatch, they could provide different emitter voltage introducing an additional offset indicated as V_{OFF3}. Being this offset component not present during normal operation, it does not have to be stored on the capacitors; therefore, the emitter voltages are swapped when O_a goes low and O_b goes high; consequently V_{OFF3} is stored with opposite sign on the capacitors C1 and C2, while V_{OFF1} and V_{OFF2} are stored with the same sign. Hence, the voltages stored on the capacitors for the offset components are:

$$V_{C2} = (V_{OFF1} + V_{OFF2} - V_{OFF3}) \cdot A_1 \cdot [A_2/(A_2 \cdot A_{AUX})] \quad (2)$$

$$V_{C1} = (V_{OFF1} + V_{OFF2} + V_{OFF3}) \cdot A_1 \cdot [A_2/(A_2 \cdot A_{AUX})] \quad (3)$$

where A_1, A_{AUX} and A_2 represent respectively the gain of the main input stage, the gain of the auxiliary input stage and the one of the second stage of Opamp1. The equivalent circuit during the normal operation is reported in Fig. 6b. The effective bandgap loop is restored; now C1 and C2 are in a parallel configuration: as a result the component due to V_{OFF3} has been cancelled.

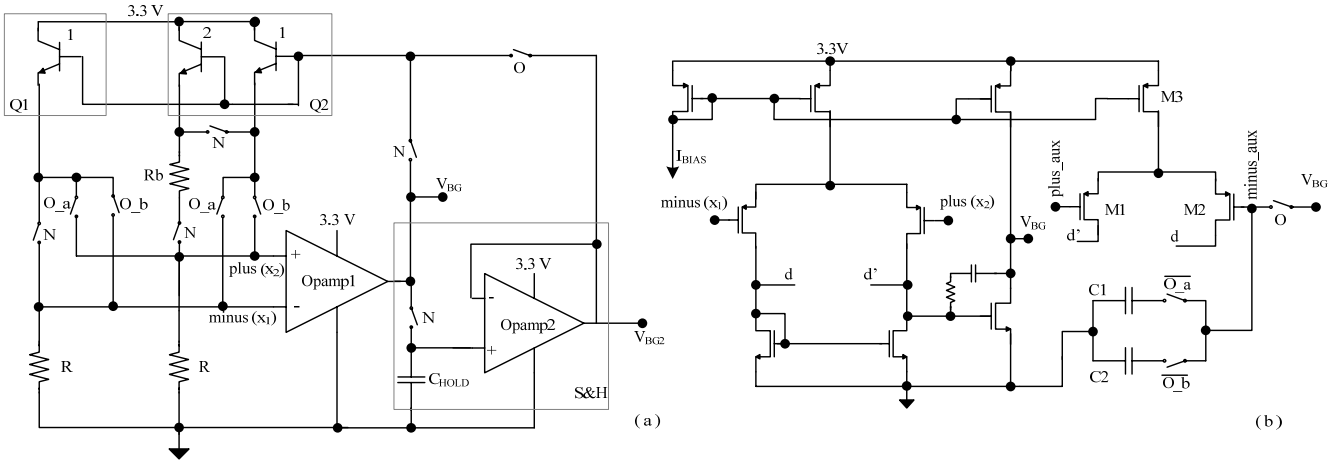

Fig. 3 – (a) Proposed topology of bandgap reference including S&H and switches; (b) Opamp1: modified Op-amp with auxiliary input stage

Therefore, on the inverting input of A_{AUX} there is a voltage:

$$V_C = (V_{OFF1} + V_{OFF2}) \cdot A_1 / A_{AUX} . \qquad (4)$$

Then, the theoretical residual offset on V_{BG} after the compensation phase is:

$$(V_{OFF1} + V_{OFF2}) \cdot (A_1 \cdot A_2) - V_C \cdot (A_2 \cdot A_{AUX}) = 0. \qquad (5)$$

In this way the considered offsets components that could influence the characteristics of V_{BG} have been eliminated. Some problems could occur if there is a mismatch between C1 and C2. Given ΔC as the difference between the values of the capacitors, with simple math operations it is possible to work out that the introduced error is proportional to the ratio $\Delta C/2C$ and it is consequently negligible. In fact, a good matching between the capacitor in layout phase and the insertion of dummy elements could minimize the problem. (the error could be about 0,1%). The input offset for Opamp2 was not compensated in this release of the circuit: however, it does not influence the curvature of the generated reference, but it only could impose a shift of few millivolt between V_{BG} and its replica V_{BG2}. It will be taken in consideration in a future version of the circuit.

IV. Simulations Results

The most relevant simulation in Spectre® environment was the analysis of the bandgap output voltage versus the operating temperature. The analysis was also performed while introducing both an offset between the input terminal of Opamp1 through an ideal voltage source and a mismatch between the value of R resistors. The added offset values fell in the interval $10mV \leq V_{OFF1} \leq 10mV$, while the maximum mismatch between resistors R (whose nominal value was 110kΩ) was 5%. Curves for these simulations are reported in Fig. 7. The precision of V_{BG} is 12.7ppm/°C. The spread for the corner curves (which includes the effect of the offsets, the variation of MOSFETs, resistors and capacitor models and the variation of the supply voltage) is negligible. The residual offset value between node x_1 and x_2 is reduced to 30μV (see Fig. 8).

In the same circuit without offset compensation, the precision of the reference was about 245ppm/°C and the deviation of the corner curves from the ideal one was about 16%.

The residual curvature is due to the characteristic of polysilicon resistor versus temperature. A start-up circuit was necessary to pre-charge the capacitor C_{HOLD} at the circuit turn-on: a simple voltage divider brought the capacitor to a voltage near to 1.2V allowing the first compensation phase to work correctly. After the first cycle the start-up circuit was disconnected.

The total power consumption was about 150μW: the current required by the S&H buffer stage increased the power consumption of the circuit by about 15%.

However, without the introduction of any offset compensation technique, a way to reduce the offset of the Opamp1 is to size the input MOS significantly larger than in the present case: but in this way area consumption limitation come into play, and it is impossible to achieve an offset <<1mV.

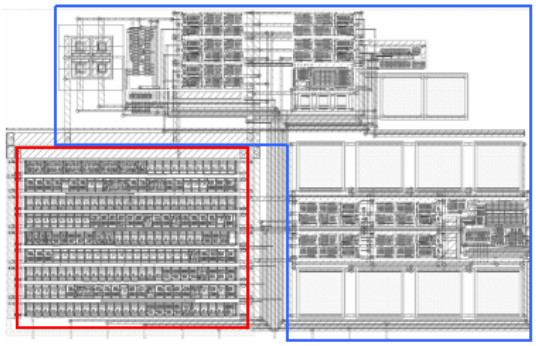

Fig. 4 - Layout cell of test chip: bandgap circuit (blue) and clocks generator block (red)

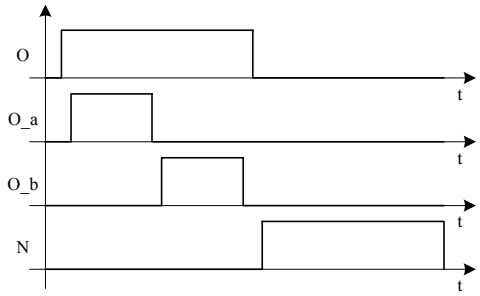

Fig. 5 – Timing signal: O: compensation phase; N: normal operation phase; O_a and O_b: select the two parts in which the compensation phase is divided

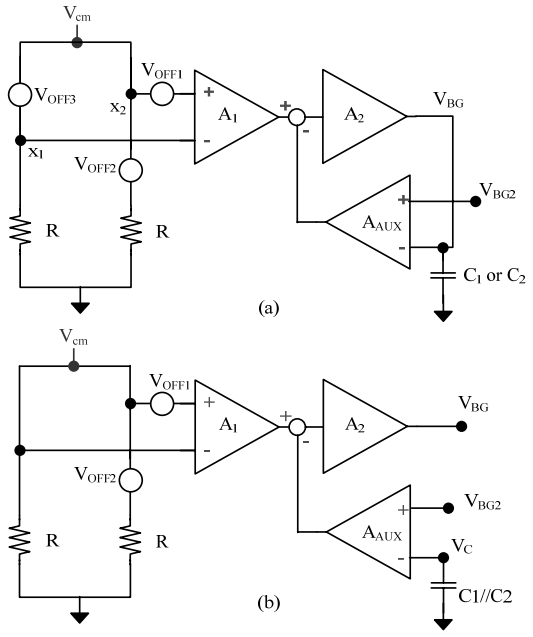

Fig. 6 – (a) Equivalent circuit for compensation phase. (b) Equivalent circuit for normal operation phase

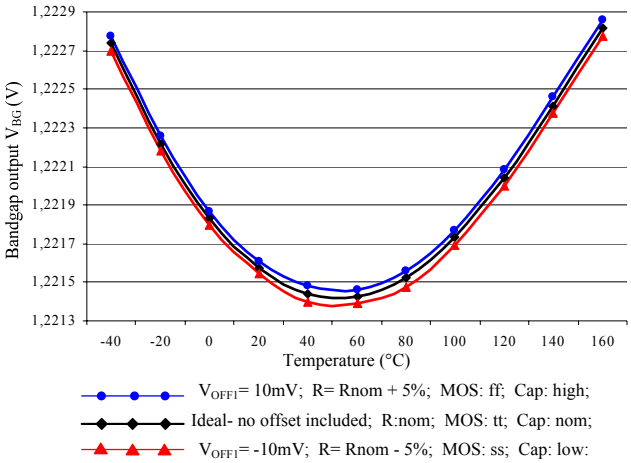

Fig. 7 – Behavior of V_{BG} and corner cases versus temperature

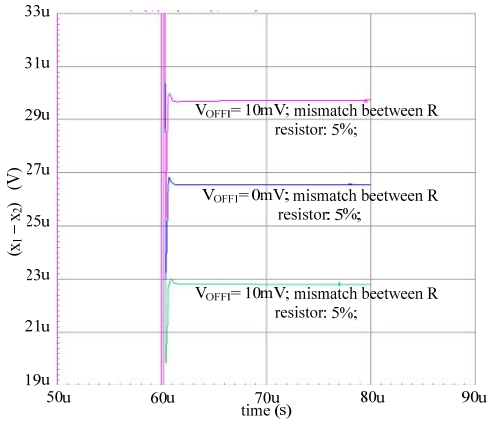

Fig. 8 – Residual offset between Opamp1 inputs after compensation phase

V. Conclusion

A topology of CMOS bandgap reference has been presented. A sample and hold technique to compensate errors due to Op-amp input offset and mismatches between bias current has been analytically explained. The generated output voltage shows a TC of 12.7 ppm/°C. This result could be further improved by trimming Rb and consequently reducing the residual curvature of the bandgap output. However, the obtained result has a good balance between performance and complexity for a large number of applications.

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