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Evaluation of Power MOSFET Thermal Solutions for Desktop and Mobile Processor Power

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as presented at PCIM China, March 2002

Abstract

This paper surveys the thermal performance capabilities of various power semiconductor package types available to the designer of surface mounted motherboard and/or mobile processor power systems. The packages studied are mostly variants of the "SO-8 type footprint" and include standard SO-8, several "improved thermal" SO-8 types, D-Pak and D2Pak footprint packages and the DirectFET™ MOSFET. Steady state thermal Resistance is measured and the effects of heatsinking, PCB layout/area, and airflow are all considered. It is seen that the DirectFET™ MOSFET packaging technology allows for dramatically cooler operation or much higher output power in a given footprint, especially when two sided cooling is allowed.

Introduction

The desktop or mobile computer system designer is challenged today to provide appropriate power to latest microprocessors. With each successive generation operating frequency, performance, and integration level have gone up, increasing power dissipation. At the same time operating voltage has gone down thus driving up the current needed for given power level. As performance/frequency have increased, the required slew rates go up[1]. At the power switch packaging level, these demands add up to requirements of higher power dissipation and lower parasitics.

Power Packaging Solutions

Historically, traditional SOIC packages such as SO-8 (see figure 1) have been adapted to power semiconductor use in microprocessor voltage regulation. As one might expect from a package not designed to the purpose, serious performance limitations result. Standard construction SO-8 thermal performance is limited by heat dissipation through the leads and onto the PCB[2]. Stray package resistance and inductance likewise suffer from the wirebond and lead construction.

Figure 1: SO-8

More recently several “improved thermal” variants of SO-8 have been introduced by multiple suppliers. These packages include Copper strap SO-8[3] (see figures 2-3) wherein the lead and wirebond construction are replaced by a solder and Copper strap assembly (reduces Rds-on and improves thermal resistance), and MLP or “leadless SO-8” types (new JEDEC MO220 designation, see figure 4) which have exposed Cu die mounting pad (reduces Rth) and Cu lead pads molded into the epoxy body coplanar with the die mounting pad. Yet another package option is the D-pak (see figure 5).

Compared to SO-8 types, and thanks to a Silicon die to Copper tab to PCB design, both D-Pak and MLP/Leadless thermal resistance junction to case/lead is improved. But as with SO-8, wirebond and lead construction still results in higher than desired package stray resistance.

For all types so far mentioned, Power dissipation is limited by the ability to dissipate heat from the Silicon junction through packaging material to the PCB and then from the PCB to ambient. For the most thermally efficient packages listed, the D-Pak and MLP, the Rth contribution from Junction through packaging materials is quite low but the power dissipation is still very constrained by R_{TH} between lead to PCB to ambient. It is clear that if further power is to be dissipated from the same form factor, then it must seek another path.

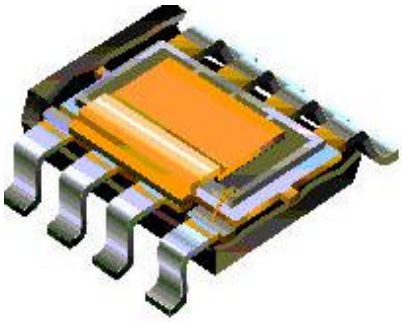

Fig.2 – ***CopperStrap***™ with mold cut-away

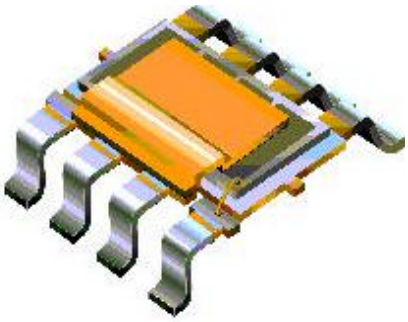

Fig.3 – ***CopperStrap***™ without mold

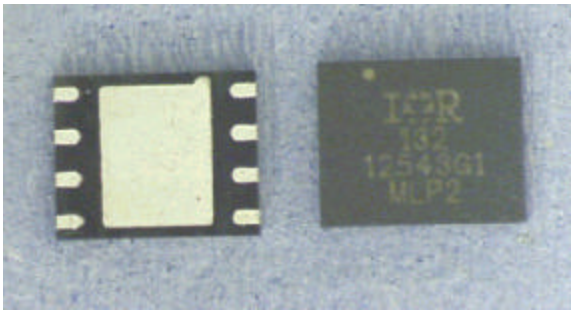

Figure 4: MLP1 and MLP2 "leadless" SO-8 packages have 5 x 6 mm footprint, same as SO-8. At right is the top view and at left the bottom showing the central die mounting "pad" that is directly soldered to the PCB resulting in thermal improvement compared to standard SO-8 package.

Enter the DirectFET™ MOSFET from International Rectifier[4]. This new package has the silicon source and gate directly mounted to the PCB. A protective metal "lid" covers the drain and acts as contact to the PCB (see figure 6). Package stray resistance is kept to an absolute bare minimum: the source is directly bonded to the PCB and the drain attachment through the "lid" has much larger area and lower resistance than occurs for paddle and lead assemblies. Most importantly, with no mould compound to act as a thermal barrier (as occurs for all the other packages considered) heat can be efficiently sunk directly from the drain "lid" . This additional pathway results in breakthrough thermal performance as will shortly be seen.

Methodology

All packages were tested for thermal performance with thermal resistance junction to drain lead (R_{TH}J-Drain lead) and junction to ambient (R_{TH} J-A) measured for two different PCB patterns with traditional "one sided" cooling only. A select group were then tested for several techniques of "two sided" cooling and for effects of airflow.

Fig 5: D-Pak

Herein is described the device mounting and heatsinking used and the test methods employed to measure Thermal Resistance of the various packages.

Standard printed circuit boards were developed to which devices were solder-mounted for measuring thermal resistance. FR-4 material with 2 oz. Cu was used. Board dimension were 4.75 inches by 4.5 inches and backside of board had full metal pattern. Two different PCB metallization patterns were tested: one with 1 inch of Cu area and one with Cu trace minimized so as to cover only as much area as taken up by the Device Under Test (DUT) and necessary lead mounting pads (described as "modified minimum pattern", see figure 7).

Thermal Resistance was measured according to industry practice[5] by first performing a reference temperature estimate; a temperature sensitive

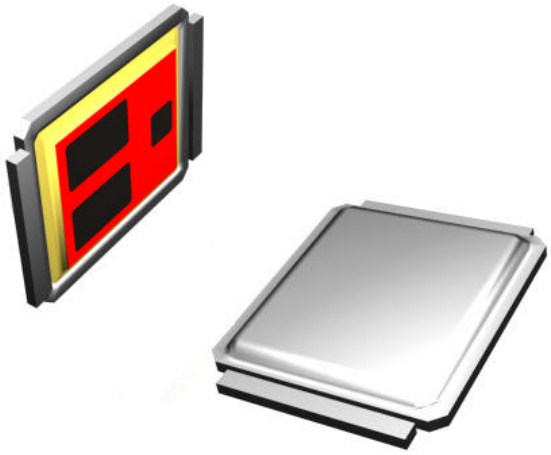

Figure 6: DirectFET™ MOSFET on end (left) and "face down" (right) views. One small gate pad and two source pads are visible; drain contact is made from the "lid" which mounts to the PCB via downset edge contact.

electrical parameter (TSEP) such as Vsd is measured and compared with a calibration value to determine Tj. Then a heating pulse of known power is applied followed by a second TSEP measurement. That measurement was compared to a calibration table to estimate junction temperature and calculate the temperature rise due to the heating pulse. From the familiar equation[2]:

$$\Delta T = R_{TH} \times P_D \qquad \text{(equation 1)}$$

and where:

ΔT = Temperature difference (C) between junction and reference (here either ambient or package lead) ,

R_{TH} = Thermal Resistance (C/W) between junction and reference point (again either ambient or package lead),

P_D = Power dissipated (W)

We can calculate the thermal resistance by plugging in the measured values of temperature rise and Power.

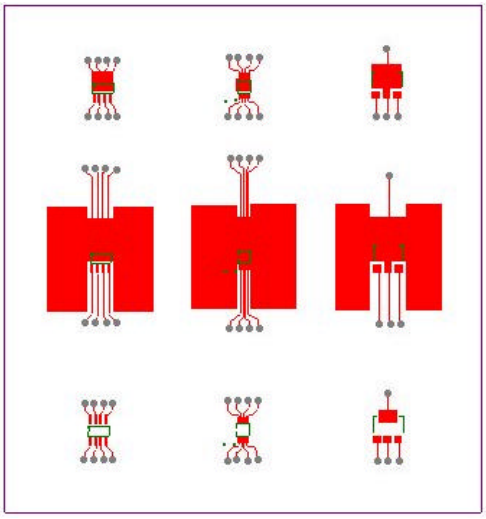

Figure 7: typical test PCB. Patterns in middle row are 1" Cu (for three different packages), Top patterns are the modified minimum Cu area (again for three different packages) and take up only enough area to mount the part. Cu is patterned directly under the device to enhance heat dissipation.

In this way measurements were taken on representative samples of Standard SO-8, Copperstrap SO-8, MLP/Leadless (same area or "footprint" as standard SO-8), D-Pak , D^2-Pak and DirectFET™ MOSFET.

In a second set of measurements, for standard SO-8, MLP and DirectFET™ MOSFET, thermal resistance measurements were taken with double-sided cooling. For these measurements the parts were mounted to the test board on the "modified minimum" patterns (eg: top row of patterns in figure 7) then put in contact with a heat sink attached to the package "top". Commercially available[6] thermally conductive and electrically insulating "gap" filler pads or Powersite[6] were used between DUT and heatsink. Figure 8 shows a cross sectional representation of the DirectFET™ MOSFET mounted to a PCB with a (thin) gap filler and heat sink attached.

Additionally, the measurements were taken with the test boards situated in a wind tunnel. Measurements were taken with airflow between 0 and 750 feet/minute; sensitivity of thermal resistance to cooling airflow is seen.

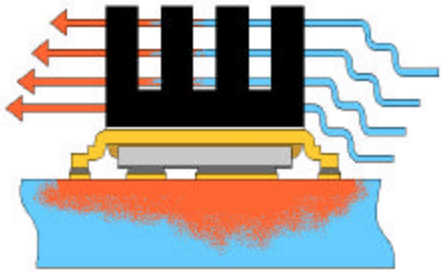

Figure 8 DirectFET™ MOSFET mounted to a PCB with a (thin) gap filler and heat sink attached. Arrows represent airflow for additional cooling

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Results

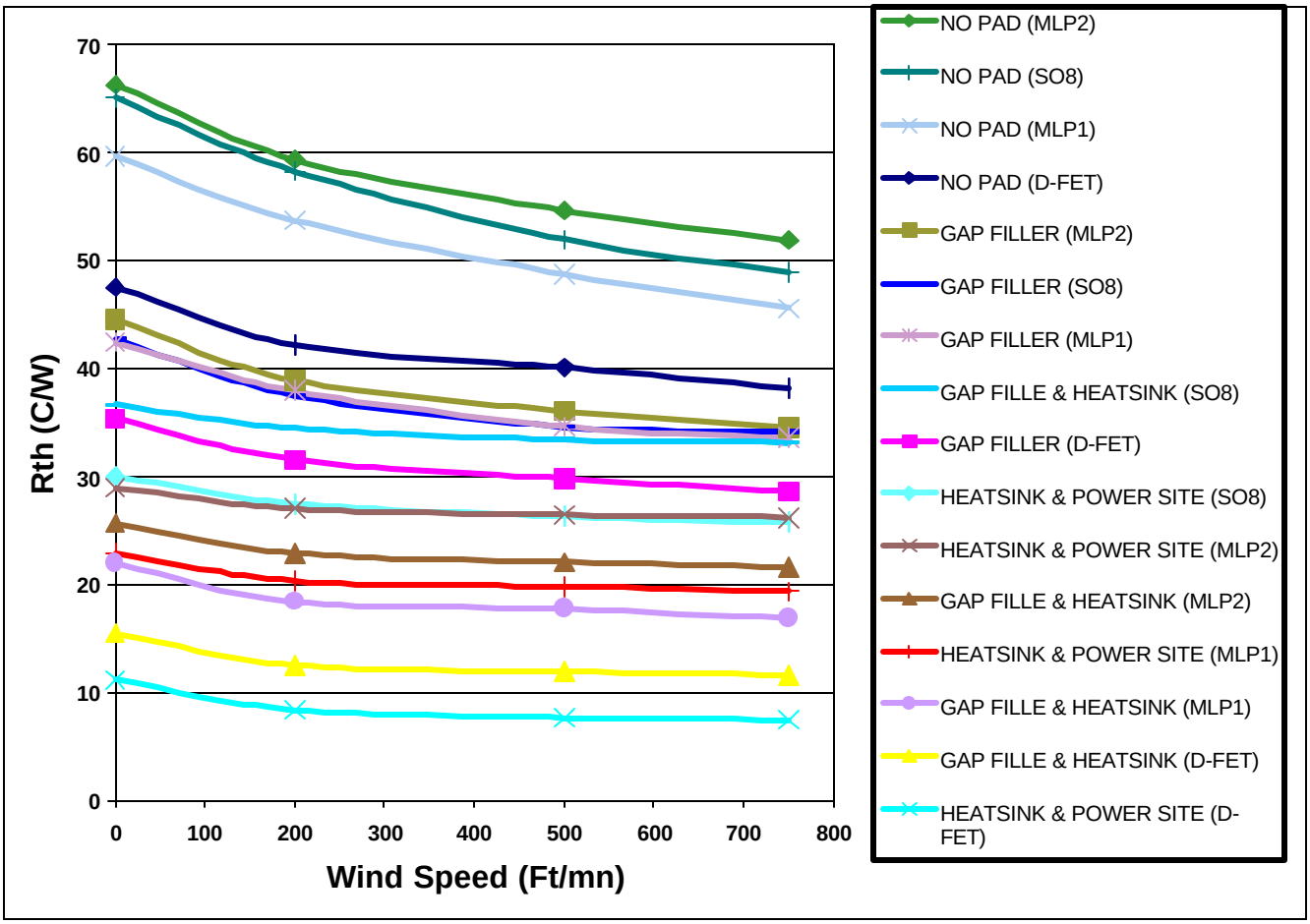
Thermal Performance of Various Power SMT Packages

		1" square Cu area on PCB		Modified Minimum Cu Area	
Package Type	Test Device ID	Average R_{TH}J-A (C/W)	Average R_{TH}J-Drain lead (C/W)	Average R_{TH}J-A (C/W)	PCB Footprint Area ($mm.^2$)
SO-8 (Standard)	IRF7467	33.5	10.6	66.3	35
SO-8 (Copper Strap)	--	30	9*	62	35
D-Pak	IRFR3706	20.2	N/A	42	49
D2-Pak	IRF3706S	18	N/A	33.6	122
MLP-1	--	26.4	N/A	59.3	35
MLP-2	--	28.6	N/A	66	35
DirectFET™ MOSFET	--	31.1	N/A	46.6	45

*= Compared to standard SO-8, Copper Strap has much lower RTH J-Source lead, but RTH J-Drain values are comparable, N/A = Not applicable

Table 1

Table 1 reports the Rth values measured for one sided cooling on all packages tested. Note that R_{TH} J-x represents thermal resistance between Junction and "x" reference point where x can be either A for Ambient air temperature or Drain Lead where the reference measurements are taken on the package drain lead. See again figure 7 for description of different PCB patterns tested.
Note in table 1 that when PCB area is the same (ie: 1" square) differences in package thermal resistance are seen, but since the one sided cooling through the PCB is common to all and dominates Rth, the overall range is relatively narrow. Specifically, Max/min= 33.5/18, or <2 even though package area varies by a factor of 122/35, or almost 4. D2-Pak performs best followed by D-Pak and so on as the package area decreases. For 1" pattern and one sided cooling DirectFET™ MOSFET, MLP/Leadless and Standard SO-8 have relatively comparable R_{TH}JA since the pattern and package areas are similar. For Modified minimum pattern, R_{TH}JA follows the PCB footprint directly. This case is more realistic than the 1" pattern and the data shows how clearly that (for one sided cooling) R_{TH}JA depends on package footprint/PCB trace area.



Graph 1: RTHJA for SO-8, MLP and DirectFET™ MOSFET (designated as D-FET) with and without gap filler/Powersite, heatsink and airflow.

Graph 1 shows data for the second set of measurements which includes single and double sided cooling, with and without airflow. There is an extremely wide performance gap between the various packages. At one extreme (low performance) is standard SO-8, single sided cooling with $R_{TH}JA$ at 66 °C/W improving with 750 ft/minute airflow to just below 50 °C/W (for a reduction of approximately 26%). At the other, highest performance extreme is the DirectFET™ MOSFET with double sided cooling which has $R_{TH}JA$ of 11 C/W with zero airflow improving to 8 C/W at 750 ft./minute of flow. The DirectFET™ MOSFET with double sided cooling thus represents a dramatic 6 fold improvement over standard SO-8 solution. The closest performance to DirectFET™ MOSFET is the MLP1 "leadless" SO-8 with double sided cooling. Here, even though the footprints are close, DirectFET™ MOSFET performance is still a dramatic 50% better, by the difference between 22 °C/W and 11 °C/W.

Conclusions

Thermal performance was measured for several power SMD packages suitable for processor power application. Effects of PCB pattern and size, package size, and air flow were examined. Specifically, two sided cooling was examined and large performance differences were seen favoring a new package, the DirectFET™ MOSFET which is application optimized. Due to close thermal contact of drain with no intermediate, poor thermal conductance mould compound, the DirectFET™ MOSFET thermal resistance is 50% less than the closest competitor when double sided cooling is used.

References

[1] "Device Requirements for Low Voltage, Fast Transient Response Regulators Used to Power Future Microprocessors and other Low Voltage Logic Chips", Edward Stanford, HFPC2001 Procedings, pp 1-10,
[2] "Maximizing the Effectiveness of Your SMD Assemblies", Application Note AN-994, International Rectifier Corporation, www.irf.com
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[4] Sawle, Andrew; Standing, Martin; Sammon, Tim; Woodworth, Arthur, International Rectifier "DirectFET™ - A Proprietary New Source Mounted Power Package for Board Mounted Power", PCIM Europe Proceedings, June 2001.
[5] JEDEC, "THERMAL IMPEDANCE MEASUREMENTS FOR VERTICAL POWER MOSFETS (DELTA SOURCE-DRAIN VOLTAGE METHOD)" ,JESD24-3, November 1990
[6] See Parker Chomerics material at www.chomerics.com for example