TC1766

Highly Integrated 32-bit TriCore™-based Next Generation Microcontroller for Automotive Applications

The TC1766 - member of the AUDO-NG family - is optimized for highly demanding applications where embedded real-time performance and DSP capabilities combined with an extremely fast interrupt response time and highest level of fault tolerance are needed. AUDO-NG is based on the award-winning unified 32-bit TriCore™ architecture combining RISC, CISC and DSP functionality in a single chip. New innovative peripherals like the Micro Second bus, fast analog-to-digital converter unit or the Micro Link Interface as well as the advanced triple layer structure boosting the overall system performance turns the TC1766 into the most cost effective 32-bit microcontroller for high demanding applications of the automotive and industrial market.

Applications
- Automotive engine and transmission control
- Automotive by-wire systems
- Industrial robotic control

Features
- High performance 32-bit super-scalar TriCore™ V1.3 CPU with 4 stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Single precision floating point unit (FPU)
  - 80 MHz at full automotive temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
- Memories
  - 1.5 MByte embedded program flash with ECC
  - 32 KByte data flash for scalable EEPROM emulation
  - 76 KByte on-chip SRAM
  - 8 KByte instruction cache
  - 16 KByte Code Scratchpad Memory
- 8-channel DMA controller
- Sophisticated interrupt system with 2 x 255 hardware priority arbitration levels serviced by CPU and PCP2
- High performing triple bus structure
  - 64-bit local memory buses to internal flash and data memory
  - 32-bit system peripheral bus for interconnections of on-chip peripherals and further functional units
  - 32-bit remote peripheral bus serving the requirements of high speed peripherals
- One Micro Second bus interface (MSC) for port expansion to external Power ASIC's

- One general purpose timer array module with a digital signal filtering and timer functionality to realize autonomous and complex I/O management (GPTA4)
- Two asynchronous/synchronous serial channels with baud rate generator, parity, framing and overrun error detection (ASC)
- Two high speed synchronous serial channels with programmable data length and shift direction (SSC)
- Two high-speed Micro Link Interfaces for serial inter-processor communication (MLI)
- MultiCAN module with two CAN nodes and 64 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer
- 2-channel fast analog-to-digital converter unit (FADC) with concatenated comb filters for hardware data reduction; 10-bit resolution/min. conversion time 280 ns
- One 32-channel analog-to-digital converter unit (ADC) with 8-bit, 10-bit or 12-bit resolution
- 36 analog input lines for ADC and FADC
- 81 digital general purpose I/O lines
- Digital I/O ports with 3.3 V capability
- On-chip debug support OCDS level 1 + 2 (CPU, PCP, DMA)
- Dedicated emulation device chip for multicore debugging, tracing and calibration via USB 1.1 interface
- Power management system
- Clock generation unit with PLL
- Supply Voltage 1.5 V
- I/O Voltage 3.3 V
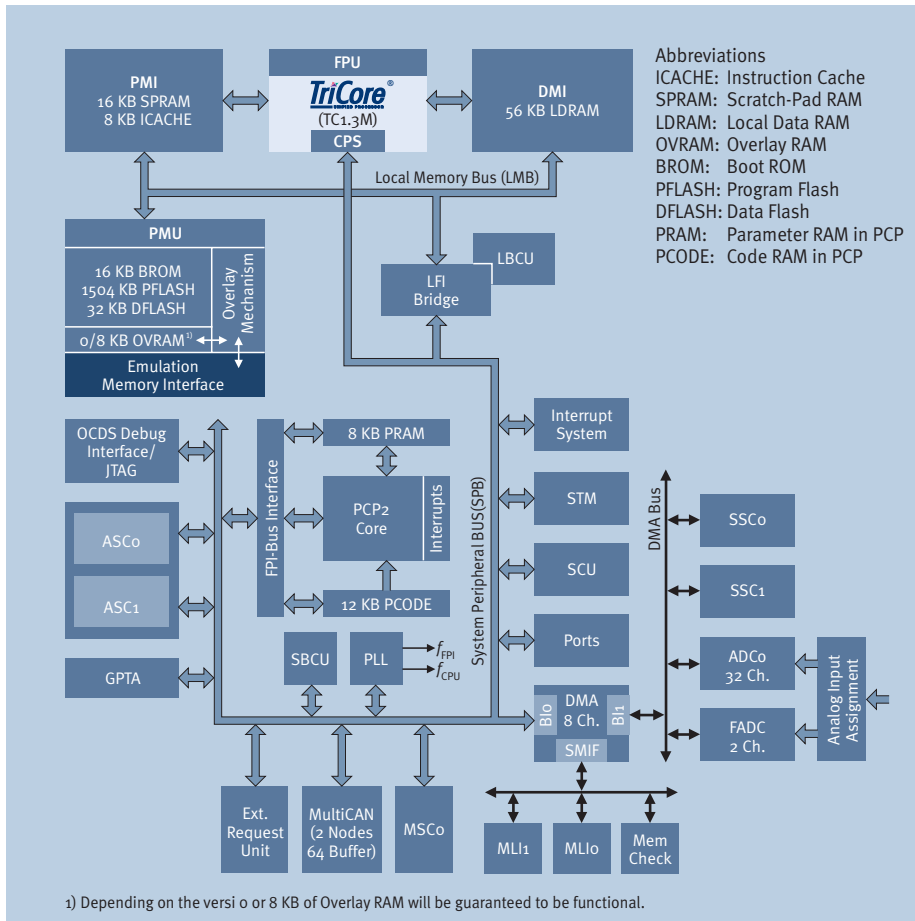- Full automotive temperature range -40 to +125°C
- LQFP-176 package

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Never stop thinking.

TC1766 Block Diagram

Abbreviations
ICACHE: Instruction Cache
SPRAM: Scratch-Pad RAM
LDRAM: Local Data RAM
OVRAM: Overlay RAM
BROM: Boot ROM
PFLASH: Program Flash
DFLASH: Data Flash
PRAM: Parameter RAM in PCP
PCODE: Code RAM in PCP

PMI — 16 KB SPRAM, 8 KB ICACHE
FPU — TriCore® (TC1.3M) — CPS
DMI — 56 KB LDRAM
Local Memory Bus (LMB)
PMU — 16 KB BROM, 1504 KB PFLASH, 32 KB DFLASH — Overlay Mechanism — 0/8 KB OVRAM[1] — Emulation Memory Interface
LBCU
LFI Bridge
OCDS Debug Interface/JTAG
FPI-Bus Interface
8 KB PRAM
PCP2 Core — Interrupts
12 KB PCODE
System Peripheral BUS(SPB)
Interrupt System
STM
SCU
Ports
ASC0
ASC1
SBCU
PLL — f_{FPI}, f_{CPU}
GPTA
DMA 8 Ch. — Bl0, Bl1 — SMIF
Ext. Request Unit
MultiCAN (2 Nodes 64 Buffer)
MSC0
MLI1
MLI0
Mem Check
DMA Bus
SSC0
SSC1
ADC0 32 Ch.
FADC 2 Ch.
Analog Input Assignment

1) Depending on the versi 0 or 8 KB of Overlay RAM will be guaranteed to be functional.

TC1766
The most cost effective Solution for Engine and Transmission Control

Diesel & Gasoline Engine Control
- Reduced emission levels
- Better engine behavior
- Less fuel consumption

Automated Transmission Control
- Better acceleration
- More comfort
- Less fuel consumption

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