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# System Accuracy Analysis of the Multiphase Voltage Regulator Module

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***Abstract*-The paper analyzes the system accuracy of the multiphase voltage regulator module (VRM), and identifies the influential factors contributing to the system errors. PSpice Monte Carlo analysis, a more realistic statistical method of system accuracy prediction, is used to simulate the load line of the multiphase voltage regulator module for the next generation microprocessors. The Monte Carlo simulation result is compared with a worst-case analysis, a root-sum-square method, and is verified by the experimental results of a three phase synchronous buck converter.**

***Keywords – VRM; load line; Monte Carlo simulation, multiphase converter***

## I. INTRODUCTION

Intel Pentium 4 microprocessors require the voltages between 1.5V and 1.75V with the tolerances for the entire load range (up to 70A) being limited within a band of +/- 25mV [1]. Next generation microprocessors have even tougher load line requirements; lower voltage and higher current along with smaller output impedance [2] imposes serious challenges to the system design of the voltage regulator module (VRM). Adaptive voltage positioning is required to lower the power loss of the microprocessor at heavy load and to reduce the voltage deviation during dynamic load conditions. The factors contributing to the load line errors include the Digital to Analog Converter (DAC) voltage accuracy, the blocks in the voltage control loop, e.g. error amplifier input offset, no load set point accuracy, and adaptive voltage positioning (AVP). Because of AVP, the blocks in the current loop also affect load line accuracy. The AVP output is proportional to the load current, therefore the accuracy of the current sensing circuits and current amplifiers is very important.

The load line equations are derived in this paper for a three phase voltage regulator module with average current sharing and used in the root-sum-square and worst-case analysis of the load line error. The worst-case analysis method is useful in bounding the error, but cannot give accurate prediction of a real design.

Monte Carlo analysis is a statistical method, and is used in this paper to simulate the load line error. The device and lot tolerances are specified in PSpice for the integrated circuits and discrete devices contributing to the error. During a Monte Carlo simulation, PSpice randomly varies all device model parameter values with respect to the tolerances and distribution specified, and runs a simulation for each value. This statistical result is more realistic than the worst-case and root-sum-square calculations and provides a more accurate prediction of the system output voltage.

## II. SYSTEM ERROR ANALYSIS

Fig. 1 shows a system that has been developed to provide a highly accurate load line for the next generation microprocessors. The control IC IR3080 [3] consists of DAC, error amplifier, droop buffer and reference current source, while the phase IC IR3085 [4] includes the current sense amplifier and current sharing circuitry.

DAC accuracy is the most influencing factor in the entire system, and must be trimmed to meet the load line specification. If the trim is performed at the output of the error amplifier, the input offset voltage $V_{EAOS}$ is reduced. The no load set point voltage error is a result of the external resistor $R_{FB}$ accuracy and the internal current source accuracy which is generated and mirrored from the oscillator current source $V_{OSC}/R_{OSC}$.

The load current information also affects the output voltage since adaptive voltage positioning effectively decreases the converter's output voltage as load is applied. The gain and offset of the current sense amplifiers should be considered along with the offset of the droop amplifier. Current sensing error is also an important contributing factor and the accuracy depends on the current sensing method used. Current sense power resistor, top or bottom MOSFET $R_{DS}(on)$, and inductor DC resistance are the popular current sensing methods commonly used in the multiphase voltage regulator modules. Because inductor current sensing is a loss-less, low-cost method of providing reasonably accurate real-time current information [5], it is selected for this solution.

As shown in Fig. 1, the inductor current sensing method utilizes the DC resistance component ($R_L$) of the inductor L. A low power resistor $R_{CS}$ and a small capacitor $C_{CS}$ placed across the inductor are used to retrieve the inductor

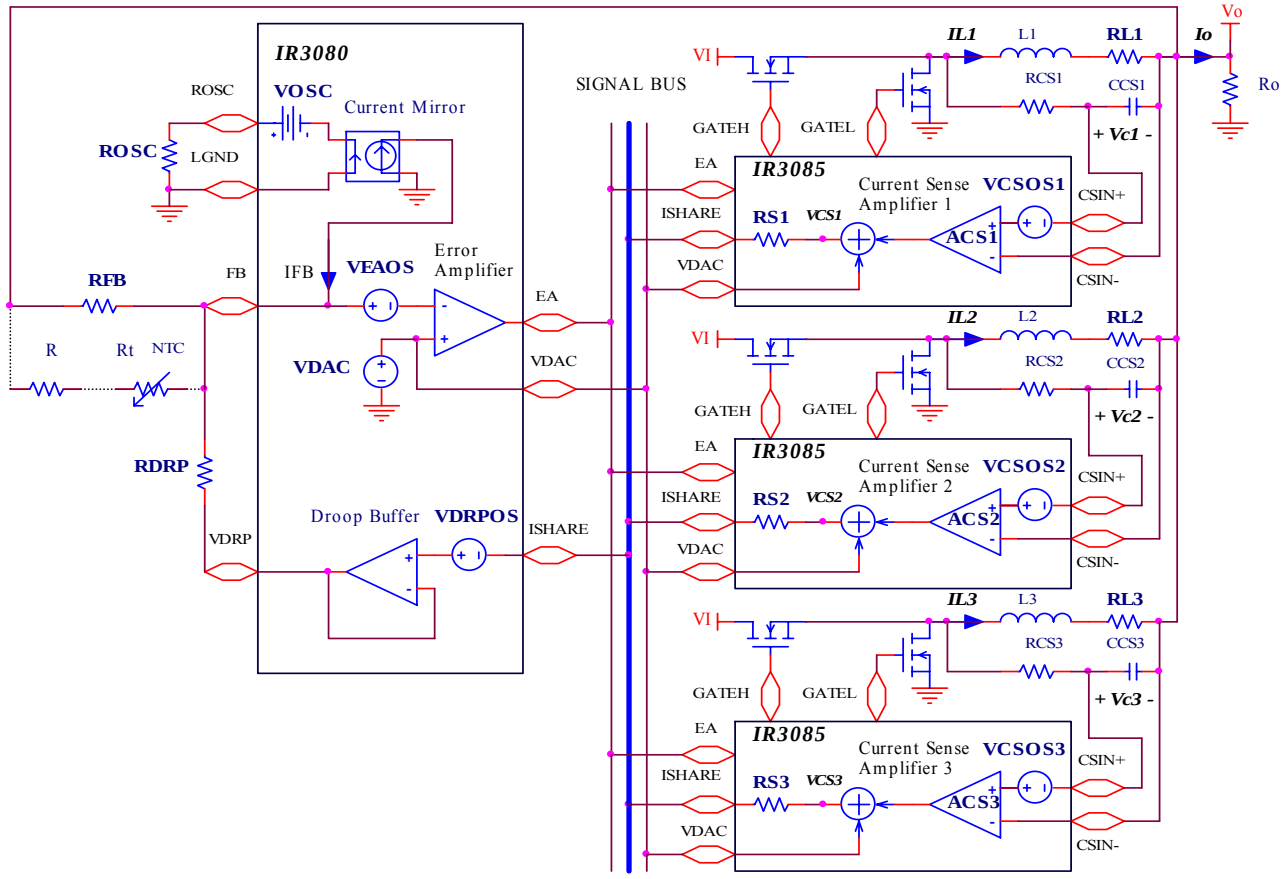



Fig.1 The blocks contributing to the load line error

current information by reproducing the voltage drop $I_L$*$R_L$ across $C_{CS}$. The voltage across $C_{CS}$ is a function of the inductor current $I_L$, as shown in (1). The variations of the inductance L and its inherent DC resistance $R_L$, as well as $R_{CS}$ and $C_{CS}$ accuracy affect the ripple (AC) component of the inductor current waveform. However, the inductor average current (DC) component error comes solely from $R_L$ variations [5].

$$\frac{v_C(s)}{I_L(s)} = R_L \frac{1 + s\,L/R_L}{1 + sR_{CS}C_{CS}} \qquad (1)$$

The output of the three current sense amplifiers are averaged through the resistors $R_{S1}$-$R_{S3}$ and buffered by the droop amplifier before being connected to the error amplifier input FB through resistor $R_{DRP}$. The ripple of the current signal does not affect the accuracy of the output voltage Vo, because the crossover frequency of the voltage loop is much lower than the current signal frequency, which is the product of the switching frequency and the number of phases. Therefore, only $R_L$ is considered in the steady-state load line analysis. If the load line during transients needs to be calculated, the additional variation in L, $R_{CS}$ and $C_{CS}$ should be considered.

The parameters in bold letters in Fig. 1 contribute to the load line errors. For a single phase converter, the relationship of the output voltage Vo with the contributing parameters is derived in (2), where the first term represents the DAC voltage setting, the second term is the no-load offset voltage, and the third term is the adaptive voltage positioning.

$$V_O = V_{DAC} - \frac{V_{OSC}}{R_{OSC}} R_{FB} - \frac{R_{FB}}{R_{DRP}}\left[(I_L R_L + V_{CSOS})A_{CS} + V_{DRPOS}\right] \qquad (2)$$

In a three phase synchronous buck converter, the current sharing loop ensures that the output voltages of the current sense amplifiers $V_{CS1}$ to $V_{CS3}$ are the same, i.e.

$$V_{CS1} = (I_{L1}R_{L1} + V_{CSOS1})A_{CS1} + V_{DAC} = V_{CS2} = (I_{L2}R_{L2} + V_{CSOS2})A_{CS2} + V_{DAC} \qquad (3)$$

$$V_{CS1} = (I_{L1}R_{L1} + V_{CSOS1})A_{CS1} + V_{DAC} = V_{CS3} = (I_{L3}R_{L3} + V_{CSOS3})A_{CS3} + V_{DAC} \qquad (4)$$

And

$$I_{L1} + I_{L2} + I_{L3} = I_O \qquad (5)$$

From (3), (4) and (5) the inductor current and the output voltage of the three phase converter with average current sharing can be derived as shown in (6) and (7) respectively on the next page.

TABLE I. LOAD LINE ERROR CAUSED BY EACH PARAMETER

| Contributing Factors | | Tolerance of the Parameters | Output Voltage Errors (mV) Calculated from (5), (6) and (7) | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | RL Change at 0.385%/ºC without CSA Gain Compensation (RFB=1.15kΩ, RDRP=11.8kΩ) | | RL Change at 0.385%/ºC with Compensati on from CSA Gain Variation at -0.114 %/ºC (RFB=1.10kΩ, RDRP=10.2kΩ) | | RL Change at 0.385% /ºC with Compensation from CSA Gain Variation at -0.2 %/ºC (RFB=976Ω, RDRP=8.31kΩ) | |
| | | | ***Io=0A*** | ***Io=75A*** | ***Io=0A*** | ***Io=75A*** | ***Io=0A*** | ***Io=75A*** |
| DAC Voltage (VDAC) | | 1.35V +/- 0.5% | +/- 6.750 | +/- 6.750 | +/- 6.750 | +/- 6.750 | +/- 6.750 | +/- 6.750 |
| Oscillator Voltage (VOSC) | | 1.2V +/- 3% | -/+ 0.719 | -/+ 0.719 | -/+ 0.688 | -/+ 0.688 | -/+ 0.610 | -/+ 0.610 |
| Oscillator Resistor (ROSC) | | 57.6kΩ +/- 1% | +0.237<br>-0.242 | +0.237<br>-0.242 | +0.227<br>-0.231 | +0.227<br>-0.231 | +0.201<br>-0.205 | +0.201<br>-0.205 |
| Set Point Resistor (RFB) | | RFB +/- 1% | -/+ 0.238 | -/+ 1.571 | -/+1.737 | -/+ 1.940 | -/+0.206 | -/+1.466 |
| Droop Resistor (RDRP) | | RDRP +/- 1% | 0 | +1.318<br>-1.345 | 0 | +1.283<br>-1.309 | 0 | +1.472<br>-1.502 |
| Droop Amplifier Offset (VDRPOS) | | -2mV +/- 10mV | +/- 0.975 | +/- 0.975 | -/+1.078 | -/+1.078 | -/+1.175 | -/+1.175 |
| DCR of Inductor (RL1/RL2/RL3) | | 1.2mΩ +/- 5%<br>(1.2mΩ +/- 10%) | 0<br>(0) | -2.151<br>+2.299<br>(-4.167<br>+4.762) | 0<br>(0) | -2.087<br>+2.231<br>(-4.043<br>+4.621) | 0<br>(0) | -2.033<br>+2.174<br>(-3.940<br>+4.502) |
| Current Sense Amplifier Input Offset (VCSOS1/ VCSOS2/ VCSOS3) | | 0mV +/- 5 mV | -6.075<br>+5.295 | -6.075<br>+5.295 | -/+6.136 | -/+5.516 | -/+6.557 | -/+5.374 |
| Current Sense Amplifier (CSA) Gain (ACS1/ACS2 /ACS3) | | 35 +/- 9% | 0 | -3.774<br>+4.256 | 0 | -3.662<br>+4.129 | 0 | -4.638<br>+5.301 |
| Share Resistor (RS1/RS2/RS3) | | 10kΩ +/- 20% | 0 | 0 | 0 | 0 | 0 | 0 |
| ***Deviation from the Typical Load Line*** | Root-Sum-Square Analysis (See Fig. 3) | | +13.830<br>-11.290 | +12.160<br>-18.320 | +14.560<br>-10.760 | +15.960<br>-12.930 | +17.712<br>-8.848 | +21.525<br>-6.798 |
| | Worst-Case Analysis (See Fig. 4) | | +16.640<br>-24.700 | +32.640<br>-51.400 | +20.480<br>-27.590 | +38.180<br>-47.590 | +24.099<br>-26.427 | +43.109<br>-40.685 |
| | PSpice Monte Carlo Simulation (See Fig. 7) | | | | +21.200<br>-15.660 | +13.340<br>-29.400 | | |

$$IL_1 = \frac{-A_{CS2}R_{L2}A_{CS1}V_{CSOS1} + A_{CS2}R_{L2}A_{CS3}V_{CSOS3} - A_{CS1}V_{CSOS1}A_{CS3}R_{L3} + A_{CS2}R_{L2}I_O A_{CS3}R_{L3} + A_{CS2}V_{CSOS2}A_{CS3}R_{L3}}{A_{CS1}R_{L1}A_{CS2}R_{L2} + A_{CS1}R_{L1}A_{CS3}R_{L3} + A_{CS2}R_{L2}A_{CS3}R_{L3}}]$$

$$IL_2 = \frac{A_{CS1}V_{CSOS1}A_{CS3}R_{L3} - A_{CS2}V_{CSOS2}A_{CS3}R_{L3} - A_{CS1}R_{L1}A_{CS2}V_{CSOS2} + A_{CS3}V_{CSOS3}A_{CS1}R_{L1} + I_O A_{CS1}R_{L1}A_{CS3}R_{L3}}{A_{CS1}R_{L1}A_{CS2}R_{L2} + A_{CS1}R_{L1}A_{CS3}R_{L3} + A_{CS2}R_{L2}A_{CS3}R_{L3}}] \quad (6)$$

$$IL_3 = \frac{A_{CS1}R_{L1}A_{CS2}R_{L2}I_O + A_{CS1}R_{L1}A_{CS2}V_{CSOS2} + A_{CS2}R_{L2}A_{CS1}V_{CSOS1} - A_{CS3}V_{CSOS3}A_{CS1}R_{L1} - A_{CS2}R_{L2}A_{CS3}V_{CSOS3}}{A_{CS1}R_{L1}A_{CS2}R_{L2} + A_{CS1}R_{L1}A_{CS3}R_{L3} + A_{CS2}R_{L2}A_{CS3}R_{L3}}]$$

$$V_O = V_{DAC} - \frac{V_{OSC}}{R_{OSC}}R_{FB} + \frac{R_{FB}}{R_{DRP}}[V_{DAC} - \frac{V_{CS1}\cdot R_{S2}\cdot R_{S3} + V_{CS2}\cdot R_{S1}\cdot R_{S3} + V_{CS3}\cdot R_{S1}\cdot R_{S2}}{R_{S1}\cdot R_{S2} + R_{S2}\cdot R_{S3} + R_{S1}\cdot R_{S3}}] \quad (7)$$

Table I shows the tolerance of all the parameters in Fig. 1 which contribute to the load line error. The tolerances are available from the IC specifications [3] [4]. Equations (5), (6) and (7) are used to evaluate the contribution of each parameter to the accuracy of the load line.

Sensitivity analysis of the output voltage is performed by calculating the deviation from the nominal output voltage along with the deviation direction corresponding to the tolerance of one parameter while the tolerances of other parameters are set to zero. The calculation is repeated for each parameter, and the deviations are root-sum-squared to

obtain the overall tolerance of the output voltage. Based on the direction of the deviation caused by each parameter, the worst-case load line error can be calculated, as shown in Table I.

The inductor DC resistance changes with temperature at the rate of 0.385%/ºC. Fig. 2 shows the measured inductor wire temperature of a three phase converter at different load currents, and curve-fitting is used to obtain the relationship between temperature and the current. The dependency of DC resistance on the current is included in the calculation of the output voltage errors. Column 3 and 4 of Table I show the output voltage errors at load currents of 0A and 75A respectively without inductor resistance temperature coefficient (TC) compensation. The non-compensated TC root-sum-square analysis and worst-case analysis results are shown in Fig. 3(a) and Fig. 4(a) respectively.

In contrast to MOSFET $R_{DS(ON)}$, the inductor DCR has a constant temperature coefficient, therefore it is possible to compensate the DCR variation with the temperature. In the phase IC IR3085, the gain of the current sense amplifier (CSA) automatically reduces at a rate of about -0.114%/ºC when the die temperature increases. The case temperature of the phase IC is measured by an IR Thermo Probe Meter, as shown in Fig. 2. The die temperature of the phase IC is calculated based on the thermal impedance of the IC package and the power loss of the phase IC. The die temperature is proportional to the inductor temperature because the phase IC is placed close to the inductor. Although the temperature coefficient of the CSA is smaller than that of the inductor, the phase IC die temperature is higher than that of the inductor due to quiescent and gate drive power loss. The effect of the compensation depends on the layout of the power stage, i.e. the relative location of the phase IC and the inductor. Column 5 and 6 in Table I, Fig. 3(b) and Fig. 4(b) show the root-sum-square analysis and the worst-case analysis results of the load line error with TC compensation from the CSA gain variation.

If the temperature coefficient of the CSA gain is further increased to 0.2%, the better compensation of inductor DCR can be obtained and the load lines are more flat both in the root-sum-square analysis in Fig. 3 (c) and in the worst-case analysis in Fig. 4 (c).

To make sure that the load line error from both the worst-case and root-sum-square analysis fall within the boundaries, different no-load offset resistor $R_{FB}$ and droop resistor $R_{DRP}$ are used for the above three cases.

Table I clearly demonstrates the most influential factors affecting the load line. DAC voltage $V_{DAC}$ is still one of the most important factors even after it is trimmed to +/- 0.5%. The offset of the current sense amplifier $V_{CSOS}$ is critical because its value is comparable to the magnitude of the current signal at the amplifier input under light load condition. The influence of the inductor DC resistance $R_L$ is significant especially if $R_L$ tolerance is large (both +/-5% and +/-10% tolerance cases are shown in Table I ). Another important factor is the current sense amplifier gain $A_{CS}$. The share resistor $R_S$ has no effect on the load line error, although it does affect the current sharing accuracy of the three phases.

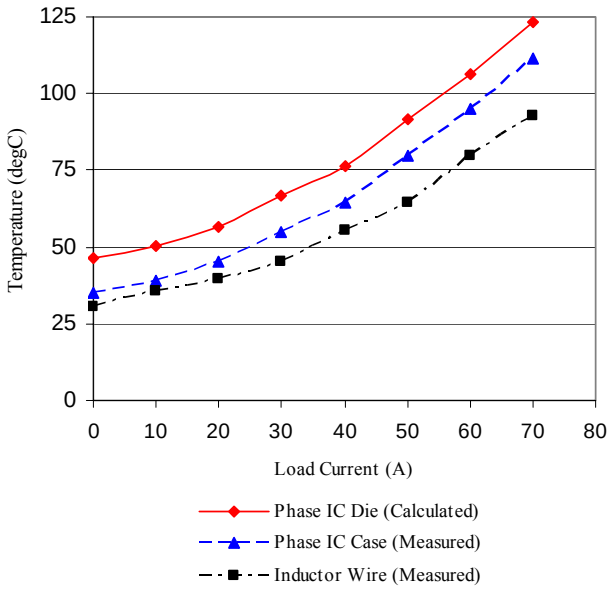



Fig. 2 Temperature of the phase IC and the inductor in a three phase converter

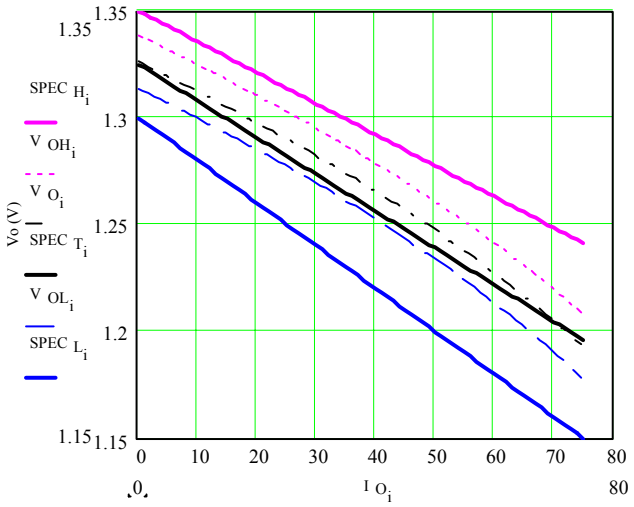
## III. PSPICE MONTE CARLO SIMULATION

PSpice is used for the Monte Carlo analysis of the load line error by simulating the block diagram of a three phase buck converter shown in Fig. 5. The circuit consists of transistor level circuits in the IC and the required external components. The model parameters of all devices and components are varied randomly within the tolerance specified for these devices. The three-terminal PWM average model is used for the power stage to save simulation time. Each simulation is run 1000 times to obtain reasonable results, because run times exceeding 1000 make minimal difference in the result. Fig. 6 shows the simulated Gaussian distribution of the output voltage $V_O$ at one operating point, and the IC die temperature is set corresponding to the load current as shown in Fig. 2. The simulation is repeated at different load conditions and temperatures using 3-sigma values to determine the error of $V_O$.

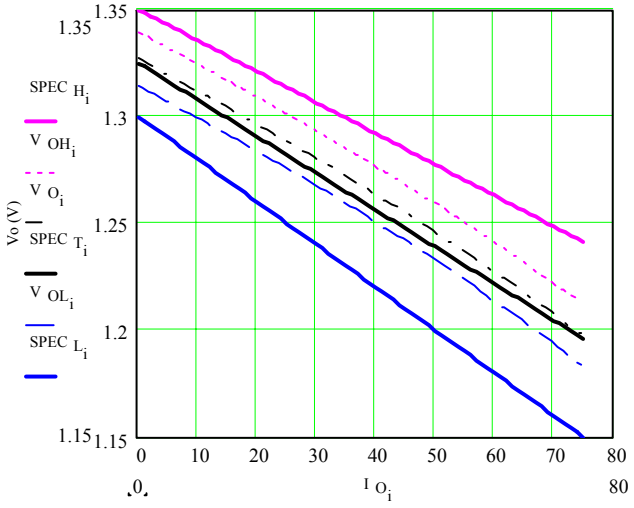
Fig. 7 shows the Monte Carlo simulation of the load line with two different $R_L$ tolerances. The error is much smaller than the result from worst-case analysis, especially at heavy load condition. The error band is similar to the result from root-sum-square analysis except at heavy load, but is wider. Therefore, root-sum-square analysis underestimates the load line error.

## IV. EXPERIMENTAL RESULTS

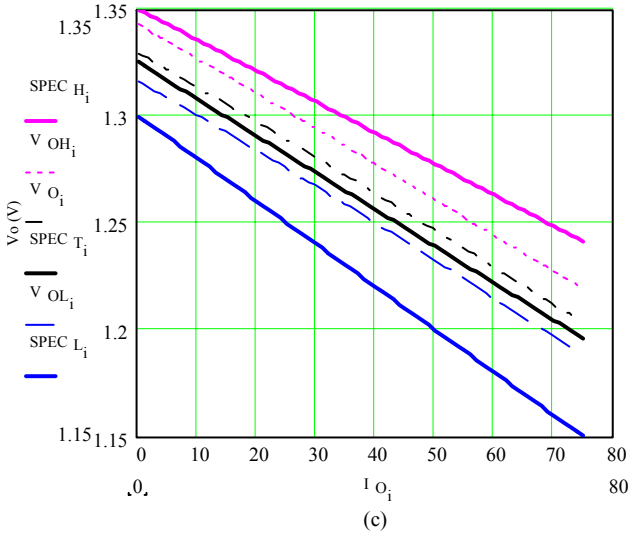
An actual three phase synchronous buck converter with inductor current sensing is used to verify the load line analysis and simulation. In the course of recording data, the converter is operated for an extended duration to allow it thermally stabilized whenever the load current is adjusted.




(a)



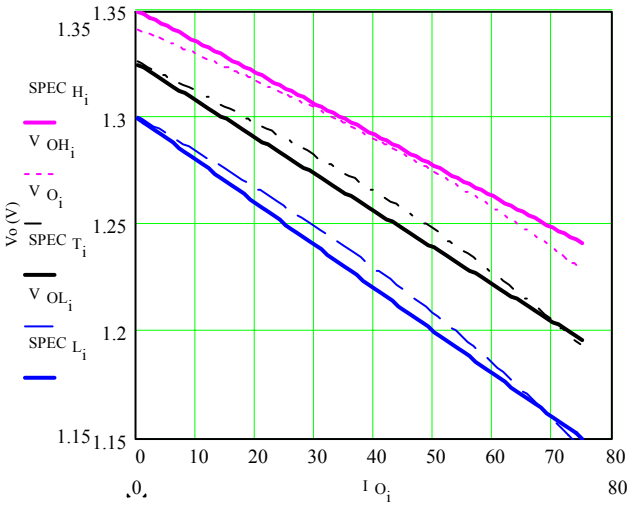

(b)



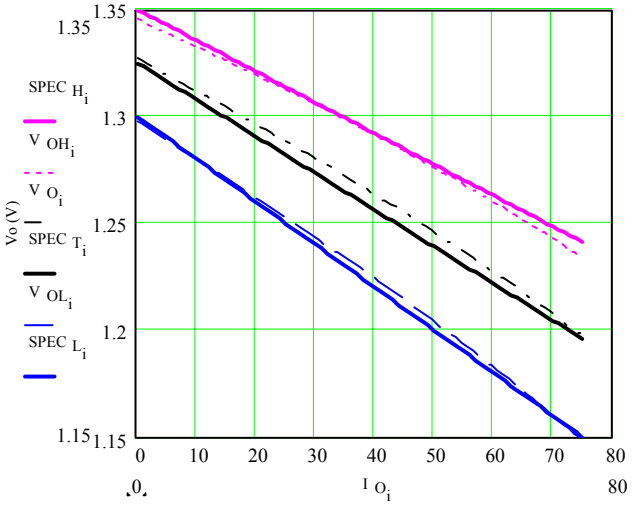

(c)

Fig. 3 Root-sum-square analysis of the load line

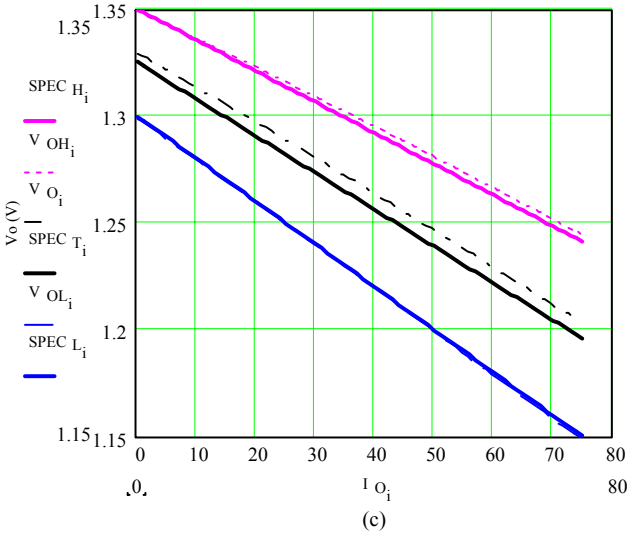
(a) No CSA gain temperature compensation;
(b) CSA gain compensation at -0.114 %/ºC;
(c) CSA gain compensation at -0.2 %/ºC.




(a)




(b)




(c)

Fig. 4 Worst-case analysis of the load line

(a) No CSA gain temperature compensation;
(b) CSA gain compensation -0.114 %/ºC;
(c) CSA gain compensation at -0.2 %/ºC.

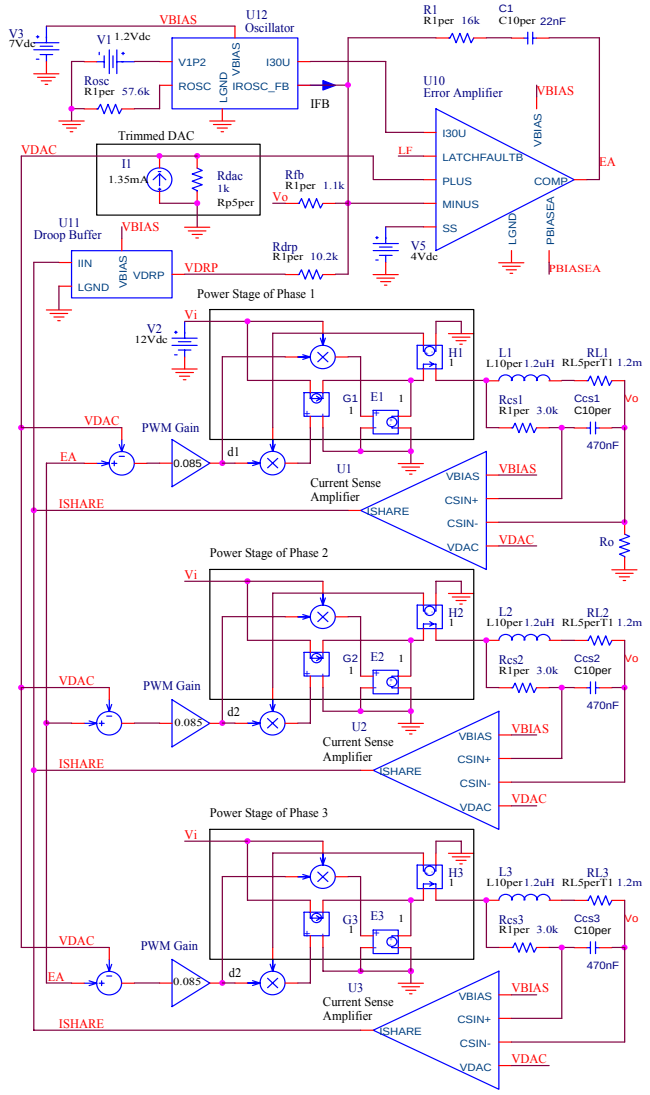



Fig. 5 PSpice Monte Carlo simulation circuit

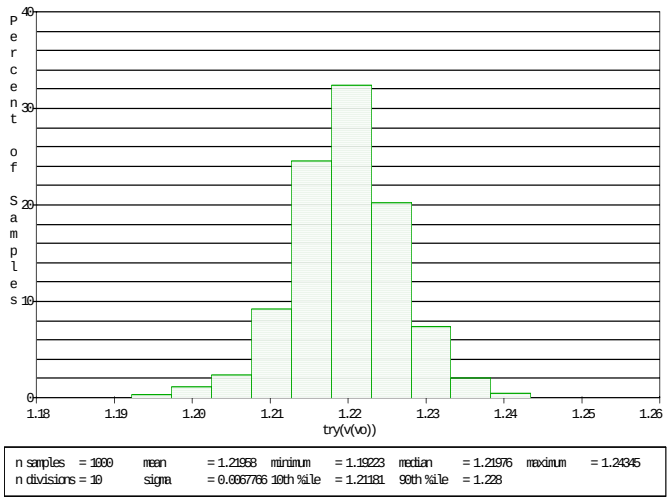



Fig. 6 PSpice Monte Carlo simulation of the load line at Io=60A, VDAC=1.35V, and IR3085 die T=105ºC

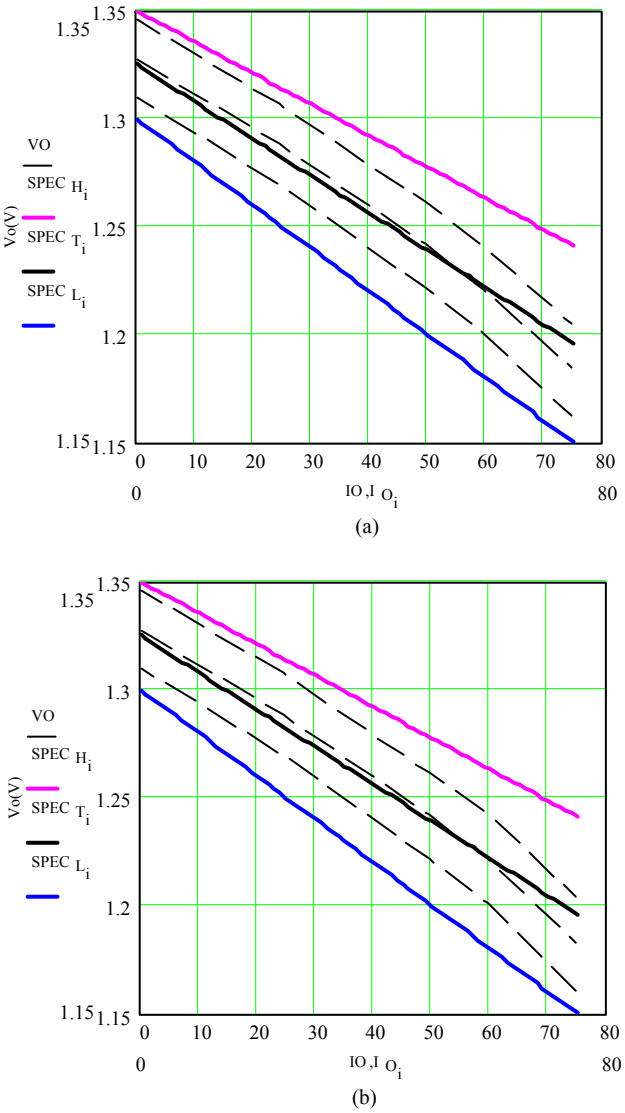



Fig. 7 PSpice Monte Carlo simulation of the load line

(a) Inductor DC resistance RL tolerance =+/-5%
(b) Inductor DC resistance RL tolerance = +/-10%

Fig. 8 shows the measurement of the load line, which coincides to the required typical load line at light load but dips a few mille-Volts away from the ideal at heavy load because of the insufficient temperature compensation from the CSA gain variation. Better temperature compensation can be attained with the addition of a negative temperature coefficient (NTC) thermistor Rt placed in parallel with the feedback resistor RFB, as shown in the dashed lines in Fig. 1. The resistor R (10.0kΩ) in series with Rt (TDK NTCG164BH474JT 47kΩ) is used to adjust the temperature coefficient of the thermistor Rt. When the temperature increases, the equivalent resistance of RFB, Rt and R resistor network is reduced, and the output voltage is raised at heavy load, as shown in Fig. 8.

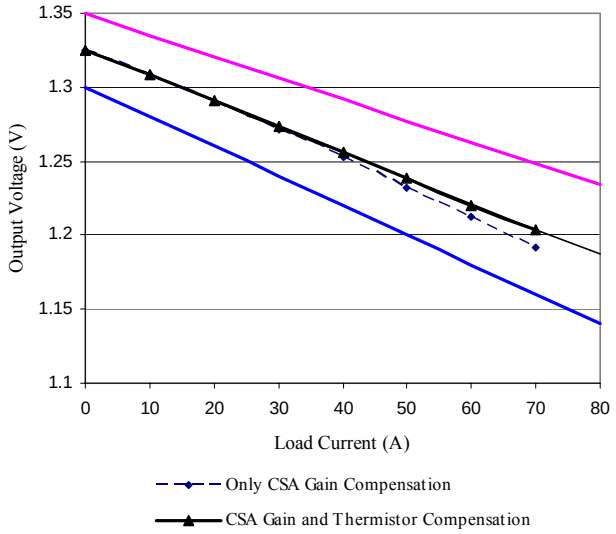



Fig. 8 Measured load line with temperature compensation

## V. CONCLUSIONS

The load line equations of a three phase buck converter are derived and used in the root-sum-square and worst-case analysis of the system accuracy. The analysis can be extended to any phase number. The most critical parameters to the load line error are identified, which are DAC voltage, the offset and gain of the current sense amplifier, as well as the DC resistance of the inductor. PSpice Monte Carlo statistical simulation is used to determine the system accuracy of a three phase voltage regulator module, and is compared with the root-sum-square method and the worst-case analysis. The comparison shows that the root-sum-square analysis underestimates the error while the worst-case analysis overestimates it. Monte Carlo simulation is a good method to provide realistic prediction of system performance.

## ACKNOWLEDGMENT

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