Compatibility Analysis of Space Qualified Intermediate Bus Converter and Point of Load Regulators for Digital Loads

Bjarne Soderberg[1], Tiva Bussarakons[2]
[1]International Rectifier, Aerospace and Defense (Denmark), bsoderb1@irf.com
[2]International Rectifier, Aerospace and Defense (USA), tbussar1@irf.com

ABSTRACT

Distributed power architecture (DPA) has become the power system solutions of choice for digital loads such as FPGAs and other ASIC devices to optimize the system efficiency and dynamic response due to negative effect of parasitic impedances. IR's ZB with its world class efficiency performance and SBB design platforms are the key power conversion elements of such DPA power system solutions. This paper examines the compatibility of the ZB series, an intermediate bus converter (IBC) and the SBB series, a non-isolated synchronous buck point of load (POL) regulator to insure the stability of the power converters and the power system under various static and dynamic loading conditions.

BACKGROUND

Historically, supply power for digital logic and signal processing devices of a large processing payload was distributed from a central power supply via a back plane or other distribution wiring to the processing assembly boards. The most common voltage was 5 volts. The required current for large and small scale integrated circuits were easily handled with a centralized power system. Other voltages such as 3.3 volts could also be used. With the recent advances of integrated circuit and ASIC technology, the required core and I/O supply voltages have declined. The common voltages are now 3.3V, 2.5V and lower toward 1V. Lower voltages are expected in the near future as the IC manufacturers continue to reduce the feature sizes and increase the gate counts to add functionality and improve performances. While the operating power decreases, the supply current has increased though not with the same proportion as the supply voltage. In addition, the new FPGA and ASIC devices are sensitive to supply voltage variations. The supply voltage must be maintained within a tight regulation band to insure proper functionality of the devices. This restriction necessitates a new method of distributing power where the physical proximity of a power source and the new digital FPGA and ASIC devices must be sufficiently close to insure an acceptable voltage excursion due to parasitic impedances.

DISTRIBUTED POWER ARCHITECTURE (DPA)

To meet the specific supply voltage requirements of the new FPGA and ASIC devices, distributed power system (DPA) has recently become the power system of choice especially for medium to high power design applications. Figure 1 depicts a DPA system. The system consists of an intermediate bus converter (IBC) and point of load (POL) regulators. Two, three or more POLs may be deployed depending on system designs. The IBC converts the spacecraft power to a regulated DC voltage typically 5 volts, which powers the POLs. Each POL is placed on a board near the FPGAs or ASICs to minimize parasitic impedances. An IBC is usually placed some distance away and is usually not on the same assembly card as the FGPA/ASIC devices due to cooling and other mechanical considerations.

As FPGAs/ASICs require a well controlled and regulated power from the POLs, the POLs pose similar requirements for their power source, an output voltage of the IBC. It becomes clear that design considerations must be given to the compatibility of an IBC and POLs. In the subsequent analysis, IR's ZB and SBB series will be used as an intermediate bus converter and point of load regulators, respectively.

Zx Series DC-DC Converters – Intermediate Bus Converter (IBC)

The Zx series DC-DC converters are low output voltage, high current DC-DC converters targeting digital signal processors, FPGA, ASIC, and other digital applications in moderate to high radiation environments. A functional block diagram of the Zx series is shown in Figure 2. With its excellent efficiency performance the platform is well suited as a standalone ultra efficient module or as a primary down converter providing an intermediate voltage in the distributed power architecture (DPA) systems. The Zx series offers three output current platforms, 25A (ZA), 50A (ZB) and 125A (ZC). The design platform incorporates many functional features that are demanded by today's space design applications. They include under-voltage lockout (UVLO), over-voltage protection, pulse on/off command, output status, input current telemetry, and a trim pin for external output

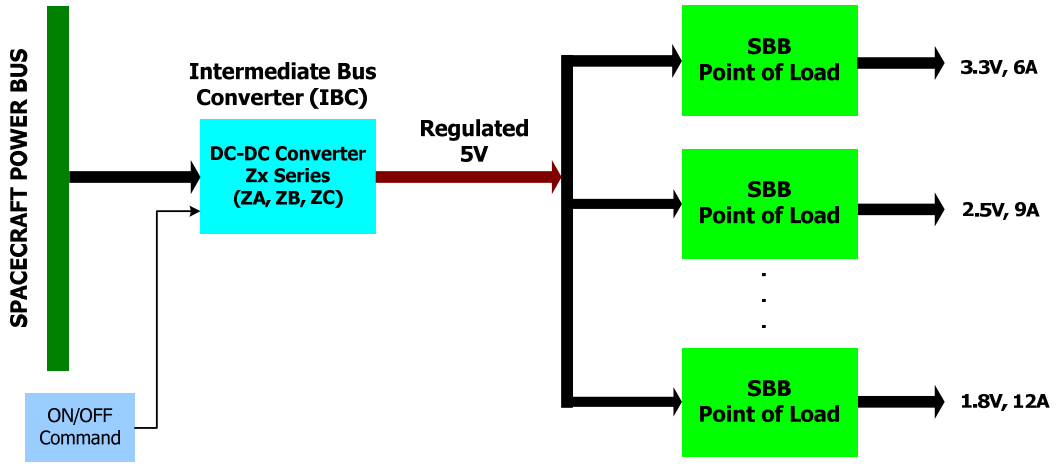

Figure 1 – A Simplified Block Diagram of a Distributed Power Architecture (DPA) Power System

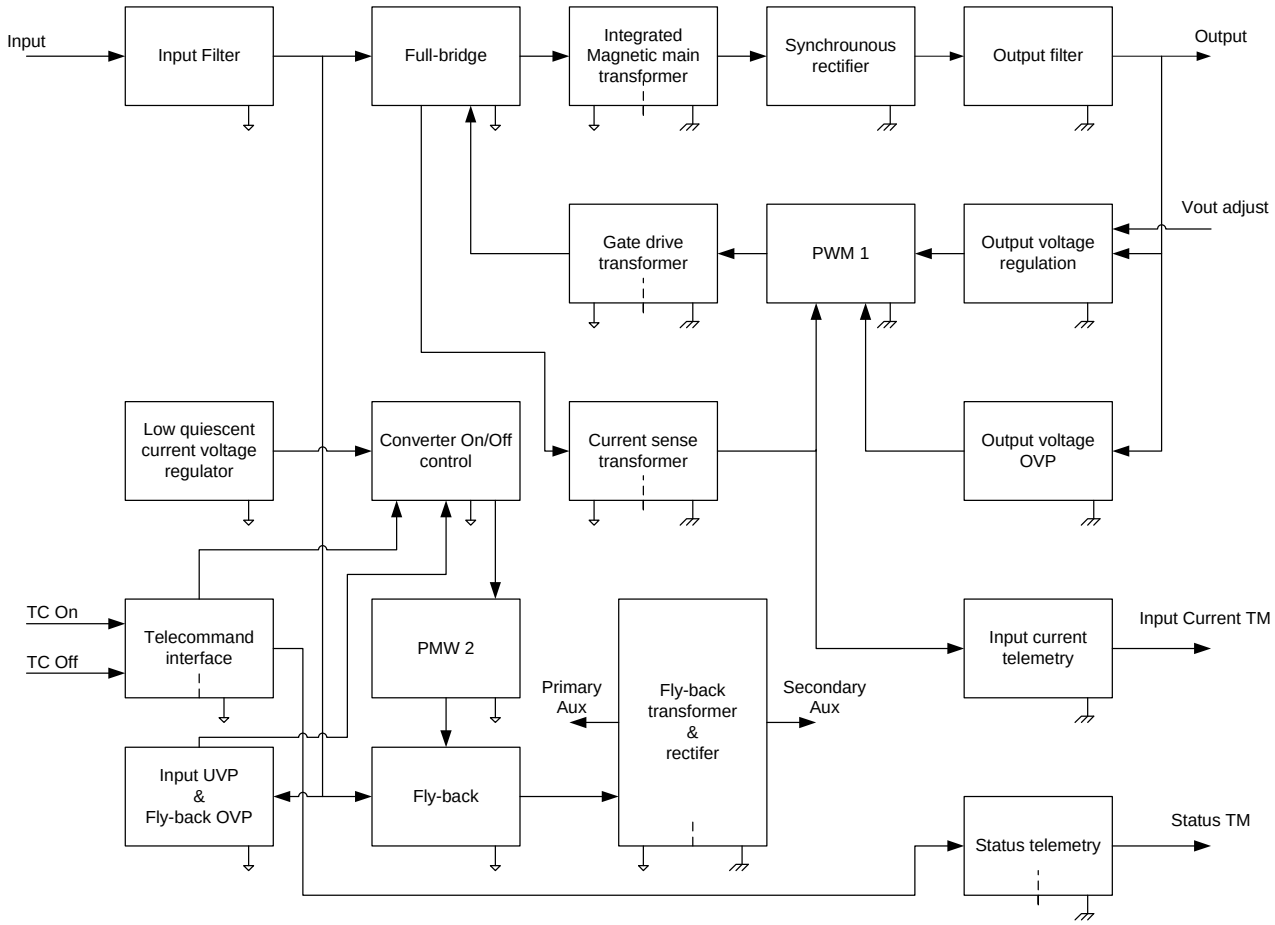

Figure 2 – Zx Series DC-DC Converter Functional Block Diagram

voltage adjustment. The Zx converters can be tailored to operate with any popular satellite power bus voltages from 20V to 100V DC. A typical end-of-life (EOL) efficiency is greater than 92% for a 5V output model.

The design platform uses a two-converter configuration with a simple fly-back converter providing all the internal supplies necessary and a high efficient full-bridge converter with synchronous rectification providing the output. The fly-back converter starts after receiving an On-command. The tele-command interface is using opto-couplers to provide the necessary isolation. The interface is compatible with standard high level pulse commands intended for relays. A tele-command status telemetry is derived from an extra opto-coupler.

SBB – Point of Load (POL) Regulator

The SBB series of 30W POLs the first Class K hybrid POL family in the industry utilize a non-isolate buck converter topology with synchronous output rectification to maximize efficiency performance. Figure 3 presents an SBB functional block diagram. The POL operates from a regulated input power source of 5±0.5V DC. The standard output voltages are 3.3V, 2.5V, 1.8V, 1.5V, and 1.0V, and up to 14A output current with output power limited to 30W maximum. The nominal switching output frequency is 400 kHz. An internal EMI filter minimizes the reflected switching ripple current to allow easy filtering to meet most space applications at the system level. A two-stage output filter reduces the typical output ripple to less than 20mV peak-to-peak when measured with 20MHz bandwidth. A typical efficiency for a 3.3V model is 88%.

Output current is limited under any load fault condition. It is designed to behave similar to a constant current source with the output voltage dropping below nominal. The regulator will resume normal operation when the load current is reduced below the current limit point. This protects the POL module from both overload and short circuit conditions. The current limit point exhibits a negative temperature coefficient to reduce the possibility of thermal runaway. There are no latching elements included in the load fault protection circuits to eliminate the possibility of falsely triggering the protection circuits during single event radiation exposure.

An under-voltage lockout circuit prohibits the POL module from operating when the line voltage is too low to maintain the output voltage. The POL will not start until the input voltage rises to 4.2 ± 0.3 volts and will shut down when the input voltage drops below 4.0 ± 0.3 volts.

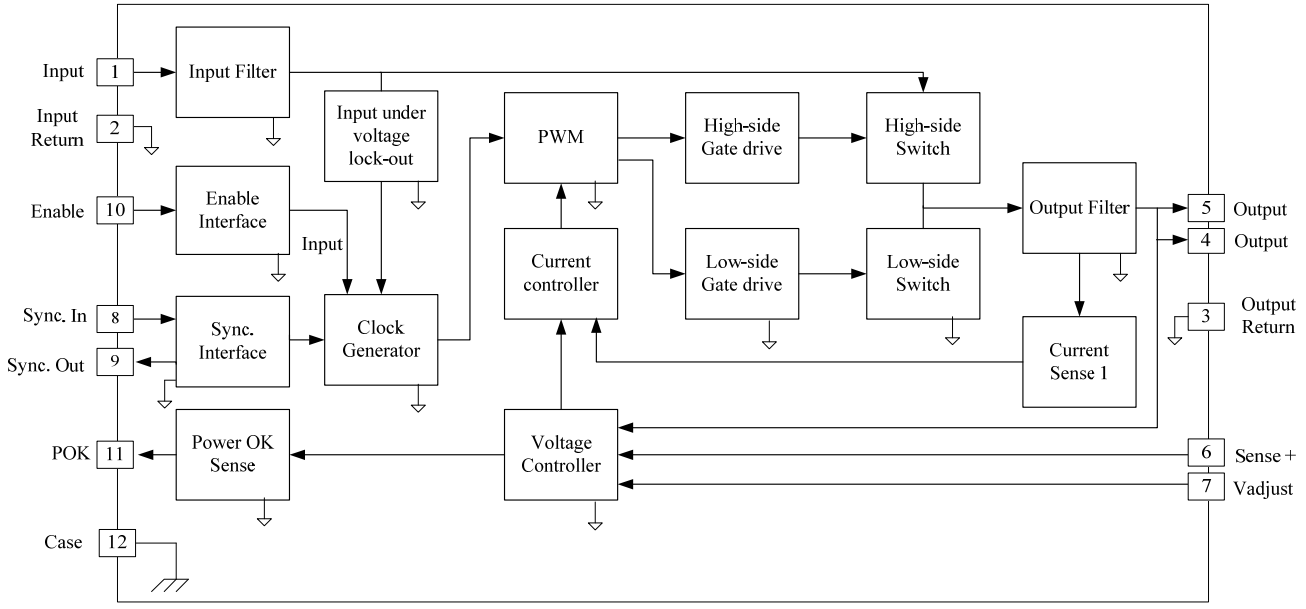

Figure 3 – SBB Synchronous Buck Regulator Block Diagram

SIMULATION/ANALYSIS

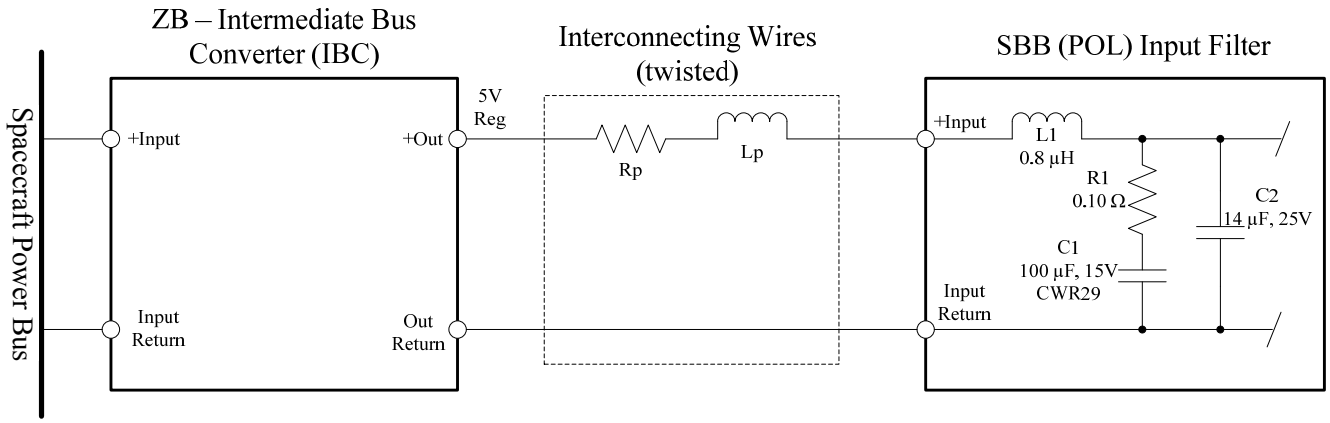

Figure 4 – A Simplified Power System Block Diagram

A simplified block diagram of a sample power system is shown in figure 4. Design of an IBC must take into account the ripple current demanded by the POLs, step load response performance of the IBC, and the effect of the parasitic impedance (Rp and Lp) of the interconnecting wires from the output of an IBC to the POLs. Output voltage excursion of the IBC must be such that the over/under voltages are within the operating threshold of the required input voltage of the POLs under the extreme dynamic loading conditions. The input filter of the POLs and the interconnecting wires must be sized to insure the source voltage at the input terminals of each POL does not dip below the under-voltage lockout threshold of the POLs.

IR's ZB series (5V/50A) DC-DC converter is selected to provide a regulated intermediate bus voltage of 5V and IR's SBB POLs are chosen to provide the regulated voltages which power the FPGAs or ASICs loads of the modern day signal processing design applications. Up to 10 SBB POLs are used in this analysis which represents the worst case scenario as most design applications may require only 2 to 4 POLs. Figure 4 shows a typical power system for such digital loads with the loads excluded. And only one POL is shown for simplification. Please note that this analysis includes circuit simulation for the ZB converter in combination with actual circuit designs of the SBB POL. Figures 5 to 13 illustrate a step by step analysis of the power system of Figure 4.

1. ZB as a Power Source for POLs

The ZB is designed to provide a load step response of <5% (250mV) for a load step of 25A, 50% to 100% of the rated load. It follows that the maximum effective output impedance must be less than 10mΩ which yields a maximum output voltage excursion of 250mV (10mΩ x 25A) under this condition.

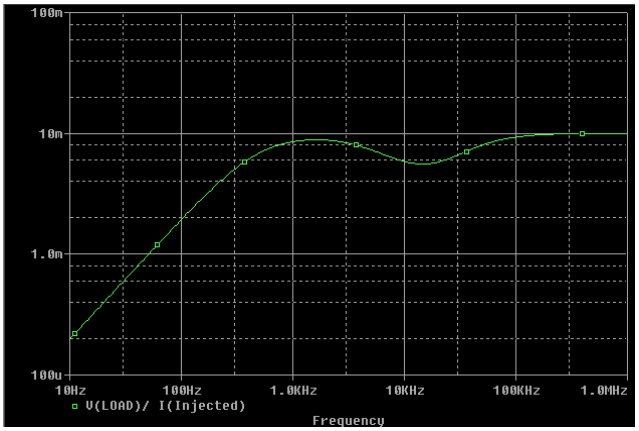

Figure 5 – Simulated Output Impedance (Zout) of the ZB Converter

2. Modeling a System with one ZB and 10 SBB POLs

With a ZB capable to power 10 SBB POLs, the analysis will examine only one POL (one-tenth of the system) where Zout of the ZB becomes 10 times under this scenario. Figure 6 represents this simulated Zout.

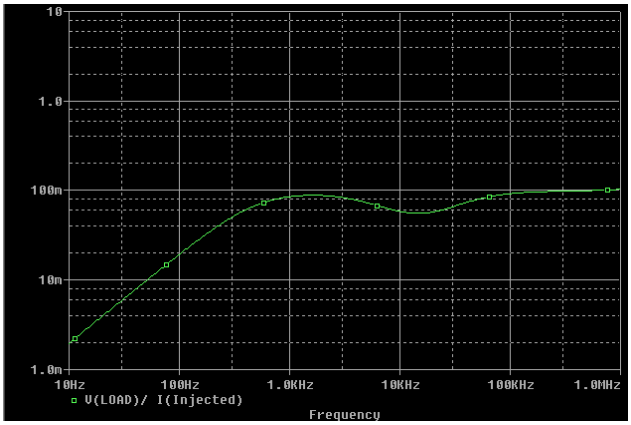

Figure 6 – Output Impedance of One-Tenth of the ZB Converter

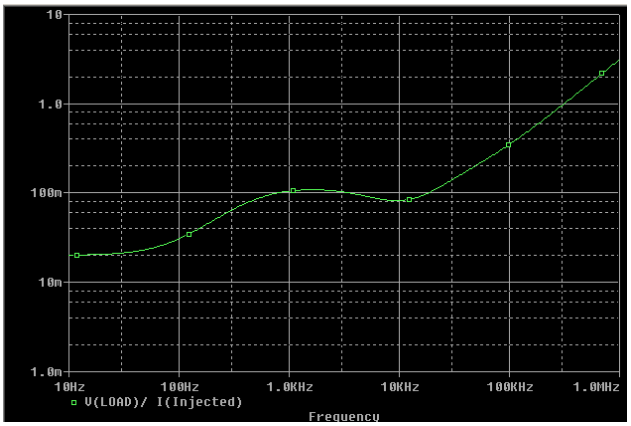

Figure 7 – Impedance of Power Source at the Input of the POL

3. Including ZB/SBB Interconnecting Wires

A voltage drop in the connecting wires must be taken into account. If a POL is assumed to draw approximately 5A (under a heavy load condition) and if a voltage drop in the wires of <100 mV is desired then the wire or conductor resistance must be <20 mΩ. Table 1 shows the wire sizes, length of wire and corresponding inductance for interconnecting wire candidates for up to 20 mΩ of wire resistance. The total wire length is limited to 74 cm should 16 gage wire be selected for the interconnection. Similar consideration must be given to other means of connection if wires are not used. The maximum wire/conductor length includes the positive and the return lines.

Wire Size (AWG)	Ohm/ 100 meter	Resistance (mΩ)	Wire Length for 20 mΩ (cm)	Corresponding Inductance (μH) [1]
14	1.69	20	118.34	1.710
16	2.68	20	74.63	1.044
18	4.27	20	46.84	0.633

Table 1 – Wire Length Yielding Wire/Conductor Resistance of 20 mΩ for Different Wire Sizes and the Corresponding Wire Inductance

Figure 7 is a plot of power source impedance including the interconnecting wires at the input of the POL.

4. Effect of the POL Internal Input Filter – Decoupling Ceramic Capacitor only

Each POL requires source impedance at the switching frequency and above. This is ensured with inclusion of an appropriate internal input filter. We will first exam a design with only the inclusion of a ceramic capacitor C2 (14μF, 25V) of Figure 4. Figure 8 below shows the plot of the resultant source impedance. The resonance peaking at 50KHz leads to an unacceptable load step response as the input voltage may dip below input under voltage lockout threshold (4.0 ±0.3V) and disable the POL. A plot of this dip of the POL input voltage is shown in Figure 9.

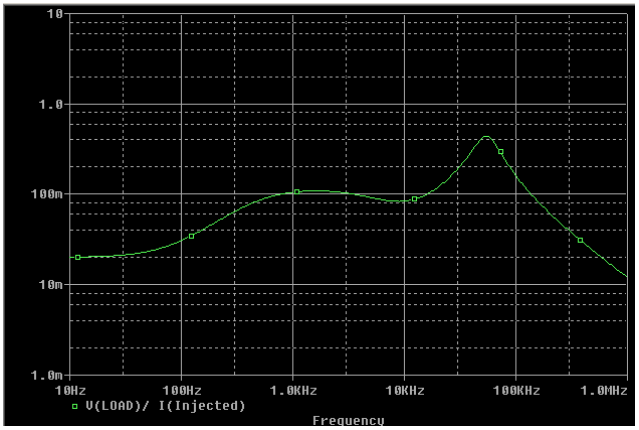

Figure 8 – Source Impedance at the Input of the POL with only the Decoupling Ceramic Capacitor C2

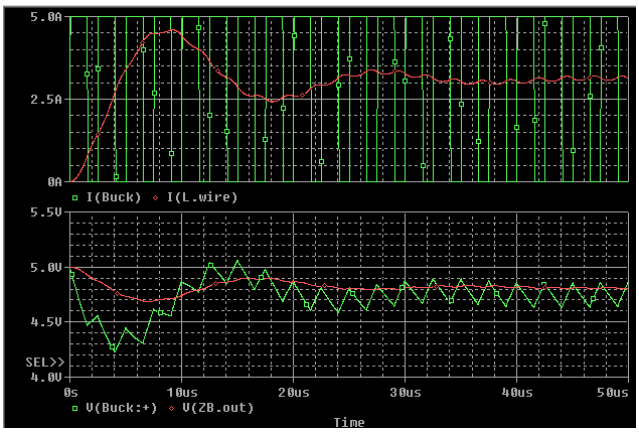

Figure 9 – Input Voltage, V(Buck+) at Input Terminals of the POL with a Load Step Response (50% to 100% load) – Ceramic Capacitor (C2) only

5. Effect of the POL Internal Input Filter Including an R1/C1 Damping Filter (R1 and C1 of Figure 4)

Figure 10 shows a plot of the source impedance at the input of the POL with the inclusion of decoupling capacitor C2 and the R1/C1 damping filter, a tantalum capacitor in series with a resistor. Figure 11 shows the resultant input voltage, V(Buck+) of the POL in response to the 50% step load including the wire resistance of approximately 20 mΩ. The input voltage is above the turn-off threshold of 4.3V allowing the POL to operate without interruption.

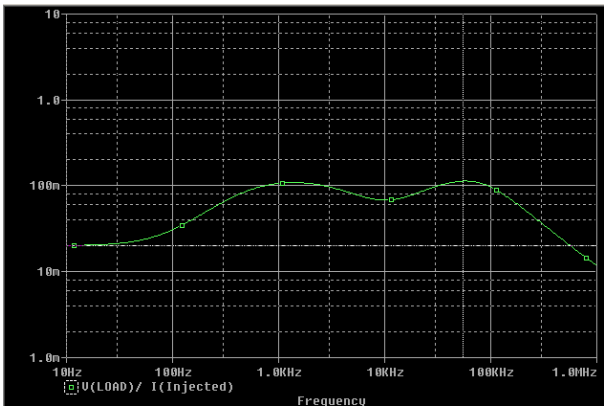

Figure 10 – A Plot of Source Impedance with the Decoupling Capacitor and R1/C1 Damping Filter at the Input of the POL Including the Interconnecting Wire Resistance

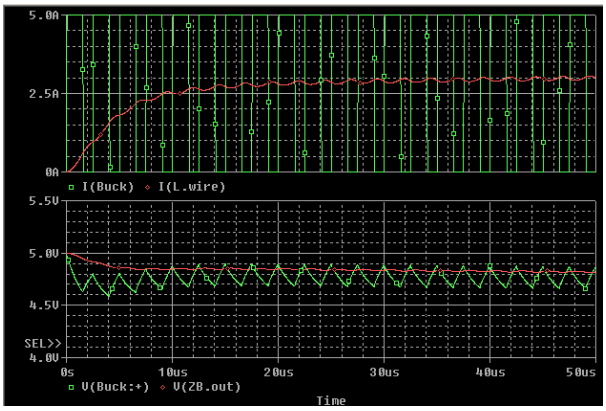

Figure 11 – Input Voltage, V(Buck+) at the Input of the POL in Response to a 50% Step Load with Interconnecting Wires

6. ZB Output Ripple Current and Interconnecting Wire Inductance

In case the interconnection of a ZB to a POL is accomplished with very short wires, the parasitic inductance of the wires may be very low or non-existent. The output ripple current may reach a level harmful (violating de-rating requirements) to the output capacitors of the ZB and induces an unacceptable conducted emission (CE) at the 5V line. This may also affect other electronics that are connected to this power line. Figure 12 presents a plot of the resultant ripple current I(L.wire) and ripple voltage into ZB output V(ZB.out).

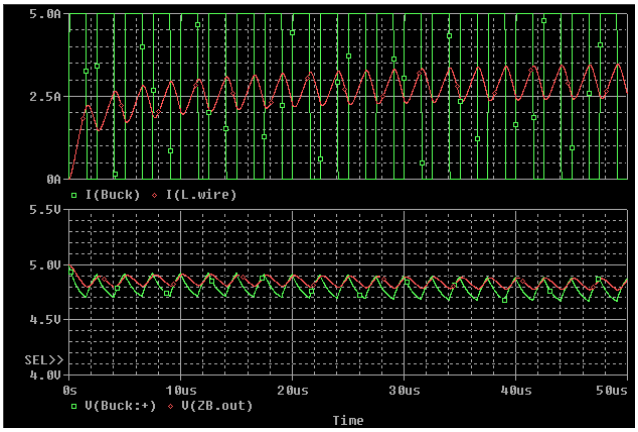

Figure 12 – Ripple Current, I(L.wire) and Ripple Voltage into ZB Output V(ZB.out) with Minimal Wire Inductance

7. ZB Output Ripple Current with a Complete POL Input Filter

To insure that the output ripple current of the ZB is reduced to an acceptable level, an inductor is added in series with the positive input of the POL. Figure 13 shows a plot of this reduce ripple current, I(L.wire). Please note also that input voltage V(Buck+) at the input terminals of the POL is above the turn-off threshold voltage of 4.3V allowing the POL to operate without an interruption.

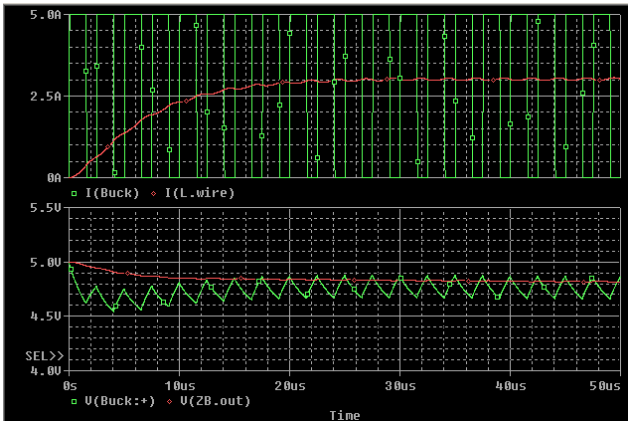

Figure 13 – Ripple Curren I(L.wire) and Ripple Voltage into ZB Output V(ZB.out) in a System with Minimum Wiring Inductance but with the Addition of Inductor L1 in Figure 4.

CONCLUSION

To insure a continuously unconditionally stable operation of the POLs, an IBC must provide an acceptable transient response performance under all possible loading conditions. The analysis uses a 50% (25A step load) of the rated load current which is very conservative. A low source impedance from an IBC cannot in itself ensure an acceptable output voltage undershoot. It is also necessary to take into account the interconnection inductance and wire/conductor resistance. IR SBB POLs can be connected to the intermediate bus converter ZB with appropriate wire size and length as described in Table 1 without the need for additional filtering at the input of the POLs. In general, a POL requires an input filter including an input inductance to ensure that the ripple current as seen by the output filter of the IBC is kept to an acceptable level as required by system EMI requirements. The SBB POLs can also be connected with minimum inductance without a concern for excessive ripple current.

ACKNOWLEDGEMENT

We would like to thank our colleagues Lass Pedersen, and Soren Petersen. for their valuable input and technical support.

REFERENCES

1. Grover, F.W. (2004) Inductance Calculations, Dove Publications
2. Smith, Carl. (2005). DC Bus Converter and Point of Load Modules, Power System Design Europe
3. Bussarakons, Tiva. (2004). Military Satellites Pose Engineering Challenges in DC-DC Converter Development, Defense Electronics, A Primedia Publication
4. Zx Series Fact Sheet. (2006). International Rectifier (file: fs8516.pdf)
5. SBB Preliminary Data Sheet. (2008). International Rectifier (file: SBB-SERIES-VRM-PRELIM.pdf)

END OF DOCUMENT