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Combined Device and System Simulation for Automotive Application Using SABER

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Abstract:

For Automotive applications, device optimization requires both system and device level simulation in order to properly predict its performance and thermal response, especially in the case of adverse dynamic conditions.

In this paper, the SABER model of IR's power MOSFET IRFP2907 is validated in a half-bridge circuit using a low frequency two-pulse test. This model is then applied to simulate the performance of an inverter system. Simulation results accurately match the measurement. This work can be extended to evaluate power MOSFETs in other automotive applications such as ISA, EPAS and DC/DC conversion as well as IGBT and anti-parallel diodes in inverter switching applications

***Index Terms* – MOSFET, Modeling, Simulation, SABER**

I: Introduction:

All automotive applications are cost sensitive. It is nearly always desirable to optimize the die size to reduce the cost. However, because of reliability requirements, power devices have to survive system transients and very harsh electrical environments in today's car. Therefore, accurate performance prediction of the power device is essential for the designer to satisfy the trade-off between performance and cost.

Although analytic methods are widely used to estimate the device and system steady state performance, some dynamic characteristics such as device switching loss, stray inductance effect, device avalanche and machine transient are not easily handled by this simple approach. On the other hand, numerical simulation can effectively combine system and device level characteristics to accurately calculate the loss and can predict the device junction temperature, which is the key parameter for power device selection. So with good prediction of the transient and the device thermal response, a device with optimized performance and low cost in the dynamic system environment can be selected.

From the design standpoint, this numerical approach can save not only design time but also the cost of building prototypes.

SABER [1] provides a good platform for device performance prediction in a system environment. It has the capability to deal with both circuit and device level models. Moreover, its mixed signal simulation can handle electrical analog, digital, mechanical, thermal and magnetic blocks in their native domain, with optimized algorithms implemented to balance the accuracy and speed. So in this study, SABER is used as the simulation tool.

Also, device SABER models are now readily available for most new MOSFET products, which provide broad resources and is convenient for benchmark comparison.

II: Simulation and Results:

For device modelling, different levels of model have been developed to support analysis of different level of behavioural complexity [2]. The essential difference is the accuracy of prediction of switching characteristics, especially in automotive applications from medium (12K to 20KHZ in ISA and EPS) to high bandwidth (75K-120KHZ in DC/DC converter) where the switching losses account for a large portion of the total losses and are a nonlinear function of current and device parasitics. By comparison, conduction loss is easy to calculate even considering its temperature dependency.

In this study, to validate the SABER model, the switching characteristics are investigated in a half-bridge circuit, using a low frequency two-pulse test. The simulation results are then compared to measurement. After that, stray inductance effect is examined to clarify the loss distribution between turn-off and turn-on. Following this, a system with a PWM driven three-phase inverter and passive load is simulated to predict the thermal dynamic. Results are compared to the measurements from a real system.

International Rectifier's IRFP2907 is used as an example in this study. Its SABER model was downloaded from IR's website at www.irf.com.

Section 1: Half-Bridge, two-pulse test

Figure 1 shows the circuit diagram. Figure 2 compares simulated and measured Vds and Id during turn-off, while the waveform in Figure 3 is the corresponding gate to source voltage Vgs. Data fitting is achieved by adding

stray inductances to the drain and source leads such that Ld_stray=16nH, Ls_stray=14nH. Figure 4 and 5 illustrate the waveforms during the turn-on process with the same parameters given above.

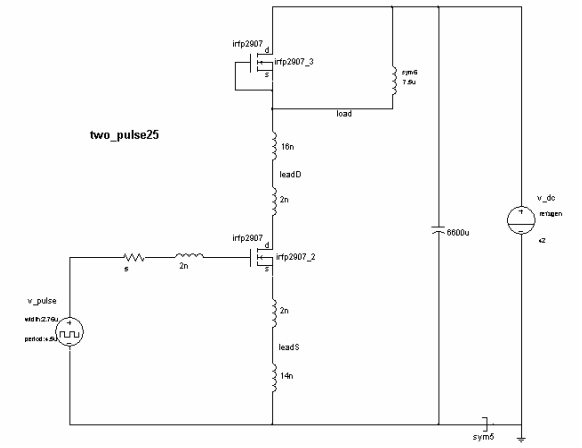

Figure 1: Schematic of the two-pulse test circuit

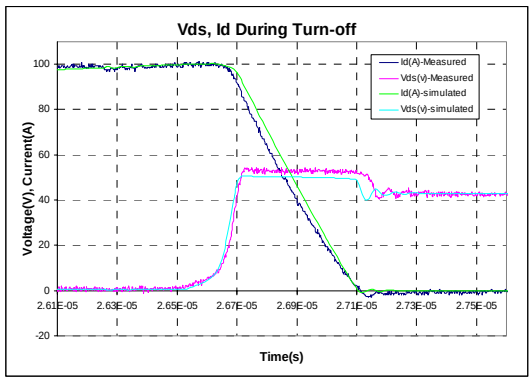

Figure 2: Comparison of Vds and Id during turn_off

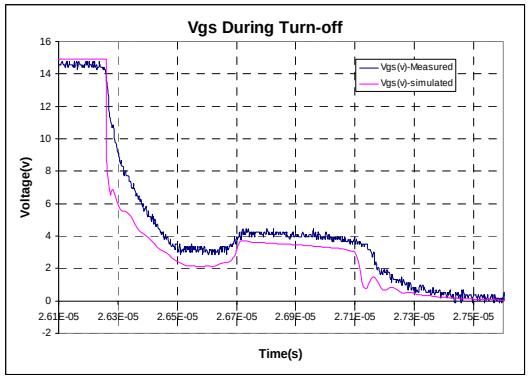

Figure 3: Comparison of Vgs during turn-off

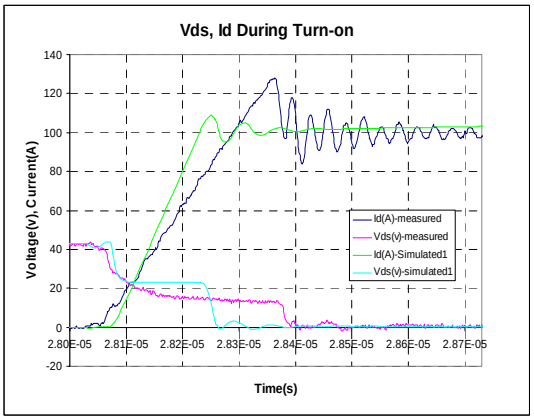

Figure 4: Comparison of Vds and Id during turn-on

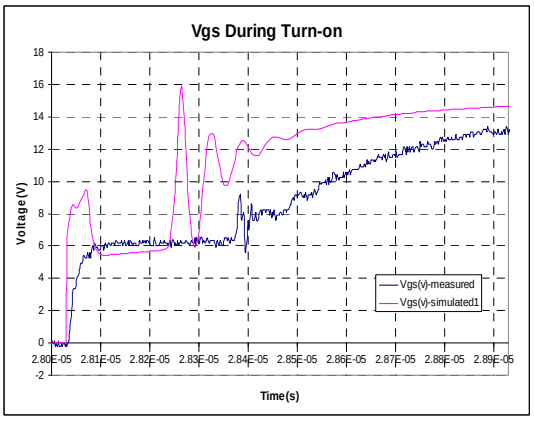

Figure 5: Comparison of Vgs during turn-on

Simulation of the turn-off process matches the measurement with very good accuracy. However, the di/dt doesn't correspond to the measurement in the simulation of the turn-on process. It should be noted that selection of the stray inductances greatly affects the switching characteristics. On the other hand, because the turn-off loss dominates the total loss, the accuracy of turn-off simulation is of more concern.

Section 2: Stray Inductance Effect on Switching Characterics

From the measurement shown in last section, the turn-off loss is 3 to 4 times greater than the turn-on loss. This result indicates that stray inductance generated by both the terminal connection and the profile of the PCB board affects the switching measurement.

During turn-on, the stray inductance stores energy. When the device turns off, the device dissipates the energy stored in the stray inductance, shifting the loss from turn-on to turn-off. This also implies that in any real system the turn-off loss dominates or at least is more important in the total loss.

Moreover, the waveform in the switching region may be misidentified as avalanche, which can yield the wrong solution. So a careful investigation is necessary to identify the difference between stray inductance effect and device avalanche.

To simplify the analysis, all the distributed stray inductances are lumped as one inductance shown in Figure 6.

As shown in Figure 7, during the control FET turn-on, the drain current I_D increases, which induces a voltage V_S in the stray inductance. Now, the voltage from drain to source of the control FET can be expressed as $V_{DS} = V_{BUS} - V_S - V_{Load}$, which means the voltage is smaller than without the stray inductance. This can also be explained from the energy point of view. During the turn-on, the stray inductance stores some energy and the turn-on loss is therefore lower.

The turn-off process is shown in Figure 8. The drain current decreases during the turn off and the induced voltage in the stray inductance therefore changes the polarity. So $V_{DS} = V_{BUS} + V_S - V_{Load}$ and the VDS of the control FET is higher than without the stray inductance. Consequently, during the turn-off, the stray inductance feeds the stored energy back to the device and the turn-off loss is therefore higher.

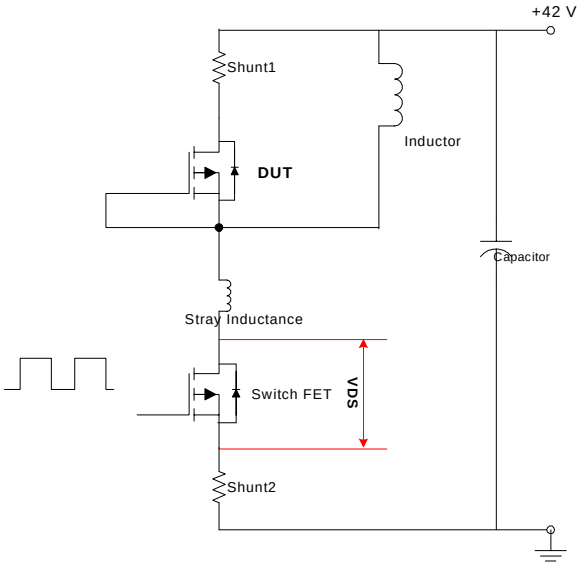

Figure 6: Circuit Diagram of the Two Pulse Test

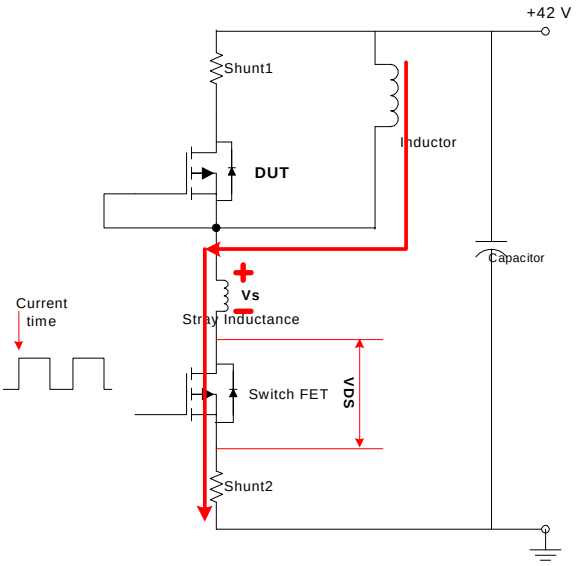

Figure 7: Transient Process During Turn-on

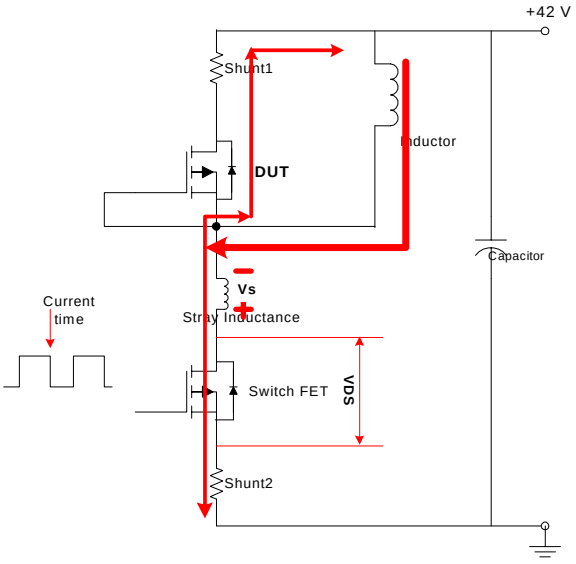

Figure 8: Transient Process During Turn-off

To prove the above analysis, MOSFETs with external inductances as shown in Figure 9 are put into the circuit. Figure 10 illustrates the difference between tests with an 80nH external inductance and no external inductance. The V_{DS} "hump" is higher, but the peak of V_{DS} is still lower than the avalanche voltage 75-80V.

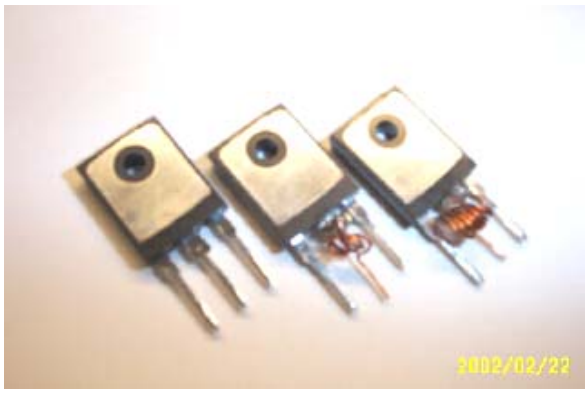

Figure 9: Terminal Connection of the external inductance

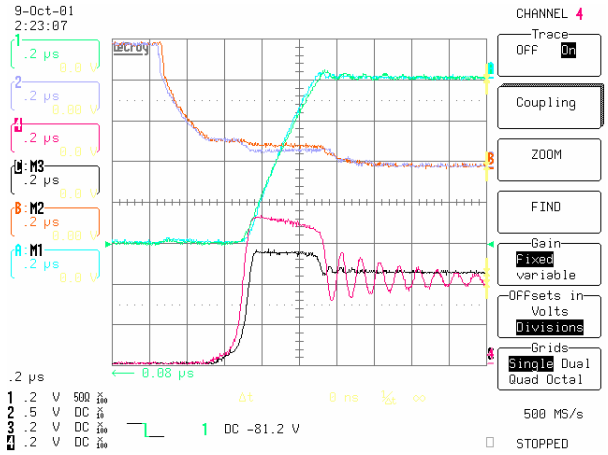

Figure 10: Channel 1 2 4 IRFP2907 with 80nH external inductance Vbus=42.7V
Channel A B C IRFP2907 with original 40nH stray inductance Vbus=42.7V

Channel 1: ID with an external inductance. 20A/div
Channel: 2: VGS with an external inductance. 5V/div
Channel 3: VDS with an external inductance. 20V/div
Channel 4: VDS with an external inductance. 20V/div
Channel A: ID with stray inductance. 20A/div
Channel B: VGS with stray inductance. 5V/div
Channel C: VDS with stray inductance. 20V/div

Section 3: Three-phase PWM Inverter with Passive Load

After validation of the device switching model, a system model using a three-phase inverter is simulated to examine the device characteristics in the system. The real system parameters are in table 1. The system model is shown in Figure 11. The three-phase inverter is shown in Figure 12. Each switch consists of two MOSFET in parallel.

The three-phase PWM generator is in Figure 13, which provides the right firing signals to the gates to build sinusoidal load voltage. 1 μS dead time is set between the control signals of the top and bottom MOSFETs on the same leg. Figure 14 gives the thermal model of one MOSFET with water-cooled heatsink. The thermal parameters are chosen from data sheet and measurement.

Table 2: System Information

Inverter Type	Three phase Inverter
Switch	Two IRFP2907 In parallel
Load	80 μH Inductor with 0.08 Ω resistance
DC Bus Voltage	42 V
Control Scheme	PWM open loop control
Heatsink	Water-cooled Aluminium

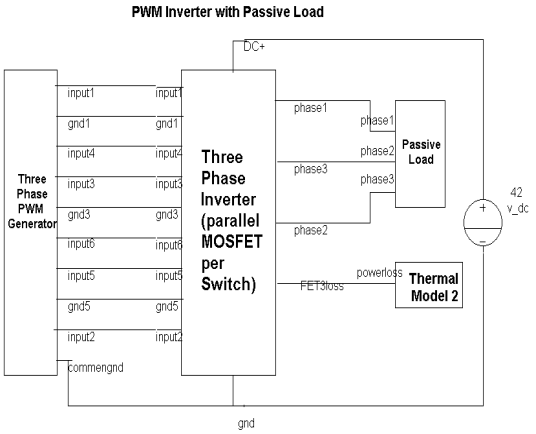

Figure 11: System Schematic

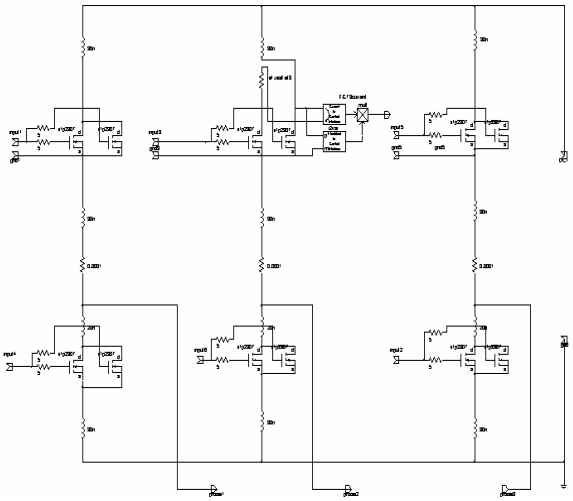

Figure 12: Schematic of the Inverter

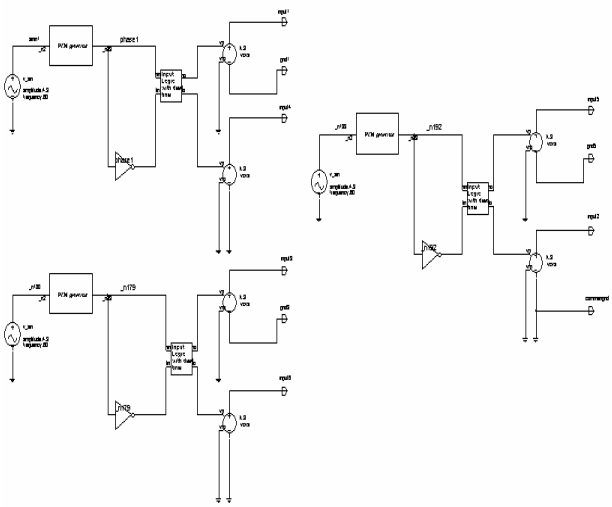

Figure 13: Schematic of the three-phase PWM Signal Generator

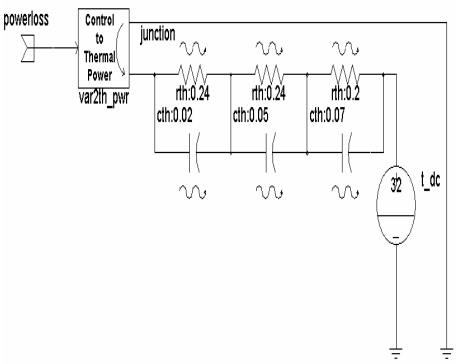

Figure 14: Schematic of the Thermal Model

In this simulation, a 30nH stray inductance is applied to all MOSFET's drain and source leads respectively. Figure 15 gives the simulated junction temperature with three phase currents shown in Figure 16. Figure 17 illustrates the simulated turn-off process including power loss. This is compared to measurements in Figure 18. Figure 19 and Figure 20 show simulated and measured results for the turn-on process respectively.

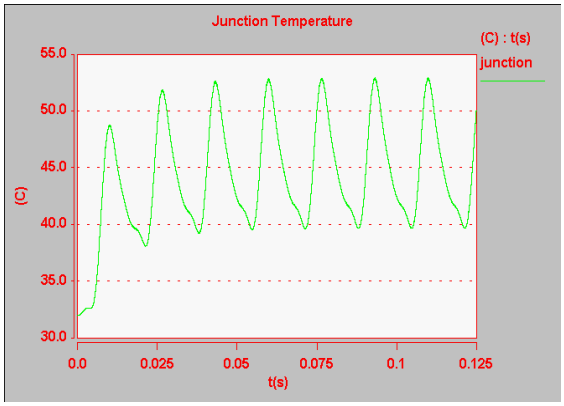

Figure 15: Tjunction Response of one MOSFET

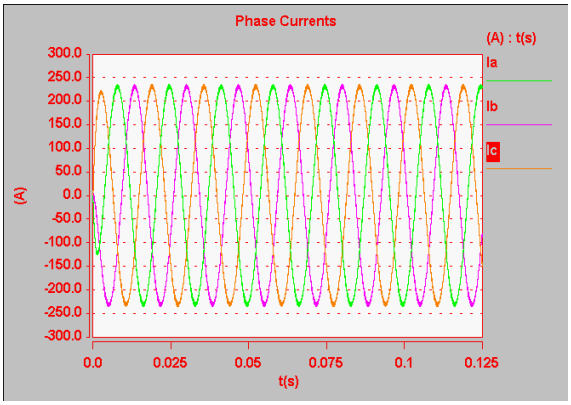

Figure 16: Phase current

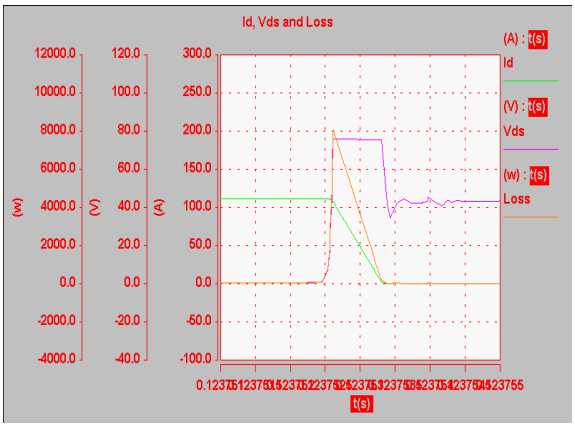

Figure 17: Vds and Id During turn-off (0.5 μS /div)

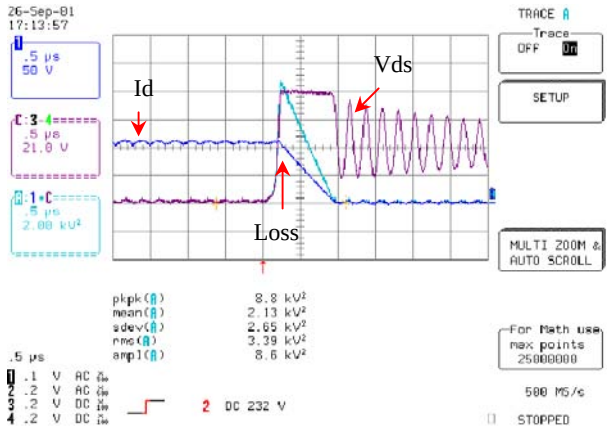

Figure 18: Measured Vds and Id During Turn-off

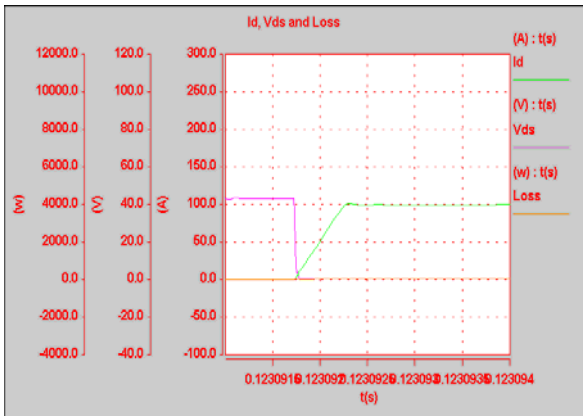

Figure 19: Vds and Id during Turn-on (0.5 μS /div)

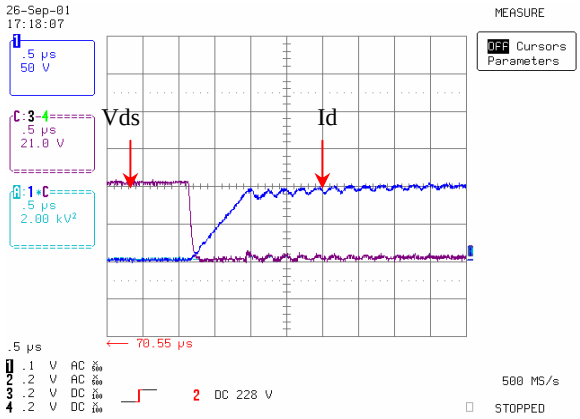

Figure 20: Measured Vds and Id during Turn-on

Simulation results match the measurements with very good agreement. There is a trade-off between simulation time and accuracy. If power loss is of concern, a comparatively bigger time step can be chosen to simulate the thermal response. If the voltage ringing is of more interest (e.g investigation of conductive EMI), a very small time step should be used.

III: Conclusion:

1: For device modeling, numerical simulation can simulate device switching characteristics with very good accuracy. The accuracy of the simulation depends on not only the device model but also the circuit stray inductance characterization.

2: The device behavioral model is validated by correlating simulation and measurements using a passive-load three-phase inverter system.

3: This work can be extended to evaluate power MOSFETs in other automotive applications such as ISA (Integrated Stator/Alternator), EPAS (Electric Assisted Power Steering), ABS (Anti-brake System) as well as IGBT and antiparallel diodes in inverter switching applications.

References:

[1]: "Guide to Writing MAST Templates", Analogy, Inc.

[2]: Giuseppe Massobrio, " Semiconductor Device Modeling with SPICE", Second Edition, 1993 by McGraw-Hill, Inc.