High Accuracy WEB Based Simulator for High Current Multi-phase DC-DC Power Converters

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Abstract:
With the evolutionary complexity of electronic circuits, reliance on computer-aided design tools (CAD) have surfaced in power design to help in device selection, system performance, and to expedite design completion. However, the design paradox is trying to minimize simulation time and inaccuracies while increasing circuit complexity. A new high-speed, high-accuracy simulation tool for high current multiphase converters will be presented along with actual measured data. By incorporating parasitics into the model and mathematically reducing them to a few equations with Mathcad, the Spice simulator demonstrated high accuracy and reduced simulation time.

I. Introduction

The need for simulation tools in power supply design has grown in recent years because of the increased complexity and time to market of electronic designs. Before the availability of circuit simulation tools, engineers had to perform very time consuming manual calculations to verify circuit performance. To circumvent the calculation rigors and satisfy design timeliness, some engineers opt to either redesign or modify preexisting designs, or go straight to a breadboard circuit to make performance verification measurements in the lab. This step is however costly in money and time when engineers go through iterative design rounds.

The reliance on computer-aided design tools (CAD) have become common place in power design to predicate device and system prototype performance, to simulate behavioral responses, and to expedite design completion. Spice simulation saves time by verifying component stress, component values and circuit connectivity before a breadboard is built. All values can be changed and evaluated in seconds. This gives the engineer the freedom to make lots of design iterations without the time and cost of changing components on a breadboard. Once the correct value is determined in a spice analysis, the engineer can go to the lab with confidence that the new value(s) will work. However, to construct a simulation model that satisfies accuracy, speed, convergence, and ease of use is not trivial.

This paper will describe a new high-speed, high-accuracy simulation tool for high current non-isolated DC-DC multiphase buck converters utilizing multi-chip modules. By incorporating the parasitics into the model and mathematically reducing them to a few equations with Mathcad, the Spice simulator was able to demonstrate a high level of accuracy while compressing the simulation time. As an example, a model that will show 7nS ringing on the rising edge of a switching waveform with 5uS of total simulation time would take 4 seconds (note: this is a complete 4 phase sync-buck converter with several nodes of current and voltage data available for viewing). A reiterative process of hardware testing, modifying the Spice net list, and utilizing a 1 nano-second time step, resulted in an accuracy of better than 5%. The circuit can be tested for step loads, changing input voltages, stability and steady state transient analysis. Both simulated and empirical data will be presented.

In addition to speed of execution and high accuracy, the simulation tool has the interface that makes it practical for design and optimization through the Internet. In selecting the input voltage, output voltage, frequency and load current as well as passive component values, the user quickly gets a very robust design that he can optimize on the dimensions of cost, efficiency, output ripple, transient response or size.

II. Limitations of Circuit Simulations

The main problem with simulation is minimizing inaccuracies <u>and</u> simulation time while increasing circuit construction complexity. This has caused engineers to modularize their circuits into smaller sub-circuits to expedite the simulation. However, the margin for error increases if the data is not correctly assimilated back into the complete design.

Accurate Spice models are usually very complex and therefore are very slow to simulate. Based on the assumed parameters, a model can provide extremely accurate or false data. To reduce simulation time, engineers simplify the simulation model by using ideal switches instead of accurate FET models, reducing the step time, or excluding parasitic

elements. But the simulation data fails to match the actual measured circuit waveforms - granular features such as ringing are usually absent, node and FET voltages are shown with vertical lines having infinite slopes, peak voltages are not conveyed, and the inaccuracies are considerable.

Similarly, including parasitic elements into the circuit model simulation is most difficult and time consuming for model construction. While neglecting parasitics increase simulation speed, care must be exercised in using these unreliable, inaccurate models.

The accuracy of most simulations will be within a 1% window if the exact values of components and parasitics are entered into the simulator although most components have a 1-30% tolerance (typically resistors are 1-5%, capacitors are 10-20% and the output inductors are 20-30% tolerance). When verifying component stress, every percent counts. Many modern designs push components to within 80-90% of their ratings. If a simulation had 20% accuracy, the user would not know if their design was being stressed or if it was operating within the 10-20% de-rating many companies adhere to.

For high current (20+A output) multi-phase converters used in gigahertz microprocessor applications, sophisticated, realistic simulations are necessary to mirror the power distribution losses and tight voltage regulation under high di/dt fluctuations. Consider two simulation scenarios where the waveforms are switching 20 amps at 12 volts with 100 nS time-step differences - the first simulation is showing 100nS to go from 12 volts to zero; the second simulation is showing about 5nS. This is a difference of 20:1. Over a 1uS period (1MHz) this is 10% or 0.5% of the period, or in terms of power, 12 watts versus 0.6 watts of losses. Such a wide deviation of power dissipated in a 363 mm^3 package could mean as much as product failure or longevity.

III. Spice Model Complexities

All spice circuits are comprised of individual spice models governed by mathematical representations (i.e. differential equations) of the actual physical devices and circuit. In solving the system of equations numerically through a time discretization method, such classical circuit simulation technique can be computationally intensive and expensive. Very complex circuits, therefore have a multiplicity of models within their net list. Some models are simple and simulate very quickly, a resistor is an example of this. However, complex nonlinear models are usually the slowest to simulate and cause the most problems in convergence. One problem is that all nodes must have a DC path to ground [3]. If there is no DC path to ground in any node in a circuit, most simulators cannot come up with a DC solution and therefore cannot give any steady state transient data, even though in the real world the circuit may work perfectly. By adding a high value resistor to ground at the node in question, the simulator can find the DC solution and therefore the transient solution. Time step issues can also cause errors. Too large of a time step will give inaccurate output waveforms similar to viewing a high frequency waveform on an oscilloscope with the bandwidth limit switch on. Too small of a time step can cause the simulator to take hours to complete just a few microseconds of data.

By taking a mathematical approach to simulation all of the convergence problems go away. The only thing you need to avoid is division by zero.

Model construction and optimization is also contingent upon the type of analysis you want to accomplish. Spice simulations are usually divided into AC analysis and Steady State Transient analysis. Average AC models, also known as state space models, characterize the operation of switching circuits using linear techniques, as opposed to switching techniques [1].

AC analysis generally removes all of the switching elements in a power converter. It is a small signal analysis in which all nonlinearities are linearized. The AC analysis calculates the small signal response of the circuit. Output variables such as magnitude, phase, real, or imaginary are recorded as a function of frequency, usually in the form of a bode plot. AC analysis is the fastest to simulate and usually needs no simplification to reduce simulation time.

The steady state transient analysis calculates the circuit response as a function of time over a predetermined time interval. The voltage at any node in the circuit and the current through any component or any connection can be recorded. The circuit can have several active time varying stimulus signals. Steady state transient analysis output is displayed similar to an oscilloscope, with a horizontal time base and vertical amplitude. This analysis mode is the most time consuming and mathematically intensive part of any circuit simulation. This is where the benefits of model simplification are the most needed.

In the standard Berkeley Spice 3 software, there is an arbitrary dependent source called a B element permitting instantaneous transfer function to be written as a mathematical expression [2].

Expressions for voltage and current can be any function of node voltages or currents. It can also be a variety of standard mathematical functions. This very powerful feature will enable simplification of the equations used in a spice net list circuit.

Below is an example of one line in a spice simulation circuit using this B element:

```
BK2 5 0 V=V(3)*({(R3*(VSET-
2.2988M*IOUT/P)+(RD+RP)*VIN)*R3/(RD+RP)/(R3+RD+RP)}
*(EXP((1-V(9))*{(RD+RP)/LP/FREQ})-1)-
+({-C1*(R3+R4)}*(-V(1)+V(2))-1)*(EXP((-
V(1)+V(2))*V(9)/{FREQ})-EXP((1-
V(9))*{(RD+RP)/LP/FREQ}))*V(14))/(
+(({C1*(R3+R4)}*(-V(1)+V(2))+1)*V(10)+({C1*(R3+R4)}*(-
V(1)-V(2))+1))
+*EXP((1-V(9))*{(RD+RP)/LP/FREQ})+({-C1*(R3+R4)}*(-
V(1)+V(2))-1)*EXP((-V(1)+V(2))*V(9)/{FREQ})*V(10)+
+({-C1*(R3+R4)}*(-V(1)-V(2))-1)*EXP((-V(1)-
V(2))*V(9)/{FREQ}) )+
+(1-V(3))*( V(6)*EXP(-V(9)/{C1*FREQ*(R3+R4)})+{R3*(VIN-
(VSET-2.2988M*IOUT/P))/(R3+RD+RP)}-V(4)*
+EXP(-V(1)*V(9)/{FREQ})*COS(V(2)*V(9)/{FREQ}) )/EXP(-
V(1)*V(9)/{FREQ})/SIN(V(2)*V(9)/{FREQ})
```

The plus at the beginning of each line represents a continuation of the preceding line, and in actuality represents one full line in a spice net list. Even though this appears to be a long line in Spice, this is actually a simplified equation that is used to describe one aspect of the 4 phase sync-buck converter.

Another method of speeding up a simulation is to use initial conditions. This is easy to do if you know what the initial conditions are, but if the external stimulus to the model changes, the initial conditions may also change. Spice allows you to calculate these values and pass them into the areas of the model to create an initial condition that is dependant on external stimulus. Without initial conditions, it may take several minutes for the model to attain steady state. This allocates time and computational expenditure, and further requires the user to analyze the data to determine the inception of the equilibrium.

IV. Model Construction & Optimization

In optimizing the spice model we have to first determine what nodes of data are important and what level of accuracy is required. Fewer nodes and less accuracy means a faster simulation. We will set the limit on the accuracy to 5% of the actual measured waveforms; this will be determined largely by the time step dependent on the highest frequency in the circuit. The necessary nodes of data in a typical buck converter are:

1. Input voltage and current
2. Output voltage and current
3. Switch node voltage
4. Current in the output inductor.

5. Current through top "Control" FET
6. Current through Bottom "Sync" FET

A spice circuit can be generated in several ways. A schematic circuit entry interface can be used to enter the components and create a net list. While this is the easiest for the novice user, it is usually the slowest to simulate because you exercise the least control. The second method is to enter a circuit the old fashioned way by entering numbers in a net list representing the components used. This is more difficult because the schematic diagram is not displayed on the screen as you make changes - the schematic diagram with the nodes shown must be referenced through each step. The third method of entering a circuit is using equations to represent each node in the circuit. This is the fastest and most difficult type of circuit to enter into spice.

Each node is identified by constituent relations to generate a correct output value. The change in inductor current is a function of the voltage across it and the time this voltage is applied. The duty cycle is largely dependant on the input and output voltages and slightly dependant on the losses through the circuit. The input and output capacitors' voltages are dependant on the current going into or out of them. The output ripple voltage is dependant on the output inductor's AC current and the output capacitor's ESR. Parasitic elements are also added to these equations at this point. Variables are used for parasitics as well as the actual component values so changes to the model are fast and easy.

Note that some nodes are more complex than others. The switch node has some ringing on the rising edge of the waveform. This is caused by the drain source capacitance of the Q2 FET, the parasitic inductance between this FET and the Q1 FET and finally the dv/dt of the Q1 FET when it turns on. See Figure 1. This ringing waveform has to be superposed to the square waveform caused by turning on the Q1 FET. The addition of these two waveforms has to be timed to happen at the correct time, so as to represent the actual turn on of the switch and the parasitic ringing of the switching node. See Figure 2 Switch node and figure 2a Switch node simulation.
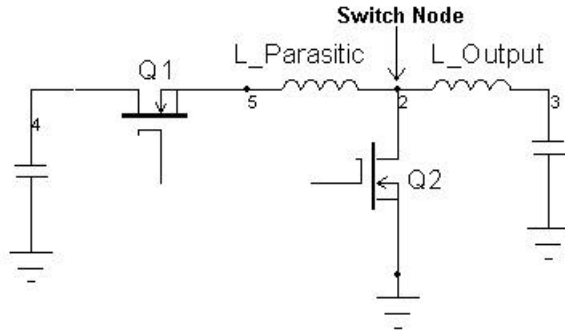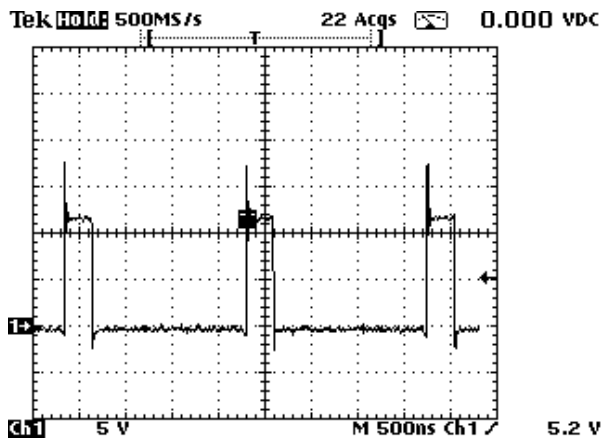
Figure 1. Circuit diagram for parasitic inductance

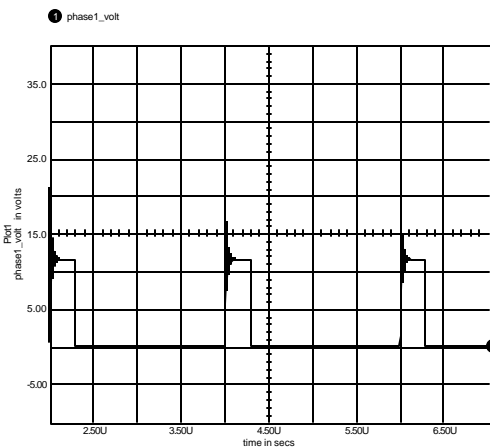**Figure 2.** Switch node.

Figure 2a. Switch node simulation.

Once an equation is written, it needs to be verified and then simplified. Verification is an iterative process of changing the parameters passed to the model (input voltage, output voltage, load current and frequency), running the simulation, verify it matches an actual circuit and then repeating this process to verify model integrity. Simplification involves creative writing of and/or combinations of the

equations to accelerate simulation times. Math CAD has several functions that work well for this. As an example, the simplified equation for the output voltage ripple in this model is the superposition of several different equations calculated separately along with supplied constraints:

BVOUT 31 0 V={VSET-
2.2988M*LOAD/PX}+V(5)+V(13) + +V(20)+V(27).

This is a simplified equation relying on variables passed to it from Spice. VSET is the output voltage set point, 2.2988M*LOAD/PX is the droop voltage that is dependant on load current and number of phases, V(5)+V(13)+V(20)+V(27) are the output ripple voltages that are superposed to create the proper output voltage waveform with output ripple. See figures 3 and 3a for a comparison of actual versus simulated waveforms. The amplitude of the measured waveform varies due to the unequal current sharing between phases, the model was set for a balance between the 4 phases.
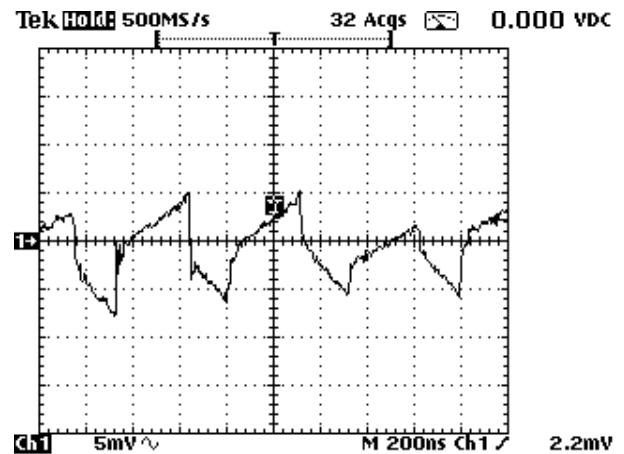

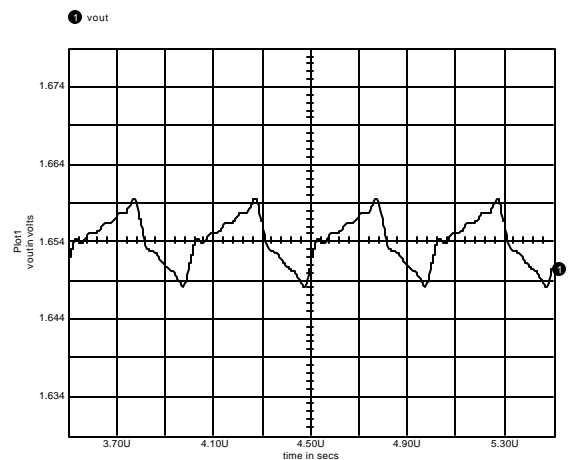**Figure 3.** Actual measured output ripple waveform.

Figure3a. Simulated output voltage waveform.

All of the equations for all of the nodes that are to be displayed in the output of the simulation have to be incorporated into the spice net list. Spice can process these equations very quickly and as a user changes the external conditions (input or output voltage and load current or circuit component values) the output waveforms remain within 5% of actual measured values. Through an iterative model verification process – comparing actual waveforms to the simulator's output, confidence in the model accuracy was assured.

Parasitic elements are critical to the design engineer. The ring frequency is a potential source of EMI generation and the peak of the ringing could damage low voltage components if not controlled correctly. Figure 4 "Switch node ringing" and figure 4a "Switch node ringing simulation" show how accurate the simulation is to the real measured waveform on a reference design board. Many simulators leave out this very important information.
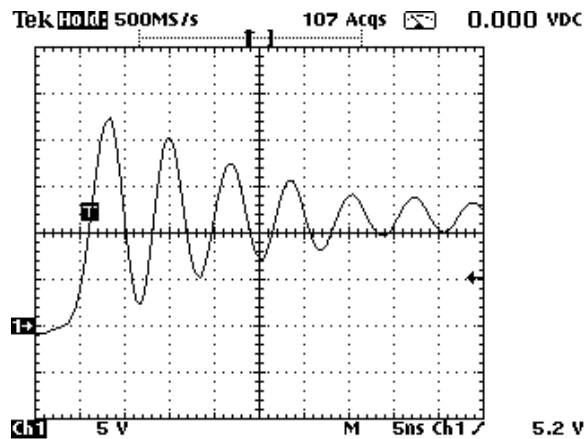

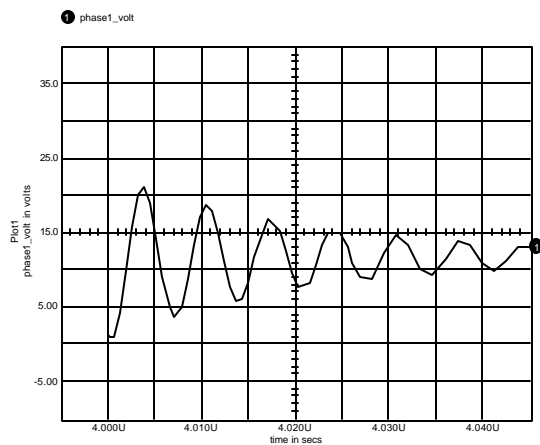**Figure 4** Switch node ringing.

Figure 4a Switch node ringing simulation

The reference design and the simulation are based on a multi-chip module that includes two FET transistors, a Schottky diode, a ceramic capacitor and a high speed gate drive IC. There are several manufacturers of these devices, but the International Rectifier part number iP2001 was selected due to its exceptionally high current rating and generous safe operating area. The benefit of using this type of module is that the parasitic inductance and capacitance is controlled within the package and thus the layout will not affect the switching performance.

Comparing the new high speed model to a standard reference board assembly allowed the comparison of waveforms at different switching frequencies and different passive component values resulting in the high accuracy that is required by today's engineers. Time was also reduced from 39 seconds on the first spice model to 4 seconds on the final optimized model without compromising any waveform fidelity. This processing time was measured on a 1.8GHz Pentium 4 PC.

V. Circuit Simplification Process

Circuit simplification using Mathcad is a very complex and time consuming process when used to simplify a complete converter. This involves creative writing of and/or combinations of the equations to accelerate simulation times [4]. To aid in understanding this process, an analysis of a simple textbook type "RC" circuit will be presented. See figure 5.
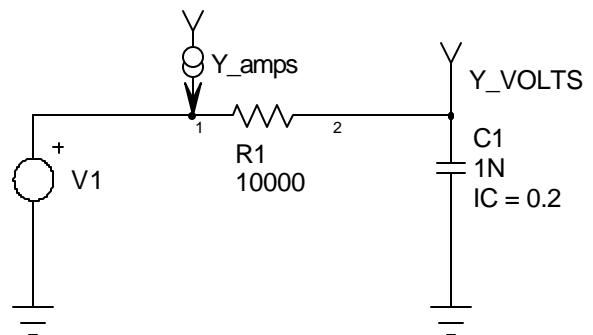

Figure 5 Simple textbook type "RC" circuit.

If instead we wanted to feed SPICE with the mathematical equivalent of the circuit – we must do some analysis of the circuit and write closed-form equations that describe its operation. These equations can be of any complexity and later superposed to create desired or correlated output.

The equations used here are those common to MathSoft's Mathcad, but the syntax is easily understood and can be applied to other software or programming languages.

C1=1nF
Vinpk=1
Duty=0.25
F=200KHz

The input source would be defined as required by the application, for this example, as follows:

$$t := 0, \frac{1}{20 \cdot F} .. \frac{1}{F}$$

$$Vin(t) = if\left(t < \frac{duty}{F}, Vinpk, 0\right)$$

The final equation that the software program (either Spice or Mathcad) will "solve" is shown in figures 6 & 7.

Assigned circuit values for this example are:
R1=10K

$$Vout(t) := if\left[t < \frac{duty}{F}, \left[Vinpk + Vinpk \cdot \frac{\left[1 - exp\left[\frac{(-1 + duty)}{F \cdot R \cdot C}\right]\right]}{\left(-1 + exp\left(\frac{-1}{F \cdot R \cdot C}\right)\right)} \cdot exp\left(-\frac{1}{R \cdot C} \cdot t\right)\right], Vinpk \cdot \frac{\left(1 - exp\left(\frac{duty}{F \cdot R \cdot C}\right)\right)}{\left(-1 + exp\left(\frac{-1}{F \cdot R \cdot C}\right)\right)} \cdot exp\left(-\frac{1}{R \cdot C} \cdot t\right)\right]$$

Figure 6. V_{out} Final Equation

$$Iin(t) := if\left[t < \frac{duty}{F}, \frac{-Vinpk}{R} \cdot \frac{\left[1 - exp\left[\frac{(-1 + duty)}{F \cdot R \cdot C}\right]\right]}{\left(-1 + exp\left(\frac{-1}{F \cdot R \cdot C}\right)\right)} \cdot exp\left(-\frac{1}{R \cdot C} \cdot t\right), \frac{-Vinpk}{R} \cdot \frac{\left(1 - exp\left(\frac{duty}{F \cdot R \cdot C}\right)\right)}{\left(-1 + exp\left(\frac{-1}{F \cdot R \cdot C}\right)\right)} \cdot exp\left(-\frac{1}{R \cdot C} \cdot t\right)\right]$$

Figure 7. I_{in} Final Equation

These equations are the continuous time functions that are required in this example, the output voltage and input current transient results for the "RC" circuit.

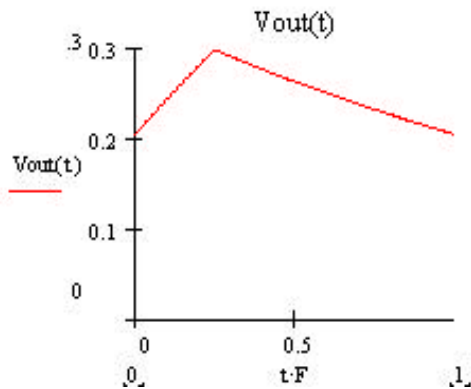The resulting plots from Mathcad are shown in figures 8 and 9.
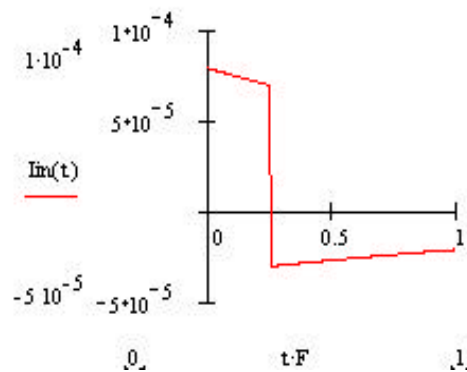

Figure 8. Output Voltage plot.

Figure 9. Input current plot

These equations may be put back into the Spice circuit analysis program as B elements to reduce the simulation time. Although you may never do this for a simple "RC" circuit, it is necessary on very complex circuits to reduce simulation times, especially when used on a WEB based simulation tool.

VI. WEB Interface and Interaction

Integrating this multi-phase model with the Internet medium provides a presence of design ubiquity for high current multi-phase buck converters. The simulation interface allows the engineer to experiment, investigate, and correlate component modifications and operating conditions with simulated behavioral results in seconds. See Figure 10.
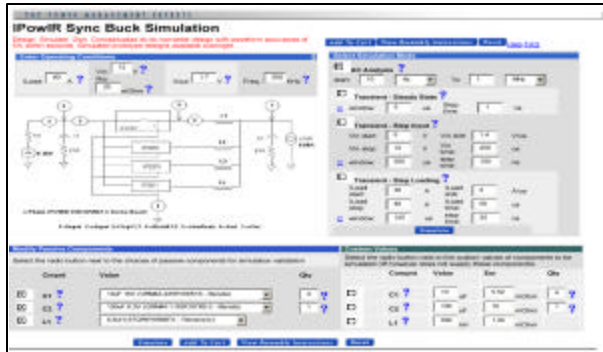

Figure 10. Sync Buck Simulation Page

The interface between the user and the simulator is designed to be seamless and transparent to the user. Phase recommendation is based on inputted parameters of: input voltage, output voltage, load current, and switching frequency. Four forms of simulation modes are provided: AC Analysis, Transient Steady State, Transient Step Input, and Transient Step Loading. See Figure 11. Time steps and total simulation time can be adjusted to zoom in on particular waveform features.
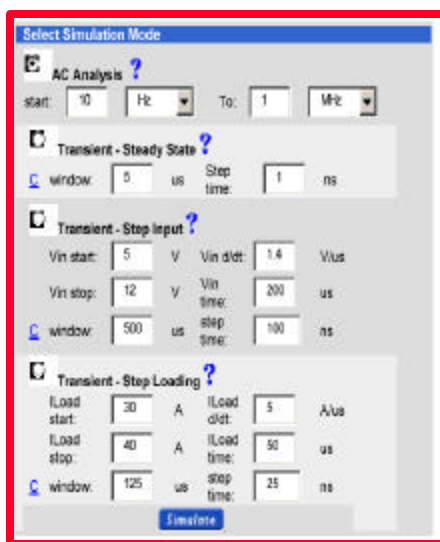

Figure 11. Simulation Mode

To provide design flexibility, the simulation also supports and upholds a 5% accuracy for all standard components for input/output capacitors and inductors. See Figure 12.

Figure 12. Design Modification/Customization

The following parameters can be changed in the simulation:
1. Input and output voltage.
2. Input capacitor's value and ESR.
3. Output capacitor's value and ESR.
4. Output inductor's inductance and winding resistance.
5. The switching frequency.
6. Input resistance between the DC source and the converter.
7. Load current
8. 2, 3 or 4 phase sync-buck DC-DC converter.

Once parameters are selected and a simulation is executed, a new browser window pops up in a matter of seconds displaying the data. The data can be drilled into to reveal rise and fall times, switch node ringing and changing currents.

VII. Prototype Fulfillment

By integrating e-commerce capability to the final step of the simulation design process, the engineer is equipped to fully verify his prototype buck converter design overnight. Fully tested and assembled reference boards, along with any customized components are delivered to expedite the entire multi-phase power converter design process. The reference designs provide flexible customizations to specific user applications - designers can realize changes to cost, efficiency, output ripple, transient response, output voltage and frequency based on external passive components chosen and modeled by the web simulator. By combining high-speed simulation, a mature design platform and overnight fulfillment, the design engineer is presented with a coherent end-to-end design solution for integration into the overall system for evaluation.

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VIII. Conclusion

The synergistic coupling of design simulation with the Internet media provides a powerful combination of rapid solution prototyping and experimentation. International Rectifier has demonstrated a new integrative approach to designing high current (20-80A) multi-phase buck converters by simplifying design complexity with an iPOWIR iP2001 module, correlating flexible component selection to overall topology performance, and realizing design performance via a high-speed (4 sec), high-accuracy (+/-5%) simulation tool. By incorporating non-idealized FET models and parasitics into the model and mathematically reducing them to a few equations with Mathcad, the Spice simulator demonstrates high integrity of accuracy while compressing computational time. The circuit simulates waveforms for step loads, changing input voltages, stability, and steady state transient analysis. By integrating the Spice simulator with Internet interactivity, users can simulate behavioral responses, expedite design completion, and optimize on the dimensions of cost, efficiency, or size. Simulated and customized designs are available within 24 hours for immediate performance validation.

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[3] Intusoft, "IsSpice4 User's Guide"
[4] Kehinde Omolayo of Magnetico Inc