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INTEGRATED POWER DEVICES SIMPLIFY AN EMBEDDED DC-DC POWER SUPPLY

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Abstract

A new class of integrated power devices has been developed to simplify embedded dc-dc power supply designs. The paper includes comparison with existing discrete/co-package solutions and a new methodology that has been developed in how integrated devices are being designed, specified, tested and qualified.

The paper also details how treating integrated devices as power supply modules instead of co-packaged components significantly improves the system performance and long-term reliability, and reduces the design complexity for the embedded dc-dc power supplies.

1. Introduction

Power levels and power density requirements continue to increase for many types of end equipment such as personal computers, servers, network and telecom systems. Today's embedded processors such as CPUs, ASICs and network processing units (NPUs) require lower voltages, better regulation and higher current levels, driving the need for power semiconductors to deliver high efficiency at higher switching frequencies.

For embedded designs, the major obstacles to design success are solution design time, reliability and PCB area. This has lead to the introduction of many types of integrated power devices. However, due to the lack of testability, these devices can only be tested and specified primarily for their dc parameters. Without being tested as a switching power supply in production, the integrated power devices are no more than several discrete dice co-packaged together. Their reliability and performance can be potentially lower than discrete solutions unless die level probe tests include the same level of ac tests similar to discrete devices such as driver ICs and power MOSFETs.

As shown in Fig. 1, for a 12V dc-dc synchronous Buck converter, the switching loss rapidly becomes dominant at high frequencies. The high switching frequency performance of a simple co-packaged device can vary significantly from part to part, due to non-guaranteed variances in ac characteristics. In most embedded dc-dc systems, there is no easy way of testing a discrete power converter efficiency in production, therefore, it is very important to have a guaranteed power supply type performance in order to meet the stringent system-level reliability requirements.

iPOWIR™ Technology devices have been introduced to specifically address the above concerns. The iPOWIR platform can easily accommodate many discrete passive components, especially bypassing capacitors, which makes testing similar to a power supply possible at frequencies up to 1MHz or beyond. By specifying and guaranteeing the power losses at 500kHz or 1MHz, the accumulating effect of all dc and ac parameters are captured, and a reliability performance close to brick power supply modules can be achieved with a discrete type design at lower cost.

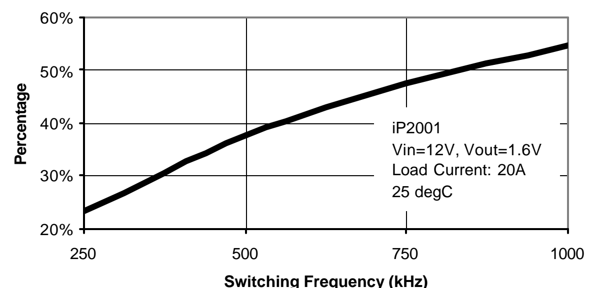

Fig. 1: iP2001 Switching Loss vs Frequency

2. Module Design

Existing iPOWIR devices are built upon high temperature PCB substrates, which interface to system motherboards through solder balls in a BGA format as shown in Fig. 2. [1] [2]

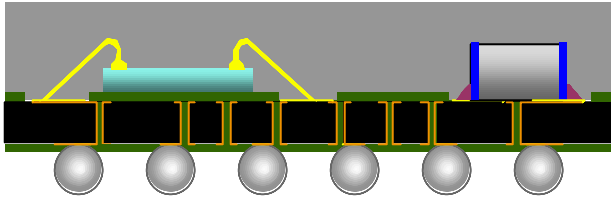

Fig. 2: Side View of iPOWIR Module

iP2002 will be used as an example through the remaining discussion.

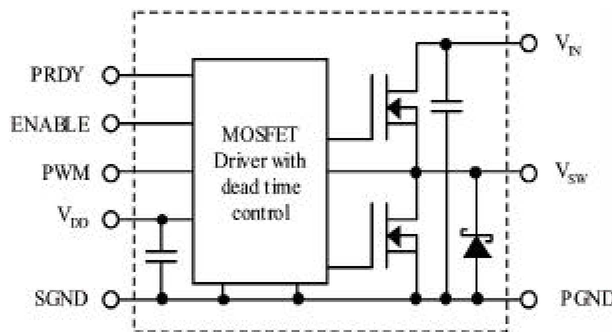

Fig. 3: iP2002 Schematic Block Diagram

A block diagram for iP2002 is shown in Fig. 3. iP2002 is a synchronous buck power block used in single or multiphase applications. It contains a driver, an upper side MOSFET, a lower side MOSFET, a Schottky diode, and most importantly, the bypassing capacitors for the dc input and the driver.

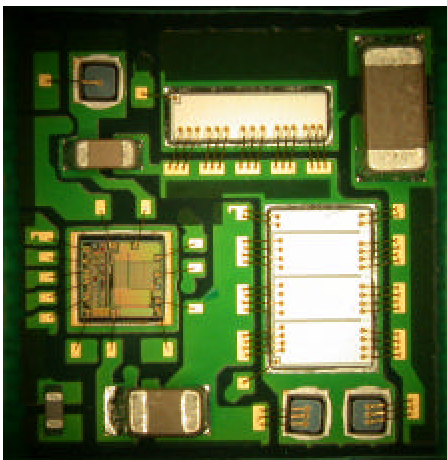

Fig. 4: iP2002 without Plastic Mold Cap

The inside view of iP2002 is shown in Fig. 4. Except for the wire bonding process, the components are attached through a traditional SMT process. The platform is so flexible that there is essentially no limitation on what kind of or how many discrete passive components can be placed inside the module.

Adding passive components including bypassing capacitors inside the modules offers several important advantages:

1. The parasitic inductance in the gate driver area and the current loop in the power train is minimized.

2. The critical switching electrical characteristics are frozen inside the module, and will not change with motherboard layout variations. As such, the layout sensitivity is minimized.

3. The bypassing capacitors reduce the module sensitivity to the contact resistance and parasitic impedance of the production test socket. They also enable the iPOWIR modules to be tested as power supplies, resulting in a guaranteed 100% tested power loss, running at the switching frequency in intended applications.

3. Module Testing

The power loss of a high switching frequency synchronous Buck converter is a complex function of all component parameters and interactions among them.

1. Rds(on) of upper and lower FETs
2. Gate charge of upper and lower FETs
3. Gate resistance of upper and lower FETs
4. Threshold voltage of upper and lower FETs
5. Output capacitance of upper and lower FETs
6. Gate charge ratio of the lower FET
7. Qrr and Vf of body and Schottky diodes
8. Driver output current
9. Driver output impedance
10. Driver dead time delays
11. Bypass capacitor ESR
12. Parasitic impendence due to system PCB layout variations
13. Others

Typically, 20-50% tolerance of the above parameters is considered normal. When switching frequency is close to 1MHz, the Rds(on) related conduction loss becomes less significant for a 12Vin synchronous buck. It is clear that dc parameter testing alone is not enough to guarantee the module performance. Even when all ac parameters are tested, which is very difficult if not impossible for co-package modules, the accumulative effect of component interactions cannot be easily predicted.

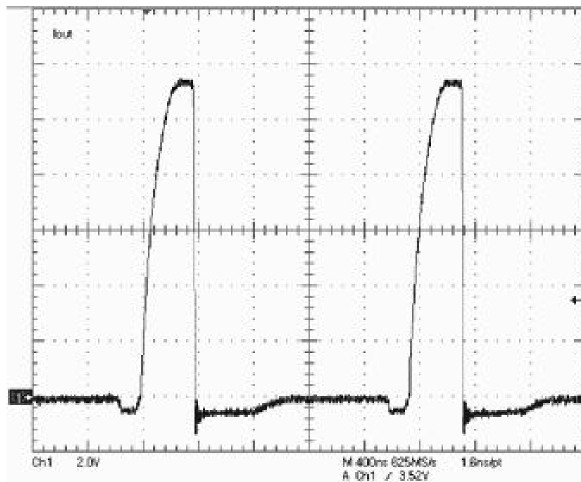

Fig. 5: Switch Node Waveform of a Module Rejected by Power Loss Tester

Fig. 5 depicts the switch node waveform of a defective module running at 500kHz with 15A output current. The time scale is 400ns/div. The power loss of this module is significantly outside the test limit. The obvious problems of this module are the extremely slow turn-on speed of the upper FET and the large dead times for both leading and trailing edges of the switching node waveform. However, all dc parameters of this module are well within the limits. If parts like this cannot be caught in production and are shipped to customers in the embedded dc-dc applications, the system-level reliability will become questionable.

Facing the above challenges, one solution is to significantly tighten the dc and ac parameters of all internal components so that the worst case combination will still produce acceptable performance. Besides the test issues and yield losses, the latest power MOSFET processes are unfortunately incompatible with this approach. Tolerances tighter than +/-20% for Rds(on) and gate charge parameters may cause entire MOSFET lots to be outside the production test limits, hence putting customers at risk of a production line down situation, as supply cannot be guaranteed.

A solution to solve this problem is to 100% test the modules as a switching power supply in production. Having integrated bypassing capacitors and other passive components becomes essential in enabling this test method. A multi-layer PCB based substrate was chosen

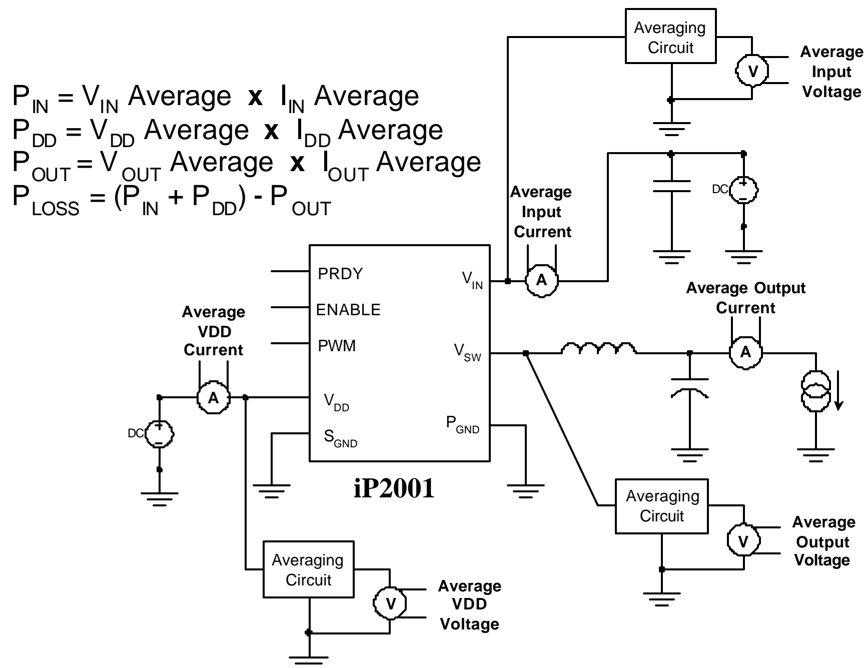

Fig. 6: Power Loss Test Setup

because of its capability and flexibility in accommodating these critical passive components.

The production power loss tester is shown in Fig. 6. The iP2002 module is placed inside a test socket with pogo pins making contact to the solder balls. The input voltage (V_{IN}) and the switch node voltage (V_{SW}) are sensed through Kelvin contacts by using separate pogo pins on the module side. The PWM signal is generated through a microcontroller with precise frequency and duty cycle. The power loss test time is limited to about 20ms to avoid variations due to heating effects.

In the datasheet, the maximum power loss is specified for a 125°C device temperature. If the device is tested at different ambient temperatures, a power loss correlation analysis is performed.

4. Datasheet Rating System

Once the power loss is tested and guaranteed, it greatly simplifies the embedded power system design. [3] With known maximum power loss, the efficiency and thermal performance of the system can be predicted and optimized prior to the completion of motherboard layout. However, in order to accomplish this goal, another piece of information is needed, which is the thermal resistance of the device. Unfortunately, for a integrated device, there is more than one heat generating component inside the package, and depending on the operating conditions, the hot spots move from one die to another. There is no easy way to test and guarantee power losses for each of these components. Therefore, a new way of specifying a discrete component was devised using a methodology common in the power supply world. A safe operating area (SOA) method was used together with maximum power loss to allow rating of the parts and facilitate ease-of-use.

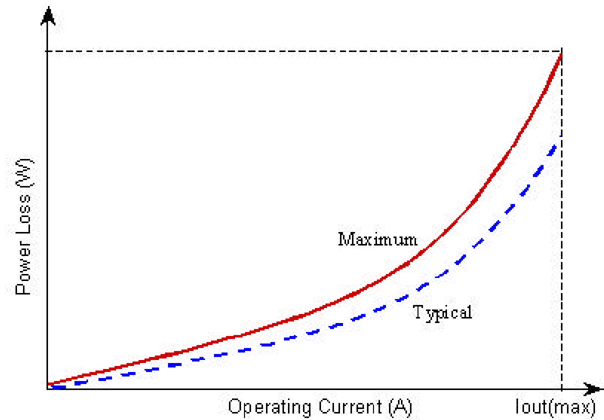

Fig. 7: Maximum Power Loss rating

The maximum/typical power loss graph is illustrated in Fig. 7 for a given switching frequency, namely 500kHz or 1MHz. The safe operating area (SOA) is illustrated in Fig. 8. Both of these are worst-case scenarios with the device temperature assumed to be 125°C.

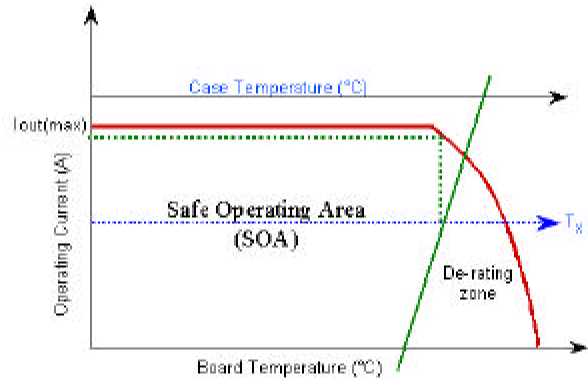

Fig. 8: Safe Operating Area

The presented SOA method incorporates power loss and thermal resistance information in a way that allows one to solve for maximum current capability in a simplified graphical manner. It incorporates the ability to solve thermal problems where heat is drawn out through the printed circuit board and the top of the case. [4]

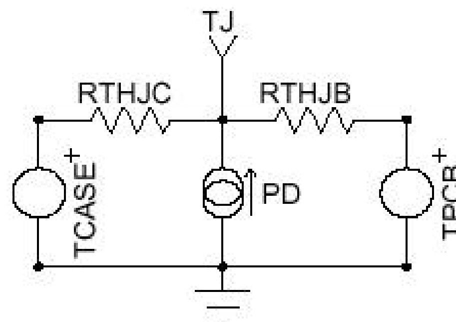

Fig. 9: Two-Branch Thermal Model

A two-branch device thermal model is shown in Fig. 9. T_{CASE} is the highest temperature of the device case surface. T_{PCB} is defined to be the highest temperature on the top side PCB around the device with 1mm clearance.

The de-rating zone in Fig. 8 is derived from the maximum power loss curve by keeping device junction temperature (Tj) at 125?C. The maximum current is truncated due to constraints other than power dissipation and junction temperature. The Tx axis location is predetermined by device thermal characteristics, and its value is defined as follows:

$$T_x ? \frac{\{R_{?jc} ? T_{pcb} ? R_{?jb} ? T_{case}\}}{(R_{?jc} ? R_{?jb})} \qquad (1)$$

Once the T_{CASE} and T_{PCB} are known, the maximum output current can be obtained graphically by using following procedure:

1) Draw a line from Case Temp axis at T_{CASE} to the PCB Temp axis at T_{PCB}.

2) Draw a vertical line from the T_X axis intercept to the SOA curve.

3) Draw a horizontal line from the intersection of the vertical line with the SOA curve to the Y-axis. The point at which the horizontal line meets the Y-axis is the SOA current.

In cases where the operating conditions are different from the standard test conditions, normalized curves are provided to adjust the power loss and SOA.

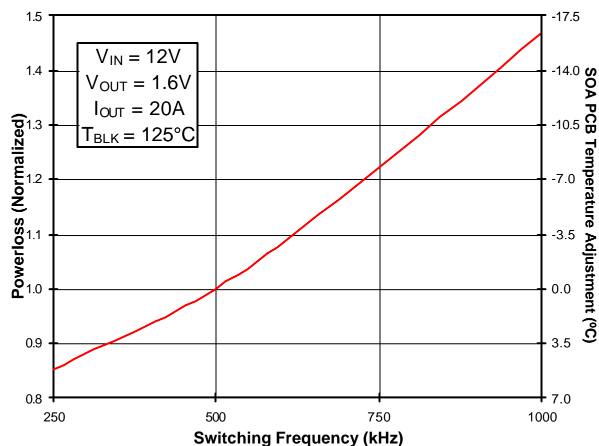

Fig. 10: Normalized Curve for Switching Frequency

A normalized curve for the switching frequency is shown in Fig. 10. Similar curves adjusting for input voltage, output voltage and output inductor are provided in the datasheet.

5. Qualification

Qualification of iPOWIR devices required many of the discrete standard qualification tests such as temperature cycling, THB, high temperature storage, power cycling, HTOL, ESD, shock and vibration.

However to enable realistic application-like reliability testing, the need for a new method to test these devices for power cycling and HTOL was required. The BGA package technology was originally designed for digital ICs with low power dissipation. The iP2002 has been specified to dissipate as much as 11W in an 11mm x 11mm footprint. The thermo-mechanical effect of this power density has to be well understood. The power cycling test shown in Fig. 11 is designed for this purpose.

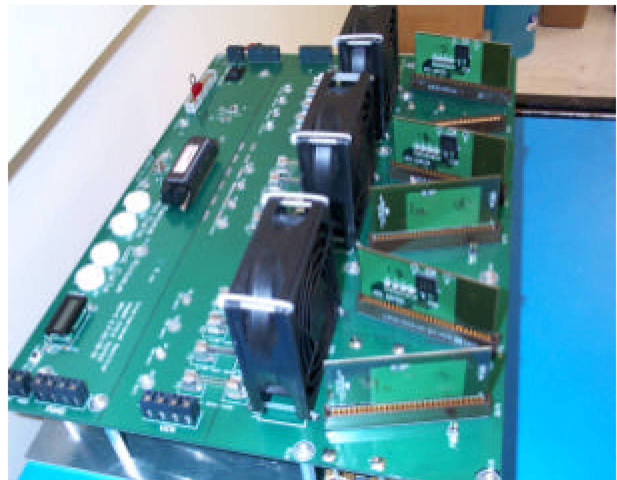

Fig. 11: Power Cycling Tester

iPOWIR devices are mounted on individual DUT cards, which have a thermal choke design to prevent heat from dissipating efficiently into the PCB. These devices are switched on with rated output current for a short duration, i.e. 40 seconds, until the rise of device temperature is 100°C, then

the devices are turned off and fans are turned on to cool the junction temperature back to ambient in 30 seconds. The important thing is to self-heat the devices in a minimal amount of time in order to create maximum temperature gradient and induce thermo-mechanical stresses. By conducting this test, the thermal stress on various material interfaces can be studied. All devices have to be cycled at least 10,000 times with less than 10% power loss shift in order to be qualified. This is the same number of cycles as discrete components but at much higher actual operating currents and also with true application-like switching. Power cycle testing is more representative to the real world applications, and more difficult to pass than the standard temperature cycle test. This is because with temperature cycling the entire device including the internal components change in temperature uniformly, minimizing the effect of coefficient of thermal expansion (CTE) induced stresses. However, with power cycling the temperature gradients are much higher, due to the switching elements creating localized hotspots within the device, and as such creating much greater thermo-mechanical stresses.

HTOL uses a similar test configuration. Instead of being turned on and off, the devices are on constantly with self-heating to maintain the junction temperature at 125°C. The devices switch like power supplies with rated output current. All devices have to be continuously running for at least 1000 hours with less than 10% power loss shift in order to be qualified.

HTOL is also used for on-going reliability and life testing to establish the demonstrated MTBF hours.

As shown in table 1, more than 14 million accumulative MTBF hours have been demonstrated for iPOWIR devices.

6. Conclusions

A new class of integrated power devices have been developed and discussed. The philosophy behind the product concept is presented. A new methodology has been developed to design, test, rate, and qualify these devices. Treating them as power supplies instead of co-packaged devices results in iPOWIR devices significantly simplifying embedded dc-dc power supply designs with reliability levels matching full functional power supply modules at lower cost.

References

[1] AN-1028: Recommended Design, Integration and Rework Guidelines for International Rectifier's iPOWIR Technology BGA Packages
[2] AN-1029: Optimizing a PCB Layout for an iPOWIR Technology Design
[3] AN-1030: Applying iPOWIR Products in Your Thermal Environment
[4] AN-1047: Graphical Solution for Two-Branch Heatsinking Safe Operating Area

Demonstrated Reliability for Q4'2002 - Data is limited. More update every quarter

Device temperaure: 90 °C

Device Number	Lots	Samples	Failures	Device-hours HTOL	Device-hours Use	@ 60% UCL FITs	@ 60% UCL MTBF (hours)
iP2001+iP1001 +iP2002+iP1201	24	870	0	2,438,899	13,424,202	68.26	14,650,603

Table 1: Demonstrate Life and MTBF Hours