High Accuracy Web Based Simulator for High Current Multi-phase DC-DC Converters

D. Barsell and E. Wu

International Rectifier

El Segundo, CA 90245, USA

Abstract:

With the evolutionary complexity of electronic circuits, reliance on computer-aided design tools have surfaced to help in device selection, system performance, and to expedite design completion. However, the design paradox is trying to minimize simulation time and inaccuracies while increasing circuit complexity. This paper will describe a high-speed, high-accuracy simulation tool for high current DC-DC multiphase buck converters using multi-chip modules. A review of the capabilities of the improved Spice model and actual comparisons to a high current power converter design will be given.

I. Introduction

The need for simulation tools in power supply design has increased in recent years because of the greater complexity and time to market of electronic designs. Before the availability of circuit simulation tools, engineers had to perform very time consuming manual calculations to verify circuit performance. By incorporating the parasitics into the spice model and mathematically reducing them to a few equations with Mathcad, the Spice simulator was able to demonstrate a high level of accuracy while compressing the simulation time. As an example, a model that will show 7nS ringing on the rising edge of a switching waveform with 5uS of total simulation time would take 4 seconds to simulate (note: this is a complete 4 phase sync-buck converter with several nodes of current and voltage data available for viewing). A reiterative process of hardware testing, modifying the Spice net list, and utilizing a 1 nano-second time step, resulted in an accuracy of better than 5%. The circuit can be tested for step loads, changing input voltages, stability and steady state transient analysis. Both simulated and experimental test data will be presented.

II. Limitations of Circuit Simulation & Spice Model Complexities

The main problem with simulation is minimizing inaccuracies <u>and</u> simulation time while increasing circuit construction complexity. This has caused engineers to modularize their circuits into smaller sub-circuits to speed up the simulation process. However, the margin for error increases if the data is not correctly assimilated back into the complete design.

Accurate Spice models are usually very complex and therefore are very slow to simulate. Based on the assumed parameters, a model can provide extremely accurate or false data. To reduce simulation time, engineers simplify the simulation model by using ideal switches instead of accurate FET models, reducing the step time, or excluding parasitic elements. But the simulation data fails to match the actual measured circuit waveforms - important features such as ringing are usually absent, node and FET voltages are shown with vertical lines having infinite slopes, peak voltages are not conveyed, and the inaccuracies are considerable.

For high current (20+A output) multi-phase converters used in gigahertz microprocessor applications, sophisticated, realistic simulations are necessary to mirror the power distribution losses and tight voltage regulation under high di/dt fluctuations. Consider two simulation scenarios where the waveforms are switching 20 amps at 12 volts with 100 nS time-step differences - the first simulation is showing 100nS to go from 12 volts to zero; the second simulation is showing about 5nS. This is a difference of 20:1. Over a 1uS period (1MHz) this is 10% or 0.5% of the period, or in terms of power, 12 watts versus 0.6 watts of losses. Such a wide deviation of power dissipated in a 363 mm^3 package could mean as much as product failure or longevity. In this example, the simulation time is also increased by one hundred times.

All spice circuits are comprised of individual spice models governed by mathematical representations of the actual physical devices and circuits. In solving the system of equations numerically through a time discretization method, such classical circuit simulation technique can be computationally intensive and time consuming.

Model construction and optimization is also contingent upon the type of analysis you want to accomplish. Spice simulations are usually divided into AC analysis and Steady State Transient analysis. Average AC models, also known as state space models, characterize the operation of switching circuits using linear techniques, as opposed to switching techniques [1].

AC analysis generally removes all of the switching elements in a power converter. It is a small signal analysis in which all nonlinearities are linearized. The AC analysis calculates the small signal response of the circuit. Output variables such as magnitude, phase, real, or imaginary are recorded as a function of frequency, usually in the form of a bode plot. AC analysis is the fastest to simulate and usually needs no simplification to reduce simulation time.

The steady state transient analysis calculates the circuit response as a function of time over a predetermined time interval. The voltage at any node in the circuit and the current through any component or any connection can be recorded. The circuit can have several active time varying stimulus signals. Steady state transient analysis output is displayed similar to an oscilloscope, with a horizontal time base and vertical amplitude. This analysis mode is the most time consuming and mathematically intensive part of any circuit simulation. This is where the benefits of model simplification are the most needed.

III. Model Construction & Optimization
In optimizing the spice model we have to first determine what nodes of data are important and what level of accuracy is required. Fewer nodes and less accuracy means a faster simulation.

Each node is identified by constituent relations to generate a correct output value. The change in inductor current is a function of the voltage across it and the time this voltage is applied. The duty cycle is largely dependant on the input and output voltages and slightly dependant on the losses through the circuit. The input and output capacitors' voltages are dependant on the current going into or out of them. The output ripple voltage is dependant on the output inductor's AC current and the output capacitor's ESR.

Note that some nodes are more complex than others. The switch node has some ringing on the rising edge of the waveform. This is caused by the drain source capacitance of the Q2 FET, the parasitic inductance between this FET and the Q1 FET and finally the dv/dt of the Q1 FET when it turns on. See Figure 1. This ringing waveform has to be superposed to the square waveform caused by turning on the Q1 FET. See Figure 2 Switch node and figure 2a Switch node simulation.
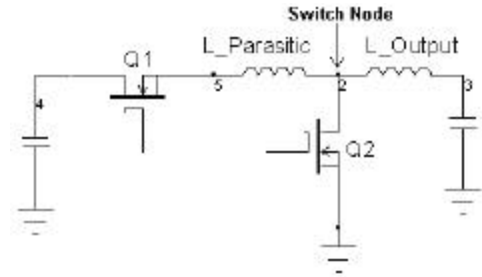

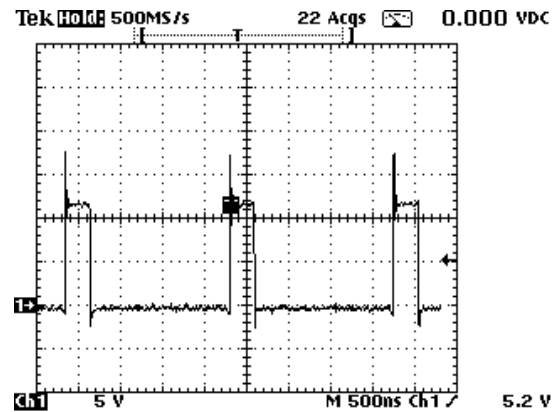**Figure 1**. Circuit diagram for parasitic inductance
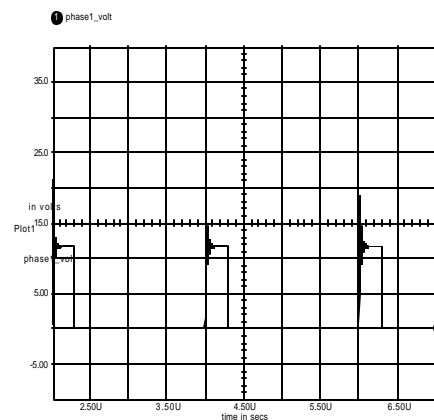

Figure 2. Switch node.

Figure 2a. Switch node simulation.

Once an equation is written, it needs to be verified and then simplified. Verification is an iterative process of changing the parameters passed to the model (input voltage, output voltage, load current and frequency), running the simulation, verify it matches an actual circuit and then repeating this process to verify model integrity. Simplification involves creative writing of and/or combinations of the equations to accelerate simulation times. Math CAD has several functions that work well for this. As an example, the simplified equation for the output voltage ripple in this model is the superposition of several different equations calculated separately along with supplied constraints:

BVOUT   31   0   V={VSET-2.2988M*LOAD/PX}+V(5)+V(13)+V(20)+V(27)
.

All of the equations for all of the nodes that are to be displayed in the output of the simulation have to be incorporated into the spice net list. Spice can process these equations very quickly and as a user changes the external conditions (input or output voltage and load current or circuit component values) the output waveforms remain within 5% of actual measured values. Through an iterative model verification process – comparing actual waveforms to the simulator's output, confidence in the model accuracy was assured.

Parasitic elements are critical to the design engineer. The ring frequency is a potential source of EMI generation and the peak of the ringing could damage low voltage components if not controlled correctly. Figure 3 "Switch node ringing" and figure 3a "Switch node ringing simulation" show how accurate the simulation is to the real measured waveform on a reference design board. Many simulators leave out this very important information.
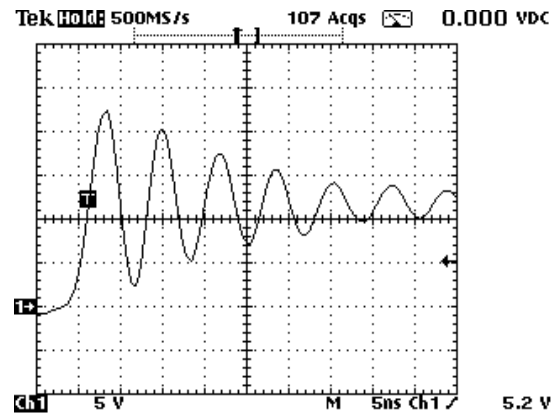

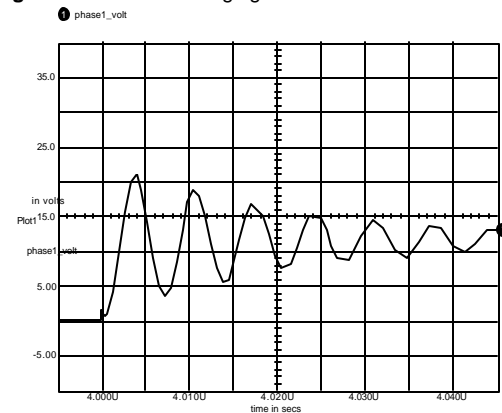**Figure 3.** Switch node ringing.

Figure 3a. Switch node ringing simulation

The reference design and the simulation are based on a multi-chip module that includes two FET transistors, a Schottky diode, a ceramic capacitor and a high speed gate drive IC. There are several manufacturers of these devices, but the International Rectifier part number iP2001 was selected due to its exceptionally high current rating and generous safe operating area. The benefit of using this type of module is that the parasitic inductance and capacitance is controlled within the package and thus the layout will not affect the switching performance.

Comparing the new high speed model to a standard reference board assembly allowed the comparison of waveforms at different switching frequencies and different passive component values resulting in the high accuracy that is required by today's engineers. Time was also reduced from 39 seconds on the first spice model to 4 seconds on the final optimized model without compromising any waveform fidelity. This processing time was measured on a 1.8GHz Pentium 4 PC.

IV. Circuit Simplification Process

Circuit simplification using Mathcad is a very complex and time consuming process when used to simplify a complete converter. This involves creative writing of and/or combinations of the equations to accelerate simulation times [2]. To aid in understanding this process, an analysis of a simple textbook type "RC" circuit will be presented. See figure 5.
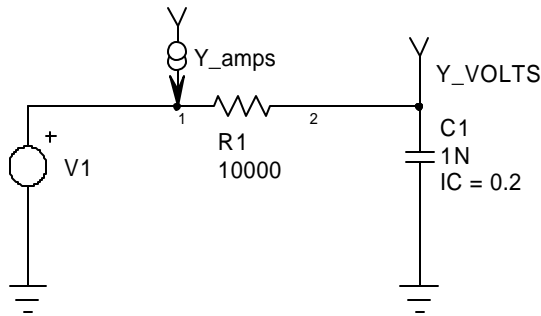

Figure 5 Simple textbook type "RC" circuit.

If instead we wanted to feed SPICE with the mathematical equivalent of the circuit – we must do some analysis of the circuit and write closed-form equations that describe its operation. These equations can be of any complexity and later superposed to create desired or correlated output.

The equations used here are those common to MathSoft's Mathcad, but the syntax is easily understood and can be applied to other software or programming languages.

The input source would be defined as required by the application, for this example, as follows:

$$Vin(t) = if\left(?t ? \frac{duty}{F} ? Vinpk ? 0 ?\right)$$

Assigned circuit values for this example are:
R1=10K
C1=1nF
Vinpk=1
Duty=0.25

F=200KHz $t ?? 0 ? \frac{1}{20?F} ?? \frac{1}{F}$

The final equation that the software (either Spice or Mathcad) will "solve" is shown in figures 6 & 7.

$$Vout(t) := if\left[t ? \frac{duty}{F} ? \left[Vinpk + Vinpk ? \frac{\left[1 - exp\left[\frac{(-1 + duty)}{F?R?C}\right]\right]}{\left(-1 + exp\left(\frac{-1}{F?R?C}\right)\right)} ? exp\left(-\frac{1}{R?C}?t\right)\right] ? Vinpk ? \frac{\left(1 - exp\left(\frac{duty}{F?R?C}\right)\right)}{\left(-1 + exp\left(\frac{-1}{F?R?C}\right)\right)} ? exp\left(-\frac{1}{R?C}?t\right)\right]$$

Figure 6 V$_{out}$ Final Equation

$$Iin(t) := if\left[t ? \frac{duty}{F} ? \frac{-Vinpk}{R} ? \frac{\left[1 - exp\left[\frac{(-1 + duty)}{F?R?C}\right]\right]}{\left(-1 + exp\left(\frac{-1}{F?R?C}\right)\right)} ? exp\left(-\frac{1}{R?C}?t\right) ? \frac{-Vinpk}{R} ? \frac{\left(1 - exp\left(\frac{duty}{F?R?C}\right)\right)}{\left(-1 + exp\left(\frac{-1}{F?R?C}\right)\right)} ? exp\left(-\frac{1}{R?C}?t\right)\right]$$

Figure 7 I$_{in}$ Final Equation

These equations are the continuous time functions that are required in this example, the output voltage and input current transient results for the "RC" circuit. The resulting plots from Mathcad are shown in figures 8 and 9.
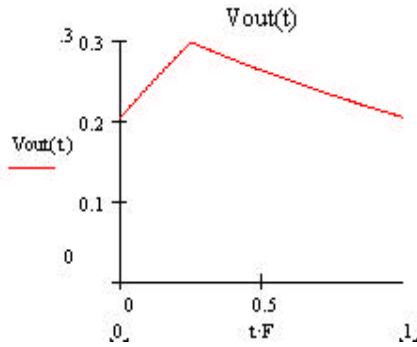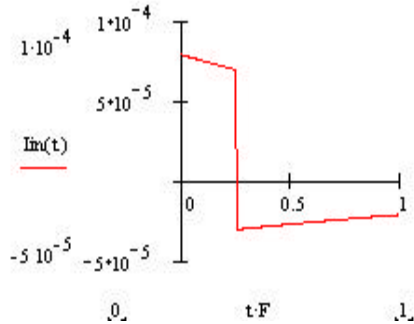
Figure 8. Output Voltage plot

Figure 9. Input current plot

These equations may be put back into the Spice circuit analysis program as B elements to reduce the simulation time. In the standard Berkeley Spice 3 software, there is an arbitrary dependent source called a B element permitting instantaneous transfer function to be written as a mathematical expression [3]. This very flexible feature is what has enabled the simplification of the equations used in this spice net list circuit. Although you may never do this for a simple "RC" circuit, it is necessary on very complex circuits to reduce simulation times, especially when used on a WEB based simulation tool.

V. WEB Interface and Interaction

Integrating this multi-phase model with the Internet medium provides a presence of design ubiquity for high current multi-phase buck converters. The simulation interface allows the engineer to experiment, investigate, and correlate component modifications and operating conditions with simulated behavioral results in seconds. See Figure 10.
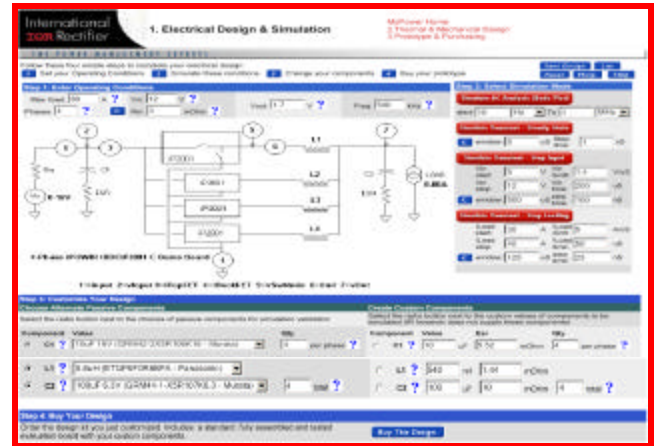

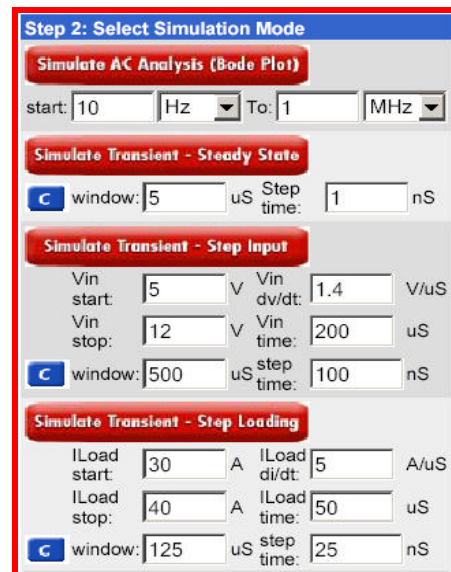**Figure 10.** Sync Buck Simulation Page

Figure 11. Simulation Mode

The interface between the user and the simulator is designed to be seamless and transparent to the user. Phase recommendation is based on inputted parameters of: input voltage, output voltage, load current, and switching frequency. Four forms of simulation modes are provided: AC Analysis, Transient Steady State, Transient Step Input, and Transient Step Loading. See Figure 11. Time steps and total simulation time can be adjusted to zoom in on particular waveform features. To provide design flexibility, the simulation also supports and upholds a 5% accuracy for all standard components for input/output capacitors and inductors. Several parameters can be changed in the simulation. Once parameters are selected and a simulation is executed, a new browser window pops up in a matter of

seconds displaying the data. The data can be drilled into to reveal rise and fall times, switch node ringing and changing currents. Designs may also be saved for future reference.

VI. Prototype Fulfillment

By integrating e-commerce capability to the final step of the simulation design process, the engineer is equipped to fully verify his prototype buck converter design overnight. Fully tested and assembled reference boards, along with any customized components are delivered to expedite the entire multi-phase power converter design process. By combining high-speed simulation, a mature design platform and overnight fulfillment, the design engineer is presented with a coherent end-to-end design solution for integration into the overall system for evaluation.

VII. Conclusion

The synergistic coupling of design simulation with the Internet media provides a powerful combination of rapid solution prototyping and experimentation. International Rectifier has demonstrated a new integrative approach to designing high current (20-80A) multi-phase buck converters by simplifying design complexity with an iPOWIR iP2001 module, correlating flexible component selection to overall topology performance, and realizing design performance via a high-speed (4 sec), high-accuracy (+/-5%) simulation tool. By incorporating non-idealized FET models and parasitics into the model and mathematically reducing them to a few equations with Mathcad, the Spice simulator demonstrates high integrity of accuracy while compressing computational time. The circuit simulates waveforms for step loads, changing input voltages, stability, and steady state transient analysis. By integrating the Spice simulator with Internet interactivity, users can simulate behavioral responses, expedite design completion, and optimize on the dimensions of performance, efficiency, size or cost. Simulated and customized designs are available within 24 hours for immediate performance validation. See: http://mypower.irf.com for details.

References:
[1] Steven M. Sandler, "SMPS Simulation with SPICE 3", McGraw-Hill Professional Publishing; ISBN: 0079132278
[2] Kehinde Omolayo of Magnetico Inc
[3] University of California, Berkeley Department of Electrical Engineering and Computer Sciences "Berkeley Spice 3"