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A Whole New Way to Design On-Board Single-Phase Synchronous Buck Converters for Hi-End Network Systems

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Abstract

Power levels and power density requirements continue to increase for many types of end equipment, like personal computers, servers and networks, as systems are expected to pack more and more functionality inside them. This is driving the requirement for power semiconductor solutions to deliver improved electrical and thermal efficiency at reduced solution footprint, enabling the operation of next generation processors and ASICs. This paper will introduce an all new way to design on-board power, using BGA style packages integrating many power semiconductor devices, including a full function PWM and driver IC, control and synchronous power MOSFETs, schottky diodes and several passive devices for up to15A operation that will offer many benefits versus alternate solutions available today, and provide a standard building block solution for system power architecture.

Introduction – How power supply design can help obtain extra system bandwidth.

Many end systems are demanding more efficient power conversion for a variety of different reasons. More efficient power conversion solutions need to deliver less losses, reduce board space, simplify solution implementation, power more demanding loads and offer overall solution flexibility to address many different operating conditions. In so many instances, the power supply design is left until the last moment, and wrongly assumed that the power solution is a "given". Also, with the ever-increasing density of on-board functionality, the current requirements are going up, making converter design even more challenging. For instance, for network systems, increased bandwidth capabilities and improved quality of service (QoS) are key to enable faster and more reliable data transfer across the switch fabric known in general terms as the backbone of the internet. In order to achieve the demands for improved performance, there are many things to consider, and power supply design is certainly a non-trivial exercise, and warrants close attention to maximize performance.

In simple terms, the power supply designer is faced with the following design issues:

- Power architecture & design complexity.
- Electrical efficiency.
- Thermal efficiency & heat generation.
- Power supply real estate.
- Time to market.

Each of these issues, if addressed adequately, can impact the overall bandwidth capability of the end system, and this paper will explain how this can be done for hi-end data transfer systems, and what specific power considerations need to be understood.

Network power architecture.

Most network systems, whether it be core switchers, routers or some other transport device in the core switch fabric of the network infrastructure, tend to follow a similar power architecture. There is usually a 48V bus voltage that is provided along a backplane of a rack mounted cabinet. Inside the cabinet are an array of cards, that have a mulitude of application specific ICs (ASICs) and network processor units (NPUs) on-board. Each of these components needs to be powered in order for them to work and to process all of the data at increasing bandwidths. Figure 1 illustrates a typical network system architecture.

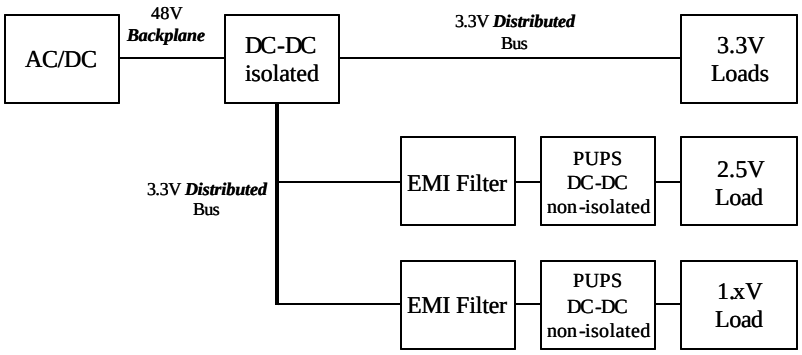


Figure 1 – Typical network power system architecture.

The power is delivered from the backplane at 48V down to the required operating voltage of the ASIC, NPU or other load. The operating voltages will tend to vary, but the majority seems to be 3.3V currently with a future trend toward 2.5V. Some applications will run directly from the 3.3V, and others will run from a lower voltage that requires a point-of-use power supply (PUPS) stage. The point-of-use power supply is usually located as close to the load as possible, to achieve tight regulation. Electrical isolation is needed between the 48V supply and the point-of-use power supplies, so usually a one-stage isolated 'brick' module is used for supplying power for the 3.3V rail. There are also some power system architectures that buck the 48V down to an intermediate voltage, like 12V, before stepping that voltage down very close in proximity to the load, in order to minimize transmission losses.

Of course, if the load is particularly demanding in terms of operating current, then by bussing the power at low voltage, like 3.3V or lower, the current has a distribution loss along the copper tracks on the board proportional to i^2R, where i is the current, and R is the track resistance. The preference is to bus high power at higher voltage to reduce the distribution losses. Less copper can then be used for on-board distribution in this case.

There are always several other rails aside from the 3.3V rail that need to be generated for specific loads, like 2.5V, 1.8V, 1.5V, 1.XV, etc. The system architect has to decide whether to use separate isolated solutions from 48V down to each individual operating voltage, or whether to use non-isolated converters from the 3.3V rail down to the lower operating voltages. There are efficiency trade offs that will effect the

decision, but there are also other factors that effect the decision. A non-isolated solution can come in two different guises, one of which is a totally discrete solution, which needs to be designed and implemented extremely well in order to get the best performance, but may give the ultimate in design flexibility, and the other is an "off the shelf" module, that gives ultimate in ease-of-design but offers little by way of design flexibility. The discrete solution can achieve relative cost and board space savings when compared to non-isolated module solutions. The key to additional bandwidth in network systems is power solution space reduction. Space reduction enables additional real estate on the line cards so that additional feature rich ASICs or NPUs can be populated, which will translate to increased bandwidth.

So, the designer's final power architecture decisions are based on several factors that determine overall board space utilization, overall efficiency and power density and ease of design. Isolated module efficiency varies depending upon manufacturer, but can be as high as 90% converting directly to the operating voltage from 48Vin. However, this is undesirable for every independent operating voltage due to space constraints and cost, so the module is generally only used to buck down to the most common highest current operating voltage rail. The other operating voltages will be dual stage, converted from the output of the module, with a slight trade-off in efficiency but advantages in space and cost.

Electrical Efficiency.

There have been many discussions regarding optimizing synchronous buck converters for best efficiency. With reference to the power loss equations in Fig 2 (and ref. 1), there are many things to consider. Any loss in efficiency can be thought of as heat dissipation onto the motherboard or into the ambient environment, which is non-desirable and therefore critical that the PUPS are fully optimized.

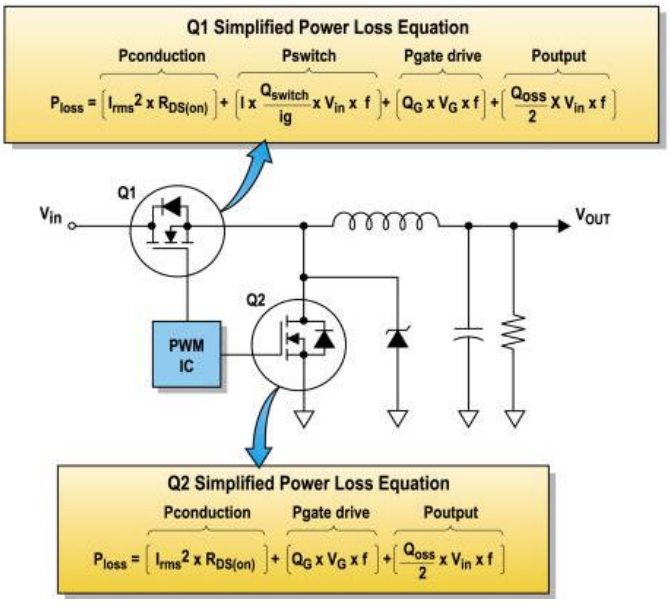


Figure 2 – Simplified power loss equations for synchronous buck circuits.

Of course, when designing this circuit with discrete devices, the selection of each component becomes critical, since the power loss equation is dependent on several critical device parameters, including on-state resistance $R_{DS(on)}$, switching charge Q_{sw}, output charge Q_{oss}, etc. This can be coupled with the parasitic effects that will vary with each different circuit board layout of the power components. These parasitic effects can cause noise in the circuit and degrade efficiency. Also proper selection of the control FET versus the synchronous FET is required, per the two separate formulae in figure 2. This design procedure can take a large amount of design resource and time. Also, since selection of the PWM & driver IC, capacitors and inductor can all also effect efficiency the design effort is further compounded. The PWM & driver IC has to be externally configured to operate at varied frequencies, duty cycles, dead-time set-points, etc and each item will effect the overall performance and efficiency of the circuit. The inductor and capacitors will effect regulation, ripple characteristics and transient response of the circuit, as well as performance of the circuit. Furthermore, by choosing non-optimized MOSFETs, undesired operating conditions can occur, like Cdv/dt induced turn-on of the MOSFETs, which can lead to short circuit conditions and large shoot through currents, that will create catastrophic failures or worsened thermal performance. Cdv/dt effects can be seen in figure 3, and can be caused if devices are chosen without the proper consideration to FET charge ratios. If the time is taken though, the ultimate in electrical efficiency can be obtained.

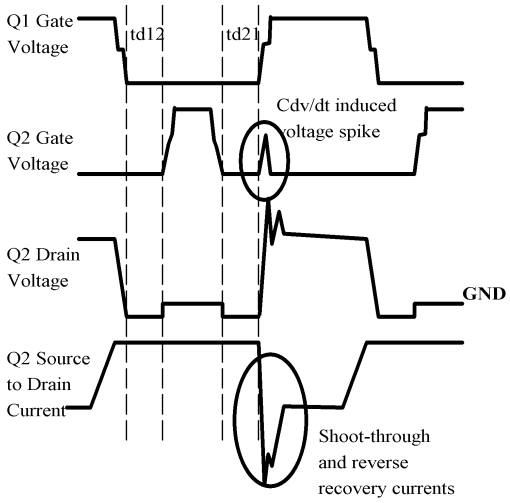


Figure 3 – Cdv/dt induced turn-on

Thermal Efficiency

The electrical efficiency defines the difference between the amount of power that is required at the input for a given output power for the load. The wasted energy that does not get supplied to the load is dissipated into the board or the air. The power dissipated into the board in watts, will heat the board proportional to it's thermal capacity rating in °C/W, i.e. for a 1°C/W board, if 4W is dissipated, a 4°C temperature rise will be measured on the board.

There are a few ways in which to impact the overall thermal efficiency of the power solution. The first is to use excess thermal mass for the power solution, by adding additional heatsinking or extra copper layers or copper area on the PCB for dissipating heat. This is costly, and adds significant board real estate for the overall solution. Another method is to use fan cooling, which does provide a good method of regulating overall ambient temperatures in an enclosed environment.

Another aspect of thermal performance is the temperature de-rating of the solution. Some

solutions will have a performance de-rating curve, similar to the one shown in figure 4.

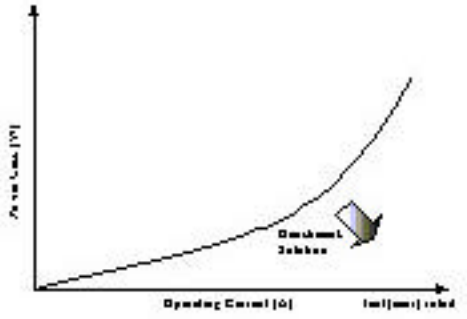


Figure 4(a) Power loss curve

Figure 4(b) SOA curve

There are cases where the ambient and/or PCB temperatures are regulated to a certain temperature. The power solution will be required to operate at a specified current, which will correspond to a power loss in watts, as shown in figure 4a. The board has a known thermal capacity ($R_{th(board)}$) in °C/W, and is regulated to a steady state temperature, but once the additional power loss from the power supply is added to the board, there will be an attributed local temperature rise on the board, equal to :

$$T_{pcb(new)} = T_{pcb(regulated)} + \{P_{loss} * R_{th(board)}\}$$

Reduced power loss is most desirable in order to not violate the maximum board temperatures of the maximum power solution temperature.

Selecting the optimal power solution can be complex unless it has been thermally optimized already. By deriving the new temperature of the board, from the above equation, a correlation back to the safe operating area of the power solution is required, as shown in figure 4b. This shows the maximum current rating of the power solution at elevated board temperatures, and whether the solution can or cannot be used. The solution with the least de-rating at elevated board temperatures is obviously desired.

Power Supply Real Estate

Space that can be saved for the power stage is incremental space that could be used for additional ASICs or NPUs, which would give the opportunity to result in additional bandwidth for the system. However, finding a power solution that provides the levels of power density required is difficult. Integrated solutions will nearly always beat discrete solutions in total board space, due to the removal of many discrete level semiconductor packages (SOIC, etc) in preference of silicon die level integration or monolithic solutions. Silicon die level integration and advanced packaging methods will improve power density and therefore provide best board space savings.

Time to market

Time to market is a major issue for today's designs, and having the flexibility to address all power challenges with the same essential building block solution helps this. Module solutions will offer the easiest solution to implement, but for hi-end systems this becomes an undesirable solutions since they may be too bulky, and therefore take up too much space, or simply will not fit into the space that's allocated for the power supply. Discrete solutions offer a relative space savings versus

module solutions, but this approach is also undesirable, since the design time and required resource is too much. The ideal solution is one that uses less board space compared to either solution, and is still extremely easy to implement, across a broad range of applications.

iPOWIR™ Technology - A whole new way to design on-board power

The discrete and module solutions have been compared throughout this paper, however it seems that for the perfect solution, attributes from both solutions are required to really help solve the power architecture headaches, presented to the designers today. Hi-end solutions need to offer the following:

- Integration of features and functionality using advanced packaging technology to obtain very small solution form factor.
- Optimize critical power components for synchronous buck converters within the solution, using next generation silicon to enhance electrical efficiency, and improving power density.
- Optimize layout-critical components within the solution to eliminate the need for careful layout considerations for the system designer.
- Offer significant design flexibility for the system designer to enable some application specific alterations, but make the whole solution simple to implement.

An example of a solution that can enable all of these features is the new iP1001 product from International Rectifier's new iPOWIR™ Technology family of products.

The iP1001 is a 14mm square plastic Ball Grid Array (BGA) product with a profile of just 3mm, as shown in figure 5 that will handle up to 15A output current. It can be used across a wide range of applications suitable for hi-end data transfer systems, namely 3.3Vin – 21Vin and 0.925Vout – 3.3Vout*. The critical components that need careful selection and layout are contained within the package, so it makes the overall converter design very easy for the designer.

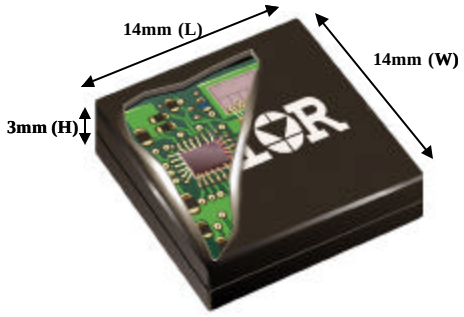


Figure 5 – iP1001 BGA package outline (partially decapsulated)

The actual devices inside the BGA are the power FETs, the PWM & driver IC, schottky diodes and some passives, as shown in figure 6a. The only external components that are needed are the input and output capacitors and output inductor, as shown in figure 6b.

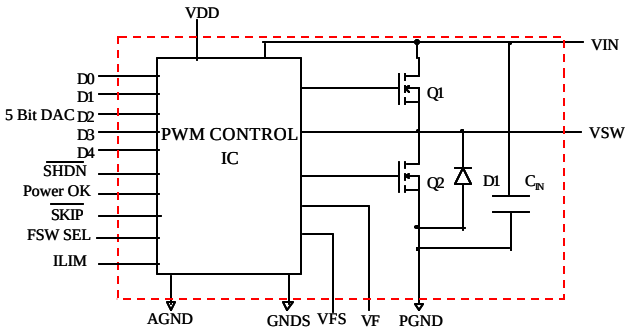


Figure 6 (a) iP1001 internal schematic of iP1001

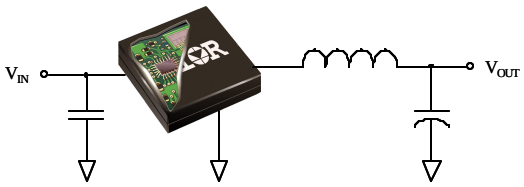
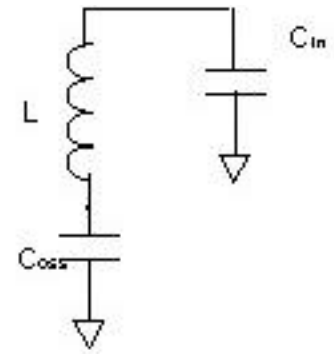
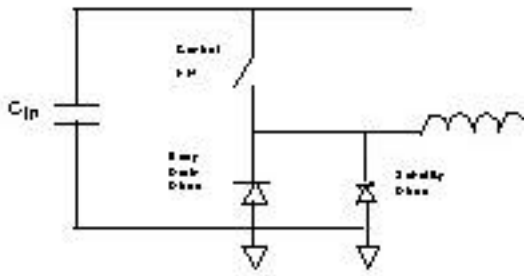


Figure 6 (b) iP1001 external component schematic for complete converter

The external components do not have to be too tightly controlled in terms of layout placement relative to the BGA, since it is "layout non-critical". Included within the BGA is a bypass capacitor that provides two main advantages. The equivalent circuit in figure 7a shows the control FET "on" and synchronous FET "off". By having the bypass capacitor in the iP1001 device, and hence in close proximity to the synchronous FET, it helps minimize the inductive path from C_{in} & C_{oss}. This inductive path is what typically causes the ringing at the switch node. In a normal discrete design, this ringing could become significant if the input capacitors are placed too far from the MOSFETs. Secondly, by referring to figure 7b, where the control and synchronous MOSFETs are off, the inclusion of the bypass capacitor in the device helps to reduce ground plane bounce by effectively minimizing the distance between C_{in} and the synchronous FET body diode, which in turn dampens the effects of reverse recovery (Q_{rr}) current through the synchronous MOSFET. It takes a great deal of power design expertise to ensur
e that these issues do not exist in discrete solutions.



(7a)



(7b)

Figure 7 - Equivalent circuits to demonstrate how input bypass capacitance effects switching characteristics.

The complete converter solution implementing the iP1001 will fit into a real estate area of approximately 45mm x 65mm which can offer up to 58% board space savings versus module solutions and 44% board space savings versus discrete solutions. Figure 8 shows a typical physical design that uses a BGA solution.

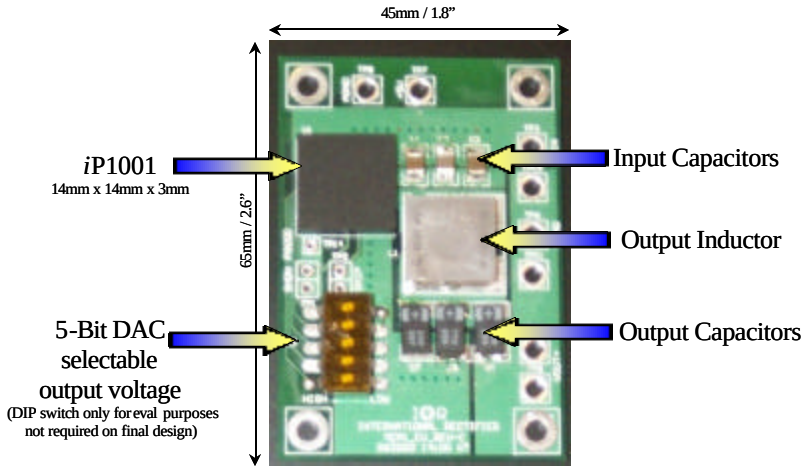


Figure 8 – Typical board layout design implementing iP1001.

For a fully optimized solution, like the iPOWIR™ Technology BGA, there is no de-rating up to 90°C board temperature, so the rated output current does not need to be compromised at elevated temperatures, as in reality, systems are run at elevated temperatures.

The iP1001 solution achieves extremely good electrical efficiency, as shown in figure 10, for 3.3Vin, 1.8Vout, 300kHz with peak efficiency up to 94%. This level of performance is higher than discrete performance by up to 1.5%. This difference can be attributed by the reduced parasitic inductances and reduced package resistances versus discretes.

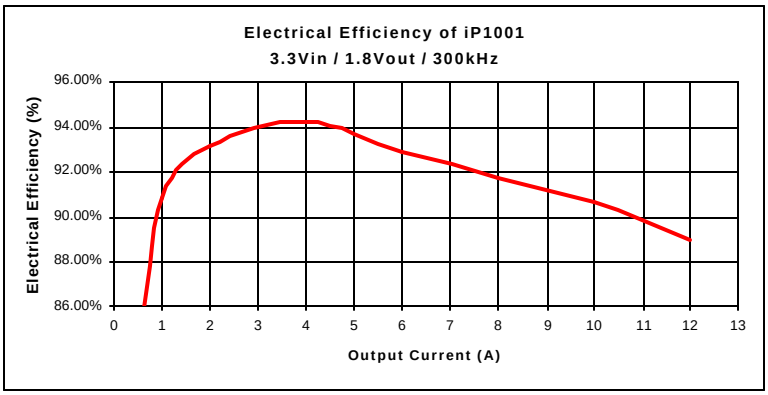


Figure 10 – iP1001 electrical efficiency curve for a typical peripheral application in a network system.

Conclusions

With the increased demands for faster time to market of improved performance data transfer systems, it is apparent that there are many challenges for the power designers and architects. The solutions available today do not address all of the requirements for these systems, so a whole new way of completing the

power design is required, which is where International Rectifier's new iP1001 addresses these issues and can help enable the new required higher levels of bandwidth. The iP1001 can address many applications, requiring 3.3Vin to 21Vin, and 0.925Vout to 3.3Vout, up to 15A load current, meaning that this one device is flexible enough to potentially solve power conversion problems for all peripheral rails in hi-end data processing systems. The ideal power solution is one that utilizes the smallest board real estate, whilst maintaining significant design flexibility, but without the design complexity issues and still achieving best performance. The iP1001 offers these benefits, and will help expedite system design completion.

References

1. IRF7805 application note/datasheet, PD-91746C, 10/10/00

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* Refer to iP1001 datasheet for further information.