BENEFITS OF THE DC BUS CONVERTER IN DISTRIBUTED POWER ARCHITECTURES FOR NETWORKING & COMMUNICATIONS SYSTEMS

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Abstract

The DC Bus Converter is a novel approach for isolated DC-DC converters that improves power delivery for next generation Networking & Communications systems. It will be shown through the use of innovative technologies and a novel control scheme, how a new, more optimal approach can be completed for isolated DC-DC converter designs in Networking & Communications end systems. The DC Bus Converter chipset employs a fixed 50% duty cycle, self oscillating controller and driver on the primary side for half- and full-bridge topologies, coupled with optimised MOSFET technologies on the primary and secondary side. Key operating characteristics and innovation of the IC and MOSFETs within the topology will be discussed with analysis correlating their specifications to the impact on performance of the overall converter and the complete system board. The paper will also provide some discussion comparing ease of use and complexity of design for the various topologies.

This paper will show how a DC Bus Converter can be completed with the selection of just a few components, and how the overall size, efficiency, component count and cost of a typical isolated converter can be improved significantly, making the DC Bus Converter an extremely attractive solution for next generation Networking & Communications equipment. A real design example will be demonstrated using new DC Bus Converter chip sets from International Rectifier, with demonstrated in-circuit results.
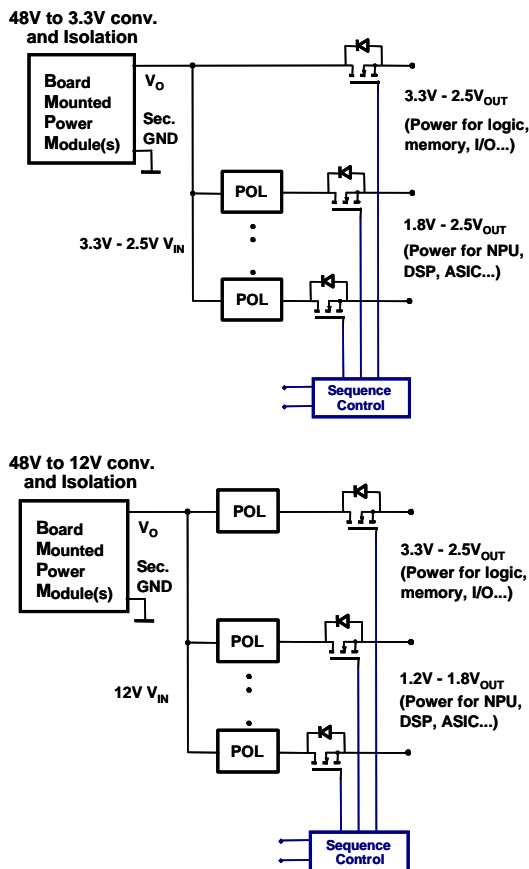
Introduction

Trends within Networking and Communications end equipment have been continually driving the need for more advanced network processor units (NPUs) and ASICs. The need for increased information bandwidth and more complex analysis of information as it travels across the backbone of the internet or transmitted from one mobile communications device to the next has forced the usage of more powerful processing capabilities. As the processors become more optimised to cope with these specific tasks, the power requirements become more complex. The growing variety of processors brings a proliferation of power requirements, since adjustment of the operating voltage can directly impact the performance of the processor. Legacy system power architectures were selected in order to cope with just a few different voltages and power levels, but these architectures now become poorly optimised to handle such a wide range of requirements. The various schemes have trade offs in system efficiency, cost and complexity from one to the other. Optimized 2-stage architectures are the trend for next generation systems [1].

The power architectures in Networking & Communications systems today (including Telecom systems) have a 48V input provided from a bulk AC/DC rectifier module. The 48V is the nominal input, and various systems will have a range either side of nominal that might vary. For instance, a universal telecom range is from 36Vin to 75Vin, and an ETSI (European Telecom Standard Input) range is 36V to 60V. There are also some systems today operating from a regulated 48V bus, where the range can be +/-10%. This input voltage to the card needs to be distributed to the point-of-load in the most electrically efficient, space efficient and cost effective way possible.

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Traditional methods of distributing the power across the board followed two basic schemes. The first was to convert the 48V down to 3.3Vout, then convert the 3.3V to the required point-of-load voltages through several Point-of-Load (POL) converters. Traditionally, the 3.3V would be the most power hungry rail on the board, and so the 3.3Vbus was selected to get the benefit of single stage conversion, thus eliminating compound efficiency loss. The other scheme, more suitable for higher power boards was to convert the 48V down to 12Vout. The 12Vbus would then be converted down to the point-of-load voltages. The 12V was not fed to any load directly. Figure 1 shows these two distributed power architectures (DPA).

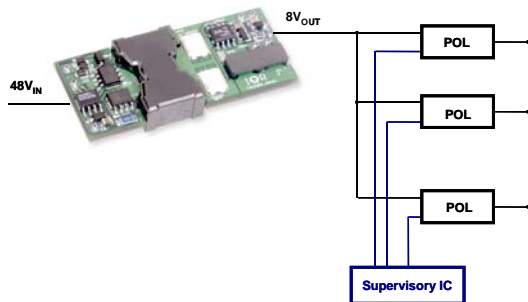**Fig. 1 – 3.3V & 12V Distributed Power Architectures (DPA)**

Each method of DPA has it's advantages, but each also have significant disadvantages. The 3.3Vbus DPA is usually used when there is a dominant load on the board that requires a 3.3V operating voltage,

and if there are multiple 3.3V requirements all over the board. This decision is normally made in order to minimize the amount of two-stage conversion on the board, and therefore maximize efficiency on the most power hungry output. However, when using a 3.3Vbus DPA, bias supplies are needed for each of the POL converters that generate other operating voltages. Another issue is that the 3.3V output needs an in-line sequencing FET. Most operating voltages on a line card need to have a controlled power-up and power-down sequence. This can only be controlled with the in-line sequencing FET in this type of architecture, since the isolated converter has no control over the rate-of-rise of output voltage. The in-line sequencing FET is only useful during the start-up and power-down, and at all other times, there is a DC loss overhead to deal with which impacts efficiency, and adds extra component count and cost. Also, since operating voltages are decreasing year after year, the dominant rail is most likely moving toward 2.5V. For the same on-board power, the on-board current increases by 32%, and distribution losses increase by approximately 74%. All other operating voltages on the board need to be generated from the 3.3Vbus. There can usually be several additional output voltages and each output can use high frequency switching dc-dc POL converters. The high frequency switching of the POL converters can inject noise back onto the 3.3V input line, and since the 3.3V is used to feed directly to a load, a large amount of filtering is required to protect the 3.3V load. The ASICs being powered by the 3.3Vbus can be very sensitive to noise, and can be damaged if the input is not filtered sufficiently. This is extremely undesirable, since the ASICs are usually very expensive items.

The 12V DPA is normally adopted when the total on-board power is high, and there are no dominant loads on the board. When using this approach, the distribution losses are lower, since the current is lower for the same given power level. For this architecture, all operating voltages are generated from POL converters. When biasing the POL converters, it is much easier when using a 12V DPA. In-line sequencing FETs can also be used for controlling the power start-up and power-

down at the POL, however some sequencing can be controlled directly by the POL itself, eliminating the need for sequencing FETs and removing the overhead of DC loss. The 12V output modules available on the market today are typically full-featured bricks that provide a fully regulated 12V output. There is feedback within the 12V brick that provides a signal back to the primary side of the converter via optocouplers. The 12V brick solutions are relatively inefficient, with high rms currents, and they require 40V – 100V secondary side FETs, which generally have higher Rds(on) than would be used if the average output voltage was lower allowing for usage of lower voltage rated FETs. The fully regulated bricks tend to be quite expensive and are large for a given output power since there is significant component count within the module. The distributed 12V bus also makes the POL slightly less efficient, since the input voltage directly impacts switching loss in the POL.

The optimal approach to on-board power distribution, as seen in figure 2, is for an intermediate voltage between 3.3V & 12V, and when using two-stage power conversion, there is no need for a tightly regulated intermediate bus voltage.

Fig. 2 – Optimal DPA scheme using intermediate bus.

New POL converter solutions can take a wide input voltage range, which means that a simpler approach can be taken with the isolated converter stage that generates the intermediate bus voltage. An optimal input voltage for a POL tends to be somewhere between 6-8V, where power loss is at a minimum. This is the best approach for optimizing a two-stage architecture, particularly for 150W systems. The result is

that a highly efficient isolated converter can be designed, in an extremely small area, with minimal component count. Full-featured bricks can use up to 50 components or more, increasing overall design complexity that is unnecessary. When removing the output voltage regulation, there is a significant opportunity to reduce the component count within the module. A DC bus converter utilizes an isolated converter that runs at a fixed 50% duty cycle to allow simple, self-driven secondary synchronous rectification, maximizing power conversion efficiency, minimizing input and output filtering, and improving reliability.
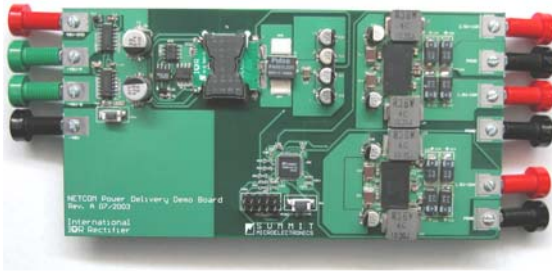
The way forward for on-board two-stage power conversion

A DC bus converter is a new way of converting the 48V input to an intermediate bus that would then be fed into the POL. It is a simple method of creating an isolated converter, with open loop, fixed 50% duty cycle, converting the 48Vin to an 8V intermediate bus. This approach uses a 3:1 transformer turns ratio, with the primary side half-bridge to achieve the overall 6:1 input-to-output voltage ratio. This approach is extremely attractive for 48V systems and wide range input systems (36V to 75V), with availability of second stage POL converter solutions, such as iPOWIR[TM] Technology, having a wide input voltage range. For wide range inputs, the output voltage swings with the same ratio, so for 36V-75Vin, the output varies between 6V-12Vout. The DC Bus Converter front-end plus iPOWIR[TM] second stage will provide a highly efficient two-stage solution. The DC bus converter topology provides the best efficiency, in the smallest space to give the best in power density with significantly reduced component count that can help reduce overall costs. This topology also requires minimum input and output filtering, thus reducing additional capacitors and other components. The control, monitoring, synchronization and sequencing within the power architecture are greatly simplified. Figure 3 shows an example of a DC bus converter design using several innovative technologies that enable this type of performance. Figure 4 shows how the DC bus converter solution can be implemented into a typical 2-stage distributed power

architecture, using two of the new iP1202 iPOWIR products for three separate outputs.
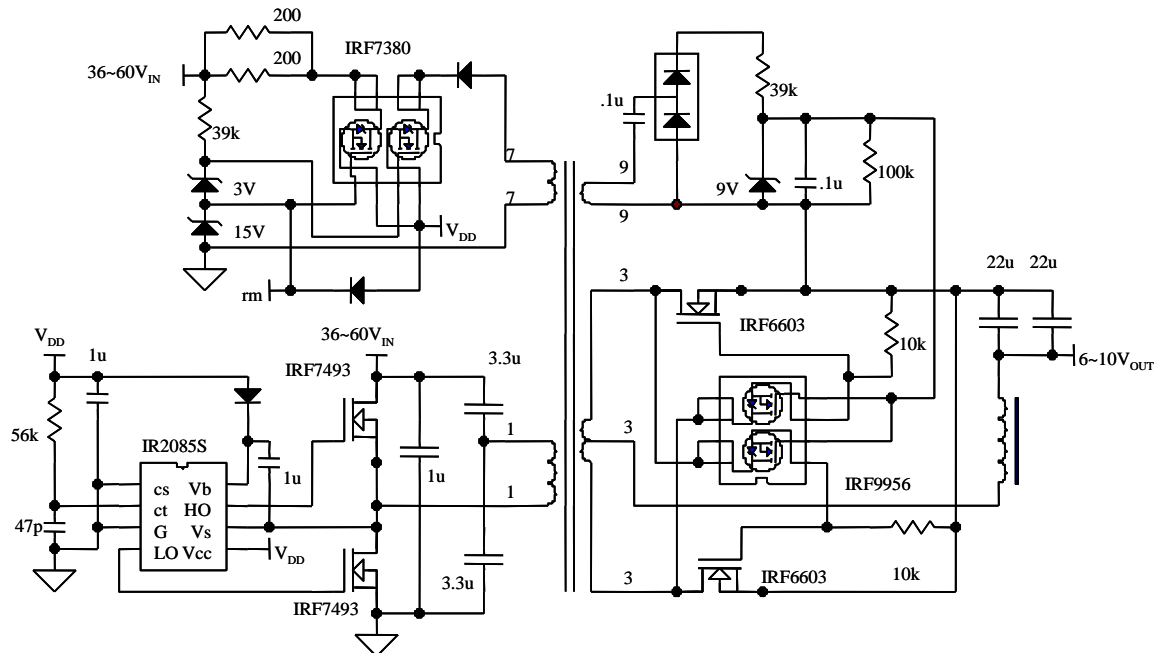

Fig. 3 – DC Bus Converter demo board.

Fig. 4 – 2-stage DPA board using DC Bus Converter & iPOWIR

The chipset that enables this performance is hinged around the primary side half-bridge controller and driver IC and MOSFET technologies.

The IR2085S, a novel IC controller, was developed for unregulated isolated DC bus converters used in 48V two-stage on-board power distribution systems. The controller is optimized for performance, simplicity, and cost. It integrates a 50% duty cycle oscillator with a 100V, 1A half-bridge driver IC into a single SO-8 package. Its frequency and dead time can be adjusted externally for various application requirements. An enable and current limit function is also provided. To limit in-rush current during start-up, an internal soft-start feature on the IR2085S allows a gradual increase in duty cycle from zero to 50%. Typical duration of the soft-start is about 2000 pulses of gate drive signals. Using the new IC controller in conjunction with low charge primary side MOSFETs and low on-state resistance, thermally enhanced secondary side MOSFETs, a 48V DC bus converter demo board was designed to deliver 150W at 8V output voltage with over 96% efficiency in smaller than an 1/8th brick outline, as shown in figure 3. This is 3~5% higher efficiency and 50% smaller size than conventional, fully regulated, board mounted power converters. A similar approach can also be used for full-bridge DC Bus Converters,

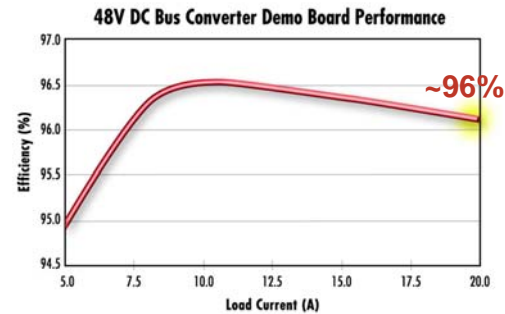**Fig. 5 – DC Bus Converter Demo Board Schematic**

using the new IR2086S, for up to 240W in a similar form factor, with ~96.4% efficiency at full load current.

Fig. 5 shows the DC bus converter circuit schematic using the IR2085S primary side controller and driver IC. On the primary side, the IR2085S is driving two IRF7493 FETs - next generation low charge 80V n-channel power MOSFETs in an SO-8 package. For 36-75Vin inputs this FET can be exchanged with a 100V device, the IRF7495. The primary side bias is obtained through a linear regulator for start-up, and then from the transformer in steady state. The IRF7380, dual 80V n-channel power MOSFET in an SO-8 package is used for this function. Two IRF6603 - Novel 30V n-channel DirectFET power MOSFETs, are used on the secondary side in a self-driven synchronous rectification topology. DirectFET semiconductor packaging practically eliminates MOSFET packaging resistance, which maximizes circuit efficiency, allowing for low overall on-state resistance. The DirectFET packaging also allows for extremely good thremal resistance to the PCB of ~1°C/W, and through the top side (case) of the device of ~3.0°C/W. The IRF6603 gate drive voltage is clamped to an optimum value of 7.5V with the IRF9956 dual 30V SO-8 MOSFET. The secondary side bias scheme is designed to allow outputs of two bus converters to be connected in parallel, while operating from different input voltages, and also to allow continuing output if one of those two input sources is shorted or disconnected.

The size of a potential 150W DC bus converter can be 1.95" x 0.85", which is smaller than an industry standard 1/8th brick, which has a standard size of 2.30" x 0.90", a saving of up to 25%. Some full featured solutions offered today are in ¼ brick form factors, which have a standard size of 2.30" x 1.45", offering a potential of up to 53% space savings if the DC bus converter design approach is used. The DC bus converter chipset is also able to achieve ~96% at 150W within this very small size, as shown in figure 6.

A primary side switching frequency of 220kHz was selected for demonstrating optimum performance. Higher switching frequency decreases the output voltage ripple and can allow the use of smaller magnetic components since the magnetic flux density is reduced. Also a smaller core for the transformer provides lower losses. However, higher switching frequencies increase the primary and secondary switching losses, and results in lower overall circuit efficiency.

Fig. 6 – 150W DC Bus Converter demo board efficiency using the IR2085S half-bridge topology.

The pulse width difference between the high side and low side is less than 25ns to prevent magnetic flux imbalance, which is the main concern in the bridge topology. The frequency and dead time between the low side and the high side pulses for half-bridge circuits can be adjusted based on an external timing capacitor to fit various applications, power levels, and switching devices.

The DC Bus Converter forms the optimal front-end stage in a two-stage DPA. There are also many unique considerations when optimizing the second stage non-isolated POL converter. Embedded on-board "building block" designs offer many benefits versus complete modules or fully discrete designs when board space and design complexity are prime concerns, coupled with meeting overall performance targets. By using a few external components around the new iPOWIR™ iP1202 power building block, as shown in Figure 4, a designer can quickly and easily build a high performance 2-phase, dual-output synchronous buck converter for several of the load voltage requirements. Besides making the designer's job easier, this building block approach also offers up to 50% savings in

pc-board space versus alternate equivalent discrete solutions, while drastically reducing design time. The engineer is provided with a 100% tested and guaranteed performance device, which in general does not have the intricate layout issues associated with discrete designs as well as providing a known maximum power loss. This is not possible with discrete on-board designs. Additionally, it delivers high conversion efficiency, along with much desired flexibility to allow the device to be easily configured for other load voltages.

Distributed Power Architecture

For many reasons, including high efficiency and tight regulation at low voltages, DPA has become an attractive architecture for multi-load or multi-voltage applications. Aside from bringing dc-dc converters closer to the point of load, DPA allows flexible POL converters to be used and specifically optimized for the intended application. The POL allows for adjustable output voltages that can be trimmed at the load, if necessary, and also the ability to control complex sequencing and tracking functions specific to the type of load used. Simply deploying DPA is not the final solution, there is more to it than meets the eye. The electrical efficiency of dc-dc converters determines how much power is dissipated, and is directly related to the temperature rise on the board. This affects the device temperature and ultimately the reliability of the product. Thus, power loss must be properly managed to ensure reliable operation of the system. Furthermore, to ensure proper operation of the system, the multiple operating voltages on a system card must be initiated in a proper sequence per the processor manufacturers specification. In fact, many applications demand that the loads are turned on in compliance with system level start-up protocols, so that high performance NPUs, FPGAs, ASICs and other devices are protected from transients, shorts or some sort of a breakdown. Users cannot afford to lose such expensive chips due to ineffective or inapt power designs or solutions.

To minimize compound efficiency loss, which can be significant at times, the POL converters should offer efficiency close to or above 90%. For instance, if two 90% efficient converters are utilized in series, the overall result can be as low as 81%. Therefore, it is clear that POL converters deployed in this scheme must achieve high efficiency to minimize the throughput efficiency loss. In the particular example in Figure 4, the bus voltage of 8V was produced at 96% efficiency and the iP1202 produced an efficiency of 92% with a load current of 8A. This provides a very respectable overall efficiency of ~84.5%, as shown in figure 8, with a lower cost architecture.
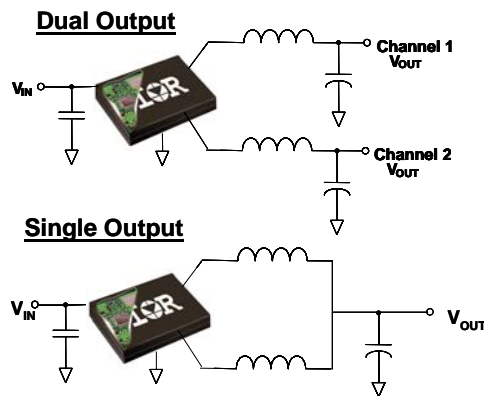
Since efficiency determines the amount of wasted energy in a given system, which translates into heat on the board, it is important that the converter power loss is kept to the bare minimum. That means, the POL converter efficiency must be maximized to maintain pc-board temperature within specifications. Higher loss results in higher board temperature, which means extra cost to manage that heat. Lower power loss means less heat, which in turn means higher system reliability and guaranteed system quality of service (QoS).

Simple Solution

To offer a solution that addresses the above issues, and in addition delivers the desired features, IR has applied its advanced iPOWIR packaging technology to create an integrated building block. Applying expertise in power system design and the chipset interaction it has integrated PWM controller and driver functions with associated control and synchronous MOSFET switches, schottky diodes and input bypass capacitors in a single package. For maximum performance, the power components used in this single package have been closely matched, with optimized internal layout. The result is that a single device that can now be treated as a building block toward the design of a high performance two-channel synchronous buck converter. The only components needed to complete this dual-output power supply are the output inductors, output capacitors and input capacitors (Fig. 7a), in addition to a few other passives. Both the channels of the power supply operate from a common input. Because the internal topology is

synchronous with fixed frequency voltage mode control, the two outputs can be easily paralleled to achieve a single output voltage with twice the current handling ability (Fig. 7b).
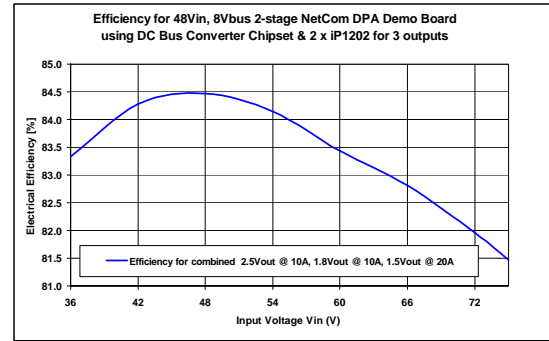
A 180° out of phase operation is used for single or parallel output and the benefits from increased ripple frequency can be seen with external component count and size reduction. The iP1202 is capable of being powered directly from the DC Bus Converter output voltage eliminating the need for external bias circuits, thereby cutting additional external components and design complexity. This new building block measures only 9.25mm x 15.5mm x 2.6mm in size, saving the designer precious board space, and making valuable contributions to the desired power density.

Dual Output

Single Output

Fig. 7a & 7b – iP1202 schematics

By using a simple resistive voltage divider for each channel, the output voltages are independently adjustable for the iP1202, and the input operating voltage range is from 5.5V to 12V, allowing for easy implementation into a DC Bus Converter front-end architecture. This POL solution allows for independent 15A outputs or a dual phase 30A single output.

The overall throughput efficiency for the DC bus converter feeding the iP1202 for three outputs is shown in figure 8.

Fig. 8 – Overall throughput efficiency of the DC bus converter chipset plus iPOWIR in a 2-stage DPA

A Hiccup pin is made available to set over-current protection protocols. It can be configured to either latch or hiccup (auto-restart) when a short circuit is detected. Hiccup is key in today's end telecom or networking systems, many of which are in remote locations, so increased up-time and auto restart capabilities reduce maintenance costs and inconvenience that can effect QoS.

In addition, the iP1202 has the ability to be externally synchronized with other POLs, such that input EMI filtering can be simplified.

To enable accurate thermal design of the pc-board, this building block is also constructed to guarantee a power loss limit and safe operating area. Such calculations are complex and time consuming in traditional discrete based power circuits, wherein many first order power loss dependent variables from the power semiconductors have to be taken into account. Added to this is the virtual elimination of second order layout and stray parasitic loss effects that are more difficult to account for accurately in the initial design phase. By having a guaranteed maximum power loss rating and SOA, the thermal design considerations are simplified as a known tested power loss limit is given and can more easily be correlated to the SOA to ensure reliable and safe long term operation.

Conclusions

Next generation MOSFET technologies and a simple, fixed 50% duty cycle 8-pin SOIC controller from International Rectifier allows a 48V DC bus converter to deliver **150W at over 96% efficiency**, and in **less than 1.7in^2 space**. This is **3-5% higher efficiency and 50% less space than a typical BMP converter** used in two-stage on-board power distribution, making this much more of an optimal solution defining the trend for on-board power architectures. This novel chipset solution achieves benchmark performance while remaining extremely cost effective for most 48V and 24V converters in two- stage on-board power distribution. When this approach is used to provide an intermediate bus voltage that feeds into a series of optimized second stage POLs, such as iP1202, overall throughput efficiencies up to ~84.5% can be achieved, thus providing a very attractive approach to two-stage on board power distribution.

References

[1] David G. Morrison, "Distributed Power Movers To Intermediate Voltage Bus," Electronic Design, Sept. 16, 2002, P. 55

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Note: *Some of the concepts presented in this paper are subject to granted patents and patent pending*