

A Solution to Simplify 60A Multiphase Designs

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As presented at PCIM 2001

Today's servers and high-end desktop computer CPUs require peak currents of around 60A-80A and next generation processors will be in the order of 100A. Similarly, the transient response in today's CPUs is in the order of 30A/us while next generation processors are anticipated to exceed 300A/us. This paper will show a simple method of achieving these extremely high currents simply, efficiently and with the minimum footprint.

Power Design Challenges

The demands of high current, low voltage and fast transient response microprocessors or ASICs present a great challenge for power designers that are required to provide efficient power supplies in the smallest board area when converting from intermediate supply voltage rails to very low voltage outputs.

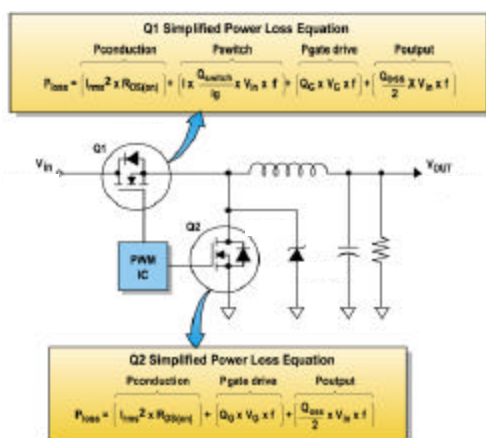


Figure 1: Simplified power loss equations

As the ratio of output voltage to input voltage increases, and/or switching frequency increases, the high and low side power MOSFET switches must be carefully optimized and balanced for the application as outlined in the power loss equations of Figure 1 (ref. 1). Significant advances in technology (both silicon and packaging) have improved the performance of discrete components significantly. For instance only 3-4 years ago it was state of the art to have a buck converter delivering about 7A to a microprocessor with a single high and low side MOSFET, but this level has now moved to around 15A.

The layout of power components relative to the input, the output and drive components also needs to be considered carefully. Improper layout can lead to undesirable effects such as excessive power losses caused by the Cdv/dt induced turn-on of the synchronous MOSFET. It can also lead to large swing voltage spikes at the switch node that may cause ground bounce and excessive EMI. These shortcomings become most apparent as switching frequency and/or the delta between input voltage and output voltage increase. The trend to higher input voltage in order to lower buss current and hence dc resistive input losses around today's systems compounds this effect.

Multiphase conversion addresses the higher current requirements and faster transient response problem, but this type of conversion conflicts with footprint area and also introduces undesired design complexity. Since today's surface mount MOSFETs are typically capable of handling about 15A per phase (assuming a single MOSFET for each the Q1 and Q2 sockets), a 60A converter would require four phases for this type of an approach. This translates to eight MOSFETs plus four drivers and other associated passive components just for the power portion of the converter. A multiphase PWM IC and the passive components that are required for proper

configuration of the control function are also required. This not only requires a lot of board space, but also calls for a great deal of layout consideration and optimization. Designing an efficient and cost effective single stage DC-DC converter is a non-trivial task and doing so for a multiphase converter can be non-trivial to the n^{th} degree (where n is the number of phases).

The challenge for power semiconductor manufactures is to provide solutions that maintain footprint and complexity similar to single phase conversion, but for higher current multiphase systems. Even though the two will never be equal, component integration can dramatically reduce board space and design complexity while maintaining flexibility and performance.

Addressing the challenge

A new alternative solution to address these challenges has been developed by International Rectifier and is called iP2001. The solution is not just a simple integration of components, but an advanced method of combining carefully optimized power components, driver IC and layout critical passive components into a very small 11 x 11 x 3mm ball grid array (BGA) building block. As shown in the simplified internal block diagram of *Figure 2* the iP2001 power block contains a high side and low side FET, a MOSFET driver, a freewheeling diode and a bypass capacitor that is required in order to guarantee layout 'independence'. There are also other miscellaneous capacitors and resistors incorporated in each block to assist with functionality and layout independence, but are not shown for simplicity.

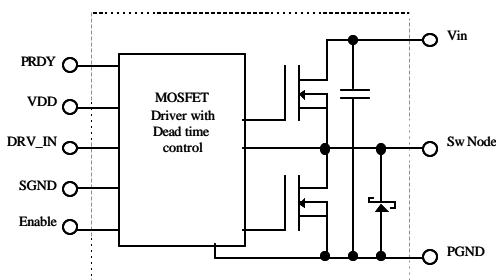
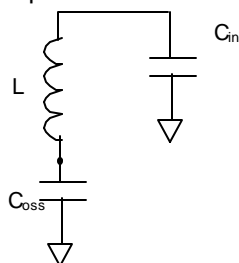
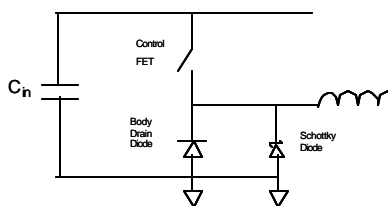


Figure 2: iP2001 internal block diagram

There are two significant advantages of including the bypass capacitor in the iP2001 building block. First of all, by referring to the equivalent circuit in *Figure 3a* with the control FET on and synchronous FET off, having the bypass capacitor in the iP2001 device and hence close proximity to the synchronous FET, this helps minimize the inductive path from C_{in} & C_{oss} . This inductive path is what typically causes the ringing on the switch node, shown in *Figures 4a and 4b*. In a normal discrete design this ringing could become significant if the input capacitors are placed too far from the MOSFETs.



3a)



3b)

Figure 3a and 3b: Circuit equivalents to demonstrate how the input bypass capacitor affects switching characteristics

Secondly, by referring to *Figure 3b* where synchronous and control MOSFETs are off. The inclusion of the bypass capacitor in the device helps to reduce ground plane bounce by effectively minimizing the distance between C_{in} and the Synchronous FET body diode, which in turn dampens the effects of reverse recovery (Q_{rr}) current through the synchronous MOSFET. With a discrete design ground bounce could become significant if the input

capacitors are placed too far from the MOSFETs. The layout independence just described significantly reduces engineering complexity because with discrete designs proper component placement and trace layout require a great deal of thought and may require several revisions to attain adequate electrical performance.

Figures 4a and 4b show examples of the performance of a simulated poor layout vs. a typical iP2001 layout. Both examples are shown with the following test conditions:

$V_{in} = 5V$, $V_{out} = 1.6V$, $I_{out} = 15A$, $f = 150kHz$.

As shown in the picture in *Figure 4a* a four inch copper wire is placed between the input to the iP2001 and the bulk capacitors to simulate very poor layout or an excessively long trace from the capacitors to the input of the converter. The waveform in *Figure 4a* is measured at the switch node to demonstrate that the iP2001 is still capable of switching full load current. The sinusoidal waveform that is superimposed on the switch node waveform is due to the LC resonance created by the wire inductance and input capacitance. *Figure 4b* shows a normal layout and the waveform measured at the switch node. The iP2001 devices were operated at the lowest rated input voltage and switching frequency. The test conditions were chosen as they place the greatest burden on the input capacitors, due to the larger duty cycles the devices are required to support.

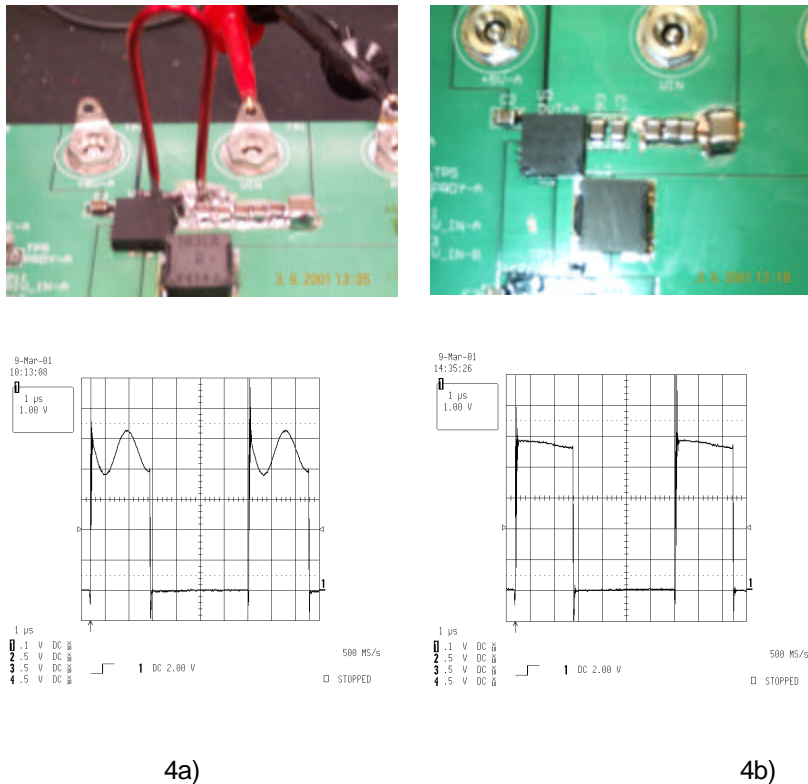


Figure 4a. Switch node waveform showing the switch node of simulated poor layout
Figure 4b. Switch node waveform showing the switch node of a typical iP2001 layout

Another benefit of integration is that all of the internal interconnects are very small compared to the traces and pins required in discrete designs. These smaller internal interconnects dramatically reduce the parasitic inductance and capacitance that are inherent to discrete power architectures. The reduction of parasitics translates into less noise and power losses, enabling the iP2001 devices to operate into the one-MHz frequency range, while maintaining high efficiency levels. This enables converters to provide very fast transient response while providing the opportunity for designers to reduce the size and quantity of external filter components. This can help reduce the negative impact of increased board space that is inherent to multiphase buck converters.

Each iP2001 power block is capable of delivering 15A at 1MHz switching frequency and only requires an external inductor plus input and output capacitors per multiphase power phase. *Figure 5* demonstrates the difference in complexity and board space of a 60A D-Pak solution compared to the new iP2001 solution. An *iPOWIR* solution such as this can provide up to 44% board space savings when compared to discrete solutions.

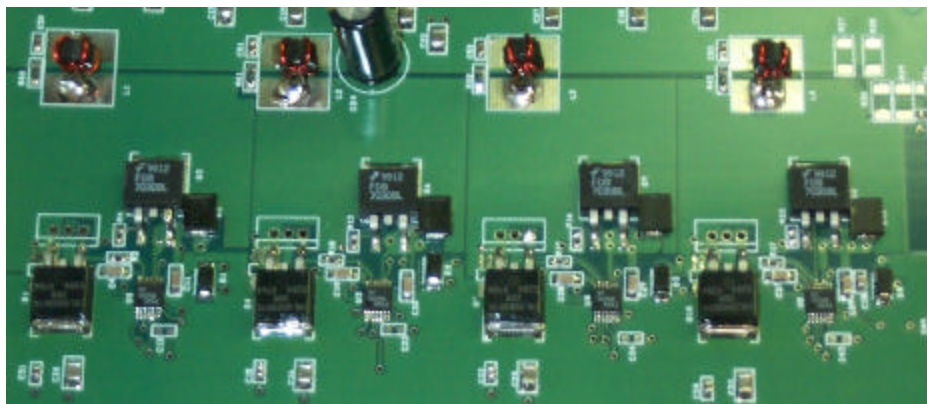


Figure 5a. Typical 4 Phase D-Pak Solution

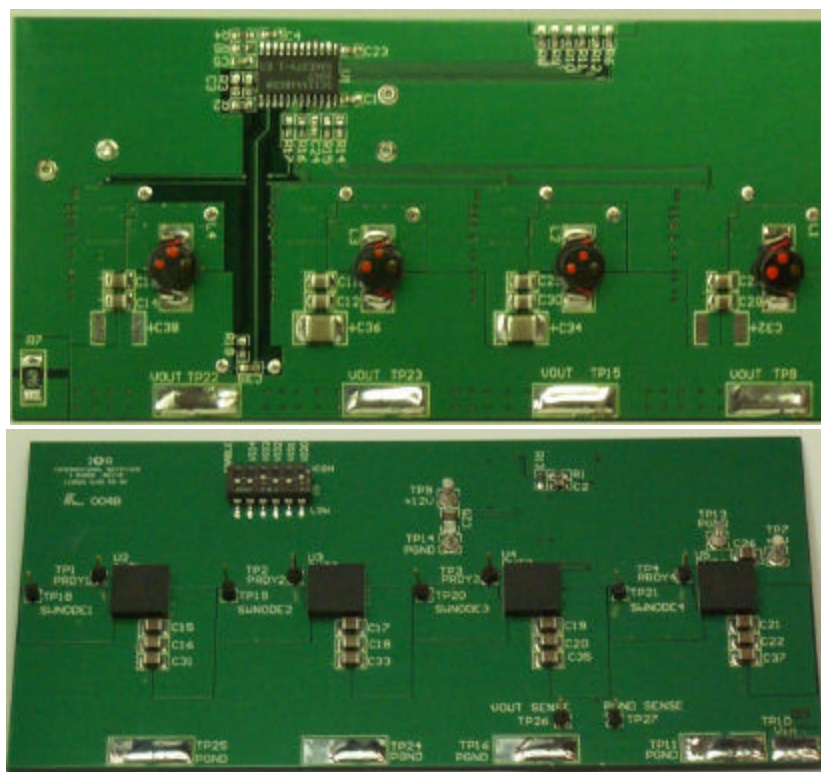


Figure 5b. The front and back side of a four Phase iP2001 solution

As demonstrated in *Figure 6* a four phase iP2001 solution compared to a D-Pak solution can provide up to 6% efficiency gain at a full load output of 60A. The tests were performed with each solution having a 12V input, 1.6V output, 1MHz switching, in 25°C ambient temperature with no airflow.

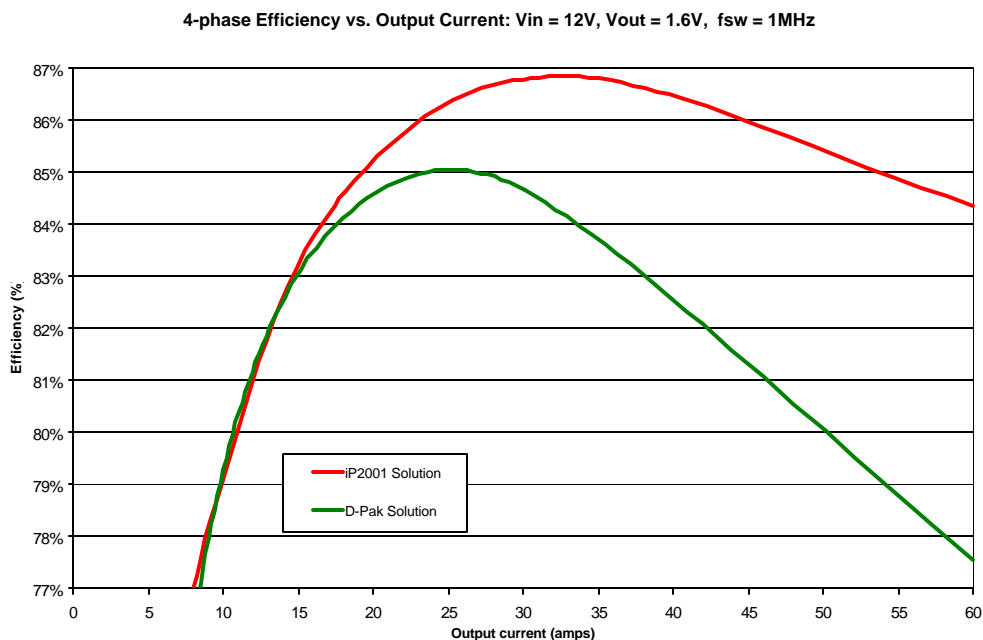


Figure 6. iP2001 vs. Discrete Solution Efficiency

There are two reasons for this potentially large increase in efficiency. Within the iP2001 the MOSFETs and driver IC have been matched to provide the cleanest and fastest switching possible. Because the traces between them are very small, the stray inductances and capacitive elements on the path from the gate driver to the MOSFET gate are also minimized. This in itself can offer up to 2% efficiency gain at 300kHz that is then amplified at 1MHz. The second reason for the improved performance is the fact that the high side control FET can be sized up to minimize conduction loss. In the example in *Figure 6* if the discrete alternative control FET silicon size had been increased then the efficiency would have actually decreased due to increased charge and switching losses. It is because of the very clean and fast gate drive signal and matching the driver and MOSFETs that allows the optimum size of the control MOSFET to be redefined. This is much more difficult to accomplish with discrete alternatives because the drivers need to be mounted on a board and then the signals routed through pins and board traces to the MOSFETs. These conduits inherently introduce parasitic inductance and capacitance, which distorts the gate drive signal by the time it reaches the control FET. Because of this, the control FET generally needs to be sized conservatively with respect to gate charge in order to minimize overall losses. *Figure 7* shows a simple four phase design that can thermally handle 60A with headroom to spare. These devices were mounted on 4 layer 2oz Cu and then operated for over 5minutes at 60A with $V_{in} = 12V$, $V_{out} = 1.6V$ and $freq = 1MHz$. Obviously thermal management must be considered when designing with these BGA solutions, as about 90% of the power dissipation will be delivered to the board.

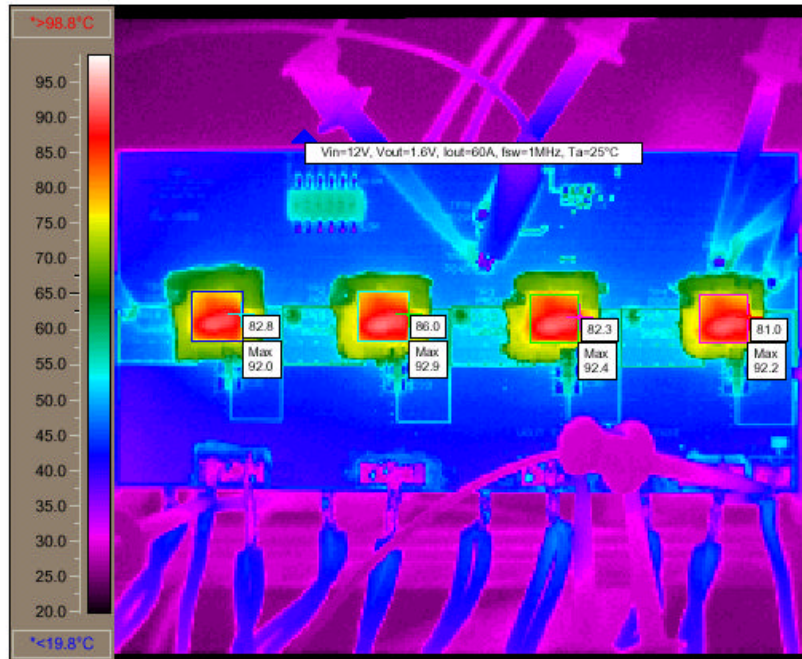


Figure 7. Thermal picture of simple four phase converter

Conclusion

Designers are currently faced with considerable design challenges in order to power today's demanding, high current and fast transient response processors and ASIC's. In addition to this, they are also required to design these converters to fit in about the same amount of space as previous designs. Multiphase converters address the high current and fast transient demands, but typically require more footprint area and are more complex to design than standard dc-dc converters. The iP2001 from International Rectifier addresses both of these issues by providing up to 44% footprint reduction compared to discrete designs while dramatically reducing the power supply design workload.

References

1. IRF7805 application note/data sheet, PD-91746C, 10/10/00