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Choosing The Right Power MOSFET Package

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Introduction

Power levels and power density requirements continue to increase for many types of end equipment such as personal computers, servers, network and telecom systems. It demands higher performance from the components that make up the power management system. Until recently silicon has been the most important factor in improving power management system performance. However, improvements in silicon technology over the years have significantly reduced MOSFET $R_{DS(on)}$ and the amount of heat generated by power semiconductors to the point where packaging becomes the limit to higher performance devices. As system current requirements increase exponentially, many advanced power MOSFET packages have been introduced to the market. The popular packages include DPAK, SO-8, CopperStrap™ SO-8, PowerPak™, LFPAK™, DirectFET™, iPOWIR™, etc. While offering more design freedom, too many choices can also be confusing, especially to an embedded power supply designer, who has limited resources to experiment with all these unfamiliar devices. This article will compare each package, and simplify the component selection by highlighting the performance difference in the embedded applications.

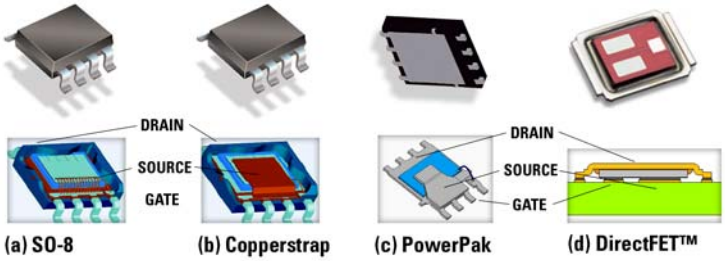
The Need for New Packaging Technology

With cost and size pressures, and with the recent adoption of 12V distributed bus architectures, the embedded point-of-load (POL) dc/dc power supplies become increasingly popular.

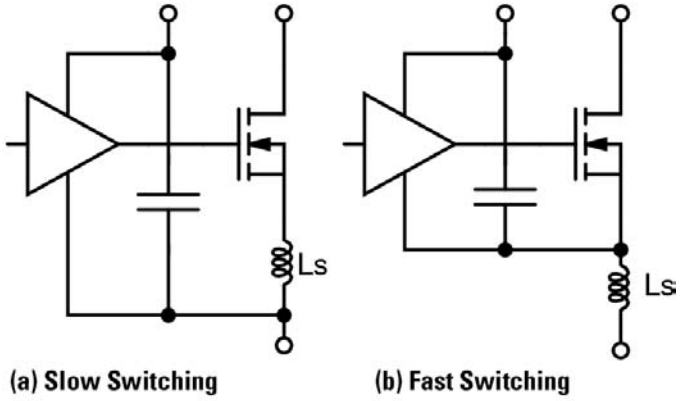
The standard wire-bonded SO-8 has been the standard package of choice for embedded POL power supplies for years due to its small size, low profile, standard footprint and reasonable performance. However, with the rapid progress in MOSFET silicon technology, the silicon $R_{DS(on)}$ starts to approach sub-m. range, and the standard SO-8, with significantly higher fixed Die Free Package Resistance (DFPR), has become the bottleneck for bringing out the silicon performance.

There are four major areas where the wire-bonded SO-8 has serious limitations:

1. Package resistance
   1.6mΩ typical. About 50% of total MOSFET R_{DS}(on) for the latest devices comes from the package resistance. The primary reason is that internal bonding wires are used to bring the source terminal to the leads, as shown in Figure 1(a).



2. Package inductance
   A leadframe-based package with internal wirebonds introduces parasitic inductance on the gate, source and drain terminals. The source inductance will show up in the circuit in the form of common source inductance shown in Figure 2(a), and has the most significant impact on the switching speed of the MOSFET. Due to the lack of direct access to the source of the silicon die, both the gate drive circuit and main power train path share the same inductance. During current switching, this inductance will produce a large Ldi/dt effect to slow down the turn-on and turn-off of the device. This effect will significantly hinder the performance at high switching frequencies.



3. Junction-to-PCB thermal impedance
   The MOSFET drain is attached to the lead frame, which is molded into a plastic. Power dissipation has to travel laterally to the drain leads and PCB, as

the main thermal conductivity path. The source connection has even higher thermal impedance to PCB.

4. Junction-to-case (top) thermal impedance
   Covered by plastic, the standard SO-8 has a very poor thermal conduction path to the top of the case.

The package limitation of the SO-8 has a significant impact on both electrical and thermal performance. The DPAK can be used to solve some of the thermal limitations of an SO-8. However, due to its large size, package resistance and source inductance, the DPAK is not very practical in the embedded applications. As current density requirements increase, it's obvious that a novel packaging technology in a similar size of an SO-8 is required.

Several enhanced packages are shown in Figure 1. Each improves the package performance over SO-8 to some extent by addressing part or all of the four major limitations of standard SO-8.

CopperStrap™ SO-8 Technology

The CopperStrap is an interconnect technology that replaces the wirebonds connecting the source to the leadframe with a solid copper strap that covers the surface of the die. Figure 1(b) illustrates the CopperStrap SO-8 structure, which is also branded as PowerConnect™. CopperStrap provides a better conductive path, thermally and electrically, from the die to the leadframe and PCB. This has resulted in a 10 to 20% reduction in thermal resistance and a 60% reduction in package contribution to electrical resistance for source connections. Specifically, by replacing the 21 2-mil gold wirebonds (the maximum number for an SO-8 package can handle) with the CopperStrap, the die-source resistance was reduced from 1 mΩ to 0.4 mΩ. In order to release the thermal stress caused by the CTE mismatch of the copper strap and silicon, silver-filled epoxy is used to attach the copper strap to aluminum top metal. The shape and features of the strap also play a key role in how well stresses are distributed under thermal cycling conditions.

The CopperStrap is a large step forward in reducing the SO-8 package resistance, and there is no footprint difference from the traditional SO-8. In fact, there are so many low R_{DS}(on) SO-8 devices today containing the CopperStrap that the technology itself is now seen as a standard SO-8.

However, the CopperStrap doesn't improve Rthj-case top, Rthj-pcb and source inductance in any significant way. So its advantage is quickly outpaced by the continuous demand for higher current.

PowerPak™ Technology

One of the biggest issues with the SO-8 is its high thermal impedance between junction and the PCB. Excessive amount of power dissipation can significantly raise its silicon temperature. The next natural package evolution is to improve the thermal contact between the die and the PCB board by removing the molding compound below the lead

frame and placing the metal of the lead frame in direct contact with the PCB. The lower surface of the lead frame becomes a large drain contact that gets soldered to the PCB. It provides a much greater area of contact to conduct heat away from the die. As a byproduct, it also results in a lower profile device, because eliminating the molding reduces thickness. This package technology is exemplified in PowerPak shown in Figure 1[c]. In the PowerPak implementation, the package retains a footprint of SO-8, but its thickness measures around 1mm. The CopperStrap technique is preserved in the PowerPak to maintain the low contact resistance to the source. This technology is comparable to MLP, LFPAK™, SuperSO8™, WPAK™, PowerFlat™ and Bottomless SO-8™, etc.

PowerPak significantly reduces Rthj-pcb, which allows efficient heat transfer to the motherboard. However, due to rapid rise of current demand, the motherboard becomes saturated with heat, so there is an increasing demand for not dumping heat to motherboard. Top-side cooling through a heatsink becomes more and more popular.

DirectFET ™ Technology

DirectFET is a revolutionary concept that virtually removes all four limitations of SO-8 at once. Figure 1(d) shows the DirectFET package applied to a MOSFET die. The silicon die is mounted in a copper housing. The bottom of the package consists of a die specifically designed with source and gate contact pads that can be soldered directly to the PCB. The copper "can" forms the drain connection from the other side of the die to the board. This package eliminates the conventional lead frame and wirebonds that are the main source of package resistance and eliminates the plastic packaging that limits thermal performance of most SMT packages.

This configuration maximizes contact area between the source and gate pads and the PCB for best electrical and thermal efficiency. The copper can drain connection also provides an alternate path for heat dissipation and makes the use of a heatsink very efficient.

There is virtually no source inductance in DirectFET, and the complete access to the source side of MOSFET enables the driver connection to the MOSFET gate and source terminals without including any PCB stray inductance in the high current path, as shown in Figure 2(b). Therefore, the high frequency switching performance of DirectFET is exceptionally good.

In-circuit results show that one DirectFET, without topside cooling, can easily replace two SO-8 in parallel, and sometimes two PowerPAKs in parallel. With a heatsink attached to its can, DirectFET makes paralleling MOSFET less necessary.

DirectFET is such an ultimate package that the silicon once again becomes the limiting factor in further MOSFET performance improvement.

Table 1. Comparison of different packages

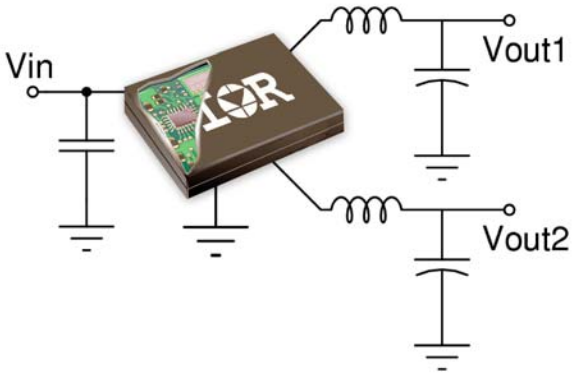
	Package Resistance (mΩ)	Source Inductance (nH)	Rth junction_pcb mounted (°C/W)	Rth junction_case top (°C/W)
SO-8	1.6	1.5	11	18
CopperStrap	1	0.8	10	15
PowerPak	0.8	0.8	3	10
DirectFET	0.15	<0.1	1	1.4

iPOWIR ™ Technology

With the advancement of package and silicon technology, the power MOSFET has been able to keep up with the rapid increase of current demand. However, for an embedded POL converter, the design effort is not getting any easier, and in fact, in order to obtain the necessary electrical and thermal performance, the layout and component selection become so critical that any oversight can create reliability problems. The testability of embedded power supplies is limited to dc parameters only, and also contributes to additional reliability concerns.

iPOWIR technology is introduced to simplify the design. With adding a few external components, a high current power supply can be designed in a single layout iteration. Different from co-package or DrMOS concept, iPOWIR devices tightly integrate silicon as well as all critical active and passive components, and are tested in production as high switching power supplies. Power loss or efficiency is used as test limits in addition to dc parameters. Treating them as power supplies instead of co-packaged devices results in iPOWIR devices significantly simplifying embedded POL power supply designs with reliability levels matching full functional power supply modules at lower cost.

Figure 3 shows a dual channel iPOWIR device (iP1202) that outputs up to 15A per channel or up to 30A as a combined output (2-phase solution).



Choosing The Right Package

It is common sense to use the cheapest components to meet the electrical and thermal requirements. However, the SO-8, which is at the bottom of the evolution chain, is not necessarily the cheapest. Quite often, the die size in an SO-8 device is big in order to compensate for its large package resistance and higher Tj. For example, the DirectFET MOSFET can either reduce part count or reduce power loss to the extent that system level designs are less expensive than many SO-8 implementations. Besides the more tangible benefits in performance, lowering Tj by using advanced package is always beneficial in system-level reliability. Every 10°C reduction in Tj roughly improves MTBF by 2x.

Whenever there is need to use two or more devices in parallel in order to meet the efficiency or thermal requirement, it is good time to think of using devices higher on the evolution chain to reduce number of devices. Paralleling MOSFET devices in a high switching power supply is not always effective, and can be sensitive to circuit stray impedance and device variations. It is cheaper and more reliable to use a single device to do the job.

Two-phase solutions generally provide lower output voltage ripple and better transient response than a single-phase design. However, adding more phases for resolving thermal or efficiency problems is not the best approach. Using better packages and keeping the number of phases at around two can usually provide the most cost effective solution.

Whenever top side cooling options are available, DirectFET type packaging should always be considered first. Adding a heatsink is usually cheaper than adding more MOSFET devices or more phases in parallel.

For designers not comfortable with discrete on-board implementations, iPOWIR devices offer an excellent cost/performance trade-off.

Note to Editors: