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Design Considerations for a New Generation Mid-voltage Power MOSFET Technology

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***Abstract* — N-Channel power MOSFETs in 40V to 200V breakdown voltage range (mid-voltage) are used in a wide range of switching power supply applications. Furthermore, they can be used for very different functions within the same circuits, from primary side switch, to secondary synchronous rectifier, to DC load management. Modes of operations include both hard switching and soft switching, while the switching frequency varies from DC all the way up to a Mega Hertz. It is always possible to optimize power MOSFET for each unique socket and application. However, this approach is very costly and time consuming, and can result in a large number of custom parts with very limited usability. The optimization effort for single application can significantly slow the rate at which new, fundamentally better technologies are developed and applied. In this paper, the development of a new generation mid-voltage MOSFET technology covering multiple emerging applications is described. The basic methodology is based on advanced loss modeling of typical applications to find the optimized designs. Optimized designs are compared in terms of power loss and cost, and then consolidated into a single design with optimized cell density. The best tradeoff of power loss and cost was achieved for individual application by varying the active areas of the die. The optimized designs are experimentally verified.**

Index Terms* — *MOSFET, Modeling, Class D, Bus Converter

I. Introduction

The aggressive computing CPU roadmap [1][2] provides a compass for the development of low voltage 20V and 30V power MOSFETs. Those devices are used in synchronous buck converters that operate with either 12V (desktop, server), or 19V input (mobiles) and with very low duty cycle. Unlike the low-voltage MOSFETs, the mid-voltage MOSFETs ranging from 40V to 200V cover numerous relatively unique applications. These include isolated DC-DC converters, hot swap, active ORing, class D audio amplifiers, plasma display drivers, UPS inverters, and motion control. Although it is possible to optimize power MOSFET for each application, this would be very costly and result in a huge number of custom parts and would slow the rate at which new, fundamentally better technologies are developed and applied.

In this paper, a procedure for developing and optimizing a new generation of power MOSFET technology is described. The 100VN MOSFET breakdown voltage rating is the most popular mid-voltage rating, and was selected as the driver for technology development. The goal was to determine if a single cell design and cell density can be used in multiple applications without having to make significant trade-offs. The methodology used to do this is based on the development of loss models for identified target applications. The models are verified with experimental tests using existing generation of MOSFET technology, so that a reasonable confidence level in accuracy is built. Projected parameters of several most promising new generation MOSFET design choices are then plugged into the verified models. Calculated power losses are compared as for different active areas. It will be shown that a single cell density design can be adopted, resulting in drastic reduction in development time and cost. With single cell density design, needs of a particular application is addressed by varying the active area of the device.

Power loss modeling is crucial for this work in order to narrow down design choices and determine optimum die size for a given application. However, most of the existing loss models assume that the MOSFET voltage and current transition are linear, which is not accurate [3][4]. The loss modeling based on this assumption tends to exaggerate the switching loss. In this paper, nonlinear voltage and current transitions are used for switching loss calculation. Detailed power loss models are developed for three key mid-voltage MOSFET applications: primary switch and the secondary synchronous rectifier for 48V isolated DC-DC bus converter, and Class-D audio amplifier.

The results of modeling and the in-circuit experimental verifications show that with minimal power loss and cost trade-offs it is possible to address multiple applications with a single power MOSFET design, while varying only the active area of the die. Based on this result, two lead 100VN devices for a new generation of power MOSFET technology were designed and manufactured, and experimentally verified.

II. MOSFET Design Trade-offs

In a switching mode power converter, a MOSFET generates conduction and switching losses. Conduction losses are caused by channel on-state resistance, $R_{DS(on)}$, and switching losses are caused by voltage and current overlaps during short switching transitions. To reduce conduction loss, $R_{DS(on)}$ needs to be minimized. To reduce switching loss, interelectrode capacitance needs to be reduced. One of the key...

aspects of MOSFET design is cell density selection, the number of individual cells connected in parallel in a given active area. Increasing cell density is the simplest way to reduce MOSFET on-state resistance, $R_{ds(on)}$. This means that for a given MOSFET active area (AA), the cell pitch between the individual cells needs to be reduced. However, the reduction of the cell pitch results in increases gate charge. Gate-to-drain charge, Q_{gd}., and gate-to-source charge, Q_{gs}, are particularly important as they determine the switching loss during voltage (Q_{gd}), and current (Q_{gs}) transitions.

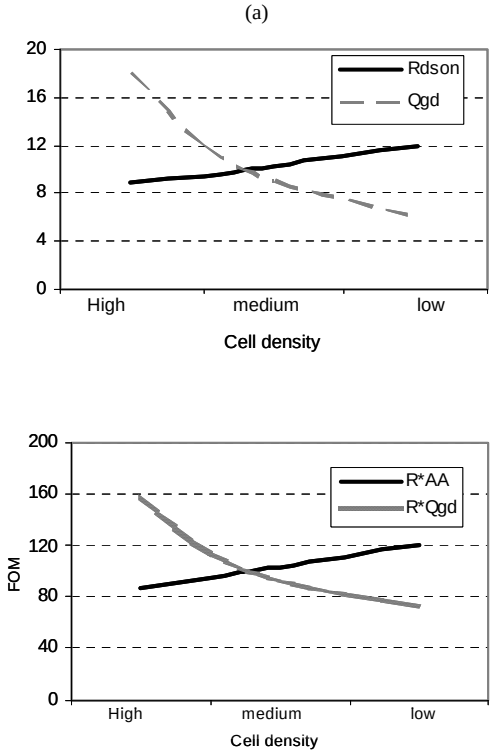
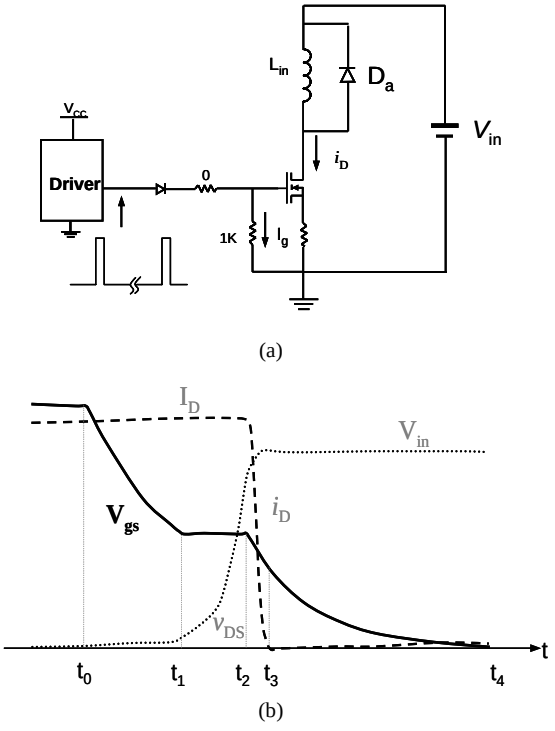


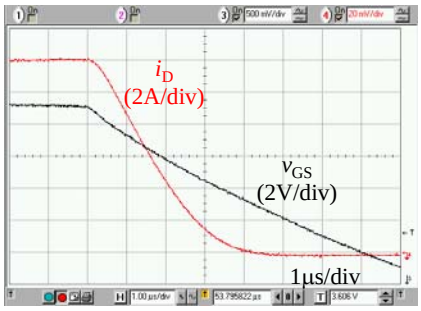
Fig. 1. Examples of MOSFET parameters as a function of cell density: (a) $R_{ds(on)}$ and Q_{gd}; (b) $R_{ds(on)}$ *Q_{gd} and R*AA.

Since Q_{gd} is typically several times larger than Q_{gs}, $R_{ds(on)}\cdot Q_{gd}$ product is often used as so-called figure of merit (FOM) for comparing various generations and types of power MOSFET [5]. Fig. 1 (a) shows the trends of $R_{ds(on)}$ and Q_{gd} as a function of cell density for a typical MOSFET with a fixed AA. It can be seen that Q_{gd} is a stronger function of cell density than $R_{ds(on)}$ – reduces faster with the reduced cell density than the increase of $R_{ds(on)}$. This means that lower cell density results in lower $R_{ds(on)}\cdot Q_{gd}$, as shown in Fig. 1(b), and indicates that better performance can be achieved with lower cell density. However, lower cell density results in higher $R_{ds(on)}\cdot$AA product, which means that a larger, more costly die is required to achieve a desired $R_{ds(on)}$. In order to come up with optimized cell density that provides the best tradeoff between the device performance and cost, we need to perform detailed and accurate power loss modeling for each target application.

III. MODELING OF NON-LINEAR SWITCHING TRANSITIONS

It is well known that switching loss is difficult to model accurately due to the non-linear characteristics of MOSFET parasitic inter-electrode capacitors. Existing loss modeling typically assumes linear transitions of switch current and voltage, which results in inaccurate results. To investigate the non-linear effect, a gate charge tester as shown in Fig. 2(a) was built. This tester can measure the voltage and current waveforms during the MOSFET turn-off transition. The transition time is enlarged by forcing the discharge C_{gs} via a 1K resistor. Fig. 2(b) illustrates the current and voltage transition waveforms for a device under test (DUT) in the tester. Fig. 2(c)(d) shows the measured current and voltage transition, respectively. As can be seen, the current and voltage transitions are highly non-linear. The switching loss would be exaggerated if the current and voltage transition were modeled along a straight line.





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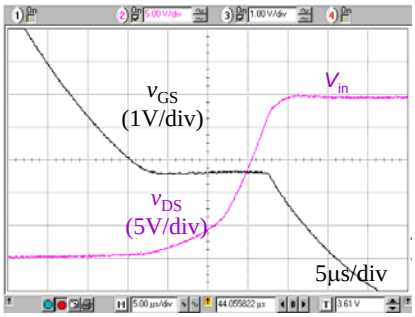


Fig. 2. The transition of switch voltage and current.
(a) the tester, (b) the typical waveforms, (c) (d) the measured waveform showing the non-linear transition of current and voltage.

A general equation to calculate the switching loss for non-linear voltage transition is shown in Eq. 1. It is not convenient if the integration part shows up in the loss model. To simplify the model, a K_v factor is introduced given by Eq. 2. A more accurate model for the voltage transition switching loss can be calculated by Eq. 3 with a simple mathematical manipulation of Eq. 1. Since Eq. 1 and Eq. 3 are equivalent, the introduction of K_v does not reduce the accuracy of Eq. 3. The K_v of the waveform showing in Fig. 2(d) is about 0.25. If a linear transition is assumed, the factor is 0.5. As can be seen, the switching loss would be overestimated by a factor of two if the non-linear effect is not included.

Similarly, the factor K_i can be introduced to define non-linear current transitions. The K_i of the waveform showing in Fig. 2(c) is about 0.32. The lumped K_i and K_v will be used to enhance the accuracy of the loss modeling.

$$P_{sw\_Qgd} = \frac{1}{t_2 - t_1}\int_{t_1}^{t_2} I_o \cdot V_d(t)\cdot dt \qquad \text{Eq. 1}$$

$$= \frac{1}{t_2 - t_1}\cdot I_o \cdot V_{in}\cdot(t_2 - t_1)\cdot\frac{\int_{t_1}^{t_2} V_d(t)\cdot dt}{(t_2 - t_1)\cdot V_{in}}$$

$$K_v = \frac{\int_{t_1}^{t_2} v_{DS}\,dt}{(t_2 - t_1)\cdot V_{in}} \qquad \text{Eq. 2}$$

$$P_{sw\_Qgd} = I_o \cdot V_{in} \cdot K_v \qquad \text{Eq. 3}$$

Knowing exact characteristics of the MOSFET gate driver IC is also very important for the switching speed. In orded to characterize the driver used in the target circuit, an external capacitor is connected to the driver simulating the C_{in} of a typical MOSFET. The major purpose is to find the equivalent internal resistor of the driver. For example, the bold line in Fig. 3 is the measured waveform of the voltage across the external capacitor. The thin line is the ideal curve of a RC circuit with a time constant τ=20. From the waveform, the equivalent gate resistor is calculated to be 2.9Ω during the turn off process. The equivalent resistor during turn on can also be found.

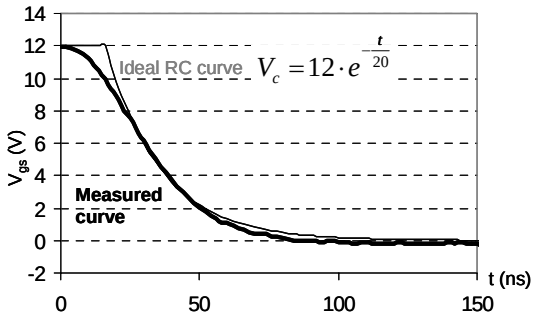


Fig. 3. Characterization of the driver.

IV. Power Loss Modeling and Verification for Power MOSFETs in DC Bus Converter

The first key target application is isolated dc-dc converters for 36V – 75V power distribution systems [6][7]. Fig. 4 shows an example of 50% duty cycle half-bridge DC Bus Converter. Compared to the traditional power conversion scheme, the intermediate DC bus converter provides improved efficiency, higher power density and overall system performance with reduced cost. In this application, the required voltage rating of the primary MOSFET and the secondary synchronous rectifier are 100V and 30V respectively.

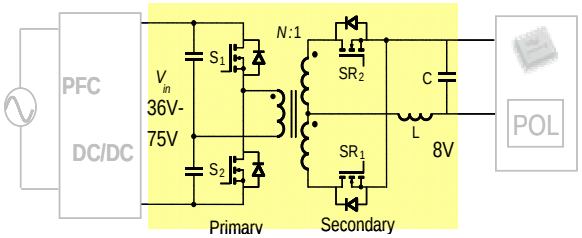


Fig. 4. The typical application addressed in this paper--- non-regulated DC bus converter.

A power loss model was developed for the dc bus converter. To verify the model accuracy, calculated results

were compared with experimental measurements. The experiments were carried out using two existing state-of-the-art parts. Fig. 5 shows the measured V_{GS} and V_{DS} during the turn-off process. Table 1 compares the calculated switching times and the real measured values. The maximum difference is 5%.

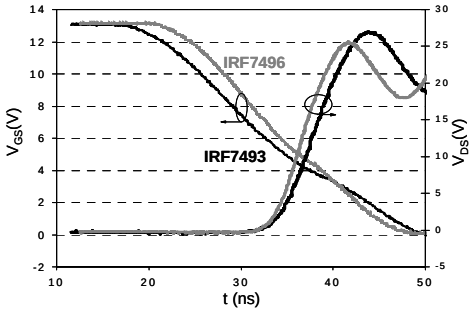


Fig. 5. The measured waveforms of the V_{GS} and V_{DS} for the verification of loss modeling.

Table 1. Calculated and masured turn off time.

	IRF7493	IRF7496
Calculated (ns)	8.6	6.2
Measured (ns)	7.5	6.5

Once the model is verified, the projected parameters for several devices of different cell density were plugged into the model to find the optimum performance and die sizes.

It is almost impossible to accurately measure the loss of the MOSFETs. The comparisons of the loss difference, however, is a easy and accurate way to compare performance of different devices. The DC-bus converter is operated under the same condition for IRF7493 and IRF7496 in the primary socket. The input voltage is 48V and the output voltage is 8V with Po=160W. The switching frequency is 220KHz. The test with IRF7493 has 0.42W less loss than the case with IRF7496. This measured result matches well with the calculated 0.41W.

As can be seen, the loss modeling has reasonable accuracy. With the verifications of switching time and loss difference showing in Table 1 and the comparison of the loss difference, we have good confidence to use the model for the new generation mid-voltage MOSFETs' optimization.

V. Optimization of the Power MOSFETs in DC Bus Converter

The predicted MOSFET parameters of the new generation are plugged in the model. Fig. 6 shows the loss of the primary MOSFET as a function of active area for the half bridge converter with different cell densities and active areas. The converter is operated with $48V_{in}$, $8V_{out}$, 20A and 220KHz switching frequency. Table 2 lists the optimized active area with different cell densities and the corresponding losses. It can be seen that option 2 offers 15% power loss reduction compared to option 1, with 23% die cost increase. Option 3, achieves only 3.6% additional power loss reduction over option 2, while further increasing the cost by 20%. It is an engineering judgment that the cell density with option 2 is the best design in terms of performance and cost.

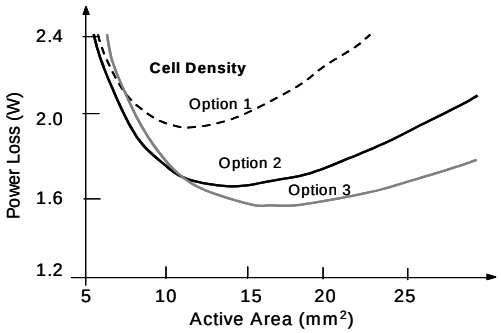


Fig. 6. Optimizing devices for isolated DC-DC converter.

Table 2. Optimized active area for different cell densities and the corresponding loss.

Cell Density	Optimized AA (mm^2)	Loss (W)
Option 1 (high)	11.7	1.95
Option 2 (medium)	**14.4**	**1.65**
Option 3 (low)	17.3	1.59

VI. Power Loss Modeling for Class-D Audio Amplifier

The Class D audio amplifier is a rapidly growing application because of its huge efficiency advantage over linear audio amplifiers. Fig. 7 shows an example of a car stereo system (one of the typical Class-D audio applications), where analog signal with small amplitude is converted to a series of PWM pulses to drive the power MOSFETs in a half-bridge or full-bridge configuration. The second-order filter then filters the high frequency PWM signal and generates enlarged analog signal to drive the high power speakers.

Class D audio amplifier is similar to the Sync buck converter. The difference is that Class D converter has a variable duty cycle, and that during the positive part of the input signal, the top switch is a 'ctrl FET' alike and is 'sync FET' alike in negative part [8], as shown in Fig. 8.

For the loss modeling of class-D amplifier, an equivalent DC current as given by

Eq. 4 is used to calculate the conduction loss during the positive line cycle. The shaded part in the formula is the equivalent RMS current for the conduction loss calculation.

This calculation method is mathematically accurate if the current ripple is neglected. Eq. 5 shows how the switching loss related to the miller charge is calculated. The shaded part in the formula is the equivalent DC current for switching loss calculation.

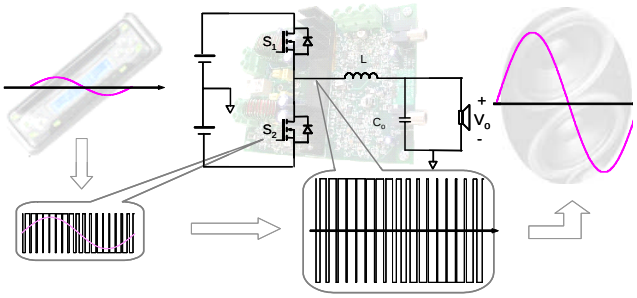


Fig. 7. Another typical application addressed in this paper---class D audio amplifier.

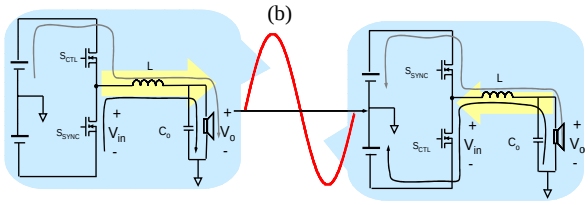


Fig. 8. The variations of power flow and operation points of a class-D audio amplifier.

$$P_{cond} = \sqrt{\frac{1}{T}\int_0^T [I_{pk}\cdot\sin(\omega\cdot t)]^2\cdot[D\cdot\sin(\omega\cdot t)]dt}^{\,2}\cdot R_{ds\_on} \qquad \text{Eq. 4}$$

$$P_{sw\_Qgd} = \frac{1}{T}\int_0^T [I_{pk}\cdot\sin(\omega\cdot t)]\,dt\cdot V_{in}\cdot K_v\cdot T_{\text{(} \qquad \text{Eq. 5}$$

Fig. 9 shows the design tradeoff based on loss modeling for 200W class D converter with 65V DC bus voltage, 395KHz switching frequency. Table 3 shows the loss breakdown and optimized active area. As can be seen, the cell density of option 2 is the best choice for the cost and performance tradeoff.

The option 2 of the cell density is the best choice for both DC bus converter and the class D audio amplifier applications. Therefore, single design with the cell density identified by the modeling can be adopted. Single design can dramatically reduce the design cycle for new products. This single design does not compromise the performance because the optimized design for each application is achieved by varying the active areas. A family of new generation devices in the DirectFET™ package is generated covering multiple applications. DirectFET™ package meets the requirements of high power/current density with reduced size, and electrical and thermal resistance of the package [9][10].

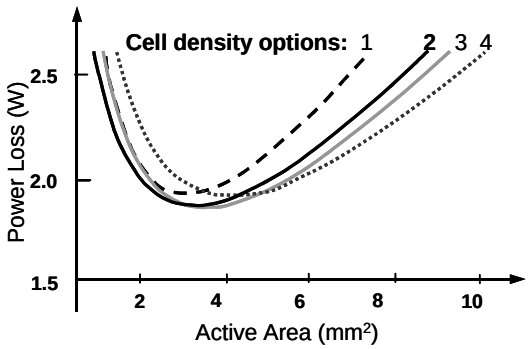


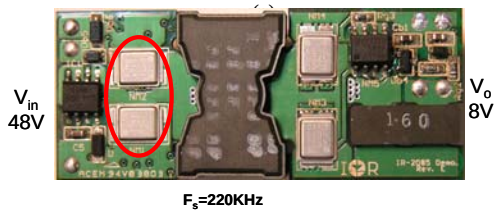
Fig. 9. Optimizing devices for class D audio amplifier.

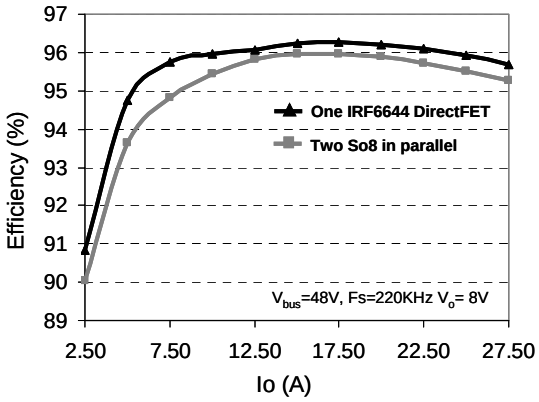
Table 3. Loss comparison of class D audio amplifier.

Cell Density	Optimized AA (mm^2)	Loss (W)
Option 1 (high)	2.71	1.92
Option 2 (medium)	**3.08**	**1.85**
Option 3 (low)	3.61	1.84
Option 4 (extra low)	3.83	1.86

VII. EXPERIMENTAL RESULTS

Two devices with the same cell density and different active area are manufactured as leading devices for new generation devices for the targeted applications. The IRF6644 has 13.8mm^2 AA in a medium-can DirectFET™ package, which is for HB DC-DC converter, as shown in Fig. 10(a). Fig. 10(b) shows the measured efficiency improvement with 400LFM by replacing the two paralleled primary switches of HB DC-DC converter with a single DirectFET™ IRF6644. As can be seen, using the new IRF6644 results in 0.3% higher efficiency at 200W load. This can be translated into 20% power loss reduction of the device in the loss model. Fig. 10(c) shows the measured temperature at the full load condition. The temperature is about 20°C lower with one new IRF6644 than the case with two SO-8 in parallel. The secondary also has about 10°C temperature difference due the thermal coupling on the same small PCB board.





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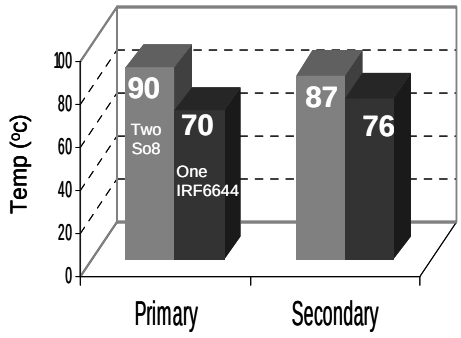


(c)

Fig. 10. Measure efficiency and device temperature for HB unregulated converter: (a) the picture of the DC bus converter, (b) measured efficiency and (c) measured device temperature.

Another device with a smaller AA is also manufactured - the IRF6665 in small-can DirectFET™ package, optimized for class-D audio amplifiers.

The 100W half-bridge class D audio amplifier using the new IRF6665 is demonstrated without any heat sink and airflow. The operation conditions are: V_{bus}=±35V; R_{load}=8Ω, and F_s=400KHz. The case temperature is 105°C, which is a 83°C above the 21°C ambient temperature. With one eighth of the full power, the case temperature is 58°C, or 39°C above ambient.

Fig. 12 shows the efficiency curves covering from 10W to 160W with 4Ω load. The operation switching frequency is 395KHz. It can be seen that the efficiency improvement with the new developed device is about 2% higher than the current best practice.

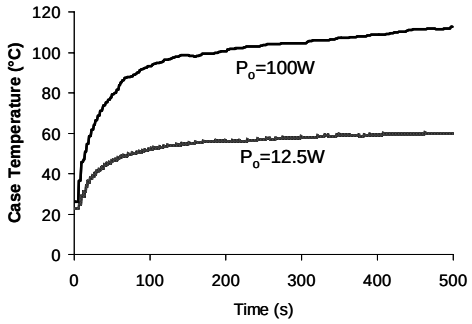
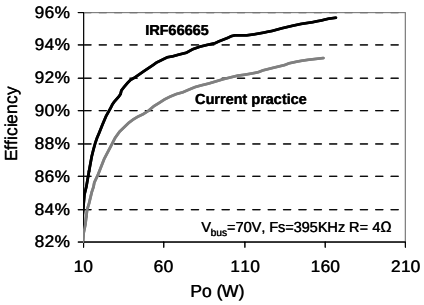


Fig. 11. The temperature measurement of the device without heatsink..

(a)



(b)

Fig. 12. Prototype and measured efficiency of class D audio amplifier: (a) the photograph of the class D audio amplifier, (b) the measured efficiency.

Another major benefit of using the IRF6665 DirectFET™ in class D application is the low total harmonic distortion (THD) and noise level. As we know, the output distortion is tightly related to the gate charge and the dead time [11]. The low charge of the IRF6665 contributes significantly to the distortion reduction. At 1/8 of the normalized power, the total distortion (THD +Noise) is 0.0057% with a 4Ω load and 0.0031% with a 8Ω load.

VIII. CONCLUSIONS

In this paper, a procedure for developing and optimizing a new generation mid-voltage power MOSFETs covering multiple applications is described. The optimization is based on detailed device characterization and loss modeling. The

accuracy of loss models was enhanced by including nonlinear voltage and current transitions into switching loss calculation and verified with existing devices. Projected parameters of MOSFETs with new technology are input into the verified models for cell density and active area optimization. The modeling and experimental results show that with minimal power loss trade-offs it is possible to address multiple applications with a single cost-effective power MOSFET design, while varying only the size of the die.

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