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New Trench MOSFET Technology for DC-DC Converter Applications

Ling Ma, Adam Amali, Siddharth Kiyawat, Ashita Mirchandani,
Donald He, Naresh Thapar, Ritu Sodhi, Kyle Spring, Dan Kinzer
International Rectifier Corporation, 233 Kansas Street, El Segundo, CA 90245

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Abstract. New trench MOSFET technology presented in this paper includes several major technological breakthroughs that significantly improved device performance in DC-DC converter applications. The figure of merit R*AA has reached as low as 12 mOhm.mm^2 for a 30 VN SyncFET and R*Qg is only 75 mOhm.nC for a 30VN Control FET, one of the lowest reported in industry.

I. INTRODUCTION

The ever-increasing demands for greater power supply and longer lasting battery-powered electronic devices have made efficiency in power management system one of most challenging areas for engineers. The requirements on discrete power MOSFET in power management system continue to push manufacturers to produce parts with lower on-resistance, lower gate charge and higher current capability. Significant progress has been reported [1-4] on the efforts to reduce feature size and hence, device on-resistance. The development presented here is the latest effort to meet the challenges of power conversion.

The new generation of trench power MOSFET technology developed by International Rectifier offers ultra-low on-resistance, gate charge and superior current capability. As a result, applications such as switching in 1MHz frequency are possible without excessively heating up the board.

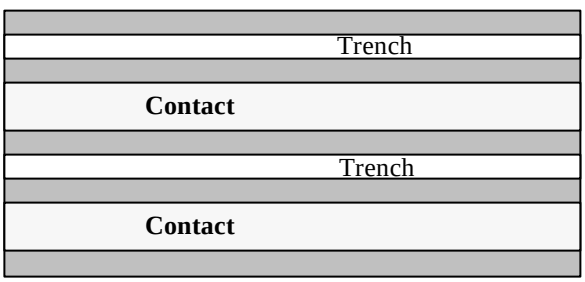

Figure 1. Device topology

II. DEVICE DESIGN AND PROCESS

Device topology. Though many different topologies such as hexagonal, cellular, stripes, etc. have been widely used, a stripe topology was selected for this new technology for better Rdson and gate charge trade-off (see Figure 1).

Recessed Termination Structure. This innovative termination structure eliminated the need for P+ guard ring. In addition, with the field oxide and field plate recessed below the silicon surface, the manufacturability of sub-micron features is significantly improved. (Figure 2)

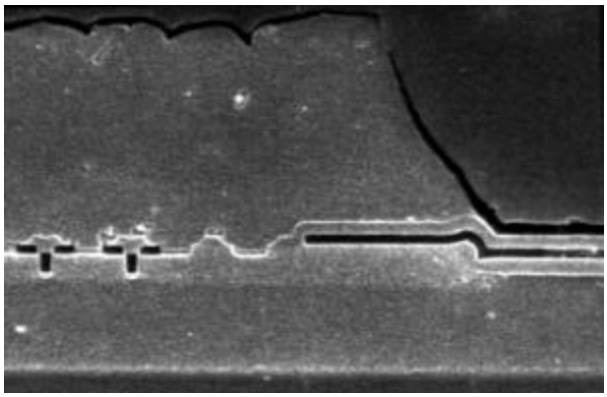

Figure 2. Recessed termination structure

This recessed structure can significantly reduce the electrical field crowding at termination, thus eliminating the need for P+ implant guard rings without compromising the device breakdown voltage and ruggedness performance. Typical avalanche energy measured for this termination structure was over 1J for a maximum die in a DPAK.

The field oxide is grown using LOCOS process after the termination trench has been etched. By placing the field oxide beneath the surface of active area, it dramatically improved wafer planarity at active trench lithography stage.

Reduction in Feature Sizes. The new technology offers a significant reduction in feature size, when compared to the previous generation of technology. As a result, the new technology delivers even higher channel density and yet keeps gate charges low, especially the Q_{GD} and Q_{SWITCH}.

The much improved wafer surface planarity at trench lithography stage, because of the recessed termination structure, enabled further reduction of trench width by 20%. In the meantime, the trench depth was reduced as well to maximize the gain in overall device performances.

While the feature sizes such as trench width and depth are being reduced, the gate oxide integrity remains high. The dielectric integrity is over 7MV/cm.

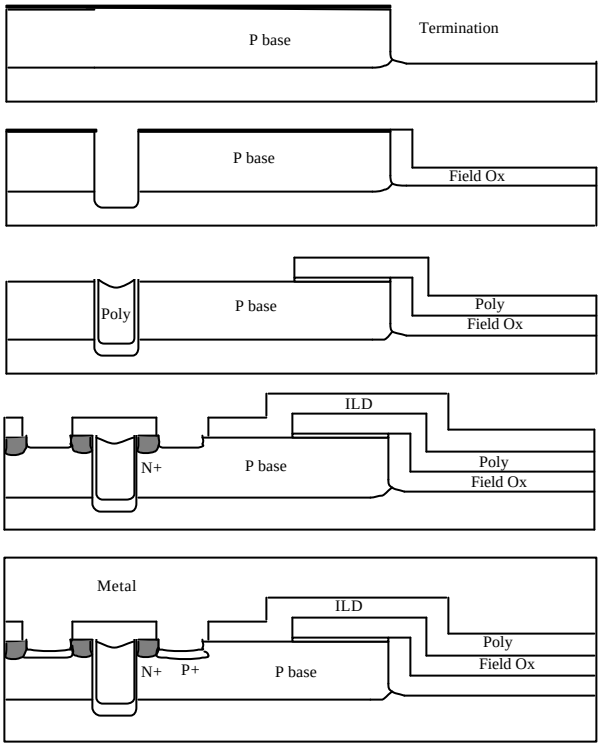

Figure 3. Schematic of process flow

Process Highlights. The termination trenches and active trenches are defined with a nitride hard mask. The p body was implanted through screen oxide into n-type epi. After active trenches are etched, a proprietary process was used to form thick oxide at bottom of the trenches. Polycrystalline silicon was deposited and etched back after gate oxide growth. Then the N+ source was implanted and p body contact was formed using photo-defined dry etch process. Finally aluminum was sputtered to form the gate and source electrodes (see Figure 3).

Contact Formation Process. Using a novel contact process sequence, the channel length was further optimized to reduce the device on-resistance. The new process sequence made it possible to have 100% metal step-coverage in spite of the sub-micron feature size (Figure 4). It also enables the use of thinner epi to further reduce on-resistance.

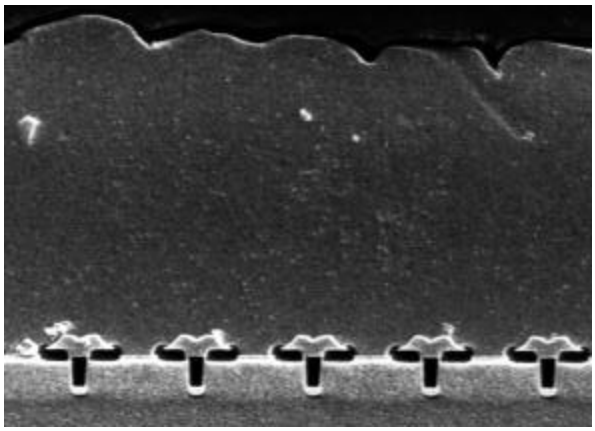

Figure 4. Active cells and metal step coverage

Epi/Substrate Optimization. Further optimization of substrate resistivity provided almost 50% reduction in substrate resistance. Several process integration issues have to be resolved in order to prevent substrate dopant outgassing and cross contamination. The thermal budget of the entire process flow has to be carefully controlled to limit the dopant out-diffusion from substrate to epi layer. Another benefit of reduced epi thickness is the reduction in Qrr, which is very critical at high frequencies

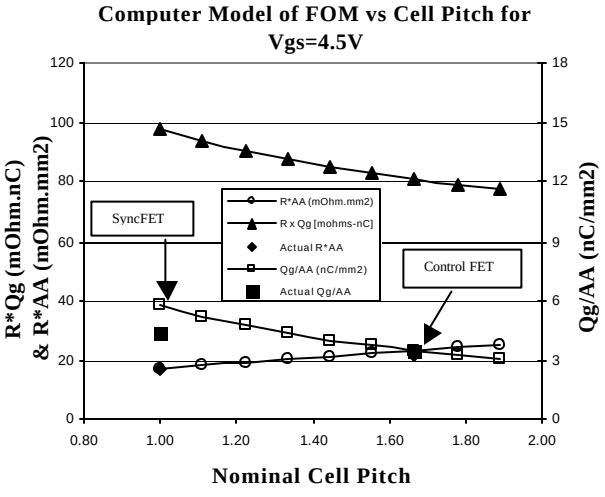

Figure 5. Device figures of merit as a function of cell pitch

III. EXPERIMENTAL RESULTS

The results presented here are of a 30V, N-channel MOSFET unless otherwise specified. The cell pitch was individually optimized for the Control FET and Synchronous FET, to achieve the best in-circuit performance (see Fig. 5). A summary of key figures of merit for these two cell pitches is tabulated in Table 1.

Parameter	Unit	Control FET	Sync FET
R_{Si}*AA @ 10V_{GS}	mOhm*mm^2	16	12
R_{Si}*AA @ 4.5V_{GS}	mOhm*mm^2	22	17
R_{Si}*Q_G @ 4.5V_{GS}	mOhm*nC	75	77
Q_G/AA @ 4.5V_{GS}	nC/mm^2	3.4	4.7
Q_{GD}/AA @ 4.5V_{GS}	nC/mm^2	0.9	1.4
Q_{switch}/AA @ 4.5Vgs	nC/mm^2	1.3	1.8

Table 1. Summary of Figures of Merit for 30VN

Further performance optimization was achieved by proper design of key device features, e.g. trench depth, trench width, junction depths, etc. At a given p-base depth, the deeper the trench depth, the lower the on-resistance. However the deeper trench comes with a higher gate charge. Experimental data indicated that an optimal combination of on-resistance and gate charge can be obtained, as shown in Figure 6.

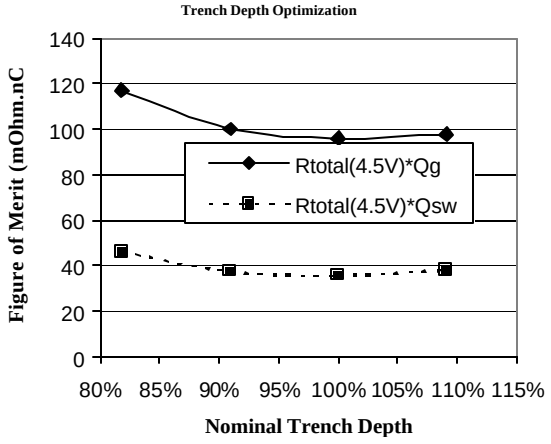

Figure 6. R*Qg as a function of trench depth

To achieve the lowest possible on-resistance for a given die size in Sync-FET socket, narrow cell pitch was used. Combined with shallower trench depth, low resistivity substrate, and optimized epi layer, an R_{Si}*AA product of 12 mOhm.mm^2 for 10Vgs and 17 mOhm.mm^2 for 4.5Vgs were obtained. These values are among the lowest that have been reported [5, 6 & 7] (See Figure 7). However this has been achieved without significantly increasing the gate charge.

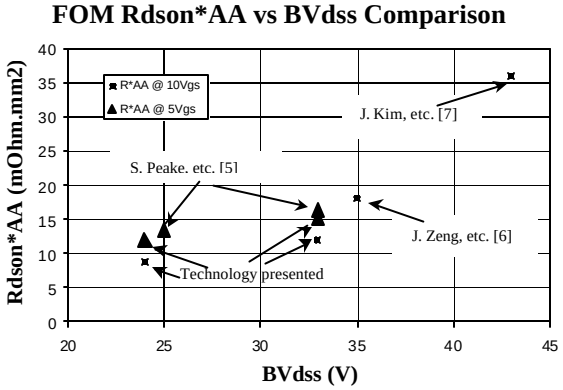

Figure 7. Rdson*AA vs BVdss

In Control-FET socket, switching loss is the dominant component of the total power loss. As the switching frequency increases, the requirements on the Control FET become more stringent. In designing the Control-FET, making the right trade-off between the Rdson and gate charge is very critical. The advantage of this new technology is that it enables the improvement in both R*AA and Qg/AA. The Control-FET can be made with low gate charge and low on-resistance. The optimized control FET design gave an R*Qg product as low as 75 mOhm.nC.

In addition, with the proper epi optimization, the Qrr for our new technology has been reduced from 13.4nC/mm^2 to 5.1nC/mm^2 (see Figure 8). This reduction in Qrr is very significant as the switching frequency goes up (>1MHz).

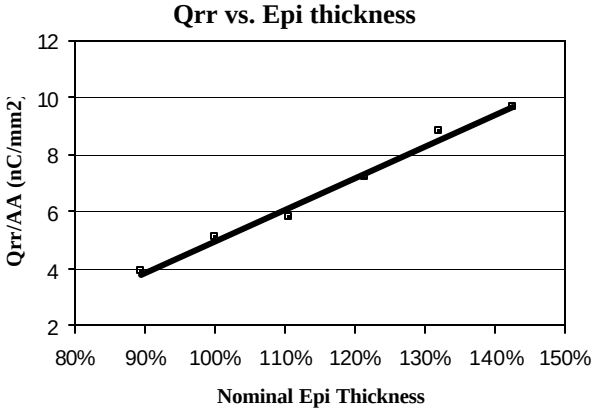

Figure 8. Qrr as a function of epi thickness

Figures 9 and 10 show the in-circuit efficiency results for the new technology as compared to the prior benchmark at different switching frequencies. As seen in Fig. 9, the new Control FET offers upto 1% higher

efficiency at 200kHz and upto 2% higher efficiency at 1MHz. Figure 10 shows that the new Sync FET offers 0.5% to 1.5% better efficiency at 200kHz and 750kHz.

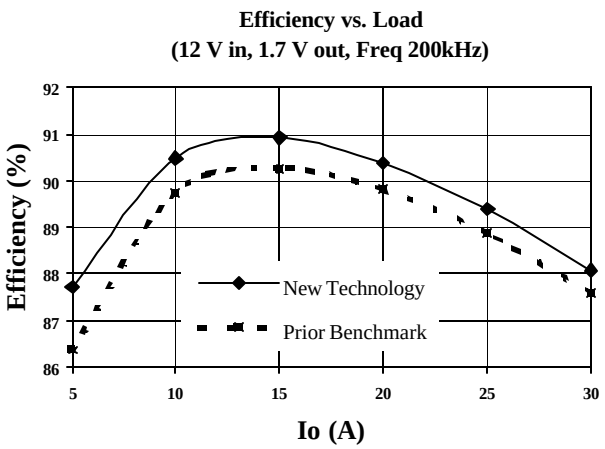

Figure 9a. In-circuit efficiency comparison for the Control FET at 200kHz

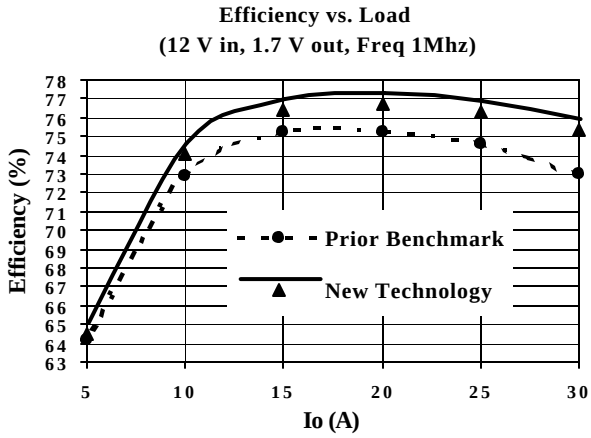

Figure 9b. In-circuit efficiency comparison for the Control FET at 1MHz

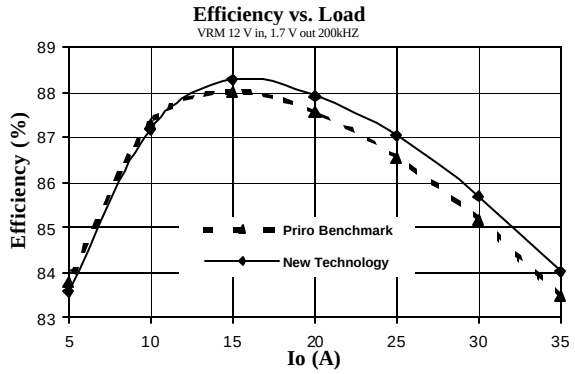

Figure 10a. In-circuit efficiency comparison for the Sync FET at 200kHz

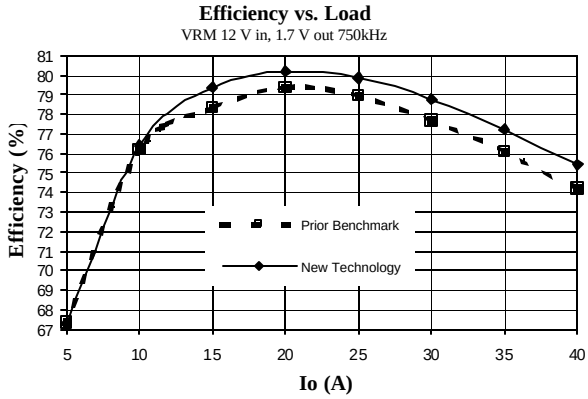

Figure 10b. In-circuit efficiency comparison for the Sync FET at 750kHz

IV. CONCLUSION

These technological breakthroughs enable us to manufacture devices with superior performance. For example, the figure of merit R*AA has reached as low as 12 mOhm.mm^2 for a 30V N-channel FET when optimized for SyncFET. Combined with IR's proprietary DirectFET package [8], it can deliver a peak current of **113** Amperes with a footprint that is no more than that of a SO-8. Yet when optimized for control FET, R*Qg is only 75 mOhm.nC for a 30VN N-channel FET. The reverse recovery charge Qrr/AA is also reduced from 13.4 nC/mm^2 to 5.1 nC/mm^2 due to optimized epi thickness. This reduced reverse recovery charge is very critical for high switch frequency (>=1MHz). All these advancements in new technology directly translate into much improved in-circuit efficiency at various switch frequencies.

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