Data Sheet No. PD60265

International
IOR Rectifier

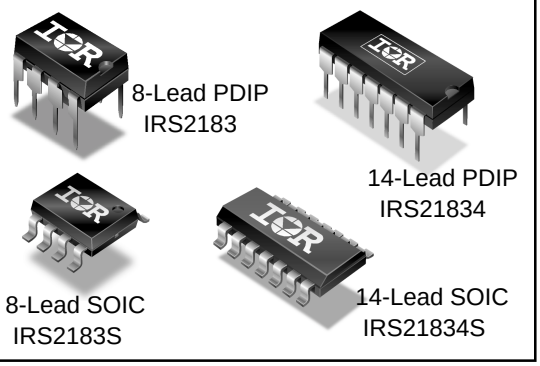
IRS2183/IRS21834(S)PbF

HALF-BRIDGE DRIVER

Features

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V and 5 V input logic compatible
- Matched propagation delay for both channels
- Logic and power ground +/- 5 V offset
- Lower di/dt gate driver for better noise immunity
- Output source/sink current capability 1.4 A/1.8 A
- RoHS compliant

Packages



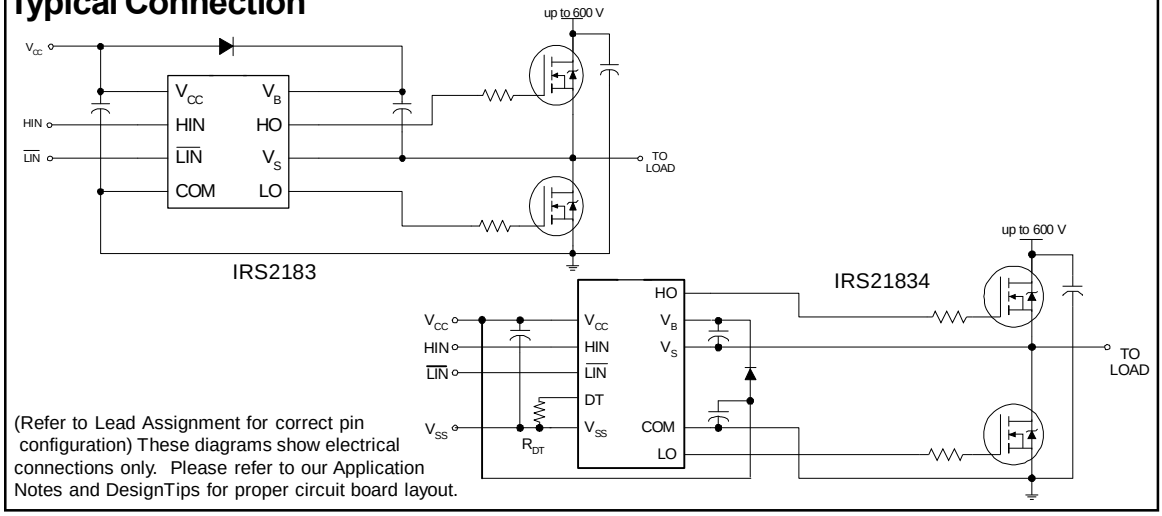
Description

The IRS2183/IRS21834 are high voltage, high speed power MOSFET and IGBT drivers with dependent high-side and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

Feature Comparison

Part	Input logic	Cross-conduction prevention logic	Deadtime (ns)	Ground Pins	t_{on}/t_{off} (ns)
2181	HIN/LIN	no	none	COM	180/220
21814				V_{SS}/COM	
2183	HIN/$\overline{\text{LIN}}$	yes	Internal 400	COM	180/220
21834			Program 400-5000	V_{SS}/COM	
2184	IN/$\overline{\text{SD}}$	yes	Internal 400	COM	680/270
21844			Program 400-5000	V_{SS}/COM	

Typical Connection



(Refer to Lead Assignment for correct pin configuration) These diagrams show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High-side floating absolute voltage		-0.3	620 (Note 1)	V
V_S	High-side floating supply offset voltage		V_B - 20	V_B + 0.3	
V_{HO}	High-side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low-side and logic fixed supply voltage		-0.3	20 (Note 1)	
V_{LO}	Low-side output voltage		-0.3	V_{CC} + 0.3	
DT	Programmable deadtime pin voltage (IR21834 only)		V_{SS} - 0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN & $\overline{LIN}$)		V_{SS} - 0.3	V_{CC} + 0.3	
V_{SS}	Logic ground (IR21834 only)		V_{CC} - 20	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25$ °C	(8-lead PDIP)	—	1.0	W
		(8-lead SOIC)	—	0.625	
		(14-lead PDIP)	—	1.6	
		(14-lead SOIC)	—	1.0	
Rth_{JA}	Thermal resistance, junction to ambient	(8-lead PDIP)	—	125	°C/W
		(8-lead SOIC)	—	200	
		(14-lead PDIP)	—	75	
		(14-lead SOIC)	—	120	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-50	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Note 1: All supplies are fully tested at 25 V and an internal 20 V clamp exists for each supply.

Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating are tested with all supplies biased at 15 V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High-side floating supply offset voltage	Note 2	600	
V_{HO}	High-side floating output voltage	V_S	V_B	
V_{CC}	Low-side and logic fixed supply voltage	10	20	
V_{LO}	Low-side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (HIN & $\overline{LIN}$)	V_{SS}	V_{CC}	
DT	Programmable deadtime pin voltage (IR21834 only)	V_{SS}	V_{CC}	
V_{SS}	Logic ground (IR21834 only)	-5	5	
T_A	Ambient temperature	-40	125	°C

Note 2: Logic operational for V_S of -5 V to +600 V. Logic state held for V_S of -5 V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15 V, V_{SS} = COM, C_L = 1000 pF, T_A = 25 °C, DT = V_{SS} unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	180	270	ns	V_S = 0V
t_{off}	Turn-off propagation delay	—	220	330		V_S = 0V or 600V
MT	Delay matching | t_{on} - t_{off} |	—	0	35		
t_r	Turn-on rise time	—	40	60		V_S = 0 V
t_f	Turn-off fall time	—	20	35		
DT	Deadtime: LO turn-off to HO turn-on(DT_{LO-HO}) &	280	400	520		R_{DT}= 0 Ω
	HO turn-off to LO turn-on (DT_{HO-LO})	4	5	6	µs	R_{DT} = 200 kΩ (IR21834)
MDT	Deadtime matching = | DT_{LO-HO} - DT_{HO-LO} |	—	0	50	ns	R_{DT}=0 Ω
		—	0	600		R_{DT} = 200kΩ (IR21834)

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15 V, V_{SS} = COM, DT= V_{SS} and T_A = 25 °C unless otherwise specified. The V_{IL}, V_{IH}, and I_{IN} parameters are referenced to V_{SS}/COM and are applicable to the respective input leads: HIN and $\overline{\text{LIN}}$. The V_O, I_O, and Ron parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic “1” input voltage for HIN & logic “0” for $\overline{\text{LIN}}$	2.5	—	—	V	V_{CC} = 10 V to 20 V
V_{IL}	Logic “0” input voltage for HIN & logic “1” for $\overline{\text{LIN}}$	—	—	0.8		
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	—	1.4		I_O = 0 A
V_{OL}	Low level output voltage, V_O	—	—	0.2		I_O = 20 mA
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600 V
I_{QBS}	Quiescent V_{BS} supply current	20	60	150		V_{IN} = 0 V or 5 V
I_{QCC}	Quiescent V_{CC} supply current	0.4	1.0	1.6	mA	
I_{IN+}	Logic “1” input bias current	—	25	60	µA	HIN = 5 V, $\overline{\text{LIN}}$ = 0 V
I_{IN-}	Logic “0” input bias current	—	—	5.0		HIN = 0 V, $\overline{\text{LIN}}$ = 5 V
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	8.0	8.9	9.8	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	7.4	8.2	9.0		
V_{CCUVH} V_{BSUVH}	Hysteresis	0.3	0.7	—		
I_{O+}	Output high short circuit pulsed current	1.4	1.9	—	A	V_O = 0 V, PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	1.8	2.3	—		V_O = 15 V, PW ≤ 10 µs