Features

• Floating channel designed for bootstrap operation
• Fully operational to +600 V
• Tolerant to negative transient voltage, dV/dt immune
• Gate drive supply range from 10 V to 20 V
• Undervoltage lockout
• 3.3 V, 5 V, and 15 V logic input compatible
• Matched propagation delay for both channels
• Outputs in phase with inputs
• RoHS compliant

Description

The IRS2101 is a high voltage, high speed power MOSFET and IGBT driver with independent high-side and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

Typical Connection

(Refer to Lead Assignments for correct pin configuration). This diagram shows electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

HIGH AND LOW SIDE DRIVER

Product Summary

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOFFSET</td>
<td>600 V max.</td>
</tr>
<tr>
<td>IO+/-</td>
<td>130 mA/270 mA</td>
</tr>
<tr>
<td>VOUT</td>
<td>10 V - 20 V</td>
</tr>
<tr>
<td>ton/off (typ.)</td>
<td>160 ns/150 ns</td>
</tr>
<tr>
<td>Delay Matching</td>
<td>50 ns</td>
</tr>
</tbody>
</table>

Packages

- 8-Lead SOIC
  IRS2101S
- 8-Lead PDIP
  IRS2101

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Absolute Maximum Ratings
Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_B )</td>
<td>High-side floating supply voltage</td>
<td>-0.3</td>
<td>625</td>
<td>V</td>
</tr>
<tr>
<td>( V_S )</td>
<td>High-side floating supply offset voltage</td>
<td>( V_B - 25 )</td>
<td>( V_B + 0.3 )</td>
<td></td>
</tr>
<tr>
<td>( V_{HO} )</td>
<td>High-side floating output voltage</td>
<td>( V_S - 0.3 )</td>
<td>( V_B + 0.3 )</td>
<td></td>
</tr>
<tr>
<td>( V_{CC} )</td>
<td>Low-side and logic fixed supply voltage</td>
<td>-0.3</td>
<td>25</td>
<td></td>
</tr>
<tr>
<td>( V_{LO} )</td>
<td>Low-side output voltage</td>
<td>-0.3</td>
<td>( V_{CC} + 0.3 )</td>
<td></td>
</tr>
<tr>
<td>( V_{IN} )</td>
<td>Logic input voltage (HIN &amp; LIN)</td>
<td>-0.3</td>
<td>( V_{CC} + 0.3 )</td>
<td></td>
</tr>
<tr>
<td>( dV_S/dt )</td>
<td>Allowable offset supply voltage transient</td>
<td>—</td>
<td>50</td>
<td>V/ns</td>
</tr>
<tr>
<td>( P_D )</td>
<td>Package power dissipation @ ( T_A \leq +25 \ ^\circ C )</td>
<td>—</td>
<td>1.0</td>
<td>W</td>
</tr>
<tr>
<td>( R_{thJA} )</td>
<td>Thermal resistance, junction to ambient</td>
<td>(8 lead PDIP)</td>
<td>—</td>
<td>0.625</td>
</tr>
<tr>
<td>( T_J )</td>
<td>Junction temperature</td>
<td>(8 lead SOIC)</td>
<td>—</td>
<td>125</td>
</tr>
<tr>
<td>( T_S )</td>
<td>Storage temperature</td>
<td>(8 lead PDIP)</td>
<td>—</td>
<td>200</td>
</tr>
<tr>
<td>( T_L )</td>
<td>Lead temperature (soldering, 10 seconds)</td>
<td>(8 lead SOIC)</td>
<td>—</td>
<td>300</td>
</tr>
</tbody>
</table>

Recommended Operating Conditions
The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The \( V_S \) offset rating is tested with all supplies biased at a 15 V differential.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_B )</td>
<td>High-side floating supply absolute voltage</td>
<td>( V_S + 10 )</td>
<td>( V_S + 20 )</td>
<td>V</td>
</tr>
<tr>
<td>( V_S )</td>
<td>High-side floating supply offset voltage</td>
<td>Note 1</td>
<td>600</td>
<td></td>
</tr>
<tr>
<td>( V_{HO} )</td>
<td>High-side floating output voltage</td>
<td>( V_S )</td>
<td>( V_B )</td>
<td></td>
</tr>
<tr>
<td>( V_{CC} )</td>
<td>Low-side and logic fixed supply voltage</td>
<td>10</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>( V_{LO} )</td>
<td>Low-side output voltage</td>
<td>0</td>
<td>( V_{CC} )</td>
<td></td>
</tr>
<tr>
<td>( V_{IN} )</td>
<td>Logic input voltage (HIN &amp; LIN)</td>
<td>0</td>
<td>( V_{CC} )</td>
<td></td>
</tr>
<tr>
<td>( T_A )</td>
<td>Ambient temperature</td>
<td>-40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

Note 1: Logic operational for \( V_S \) of -5 V to +600 V. Logic state held for \( V_S \) of -5 V to -\( V_{BS} \). (Please refer to the Design Tip DT97-3 for more details).
## Dynamic Electrical Characteristics

$V_{BIAS} (V_{CC}, V_{BS}) = 15 \, V$, $C_L = 1000 \, pF$ and $T_A = 25 \, ^{\circ}C$ unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{on}$</td>
<td>Turn-on propagation delay</td>
<td>—</td>
<td>160</td>
<td>220</td>
<td>ns</td>
<td>$V_S = 0 , V$</td>
</tr>
<tr>
<td>$t_{off}$</td>
<td>Turn-off propagation delay</td>
<td>—</td>
<td>150</td>
<td>220</td>
<td>ns</td>
<td>$V_S = 600 , V$</td>
</tr>
<tr>
<td>$t_r$</td>
<td>Turn-on rise time</td>
<td>—</td>
<td>70</td>
<td>170</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_f$</td>
<td>Turn-off fall time</td>
<td>—</td>
<td>35</td>
<td>90</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$MT$</td>
<td>Delay matching, HS &amp; LS turn-on/off</td>
<td>—</td>
<td>—</td>
<td>50</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Static Electrical Characteristics

$V_{BIAS} (V_{CC}, V_{BS}) = 15 \, V$ and $T_A = 25 \, ^{\circ}C$ unless otherwise specified. The $V_{IN}$, $V_{TH}$, and $I_{IN}$ parameters are referenced to COM. The $V_O$ and $I_O$ parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>Logic “1” input voltage</td>
<td>2.5</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>$V_{CC} = 10 , V$ to $20 , V$</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Logic “0” input voltage</td>
<td>—</td>
<td>—</td>
<td>0.8</td>
<td>V</td>
<td>$I_O = 2 , mA$</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>High level output voltage, $V_{BIAS} - V_O$</td>
<td>—</td>
<td>0.05</td>
<td>0.2</td>
<td>V</td>
<td>$V_B = V_S = 600 , V$</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low level output voltage, $V_O$</td>
<td>—</td>
<td>0.02</td>
<td>0.1</td>
<td>V</td>
<td>$V_I = 0 , V$ or $5 , V$</td>
</tr>
<tr>
<td>$I_{LK}$</td>
<td>Offset supply leakage current</td>
<td>—</td>
<td>—</td>
<td>50</td>
<td>µA</td>
<td>$V_{O} = 0 , V$</td>
</tr>
<tr>
<td>$I_{QBS}$</td>
<td>Quiescent $V_{BS}$ supply current</td>
<td>—</td>
<td>30</td>
<td>55</td>
<td>µA</td>
<td>$V_{IN} = 0 , V$ or $5 , V$</td>
</tr>
<tr>
<td>$I_{QCC}$</td>
<td>Quiescent $V_{CC}$ supply current</td>
<td>—</td>
<td>150</td>
<td>270</td>
<td>µA</td>
<td>$V_{IN} = 5 , V$</td>
</tr>
<tr>
<td>$I_{IN+}$</td>
<td>Logic “1” input bias current</td>
<td>—</td>
<td>3</td>
<td>10</td>
<td>µA</td>
<td>$V_{IN} = 0 , V$</td>
</tr>
<tr>
<td>$I_{IN-}$</td>
<td>Logic “0” input bias current</td>
<td>—</td>
<td>—</td>
<td>5</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>$V_{CCUV+}$</td>
<td>$V_{CC}$ supply undervoltage positive going threshold</td>
<td>8</td>
<td>8.9</td>
<td>9.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{CCUV-}$</td>
<td>$V_{CC}$ supply undervoltage negative going threshold</td>
<td>7.4</td>
<td>8.2</td>
<td>9</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{O+}$</td>
<td>Output high short circuit pulsed current</td>
<td>130</td>
<td>290</td>
<td>—</td>
<td>mA</td>
<td>$V_O = 0 , V$</td>
</tr>
<tr>
<td>$I_{O-}$</td>
<td>Output low short circuit pulsed current</td>
<td>270</td>
<td>600</td>
<td>—</td>
<td>mA</td>
<td>$V_O = 15 , V$</td>
</tr>
</tbody>
</table>

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Lead Definitions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>HIN</td>
<td>Logic input for high-side gate driver output (HO), in phase</td>
</tr>
<tr>
<td>LIN</td>
<td>Logic input for low-side gate driver output (LO), in phase</td>
</tr>
<tr>
<td>VB</td>
<td>High-side floating supply</td>
</tr>
<tr>
<td>HO</td>
<td>High-side gate drive output</td>
</tr>
<tr>
<td>VS</td>
<td>High-side floating supply return</td>
</tr>
<tr>
<td>VCC</td>
<td>Low-side and logic fixed supply</td>
</tr>
<tr>
<td>LO</td>
<td>Low-side gate drive output</td>
</tr>
<tr>
<td>COM</td>
<td>Low-side return</td>
</tr>
</tbody>
</table>

Lead Assignments

<table>
<thead>
<tr>
<th></th>
<th>8 Lead PDIP</th>
<th>8 Lead SOIC</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRS2101PbF</td>
<td><img src="diagram1.png" alt="Diagram" /></td>
<td><img src="diagram2.png" alt="Diagram" /></td>
</tr>
<tr>
<td>Part Number</td>
<td>IRS2101SPbF</td>
<td></td>
</tr>
</tbody>
</table>
Figure 1. Input/Output Timing Diagram

Figure 2. Switching Time Waveform Definitions

Figure 3. Delay Matching Waveform Definitions
Figure 6A. Turn-On Time vs. Temperature

Figure 6B. Turn-On Time vs. Supply Voltage

Figure 6C. Turn-On Time vs. Input Voltage

Figure 7A. Turn-Off Time vs. Temperature

Figure 7B. Turn-Off Time vs. Supply Voltage

Figure 7C. Turn-Off Time vs. Input Voltage
Figure 13A. Logic "0" Input Bias Current vs. Temperature

Figure 13B. Logic "0" Input Bias Current vs. Voltage

Figure 14A. High Level Output Voltage vs. Temperature

Figure 14B. High Level Output vs. Supply Voltage

Figure 15A. Low Level Output Voltage vs. Temperature

Figure 15B. Low Level Output vs.Supply Voltage
Figure 16A. Offset Supply Current vs. Temperature

Figure 16B. Offset Supply Current vs. Voltage

Figure 17A. V_{BS} Supply Current vs. Temperature

Figure 17B. V_{BS} Supply Current vs. Voltage

Figure 18A. V_{CC} Supply Current vs. Temperature

Figure 18B. V_{CC} Supply Current vs. Voltage
Figure 19A. Logic "1" Input Current vs. Temperature

Figure 19B. Logic "1" Input Current vs. Voltage

Figure 20A. Logic "0" Input Current vs. Temperature

Figure 20B. Logic "0" Input Current vs. Voltage

Figure 21A. V\textsubscript{CC} Undervoltage Threshold(+) vs. Temperature

Figure 21B. V\textsubscript{CC} Undervoltage Threshold(-) vs. Temperature
Figure 22A. Output Source Current vs. Temperature

Figure 22B. Output Source Current vs. Supply Voltage

Figure 23A. Output Sink Current vs. Temperature

Figure 23B. Output Sink Current vs. Supply Voltage
8 Lead PDIP

NOTES:
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS.
6. MOLD PROTRUSIONS SHALL NOT EXCEED 0.25 [.010].
7. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS.

8 Lead SOIC

NOTES:
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-002AA.
# Tape & Reel

8-lead SOIC

## Carrier Tape Dimensions for 8SOICN

<table>
<thead>
<tr>
<th>Code</th>
<th>Metric Min</th>
<th>Metric Max</th>
<th>Imperial Min</th>
<th>Imperial Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>7.90</td>
<td>8.10</td>
<td>0.311</td>
<td>0.318</td>
</tr>
<tr>
<td>B</td>
<td>3.90</td>
<td>4.10</td>
<td>0.153</td>
<td>0.161</td>
</tr>
<tr>
<td>C</td>
<td>11.70</td>
<td>12.30</td>
<td>0.46</td>
<td>0.484</td>
</tr>
<tr>
<td>D</td>
<td>5.45</td>
<td>5.55</td>
<td>0.214</td>
<td>0.218</td>
</tr>
<tr>
<td>E</td>
<td>6.30</td>
<td>6.50</td>
<td>0.248</td>
<td>0.255</td>
</tr>
<tr>
<td>F</td>
<td>5.10</td>
<td>5.30</td>
<td>0.200</td>
<td>0.208</td>
</tr>
<tr>
<td>G</td>
<td>1.50</td>
<td>n/a</td>
<td>0.059</td>
<td>n/a</td>
</tr>
<tr>
<td>H</td>
<td>1.50</td>
<td>1.60</td>
<td>0.059</td>
<td>0.062</td>
</tr>
</tbody>
</table>

## Reel Dimensions for 8SOICN

<table>
<thead>
<tr>
<th>Code</th>
<th>Metric Min</th>
<th>Metric Max</th>
<th>Imperial Min</th>
<th>Imperial Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>329.60</td>
<td>330.25</td>
<td>12.976</td>
<td>13.001</td>
</tr>
<tr>
<td>B</td>
<td>20.95</td>
<td>21.45</td>
<td>0.824</td>
<td>0.844</td>
</tr>
<tr>
<td>C</td>
<td>12.80</td>
<td>13.20</td>
<td>0.503</td>
<td>0.519</td>
</tr>
<tr>
<td>D</td>
<td>1.95</td>
<td>2.45</td>
<td>0.0767</td>
<td>0.096</td>
</tr>
<tr>
<td>E</td>
<td>98.00</td>
<td>102.00</td>
<td>3.858</td>
<td>4.015</td>
</tr>
<tr>
<td>F</td>
<td>n/a</td>
<td>18.40</td>
<td>n/a</td>
<td>0.724</td>
</tr>
<tr>
<td>G</td>
<td>14.50</td>
<td>17.10</td>
<td>0.570</td>
<td>0.673</td>
</tr>
<tr>
<td>H</td>
<td>12.40</td>
<td>14.40</td>
<td>0.488</td>
<td>0.566</td>
</tr>
</tbody>
</table>
LEADFREE PART MARKING INFORMATION

Part number
IRSxxxxx
Date code
YWW?
IR logo
Pin 1 Identifier

? MARKING CODE
P Lead Free Released
Non-Lead Free Released

Lot Code
(Prod mode - 4 digit SPN code)

Assembly site code
Per SCOP 200-002

ORDER INFORMATION

8-Lead PDIP  IRS2101PbF
8-Lead SOIC  IRS2101SPbF
8-Lead SOIC  Tape & Reel  IRS2101STRPbF

The SOIC-8 is MSL2 qualified.
This product has been designed and qualified for the industrial level.
Qualification standards can be found at www.irf.com

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245  Tel: (310) 252-7105
Data and specifications subject to change without notice.  11/27/2006