**Features**
- Floating channel designed for bootstrap operation
- Fully operational to +200 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout
- 3.3 V, 5 V, and 15 V logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- Internal set deadtime
- High-side output in phase with HIN input
- Low-side output out of phase with LIN input
- RoHS compliant

**Description**
The IRS2003 is a high voltage, high speed power MOSFET and IGBT drivers with dependent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 200 V.

**Typical Connection**

![Typical Connection Diagram](Refer to Lead Assignments for correct configuration). This diagram shows electrical connections only. Please refer to our Application Notes and Design Tips for proper circuit board layout.

**Product Summary**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOFFSET</td>
<td>200 V max.</td>
</tr>
<tr>
<td>IO+/-</td>
<td>130 mA/270 mA</td>
</tr>
<tr>
<td>VOUT</td>
<td>10 V - 20 V</td>
</tr>
<tr>
<td>t\text{on/off (typ.)}</td>
<td>680 ns/150 ns</td>
</tr>
<tr>
<td>Deadtime (typ.)</td>
<td>520 ns</td>
</tr>
</tbody>
</table>

**Packages**

- 8-Lead PDIP: IRS2003
- 8-Lead SOIC: IRS2003S

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IRS2003(S)PbF

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VB</td>
<td>High-side floating absolute voltage</td>
<td>-0.3</td>
<td>225</td>
<td>V</td>
</tr>
<tr>
<td>VS</td>
<td>High-side floating supply offset voltage</td>
<td>VB - 25</td>
<td>VB + 0.3</td>
<td></td>
</tr>
<tr>
<td>VHO</td>
<td>High-side floating output voltage</td>
<td>VS - 0.3</td>
<td>VB + 0.3</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>Low-side and logic fixed supply voltage</td>
<td>-0.3</td>
<td>25</td>
<td></td>
</tr>
<tr>
<td>VLO</td>
<td>Low-side output voltage</td>
<td>-0.3</td>
<td>VCC + 0.3</td>
<td></td>
</tr>
<tr>
<td>VN</td>
<td>Logic input voltage (HIN &amp; LIN)</td>
<td>-0.3</td>
<td>VCC + 0.3</td>
<td></td>
</tr>
<tr>
<td>dVs/dt</td>
<td>Allowable offset supply voltage transient</td>
<td>—</td>
<td>50</td>
<td>V/ns</td>
</tr>
<tr>
<td>PD</td>
<td>Package power dissipation @ TA ≤ +25 °C</td>
<td>—</td>
<td>1.0</td>
<td>W</td>
</tr>
<tr>
<td>RthJA</td>
<td>Thermal resistance, junction to ambient</td>
<td>—</td>
<td>125</td>
<td>°C/W</td>
</tr>
<tr>
<td>TJ</td>
<td>Junction temperature</td>
<td>—</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>TS</td>
<td>Storage temperature</td>
<td>-55</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>TL</td>
<td>Lead temperature (soldering, 10 seconds)</td>
<td>—</td>
<td>300</td>
<td>°C</td>
</tr>
</tbody>
</table>

Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The VS offset rating is tested with all supplies biased at a 15 V differential.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VB</td>
<td>High-side floating supply absolute voltage</td>
<td>VS + 10</td>
<td>VS + 20</td>
<td>V</td>
</tr>
<tr>
<td>VS</td>
<td>High-side floating supply offset voltage</td>
<td>Note 1</td>
<td>200</td>
<td></td>
</tr>
<tr>
<td>VHO</td>
<td>High-side floating output voltage</td>
<td>VS</td>
<td>VB</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>Low-side and logic fixed supply voltage</td>
<td>10</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>VLO</td>
<td>Low-side output voltage</td>
<td>0</td>
<td>VCC</td>
<td></td>
</tr>
<tr>
<td>VN</td>
<td>Logic input voltage (HIN &amp; LIN)</td>
<td>0</td>
<td>VCC</td>
<td></td>
</tr>
<tr>
<td>TA</td>
<td>Ambient temperature</td>
<td>-40</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

Note 1: Logic operational for VS of -5 V to +200 V. Logic state held for VS of -5 V to -VBS. (Please refer to the Design Tip DT97-3 for more details).

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Dynamic Electrical Characteristics
$V_{BIAS} (V_{CC}, V_{BS}) = 15 \text{ V}, \ C_L = 1000 \text{ pF} \text{ and } T_A = 25 \text{ °C unless otherwise specified.}$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{on}$</td>
<td>Turn-on propagation delay</td>
<td>—</td>
<td>680</td>
<td>820</td>
<td>ns</td>
<td>$V_S = 0 \text{ V}$</td>
</tr>
<tr>
<td>$t_{off}$</td>
<td>Turn-off propagation delay</td>
<td>—</td>
<td>150</td>
<td>220</td>
<td>ns</td>
<td>$V_S = 200 \text{ V}$</td>
</tr>
<tr>
<td>$t_r$</td>
<td>Turn-on rise time</td>
<td>—</td>
<td>70</td>
<td>170</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_f$</td>
<td>Turn-off fall time</td>
<td>—</td>
<td>35</td>
<td>90</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$D_T$</td>
<td>Deadtime, LS turn-off to HS turn-on &amp; HS turn-on to LS turn-off</td>
<td>400</td>
<td>520</td>
<td>650</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>$M_T$</td>
<td>Delay matching, HS &amp; LS turn-on/off</td>
<td>—</td>
<td>—</td>
<td>60</td>
<td>—</td>
<td></td>
</tr>
</tbody>
</table>

Static Electrical Characteristics
$V_{BIAS} (V_{CC}, V_{BS}) = 15 \text{ V}$ and $T_A = 25 \text{ °C}$ unless otherwise specified. The $V_{IN}$, $V_{TH}$, and $I_{IN}$ parameters are referenced to COM. The $V_O$ and $I_O$ parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{H}$</td>
<td>Logic “1” (HIN) &amp; Logic “0” (LIN) input voltage</td>
<td>2.5</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>$V_{CC} = 10 \text{ V to } 20 \text{ V}$</td>
</tr>
<tr>
<td>$V_{L}$</td>
<td>Logic “0” (HIN) &amp; Logic “1” (LIN) input voltage</td>
<td>—</td>
<td>—</td>
<td>0.8</td>
<td>V</td>
<td>$I_O = 2 \text{ mA}$</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>High level output voltage, $V_{BIAS} - V_O$</td>
<td>—</td>
<td>0.05</td>
<td>0.2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low level output voltage, $V_O$</td>
<td>—</td>
<td>0.02</td>
<td>0.1</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{LK}$</td>
<td>Offset supply leakage current</td>
<td>—</td>
<td>—</td>
<td>50</td>
<td>μA</td>
<td>$V_B = V_S = 200 \text{ V}$</td>
</tr>
<tr>
<td>$I_{QBS}$</td>
<td>Quiescent $V_{BS}$ supply current</td>
<td>—</td>
<td>30</td>
<td>55</td>
<td>μA</td>
<td>$V_{IN} = 0 \text{ V or } 5 \text{ V}$</td>
</tr>
<tr>
<td>$I_{QCC}$</td>
<td>Quiescent $V_{CC}$ supply current</td>
<td>—</td>
<td>150</td>
<td>270</td>
<td>μA</td>
<td>$HIN = 5 \text{ V}, \ LIN = 0 \text{ V}$</td>
</tr>
<tr>
<td>$I_{IN+}$</td>
<td>Logic “1” input bias current</td>
<td>—</td>
<td>3</td>
<td>10</td>
<td>μA</td>
<td>$HIN = 0 \text{ V}, \ LIN = 5 \text{ V}$</td>
</tr>
<tr>
<td>$I_{IN-}$</td>
<td>Logic “0” input bias current</td>
<td>—</td>
<td>—</td>
<td>5</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>$V_{CCUV+}$</td>
<td>$V_{CC}$ supply undervoltage positive going threshold</td>
<td>8</td>
<td>8.9</td>
<td>9.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{CCUV-}$</td>
<td>$V_{CC}$ supply undervoltage negative going threshold</td>
<td>7.4</td>
<td>8.2</td>
<td>9</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{O+}$</td>
<td>Output high short circuit pulsed current</td>
<td>130</td>
<td>290</td>
<td>—</td>
<td>mA</td>
<td>$VO = 0 \text{ V}, \ VIN = V_{IH}$ $PW \leq 10 \mu s$</td>
</tr>
<tr>
<td>$I_{O-}$</td>
<td>Output low short circuit pulsed current</td>
<td>270</td>
<td>600</td>
<td>—</td>
<td>mA</td>
<td>$VO = 15 \text{ V}, \ VIN = V_{IL}$ $PW \leq 10 \mu s$</td>
</tr>
</tbody>
</table>
Functional Block Diagram

Lead Definitions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>HIN</td>
<td>Logic input for high-side gate driver output (HO), in phase</td>
</tr>
<tr>
<td>LIN</td>
<td>Logic input for low-side gate driver output (LO), out of phase</td>
</tr>
<tr>
<td>VB</td>
<td>High-side floating supply</td>
</tr>
<tr>
<td>HO</td>
<td>High-side gate drive output</td>
</tr>
<tr>
<td>VS</td>
<td>High-side floating supply return</td>
</tr>
<tr>
<td>VCC</td>
<td>Low-side and logic fixed supply</td>
</tr>
<tr>
<td>LO</td>
<td>Low-side gate drive output</td>
</tr>
<tr>
<td>COM</td>
<td>Low-side return</td>
</tr>
</tbody>
</table>

Lead Assignments

<table>
<thead>
<tr>
<th>VCC</th>
<th>VB</th>
<th>8</th>
<th>1</th>
<th>HIN</th>
<th>HO</th>
<th>7</th>
<th>2</th>
<th>LIN</th>
<th>VCC</th>
<th>6</th>
<th>3</th>
<th>LIN</th>
<th>VS</th>
<th>5</th>
<th>4</th>
<th>COM</th>
<th>LO</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>VB</td>
<td>8</td>
<td>1</td>
<td>HIN</td>
<td>HO</td>
<td>7</td>
<td>2</td>
<td>LIN</td>
<td>VS</td>
<td>6</td>
<td>3</td>
<td>COM</td>
<td>LO</td>
<td>5</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

8 Lead PDIP  8 Lead SOIC

IRS2003PbF  IRS2003SPbF
Figure 1. Input/Output Timing Diagram

Figure 2. Switching Time Waveform Definitions

Figure 3. Deadtime Waveform Definitions
Figure 4A. Turn-On Time vs. Temperature

Figure 4B. Turn-On Time vs. Supply Voltage

Figure 4C. Turn-On Time vs. Input Voltage

Figure 5A. Turn-Off Time vs. Temperature

Figure 5B. Turn-Off Time vs. Supply Voltage

Figure 5C. Turn-Off Time vs. Input Voltage
Figure 6A. Turn-On Rise Time vs. Temperature

Figure 6B. Turn-On Rise Time vs. Voltage

Figure 7A. Turn-Off Fall Time vs. Temperature

Figure 7B. Turn-Off Fall Time vs. Voltage

Figure 8A. Deadtime vs. Temperature

Figure 8B. Deadtime vs. Voltage
Figure 12A. Low Level Output Voltage vs. Temperature

Figure 12B. Low Level Output Voltage vs. Supply Voltage

Figure 13A. Offset Supply Current vs. Temperature

Figure 13B. Offset Supply Current vs. Voltage

Figure 14A. VBS Supply Current vs. Temperature

Figure 14B. VBS Supply Current vs. Voltage
NOTES:
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS SHALL NOT EXCEED 0.25 [.010].
6. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
### Tape & Reel 8-lead SOIC

#### LOADED TAPE FEED DIRECTION

![Diagram showing the loaded tape feed direction for an 8-lead SOIC package.]

**CARRIER TAPE DIMENSION FOR 8SOICN**

<table>
<thead>
<tr>
<th>Code</th>
<th>Metric</th>
<th>Imperial</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td>A</td>
<td>7.90</td>
<td>8.10</td>
</tr>
<tr>
<td>B</td>
<td>3.90</td>
<td>4.10</td>
</tr>
<tr>
<td>C</td>
<td>11.70</td>
<td>12.30</td>
</tr>
<tr>
<td>D</td>
<td>5.45</td>
<td>5.55</td>
</tr>
<tr>
<td>E</td>
<td>6.30</td>
<td>6.50</td>
</tr>
<tr>
<td>F</td>
<td>5.10</td>
<td>5.30</td>
</tr>
<tr>
<td>G</td>
<td>1.50</td>
<td>n/a</td>
</tr>
<tr>
<td>H</td>
<td>1.50</td>
<td>1.60</td>
</tr>
</tbody>
</table>

**REEL DIMENSIONS FOR 8SOICN**

<table>
<thead>
<tr>
<th>Code</th>
<th>Metric</th>
<th>Imperial</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td>A</td>
<td>329.60</td>
<td>330.25</td>
</tr>
<tr>
<td>B</td>
<td>20.95</td>
<td>21.45</td>
</tr>
<tr>
<td>C</td>
<td>12.80</td>
<td>13.20</td>
</tr>
<tr>
<td>D</td>
<td>1.95</td>
<td>2.45</td>
</tr>
<tr>
<td>E</td>
<td>98.00</td>
<td>102.00</td>
</tr>
<tr>
<td>F</td>
<td>n/a</td>
<td>18.40</td>
</tr>
<tr>
<td>G</td>
<td>14.50</td>
<td>17.10</td>
</tr>
<tr>
<td>H</td>
<td>12.40</td>
<td>14.40</td>
</tr>
</tbody>
</table>

**Note:** CONTROLLING DIMENSION IN MM

---

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LEADFREE PART MARKING INFORMATION

ORDER INFORMATION

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8-Lead SOIC IRS2003SPbF
8-Lead SOIC Tape & Reel IRS2003STRPbF