

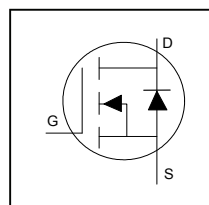
HEXFET® Power MOSFET

Application

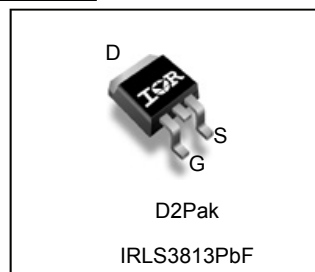
- Brushed motor drive applications
- BLDC motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC inverters

Benefits

- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free, RoHS Compliant



V_{DSS}	30V
R_{DS(on)} typ.	1.60mΩ
max	1.95mΩ
I_D (Silicon Limited)	247A①
I_D (Package Limited)	160A



G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRLS3813PbF	D ² -Pak	Tube	50	IRLS3813PbF
		Tape and Reel Left	800	IRLS3813TRLPbF

Absolute Maximum Rating

Symbol	Parameter	Max.	Units
V _{DS}	Drain-to-Source Voltage	30	V
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V (Silicon Limited)	247①	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V (Silicon Limited)	156	
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V (Package Limited)	160	
I _{DM}	Pulsed Drain Current ②	850⑩	
P _D @ T _C = 25°C	Maximum Power Dissipation	195	W
	Linear Derating Factor	1.6	W/°C
V _{GS}	Gate-to-Source Voltage	± 20	V
T _J	Operating Junction and	-55 to + 150	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)		

Avalanche Characteristics

Symbol	Parameter	Max.	Units
E _{AS} (Thermally limited)	Single Pulse Avalanche Energy ③	177	mJ
I _{AR}	Avalanche Current	148	A

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case ⑧	—	0.64	°C/W
R _{θJA}	Junction-to-Ambient (PCB Mount) ⑨	—	40	

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	23	—	mV/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1\text{mA}$ ②
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	1.60	1.95	m Ω	$V_{GS} = 10V, I_D = 148A$ ⑤
$V_{GS(th)}$	Gate Threshold Voltage	1.35	—	2.35	V	$V_{DS} = V_{GS}, I_D = 150\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	1	μA	$V_{DS} = 30V, V_{GS} = 0V$
		—	—	100		$V_{DS} = 30V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
R_G	Gate Resistance	—	0.9	—	Ω	

Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

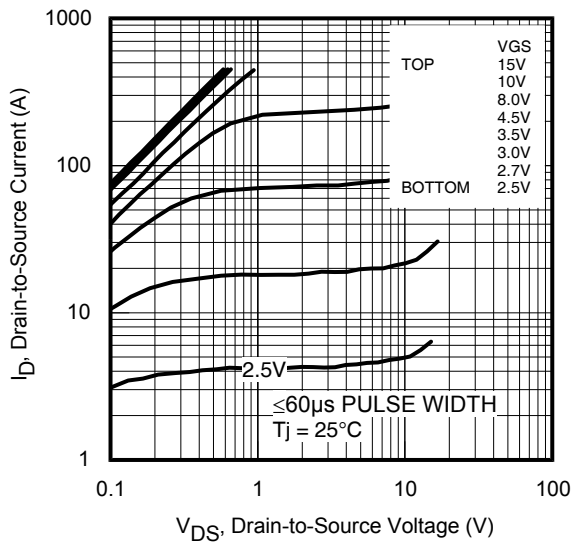
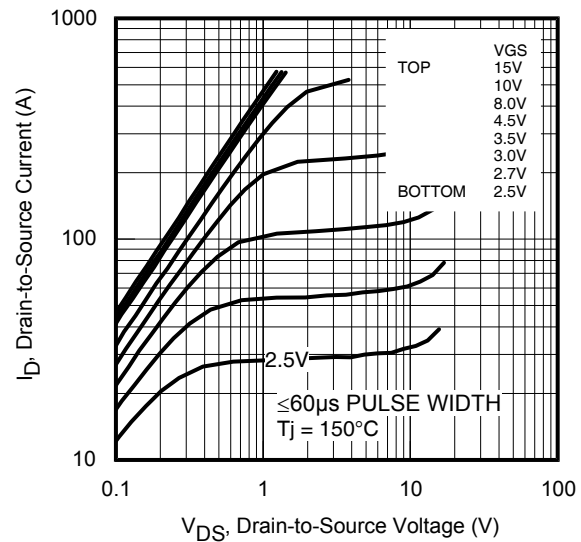
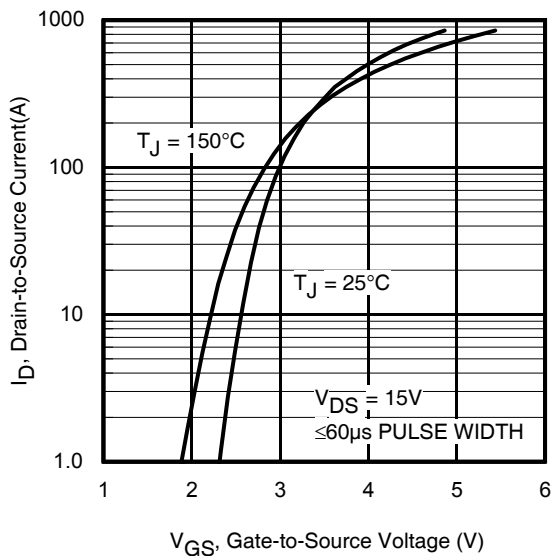
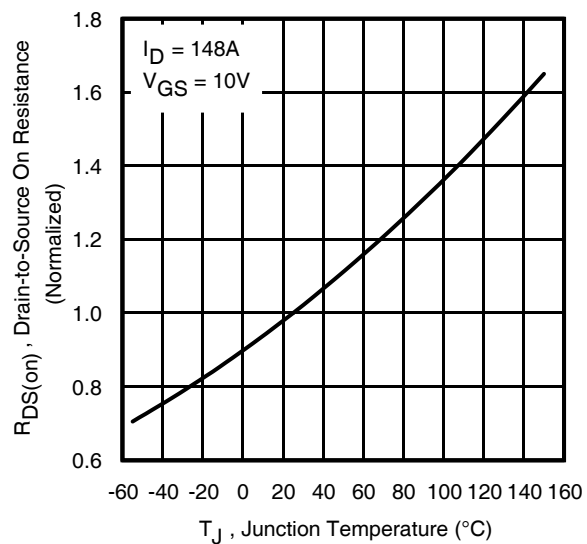
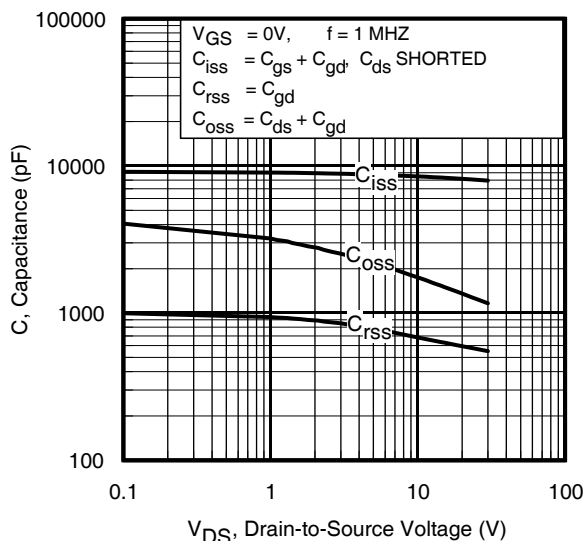
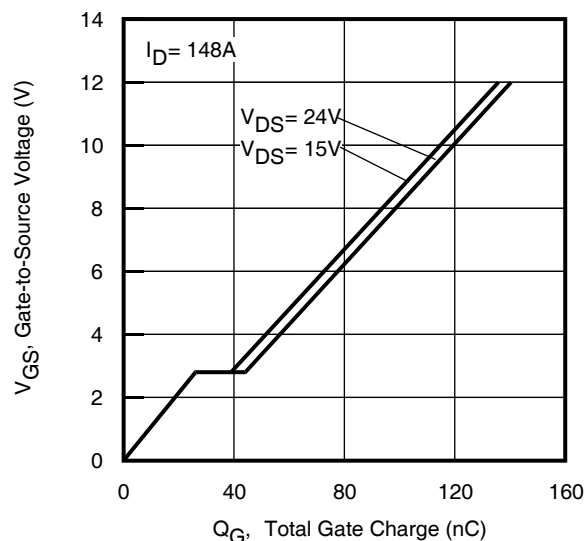
g_{fs}	Forward Transconductance	428	—	—	S	$V_{DS} = 10V, I_D = 148A$
Q_g	Total Gate Charge	—	55	83	nC	$I_D = 148A$
Q_{gs}	Gate-to-Source Charge	—	28	—		$V_{DS} = 15V$
Q_{gd}	Gate-to-Drain Charge	—	11	—		$V_{GS} = 4.5V$
$t_{d(on)}$	Turn-On Delay Time	—	32	—	ns	$V_{DD} = 20V$
t_r	Rise Time	—	202	—		$I_D = 148A$
$t_{d(off)}$	Turn-Off Delay Time	—	33	—		$R_G = 4.5\Omega$
t_f	Fall Time	—	102	—		$V_{GS} = 4.5V$
C_{iss}	Input Capacitance	—	8020	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	1250	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	570	—		$f = 1.0\text{MHz}$
$C_{oss \text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)	—	1560	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 24V$ ⑦
$C_{oss \text{ eff. (TR)}}$	Output Capacitance (Time Related)	—	1750	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 24V$ ⑥

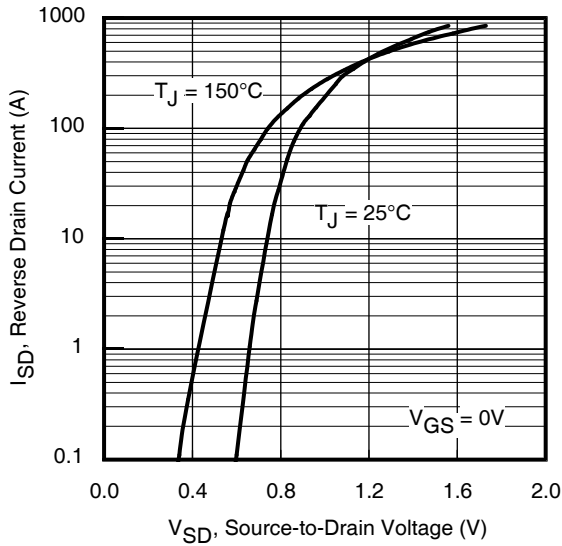
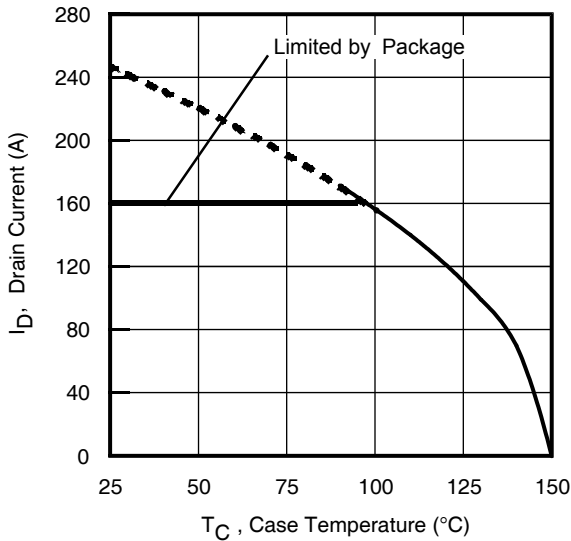
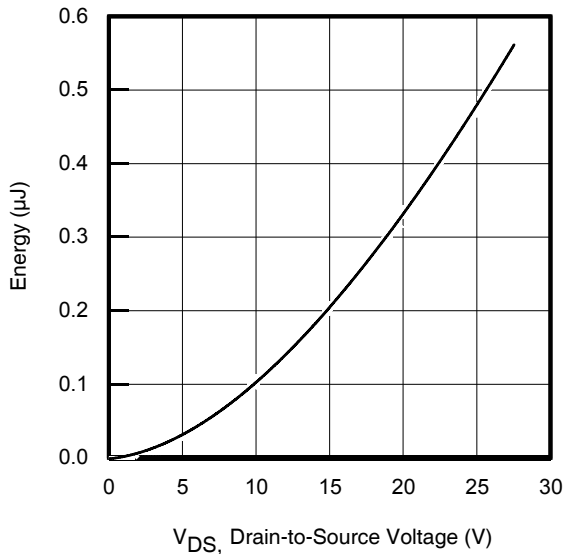
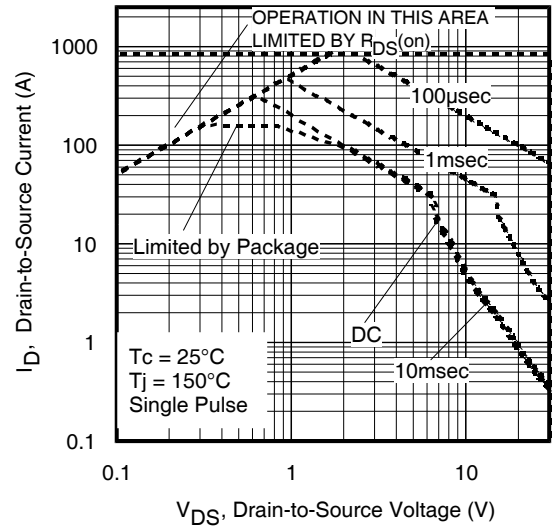
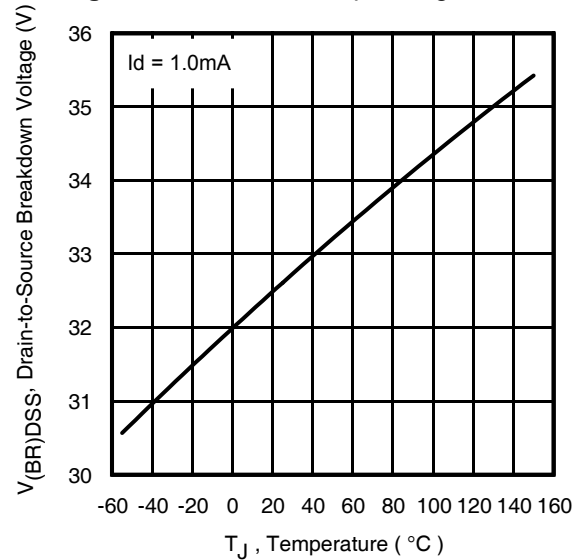
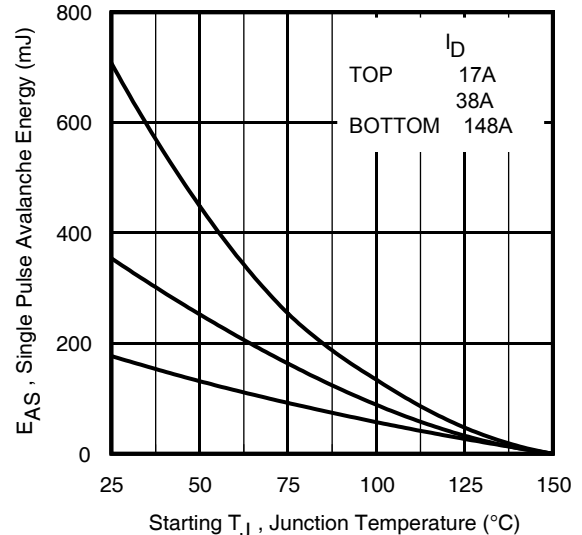
Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	247 ①	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ②	—	—	850 ③		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 148A, V_{GS} = 0V$
dv/dt	Peak Diode Recovery dv/dt ④	—	2.2	—	V/ns	$T_J = 150^\circ\text{C}, I_S = 148A, V_{DS} = 30V$
t_{rr}	Reverse Recovery Time	—	32	—	ns	$T_J = 25^\circ\text{C}$ $V_{DD} = 26V$
		—	33	—		$T_J = 125^\circ\text{C}$ $I_F = 148A$,
Q_{rr}	Reverse Recovery Charge	—	24	—	nC	$T_J = 25^\circ\text{C}$ $di/dt = 100A/\mu s$ ⑤
		—	26	—		$T_J = 125^\circ\text{C}$
I_{RRM}	Reverse Recovery Current	—	1.2	—	A	$T_J = 25^\circ\text{C}$

Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 160A by source bonding technology. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 16\mu H$, $R_G = 50\Omega$, $I_{AS} = 148A$, $V_{GS} = 10V$.
- ④ $I_{SD} \leq 148A$, $di/dt \leq 865A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$.
- ⑤ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ⑥ $C_{oss \text{ eff. (TR)}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑦ $C_{oss \text{ eff. (ER)}}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑧ R_θ is measured at T_J approximately 90°C .
- ⑨ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994: <http://www.irf.com/technical-info/appnotes/an-994.pdf>
- ⑩ Pulse drain current is limited at 640A by source bonding technology.


Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance vs. Temperature

Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage


Fig 7. Typical Source-Drain Diode Forward Voltage

Fig 9. Maximum Drain Current vs. Case Temperature

Fig 11. Typical C_{oss} Stored Energy

Fig 8. Maximum Safe Operating Area

Fig 10. Drain-to-Source Breakdown Voltage

Fig 12. Maximum Avalanche Energy Vs. Drain Current

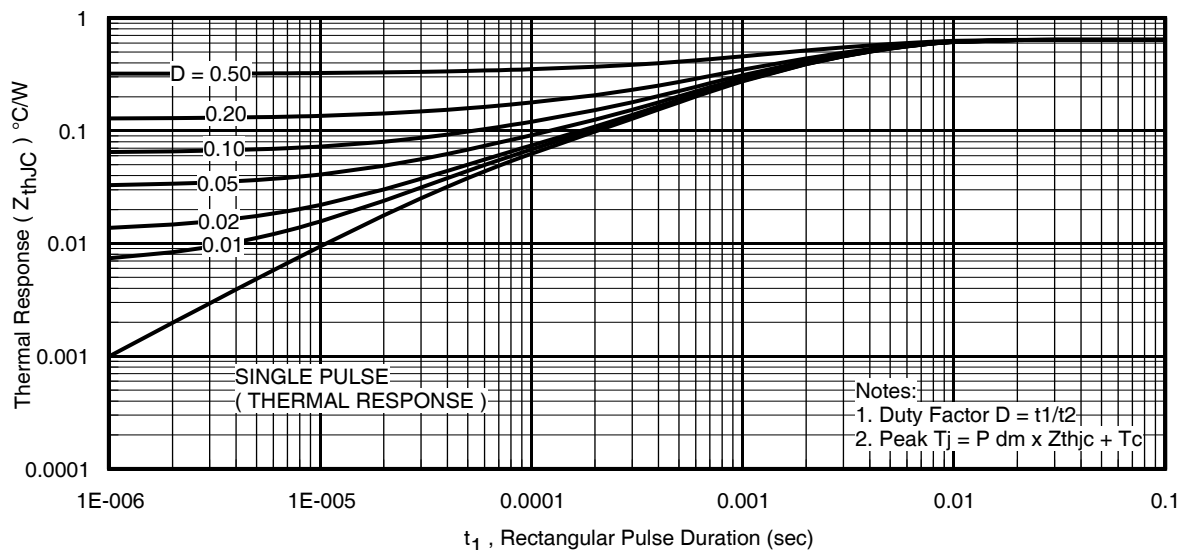


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

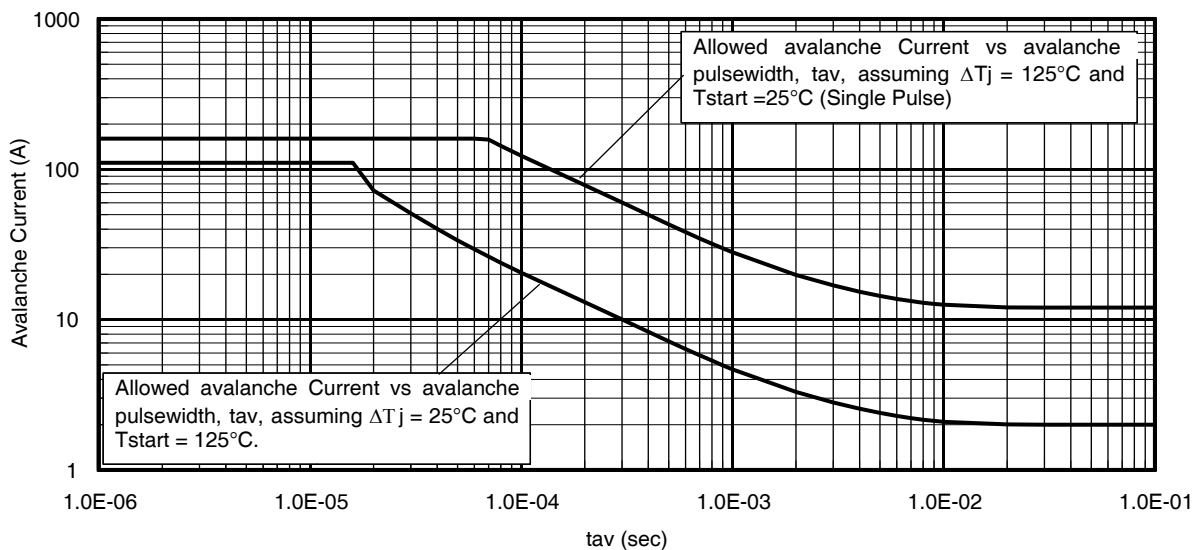
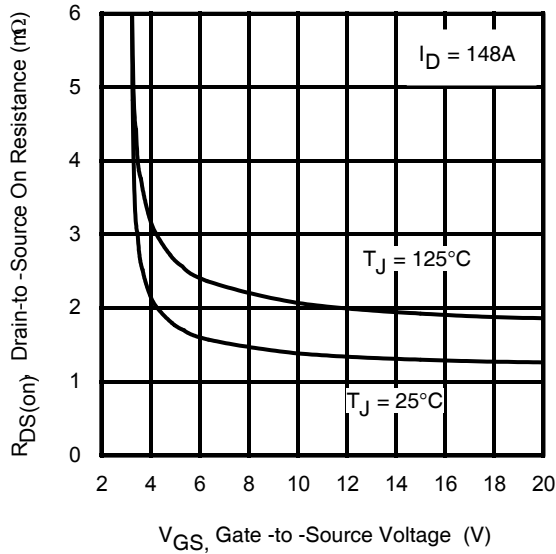
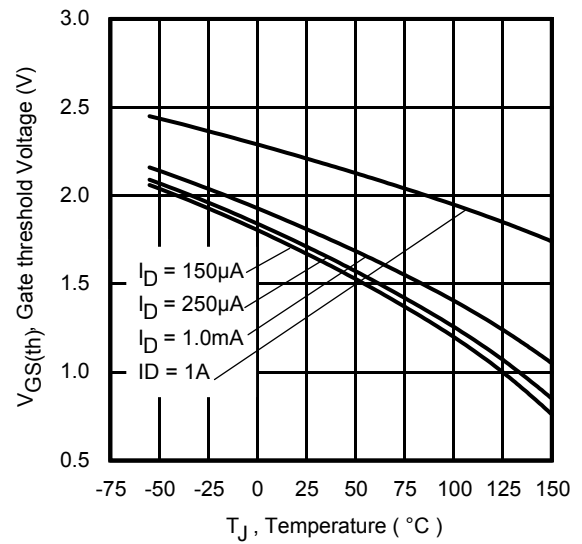
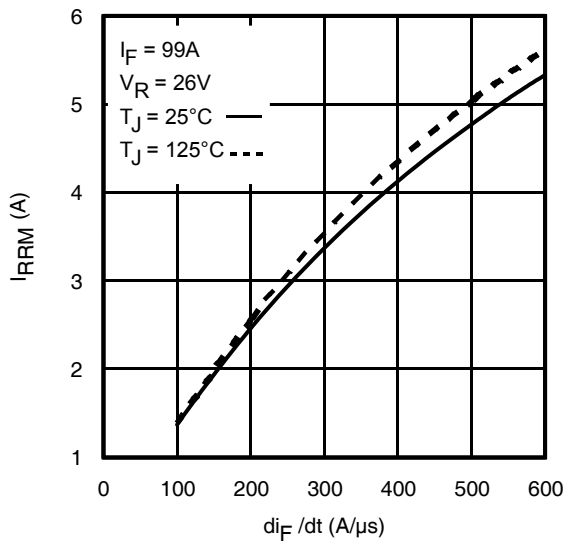
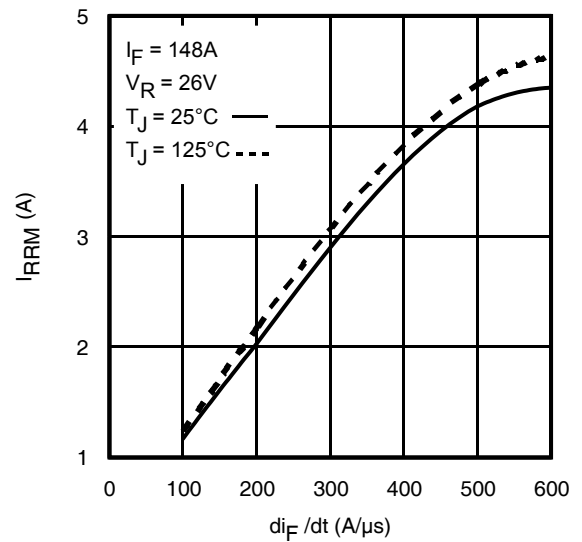
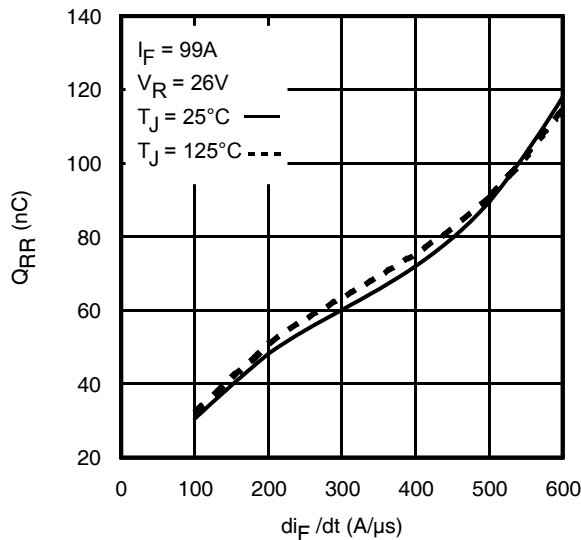
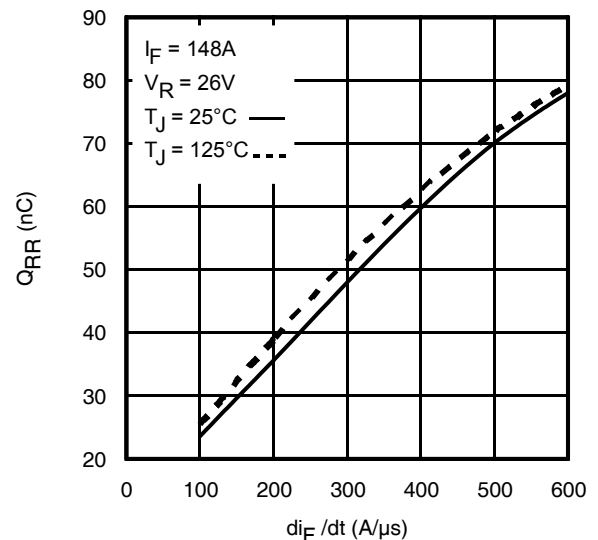


Fig 14. Single Avalanche Current vs. pulse Width


Fig 15. Typical On-Resistance vs. Gate Voltage

Fig 16. Threshold Voltage vs. Temperature

Fig 17. Typical Recovery Current vs. di_F/dt

Fig 18. Typical Recovery Current vs. di_F/dt

Fig 19. Typical Stored Charge vs. di_F/dt

Fig 20. Typical Stored Charge vs. di_F/dt

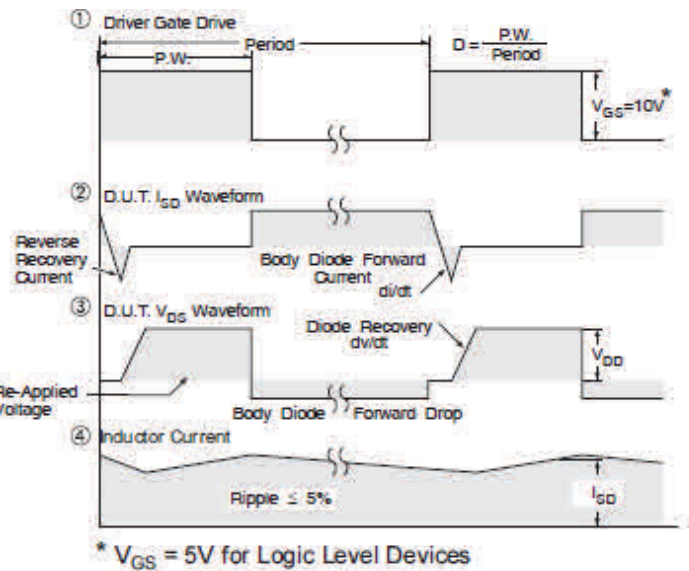
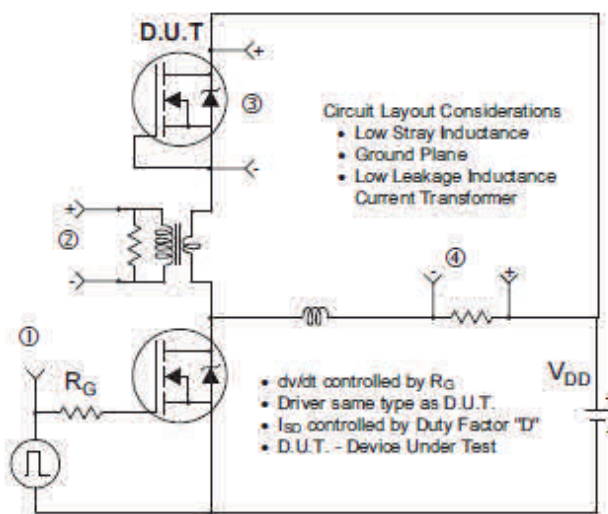


Fig 21. Peak Diode Recovery dV/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

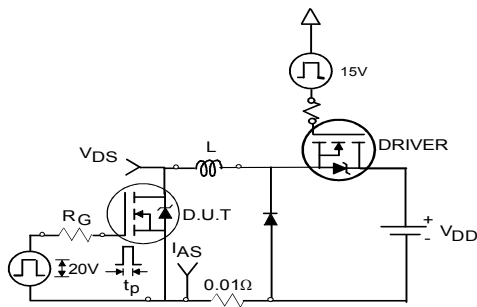


Fig 22a. Unclamped Inductive Test Circuit

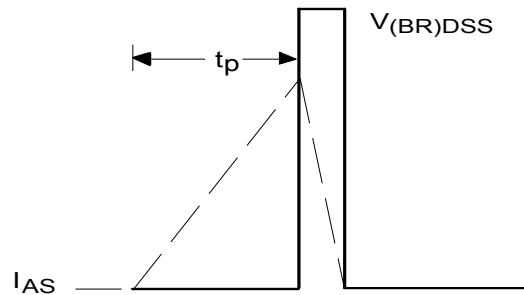


Fig 22b. Unclamped Inductive Waveforms

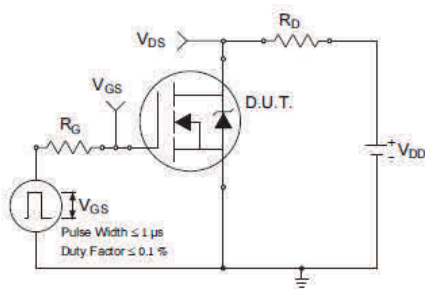


Fig 23a. Switching Time Test Circuit

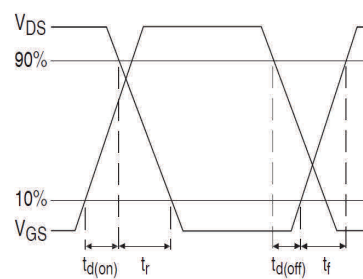


Fig 23b. Switching Time Waveforms

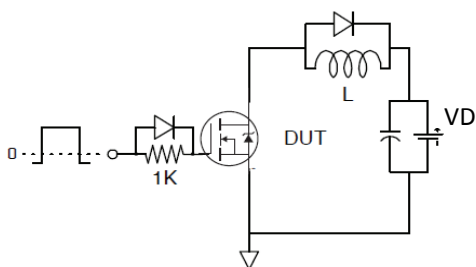


Fig 24a. Gate Charge Test Circuit

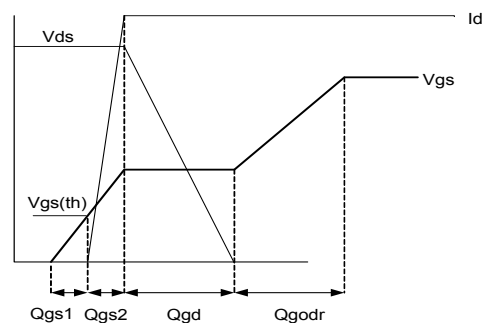
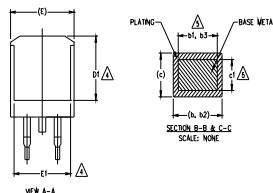
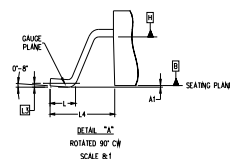
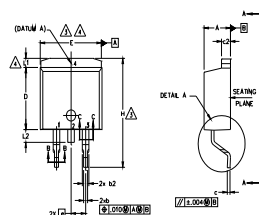


Fig 24b. Gate Charge Waveform

D²Pak (TO-263AB) Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.78	.045	.070	5
b3	1.14	1.73	.045	.068	
c	0.38	0.74	.015	.029	5
c1	0.38	0.58	.015	.023	
c2	1.14	1.65	.045	.065	3
D	8.38	9.65	.330	.380	
D1	6.86	—	.270	—	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	—	.245	—	4
e	2.54 BSC		.100 BSC		4
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	—	1.65	—	.066	
L2	1.27	1.78	—	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	

LEAD ASSIGNMENTS

HEXFET

1. — GATE
- 2, 4. — DRAIN
3. — SOURCE

IGBTs, CoPACK

1. — GATE
- 2, 4. — COLLECTOR
3. — EMITTER

DIODES

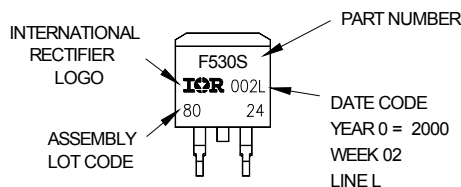
1. — ANODE *
- 2, 4. — CATHODE
3. — ANODE

* PART DEPENDENT.

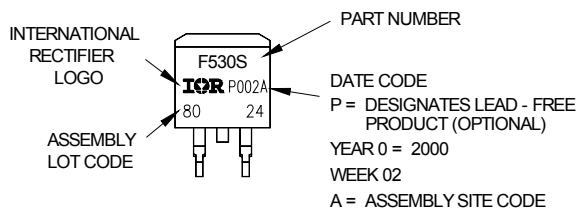
D²Pak (TO-263AB) Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

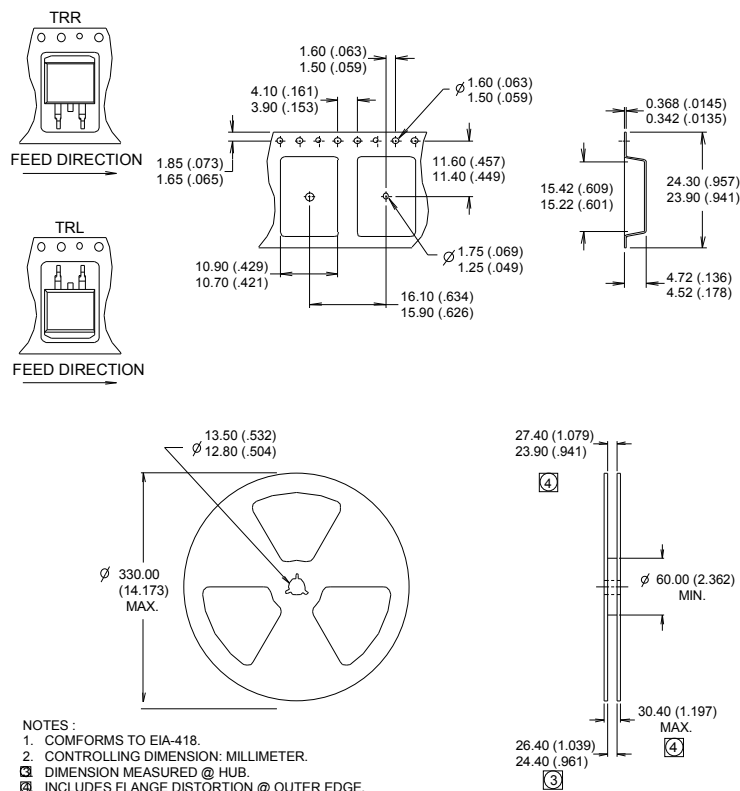
Note: "P" in assembly line position
indicates "Lead - Free"



OR



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

D²Pak (TO-263AB) Tape & Reel Information (Dimensions are shown in millimeters (inches))


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification Information[†]

Qualification Level	Industrial	
RoHS Compliant	D ² Pak	MSL1
	Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability/>

†† Applicable version of JEDEC standard at the time of product release.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 101 N. Sepulveda Blvd., El Segundo, California 90245, USA

To contact International Rectifier, please visit <http://www.irf.com/whoto-call/>

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