### Applications
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

### Benefits
- Improved Gate, Avalanche and Dynamic \( \frac{dV}{dt} \) Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode \( \frac{dV}{dt} \) and \( \frac{di}{dt} \) Capability
- Lead-Free

### Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_D )</td>
<td>Continuous Drain Current, ( V_{GS} ) @ 10V (Silicon Limited)</td>
<td>270A</td>
<td>A</td>
</tr>
<tr>
<td>( I_D )</td>
<td>Continuous Drain Current, ( V_{GS} ) @ 10V (Silicon Limited)</td>
<td>191A</td>
<td>A</td>
</tr>
<tr>
<td>( I_D )</td>
<td>Continuous Drain Current, ( V_{GS} ) @ 10V (Wire Bond Limited)</td>
<td>195A</td>
<td>A</td>
</tr>
<tr>
<td>( I_{DM} )</td>
<td>Pulsed Drain Current</td>
<td>1080</td>
<td>A</td>
</tr>
<tr>
<td>( P_D ) @ ( T_C ) = 25°C</td>
<td>Maximum Power Dissipation</td>
<td>375</td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>Linear Derating Factor</td>
<td>2.5</td>
<td>W/°C</td>
</tr>
<tr>
<td>( V_{GS} )</td>
<td>Gate-to-Source Voltage</td>
<td>±20</td>
<td>V</td>
</tr>
<tr>
<td>( dv/dt )</td>
<td>Peak Diode Recovery</td>
<td>10</td>
<td>V/ns</td>
</tr>
<tr>
<td>( T_J )</td>
<td>Operating Junction and Storage Temperature Range</td>
<td>-55 to +175</td>
<td>°C</td>
</tr>
<tr>
<td>( T_{STG} )</td>
<td>Soldering Temperature, for 10 seconds (1.6mm from case)</td>
<td>300</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>Mounting torque, 6-32 or M3 screw</td>
<td>10lb-in (1.1N-m)</td>
<td></td>
</tr>
</tbody>
</table>

### Avalanche Characteristics
- \( E_{AS} \) (Thermally limited) | Single Pulse Avalanche Energy | 320 | mJ |
- \( I_{AR} \) | Avalanche Current | See Fig. 14, 15, 22a, 22b, | A |
- \( E_{AR} \) | Repetitive Avalanche Energy | | mJ |

### Thermal Resistance

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{JC} )</td>
<td>Junction-to-Case</td>
<td>——</td>
<td>0.4</td>
<td>°C/W</td>
</tr>
<tr>
<td>( R_{JA} )</td>
<td>Junction-to-Ambient</td>
<td>——</td>
<td>40</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

www.irf.com
### Static @ \( T_J = 25\, ^\circ\text{C} \) (unless otherwise specified)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{BRDSS} )</td>
<td>Drain-to-Source Breakdown Voltage</td>
<td>60</td>
<td>——</td>
<td>——</td>
<td>V</td>
<td>( V_{GS} = 0, V, , I_D = 250, \mu A )</td>
</tr>
<tr>
<td>( \Delta V_{BRDSS}/\Delta T_J )</td>
<td>Breakdown Voltage Temp. Coefficient</td>
<td>——</td>
<td>0.07</td>
<td>——</td>
<td>V/°C</td>
<td>Reference to 25°C, ( I_D = 5, mA )©</td>
</tr>
<tr>
<td>( R_{D(on)} )</td>
<td>Static Drain-to-Source On-Resistance</td>
<td>——</td>
<td>2.0</td>
<td>2.5</td>
<td>mΩ</td>
<td>( V_{GS} = 10, V, , I_D = 170, A )©</td>
</tr>
<tr>
<td>( V_{GS(0)} )</td>
<td>Gate Threshold Voltage</td>
<td>2.0</td>
<td>——</td>
<td>——</td>
<td>V</td>
<td>( V_{DS} = V_{GS}, , I_D = 250, \mu A )</td>
</tr>
<tr>
<td>( I_{DSS} )</td>
<td>Drain-to-Source Leakage Current</td>
<td>——</td>
<td>20</td>
<td>——</td>
<td>μA</td>
<td>( V_{DS} = 60, V, , V_{GS} = 0, V )</td>
</tr>
<tr>
<td></td>
<td> </td>
<td>——</td>
<td>250</td>
<td></td>
<td></td>
<td>( V_{DS} = 60, V, , V_{GS} = 0, V, , T_J = 125, ^\circ\text{C} )</td>
</tr>
<tr>
<td>( I_{GSS} )</td>
<td>Gate-to-Source Forward Leakage</td>
<td>——</td>
<td>100</td>
<td>——</td>
<td>nA</td>
<td>( V_{GS} = 20, V )</td>
</tr>
<tr>
<td></td>
<td> </td>
<td>——</td>
<td>-100</td>
<td></td>
<td></td>
<td>( V_{GS} = -20, V )</td>
</tr>
<tr>
<td>( R_G )</td>
<td>Internal Gate Resistance</td>
<td>——</td>
<td>2.0</td>
<td>——</td>
<td>Ω</td>
<td></td>
</tr>
</tbody>
</table>

### Dynamic @ \( T_J = 25\, ^\circ\text{C} \) (unless otherwise specified)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>( g_f)</td>
<td>Forward Transconductance</td>
<td>280</td>
<td>——</td>
<td>——</td>
<td>S</td>
<td>( V_{DS} = 25, V, , I_D = 170, A )</td>
</tr>
<tr>
<td>( Q_g )</td>
<td>Total Gate Charge</td>
<td>——</td>
<td>200</td>
<td>300</td>
<td>nC</td>
<td>( I_P = 170, A )</td>
</tr>
<tr>
<td>( Q_{gs} )</td>
<td>Gate-to-Source Charge</td>
<td>——</td>
<td>37</td>
<td>——</td>
<td>nC</td>
<td>( V_{DS} = 30, V )</td>
</tr>
<tr>
<td>( Q_{gd} )</td>
<td>Gate-to-Drain (&quot;Miller&quot;) Charge</td>
<td>——</td>
<td>60</td>
<td>——</td>
<td>nC</td>
<td>( V_{GS} = 10, V ) ©</td>
</tr>
<tr>
<td>( Q_{sync} )</td>
<td>Total Gate Charge Sync. (( Q_g - Q_{gd} ))</td>
<td>——</td>
<td>140</td>
<td>——</td>
<td>nC</td>
<td>( I_P = 170A, , V_{DS} = 0, V, , V_{GS} = 10, V )</td>
</tr>
<tr>
<td>( t_{(on)} )</td>
<td>Turn-On Delay Time</td>
<td>——</td>
<td>16</td>
<td>——</td>
<td>ns</td>
<td>( V_{DD} = 39, V )</td>
</tr>
<tr>
<td>( t_r )</td>
<td>Rise Time</td>
<td>——</td>
<td>182</td>
<td>——</td>
<td>ns</td>
<td>( I_P = 170, A )</td>
</tr>
<tr>
<td>( t_{(off)} )</td>
<td>Turn-Off Delay Time</td>
<td>——</td>
<td>118</td>
<td>——</td>
<td>ns</td>
<td>( R_G = 2.7, \Omega )</td>
</tr>
<tr>
<td>( t_f )</td>
<td>Fall Time</td>
<td>——</td>
<td>189</td>
<td>——</td>
<td>ns</td>
<td>( V_{GS} = 10, V ) ©</td>
</tr>
<tr>
<td>( C_{iss} )</td>
<td>Input Capacitance</td>
<td>——</td>
<td>8970</td>
<td>——</td>
<td>pF</td>
<td>( V_{GS} = 0, V )</td>
</tr>
<tr>
<td>( C_{oss} )</td>
<td>Output Capacitance</td>
<td>——</td>
<td>1020</td>
<td>——</td>
<td>pF</td>
<td>( V_{DS} = 50, V )</td>
</tr>
<tr>
<td>( C_{rss} )</td>
<td>Reverse Transfer Capacitance</td>
<td>——</td>
<td>534</td>
<td>——</td>
<td>pF</td>
<td>( f = 1.0, \text{MHz, See Fig. 5} )</td>
</tr>
<tr>
<td>( C_{oss, \text{eff.}}, (ER) )</td>
<td>Effective Output Capacitance (Energy Related)</td>
<td>——</td>
<td>1480</td>
<td>——</td>
<td>pF</td>
<td>( V_{GS} = 0, V, , V_{DS} = 0, V ) to 48V ©, See Fig. 11</td>
</tr>
<tr>
<td>( C_{oss, \text{eff.}}, (TR) )</td>
<td>Effective Output Capacitance (Time Related)©</td>
<td>——</td>
<td>1920</td>
<td>——</td>
<td>pF</td>
<td>( V_{GS} = 0, V, , V_{DS} = 0, V ) to 48V ©</td>
</tr>
</tbody>
</table>

### Diode Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_S )</td>
<td>Continuous Source Current (Body Diode)</td>
<td>——</td>
<td>——</td>
<td>270©</td>
<td>A</td>
<td>MOSFET symbol showing the integral reverse p-n junction diode.</td>
</tr>
<tr>
<td>( I_{SM} )</td>
<td>Pulsed Source Current (Body Diode) ©</td>
<td>——</td>
<td>——</td>
<td>1080</td>
<td>A</td>
<td>©</td>
</tr>
<tr>
<td>( V_D )</td>
<td>Diode Forward Voltage</td>
<td>——</td>
<td>——</td>
<td>1.3</td>
<td>V</td>
<td>( T_J = 25, ^\circ\text{C}, , I_S = 170, A, , V_{GS} = 0, V ) ©</td>
</tr>
<tr>
<td>( I_r )</td>
<td>Reverse Recovery Time</td>
<td>——</td>
<td>44</td>
<td>——</td>
<td>ns</td>
<td>( T_J = 25, ^\circ\text{C}, , V_R = 51, V, , I_F = 170, A )</td>
</tr>
<tr>
<td>( Q_r )</td>
<td>Reverse Recovery Charge</td>
<td>——</td>
<td>63</td>
<td>——</td>
<td>nC</td>
<td>( T_J = 25, ^\circ\text{C}, , \text{di/dt} = 100, \mu\text{A/µs} ) ©</td>
</tr>
<tr>
<td>( I_{RRM} )</td>
<td>Reverse Recovery Current</td>
<td>——</td>
<td>77</td>
<td>——</td>
<td>A</td>
<td>( T_J = 125, ^\circ\text{C} )</td>
</tr>
<tr>
<td>( I_{on} )</td>
<td>Forward Turn-On Time</td>
<td>——</td>
<td>2.4</td>
<td>——</td>
<td>A</td>
<td>( T_J = 25, ^\circ\text{C} )</td>
</tr>
</tbody>
</table>

Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)

### Notes:
- © Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 195A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)
- © Repetitive rating; pulse width limited by max. junction temperature.
- © Limited by \( T_{J\max} \), starting \( T_J = 25\, ^\circ\text{C}, \, L = 0.022\, \text{mH} \) \( R_G = 25\, \Omega, \, I_{AS} = 170\, A, \, V_{GS} = 10\, V \). Part not recommended for use above this value.
- © \( I_{SD} \leq 170\, A, \, \text{di/dt} \leq 1360\, \mu\text{A/µs}, \, V_{DD} \leq V_{BRDSS}, \, T_J \leq 175\, ^\circ\text{C} \).
- © Pulse width \leq 400µs; duty cycle \leq 2%.©
- © \( C_{oss\, \text{eff.}}\, (ER) \) is a fixed capacitance that gives the same charging time as \( C_{oss} \) while \( V_{DS} \) is rising from 0 to 80% \( V_{oss} \).
- © \( C_{oss\, \text{eff.}}\, (TR) \) is a fixed capacitance that gives the same energy as \( C_{oss} \) while \( V_{DS} \) is rising from 0 to 80% \( V_{oss} \).
- © When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- © \( R_R \) is measured at \( T_J \) approximately 90°C
- © \( R_{UC} \) value shown is at time zero
Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance vs. Temperature

Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage
**Fig 7.** Typical Source-Drain Diode Forward Voltage

**Fig 8.** Maximum Safe Operating Area

**Fig 9.** Maximum Drain Current vs. Case Temperature

**Fig 10.** Drain-to-Source Breakdown Voltage

**Fig 11.** Typical $C_{OSS}$ Stored Energy

**Fig 12.** Maximum Avalanche Energy Vs. Drain Current
Notes on Repetitive Avalanche Curves, Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of $T_{j\text{max}}$. This is validated for every part type.

2. Safe operation in Avalanche is allowed as long as $T_j$ is not exceeded.

3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.

4. $PD_{(ave)} = \frac{1}{2} \left( \frac{1.3 \cdot BV \cdot I_{av}}{Z_{thJC(D, tav)}} \right)$

5. $BV$ = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).

6. $I_{av}$ = Allowable avalanche current.

7. $\Delta T$ = Allowable rise in junction temperature, not to exceed $T_{j\text{max}}$ (assumed as 25°C in Figure 14, 15).

8. $t_{av}$ = Average time in avalanche.

$D = \text{Duty cycle in avalanche} = \frac{tav}{f}$

$Z_{thJC(D, tav)}$ = Transient thermal resistance, see Figures 13)

$PD_{(ave)} = \frac{1}{2} \left( \frac{1.3 \cdot BV \cdot I_{av}}{Z_{thJC(D, tav)}} \right)$

$I_{av} = 2 \cdot \frac{\Delta T}{\left( 1.3 \cdot BV \cdot Z_{thJC(D, tav)} \right)}$

$E_{AS (AR)} = PD_{(ave)} \cdot t_{av}$

Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig 14. Typical Avalanche Current vs. Pulsewidth

Fig 15. Maximum Avalanche Energy vs. Temperature
Fig. 16. Threshold Voltage Vs. Temperature

Fig. 17 - Typical Recovery Current vs. di/dt

Fig. 18 - Typical Recovery Current vs. di/dt

Fig. 19 - Typical Stored Charge vs. di/dt

Fig. 20 - Typical Stored Charge vs. di/dt
Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

Fig 22a. Unclamped Inductive Test Circuit

Fig 22b. Unclamped Inductive Waveforms

Fig 23a. Switching Time Test Circuit

Fig 23b. Switching Time Waveforms

Fig 24a. Gate Charge Test Circuit

Fig 24b. Gate Charge Waveform
**D²Pak (TO-263AB) Package Outline**

Dimensions are shown in millimeters (inches)

---

**D²Pak (TO-263AB) Part Marking Information**

**EXAMPLE:**

THIS IS AN IRFS30S WITH LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE 'L'

Note: "P" in assembly line position indicates "Lead – Free"

---

**Notes:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH, MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PASTE CONTOUR OPTIONAL. DIMENSION E, L1, L2 & L3.
5. DIMENSION D1 AND D2 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCHES.
8. OUTLINE CONFORMS TO IEC/IEC/DATA/TO-263A.

---

**Notes:**

- LEAD ASSIGNMENTS
- HEXFET
  1. - GATE
  2. - DRAIN
  3. - SOURCE
- IGBT, CRYSTAL
  1. - GATE
  2. - COLLECTOR
  3. - Emitter

---

**Notes:**

- DIODES
  1. - ANODE
  2. - CATHODE
  3. - ANODE

* PART DEPENDENT.

---

Note: For the most current drawing please refer to IR website at [http://www.irf.com/package/](http://www.irf.com/package/)
TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE 'C'

Note: "F" in assembly line position indicates "Lead - Free"

OR

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/
www.irf.com
D²Pak (TO-263AB) Tape & Reel Information

Dimensions are shown in millimeters (inches)

Notes:
1. CONFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/