Applications
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

Benefits
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dl/dt Capability
- Lead-Free

Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>ID @ TC = 25°C</td>
<td>Continuous Drain Current, VGS @ 10V (Silicon Limited)</td>
<td>340</td>
<td>A</td>
</tr>
<tr>
<td>ID @ TC = 100°C</td>
<td>Continuous Drain Current, VGS @ 10V (Silicon Limited)</td>
<td>240</td>
<td>A</td>
</tr>
<tr>
<td>ID @ TC = 25°C</td>
<td>Continuous Drain Current, VGS @ 10V (Wire Bond Limited)</td>
<td>195</td>
<td>A</td>
</tr>
<tr>
<td>IDM</td>
<td>Pulsed Drain Current</td>
<td>1310</td>
<td>W</td>
</tr>
<tr>
<td>PD @ TC = 25°C</td>
<td>Maximum Power Dissipation</td>
<td>380</td>
<td>W</td>
</tr>
<tr>
<td>Linear Derating Factor</td>
<td></td>
<td>2.5</td>
<td>W/°C</td>
</tr>
<tr>
<td>VGS</td>
<td>Gate-to-Source Voltage</td>
<td>± 20</td>
<td>V</td>
</tr>
<tr>
<td>dv/dt</td>
<td>Peak Diode Recovery</td>
<td>4.4</td>
<td>V/ns</td>
</tr>
<tr>
<td>TJ</td>
<td>Operating Junction and Storage Temperature Range</td>
<td>-55 to +175</td>
<td>°C</td>
</tr>
<tr>
<td>TSTG</td>
<td>Soldering Temperature, for 10 seconds (1.6mm from case)</td>
<td>300</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>Mounting torque, 6-32 or M3 screw</td>
<td>10lbf-in (1.1N·m)</td>
<td></td>
</tr>
</tbody>
</table>

Avalanche Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Meas.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>EAS</td>
<td>Single Pulse Avalanche Energy</td>
<td>300</td>
<td>mJ</td>
</tr>
<tr>
<td>IAR</td>
<td>Avalanche Current</td>
<td>See Fig. 14, 15, 22a, 22b</td>
<td>A</td>
</tr>
<tr>
<td>EAR</td>
<td>Repetitive Avalanche Energy</td>
<td>---</td>
<td>mJ</td>
</tr>
</tbody>
</table>

Thermal Resistance

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>RJC</td>
<td>Junction-to-Case</td>
<td>---</td>
<td>0.40</td>
<td>°C/W</td>
</tr>
<tr>
<td>RJC</td>
<td>Case-to-Sink, Flat Greased Surface, TO-220</td>
<td>0.50</td>
<td>62</td>
<td></td>
</tr>
<tr>
<td>RJJA</td>
<td>Junction-to-Ambient, TO-220</td>
<td>---</td>
<td>62</td>
<td></td>
</tr>
<tr>
<td>RJJA</td>
<td>Junction-to-Ambient (PCB Mount), D²Pak</td>
<td>---</td>
<td>40</td>
<td></td>
</tr>
</tbody>
</table>
Static @ $T_J = 25^\circ$C (unless otherwise specified)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{(BR)DSS}$</td>
<td>Drain-to-Source Breakdown Voltage</td>
<td>40</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>$V_{GS} = 0V$, $I_D = 250\mu A$</td>
</tr>
<tr>
<td>$\Delta V_{(BR)DSS}/\Delta T_J$</td>
<td>Breakdown Voltage Temp. Coefficient</td>
<td>—</td>
<td>0.037</td>
<td>—</td>
<td>V/°C</td>
<td>Reference to $25^\circ$C, $I_D = 5mA \circ$</td>
</tr>
<tr>
<td>$R_{DS(on)}$</td>
<td>Static Drain-to-Source On-Resistance</td>
<td>—</td>
<td>1.4</td>
<td>1.75</td>
<td>mΩ</td>
<td>$V_{GS} = 10V$, $I_D = 195A \circ$</td>
</tr>
<tr>
<td>$V_{GS(min)}$</td>
<td>Gate Threshold Voltage</td>
<td>2.0</td>
<td>—</td>
<td>4.0</td>
<td>V</td>
<td>$V_{GS} = V_{GS}$, $I_D = 250\mu A$</td>
</tr>
<tr>
<td>$I_{DSS}$</td>
<td>Drain-to-Source Leakage Current</td>
<td>—</td>
<td>—</td>
<td>20</td>
<td>µA</td>
<td>$V_{GS} = 40V$, $V_{DS} = 0V$</td>
</tr>
<tr>
<td>$I_{GSS}$</td>
<td>Gate-to-Source Forward Leakage</td>
<td>—</td>
<td>—</td>
<td>100</td>
<td>nA</td>
<td>$V_{GS} = 20V$</td>
</tr>
<tr>
<td>$I_{RSS}$</td>
<td>Gate-to-Source Reverse Leakage</td>
<td>—</td>
<td>—</td>
<td>-100</td>
<td>—</td>
<td>$V_{GS} = -20V$</td>
</tr>
<tr>
<td>$R_G$</td>
<td>Internal Gate Resistance</td>
<td>—</td>
<td>2.2</td>
<td>—</td>
<td>Ω</td>
<td></td>
</tr>
</tbody>
</table>

Dynamic @ $T_J = 25^\circ$C (unless otherwise specified)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$g_{fs}$</td>
<td>Forward Transconductance</td>
<td>1170</td>
<td>—</td>
<td>—</td>
<td>S</td>
<td>$V_{GS} = 10V$, $I_D = 195A$</td>
</tr>
<tr>
<td>$Q_g$</td>
<td>Total Gate Charge</td>
<td>—</td>
<td>160</td>
<td>240</td>
<td>nC</td>
<td>$I_D = 187A$</td>
</tr>
<tr>
<td>$Q_{gs}$</td>
<td>Gate-to-Source Charge</td>
<td>—</td>
<td>40</td>
<td>—</td>
<td>—</td>
<td>$V_{GS} = 20V$</td>
</tr>
<tr>
<td>$Q_{gd}$</td>
<td>Gate-to-Drain (&quot;Miller&quot;) Charge</td>
<td>—</td>
<td>68</td>
<td>—</td>
<td>—</td>
<td>$V_{GS} = 10V \circ$</td>
</tr>
<tr>
<td>$Q_{sync}$</td>
<td>Total Gate Charge Sync. ($Q_g - Q_{gd}$)</td>
<td>—</td>
<td>92</td>
<td>—</td>
<td>—</td>
<td>$I_D = 187A$, $V_{DS} = 0V$, $V_{GS} = 10V$</td>
</tr>
<tr>
<td>$t_{(on)}$</td>
<td>Turn-On Delay Time</td>
<td>—</td>
<td>23</td>
<td>—</td>
<td>ns</td>
<td>$V_{DD} = 26V$</td>
</tr>
<tr>
<td>$t_r$</td>
<td>Rise Time</td>
<td>—</td>
<td>220</td>
<td>—</td>
<td>—</td>
<td>$I_D = 195A$</td>
</tr>
<tr>
<td>$t_{(off)}$</td>
<td>Turn-Off Delay Time</td>
<td>—</td>
<td>90</td>
<td>—</td>
<td>—</td>
<td>$R_S = 2.7\Omega$</td>
</tr>
<tr>
<td>$t_f$</td>
<td>Fall Time</td>
<td>—</td>
<td>130</td>
<td>—</td>
<td>—</td>
<td>$V_{GS} = 10V \circ$</td>
</tr>
<tr>
<td>$C_{iss}$</td>
<td>Input Capacitance</td>
<td>—</td>
<td>9200</td>
<td>—</td>
<td>pF</td>
<td>$V_{GS} = 0V$</td>
</tr>
<tr>
<td>$C_{oss}$</td>
<td>Output Capacitance</td>
<td>—</td>
<td>2020</td>
<td>—</td>
<td>—</td>
<td>$V_{GS} = 25V$</td>
</tr>
<tr>
<td>$C_{rss}$</td>
<td>Reverse Transfer Capacitance</td>
<td>—</td>
<td>1340</td>
<td>—</td>
<td>—</td>
<td>$f = 1.0 MHz$, See Fig. 5</td>
</tr>
<tr>
<td>$C_{oss eff. (ER)}$</td>
<td>Effective Output Capacitance (Energy Related)</td>
<td>—</td>
<td>2440</td>
<td>—</td>
<td>—</td>
<td>$V_{GS} = 0V$, $V_{DS} = 0V$ to $32V \circ$, See Fig. 11</td>
</tr>
<tr>
<td>$C_{oss eff. (TR)}$</td>
<td>Effective Output Capacitance (Time Related)</td>
<td>—</td>
<td>2690</td>
<td>—</td>
<td>—</td>
<td>$V_{GS} = 0V$, $V_{DS} = 0V$ to $32V \circ$</td>
</tr>
</tbody>
</table>

Diode Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_S$</td>
<td>Continuous Source Current (Body Diode)</td>
<td>—</td>
<td>—</td>
<td>340</td>
<td>A</td>
<td>MOSFET symbol showing the integral reverse p-n junction diode.</td>
</tr>
<tr>
<td>$I_{SM}$</td>
<td>Pulsed Source Current (Body Diode)</td>
<td>—</td>
<td>—</td>
<td>1310</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>$V_{SD}$</td>
<td>Diode Forward Voltage</td>
<td>—</td>
<td>—</td>
<td>1.3</td>
<td>V</td>
<td>$T_J = 25^\circ$C, $I_S = 195A$, $V_{GS} = 0V \circ$</td>
</tr>
<tr>
<td>$t_{tr}$</td>
<td>Reverse Recovery Time</td>
<td>—</td>
<td>27</td>
<td>—</td>
<td>ns</td>
<td>$T_J = 25^\circ$C</td>
</tr>
<tr>
<td>$Q_{tr}$</td>
<td>Reverse Recovery Charge</td>
<td>—</td>
<td>18</td>
<td>—</td>
<td>nC</td>
<td>$T_J = 25^\circ$C</td>
</tr>
<tr>
<td>$I_{RRM}$</td>
<td>Reverse Recovery Current</td>
<td>—</td>
<td>41</td>
<td>—</td>
<td>—</td>
<td>$T_J = 125^\circ$C</td>
</tr>
<tr>
<td>$I_{on}$</td>
<td>Forward Turn-On Time</td>
<td>—</td>
<td>1.2</td>
<td>—</td>
<td>A</td>
<td>$T_J = 25^\circ$C</td>
</tr>
</tbody>
</table>

Notes:

1. Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 195A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)
2. Repetitive rating; pulse width limited by max. junction temperature.
3. Limited by $T_{j,max}$; starting $T_J = 25^\circ$C, $L = 0.016mH$ $R_G = 25\Omega$, $I_{AS} = 195A$, $V_{GS} = 10V$. Part not recommended for use above this value.
4. $I_{SD} \leq 195A$, $di/dt \leq 930A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ$C.
5. Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
6. $C_{oss eff. (TR)}$ is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DS}$.
7. $C_{oss eff. (ER)}$ is a fixed capacitance that gives the same energy as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DS}$.
8. When mounted on 1” square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
9. $R_S$ is measured at $T_J$ approximately 90°C.
10. $R_{UIC}$ value shown is at time zero.
Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance vs. Temperature

Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

www.irf.com
**Fig 7.** Typical Source-Drain Diode Forward Voltage

**Fig 8.** Maximum Safe Operating Area

**Fig 9.** Maximum Drain Current vs. Case Temperature

**Fig 10.** Drain-to-Source Breakdown Voltage

**Fig 11.** Typical C_DSS Stored Energy

**Fig 12.** Maximum Avalanche Energy vs. Drain Current
Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig 14. Typical Avalanche Current vs. Pulsewidth

Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves, Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)
1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of Tjmax. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as Tjmax is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. PD (ave) = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. Iav = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed Tjmax (assumed as 25°C in Figure 14, 15).
   \( I_{av} = \text{Average time in avalanche.} \)
   \( D = \text{Duty cycle in avalanche} \)
   \( D = \frac{I_{av}}{1 - \frac{Z_{th,jc}}{D}} = \text{Transient thermal resistance, see Figures 13) \)

\[
P_D(\text{ave}) = \frac{1}{2} (1.3 \times BV) I_{av} = \frac{\Delta T}{Z_{th,jc}}
\]

\[
I_{av} = 2 \Delta T \left[ 1.3 \times BV Z_{th,jc} \right]
\]

\[
E_{AS (AR)} = P_D(\text{ave}) I_{av}
\]
Fig 16. Threshold Voltage vs. Temperature

Fig. 17 - Typical Recovery Current vs. $di/dt$

Fig. 18 - Typical Recovery Current vs. $di/dt$

Fig. 19 - Typical Stored Charge vs. $di/dt$

Fig. 20 - Typical Stored Charge vs. $di/dt$
Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

Fig 22a. Unclamped Inductive Test Circuit

Fig 22b. Unclamped Inductive Waveforms

Fig 23a. Switching Time Test Circuit

Fig 23b. Switching Time Waveforms

Fig 24a. Gate Charge Test Circuit

Fig 24b. Gate Charge Waveform
TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 2000
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead - Free"

TO-220AB packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/
TO-262 Package Outline
Dimensions are shown in millimeters (inches)

TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead – Free"

INTERNATIONAL RECTIFIER
LOGO

PART NUMBER

DATE CODE
YEAR 7 – 1997
WEEK 19
LINE C

OR

INTERNATIONAL RECTIFIER
LOGO

PART NUMBER

DATE CODE
P – DESIGNATES LEAD-FREE
PRODUCT (OPTIONAL)
YEAR 7 – 1997
WEEK 19
A – ASSEMBLY SITE CODE

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

www.irf.com
D²Pak (TO-263AB) Package Outline
Dimensions are shown in millimeters (inches)

NOTES:
1. DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. DIMENSION D6 & E6 DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREME OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PASTE CONTACT AREA ILLUSION WITHIN DIMENSION T, T1, B1 & E1.
5. DIMENSION D1 AND D4 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

D²Pak (TO-263AB) Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH LOT CODE 8024 ASSEMBLED ON WW 02, 2000 IN THE ASSEMBLY LINE “L”

Note: “P” in assembly line position indicates “Lead – Free”

INTERNATIONAL RECTIFIER

PART NUMBER

DATE CODE
YEAR 0 = 2000 WEEK 02 LINE L

ASSEMBLY LOT CODE

INTERNATIONAL RECTIFIER LOGO

P = DESIGNATES LEAD - FREE PRODUCT (OPTIONAL)
YEAR 0 = 2000 WEEK 02
A = ASSEMBLY SITE CODE

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/
D²Pak (TO-263AB) Tape & Reel Information

Dimensions are shown in millimeters (inches)

**Notes:**
1. Conforms to EIA-418.
2. Controlling Dimension: Millimeter.
3. Dimension measured @ hub.
4. Includes flange distortion @ outer edge.

**Dimensions:**
- TRR: 1.85 (.073), 1.65 (.065)
- TRL: 10.90 (.429), 10.70 (.421)
- 13.50 (.532), 12.80 (.504)
- 330.00 (14.173) MAX.
- 60.00 (2.362) MIN.
- 27.40 (1.079), 23.90 (.941)
- 26.40 (1.039), 24.40 (.961)
- 4.72 (.186), 4.52 (.178)
- 24.30 (.957), 23.90 (.941)
- 15.42 (.609), 15.22 (.601)
- 11.60 (.457), 11.40 (.449)
- 1.75 (.069), 1.25 (.049)
- 1.60 (.063), 1.50 (.059)
- 4.10 (.161), 3.90 (.153)
- 15.90 (.626), 16.10 (.634)
- 11.40 (.449), 11.60 (.457)
- 0.368 (.0145), 0.342 (.0135)
- 30.40 (1.197) MAX.
- 27.40 (1.079), 23.90 (.941)
- 60.00 (2.362) MIN.
- 26.40 (1.039), 24.40 (.961)

**Notes:**
- Data and specifications subject to change without notice.
- This product has been designed and qualified for the Industrial market.
- Qualification Standards can be found on IR's Web site.

**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
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