

IRFR812TRPbF

HEXFET® Power MOSFET

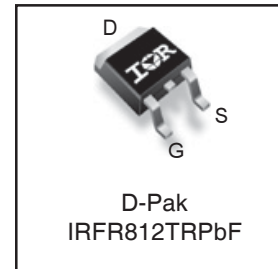
Applications

- Zero Voltage Switching SMPS
- Uninterruptible Power Supplies
- Motor Control applications

V_{DSS}	$R_{DS(on)}$ typ.	T_{rr} typ.	I_D
500V	1.85 Ω	75ns	3.6A

Features and Benefits

- Fast body diode eliminates the need for external diodes in ZVS applications.
- Lower Gate charge results in simpler drive requirements.
- Higher Gate voltage threshold offers improved noise immunity.



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	3.6	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	2.3	
I_{DM}	Pulsed Drain Current ①	14.4	
P_D @ $T_C = 25^\circ\text{C}$	Power Dissipation	78	W
	Linear Derating Factor	0.63	W/ $^\circ\text{C}$
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery dv/dt ③	32	V/ns
T_J	Operating Junction and	-55 to + 150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	3.6	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	14.4		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	$T_J = 25^\circ\text{C}$, $I_S = 3.6\text{A}$, $V_{GS} = 0\text{V}$ ④
t_{rr}	Reverse Recovery Time	—	75	110	ns	$T_J = 25^\circ\text{C}$, $I_F = 3.6\text{A}$
		—	94	140		$T_J = 125^\circ\text{C}$, $di/dt = 100\text{A}/\mu\text{s}$ ④
Q_{rr}	Reverse Recovery Charge	—	135	200	nC	$T_J = 25^\circ\text{C}$, $I_S = 3.6\text{A}$, $V_{GS} = 0\text{V}$ ④
		—	220	330		$T_J = 125^\circ\text{C}$, $di/dt = 100\text{A}/\mu\text{s}$ ④
I_{RRM}	Reverse Recovery Current	—	3.2	4.8	A	$T_J = 25^\circ\text{C}$, $I_S = 3.6\text{A}$, $V_{GS} = 0\text{V}$ ④ $di/dt = 100\text{A}/\mu\text{s}$
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes ① through ⑦ are on page 2

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.37	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 250\mu A$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	1.85	2.2	Ω	$V_{GS} = 10V, I_D = 2.2A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 500V, V_{GS} = 0V$
		—	—	2.0	mA	$V_{DS} = 400V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100	nA	$V_{GS} = -20V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	7.6	—	—	S	$V_{DS} = 50V, I_D = 2.2A$
Q_g	Total Gate Charge	—	—	20	nC	$I_D = 3.6A$
Q_{gs}	Gate-to-Source Charge	—	—	7.3	nC	$V_{DS} = 400V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	7.1	nC	$V_{GS} = 10V$, See Fig. 14a & 14b ④
$t_{d(on)}$	Turn-On Delay Time	—	14	—	ns	$V_{DD} = 250V$
t_r	Rise Time	—	22	—	ns	$I_D = 3.6A$
$t_{d(off)}$	Turn-Off Delay Time	—	24	—	ns	$R_G = 17\Omega$
t_f	Fall Time	—	17	—	ns	$V_{GS} = 10V$, See Fig. 15a & 15b ④
C_{iss}	Input Capacitance	—	810	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	47	—	pF	$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	7.3	—	pF	$f = 1.0\text{MHz}$, See Fig. 5
C_{oss}	Output Capacitance	—	610	—	pF	$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	16	—	pF	$V_{GS} = 0V, V_{DS} = 400V, f = 1.0\text{MHz}$
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	5.9	—	pF	$V_{GS} = 0V, V_{DS} = 0V \text{ to } 400V$ ⑤
$C_{oss \text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)	—	37	—	pF	

Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	150	mJ
I_{AR}	Avalanche Current ①	—	1.8	A
E_{AR}	Repetitive Avalanche Energy ①	—	7.8	mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑥	—	1.6	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient (PCB mount) ⑥ ⑦	—	40	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient ⑥	—	110	$^\circ\text{C/W}$

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 93\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 1.8A$. (See Figure 13).
- ③ $I_{SD} = 3.6A$, $di/dt \leq 520A/\mu s$, $V_{DD} V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$.

④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

⑤ $C_{oss \text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

$C_{oss \text{ eff. (ER)}}$ is a fixed capacitance that stores the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⑥ R_θ is measured at T_J approximately 90°C

⑦ When mounted on 1" square PCB (FR-4 or G-10 Material)

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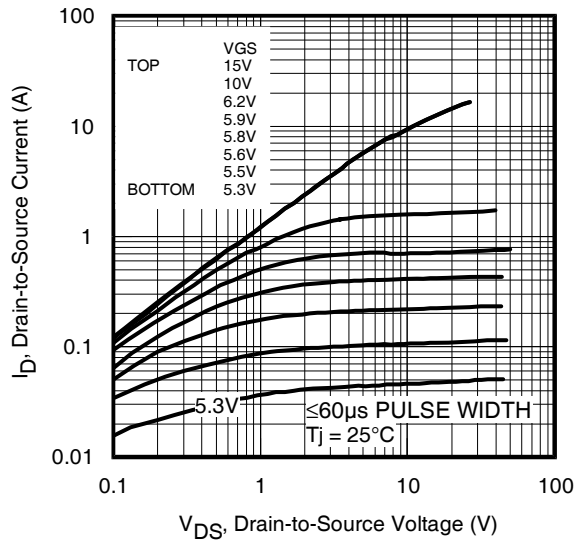


Fig 1. Typical Output Characteristics

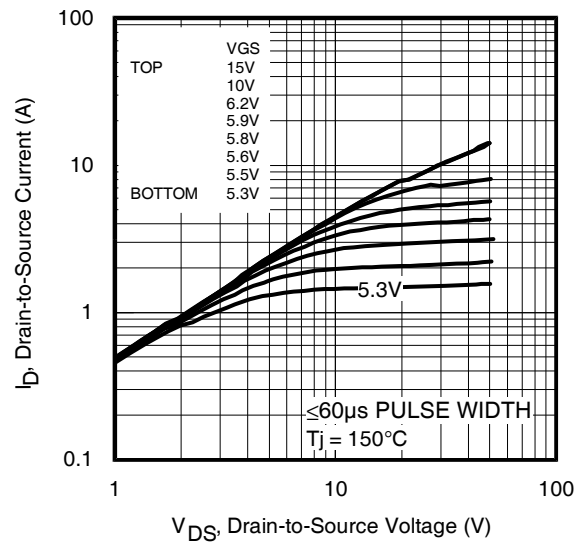


Fig 2. Typical Output Characteristics

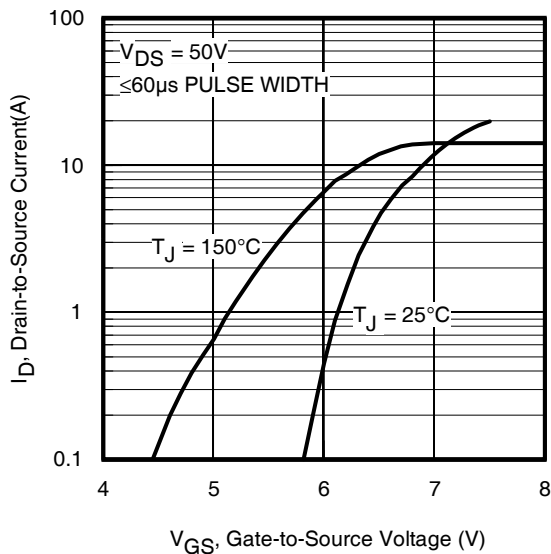


Fig 3. Typical Transfer Characteristics

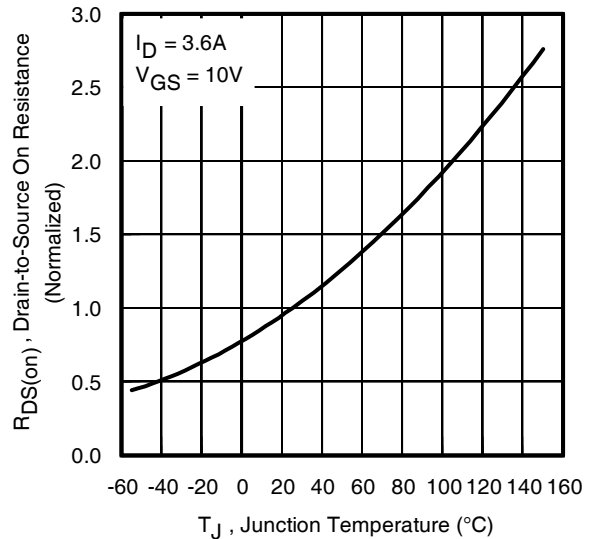


Fig 4. Normalized On-Resistance Vs. Temperature

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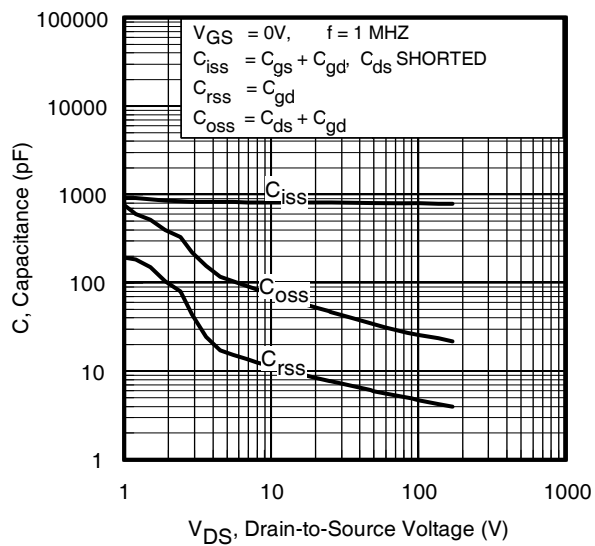


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

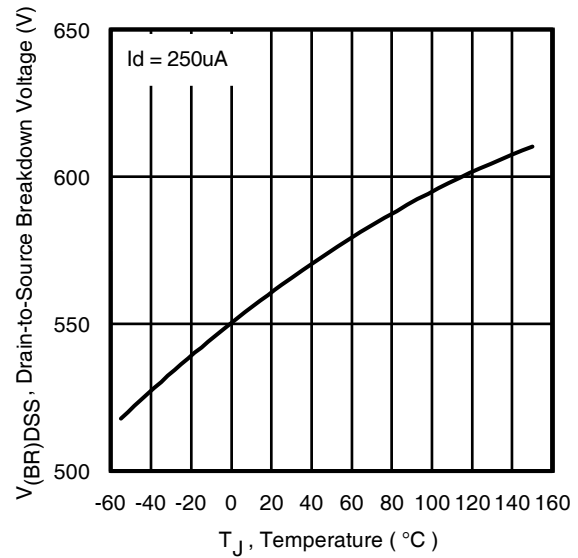
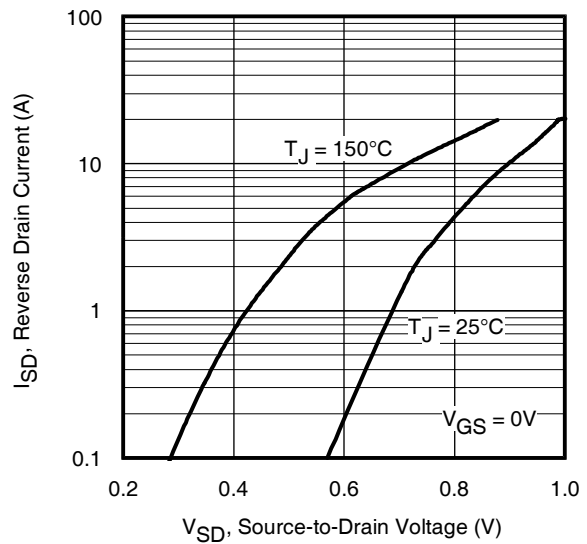
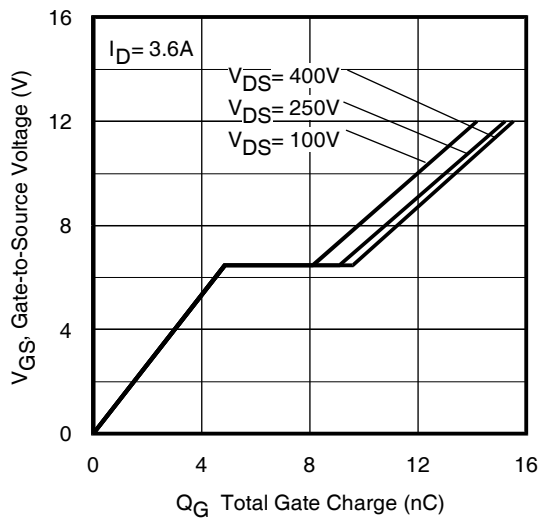


Fig 6. Typ. Breakdown Voltage vs. Temperature



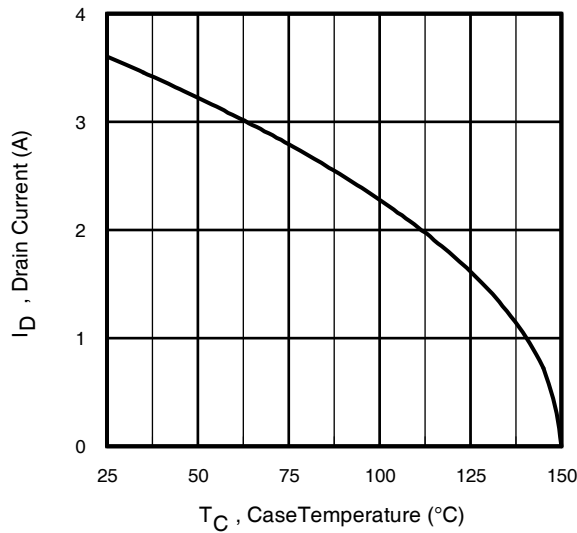


Fig 9. Maximum Drain Current Vs. Case Temperature

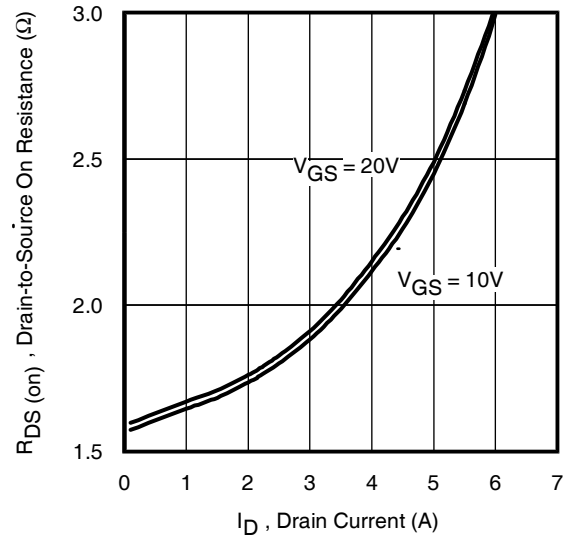


Fig 9. Typical $R_{DS(on)}$ Vs. Drain Current

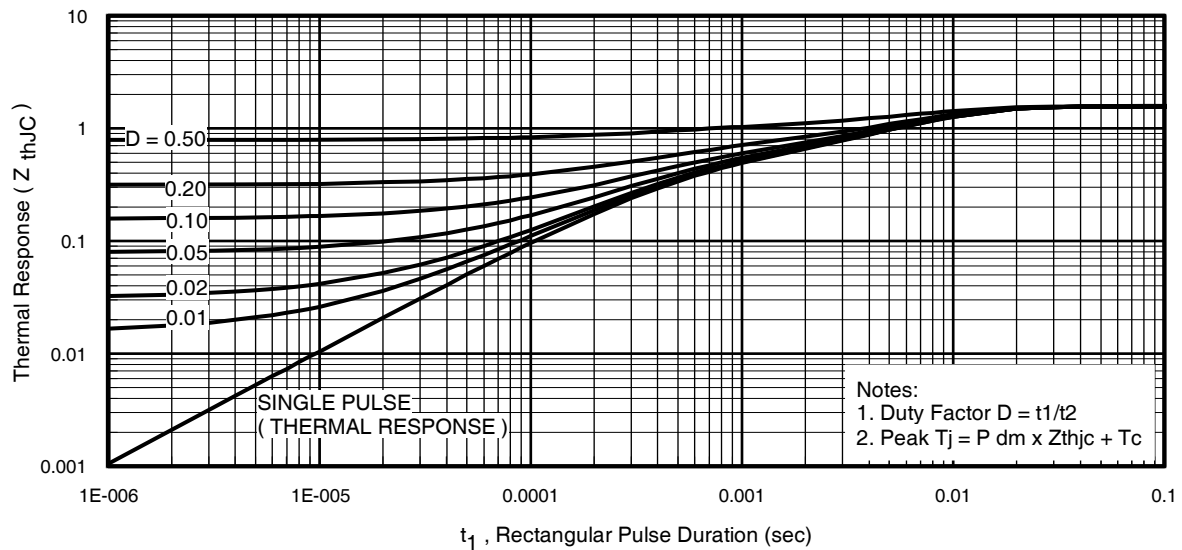


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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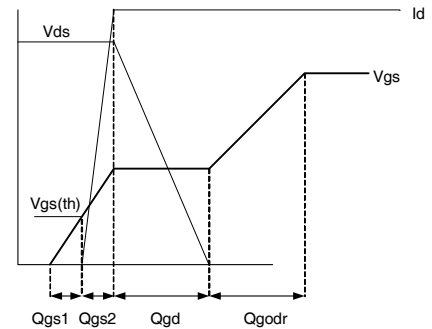
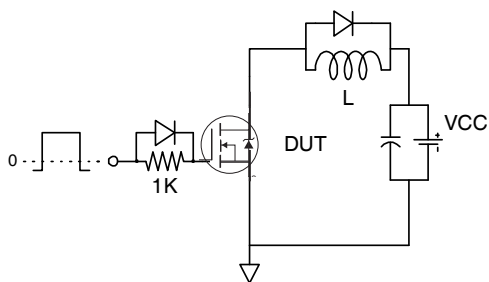
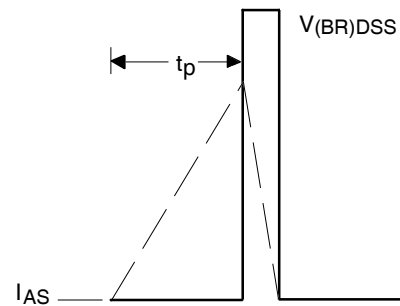
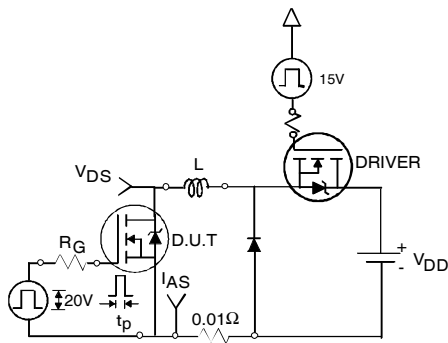
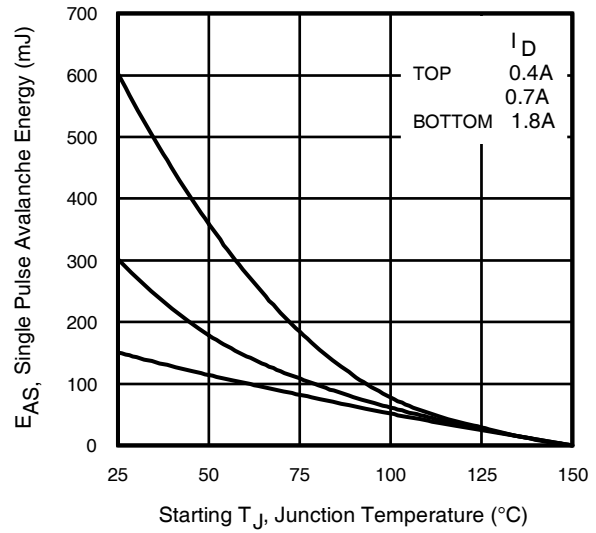
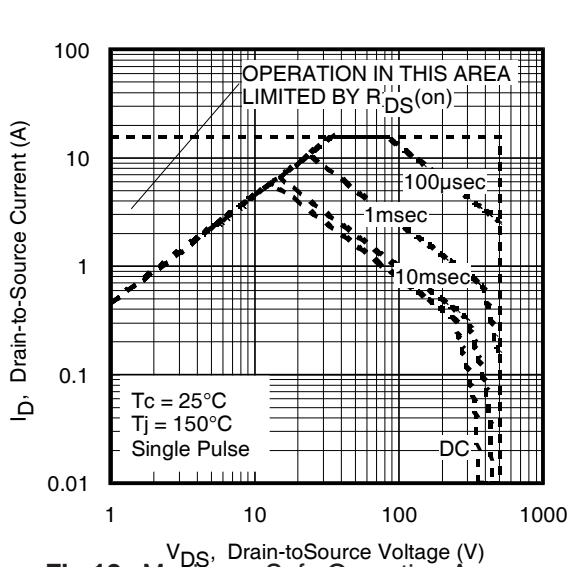


Fig 14a. Gate Charge Test Circuit

Fig 14b. Gate Charge Waveform

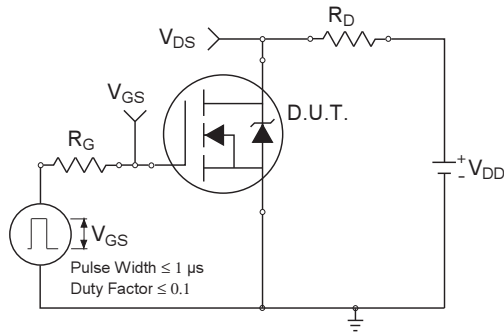


Fig 15a. Switching Time Test Circuit

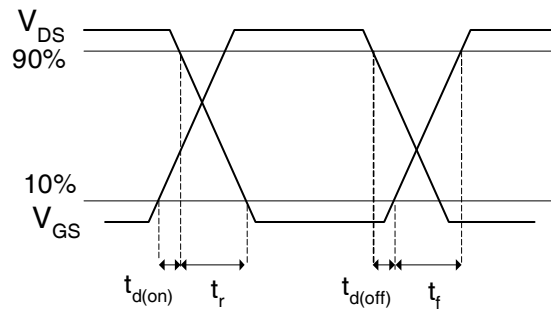
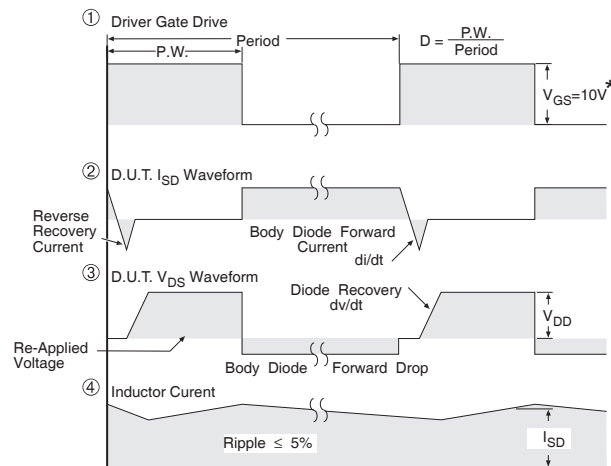
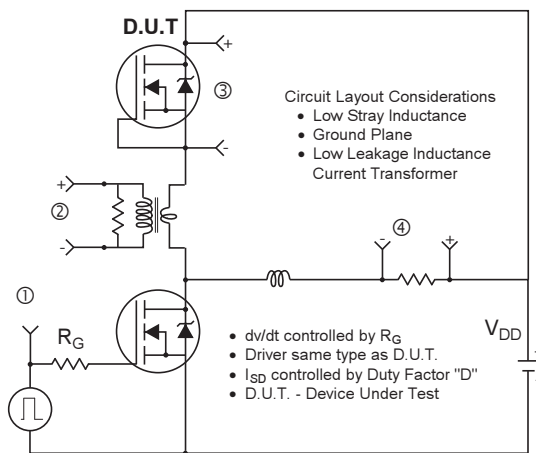


Fig 15b. Switching Time Waveforms

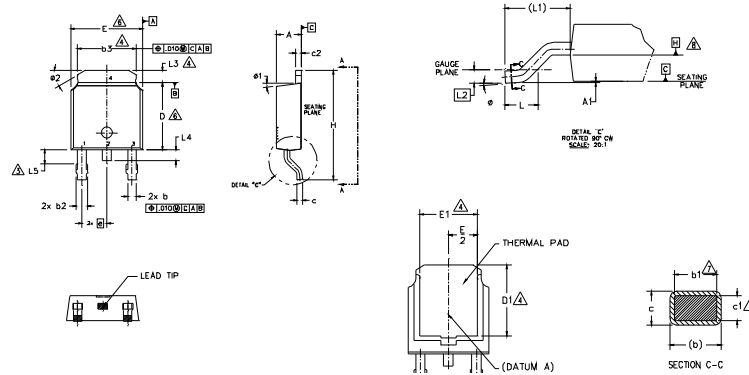


* $V_{GS} = 5V$ for Logic Level Devices

Fig 16. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

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Dimensions are shown in millimeters (inches)



NOTES:

1. - DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. - DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS]
3. Δ - LEAD DIMENSION UNLESS NOTED OTHERWISE
4. - DIMENSION D1, D1 L3 AND L3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
5. - SECTION C - DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
6. - DIMENSION D & E DO NOT INCLUDE WELD FLASH, MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER LEAD. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
7. - DIMENSION D1 & C1 APPLIED TO BARE METAL ONLY.
8. - DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
9. - OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	0.7	0.13	—	— .005	
B	0.7	0.89	.025	.035	
B1	0.76	0.14	.025	.031	
b3	4.95	5.46	.195	.215	
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	
c2	0.46	0.69	.018	.035	
D	6.32	6.22	.250	.245	
E	6.35	—	.205	—	
F	5.26	6.73	.205	.265	
E	4.22	—	.170	—	
E	4.29	BSC	.180	BSC	
L	9.14	10.41	.375	.410	
L	4.00	1.78	.055	.070	
L1	2.74	BSC	.108	RF	
L2	0.59	BSC	.020	BSC	
L3	0.81	1.27	.035	.050	
L4	1.4	1.02	—	.040	
a	1.14	1.62	.045	.060	
a1	0	0"	0"	0"	
a2	0	0"	0"	0"	
a3	0	0"	0"	0"	
a4	0	0"	0"	0"	
a5	0	0"	0"	0"	
a6	0	0"	0"	0"	
a7	0	0"	0"	0"	
a8	0	0"	0"	0"	
a9	0	0"	0"	0"	
a10	0	0"	0"	0"	
a11	0	0"	0"	0"	
a12	0	0"	0"	0"	
a13	0	0"	0"	0"	
a14	0	0"	0"	0"	
a15	0	0"	0"	0"	
a16	0	0"	0"	0"	
a17	0	0"	0"	0"	
a18	0	0"	0"	0"	
a19	0	0"	0"	0"	
a20	0	0"	0"	0"	
a21	0	0"	0"	0"	
a22	0	0"	0"	0"	
a23	0	0"	0"	0"	
a24	0	0"	0"	0"	
a25	0	0"	0"	0"	
a26	0	0"	0"	0"	
a27	0	0"	0"	0"	
a28	0	0"	0"	0"	
a29	0	0"	0"	0"	
a30	0	0"	0"	0"	
a31	0	0"	0"	0"	
a32	0	0"	0"	0"	
a33	0	0"	0"	0"	
a34	0	0"	0"	0"	
a35	0	0"	0"	0"	
a36	0	0"	0"	0"	
a37	0	0"	0"	0"	
a38	0	0"	0"	0"	
a39	0	0"	0"	0"	
a40	0	0"	0"	0"	
a41	0	0"	0"	0"	
a42	0	0"	0"	0"	
a43	0	0"	0"	0"	
a44	0	0"	0"	0"	
a45	0	0"	0"	0"	
a46	0	0"	0"	0"	
a47	0	0"	0"	0"	
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a49	0	0"	0"	0"	
a50	0	0"	0"	0"	
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a52	0	0"	0"	0"	
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a54	0	0"	0"	0"	
a55	0	0"	0"	0"	
a56	0	0"	0"	0"	
a57	0	0"	0"	0"	
a58	0	0"	0"	0"	
a59	0	0"	0"	0"	
a60	0	0"	0"	0"	

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

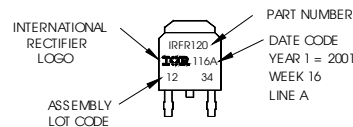
IGBT & CoPAK

1.- GATE
2.- COLLECTOR
3.- EMITTER
4.- COLLECTOR

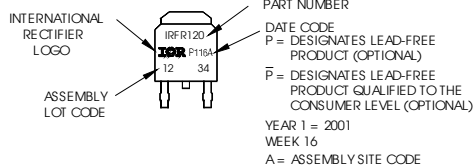
EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 2001
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position indicates "Lead-Free"

"P" in assembly line position indicates
"Lead-Free" qualification to the consumer-level



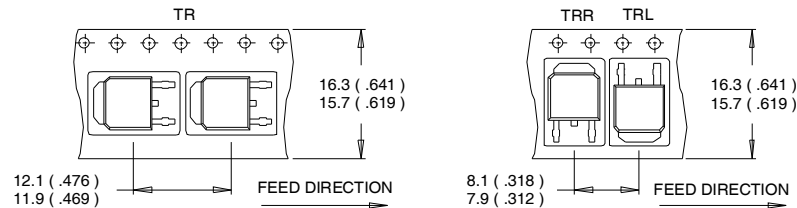
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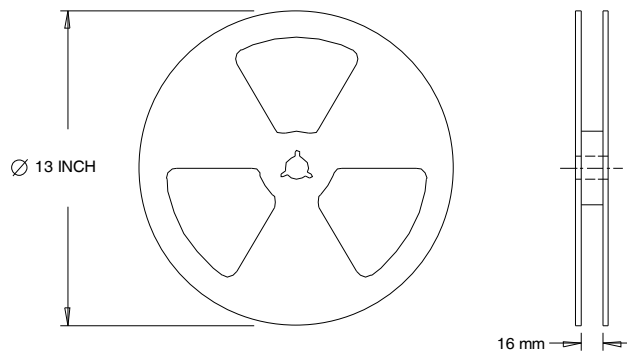
Note:For the most current drawing please refer to IR website at <http://www.irf.com/package/>

D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



- NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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TAC Fax: (310) 252-7903

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