Description
Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET® Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D-Pak is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.

Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>ID @ TC = 25°C</td>
<td>-31</td>
<td>A</td>
</tr>
<tr>
<td>ID @ TC = 100°C</td>
<td>-22</td>
<td>A</td>
</tr>
<tr>
<td>IMD</td>
<td>-110</td>
<td></td>
</tr>
<tr>
<td>PD @ TC = 25°C</td>
<td>110</td>
<td>W</td>
</tr>
<tr>
<td>VGS</td>
<td>0.71</td>
<td>W/C</td>
</tr>
<tr>
<td>EAS</td>
<td>280</td>
<td>mJ</td>
</tr>
<tr>
<td>IAR</td>
<td>-16</td>
<td>A</td>
</tr>
<tr>
<td>EAR</td>
<td>11</td>
<td>mJ</td>
</tr>
<tr>
<td>dv/dt</td>
<td>-5.0</td>
<td>V/ns</td>
</tr>
<tr>
<td>TJ</td>
<td>-55 to +175</td>
<td>°C</td>
</tr>
<tr>
<td>TSTG</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Soldering Temperature, for 10 seconds</td>
<td>300 (1.6mm from case)</td>
</tr>
<tr>
<td></td>
<td>Mounting torque, 6-32 or M3 screw</td>
<td>10 lb•in (1.1N•m)</td>
</tr>
</tbody>
</table>

Thermal Resistance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>RθJC</td>
<td></td>
<td>1.4</td>
<td>°C/W</td>
</tr>
<tr>
<td>RθJA</td>
<td></td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>RθJA</td>
<td></td>
<td>110</td>
<td></td>
</tr>
</tbody>
</table>
### Source-Drain Ratings and Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_S$ (Body Diode)</td>
<td></td>
<td></td>
<td>-31</td>
<td>A</td>
<td>MOSFET symbol showing the</td>
</tr>
<tr>
<td>$I_{SM}$ (Body Diode)</td>
<td></td>
<td></td>
<td>-110</td>
<td></td>
<td>integral reverse p-n junction diode.</td>
</tr>
<tr>
<td>$V_{DS}$</td>
<td></td>
<td></td>
<td>-1.3</td>
<td>V</td>
<td>$T_J = 25^\circ C, I_S = -16A, V_{GS} = 0V$</td>
</tr>
<tr>
<td>$Q_{tr}$</td>
<td>71</td>
<td>110</td>
<td></td>
<td>ns</td>
<td>$T_J = 25^\circ C, f = 1.0MHz$</td>
</tr>
<tr>
<td>$Q_{dr}$</td>
<td></td>
<td></td>
<td>250</td>
<td>nC</td>
<td>$di/dt = -100A/\mu s$</td>
</tr>
</tbody>
</table>

**Notes:**

1. Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 11)
2. $V_{DD} = -25V$, starting $T_J = 25^\circ C$, $L = 2.1mH$, $R_D = 25\Omega$, $I_{AS} = -16A$. (See Figure 12)
3. $I_{SD} = -16A$, $di/dt \leq -280A/\mu s$, $V_{DD} \leq V_{BRDSS}$, $T_J \leq 175^\circ C$

* When mounted on 1" square PCB (FR-4 or G-10 Material).
+ For recommended footprint and soldering techniques refer to application note #AN-994.
+ Uses typical socket mount.
Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance Vs. Temperature
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage

**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage

**Fig 7.** Typical Source-Drain Diode Forward Voltage

**Fig 8.** Maximum Safe Operating Area
Fig 9. Maximum Drain Current Vs. Case Temperature

Fig 10a. Switching Time Test Circuit

Fig 10b. Switching Time Waveforms

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case
IRFR/U5305PbF

**Fig 12a.** Unclamped Inductive Test Circuit

**Fig 12b.** Unclamped Inductive Waveforms

**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

**Fig 13a.** Basic Gate Charge Waveform

**Fig 13b.** Gate Charge Test Circuit
Peak Diode Recovery dv/dt Test Circuit

- D.U.T. - Device Under Test
- dv/dt controlled by $R_G$
- $I_{SD}$ controlled by Duty Factor "D"
- $V_{GS} = 10V$

Circuit Layout Considerations
- Low Stray Inductance
- Ground Plane
- Low Leakage Inductance
- Current Transformer

Driver Gate Drive
- $D = P.W.$ Period

D.U.T. $I_{SD}$ Waveform

Reverse Recovery Current

D.U.T. $V_{DS}$ Waveform

Re-Applied Voltage

Inductor Current

$\Delta V_{DS}$

$\Delta I_{SD}$

Ripple $\leq 5\%$

*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 14. For P-Channel HEXFETS
I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)

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Notes:
2. Dimensions are shown in millimeters (inches).
3. Dimensions D & E do not include mold flash, mold flash shall not exceed 0.005" (0.127 mm). These dimensions are measured at the outermost extremes of the plastic body.
4. Thermal pad contour option within dimension D4, L2, E1 & E4.
5. Lead dimension uncontrolled in L3.

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EXAMPLE:
WITH ASSEMBLY
LOT CODE 5678
ASSEMBLED ON WED, 10, 1999
IN THE ASSEMBLY LINE "A"
Note: "P" in assembly line position indicates "Lead-Free"

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I-Pak (TO-251AA) Part Marking Information

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www.irf.com
D-Pak (TO-252AA) Tape & Reel Information
Dimensions are shown in millimeters (inches)

NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.

NOTES:
1. OUTLINE CONFORMS TO EIA-481.
Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/
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