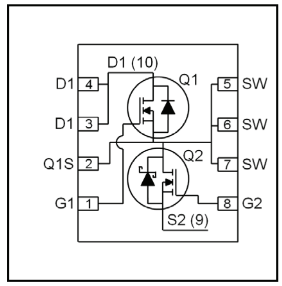
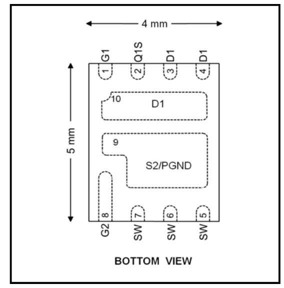
International
IOR Rectifier

Fast*IR*FET™
IRFH4257DPbF

HEXFET® Power MOSFET

	Q1	Q2	
V_{DSS}	25	25	V
$R_{DS(on)}$ max (@V_{GS} = 4.5V)	4.70	1.80	mΩ
Qg (typical)	9.7	23	nC
I_D (@T_C = 25°C)	25⑦	25⑦	A





Applications

- Control and Synchronous MOSFETs for synchronous buck converters

Dual PQFN 5X4 mm

Features		Benefits
Control and synchronous MOSFETs in one package		Increased power density
Low charge control MOSFET (9.7nC typical)		Lower switching losses
Low R_{DSON} synchronous MOSFET (<1.8mΩ)	results in	Lower conduction losses
Intrinsic Schottky Diode with Low Forward Voltage on Q2	⇒	Lower Switching Losses
RoHS Compliant, Halogen-Free		Environmentally friendlier
MSL1, Industrial Qualification		Increased reliability

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFH4257DPbF	Dual PQFN 5mm x 4mm	Tape and Reel	4000	IRFH4257DTRPbF

Absolute Maximum Ratings

	Parameter	Q1 Max.	Q2 Max.	Units
V_{GS}	Gate-to-Source Voltage	± 20		V
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 4.5V	68⑥⑦	111⑥⑦	A
I_D @ T_C = 70°C	Continuous Drain Current, V_{GS} @ 4.5V	54⑥⑦	88⑥⑦	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 4.5V (Source Bonding Technology Limited)	25⑦	25⑦	
I_{DM}	Pulsed Drain Current	120⑧	375⑧	
P_D @T_C = 25°C	Power Dissipation	25	28	W
P_D @T_C = 70°C	Power Dissipation	16	18	
	Linear Derating Factor	0.20	0.22	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150		°C

Thermal Resistance

	Parameter	Q1 Max.	Q2 Max.	Units
$R_{\theta JC}$ (Bottom)	Junction-to-Case ④	5.0	4.5	°C/W
$R_{\theta JC}$ (Top)	Junction-to-Case ④	33	26	
$R_{\theta JA}$	Junction-to-Ambient ⑤	45	40	
$R_{\theta JA}$ (<10s)	Junction-to-Ambient ⑤	30	27	

Notes ① through ⑧ are on page 12

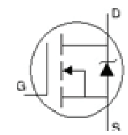
Static @ T_J = 25°C (unless otherwise specified)

	Parameter		Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	Q1	25	—	—	V	V_{GS} = 0V, I_D = 250μA
		Q2	25	—	—		V_{GS} = 0V, I_D = 1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	Q1	—	22	—	mV/°C	Reference to 25°C, I_D = 1.0mA
		Q2	—	22	—		Reference to 25°C, I_D = 10mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	Q1	—	2.7	3.4	mΩ	V_{GS} = 10V, I_D = 25A ③
		Q2	—	1.1	1.4		V_{GS} = 10V, I_D = 25A ③
		Q1	—	3.7	4.7		V_{GS} = 4.5V, I_D = 25A ③
		Q2	—	1.4	1.8		V_{GS} = 4.5V, I_D = 25A ③
$V_{GS(th)}$	Gate Threshold Voltage	Q1	1.1	1.6	2.1	V	Q1: V_{DS} = V_{GS}, I_D = 35μA
		Q2	1.1	1.6	2.1		Q2: V_{DS} = V_{GS}, I_D = 100μA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	Q1	—	-5.4	—	mV/°C	Q1: V_{DS} = V_{GS}, I_D = 35μA
		Q2	—	-5.3	—		Q2: V_{DS} = V_{GS}, I_D = 1mA
I_{DSS}	Drain-to-Source Leakage Current	Q1	—	—	1.0	μA	V_{DS} = 20V, V_{GS} = 0V
		Q2	—	—	250		V_{DS} = 20V, V_{GS} = 0V
I_{GSS}	Gate-to-Source Forward Leakage	Q1	—	—	100	nA	V_{GS} = 20V
		Q2	—	—	100		V_{GS} = 20V
	Gate-to-Source Reverse Leakage	Q1	—	—	-100		V_{GS} = -20V
		Q2	—	—	-100		V_{GS} = -20V
gfs	Forward Transconductance	Q1	100	—	—	S	V_{DS} = 10V, I_D = 25A
		Q2	138	—	—		V_{DS} = 10V, I_D = 25A
Q_g	Total Gate Charge	Q1	—	9.7	15	nC	Q1 V_{DS} = 13V V_{GS} = 4.5V, I_D = 25A Q2 V_{DS} = 13V V_{GS} = 4.5V, I_D = 25A
		Q2	—	23	35		
Q_{gs1}	Pre-Vth Gate-to-Source Charge	Q1	—	2.4	—		
		Q2	—	5.1	—		
Q_{gs2}	Post-Vth Gate-to-Source Charge	Q1	—	1.2	—		
		Q2	—	2.6	—		
Q_{gd}	Gate-to-Drain Charge	Q1	—	3.4	—		
		Q2	—	7.6	—		
Q_{godr}	Gate Charge Overdrive	Q1	—	2.7	—		
		Q2	—	7.7	—		
Q_{sw}	Switch Charge (Q_{gs2} + Q_{gd})	Q1	—	4.6	—		
		Q2	—	10.2	—		
Q_{oss}	Output Charge	Q1	—	10	—	nC	V_{DS} = 16V, V_{GS} = 0V
		Q2	—	25	—		
R_G	Gate Resistance	Q1	—	1.4	—	Ω	
		Q2	—	0.7	—		
$t_{d(on)}$	Turn-On Delay Time	Q1	—	8.2	—	ns	Q1 V_{DS} = 13V V_{GS} = 4.5V I_D = 25A, Rg = 1.8Ω Q2 V_{DS} = 13V V_{GS} = 4.5V I_D = 25A, Rg = 1.8Ω
		Q2	—	12	—		
t_r	Rise Time	Q1	—	47	—		
		Q2	—	51	—		
$t_{d(off)}$	Turn-Off Delay Time	Q1	—	12	—		
		Q2	—	20	—		
t_f	Fall Time	Q1	—	20	—		
		Q2	—	25	—		
C_{iss}	Input Capacitance	Q1	—	1321	—	pF	V_{GS} = 0V V_{DS} = 13V f = 1.0MHz
		Q2	—	3161	—		
C_{oss}	Output Capacitance	Q1	—	365	—		
		Q2	—	965	—		
C_{rss}	Reverse Transfer Capacitance	Q1	—	101	—		
		Q2	—	237	—		

Avalanche Characteristics

	Parameter	Typ.	Q1 Max.	Q2 Max.	Units
E_{AS}	Single Pulse Avalanche Energy [2]	——	42	387	mJ

Diode Characteristics

	Parameter		Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current	Q1	——	——	25[7]	A	MOSFET symbol
	(Body Diode)	Q2	——	——	25[7]		showing the
I_{SM}	Pulsed Source Current	Q1	——	——	120[8]	A	integral reverse 
	(Body Diode)	Q2	——	——	375[8]		p-n junction diode.
V_{SD}	Diode Forward Voltage	Q1	——	——	1.0	V	T_J = 25°C, I_S = 25A, V_{GS} = 0V[3]
		Q2	——	——	0.75		T_J = 25°C, I_S = 25A, V_{GS} = 0V[3]
t_{rr}	Reverse Recovery Time	Q1	——	18	——	ns	Q1 T_J = 25°C, I_F = 25A
		Q2	——	30	——		V_{DD} = 13V, di/dt = 200A/μs [3]
Q_{rr}	Reverse Recovery Charge	Q1	——	16	——	nC	Q2 T_J = 25°C, I_F = 25A
		Q2	——	37	——		V_{DD} = 13V, di/dt = 200A/μs [3]

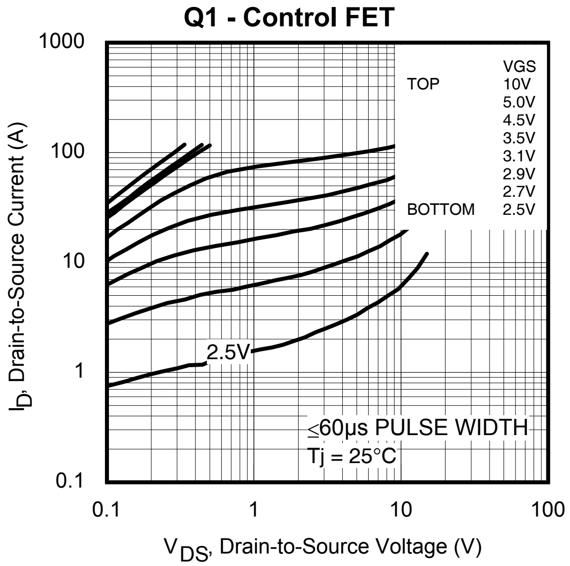


Fig 1. Typical Output Characteristics

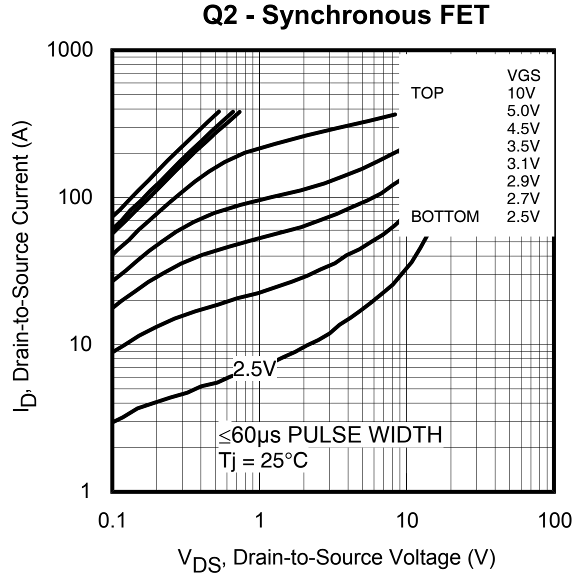


Fig 2. Typical Output Characteristics

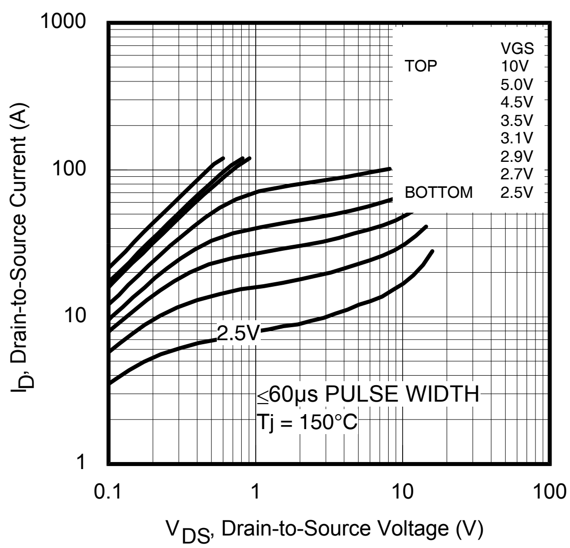


Fig 3. Typical Output Characteristics

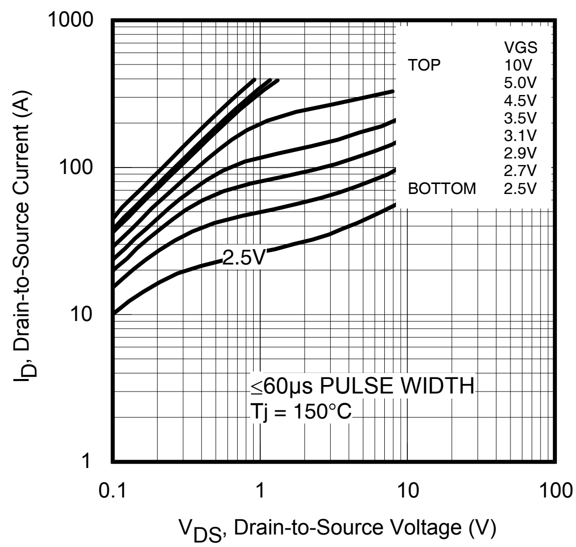


Fig 4. Typical Output Characteristics

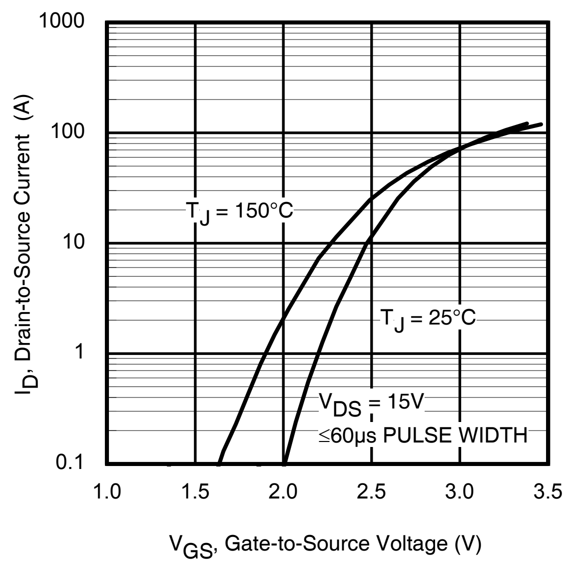


Fig 5. Typical Transfer Characteristics

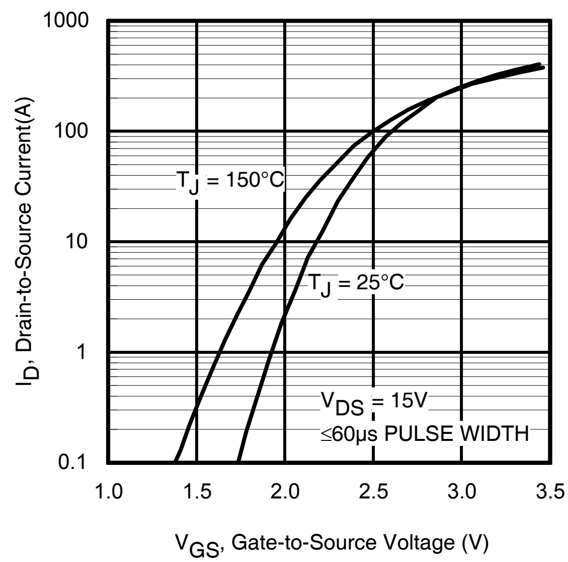


Fig 6. Typical Transfer Characteristics

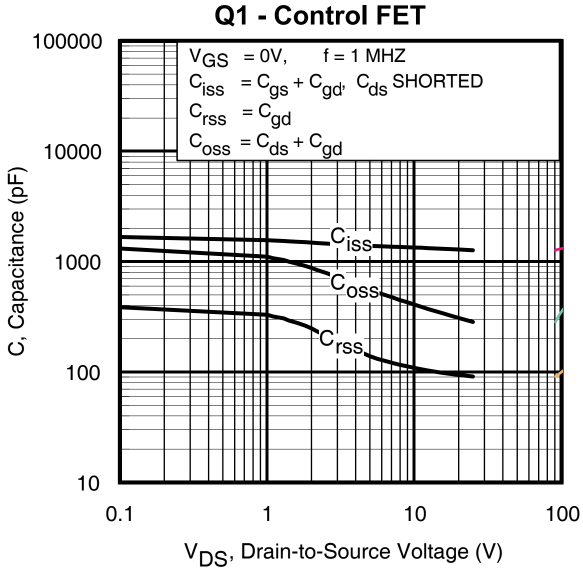


Fig 7. Typical Capacitance vs. Drain-to-Source Voltage

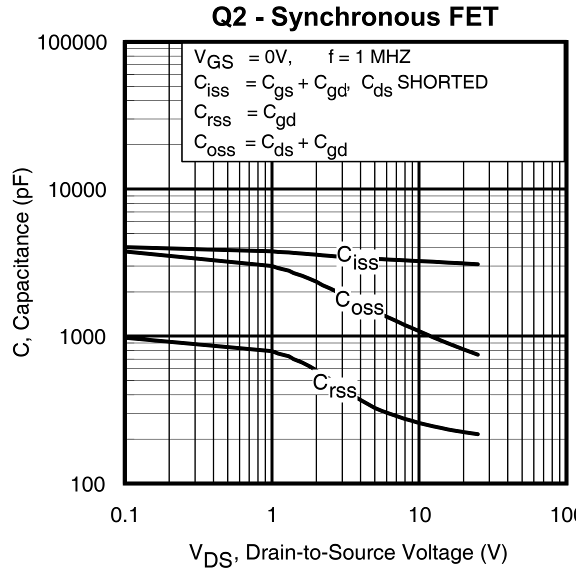


Fig 8. Typical Capacitance vs. Drain-to-Source Voltage

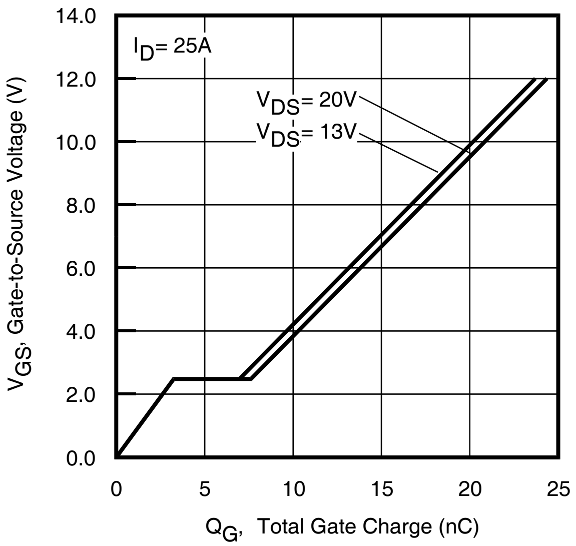


Fig 9. Typical Gate Charge vs. Gate-to-Source Voltage

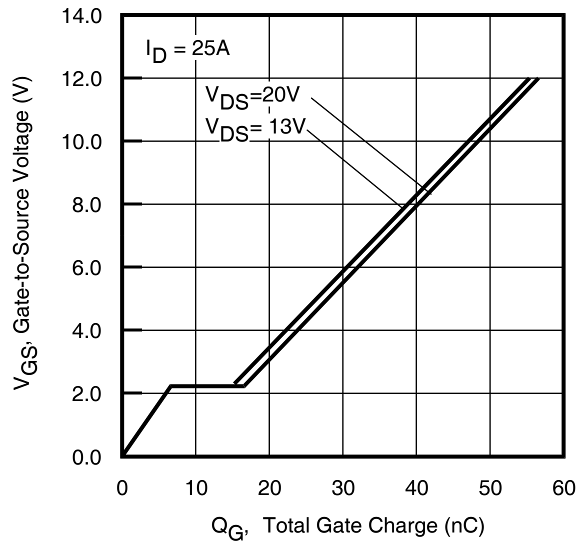


Fig 10. Typical Gate Charge vs. Gate-to-Source Voltage

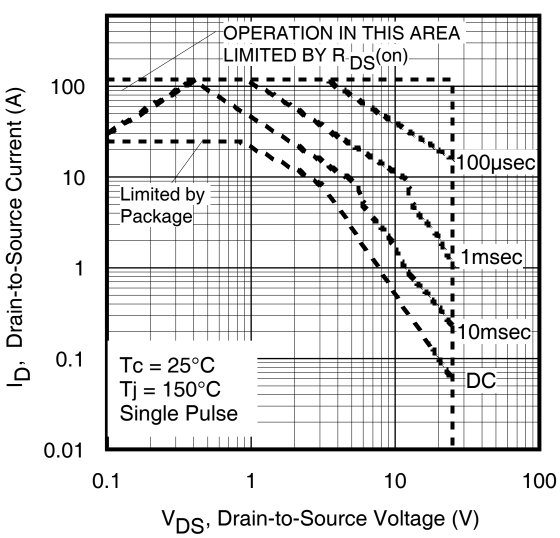


Fig 11. Maximum Safe Operating Area

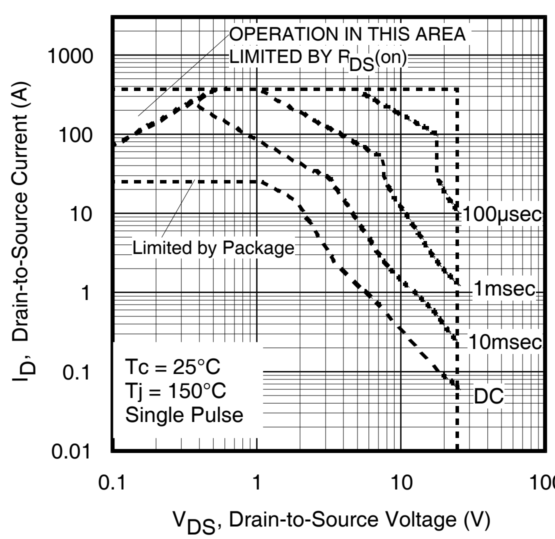


Fig 12. Maximum Safe Operating Area

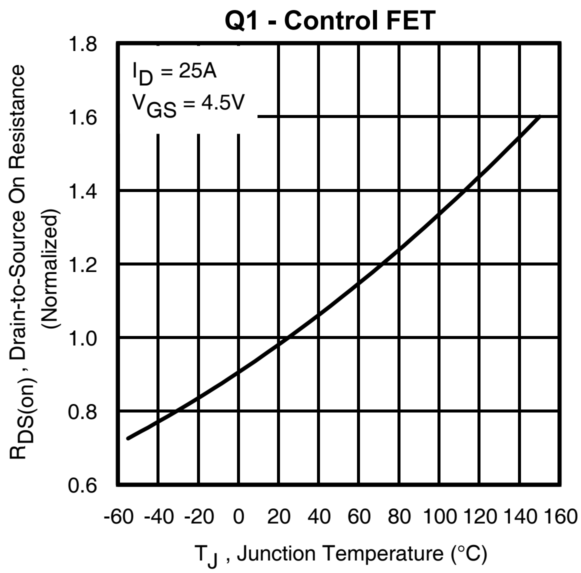


Fig 13. Normalized On-Resistance vs. Temperature

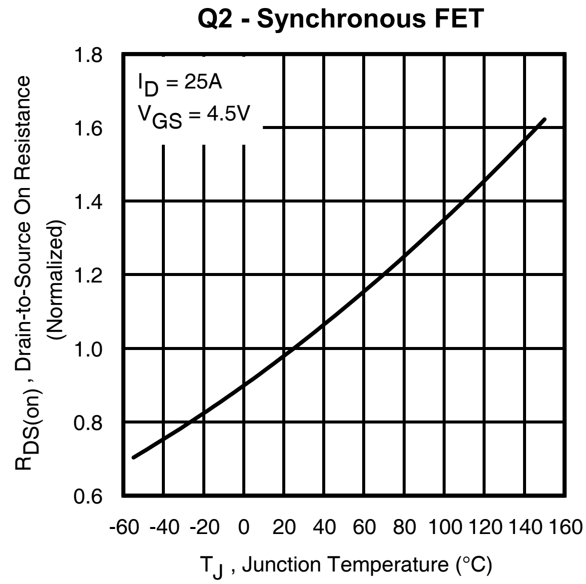


Fig 14. Normalized On-Resistance vs. Temperature

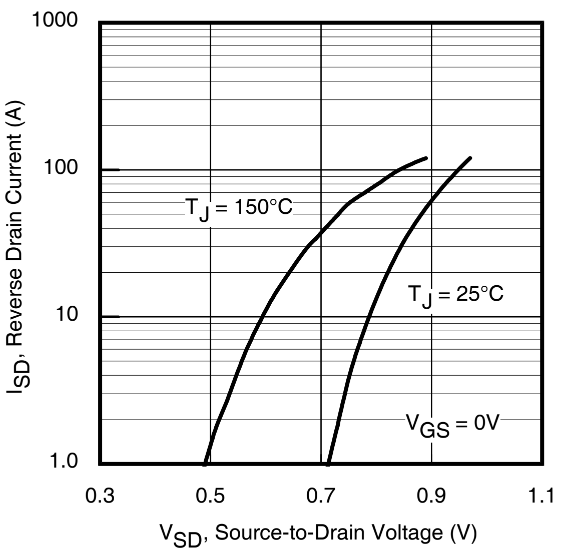


Fig 15. Typical Source-Drain Diode Forward Voltage

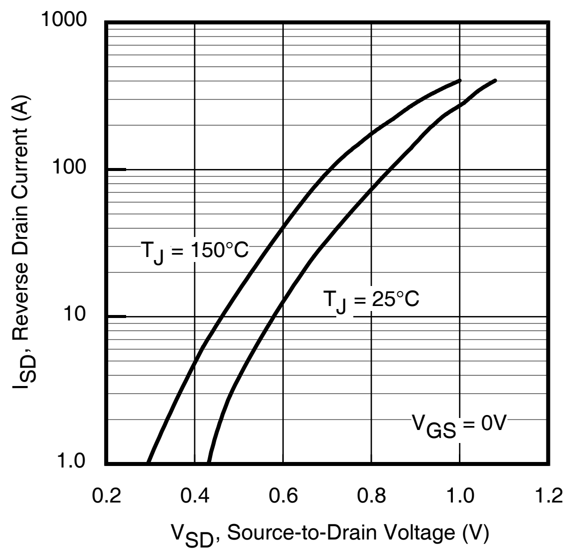


Fig 16. Typical Source-Drain Diode Forward Voltage

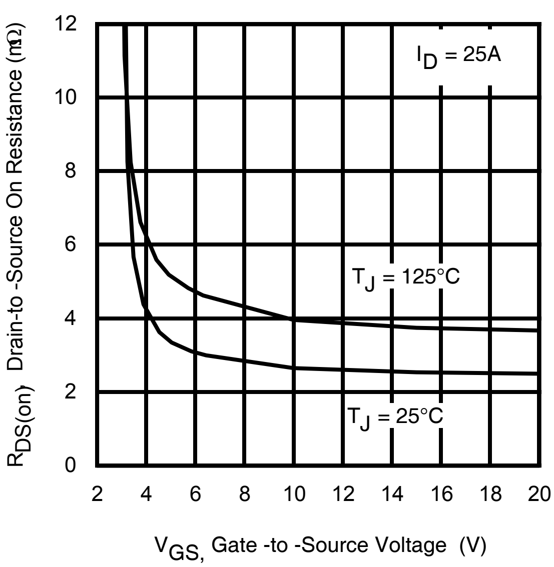


Fig 17. Typical On-Resistance vs. Gate Voltage

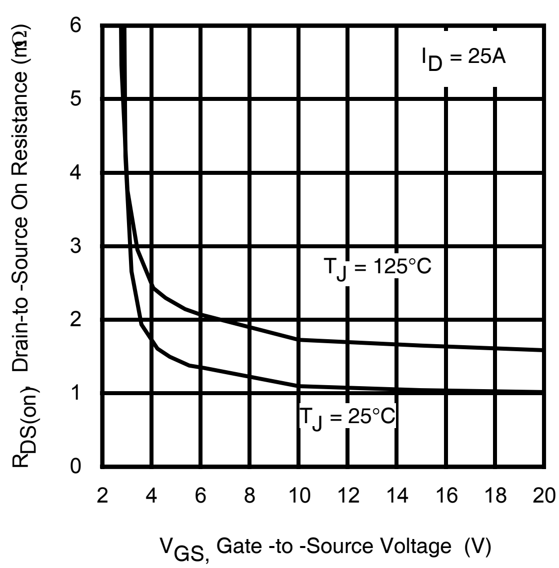


Fig 18. Typical On-Resistance vs. Gate Voltage

Q1 - Control FET

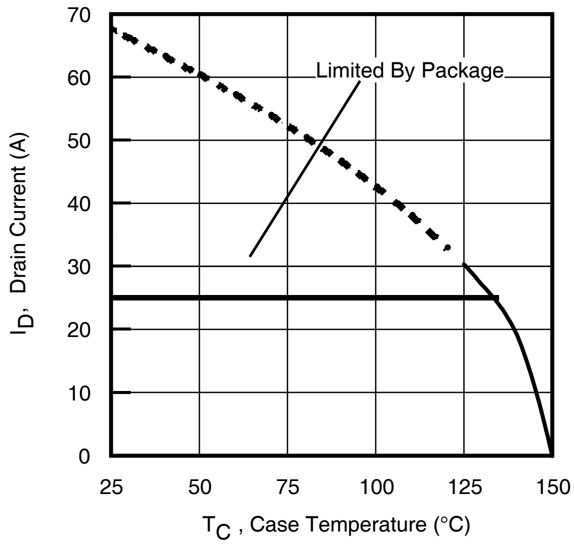


Fig 19. Maximum Drain Current vs. Case Temperature

Q2 - Synchronous FET

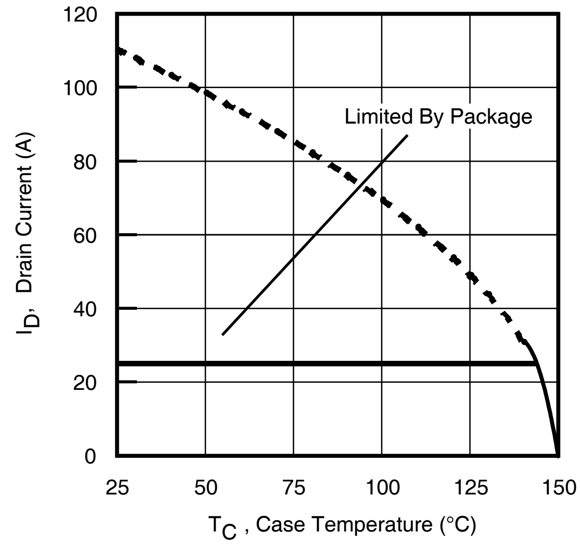


Fig 20. Maximum Drain Current vs. Case Temperature

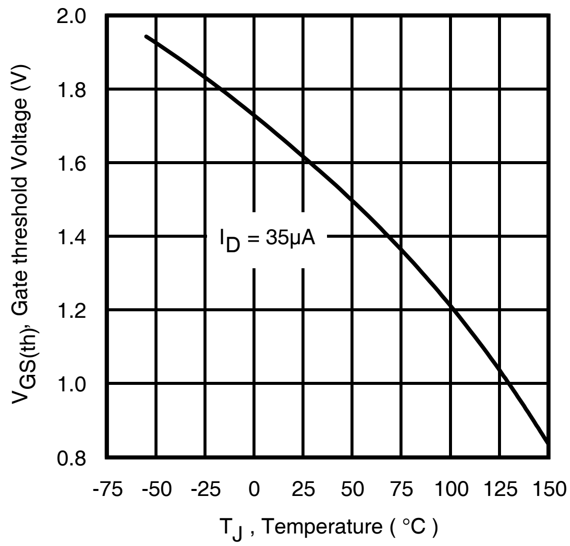


Fig 21. Threshold Voltage vs. Temperature

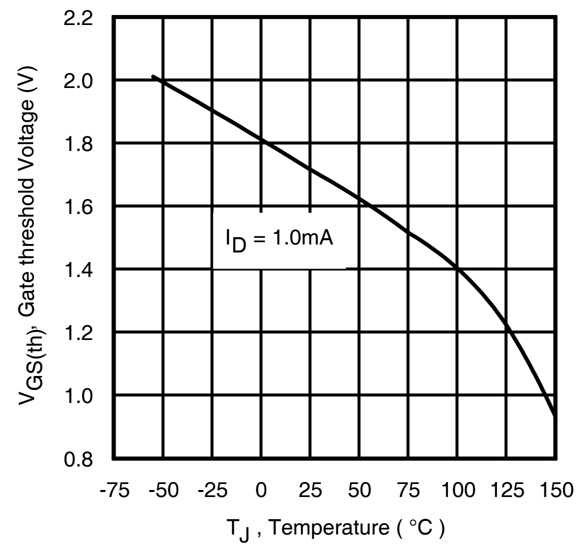


Fig 22. Threshold Voltage vs. Temperature

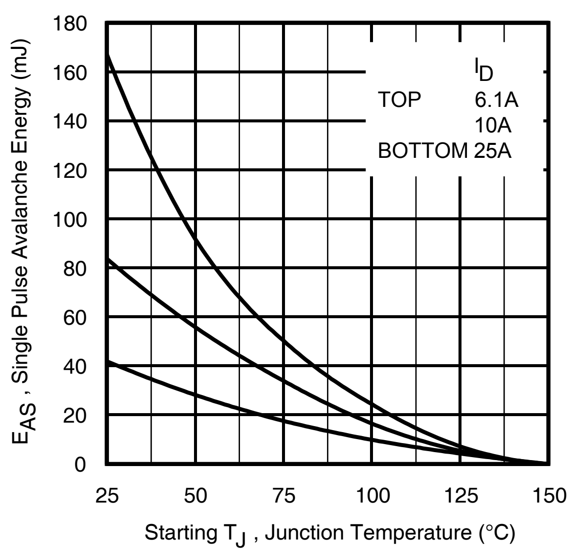


Fig 23. Maximum Avalanche Energy vs. Drain Current

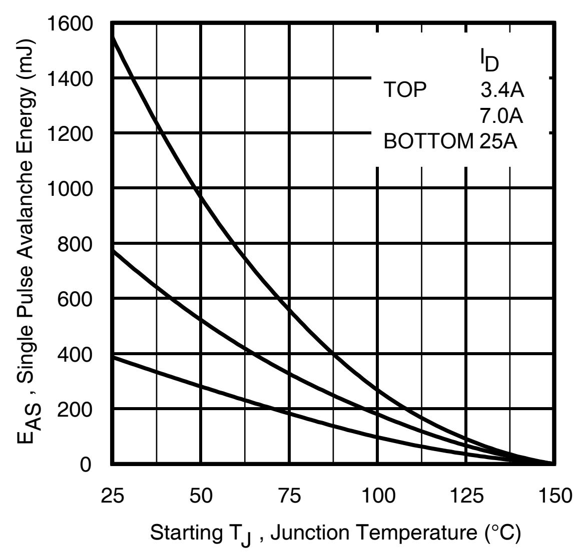


Fig 24. Maximum Avalanche Energy vs. Drain Current

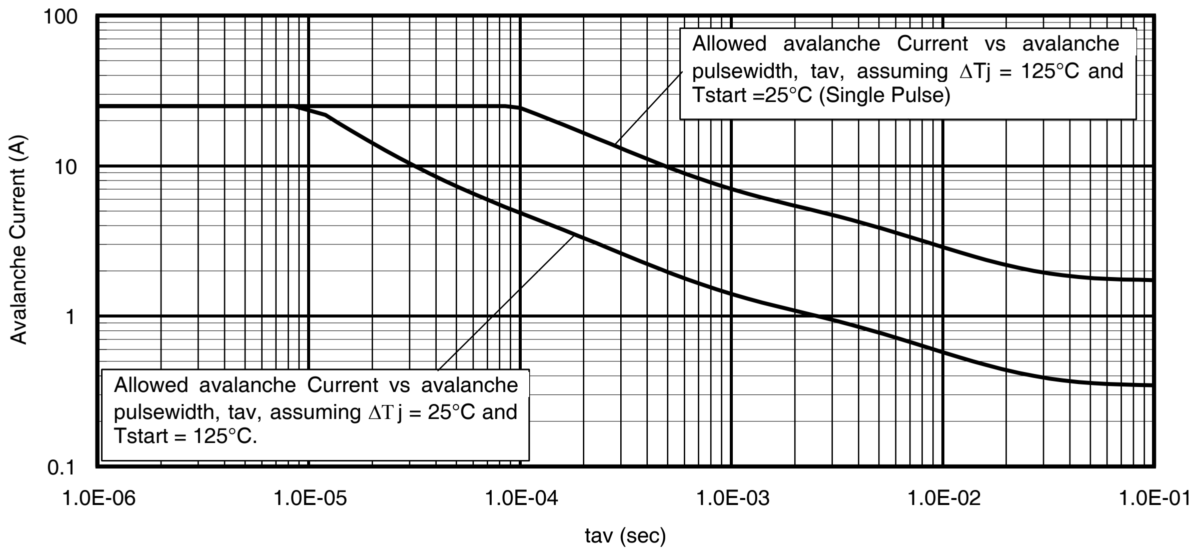


Fig 25. Typical Avalanche Current vs. Pulse Width (Q1)

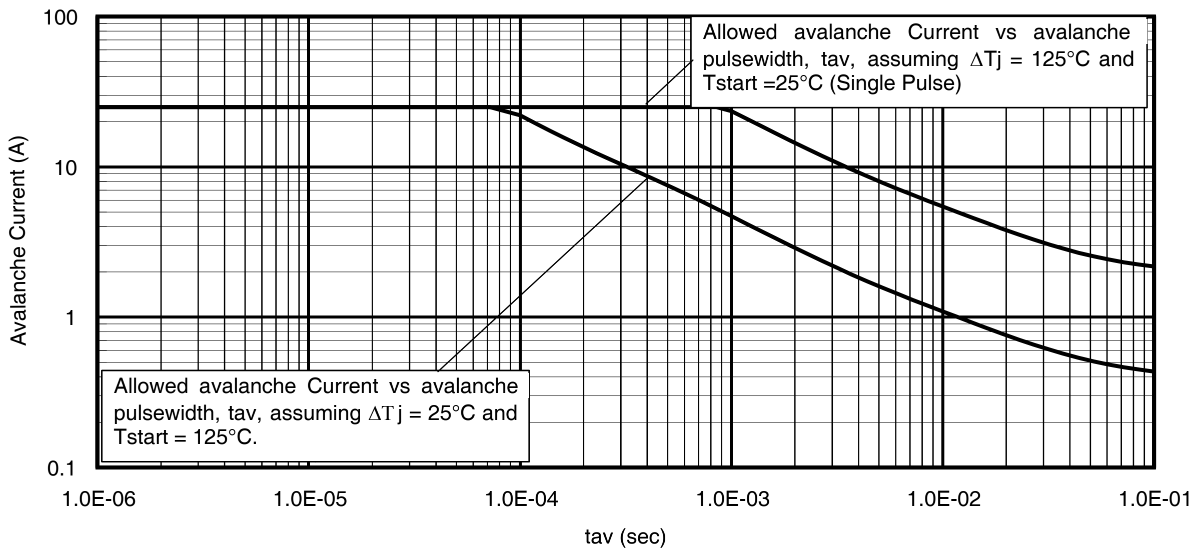


Fig 26. Typical Avalanche Current vs. Pulse Width (Q2)

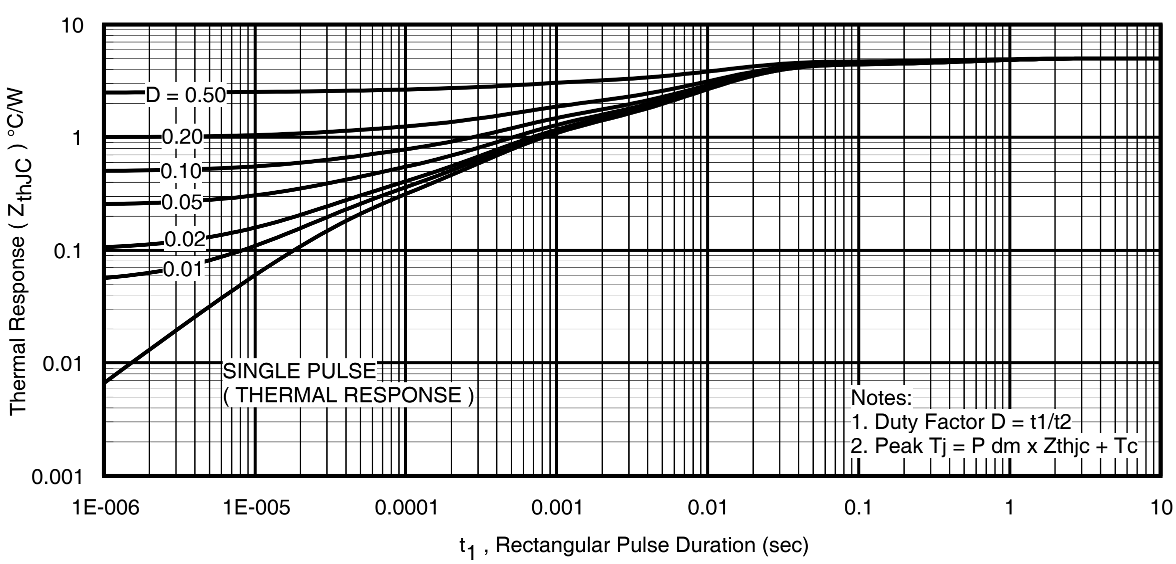


Fig 27. Maximum Effective Transient Thermal Impedance, Junction-to-Case (Q1)

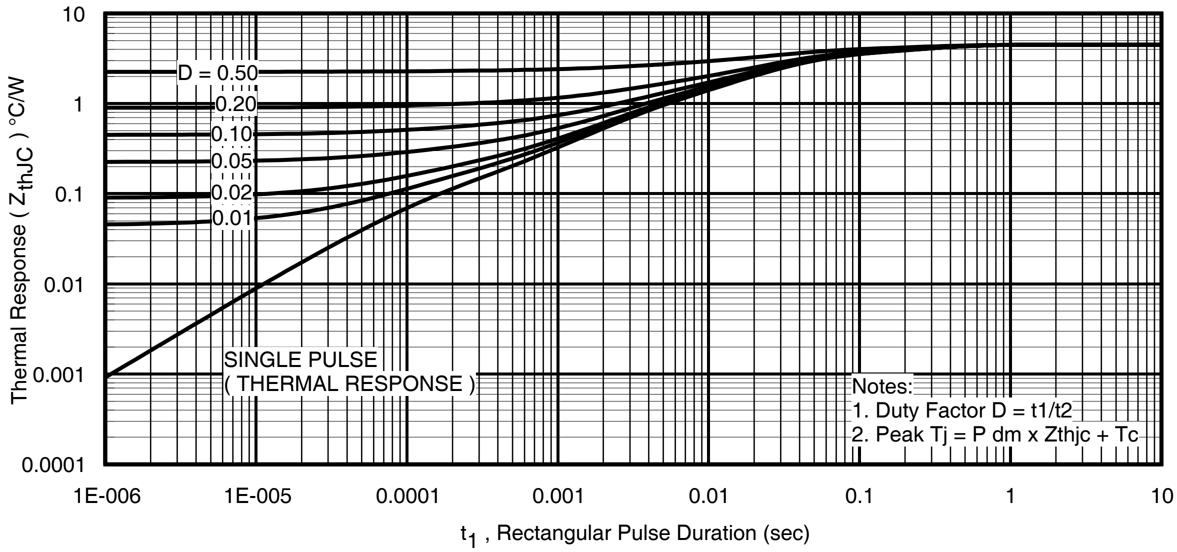
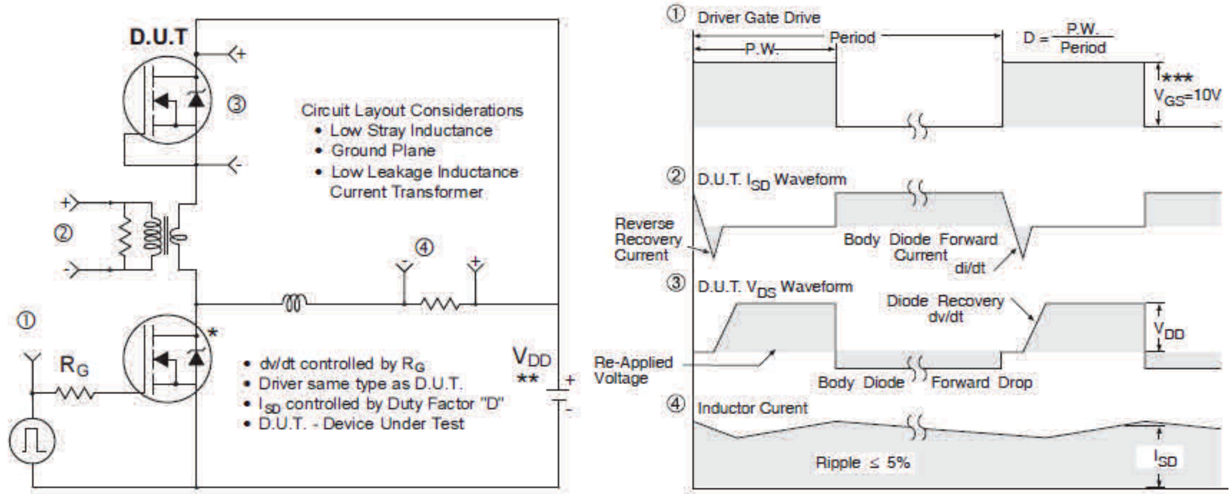


Fig 28. Maximum Effective Transient Thermal Impedance, Junction-to-Case (Q2)



* Use P-Channel Driver for P-Channel Measurements

** Reverse Polarity for P-Channel

*** V_{GS} = 5V for Logic Level Devices

Fig 29. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

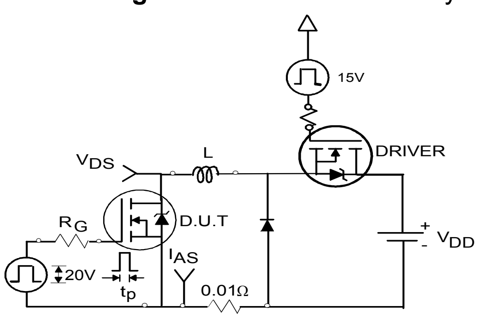


Fig 30a. Unclamped Inductive Test Circuit

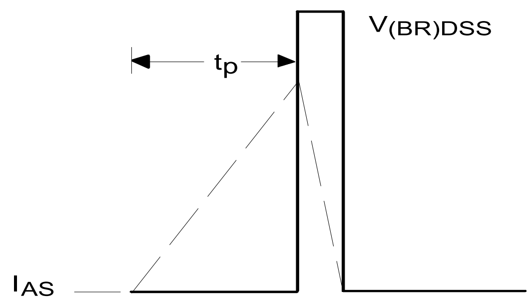


Fig 30b. Unclamped Inductive Waveforms

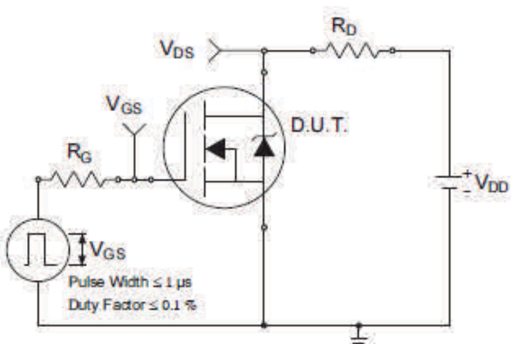


Fig 31a. Switching Time Test Circuit

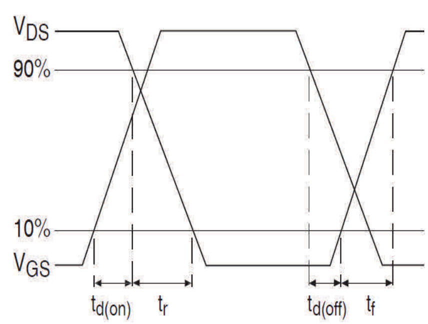


Fig 31b. Switching Time Waveforms

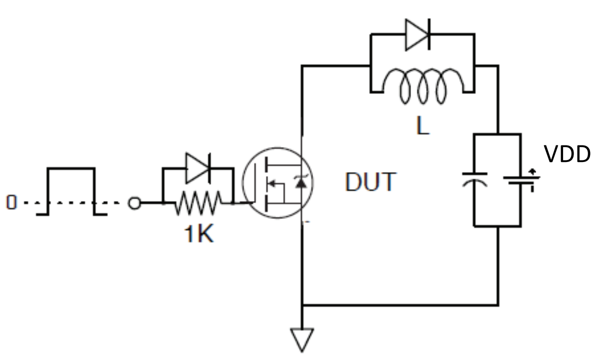


Fig 32a. Gate Charge Test Circuit

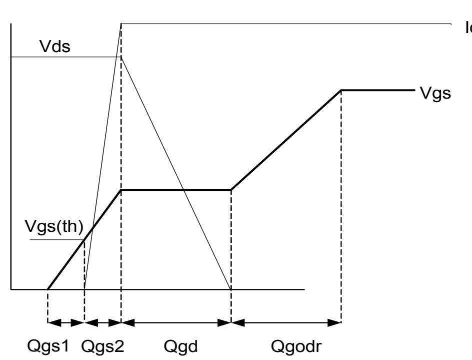
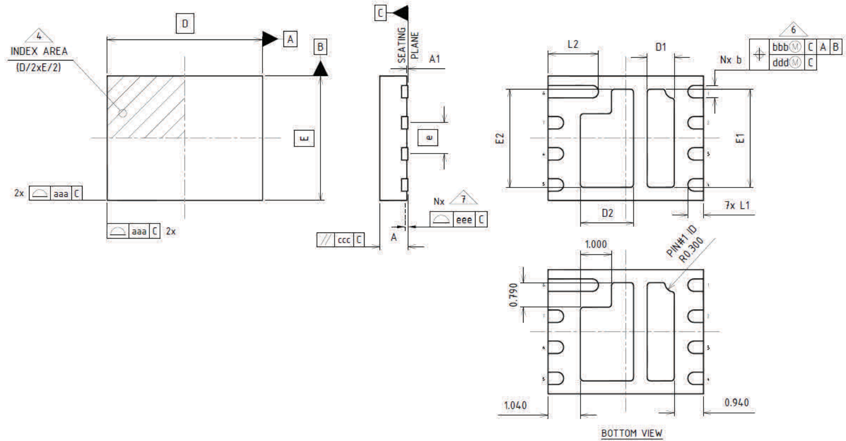


Fig 32b. Gate Charge Waveform

Dual PQFN 5x4 Package Details

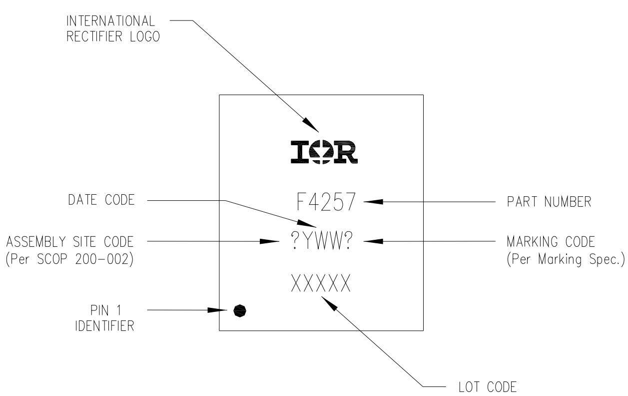


Dimension Table				
Thickness / Symbol	V-Very Thin			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
b	0.30	0.40	0.45	6
D	5.00 BSC			
E	4.00 BSC			
e	1.00 BSC			
D1	0.72	0.87	0.97	
E1	3.01	3.16	3.26	
D2	1.56	1.71	1.81	
E2	3.01	3.16	3.26	
L1	0.40	0.50	0.60	
L2	1.562	1.662	1.762	
aaa	0.05			
bbb	0.10			
ccc	0.10			
ddd	0.05			
eee	0.08			
N	8			3
NE	4			5
NOTES	1, 2			
LF DWG NO.	B-3664			
REV.	5			

NOTE:

1. Dimensioning and tolerancing conform to ASME Y14.5-2009.
2. All dimensions are in millimeters.
3. N is the total number of terminals.
4. The location of marked terminal #1 identifier is within the hatched area..
5. NE refers to the maximum number of terminals on E side.
6. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.
7. Coplanarity applies to the terminals and all other bottom surface metallization.

Dual PQFN 5x4 Part Marking

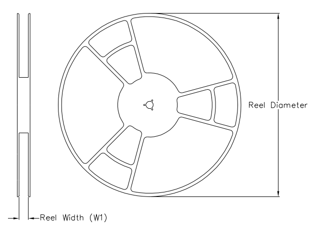


For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: http://www.irf.com/technical-info/appnotes/an-1136.pdf
For more information on package inspection techniques, please refer to application note AN-1154: http://www.irf.com/technical-info/appnotes/an-1154.pdf

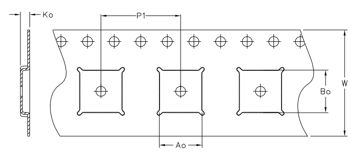
Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Dual PQFN 5x4 Outline Tape and Reel

REEL DIMENSIONS

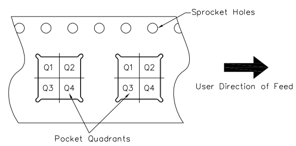


TAPE DIMENSIONS



CODE	DESCRIPTION
Ao	Dimension design to accommodate the component width
Bo	Dimension design to accommodate the component lenght
Ko	Dimension design to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note: All dimension are nominal

Package Type	Reel Diameter (Inch)	QTY	Reel Width W1 (mm)	Ao (mm)	Bo (mm)	Ko (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
5 X 4 PQFN	13	4000	12.4	5.300	4.300	1.20	8.00	12	Q1

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Qualification Information†

Qualification level	Industrial (per JEDEC JESD47F †† guidelines)	
Moisture Sensitivity Level	DUAL PQFN 5mm x 4mm	MSL1 (per JEDEC J-STD-020D††)
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/product-info/reliability

†† Applicable version of JEDEC standard at the time of product release.

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting T_J = 25°C,
Q1: L = 0.13mH, R_G = 50Ω, I_{AS} = 25A;
Q2: L = 1.24mH, R_G = 50Ω, I_{AS} = 25A.

③ Pulse width ≤ 400μs; duty cycle ≤ 2%.

④ R_θ is measured at T_J approximately 90°C.

⑤ When mounted on 1 inch square PCB (FR-4). Please refer to AN-994 for more details: http://www.irf.com/technical-info/appnotes/an-994.pdf

⑥ Calculated continuous current based on maximum allowable junction temperature.

⑦ Current is limited to Q1 = 25A & Q2 = 25A by source bonding technology.

⑧ Pulsed drain current is limited to 100A by source bonding technology.

International Rectifier

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