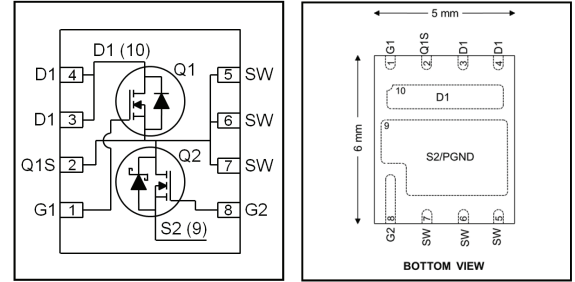


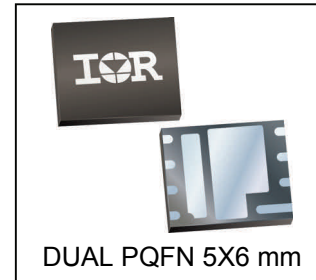
HEXFET® Power MOSFET

| | Q1 | Q2 | |
|--|-----------------|-----------------|----|
| V_{DSS} | 25 | 25 | V |
| $R_{DS(on) max}$ (@ $V_{GS} = 4.5V$) | 4.60 | 1.45 | mΩ |
| Qg (typical) | 10 | 31 | nC |
| I_D (@ $T_C = 25^\circ C$) | 35 [Ⓣ] | 35 [Ⓣ] | A |



Applications

- Control and Synchronous MOSFETs for synchronous buck converters



Features

| |
|---|
| Control and synchronous MOSFETs in one package |
| Low charge control MOSFET (10nC typical) |
| Low $R_{DS(on)}$ synchronous MOSFET (<1.45mΩ) |
| Intrinsic Schottky Diode with Low Forward Voltage on Q2 |
| RoHS Compliant, Halogen-Free |
| MSL1, Industrial Qualification |

results in



Benefits

| |
|----------------------------|
| Increased power density |
| Lower switching losses |
| Lower conduction losses |
| Lower Switching Losses |
| Environmentally friendlier |
| Increased reliability |

| Base part number | Package Type | Standard Pack | | Orderable Part Number |
|------------------|---------------------|---------------|----------|-----------------------|
| | | Form | Quantity | |
| IRFH4253DPbF | Dual PQFN 5mm x 6mm | Tape and Reel | 4000 | IRFH4253DTRPbF |

Absolute Maximum Ratings

| | Parameter | Q1 Max. | Q2 Max. | Units |
|--------------------------|--|-----------------|------------------|-------|
| V_{GS} | Gate-to-Source Voltage | ± 20 | | V |
| $I_D @ T_C = 25^\circ C$ | Continuous Drain Current, $V_{GS} @ 4.5V$ | 64 [Ⓣ] | 145 [Ⓣ] | A |
| $I_D @ T_C = 70^\circ C$ | Continuous Drain Current, $V_{GS} @ 4.5V$ | 51 [Ⓣ] | 116 [Ⓣ] | |
| $I_D @ T_C = 25^\circ C$ | Continuous Drain Current, $V_{GS} @ 4.5V$ (Source Bonding Technology Limited) | 35 [Ⓣ] | 35 [Ⓣ] | |
| I_{DM} | Pulsed Drain Current | 120 | 580 [Ⓢ] | |
| $P_D @ T_C = 25^\circ C$ | Power Dissipation | 31 | 50 | W |
| $P_D @ T_C = 70^\circ C$ | Power Dissipation | 20 | 32 | |
| | Linear Derating Factor | 0.25 | 0.40 | W/°C |
| T_J T_{STG} | Operating Junction and Storage Temperature Range | -55 to + 150 | | °C |

Thermal Resistance

| | Parameter | Q1 Max. | Q2 Max. | Units |
|--------------------------|----------------------------------|---------|---------|-------|
| $R_{\theta JC}$ (Bottom) | Junction-to-Case ^④ | 4.0 | 2.5 | °C/W |
| $R_{\theta JC}$ (Top) | Junction-to-Case ^④ | 20 | 13 | |
| $R_{\theta JA}$ | Junction-to-Ambient ^⑤ | 34 | 38 | |
| $R_{\theta JA} (<10s)$ | Junction-to-Ambient ^⑤ | 24 | 24 | |

Notes ^① through ^⑧ are on page 12

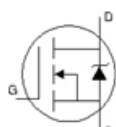
Static @ T_J = 25°C (unless otherwise specified)

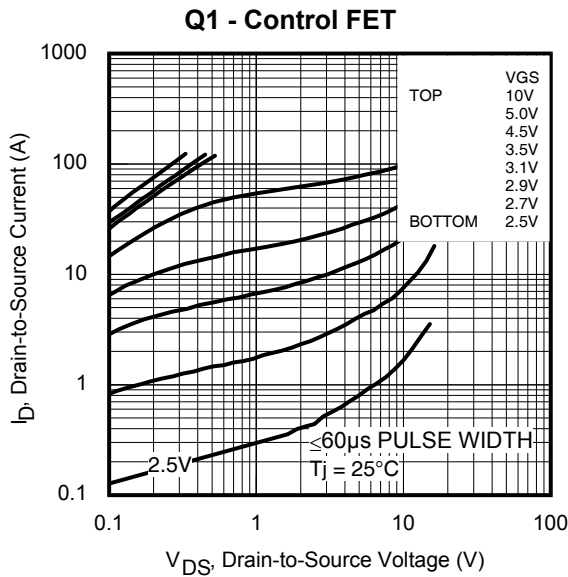
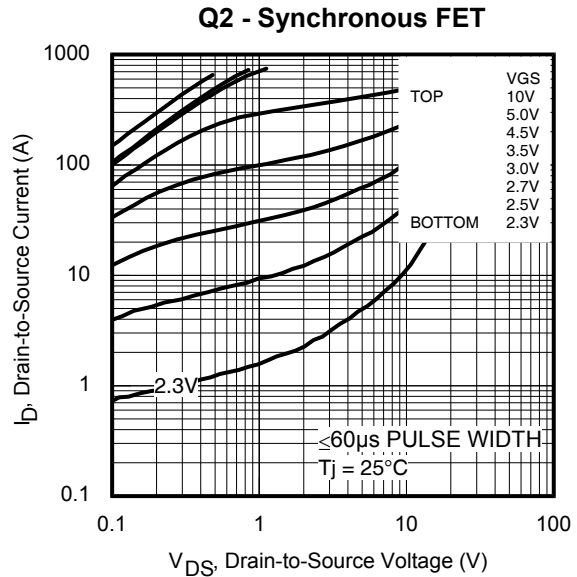
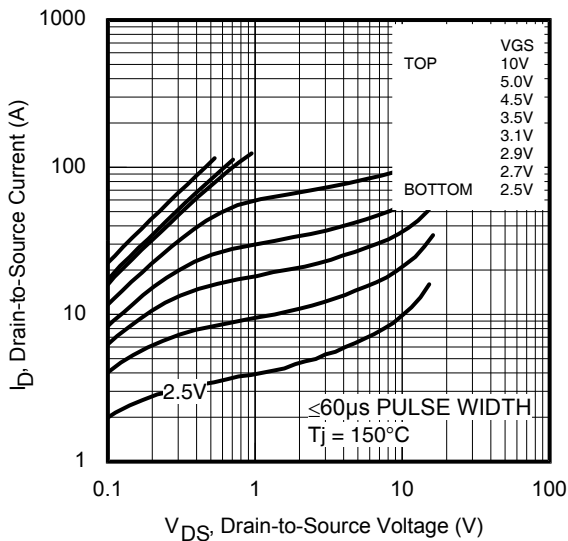
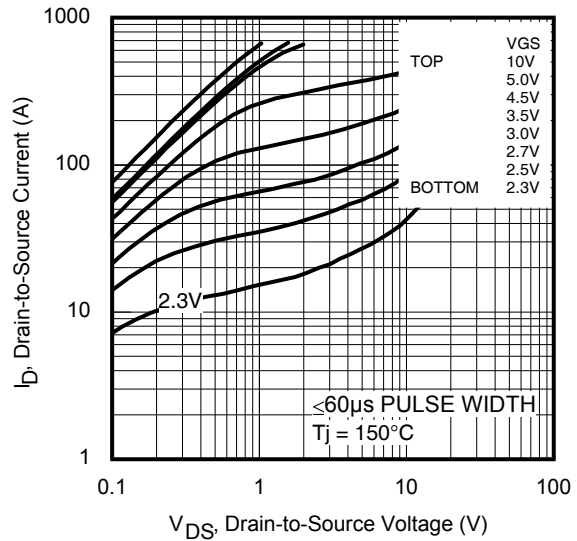
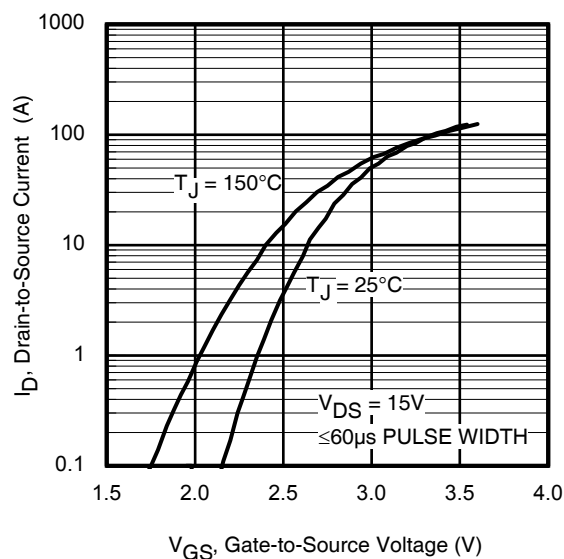
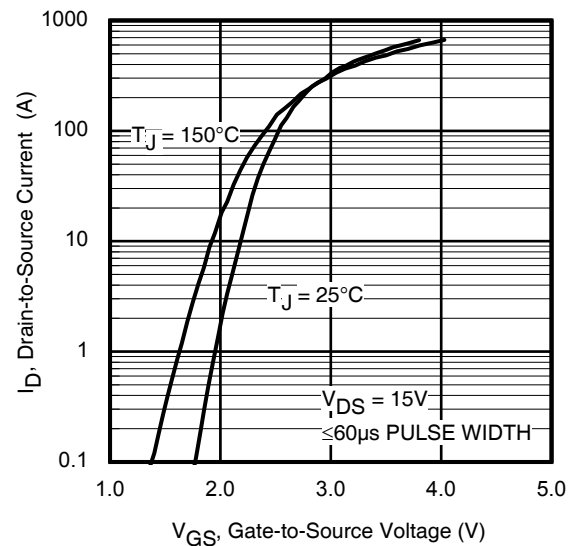
| | Parameter | | Min. | Typ. | Max. | Units | Conditions | | |
|---------------------------------------|---|-------|------|------|------|-------|--|----|---|
| BV _{DSS} | Drain-to-Source Breakdown Voltage | Q1 | 25 | — | — | V | V _{GS} = 0V, I _D = 250μA | | |
| | | Q2 | 25 | — | — | | V _{GS} = 0V, I _D = 1.0mA | | |
| ΔBV _{DSS} /ΔT _J | Breakdown Voltage Temp. Coefficient | Q1 | — | 22 | — | mV/°C | Reference to 25°C, I _D = 1.0mA | | |
| | | Q2 | — | 22 | — | | Reference to 25°C, I _D = 10mA | | |
| R _{DS(on)} | Static Drain-to-Source On-Resistance | Q1 | — | 2.50 | 3.20 | mΩ | V _{GS} = 10V, I _D = 30A ③ | | |
| | | Q2 | — | 0.90 | 1.10 | | V _{GS} = 10V, I _D = 30A ③ | | |
| | | Q1 | — | 3.70 | 4.60 | | V _{GS} = 4.5V, I _D = 30A ③ | | |
| | | Q2 | — | 1.15 | 1.45 | | V _{GS} = 4.5V, I _D = 30A ③ | | |
| V _{GS(th)} | Gate Threshold Voltage | Q1 | 1.1 | 1.6 | 2.1 | V | Q1: V _{DS} = V _{GS} , I _D = 35μA | | |
| | | Q2 | 1.1 | 1.6 | 2.1 | | Q2: V _{DS} = V _{GS} , I _D = 100μA | | |
| ΔV _{GS(th)} /ΔT _J | Gate Threshold Voltage Coefficient | Q1 | — | -5.7 | — | mV/°C | Q1: V _{DS} = V _{GS} , I _D = 35μA | | |
| | | Q2 | — | -8.9 | — | | Q2: V _{DS} = V _{GS} , I _D = 100μA | | |
| I _{DSS} | Drain-to-Source Leakage Current | Q1 | — | — | 1.0 | μA | V _{DS} = 20V, V _{GS} = 0V | | |
| | | Q2 | — | — | 250 | | V _{DS} = 20V, V _{GS} = 0V | | |
| I _{GSS} | Gate-to-Source Forward Leakage | Q1/Q2 | — | — | 100 | nA | V _{GS} = 20V | | |
| | Gate-to-Source Reverse Leakage | Q1/Q2 | — | — | -100 | | V _{GS} = -20V | | |
| g _{fs} | Forward Transconductance | Q1 | 131 | — | — | S | V _{DS} = 10V, I _D = 30A | | |
| | | Q2 | 164 | — | — | | V _{DS} = 10V, I _D = 30A | | |
| Q _g | Total Gate Charge | Q1 | — | 10 | 15 | nC | Q1 V _{DS} = 13V V _{GS} = 4.5V, I _D = 30A Q2 V _{DS} = 13V V _{GS} = 4.5V, I _D = 30A | | |
| | | Q2 | — | 31 | 47 | | | | |
| Q _{gs1} | Pre-V _{th} Gate-to-Source Charge | Q1 | — | 2.5 | — | | | | |
| | | Q2 | — | 4.9 | — | | | | |
| Q _{gs2} | Post-V _{th} Gate-to-Source Charge | Q1 | — | 1.6 | — | | | | |
| | | Q2 | — | 5.4 | — | | | | |
| Q _{gd} | Gate-to-Drain Charge | Q1 | — | 3.8 | — | | | | |
| | | Q2 | — | 12 | — | | | | |
| Q _{godr} | Gate Charge Overdrive | Q1 | — | 2.1 | — | | | | |
| | | Q2 | — | 8.7 | — | | | | |
| Q _{sw} | Switch Charge (Q _{gs2} + Q _{gd}) | Q1 | — | 5.4 | — | | | | |
| | | Q2 | — | 17.4 | — | | | | |
| Q _{oss} | Output Charge | Q1 | — | 10 | — | nC | V _{DS} = 16V, V _{GS} = 0V | | |
| | | Q2 | — | 31 | — | | | | |
| R _G | Gate Resistance | Q1 | — | 2.4 | — | Ω | | | |
| | | Q2 | — | 1.1 | — | | | | |
| t _{d(on)} | Turn-On Delay Time | Q1 | — | 10 | — | ns | Q1 V _{DS} = 13V V _{GS} = 4.5V I _D = 30A, R _G = 1.8Ω Q2 V _{DS} = 13V V _{GS} = 4.5V I _D = 30A, R _G = 1.8Ω | | |
| | | Q2 | — | 16 | — | | | | |
| t _r | Rise Time | Q1 | — | 61 | — | | | | |
| | | Q2 | — | 98 | — | | | | |
| t _{d(off)} | Turn-Off Delay Time | Q1 | — | 13 | — | | | | |
| | | Q2 | — | 26 | — | | | | |
| t _f | Fall Time | Q1 | — | 15 | — | | | | |
| | | Q2 | — | 65 | — | | | | |
| C _{iss} | Input Capacitance | Q1 | — | 1314 | — | | | pF | V _{GS} = 0V V _{DS} = 13V f = 1.0MHz |
| | | Q2 | — | 3756 | — | | | | |
| C _{oss} | Output Capacitance | Q1 | — | 365 | — | | | | |
| | | Q2 | — | 1205 | — | | | | |
| C _{rss} | Reverse Transfer Capacitance | Q1 | — | 92 | — | | | | |
| | | Q2 | — | 286 | — | | | | |

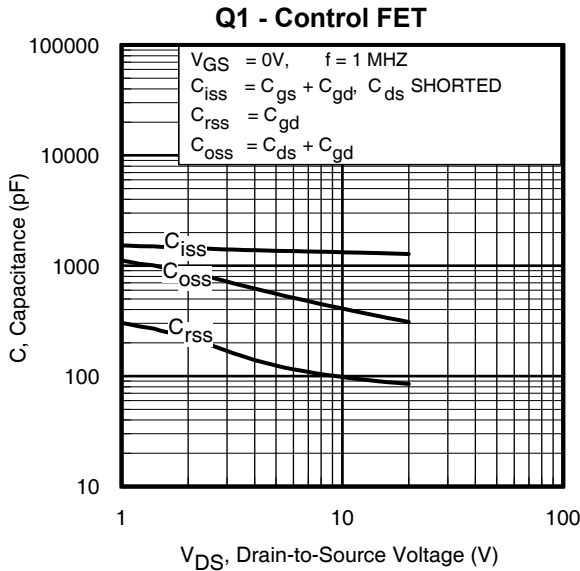
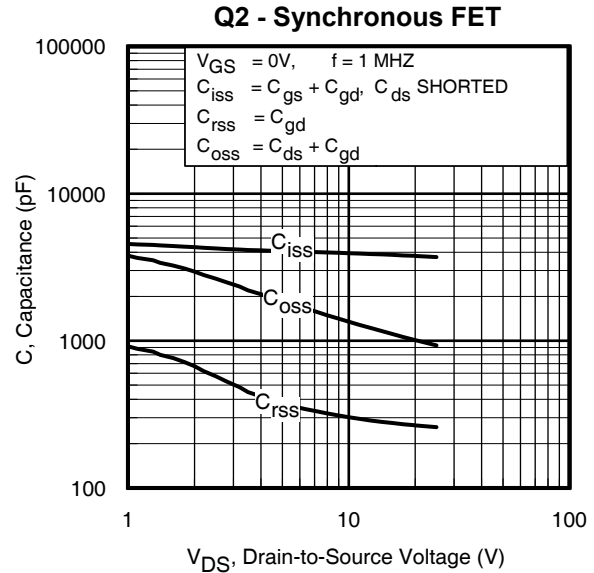
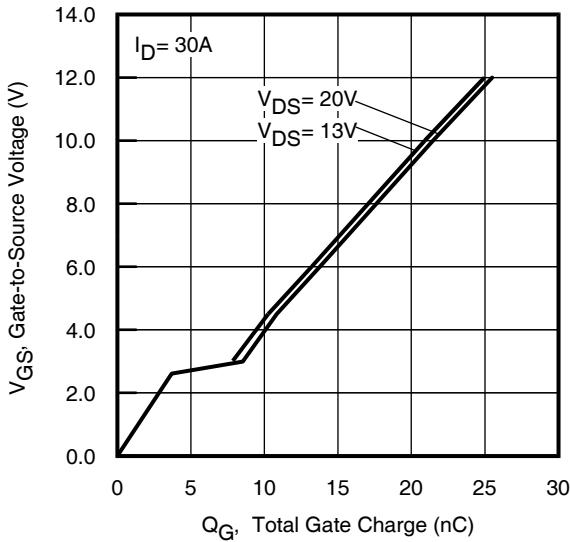
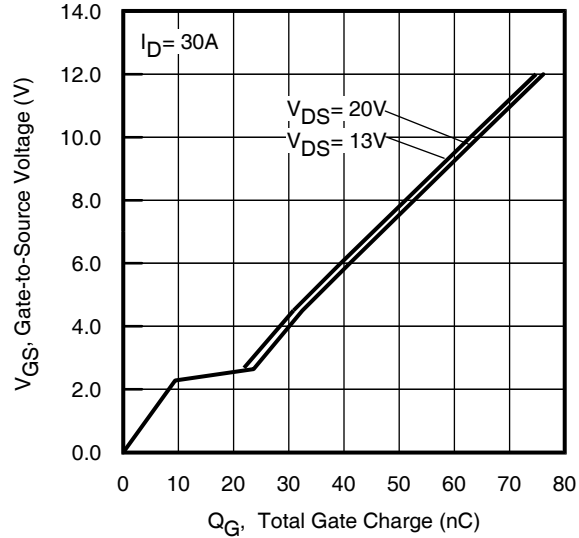
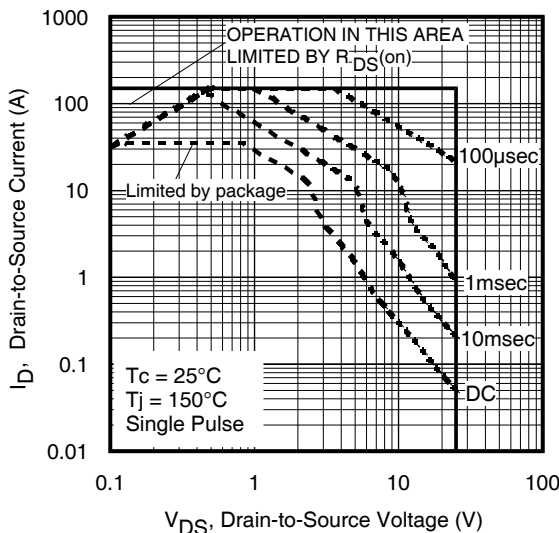
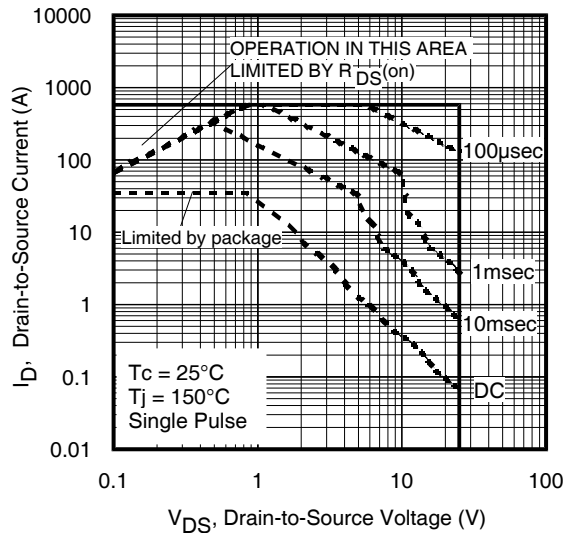
Avalanche Characteristics

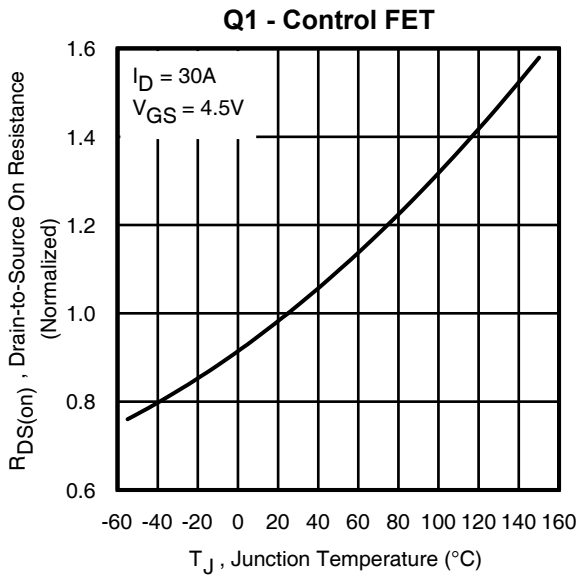
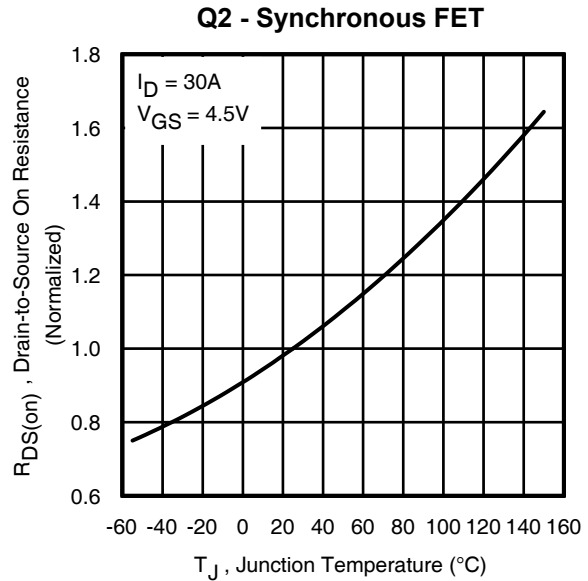
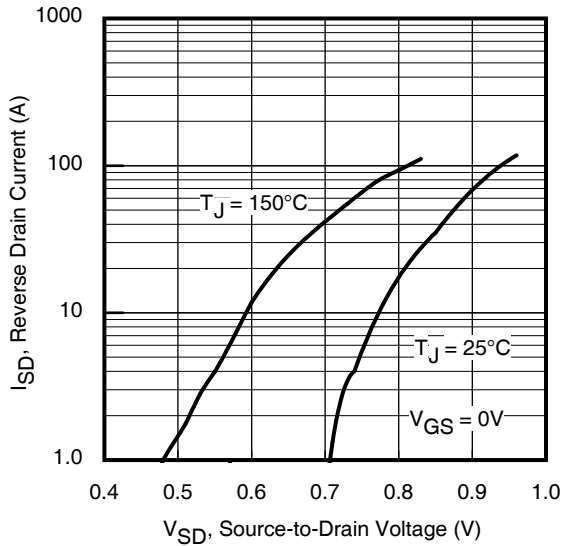
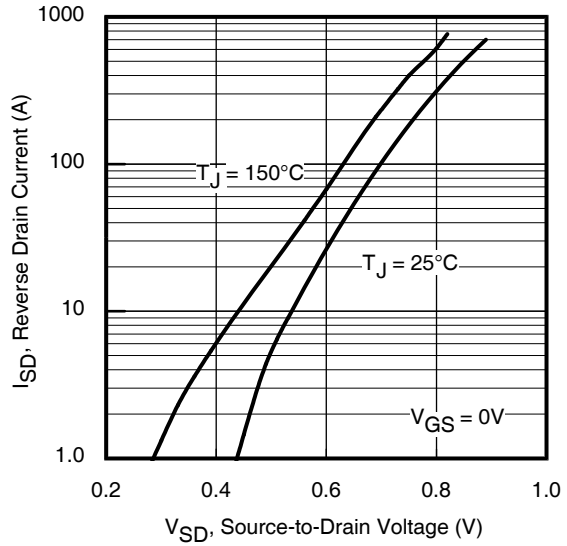
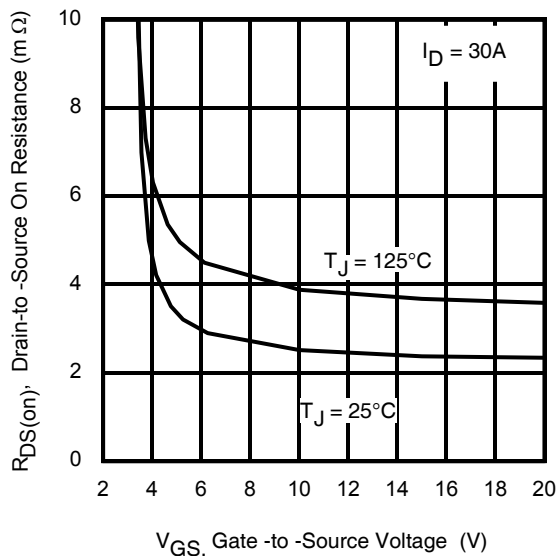
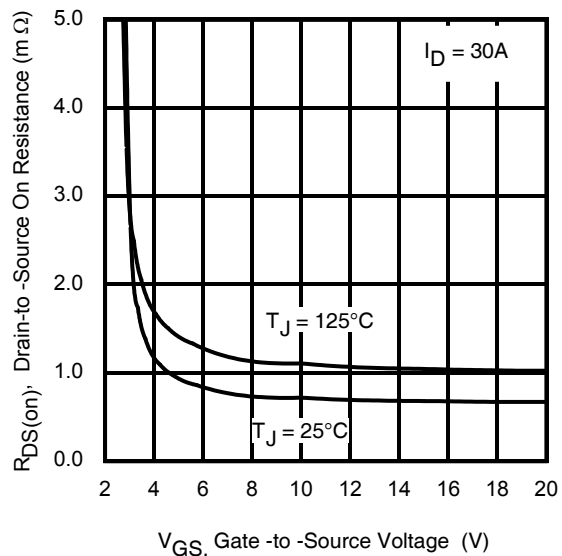
| | Parameter | Typ. | Q1 Max. | Q2 Max. | Units |
|----------|---------------------------------|------|---------|---------|-------|
| E_{AS} | Single Pulse Avalanche Energy ② | — | 61 | 568 | mJ |
| I_{AR} | Avalanche Current ① | — | 30 | 60 | A |

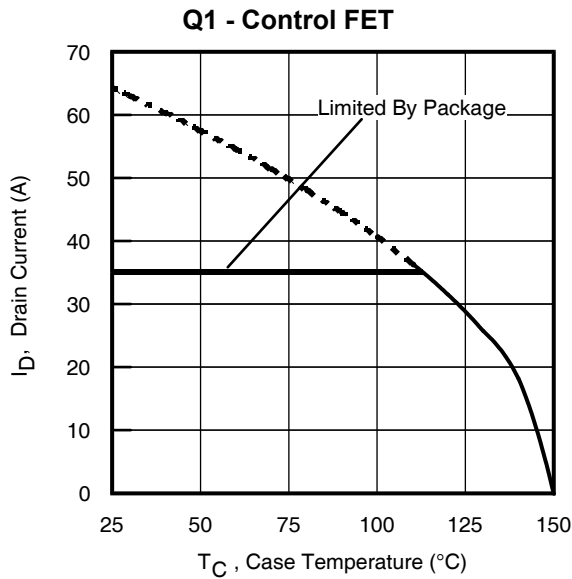
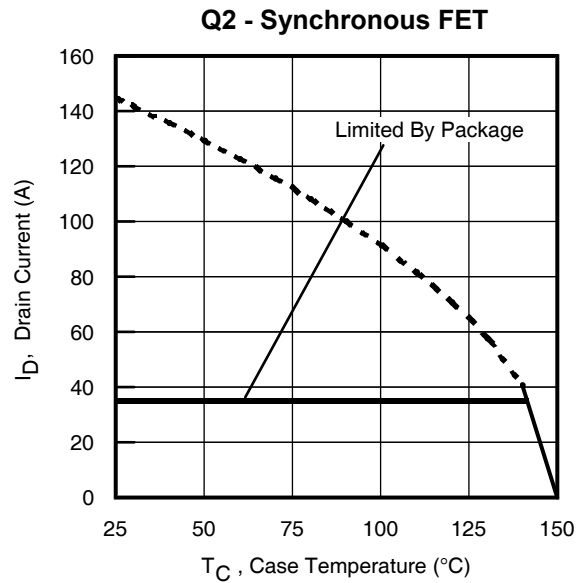
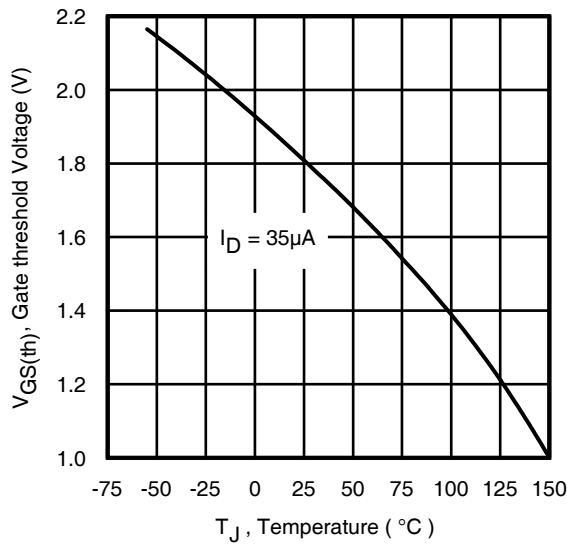
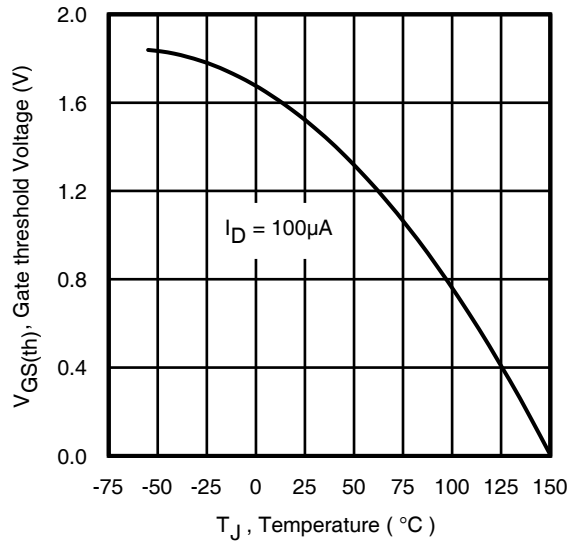
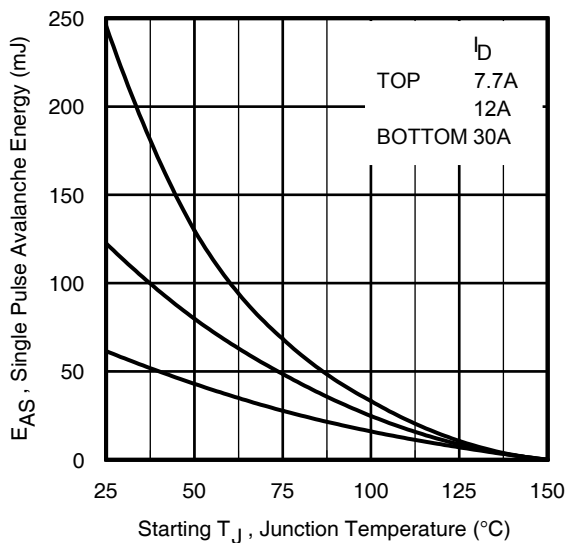
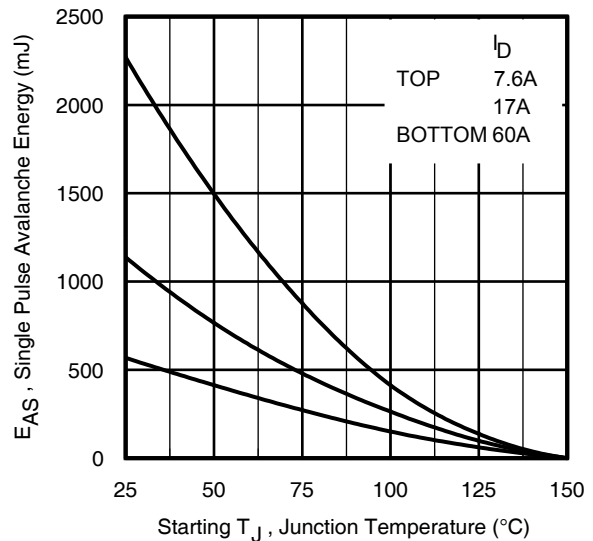
Diode Characteristics

| | Parameter | | Min. | Typ. | Max. | Units | Conditions |
|----------|--|----|------|------|------|-------|--|
| I_S | Continuous Source Current (Body Diode) | Q1 | — | — | 35⑦ | A | MOSFET symbol showing the integral reverse p-n junction diode.  |
| | | Q2 | — | — | 35⑦ | | |
| I_{SM} | Pulsed Source Current (Body Diode) | Q1 | — | — | 120 | A | |
| | | Q2 | — | — | 580⑧ | | |
| V_{SD} | Diode Forward Voltage | Q1 | — | — | 1.0 | V | $T_J = 25^\circ\text{C}$, $I_S = 30\text{A}$, $V_{GS} = 0\text{V}$ ③ |
| | | Q2 | — | — | 0.75 | | $T_J = 25^\circ\text{C}$, $I_S = 30\text{A}$, $V_{GS} = 0\text{V}$ ③ |
| t_{rr} | Reverse Recovery Time | Q1 | — | 16 | — | ns | $Q1$ $T_J = 25^\circ\text{C}$, $I_F = 30\text{A}$ $V_{DD} = 13\text{V}$, $di/dt = 235\text{A}/\mu\text{s}$ ③ |
| | | Q2 | — | 29 | — | | |
| Q_{rr} | Reverse Recovery Charge | Q1 | — | 13 | — | nC | $Q2$ $T_J = 25^\circ\text{C}$, $I_F = 30\text{A}$ $V_{DD} = 13\text{V}$, $di/dt = 250\text{A}/\mu\text{s}$ ③ |
| | | Q2 | — | 41 | — | | |


Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Output Characteristics

Fig 4. Typical Output Characteristics

Fig 5. Typical Transfer Characteristics

Fig 6. Typical Transfer Characteristics


Fig 7. Typical Capacitance vs. Drain-to-Source Voltage

Fig 8. Typical Capacitance vs. Drain-to-Source Voltage

Fig 9. Typical Gate Charge vs. Gate-to-Source Voltage

Fig 10. Typical Gate Charge vs. Gate-to-Source Voltage

Fig 11. Maximum Safe Operating Area

Fig 12. Maximum Safe Operating Area


Fig 13. Normalized On-Resistance vs. Temperature

Fig 14. Normalized On-Resistance vs. Temperature

Fig 15. Typical Source-Drain Diode Forward Voltage

Fig 16. Typical Source-Drain Diode Forward Voltage

Fig 17. Typical On-Resistance vs. Gate Voltage

Fig 18. Typical On-Resistance vs. Gate Voltage


Fig 19. Maximum Drain Current vs. Case Temperature

Fig 20. Maximum Drain Current vs. Case Temperature

Fig 21. Threshold Voltage vs. Temperature

Fig 22. Threshold Voltage vs. Temperature

Fig 23. Maximum Avalanche Energy vs. Drain Current

Fig 24. Maximum Avalanche Energy vs. Drain Current

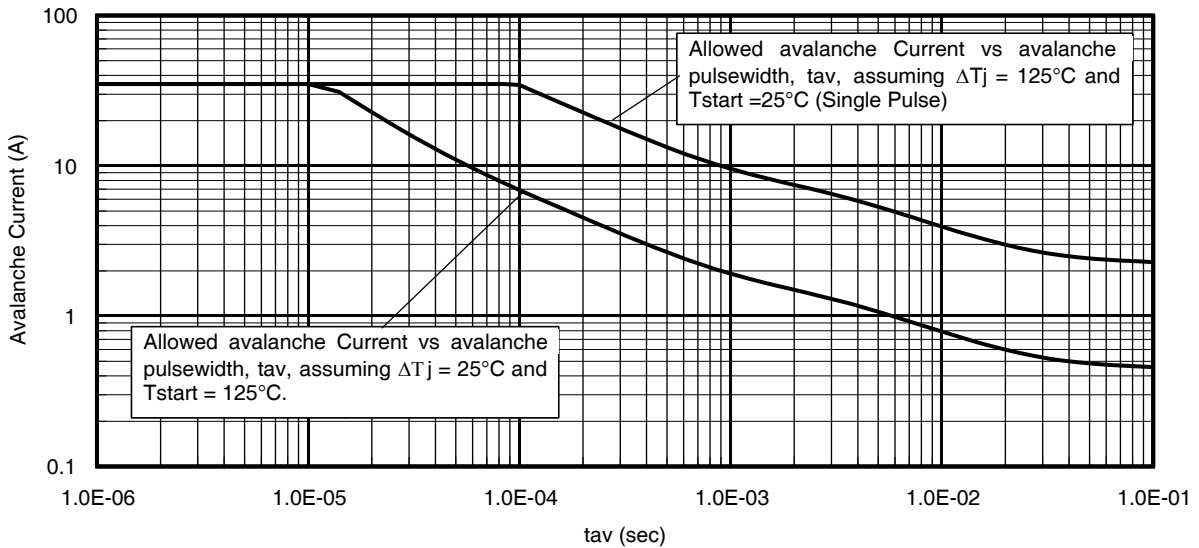


Fig 25. Max Avalanche Current vs. Pulse Width (Q1)

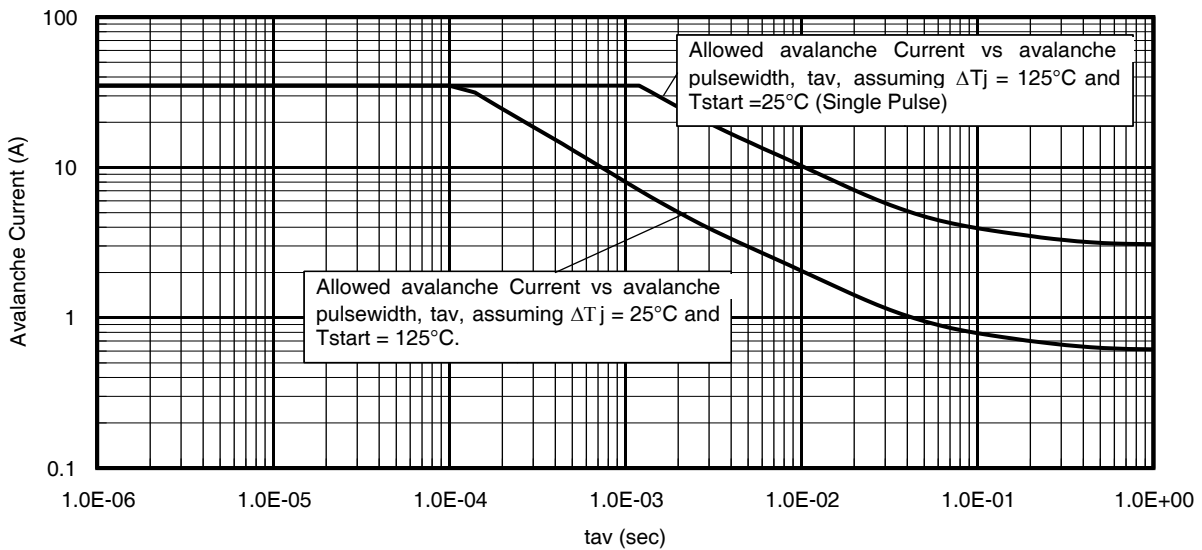


Fig 26. Max Avalanche Current vs. Pulse Width (Q2)

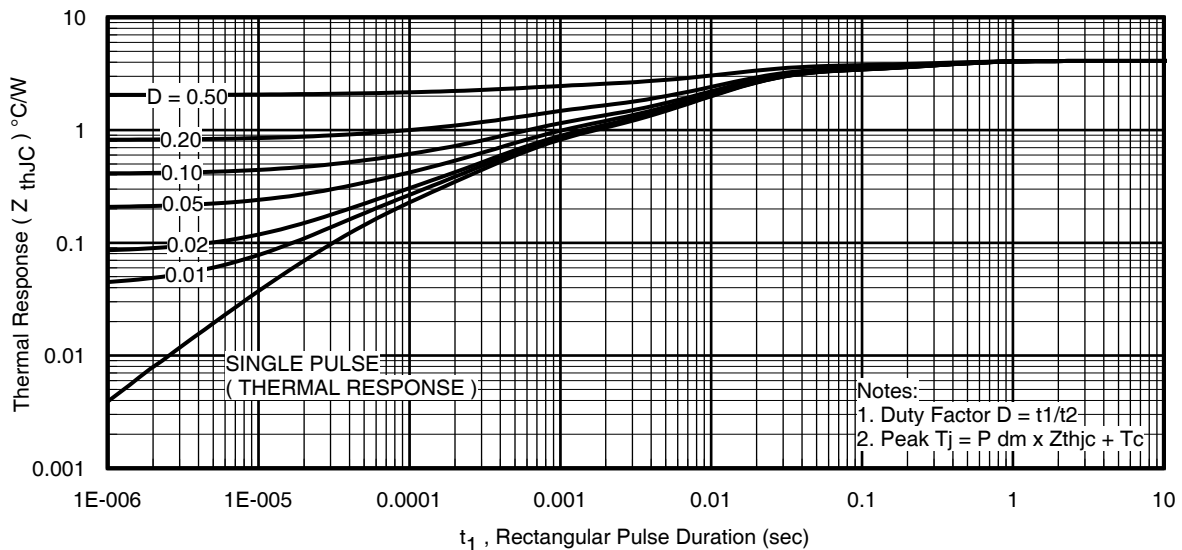


Fig 27. Maximum Effective Transient Thermal Impedance, Junction-to-Case (Q1)

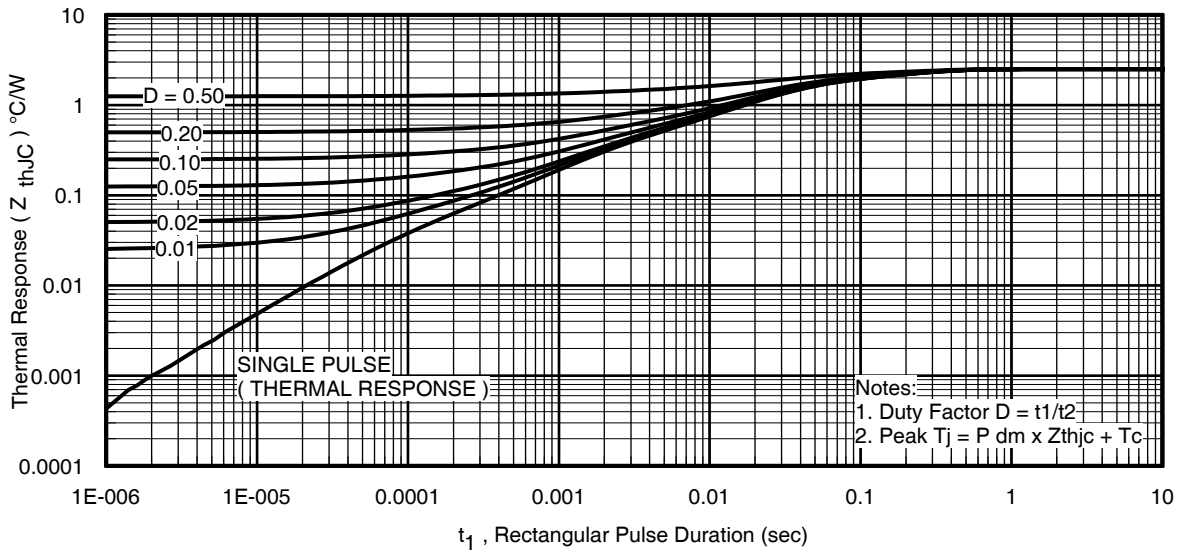
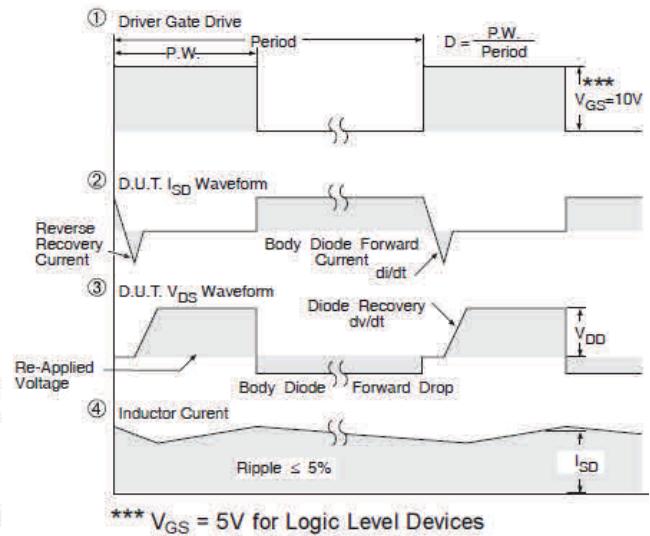
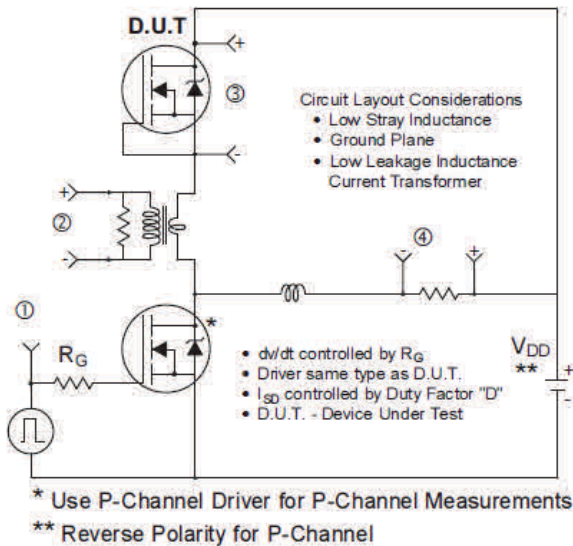
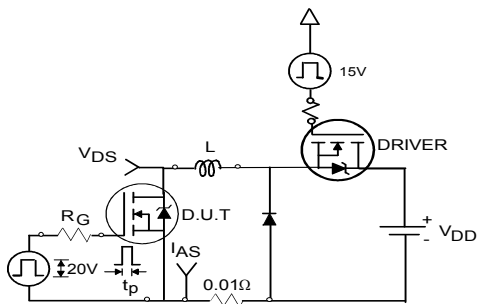
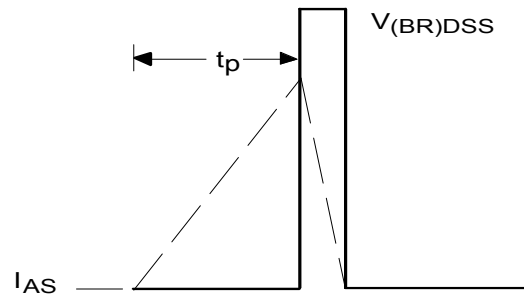
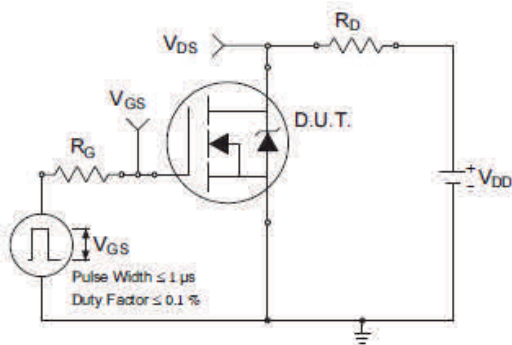
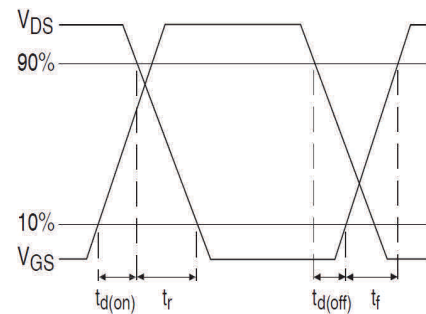
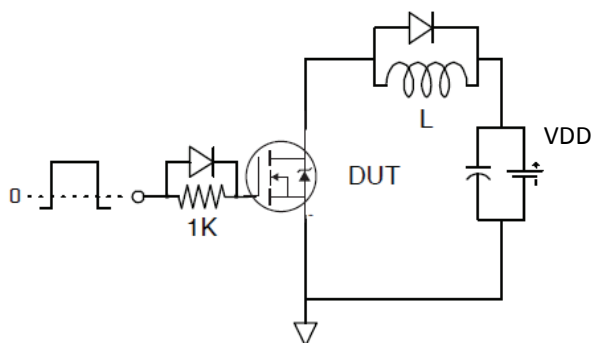
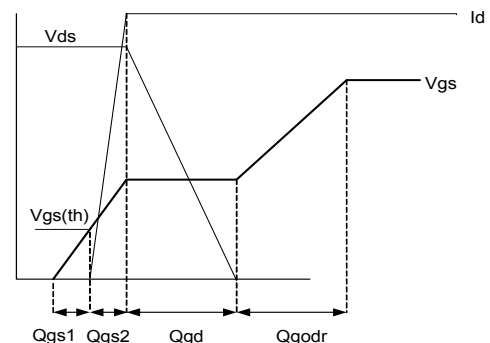
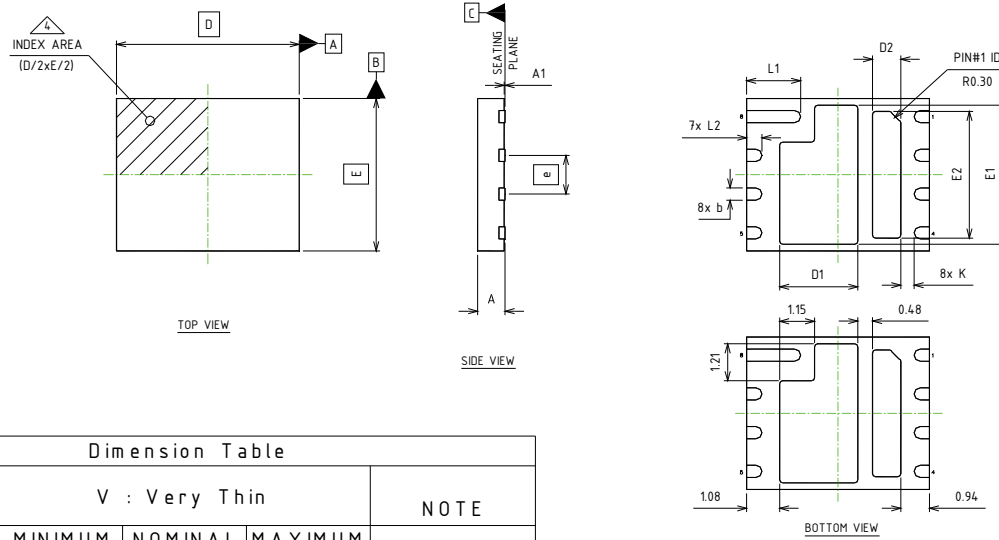


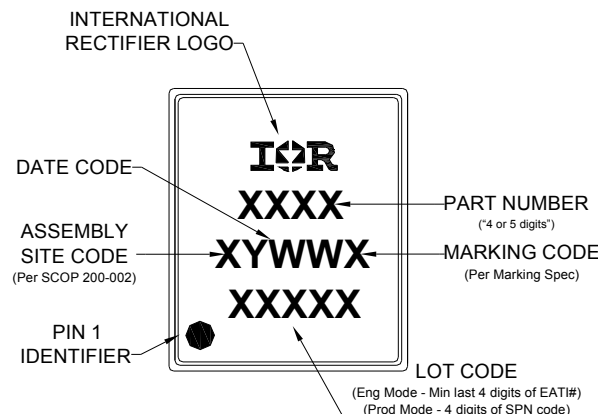
Fig 28. Maximum Effective Transient Thermal Impedance, Junction-to-Case (Q2)


Fig 29. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

Fig 30a. Unclamped Inductive Test Circuit

Fig 30b. Unclamped Inductive Waveforms

Fig 31a. Switching Time Test Circuit

Fig 31b. Switching Time Waveforms

Fig 32a. Gate Charge Test Circuit

Fig 32b. Gate Charge Waveform

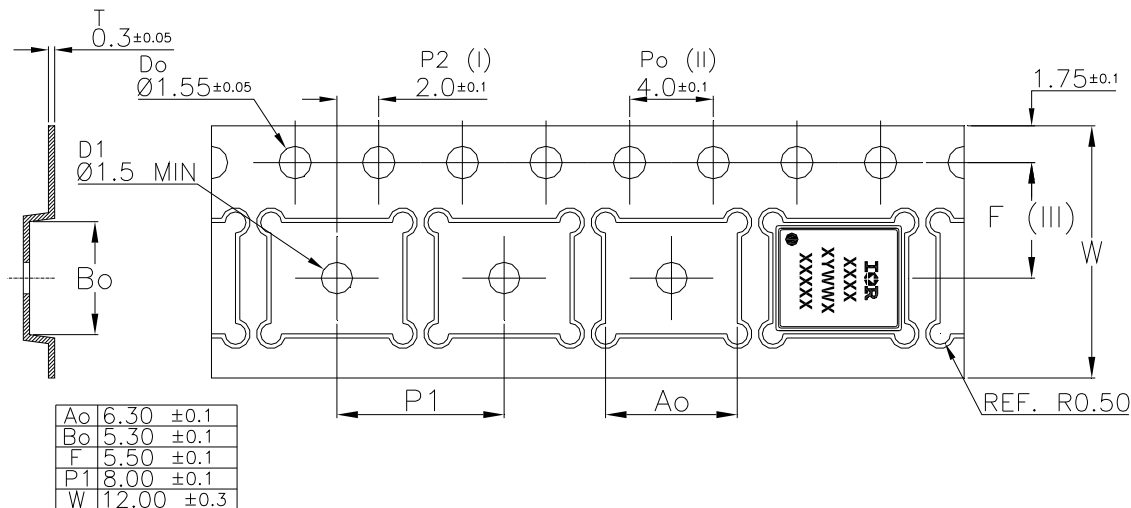
Dual PQFN 5x6 Outline "H" Package Details


| Dimension Table | | | | NOTE |
|---------------------|---------------|---------|---------|------|
| Thickness Symbol | V : Very Thin | | | |
| | MINIMUM | NOMINAL | MAXIMUM | |
| A | 0.80 | 0.90 | 1.00 | |
| A1 | 0.00 | 0.02 | 0.05 | |
| b | 0.30 | 0.40 | 0.50 | 6 |
| D | 6.00 BSC | | | |
| E | 5.00 BSC | | | |
| e | 1.27 BSC | | | |
| D1 | 2.42 | 2.57 | 2.67 | |
| E1 | 4.41 | 4.56 | 4.66 | |
| D2 | 0.78 | 0.93 | 1.03 | |
| E2 | 4.01 | 4.16 | 4.26 | |
| K | 0.20 | --- | --- | |
| L1 | 1.67 | 1.77 | 1.87 | |
| L2 | 0.40 | 0.50 | 0.60 | |

For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: <http://www.irf.com/technical-info/appnotes/an-1136.pdf>
 For more information on package inspection techniques, please refer to application note AN-1154: <http://www.irf.com/technical-info/appnotes/an-1154.pdf>

PQFN 5x6 Outline "H" Part Marking


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Dual PQFN 5x6 Outline Tape and Reel


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification Information[†]

| | | |
|-----------------------------------|---|---|
| Qualification level | Industrial (per JEDEC JESD47F ^{††} guidelines) | |
| Moisture Sensitivity Level | DUAL PQFN 5mm x 6mm | MSL1 (per JEDEC J-STD-020D ^{††}) |
| RoHS Compliant | Yes | |

[†] Qualification standards can be found at International Rectifier's web site <http://www.irf.com/product-info/reliability>

^{††} Applicable version of JEDEC standard at the time of product release.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_j = 25^\circ\text{C}$,
Q1: $L = 0.14\text{mH}$, $R_G = 50\Omega$, $I_{AS} = 30\text{A}$;
Q2: $L = 0.32\text{mH}$, $R_G = 50\Omega$, $I_{AS} = 60\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ R_θ is measured at T_j approximately 90°C .
- ⑤ When mounted on 1 inch square PCB (FR-4). Please refer to AN-994 for more details:
<http://www.irf.com/technical-info/appnotes/an-994.pdf>
- ⑥ Calculated continuous current based on maximum allowable junction temperature.
- ⑦ Current is limited to Q1 = 35A & Q2 = 35A by source bonding technology.
- ⑧ Pulsed drain current is limited to 140A by source bonding technology.

Revision History

| Date | Comments |
|------------|---|
| 08/06/2013 | <ul style="list-style-type: none"> • Added the Fast/RFET logo, on page 1. • Changed the package limitation current from 45A to 35A, on page 1. • Added the part marking drawing, on page 11. |
| 01/16/2014 | <ul style="list-style-type: none"> • Updated the MSL level from MSL2 to MSL1, on page 1 & 12. |
| 05/21/2014 | <ul style="list-style-type: none"> • Updated fig. 25 to show the max avalanche plateau at 35A, on page 8. • Corrected fig. 26 to cap the curves at package limitation current of 35A, on page 8. |

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